EXPERIMENT NO.4

1) VHDL CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL; use IEEE.STD_LOGIC_arith.ALL;

entity FIFO_4bit is
Port ( clk,rst : in  STD_LOGIC; enr,enw : in  STD_LOGIC;
datain : in  STD_LOGIC_VECTOR (3 downto 0); dataout : out  STD_LOGIC_VECTOR (3
downto 0); full,empty : out  STD_LOGIC);
end FIFO_4bit;

architecture Behavioral of FIFO_4bit is

type memory_type is array (0 to 7) of std_logic_vector(3 downto 0); signal memory :

memory_type;

signal readptr,writeptr : std_logic_vector(3 downto 0):="0000";

--signal cnt:std_logic_vector(24 downto 0);

--signal clk1:std_logic;
begin

FIFO_Process:  process(clk)
begin
if(clk'event and clk='1' and enw ='1' and enr='0') then --WRITEOPERATION
memory(conv_integer(writeptr)) <= datain; writeptr <= writeptr + '1';
end if;

if(clk'event and clk='1' and enr ='1' and enw='0') then  --READ
OPERATION
dataout <= memory(conv_integer(readptr));

readptr <= readptr + '1';
end if;
if(readptr = "1000") then
empty<='1';
else
empty<='0';
end if;
if(writeptr = "1000") then
full <='1';
else
```

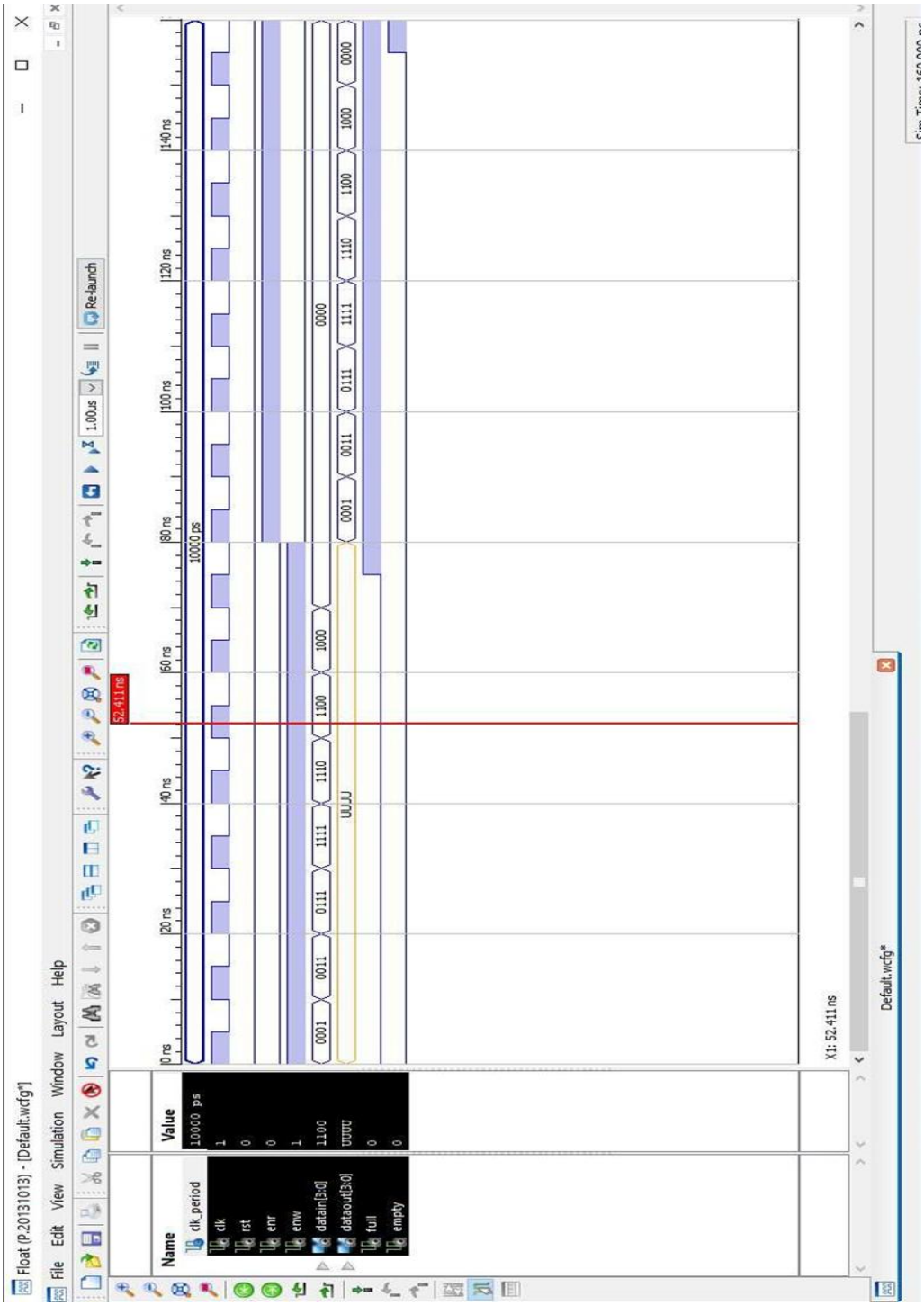
```
full <='0';
            end if; end process;
end Behavioral
```

2) VHDL TESTBENCH:

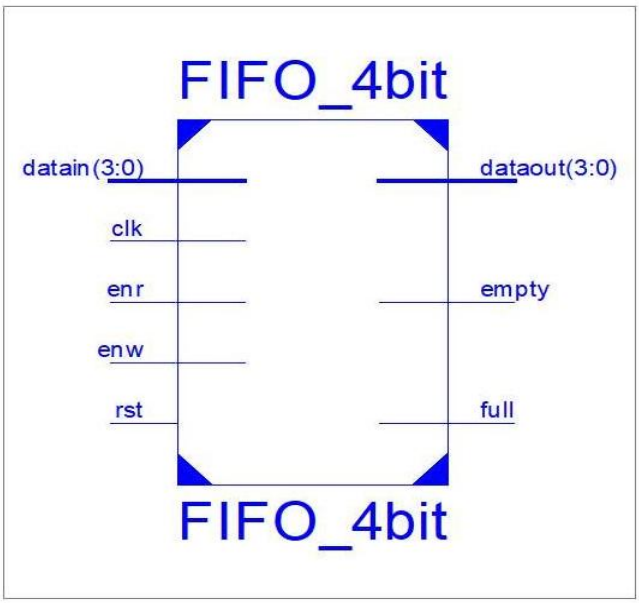
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY test1 IS END test1;

ARCHITECTURE behavior OF test1 IS
-- Component Declaration for the Unit Under Test (UUT) COMPONENT FIFO_4bit
PORT(
clk : IN std_logic; rst : IN std_logic; enr : IN std_logic; enw : IN std_logic;
datain : IN std_logic_vector(3 downto 0); dataout : OUT std_logic_vector(3 downto 0);
full : OUT std_logic;
empty : OUT std_logic
);
END COMPONENT;


--Inputs
signal clk : std_logic := '0'; signal rst : std_logic := '0'; signal enr : std_logic := '0'; signal
enw : std_logic := '0';
signal datain : std_logic_vector(3 downto 0) := (others => '0');

--Outputs
signal dataout : std_logic_vector(3 downto 0); signal full : std_logic;
signal empty : std_logic;

-- Clock period definitions
constant clk_period : time := 10 ns; BEGIN
-- Instantiate the Unit Under Test (UUT) uut: FIFO_4bit PORT MAP (
clk => clk, rst => rst, enr => enr,
enw => enw, datain => datain,
dataout => dataout, full => full,
empty => empty
);
```

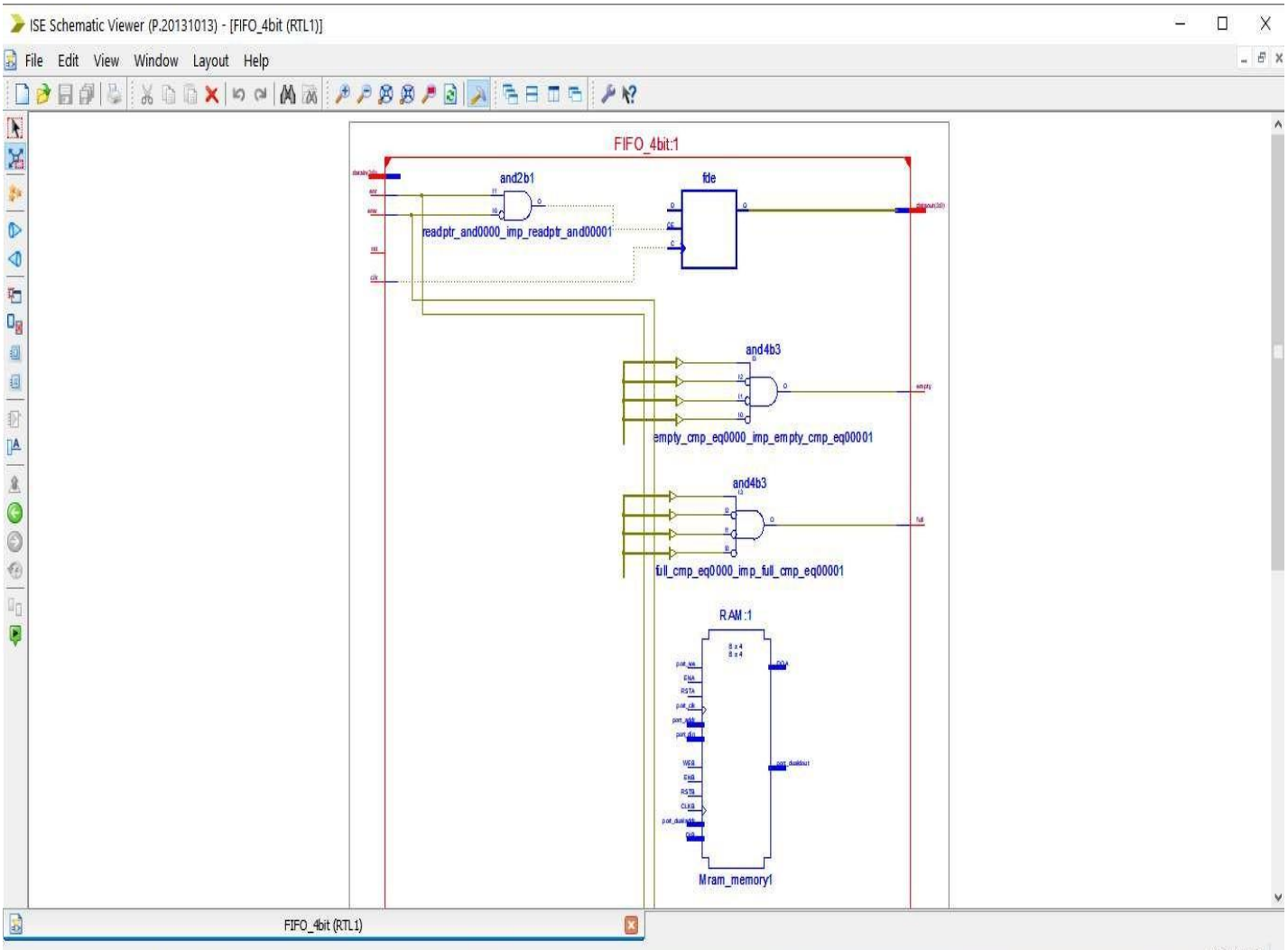
```
-- Clock process definitions clk_process :process
begin

end process;

clk <= '1'; wait for 5 ns; clk <= '0'; wait for 5 ns;
-- Stimulus process stim_proc: process begin
enw<='1';
enr<='0'; datain<="0001"; wait for 10ns;

datain<="0011"; wait for 10ns;

datain<="0111"; wait for 10ns;

datain<="1111"; wait for 10ns;

datain<="1110"; wait for 10ns;

datain<="1100"; wait for 10ns;

datain<="1000"; wait for 10ns;

datain<="0000"; wait for 10ns;

enw<='0';
enr<='1';
wait for 80ns;
end process; END;
```

3) SIMULATION RESULT



4) SCHEMATICS (RTL Technology)





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* Final Report *

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Final Results

RTL Top Level Output File Name : ALU_4bit.ngr

Top Level Output File Name : ALU_4bit

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

IOs : 15

Cell Usage :

BELS : 30

INV : 1

LUT2 : 2

LUT3 : 2

LUT4 : 18

MUXF5 : 7

IO Buffers : 15

IBUF : 11

OBUF : 4

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Device utilization summary:

Selected Device : 3s250epq208-5

```
 Number of Slices:                       13  out of   2448     0%
 Number of 4 input LUTs:                 23  out of   4896     0%
 Number of IOs:                          15
 Number of bonded IOBs:                  15  out of    158     9%
```

Partition Resource Summary:

No Partitions were found in this design.

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