Experiment 1

Name: Siddhesh Sonavane

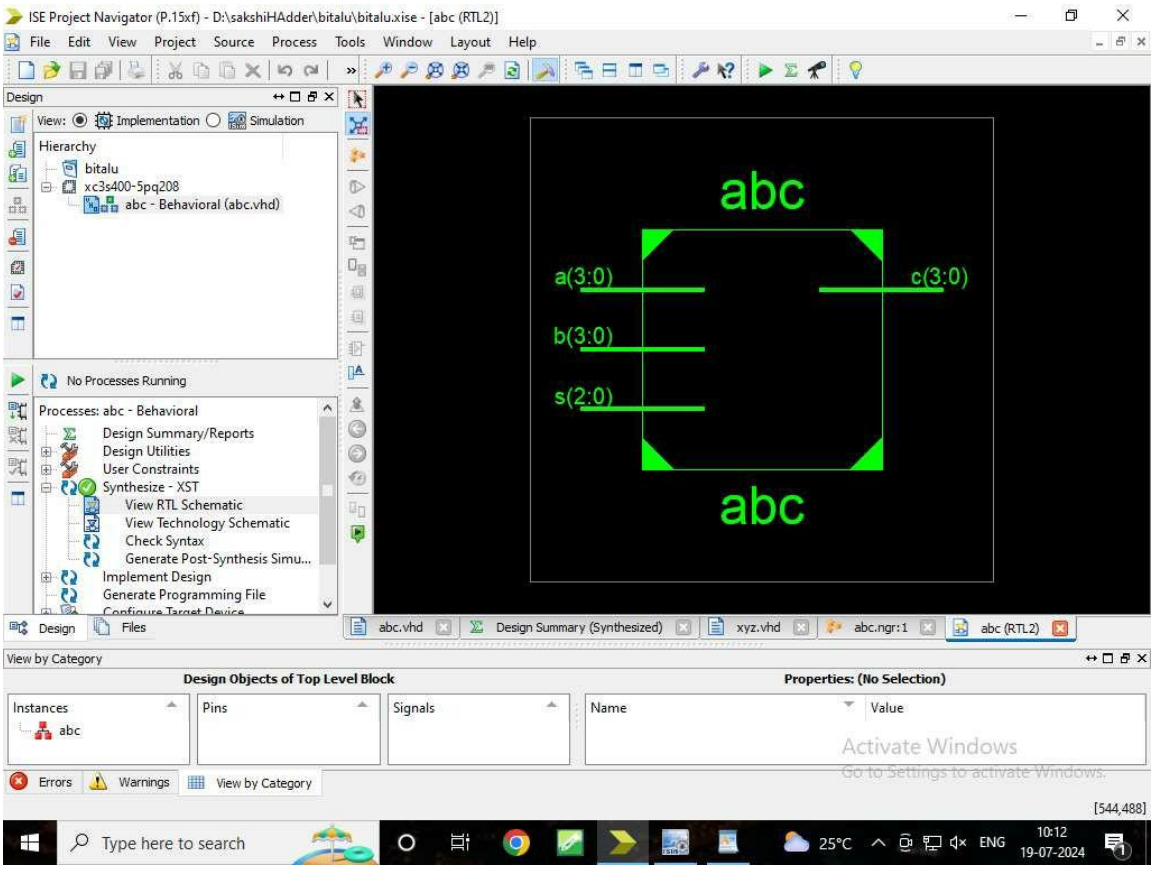
Roll no: E42007

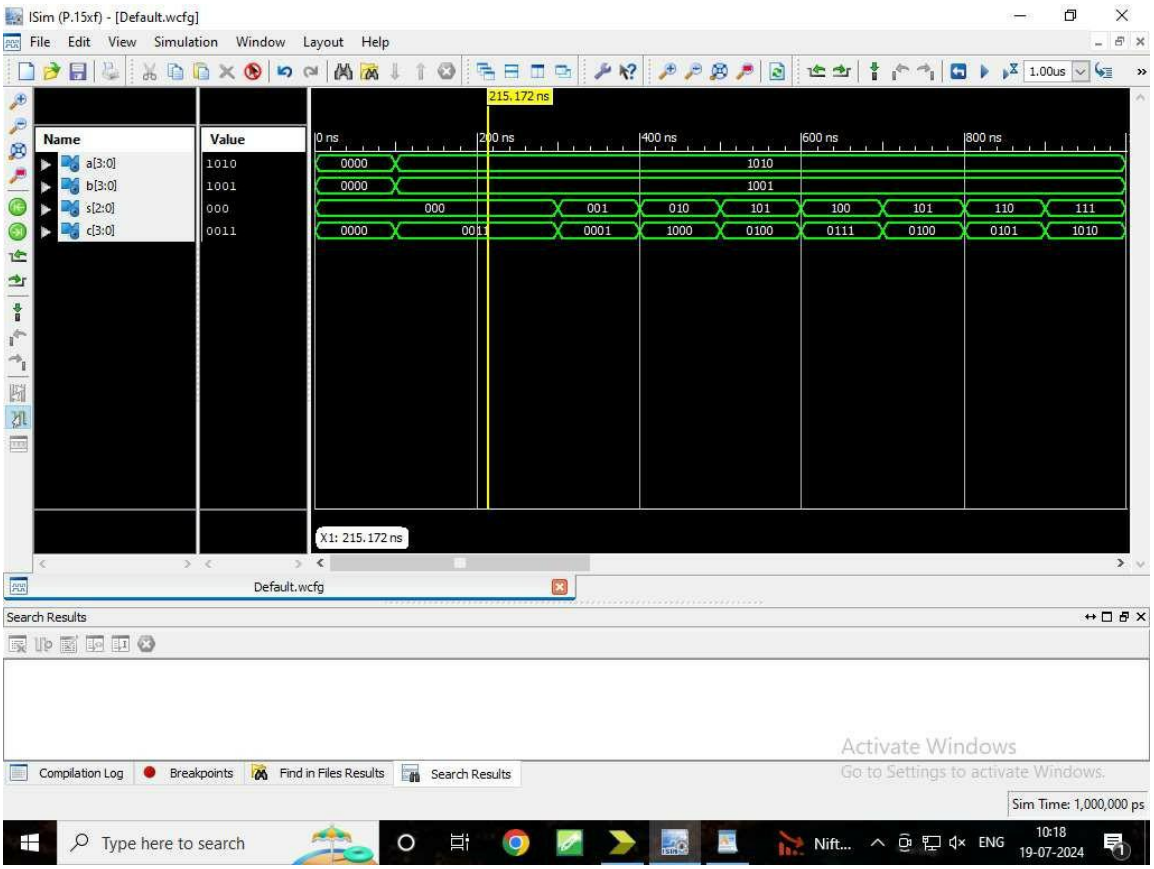
VHDL code:

```
Library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;
use IEEE.STD_LOGIC_arith.ALL;
entity abc is
    Port ( a : in    STD_LOGIC_VECTOR (3 downto 0);
           b : in    STD_LOGIC_VECTOR (3 downto
           0); s : in STD_LOGIC_VECTOR (2 downto
           0);
           c : out    STD_LOGIC_VECTOR (3 downto 0));
end abc;
architecture Behavioral of abc is
begin
process (a,b,s)
begin
case s is
when "000" => c <=a+ b;
when "001" => c <=a - b;
when "010" => c <= a and b;
when "011" => c <= a or b;
when "100" => c <= a nand b;
when "101" => c <= a nor b;
when "110" => c <=    not a;
when "111" => c <= a;
when others => null;
end case;
end process;
end Behavioral;
```

Testbench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY xyz IS
END xyz;
  ARCHITECTURE behavior OF xyz IS
        COMPONENT abc
        PORT(
                a : IN    std_logic_vector(3 downto 0);
                b : IN    std_logic_vector(3 downto
                0); s : IN    std_logic_vector(2 downto
                0);
                c : OUT    std_logic_vector(3 downto
0)); END COMPONENT;
    --Inputs
      signal a : std_logic_vector(3 downto 0) := (others => '0');
      signal b : std_logic_vector(3 downto 0) := (others => '0');
      signal s : std_logic_vector(2 downto 0) := (others => '0');
--Outputs
        signal c : std_logic_vector(3 downto 0);
  BEGIN
      uut: abc PORT MAP (
                 a => a,
                 b => b,
                 s => s,
                 c => c      );
      stim_proc: process
      begin
           -- hold reset state for 100 ns.
           wait for 100 ns;
a<="1010";
b<="1001";
s<="000";
wait for 100 ns;

  a<="1010";
b<="1001";
s<="000";
  wait for 100 ns;
a<="1010";
b<="1001";
s<="001";
  wait for 100 ns;
a<="1010";
b<="1001";
s<="010";
  wait for 100 ns;
a<="1010";
b<="1001";
s<="101";
  wait for 100 ns;
a<="1010";
b<="1001";
s<="100";
  wait for 100 ns;
a<="1010";
b<="1001";
s<="101";
  wait for 100 ns;
a<="1010";
b<="1001";
s<="110";
  wait for 100 ns;
a<="1010";
b<="1001";
s<="111";
  wait for 100 ns;
         --- wait for <clock>_period*10;
  -- insert stimulus here
wait;
end process;
END;
```


ISE Project Navigator (P.15xf) - D:\sakshiHAdder\bitalu\bitalu.xise - [abc (RTL2)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
bitalu
xc3s400-5pq208
abc - Behavioral (abc.vhd)
No Processes Running
Processes: abc - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simu...
Implement Design
Generate Programming File
abc
a(3:0)
b(3:0)
s(2:0)
c(3:0)
abc
abc.vhd
Design Summary (Synthesized)
xyz.vhd
abc.ngr:1
abc (RTL2)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
Pins
Signals
Name
Value
abc
Errors
Warnings
View by Category
Activate Windows
Go to Settings to activate Windows.
[544,488]
Type here to search
25°C
ENG
10:12
19-07-2024


ISim (P.15xf) - [Default.wcfg]
File Edit View Simulation Window Layout Help
1.00us
215.172 ns
Name
Value
a[3:0]
b[3:0]
s[2:0]
c[3:0]
1010
1001
000
0011
0 ns
200 ns
400 ns
600 ns
800 ns
0000
1010
0000
1001
000
001
010
101
100
101
110
111
0000
0011
0001
1000
0100
0111
0100
0101
1010
X1: 215.172 ns
Default.wcfg
Search Results
Activate Windows
Go to Settings to activate Windows.
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps
Type here to search
ENG
10:18
19-07-2024

UCF:

net a(3) loc=p96;

net a(2) loc=p97;

net a(1) loc=p100;

net a(0) loc=p101;

net b(3) loc=p90;

net b(2) loc=p93;

net b(1) loc=p94;

net b(0) loc=p95;

net s(2) loc=p85;

net s(1) loc=p86;

net s(0) loc=p87;

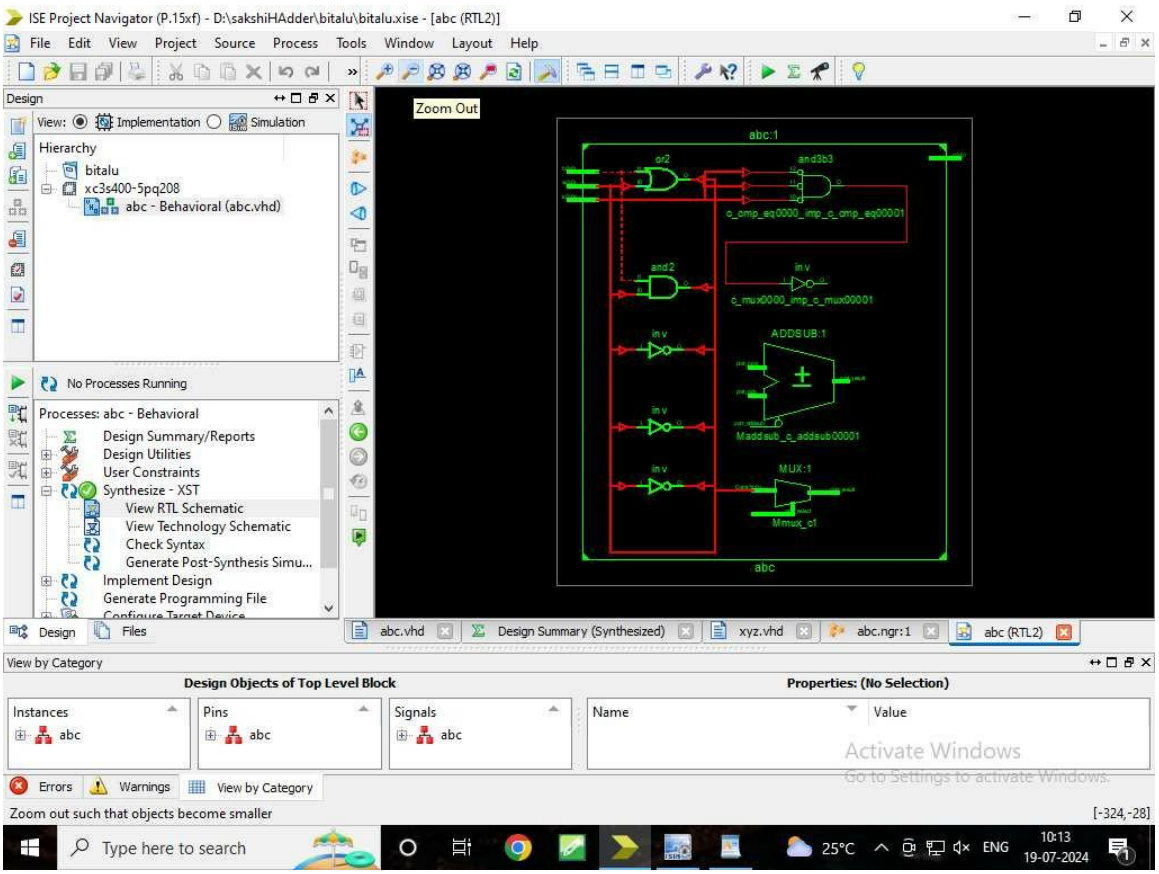
net c(3) loc=p167;

net c(2) loc=p166;

net c(1) loc=p165

net c(0) loc=p162;

RTL simulation:



```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : abc.ngr
Top Level Output File Name         : abc
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No
Design Statistics
# IOs                              : 15
Cell Usage :
# BELS                             : 34
#      LUT2                        : 5
#      LUT3                        : 10
#      LUT4                        : 6
#      MUXF5                       : 9
#      MUXF6                       : 4
# IO Buffers                       : 15
#      IBUF                        : 11
#      OBUF                        : 4
=========================================================================
Device utilization summary:
Selected Device : 3s400pq208-5
Number of Slices:                        11  out of   3584     0%
  Number of 4 input LUTs:                21  out of   7168     0%
  Number of IOs:                         15
  Number of bonded IOBs:                 15  out of    141    10%  Partition Resource Summary:
---------------------------------
  No Partitions were found in this design.
```

Experiment No: 2

Name: Siddhesh Sonavane
Roll No.: E42007

VHDL CODE

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY shiftreg IS
END shiftreg;
ARCHITECTURE behavior OF shiftreg IS
   COMPONENT unishiftreg
   PORT(
        si : IN std_logic; clk
        : IN std_logic; so :
        OUT std_logic;
        pin : IN std_logic_vector(3 downto 0);
        po : OUT std_logic_vector(3 downto 0);
        sel : IN std_logic_vector(1 downto 0)
       );
   END COMPONENT;
     --Inputs
  signal si : std_logic := '0';
  signal clk : std_logic := '0';
  signal pin : std_logic_vector(3 downto 0) := (others => '0');
  signal sel : std_logic_vector(1 downto 0) := (others => '0');
           --Outputs
  signal so : std_logic;
  signal po : std_logic_vector(3 downto 0);
  constant clk_period : time := 10 ns;
BEGIN
  uut: unishiftreg PORT MAP (
        si => si,
        clk => clk,
        so => so,
        pin => pin,
        po => po,
        sel => sel
       );
  clk_process :process
  begin
                                                    clk <= '0';
                                                    wait for clk_period/2;clk <
  end process;
```

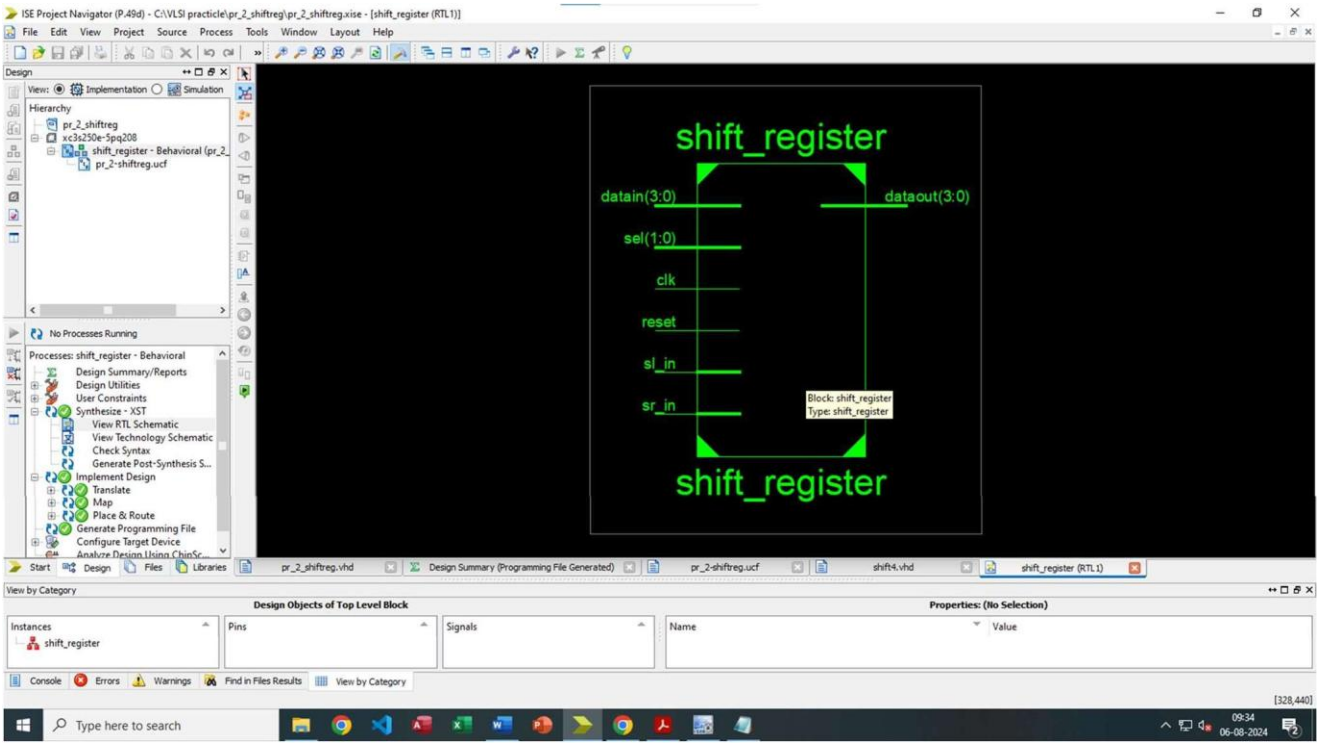
```
  =                                                    ;
  '                                                    wait for clk_period/2;
  1
  '

  stim_proc: process
  begin
     wait for 100 ns;
    wait for clk_period*10;
  end process;

END;
```

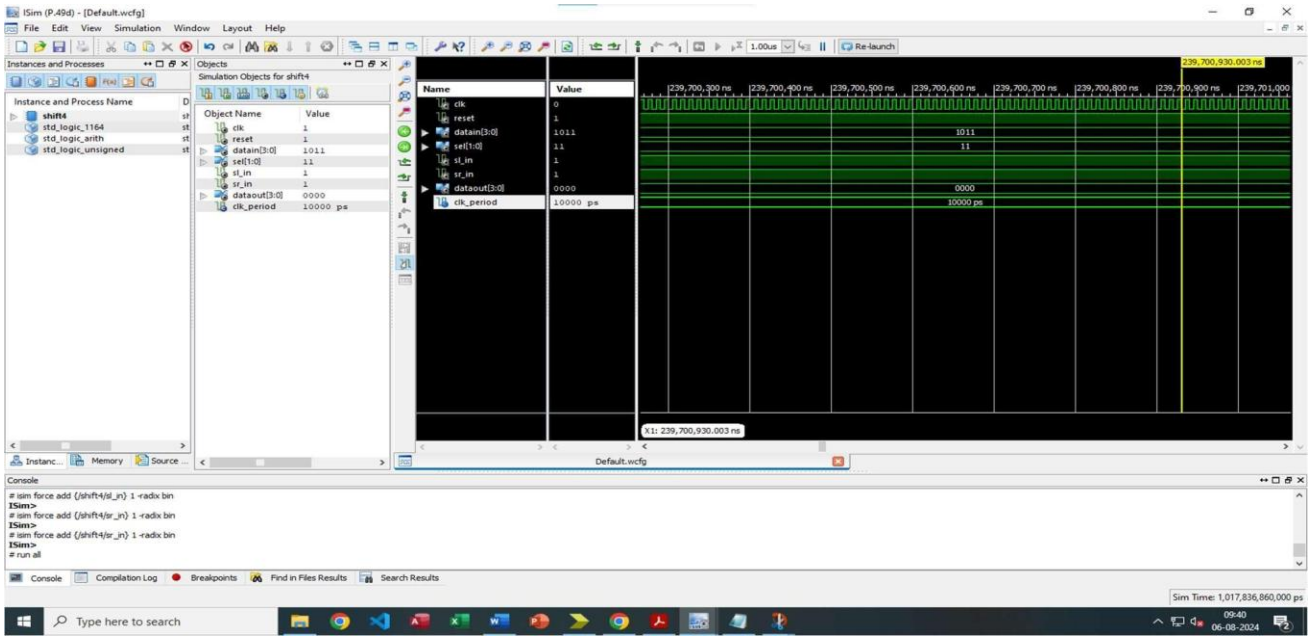
TestBench:

```
LIBRARY ieee;

USE ieee.std_logic_1164.ALL;

ENTITY tb IS

END tb;

ARCHITECTURE behavior OF tb IS

   COMPONENT unishiftreg

   PORT(

       si : IN std_logic; clk

       : IN std_logic; so :

       OUT std_logic;

       pin : IN std_logic_vector(3 downto 0);

       po : OUT std_logic_vector(3 downto 0);

       sel : IN std_logic_vector(1 downto 0)

      );

   END COMPONENT;

  --Inputs

  signal si : std_logic := '0';

  signal clk : std_logic := '0';

  signal pin : std_logic_vector(3 downto 0) := (others => '0');

  signal sel : std_logic_vector(1 downto 0) := (others => '0');

           --Outputs

  signal so : std_logic;

  signal po : std_logic_vector(3 downto 0);

  constant clk_period : time := 10 ns;

BEGIN

  uut: unishiftreg PORT MAP (

       si => si,

       clk => clk,

       so => so,
```

```
        pin => pin,
        po => po,
        sel => sel
       );
  clk_process :process
  begin
                clk <= '0';
                wait for clk_period/2;
                clk <= '1';
                wait for clk_period/2;
  end process;
  stim_proc: process
  begin
                sel <= "00";
                si <= '1';
    wait for 100 ns;
                sel <= "01";
                si <= '1';
                wait for 100 ns;
                sel <= "10";
                pin <= "1010";
                wait for 100 ns;
    wait;
  end process;
END;
```

Entity:


shift_register
datain(3:0)
dataout(3:0)
sel(1:0)
clk
reset
sl_in
sr_in
Block: shift_register
Type: shift_register
shift_register



UCF File:

NET "clk" LOC = P132; NET

"reset" LOC = P204; NET

"sl_in" LOC = P179; NET

"sr_in" LOC = P180; NET

"sel<0>" LOC = P165; NET

"sel<1>" LOC = P167;

NET "datain<0>" LOC = P192;

NET "datain<1>" LOC = P193;

NET "datain<2>" LOC = P189;

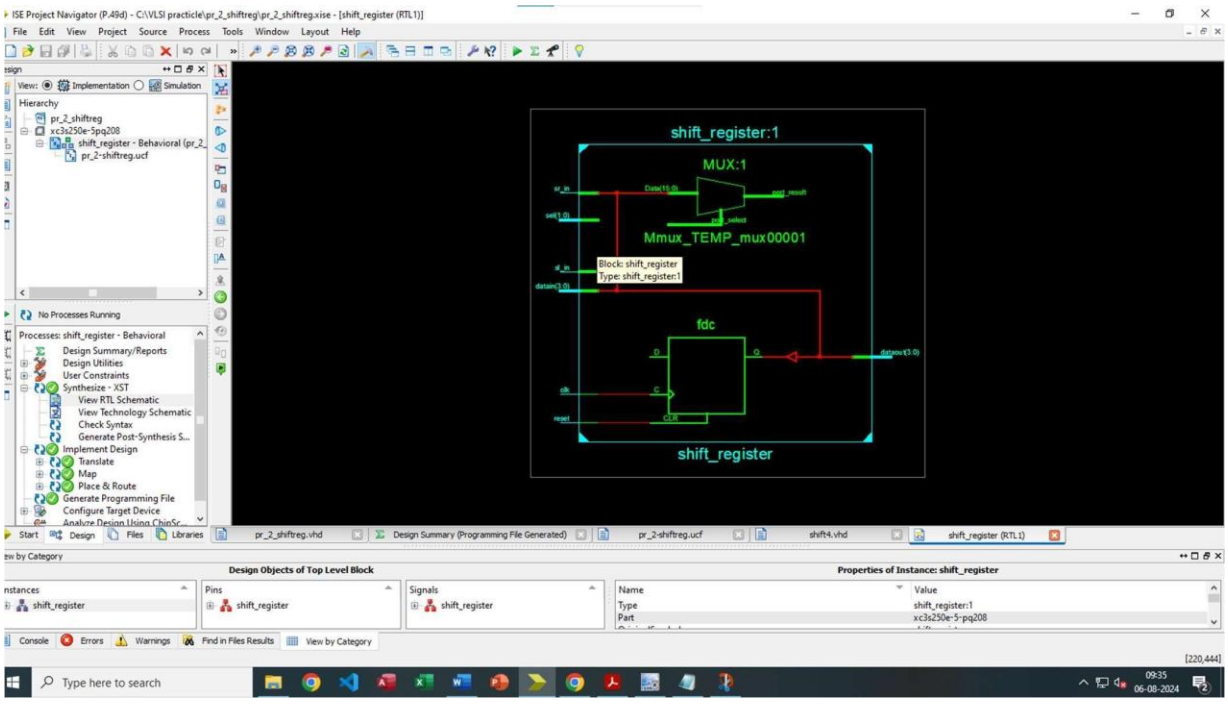
NET "datain<3>" LOC = P190;

NET "dataout<0>" LOC = P205;

NET "dataout<1>" LOC = P206;

NET "dataout<2>" LOC = P203;

NET "dataout<3>" LOC = P200;



```
=========================================================================
*                      Final Report                     *
=========================================================================
Final Results
RTL Top Level Output File Name     : unishiftreg.ngr
Top Level Output File Name         : unishiftreg
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No
Design Statistics
# IOs                              13
Cell Usage :
# BELS                             6
#      LUT2                        2
#      LUT3                        4
# FlipFlops/Latches                9
#      FD                          4
#      FDE                         5
# Clock Buffers                    1
#      BUFGP                       1
# IO Buffers                       8
#      IBUF                        3
#      OBUF                        5
=========================================================================
Device utilization summary:
---------------------------
Selected Device : 3s400pq208-5
 Number of Slices:                  5 out of 3584       0%
 Number of Slice Flip Flops:        9 out of 7168  0%
 Number of 4 input LUTs:            6 out of 7168  0%
 Number of IOs:                     13
 Number of bonded IOBs:             9 out of     141     6%
 Number of GCLKs:                   1 out of      8    12%
---------------------------
Partition Resource Summary:
---------------------------
  No Partitions were found in this design.
```

Experiment No: 3

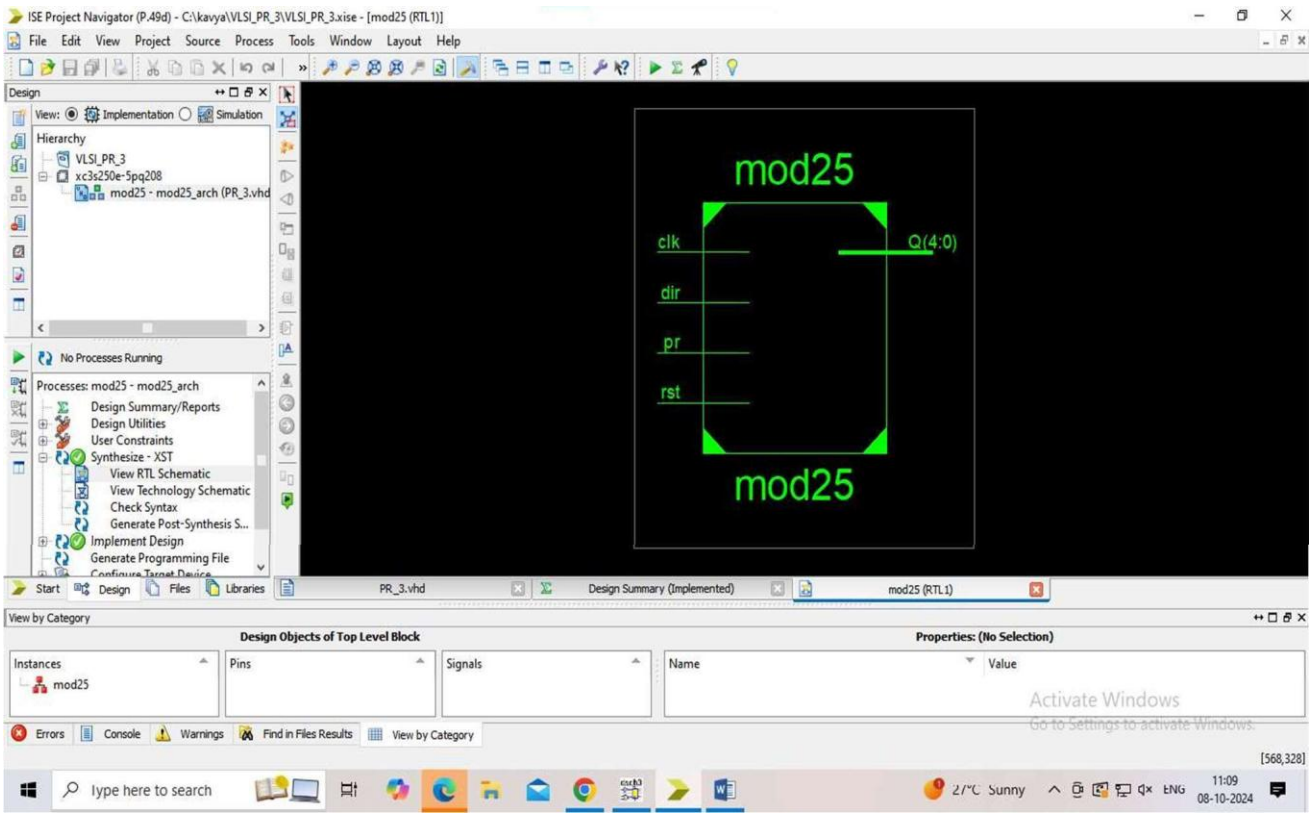
Name: Siddhesh Sonavane
Roll No: E42007

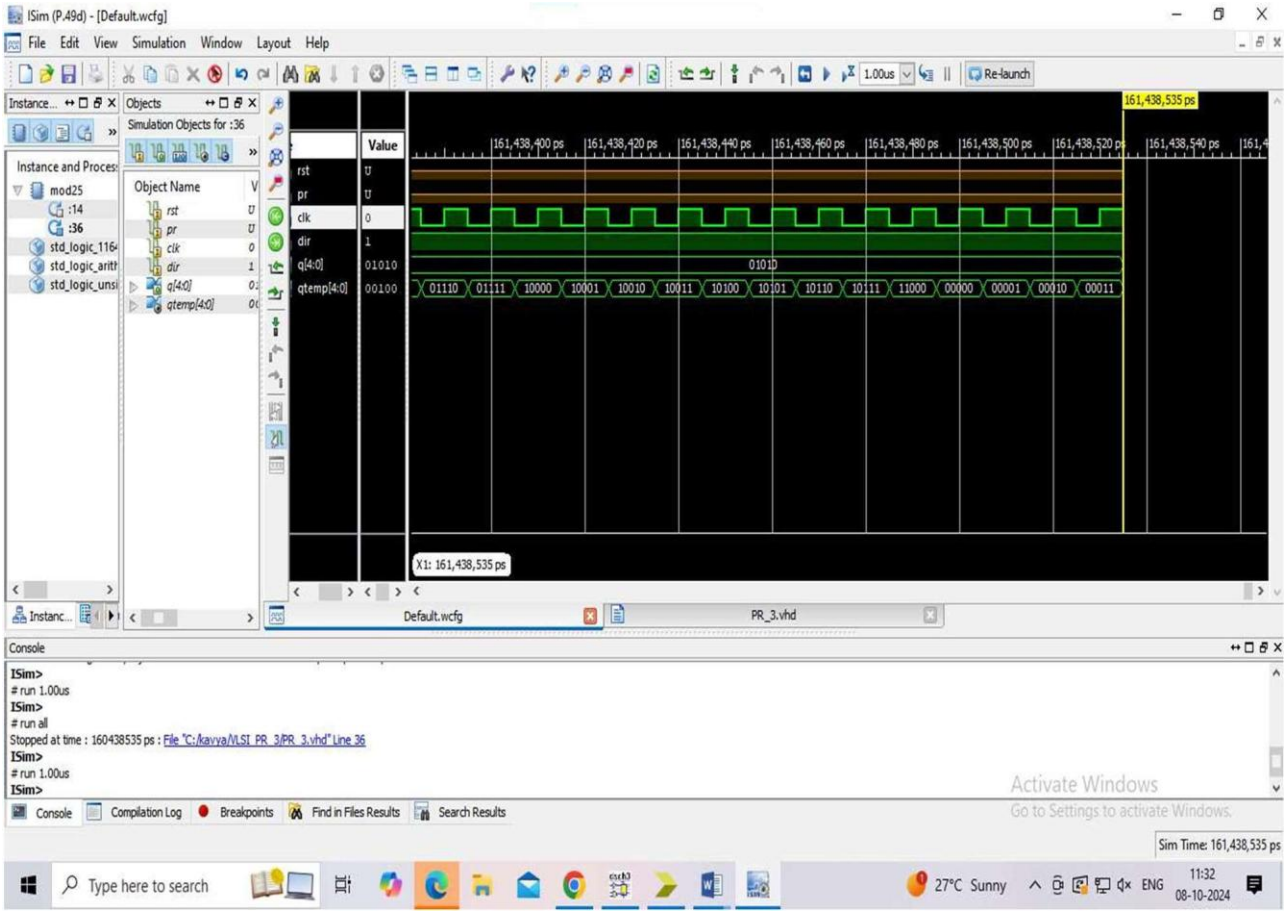
Testbench:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;
entity modncount is
   Port ( clk : in STD_LOGIC;
          clr : in STD_LOGIC;
          q : inout STD_LOGIC_VECTOR (2 downto 0));
end modncount;

architecture Behavioral of modncount is
signal count: std_logic_vector(2 downto 0);
begin
process(clk)
begin
 if (clr='1') then count <= "000";

elsif (rising_edge (clk)) then
if (count="100")
then count <= "000";

else
count<=count+ 1;
end if;
end if;
end process;
q<=count;
end Behavioral;
```

Testbench:

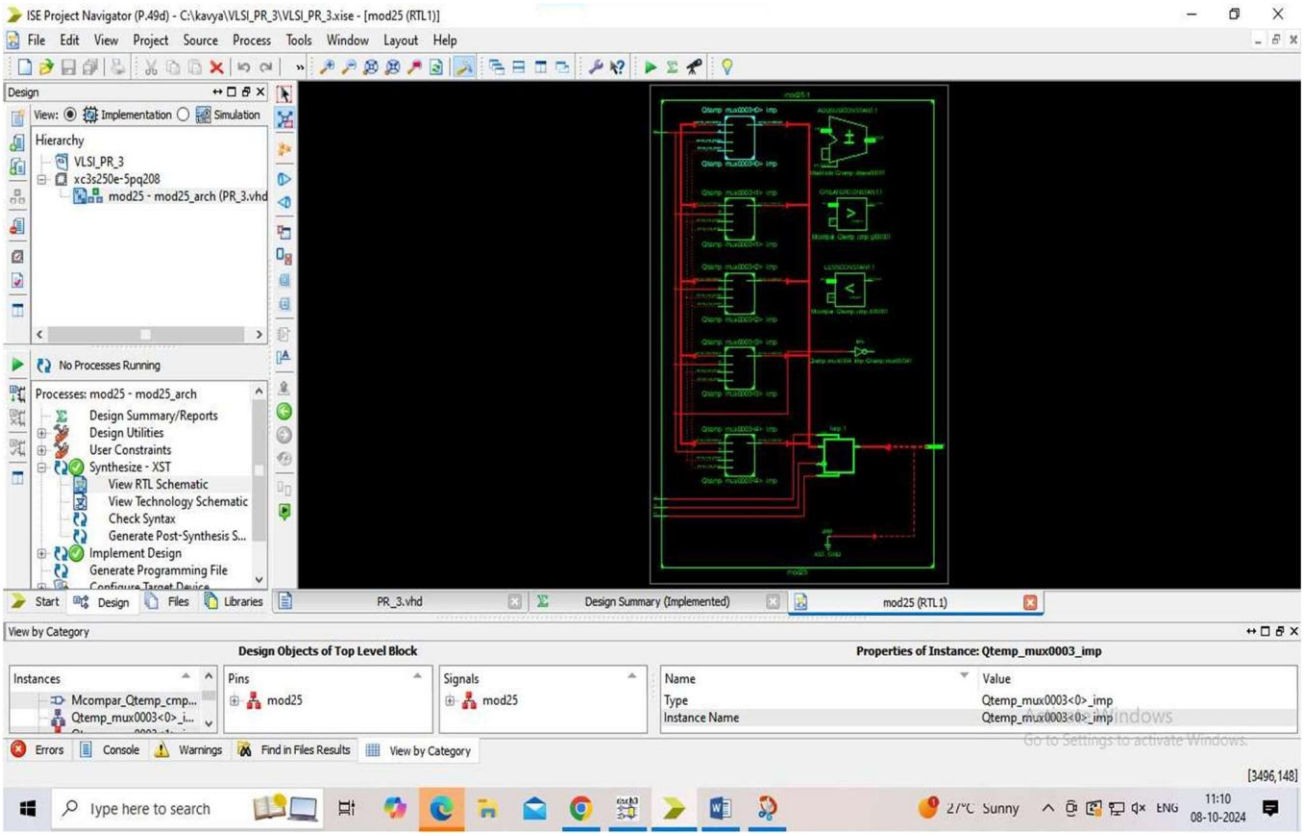
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY hhh IS
END hhh;
ARCHITECTURE behavior OF hhh IS
   COMPONENT modncount
   PORT(
        clk : IN std_logic;
        clr : IN std_logic;
        q : INOUT std_logic_vector(2 downto 0)
       );
   END COMPONENT;

  --Inputs
  signal clk : std_logic := '0';
  signal clr : std_logic := '0';
  signal q : std_logic_vector(2 downto 0);
BEGIN
   uut: modncount PORT MAP (
        clk => clk,
        clr => clr,
        q => q
       );
  clk_process :process
  begin
                        clk <= '0';
                        wait for 10 ns;
                        clk <= '1';
                        wait for 10 ns;
  end process;
  stim_proc: process
  begin
           clr<='1';
    wait for 20 ns;
                        clr<='0';
    wait for 20 ns;
    wait;
  end process;

END;
```

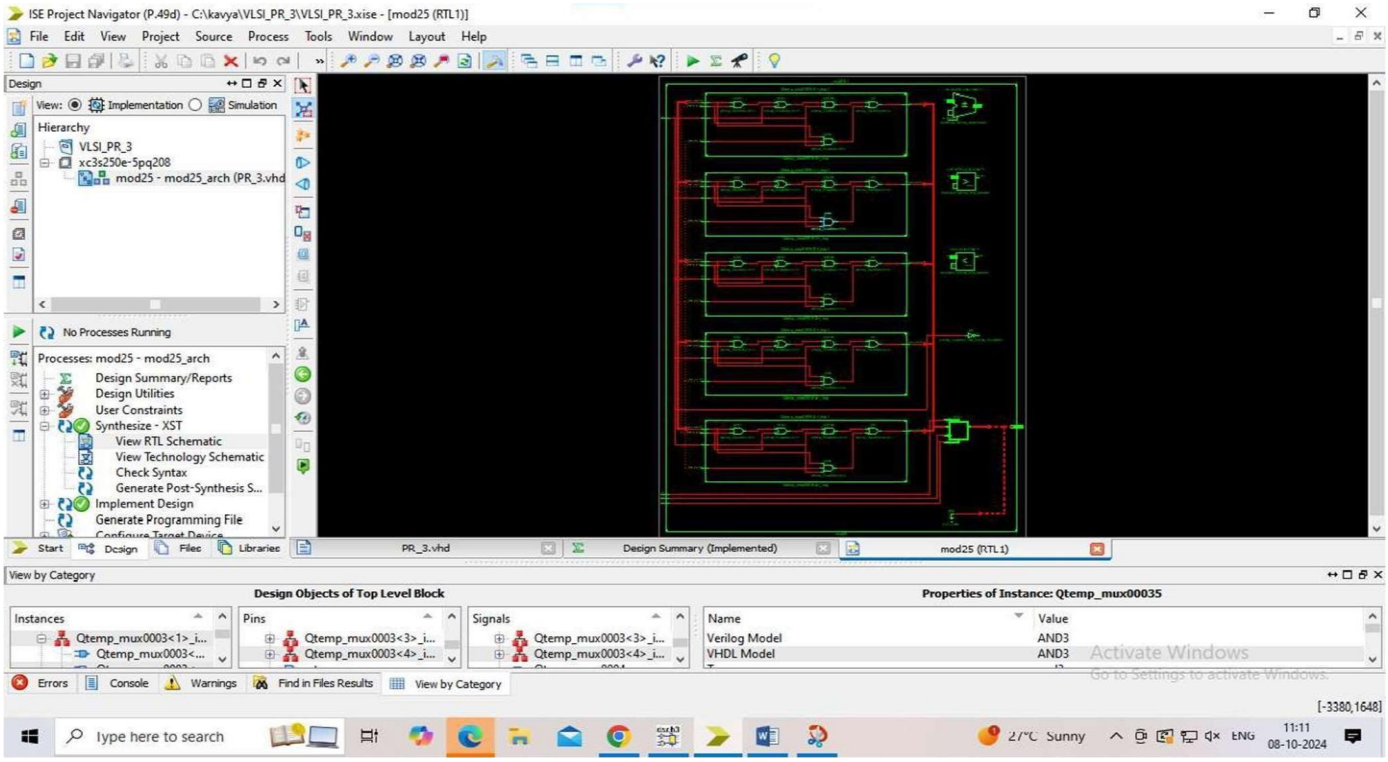

ISE Project Navigator (P.49d) - C:\kavya\VLSI_PR_3\VLSI_PR_3.xise - [mod25 (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
VLSI_PR_3
xc3s250e-5pq208
mod25 - mod25_arch (PR_3.vhd
No Processes Running
Processes: mod25 - mod25_arch
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis S...
Implement Design
Generate Programming File
mod25
clk
dir
pr
rst
Q(4:0)
mod25
Start Design Files Libraries
PR_3.vhd
Design Summary (Implemented)
mod25 (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
mod25
Pins
Signals
Name
Value
Activate Windows
Go to Settings to activate Windows.
Errors Console Warnings Find in Files Results View by Category
[568,328]
Type here to search
27°C Sunny
ENG
11:09
08-10-2024

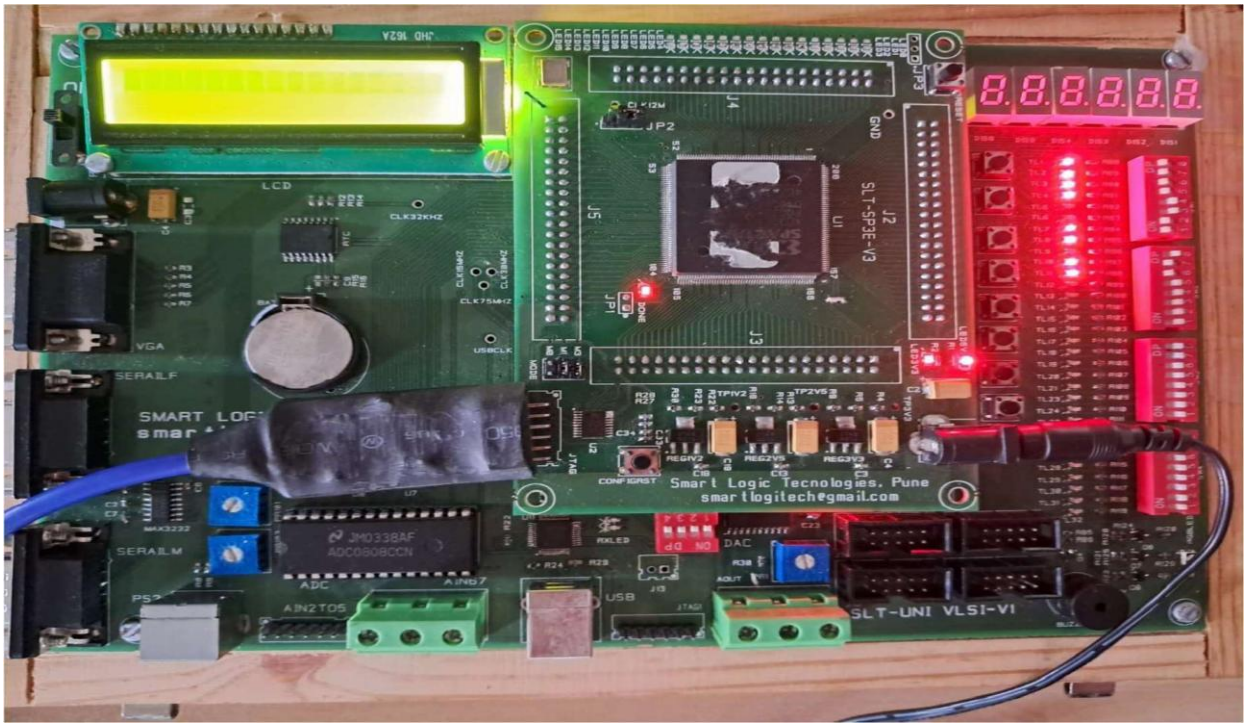

ISim (P.49d) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instance and Proces:
mod25
:14
:36
std_logic_116
std_logic_arith
std_logic_unsi
Objects
Simulation Objects for :36
Object Name
rst
pr
clk
dir
q[4:0]
qtemp[4:0]
Value
rst U
pr U
clk 0
dir 1
q[4:0] 01010
qtemp[4:0] 00100
161,438,400 ps
161,438,420 ps
161,438,440 ps
161,438,460 ps
161,438,480 ps
161,438,500 ps
161,438,520 ps
161,438,535 ps
01010
01110 01111 10000 10001 10010 10011 10100 10101 10110 10111 11000 00000 00001 00010 00011
X1: 161,438,535 ps
Default.wcfg
PR_3.vhd
Console
ISim>
run 1.00us
ISim>
run all
Stopped at time : 160438535 ps : File "C:/kavya/VLSI_PR_3/PR_3.vhd" Line 36
ISim>
run 1.00us
ISim>
Activate Windows
Go to Settings to activate Windows.
Console Compilation Log Breakpoints Find in Files Results Search Results
Sim Time: 161,438,535 ps
Type here to search
27°C Sunny
ENG
11:32
08-10-2024

UCF

Net clk loc=”p182”;
Net clr loc=”p102”;
Net q(2) loc=”p165”;
Net q(2) loc=”p166”;
Net q(2) loc=”p167”;




ISE Project Navigator (P.49d) - C:\kavya\VLSI_PR_3\VLSI_PR_3.xise - [mod25 (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
VLSI_PR_3
xc3s250e-5pq208
mod25 - mod25_arch (PR_3.vhd
No Processes Running
Processes: mod25 - mod25_arch
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis S...
Implement Design
Generate Programming File
Start
Design
Files
Libraries
PR_3.vhd
Design Summary (Implemented)
mod25 (RTL1)
View by Category
Design Objects of Top Level Block
Instances
Pins
Signals
Properties of Instance: Qtemp_mux00035
Name
Value
Verilog Model
AND3
VHDL Model
AND3
Activate Windows
Go to Settings to activate Windows.
Errors
Console
Warnings
Find in Files Results
View by Category
[-3380,1648]
Type here to search
27°C Sunny
ENG
11:11
08-10-2024


LCD
VGA
SERIALF
SERIALM
SMART LOGI
smar
Smart Logic Tecnologies, Pune
smartlogitech@gmail.com
SLT-UNI VLSI-VI
SLT-SP3E-V3
JP1
JP2
JP3
J2
J3
J5
U1
U4
GND
DONE
CONFIGRST
USB
DAC
ADC
JM0338AF
AD0808CCN
CLK32KHZ
CLK75MHZ
USBCLK

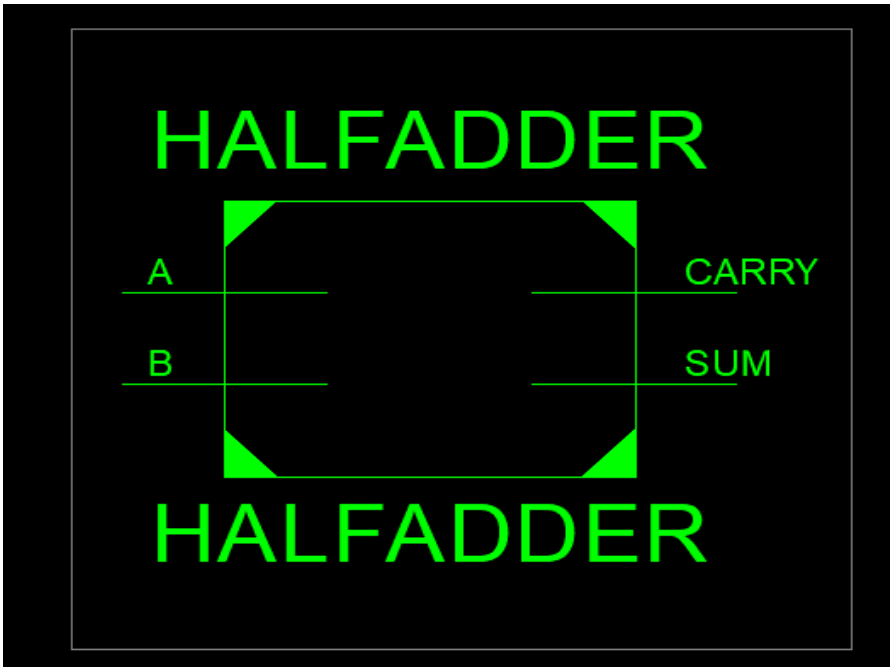
Practical 10

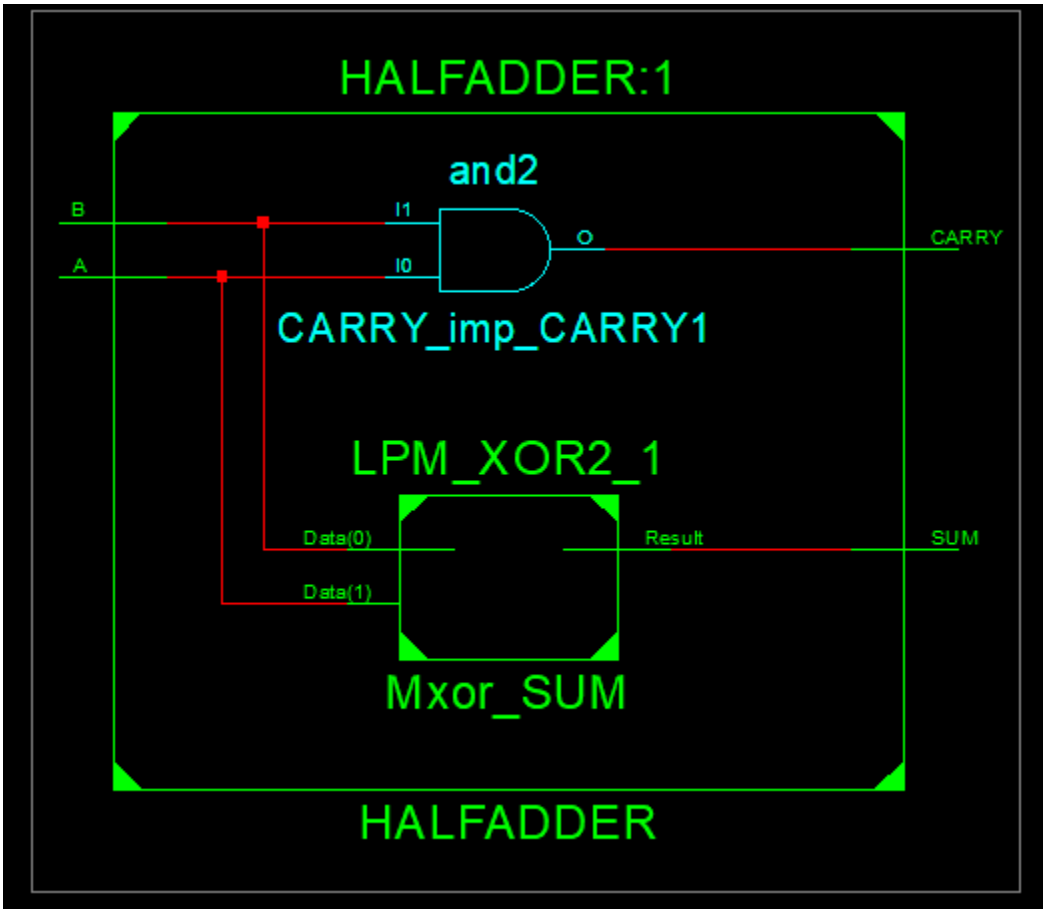
Name: Siddhesh Sonavane

Roll no: E42007

HALDADDER

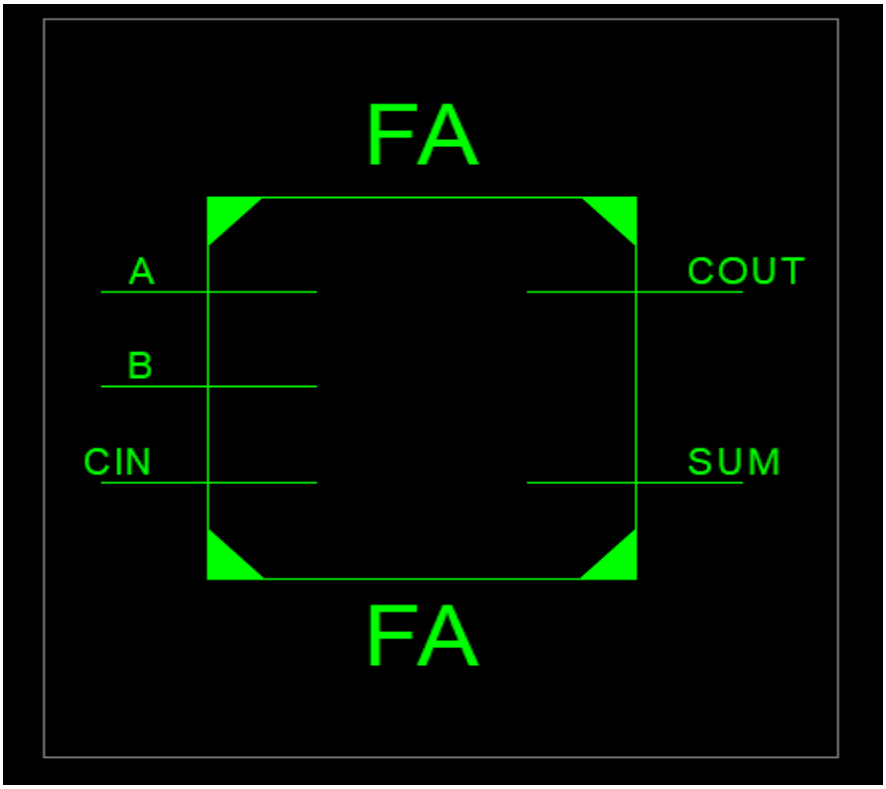
```
libraryIEEE;
use IEEE.STD_LOGIC_1164.ALL;
entityHALFADDERis
    Port ( A : in   STD_LOGIC;
           B : in   STD_LOGIC;
           SUM : out   STD_LOGIC;
           CARRY : out   STD_LOGIC);
endHALFADDER;

architectureBehavioralofHALFADDERis begin
SUM<=A XOR B;
CARRY<=AANDB;
endBehavioral;
```

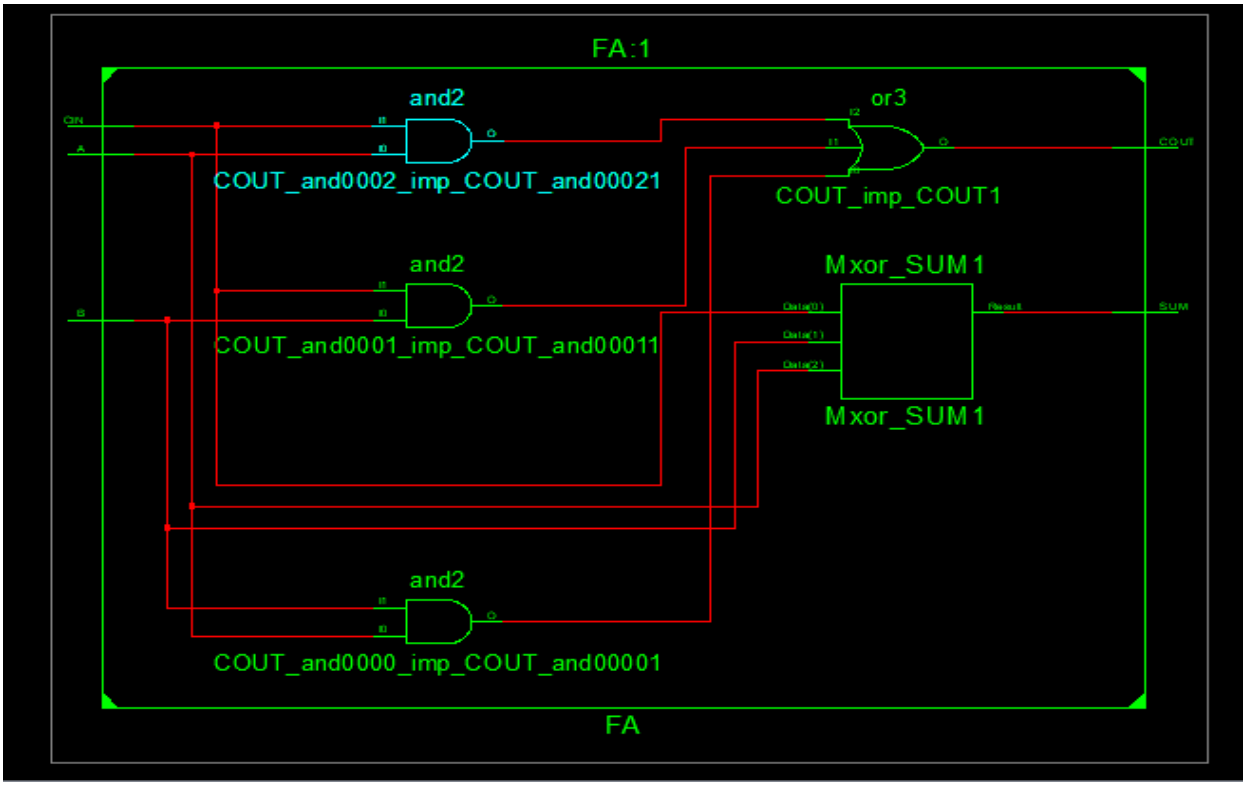

HALFADDER
A
B
CARRY
SUM
HALFADDER


HALFADDER:1
and2
B
A
I1
I0
O
CARRY
CARRY_imp_CARRY1
LPM_XOR2_1
Data(0)
Data(1)
Result
SUM
Mxor_SUM
HALFADDER

```
FULLADDER
libraryIEEE;
use IEEE.STD_LOGIC_1164.ALL;

entityFULLADDERis
    Port ( A : in   STD_LOGIC;
           B : in   STD_LOGIC;
           CIN : in   STD_LOGIC;
           SUM : out   STD_LOGIC;
           COUT : out   STD_LOGIC);
endFULLADDER;

architectureBehavioralofFULLADDERis begin
component HALFADDER
port(A:in     STD_LOGIC;
           B : in   STD_LOGIC;
           SUM : out   STD_LOGIC;
           CARRY:out     STD_LOGIC);
endcomponent;
signalS1,C1,C2:STD_LOGIC;
begin
ha1:HALFADDER port map (A,B,S1,C1);
ha2:HALFADDERportmap(S1,CIN,SUM,C2);
COUT<=C1 OR C2;
```

endBehavioral;





TESTBENCH

```
 LIBRARYieee;
USEieee.std_logic_1164.ALL;

ENTITYFAAIS
END FAA;

ARCHITECTUREbehaviorOFFAAIS
    --ComponentDeclarationfortheUnitUnderTest(UUT) COMPONENT
    FA
    PORT(
          A: IN    std_logic;
          B : IN   std_logic;
          CIN : IN   std_logic;
          SUM : OUT   std_logic;
          COUT : OUT   std_logic
         );
    ENDCOMPONENT;

   --Inputs
   signal A : std_logic := '0';
   signal B : std_logic := '0';
   signalCIN:std_logic:='0';
```

```
        --Outputs
    signal SUM : std_logic;
    signalCOUT:std_logic;
BEGIN
        --InstantiatetheUnitUnderTest(UUT) uut:
    FA PORT MAP (
            A=>A,
            B=>B,
            CIN => CIN,
            SUM=>SUM,
            COUT=>COUT);
    --Stimulusprocess
    stim_proc:  process
    begin
        --holdresetstatefor100ns.
A<='0';B<='0';CIN<='0';
waitfor100ns;
A<='0';B<='0';CIN<='1';
waitfor100ns;
A<='0';B<='1';CIN<='0';
waitfor100ns;
A<='0';B<='1';CIN<='1';
waitfor100ns;
A<='1';B<='0';CIN<='0';
```

```
waitfor100ns;
A<='1';B<='0';CIN<='1';
waitfor100ns;
A<='1';B<='1';CIN<='0';
waitfor100ns;
A<='1';B<='1';CIN<='1';
waitfor100ns; wait;
    endprocess;
```