Article

Scalable feedback stabilization of quantum light sources on a CMOS chip

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Silicon photonics could soon be used to create the vast numbers of physical qubits needed to achieve useful quantum information processing by leveraging mature complementary metal–oxide–semiconductor (CMOS) manufacturing to miniaturize optical devices for generating and manipulating quantum states of light. However, the development of practical silicon quantum-photonic integrated circuits faces challenges related to high sensitivity to process and temperature variations, free-carrier and self-heating nonlinearities, and thermal crosstalk. These issues have been partially addressed with bulky off-chip electronics, but this sacrifices many benefits of a chip-scale platform. Here we report an electronic–photonic quantum system-on-chip that consists of quantum-correlated photon-pair sources stabilized via on-chip feedback control circuits and is fabricated in a commercial 45-nm CMOS microelectronics foundry. We use non-invasive photocurrent sensing in a tunable microring cavity photon-pair source to actively lock it to a fixed-wavelength pump laser while operating in the quantum regime, enabling large-scale microring-based quantum systems. We also show that these sources maintain stable quantum properties and operate reliably in a practical setting with many adjacent photon-pair sources creating thermal disturbances on the same chip. Such dense integration of electronics and photonics enables implementation and control of quantum-photonic systems at the scale needed to achieve useful quantum information processing with CMOS-fabricated chips.

Photonics is a compelling approach for the development of quantum technologies—including quantum computing, secure communication and sensing—due to its robustness to decoherence at room temperature, natural compatibility with optical interconnects for entanglement distribution and ability to be miniaturized into chip-scale devices[1,2]. Silicon photonics[3] offers the most scalable platform for quantum-photonic systems, allowing them to be built using mature semiconductor fabrication techniques developed in the complementary metal–oxide–semiconductor (CMOS) microelectronics industry[4,5], which routinely produces chips with billions of transistors in high volumes.

Within this platform, third-order ($\chi^{(3)}$) optical nonlinearity in silicon and silicon nitride waveguides[6,7] and microring resonators[8] allows quantum-correlated photon pairs to be generated via spontaneous four-wave mixing (SFWM), which can be used to build compact sources of heralded flying qubits. Furthermore, recent advances in

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heterogeneous material integration onto silicon photonic chips have the potential to create a library of optical devices needed to assemble a large-scale photonic quantum computer in a CMOS foundry platform[9]. These include III–V lasers for pumping single-photon qubit sources[10,11]; deterministic quantum emitters based on III–V quantum dots[12–14]; electro-optic materials for high-speed, low-loss optical switches and modulators used in state preparation and manipulation[15–18]; and high-efficiency superconducting nanowire single-photon detectors (SNSPDs) for qubit read out and feed-forward operations[19–21]. To function properly, however, silicon quantum photonic devices, especially microresonator-based ones like photon-pair sources and filters, require continuous monitoring and control by electronic circuits. So far, this has been carried out using bulky off-chip electronics[22], limiting the practically achievable system size and complexity.

Microring resonator photon-pair sources are an essential building block for silicon quantum photonics as the field enhancement from their high cavity quality (Q) factors and finesse boosts the rate and spectral brightness with which photon pairs are generated[23]. They can be used to replace millimetre-scale photon sources based on straight waveguides with resonators as small as a few tens of micrometres in diameter[24]. Such miniaturized sources can provide the vast numbers of heralded single-photon qubits needed per chip for useful quantum information processing. However, the high (typically $\gg$10,000) Q factors of microrings optimized for SFWM also create calibration and control challenges that have limited practical quantum-optical experiments based on silicon photonics to no more than a few interacting microring sources[25–29], with recent larger systems so far still relying on non-resonant devices[30,31]. These challenges stem from the need for the narrow-linewidth resonances of all microrings in a system to be closely aligned to the same set of pump laser and output wavelengths (historically called the 'signal' and 'idler') to produce streams of heralded photons capable of quantum interference[26,32].

The sources of wavelength mismatch between different microring resonators can broadly be separated into two types: static mismatches and dynamic effects. The former arise from fabrication-induced variations inherent to semiconductor manufacturing such as uneven device layer film thicknesses and etch depths across a wafer, leading to initial differences on the order of nanometres between microring resonance wavelengths even in state-of-the-art processes[33,34]. Dynamic effects, however, arise from factors that are not fixed at fabrication time such as the temperature and free-carrier concentration in each microring. These include thermal crosstalk from the calibration and reconfiguration of other nearby photonic components over the course of operating a system, as well as optical loss mechanisms such as two-photon absorption[35] and free-carrier absorption[36], which lead to self-heating as the circulating optical power increases. When the pump laser power is boosted to maximize the photon-pair generation rate, this self-heating creates a positive feedback loop that eventually manifests as thermal hysteresis[37,38], preventing an on-resonance lock between a microring and pump laser unless the microring's temperature is initialized and stabilized properly[39,40].

Additionally, plasma dispersion from electrons and holes generated by two-photon absorption and other parasitic absorption mechanisms shifts microring resonances in the opposite direction of self-heating[41]. This can result in unstable behaviour such as optical pulsing[42] where the two effects take turns pushing the microring's resonances in opposite directions and cause the cavity's optical energy to oscillate, sometimes chaotically[43], which prevents stable photon-pair generation. To make microring-based sources viable for large-scale quantum systems-on-chip, these calibration and control issues must be addressed using chip-scale electronics that are densely co-packaged with the silicon photonics and capable of correcting resonance wavelength errors in real time without disrupting the quantum characteristics of the system.

In this Article, we report an electronic–photonic quantum system-on-chip that is capable of stabilizing SFWM in microring resonators in an in situ manner by sensing and minimizing their wavelength errors in the quantum regime using on-chip electronics with a compact footprint of 220 μm × 190 μm. Our system-on-chip (Fig. 1a–c)—in which active silicon photonics are optimized for generating photon pairs in the C band (wavelength, 1,530–1,565 nm)—is fabricated in the GlobalFoundries 45RFSOI CMOS process using the same silicon-on-insulator (SOI) layer as nearby analogue and digital control electronics[44].

This approach was originally developed for integrating classical optical interconnects with microprocessors, where the operation of hundreds of silicon photonic devices alongside tens of millions of transistors has already been demonstrated[45–49]. We previously demonstrated passive quantum photonics in this platform[50], including a single chip with SFWM photon-pair generation and >95-dB pump filtering[51], as proofs of concept that quantum photonics can be implemented in a CMOS platform supporting electronic circuits. Here we demonstrate techniques to enable scalable quantum photonics to be implemented within this platform. In particular, we integrate non-invasive photocurrent sensors within the SFWM-optimized microrings that allow their circulating optical power to be sensed directly, avoiding the need to switch between classical detectors for calibration and quantum detectors for operation[22], or to use separate post-filters and photodetectors that occupy additional area and must themselves be aligned to the correct range of wavelengths[28]. Our integrated and modular control approach paves the way for silicon quantum photonics to achieve the massive scale required for future generations of quantum information systems.

Electronic–photonic quantum system-on-chip

Figure 1d,e shows the schematic of the system for stabilizing SFWM in silicon microring resonators. Embedded sensors allow integrated control electronics to monitor the optical power in a resonator and then thermally tune it via an integrated heater to lock to a pump laser. Twelve such systems with variations in the photonic device parameters are present in the fabricated chip, using 400-nm-wide single-mode waveguides patterned in the sub-100-nm-thick SOI device layer to confine and route light. Optical coupling to the chip is achieved via bilayer unidirectional vertical grating couplers (VGCs) implemented in the silicon body and polysilicon gate layers[52,53]. At the core of each system is a high-Q microring resonator with a radius of ~20 μm designed to produce photon pairs via SFWM, enable optical power monitoring within the cavity and support resonance tuning. Since only one thickness of SOI is available in standard CMOS microelectronics processes and the doped polysilicon gate layer introduces large losses in the microrings[54], a conventional rib waveguide geometry was avoided. Instead, optical power sensing is achieved using a wide multimode SOI waveguide with interdigitated p–i–n diodes along the inner edge of the microring away from the fundamental optical mode. This establishes multiple parallel photodiodes that sweep out and collect photogenerated carriers in the silicon waveguide. An adiabatically wrapped ring-bus coupler prevents higher-order transverse modes from being excited in the 2.8-μm-wide waveguide cross-section of the resonator, coupling only to the fundamental mode propagating closer to the outer edge of the ring[55,56]. This separation between the heavily doped contacts and propagating light allows the resonator to maintain an intrinsic Q on the order of 10^5, comparable with undoped single-mode microrings in the same process[45,50]. The ring radius and waveguide width have been selected to optimize the four-wave-mixing strength within the constraints of the CMOS platform by trading off between the mode volume, intrinsic Q factor and dispersion (Supplementary Section 1).

Although silicon is transparent in the C band, carriers can still be generated by defect and surface-state absorption[57], as well as two-photon absorption at higher circulating optical powers in the resonator[35]. These effects produce a responsivity on the order of 1 mA W^{-1} of bus-waveguide pump light that is sufficient for sensing the alignment of the resonance wavelength to the pump laser by

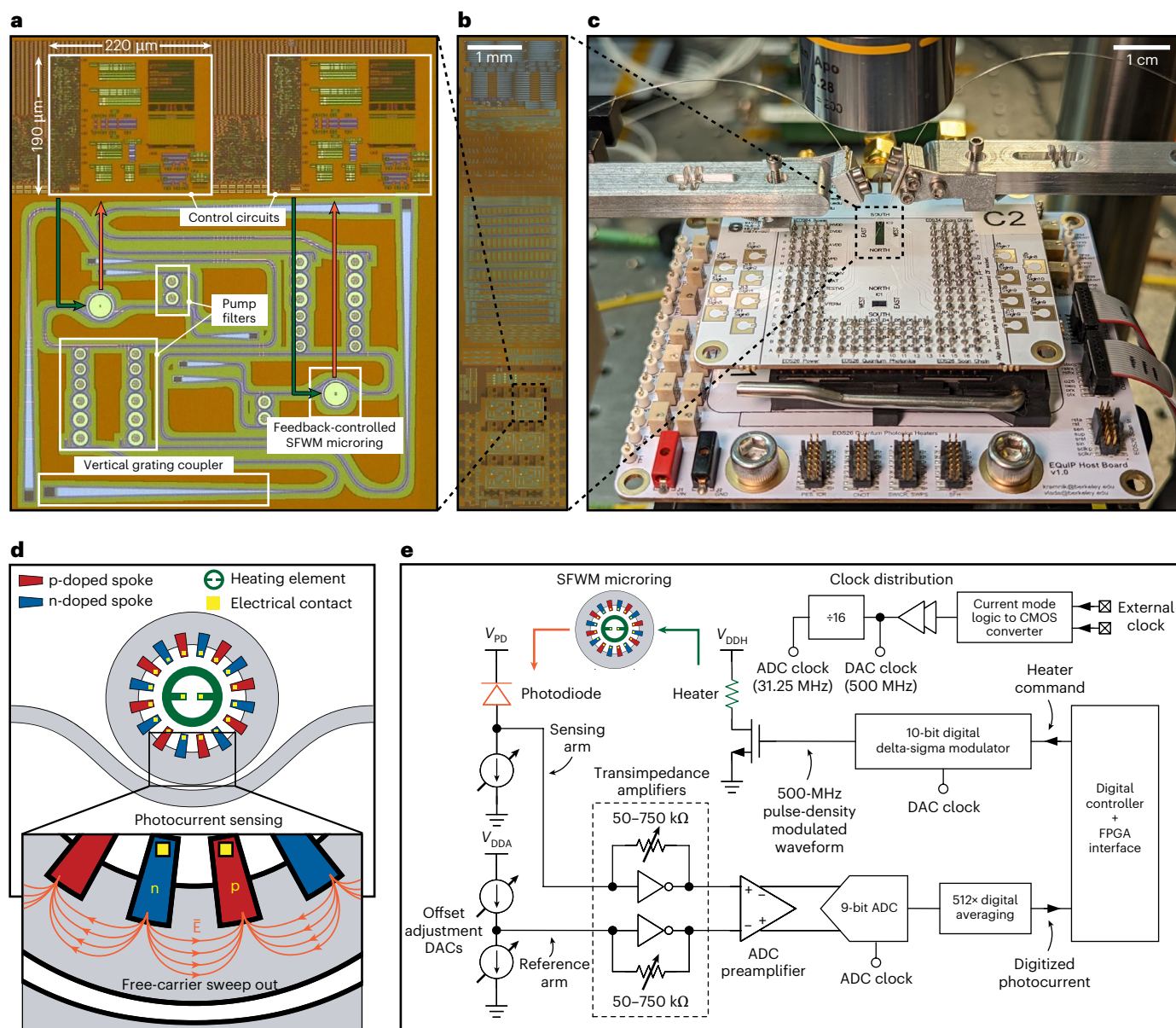**Fig. 1 | Electronic–photonic quantum system-on-chip. a**, Micrograph of two interleaved electronic–photonic quantum circuit blocks with 220 μm × 190 μm control circuits and 19.1-μm-radius SFWM microrings. **b**, Micrograph showing the entire 2 mm × 9 mm electronic–photonic CMOS chip, which contains 12 photon-pair source blocks towards the bottom. **c**, The CMOS chip is flip-chip bonded to a printed circuit board that provides power and interfaces to an FPGA and a personal computer. The silicon handle is removed via a XeF$_2$ dry etch to enable optical access from the back side of the chip via lensed fibre probes coupling to the VGCs from above. **d**, Diagram of the SFWM-optimized microring with p–i–n diodes for carrier sweep out in reverse bias. **e**, Schematic of the feedback-controlled SFWM microring pair source, showing the on-chip circuits for thermal tuning and in-cavity light intensity monitoring via the p–i–n junction photodiodes.

on-chip circuits and avoiding the loss penalty and intrinsic Q reduction of a drop-port photodetector or absorbing material such as SiGe (ref. 58). Carrier sweep out also mitigates carrier-induced losses and nonlinear effects. This boosts the efficiency of the four-wave-mixing process[59,60] and delays or eliminates the onset of free-carrier-induced instability, with the trade-off being that the work done to extract the carriers increases self-heating and lowers the pump power threshold for optical bistability[61]. To transduce the photocurrent produced at typical pump powers of 100 μW–1 mW to CMOS voltage levels, we use an inverter-based transimpedance amplifier with an adjustable gain of 50–750 kΩ to amplify the signal before it is digitized by an on-chip analogue-to-digital converter (ADC) and sent to a digital circuit block for processing. A pseudo-differential amplifier structure

is implemented to improve power supply noise rejection and programmable current sources at the input enable automatic offset calibration. Further circuit implementation and calibration details are provided in Supplementary Section 2.

The integrated digital circuits can either run a fully self-contained hard-coded algorithm to search for and lock near the maximum photocurrent or send the ADC data to an external controller and receive commands through a serial scan chain. Once this digital system processes the ADC measurements to generate a feedback command, resonance wavelength adjustments are executed by an on-chip digital-to-analogue converter (DAC) driving a resistive heater in the centre of the ring, which tunes the resonance wavelengths via the thermo-optic effect in silicon[62]. We used a high-frequency (500 MHz) switching output stage
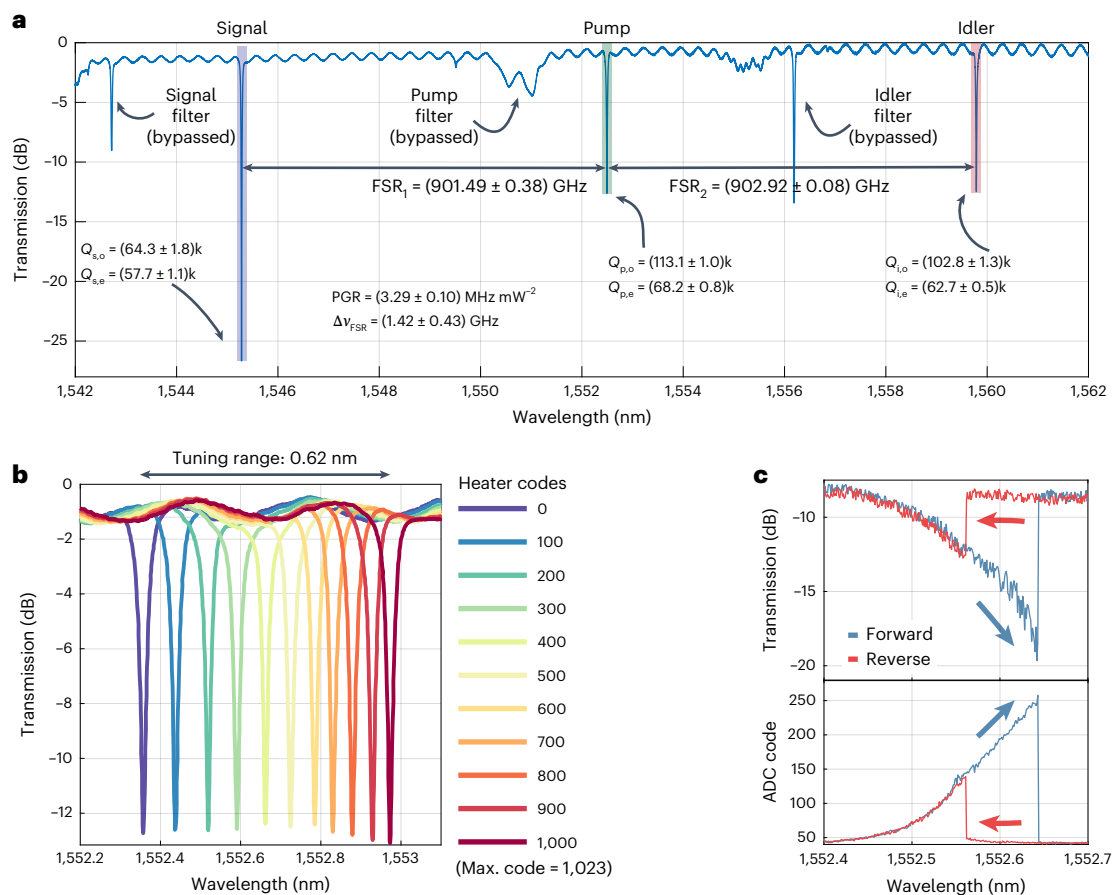
Fig. 2 | Classical characterization of the electronic–photonic integrated circuit block. a, Normalized transmission spectrum of the SFWM microring system site with fitted intrinsic and extrinsic Q factors, FSR mismatch and predicted PGR based on the equations in Supplementary Section 1. The three resonances at 1,545.3 nm (signal), 1,552.5 nm (pump) and 1,559.8 nm (idler) are chosen for photon-pair generation. On-chip pump ASE cleanup and pump rejection filters are bypassed for the experiments reported here. **b**, Stand-alone characterization of the SFWM microring heater DAC with the V_{DDH} supply set to 1.3 V, which produces an LSB step of 0.6 pm (76 MHz) and overall wavelength-

tuning range of 0.62 nm with 5.1-mW maximum heater power. **c**, Normalized transmission spectrum (top plot) and the corresponding digitized photocurrent from the SFWM microring (bottom plot) with –5.1-dBm on-chip pump power as the laser is swept forward from short to long wavelengths and in reverse from long to short wavelengths, demonstrating the thermal bistability in the microring. The microring resonance must be initialized to a longer wavelength than the pump laser (corresponding to the forward sweep) to make it possible to access the fully on-resonance state.

driven by a delta-sigma modulator to improve the circuit efficiency and ensure that the ten-bit DAC command to heater power transfer curve is monotonic[63], which is required to create a stable negative feedback loop to control the resonance wavelength. Adjusting an externally provided DAC output stage supply voltage (V_{DDH}) allows the tuning range and least-significant bit (LSB) step size to be scaled together proportionately—for the experiments here, we selected V_{DDH} = 1.3 V, resulting in an LSB step of 0.6 pm (76 MHz) and overall wavelength-tuning range of 0.62 nm with 5.1-mW maximum heater power. The LSB step is chosen to be small enough compared with the ~5-GHz full-width at half-maximum linewidths of the cold SFWM microring resonance to enable locking to within a few per cent of the peak photocurrent, maximizing the pair generation rate (PGR). Figure 2 shows the transmission spectra of a microring photon-pair source with varying DAC settings applied to the heater, and photocurrent measurements by the ADC as the heater is swept from cold to hot and vice versa, displaying the characteristic thermal bistability of high-Q silicon microrings.

Feedback control of photon-pair generation in a microring

To access the state in which its resonance is aligned with the pump laser, the microring has to be initialized hot to place the resonance at a longer wavelength than the pump laser. Then, as it is cooled,

its resonance shifts to shorter wavelengths until at a certain point, the additional self-heating from absorbing some of the pump light counteracts this by exactly the right amount to align the two, inducing the maximum amount of photocurrent in the p–i–n diodes. Any further reduction in heater power beyond this point causes the resonance to quickly snap away to shorter wavelengths as the self-heating effect reverses from stable negative feedback to unstable positive feedback[39]. The responsivity of the microring, coupling condition, pump laser optical path insertion losses and sensing circuit gain are subject to fabrication-induced variations, making it unfeasible to predict the ADC reading at which the microring balances on the edge of instability. Therefore, we perform a calibration step before attempting to lock the microring to the pump laser, separating the feedback control scheme into three stages. First, a hot-to-cold sweep determines the ADC readings corresponding to the dark current and maximum photocurrent. Second, a quick reset to the hot state reinitializes the microring properly and a new hot-to-cold sweep brings it to the point at which the photocurrent starts increasing again. Third, a proportional–integral controller engages and regulates the photocurrent to just below the maximum value (95% of the way from the dark current to maximum photocurrent levels in the experiments reported here) by fine-tuning the heater DAC code, balancing the resonance on the edge of instability and leaving enough margin to reject thermal disturbances and
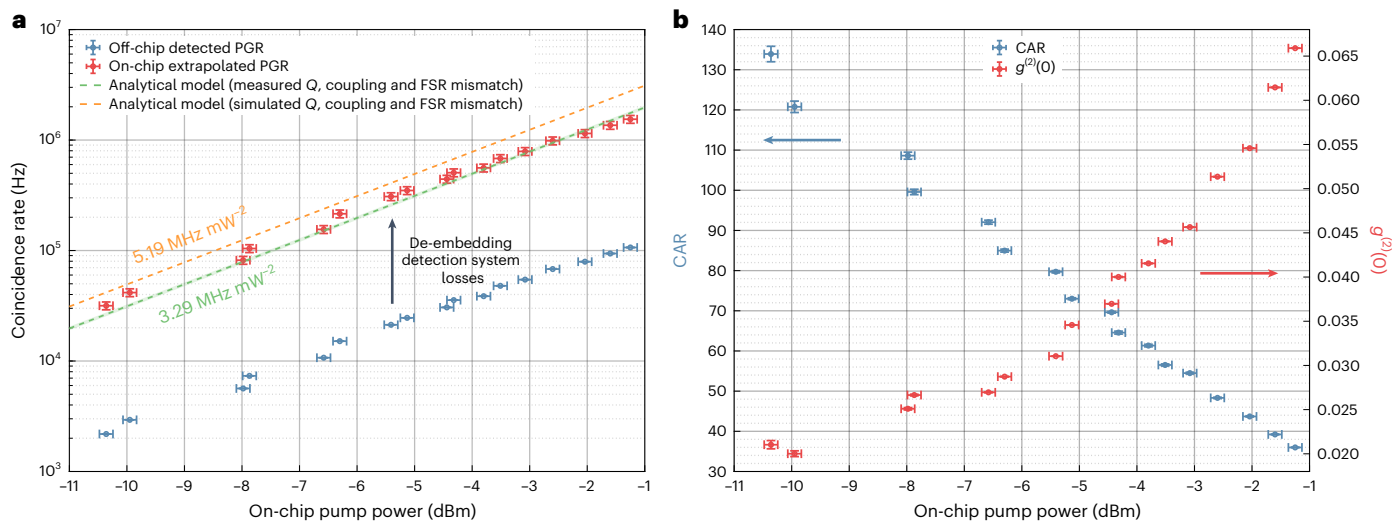
Fig. 3 | Quantum characterization of the SFWM photon-pair source with real-time feedback control. a, Plot of the coincidence rate detected at the SNSPDs and extrapolated on-chip PGR under feedback control versus the on-chip pump power at the input of the SFWM microring. Expected trends calculated using the analytical model described in Supplementary Section 1 are also plotted. The target design has $Q_{o,(s,p,i)} = 116.5 \times 10^3$, $Q_{e,(s,p,i)} = 87.4 \times 10^3$ and FSR mismatch of 1.98 GHz, yielding a predicted PGR efficiency of 5.19 MHz mW^{-2}. The fabricated microring on the tested die has parameters given in Fig. 2a, yielding a predicted PGR efficiency of 3.29 ± 0.13 MHz mW^{-2}, closely matching the extrapolated on-chip PGR. **b**, Plot of CAR and $g^{(2)}(0)$ versus on-chip pump power. The maximum measured CAR is 133.9 ± 1.9 and the corresponding $g^{(2)}(0)$ is 0.021 at 2.2-kHz off-chip coincidence rate (-31.7 kHz estimated on-chip PGR) with -10.4-dBm on-chip pump power assuming equal losses at each grating coupler $(3.0 \pm 0.1$ dB), which results in a total loss between SFWM microring and coincidence detection event of 14.5 ± 0.2 dB when accounting for all photon loss

mechanisms in the three SNSPD channels. The signal photons are sent through a 50/50 beamsplitter to enable $g^{(2)}$ measurements, and the detected off-chip coincidence rate includes counts from both signal channels; the full experimental setup is illustrated in Fig. 3. The maximum detected coincidence count rate is 106.6 kHz (-1.54-MHz estimated on-chip PGR) with a CAR of 36.0 ± 0.1 and $g^{(2)}(0)$ of 0.066 at an on-chip pump power of -1.2 dBm. We use a 320-ps-wide coincidence window $(\pm 2\sigma)$ for all the measurements reported here, with varying integration times from 70 s to 400 s depending on the pump power. The data points are presented as mean values of the plotted quantities over each integration window with the y-axis error bars being standard deviations derived from $\pm\sqrt{N}$ Poissonian photon-counting statistics, where N is the total number of detected events during each measurement's integration period. The x-axis error bars represent standard deviations in the calibrated on-chip pump power $(\pm 0.1$ dBm), derived from insertion loss measurements for each data point.

small variations in pump power from fibre alignment drift. A small deadband around the regulation point eliminates spurious dithering of the DAC code, allowing it to settle to a constant value. At this point, quantum-correlated photon pairs are generated via SFWM in the microring, separated from residual pump light using off-chip bandpass filters, and detected using a commercial SNSPD system with time-correlated single-photon counting. Figure 3a shows the raw detected photon-pair coincidence rate and the extrapolated on-chip PGR after de-embedding insertion losses and SNSPD detection efficiencies. Figure 3b shows the coincidences-to-accidentals ratio (CAR; which is the quantum signal-to-noise ratio) and the second-order correlation function $g^{(2)}(0)$ at the SNSPDs, demonstrating the single-photon nature of heralded photons from the source. We characterized the ability of the control system to stabilize the SFWM microring over approximately an order of magnitude in pump power ranging from -10.4 dBm to -1.2 dBm on chip, allowing the PGR–CAR trade-off to be tuned to the requirements of a given quantum system.

To demonstrate the effectiveness of the feedback controller in stabilizing SFWM as other photonic devices on the same die are thermally tuned, we created a worst-case thermal disturbance by rapidly pulsing the heater of a nearby inactive photon-pair source microring from a different interleaved system site located 325 µm away. Figure 4 shows a diagram of the experiment and time-domain waveforms of the photon-pair statistics during the calibration sequence, locking phase and thermal disturbances. The adjacent microring steps between the maximum and minimum heater settings, aggressively pushing the controlled microring's resonance closer to the point of instability by cooling it down. However, the action of the control loop prevents the lock from being lost since it responds faster than the slow timescale of thermal crosstalk through the chip substrate.

With -2.0-dBm on-chip pump power, the controller maintains a consistent off-chip pair rate of 38.6 ± 0.8 kHz and CAR of 42.0 ± 0.7 before and after the disturbance, with slight deviations during thermal transients. When the feedback is disabled and the heater DAC is set to a constant value, the same thermal disturbance causes a total loss of lock that cannot be restored without fully reinitializing the SFWM microring into the hot state and then cooling it back down again to meet the pump wavelength.

Stable photon-pair generation with many active microrings

For many microring-based photon-pair sources to operate together in an integrated system such as a multiplexed single-photon source[64] or a quantum information processor, they must all lock to a common laser wavelength with each microring stabilized against thermal crosstalk from calibrating and locking the others. Although we are limited to optically accessing only one on-chip photon source at a time by the placement of grating couplers and geometry of our fibre probes, we experimentally simulated the thermal environment of simultaneously locking all 12 SFWM microrings on our chip (Fig. 5a) to test the control system under realistic operating conditions. A microring near the centre of the array was first locked to the pump laser using the previously described procedure. Then, time-delayed versions of the recorded DAC waveform were replayed on all 11 other SFWM microrings on the same chip over the course of approximately an hour. This produces a similar thermal crosstalk profile to locking these sources: in reality, fabrication process variations will cause the final locked values of the heater DACs to vary among the microrings, but the largest and fastest thermal disturbances occur during the initial calibration phase. Figure 5b shows the time-domain waveforms from
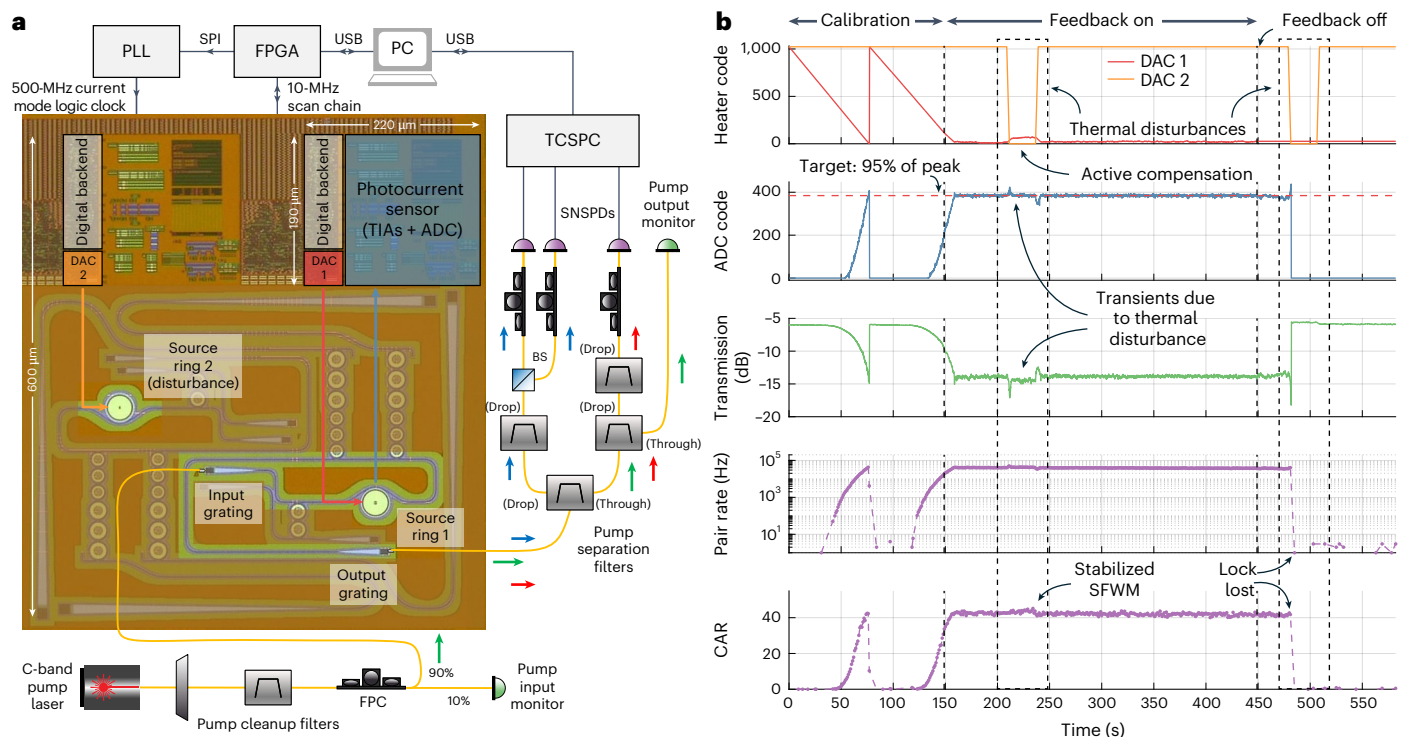
Fig. 4 | Experimental demonstration of feedback-controlled SFWM under thermal disturbances. a, Schematic of the experimental setup with active feedback control and off-chip pump filtering, highlighting active devices on the chip. A 50/50 beamsplitter added to the signal channel enables the $g^{(2)}(0)$ measurements shown in Fig. 3. TCSPC, time-correlated single-photon counting; TIA, transimpedance amplifier; BS, beamsplitter; PC, personal computer; PLL, phase-locked loop. **b**, Time-domain waveforms of the microring control experiment with −2.0-dBm on-chip pump power, locking to 95% of the maximum photocurrent reading on the ADC. We directly measure a CAR of 42.0 ± 0.7 and a PGR of 38.6 ± 0.8 kHz in one of the two signal channels after stabilizing SFWM in the microring, before de-embedding the chip coupling and detection system insertion losses. The first plot tracks the heater codes of the controlled microring (red) and an adjacent microring acting as a thermal aggressor (orange). The control heater DAC sweeps the microring from hot to cold for photocurrent

calibration and then reinitializes it hot before locking it at the determined target ADC code. Both CAR and coincidence count rate are observed to peak at resonance during the calibration phase and then stabilize as the DAC locks to the target ADC code. We plot the coincidence rate and CAR for only one of the signal channels in this case to better show the trends during the calibration step, since points are dropped when the fitting algorithm fails to converge for low numbers of total counts in the histogram and this would occur much more frequently if the results from the two channels were summed. Once calibration finishes, the aggressor heater DAC pulses the adjacent microring as strongly as possible, switching between the maximum and minimum heater codes, but the feedback loop maintains regulation with only slight variations observed in the ADC reading and pump transmission through the chip. On the other hand, when the feedback loop is disabled, the same disturbance causes a snap-off of the microring resonance from the pump laser, ending photon-pair generation.

this experiment. With −4.0-dBm initial on-chip bus-waveguide pump power, the controlled SFWM microring produces a stable off-chip pair rate of 16.9 ± 0.3 kHz with a CAR of 69.4 ± 2.0 as the feedback controller compensates for thermal crosstalk from the other heaters. Some variation in the pump laser transmission through the chip occurs due to drift in the alignment of the fibre probes, but the back off of the regulation point from the maximum photocurrent is sufficient to prevent a loss of lock (and such variations would not occur in a fully packaged die with a permanently glued fibre array (Supplementary Section 5)). This experiment proves the ability of our integrated feedback control approach to enable the next generation of large-scale quantum-photonic systems on chip to benefit from the advantages of microring-based photon sources.

Conclusions

We have reported an electronic–photonic quantum system-on-chip that enables scalable control of microring resonator quantum photon-pair sources through the monolithic integration of silicon quantum photonics with complex control electronics on the same die. Despite the extreme temperature sensitivity of high-Q silicon microrings, this system operates robustly without external stabilization from a thermoelectric cooler, simplifying chip packaging. The approach accounts for nonlinear effects present in such cavities, such as two-photon absorption and self-heating, permitting them to be stabilized at high

pump laser powers. Local feedback around each microring also avoids the complexity of thermal crosstalk cancellation schemes requiring detailed modelling and characterization of crosstalk among all devices on the same die[65,66], which is yet to be demonstrated in nonlinear systems with microrings exhibiting self-heating or thermal bistability.

Although the on-chip circuits are already compact, the fast -60-kHz-sampling-rate capability of the integrated photocurrent sensor means that the same circuit block could be time-multiplexed to control many microrings, requiring only the much smaller heater DAC and digital controller subcircuits to be duplicated (a detailed analysis of area scaling with multiplexed sensing is provided in Supplementary Section 3). Thus, in future systems with tens to hundreds of controlled microrings, the area overhead of the circuits can be much lower relative to the area of the photonics. This is essential for maximizing the benefits of photonic integration as future silicon quantum photonic systems approach the reticle-size limit (typically 26 mm × 33 mm in modern CMOS tooling) and eventually the wafer-size limit through tiling and reticle stitching[67,68].

Our use of a commercial CMOS foundry, which is geared towards high-yield volume production, makes it possible to build large-scale quantum systems for which the small footprint and high performance of microring sources is crucial. Furthermore, the recent introduction of a CMOS process (GlobalFoundries 45SPCLO[5]) with native support
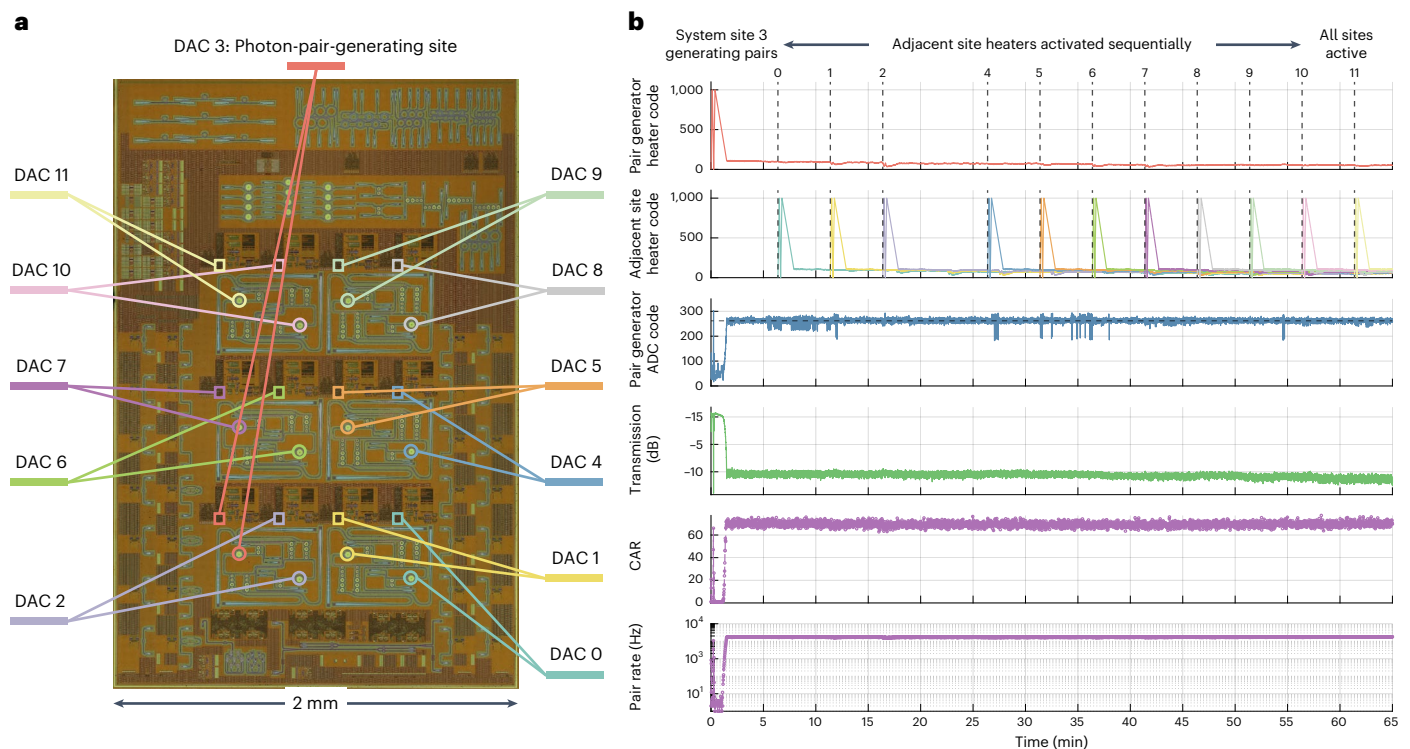
Fig. 5 | Simultaneous operation of many photon-pair sources on a single chip. **a**, Micrograph of 12 SFWM microring control systems on the chip, with each DAC and microring highlighted in the colour of the corresponding DAC code plot. **b**, Time-domain measurement of photon-pair generation in SFWM microring no. 3, whereas the 11 adjacent sites are activated sequentially with delayed heater DAC waveforms over the course of an hour, emulating the operation of many photon-pair sources on the same chip. This experiment comprises >3,900 photon-pair histograms. The off-chip detected PGR is 16.9 ± 0.3 kHz and CAR is 69.4 ± 2.0 with −4.0-dBm on-chip pump power.

for the monolithic integration of photonics and electronics without requiring any post-processing or hacking of foundry design layers makes our control approach broadly accessible. With its almost two times thicker SOI layer improving the mode confinement in the silicon core and lower-loss dielectric layer stack, our preliminary 45SPCLO device measurements (Supplementary Section 1) predict that optimized microring photon-pair sources in 45SPCLO could achieve an efficiency of ~5.6 GHz mW^{-2} given their measured intrinsic Q factors of ~0.8×10^6, a 1,000 times improvement over the results here. Tighter mode confinement can also improve the CAR by reducing noise from spontaneous Raman scattering in amorphous cladding materials.

An alternative way to scale up the control circuits is to use advanced packaging techniques such as die stacking, wafer bonding or silicon interposers to bridge separate silicon photonics and control electronics chips together with a high density of electrical interconnects. These approaches are already used in the microelectronics industry for high-end or high-volume commercial products[69–71], but in a research and development setting, they are costly and inaccessible compared with monolithic integration. With our approach, a whole quantum-photonic system can be designed in a single electronic design automation tool flow, fabricated in a single tapeout, and packaged using standard flip-chip bonding to a printed circuit board. This paradigm could lead to rapid advances in the complexity of chip-scale quantum-photonic systems.

Methods

Chip implementation
Photonic device layouts were created using Berkeley Photonics Generator, an open-source Python tool for programmatic integrated photonics chip layout available at https://github.com/BerkeleyPhotonicsGenerator/BPG. Data preparation into process-specific mask design layers compliant with the CMOS foundry's geometric design rules (consisting of over 8,000 checks) was then performed using Siemens Calibre software. Custom high-density fill shapes were placed on the silicon and lower metal layers with ~2.5-μm clearance around all the photonic waveguides to meet the density requirements for chemical–mechanical polishing, and avoiding optical losses that would be caused by the default foundry density fill profile. These shapes also reduce dishing effects originating in the low-density photonics regions that could otherwise impact the yield of nearby transistors. The specific data preparation parameters we used are based on proprietary foundry information, which is available to customers under a non-disclosure agreement. The analogue and mixed-signal circuits within the photocurrent sensor were designed using the Berkeley Analog Generator, another open-source Python tool for programmatic CMOS circuit design that wraps around Cadence Virtuoso, a standard commercial tool for integrated circuit design, to automate design and layout tasks. It is available at https://github.com/ucb-art/BAG_framework. Digital electronics design and top-level chip assembly were then performed using commercial digital synthesis and place-and-route tools from Cadence to produce the final chip design. Finally, physical verification of the full design was performed using Siemens Calibre design rule checking and layout versus schematic comparison software before sending the designs to the foundry.

Chip fabrication
The chips were fabricated as part of a multiproject wafer run on the GlobalFoundries 45RFSOI process sponsored by Ayar Labs. Some optional (non-critical) design rules were waived by the foundry, since the photonics layout contains geometric features that would reduce the performance or yield of transistors, for which the rule deck is optimized, but do not adversely affect the photonic devices.

Nonetheless, transistors were fabricated in close proximity (within 10 μm) of photonics regions without any loss of functionality observed in over 20 chips tested. Otherwise, the mask designs were treated in exactly the same way as standard electronics-only designs and processed using the ordinary manufacturing flow of the foundry. The electrical pads on the wafers were plated with Cu pillars placed at a 250-μm pitch within the multiproject wafer chip area to enable electrical connections.

Electrical packaging and photonics enablement

Once diced, the chips were flip-chip soldered onto a six-layer FR-4 high-density-interconnect printed circuit board manufactured by Candor Industries. The chips were underfilled with epoxy after soldering for improved mechanical stability. To enable photonics functionality, the entire handle substrate of each packaged chip was removed in a single post-processing step using a XeF_2 dry etching tool (Xactix Xetch) in the Marvell Nanofabrication Laboratory at the University of California Berkeley, an approach we previously developed for integrating classical photonic links into CMOS microprocessors[44,46]. The thin (<200 nm) buried oxide layer in the 45RFSOI CMOS process would otherwise lead to excessive waveguide mode leakage into the Si substrate—a problem not encountered in conventional silicon photonics wafers with 2–3-μm-thick buried oxide. This layer, on which the silicon layer with transistors and photonic devices sits, acts as an etch stop that prevents them from being removed from the back side along with the silicon handle. In this process, the performance of electronics was not affected by the removal of the silicon handle, circumventing the need to mask off the circuits and selectively etch only the photonics regions. Lithographic masking to contain the etch in this way does, however, improve heatsinking of the circuits and mechanical reliability of the chip, and has been implemented at wafer scale for volume production of photonic link chiplets in the same CMOS process[48,49].

Electro-optical testing

Light was coupled in and out of the packaged and etched chips using tapered and lensed fibres from OZ Optics with a 5-μm spot size matching the mode-field diameter of the VGCs. The fibres were held on custom-machined holders attached to three-axis Thorlabs NanoMax positioners and manually aligned to the VGCs under a microscope with a long-working-distance metallurgical objective (10X Mitutoyo Plan Apo), selected to allow sufficient clearance for the fibre holders. A Keysight 81608A C-band-tunable laser source with a continuous sweep synchronized to an Agilent 81635A InGaAs optical power sensor was used for optical transmission characterization of the photonics and initial bring-up and testing of the electronic circuits. The Q factors and free spectral ranges (FSRs) reported in Fig. 2 and Supplementary Section 1 were measured by locally fitting Lorentzian curves to the signal, pump and idler resonances with several varying on-chip powers of roughly −20 dBm to −50 dBm to provide reasonable estimates of uncertainty and avoiding distortion from self-heating at higher laser powers.

Since the tuning range of the microrings is less than their FSR, arbitrary pump wavelengths cannot be supported. Instead, a pump laser wavelength is chosen around 0.25 nm to 0.5 nm longer than the measured SFWM microring resonance wavelength after performing a transmission sweep. The low tuning range of the SFWM microrings was caused by a correctable design bug in the heater layout code that caused the entire microring to be filled with a disc-shaped heater instead of a narrower track near the waveguide, reducing the thermal tuning efficiency. Corrections to this issue that have been implemented on subsequent chip tapeouts are described in Supplementary Section 2.

Feedback controller implementation

In the experiments reported here, we read out and control the on-chip ADC and DAC through a serial scan chain interface from an external field-programmable gate array (FPGA), bypassing the on-chip digital feedback control circuits to allow the full customization of the tuning algorithm. The FPGA relays commands to a personal computer through a USB interface, allowing arbitrary control algorithms and command sequences to be executed using Python code. The controller we implemented can later be hardened to custom logic in future chips; given the simplicity of our three-step finite-state machine controller, it can easily fit in the same area as the existing circuit (which is similar in nature, but cannot lock as close to the maximum photocurrent due to some hard-coded parameters). The long latency of the FPGA to Python software interface limits the control loop update rate to ~10 Hz when running from Python code; this could be improved to ~2 kHz by implementing the same algorithms on the FPGA directly (limited by the 10-MHz scan clock and 4,674-bit length of the scan chain), or ~60 kHz with fully custom logic on the chip operating at the ADC sample rate (including a 512× on-chip averaging filter we used here to reduce noise).

Single-photon measurements

A Pure Photonics PPCL200 low-noise micro-integrable tunable laser assembly was used as the pump in the single-photon-counting experiments. It was routed through a three-paddle manual fibre polarization controller (FPC) to a set of fibre-coupled bandpass (channel add–drop) thin-film filters with >100-dB extinction in aggregate at the signal and idler wavelengths to filter out the noise from amplified spontaneous emission (ASE) in the laser and spontaneous Raman scattering in the fibre connecting the laser to the input of this filter (Raman noise generated after this filter is not attenuated). The input laser power to the chip was monitored through the 10% tap of a 90:10 power splitter between the filter and the lensed fibre probe coupled to the input VGC. Estimated on-chip pump powers are reported by accounting for the insertion loss of the input VGC. Light transmitted through the chip was collected by a second lensed fibre coupled to an output VGC and sent to an AC Photonics 1 × 2 dense wavelength-division multiplexing channel-dropping filter with a 100-GHz-wide passband centred at 1,545.3 nm (ITU grid channel C40) to extract the signal photons onto its 'pass' port. The signals photons are detected on a pair of SNSPDs after a 50:50 beamsplitter to enable $g^{(2)}$ measurements. A second identical filter was cascaded in the signal photon path to provide a total of >120-dB isolation of the residual pump light. The idler and residual pump photons exiting the 'reflect' port of the first dense wavelength-division multiplexing filter were connected to a different pair of cascaded dense wavelength-division multiplexings with a 100-GHz-wide passband centred at 1,559.8 nm (ITU grid channel C22). These filters route the idler photons to their 'pass' port (also with >120 dB of isolation of the residual pump) and route the residual pump to the reflect port, which is connected to a Thorlabs S154C photodiode to measure the pump laser transmission through the chip, which is used to estimate the VGC insertion losses. The input FPC is adjusted to maximize the pump transmission through the chip before aligning the SFWM microring, since the VGCs efficiently couple a single polarization of light. With the SFWM microring aligned, signal and idler photons are detected using three channels of a Quantum Opus One SNSPD system, which operates the single-photon detectors in a 2.4-K cryostat. This system also requires manual FPC adjustments on each channel to maximize the photon detection efficiency. The photon detection efficiencies of the idler and two signal SNSPD channels, including fibre and FPC losses, were characterized using variably attenuated laser light to be 63%, 77% and 74%, respectively. The various manual FPC adjustments could be eliminated in a packaged system with polarization maintaining fibres.

Coincidence count analysis

Photon detection events from the SNSPDs were recorded using a Swabian Instruments Time Tagger 20 time-correlated single-photon-counting system that collected time stamps of trigger events with 1-ps time-bin quantization. The time stamps were then processed using

the 'start–stop' measurement software provided with the instrument to produce a histogram of time-of-arrival differences between the signal and idler photons. The timing jitters of the signal and idler SNSPDs were characterized by the manufacturer to be ~80 ps and the timing jitter of the time tagger is 35 ps. We observed histograms with coincidence peaks having much wider widths in time, which we attribute primarily to the time uncertainty corresponding to the linewidth (photon energy uncertainty) of the SFWM process in the microring; ref. [32] provides a detailed discussion of how the timing uncertainty of single-photon detection interacts with the cavity linewidth. To extract the PGR and CAR from a given histogram, we fitted an offset Gaussian (a good approximation of the convolution of the three different sources of timing uncertainty) within ±0.8 ns of the coincidence peak. We then used a 320-ps-wide coincidence window (roughly ±2σ, kept constant throughout all the measurements) to extract the total numbers of coincidences and accidentals, and compute their ratio (the CAR)[72]. The PGR is then defined as the ratio of the coincidences to the integration time of the histogram, and the PGR and the corresponding CAR can be traded off by varying the choice of coincidence window (although there is no single correct choice, we have picked a standard one here).

To verify the quantum nature of our source and characterize multi-pair emissions, we measure the conditional second-order correlation function $g^{(2)}(0)$ using a standard three-detector setup[73]. We first perform correlation measurements between the idler and two signal channels to determine their relative delays. After digitally compensating for those delays, we use the same 320-ps coincidence window as that used for measuring the CAR and PGR. We then compute the time-integrated $g^{(2)}(0)$ using the following expression: $g^{(2)}(0) = N_{I,S1,S2}N_I/N_{I,S1}N_{I,S2}$, where $N_{I,S1,S2}$ is the number of threefold coincidences between the signal channels and the idler; N_I is the number of single counts in the idler detector; and $N_{I,S1}$ and $N_{I,S2}$ are the numbers of twofold coincidences between the idler and the individual signal channels, respectively.

Potential for on-chip pump filtering and SNSPD integration

The experiments reported here relied on an external pump ASE cleanup filter at the input side and external pump rejection and signal–idler demultiplexing filters on the output side to isolate the photon pairs generated in the SFWM microring from noise and residual pump light. They were then detected by off-chip SNSPDs in a cryostat separate from the rest of the system operating at room temperature. Ultimately, large-scale quantum systems will need to include these functions on a single chip to fully realize the benefits of an integrated platform with single-photon sources and detectors. Supplementary Section 4 reviews and discusses possible routes for integrating SNSPDs and prospects for operating CMOS circuits and thermally tuned microring resonators at the requisite few-kelvin cryogenic temperatures for SNSPD compatibility. Furthermore, we previously showed that high-order cascaded microring filters located on the same chip as an SFWM source can achieve the large (>95 dB) levels of stopband rejection required for these applications[51]. On the basis of the measured microring Q factors, these types of filter could also achieve state-of-the-art (<1 dB) passband insertion losses if actively aligned to compensate for process variations. We included such filters (with fourth- and sixth-order cascaded microring variants) along with tuning circuits on this chip.

Extended Data Fig. 1 shows a measurement of the >100-dB contrast between the passband and stopband needed for on-chip filtering, consistent with our previous results using this platform. However, correctable design bugs limited the tuning range of these filters, as well as nominally placing the signal and idler passbands at the same wavelength, instead of nominally placing them two FSRs of the SFWM microring apart. This prevented them from being aligned for such a system demonstration, and they were bypassed. We also bypassed an included second-order cascaded microring filter with 40 dB of stopband rejection intended for pump cleanup because we found that the large ASE noise of the available pump laser source (Pure Photonics PPCL200) required a much higher degree of stopband rejection for a coincidence peak to be observable above the noise floor. In the future, a higher-order filter can be used for pump cleanup and the initial (unaligned) wavelengths of the signal and idler separation filters can be placed closer to the relevant resonance wavelengths of the SFWM microring to enable the alignment of a fully integrated photon-pair generation system without external filtering.

Data availability
Datasets generated during the current study are available from the corresponding authors upon reasonable request.

References

1. Rudolph, T. Why I am optimistic about the silicon-photonic route to quantum computing. *APL Photon.* **2**, 030901 (2017).
2. Wang, J., Sciarrino, F., Laing, A. & Thompson, M. G. Integrated photonic quantum technologies. *Nat. Photon.* **14**, 273–284 (2020).
3. Adcock, J. C. et al. Advances in silicon quantum photonics. *IEEE J. Sel. Topics Quantum Electron.* **27**, 1–24 (2020).
4. Giewont, K. et al. 300-mm monolithic silicon photonics foundry technology. *IEEE J. Sel. Topics Quantum Electron.* **25**, 8200611 (2019).
5. Rakowski, M. et al. 45nm CMOS-silicon photonics monolithic technology (45CLO) for next-generation, low power and high speed optical interconnects. In *Optical Fiber Communication Conference (OFC) 2020, OSA Technical Digest* T3H.3 (Optica Publishing Group, 2020).
6. Sharping, J. E. et al. Generation of correlated photons in nanoscale silicon waveguides. *Opt. Express* **14**, 12388–12393 (2006).
7. Harada, K.-i et al. Generation of high-purity entangled photon pairs using silicon wire waveguide. *Opt. Express* **16**, 20368–20373 (2008).
8. Clemmen, S. et al. Continuous wave photon pair generation in silicon-on-insulator waveguides and ring resonators. *Opt. Express* **17**, 16558–16570 (2009).
9. PsiQuantum team. A manufacturable platform for photonic quantum computing. *Nature* **641**, 876–883 (2025).
10. Bian, Y. et al. 3D integrated laser attach technology on a 300-mm monolithic CMOS silicon photonics platform. *IEEE J. Sel. Topics Quantum Electron.* **29**, 8200519 (2023).
11. Mahmudlu, H. et al. Fully on-chip photonic turnkey quantum source for entangled qubit/qudit state generation. *Nat. Photon.* **17**, 518–524 (2023).
12. Kim, J.-H. et al. Hybrid integration of solid-state quantum emitters on a silicon photonic chip. *Nano Lett.* **17**, 7394–7400 (2017).
13. Katsumi, R. et al. Quantum-dot single-photon source on a CMOS silicon photonic chip integrated using transfer printing. *APL Photon.* **4**, 036105 (2019).
14. Larocque, H. et al. Tunable quantum emitters on large-scale foundry silicon photonics. *Nat. Commun.* **15**, 5781 (2024).
15. Eltes, F. et al. A BaTiO₃-based electro-optic Pockels modulator monolithically integrated on an advanced silicon photonics platform. *J. Lightwave Technol.* **37**, 1456–1462 (2019).
16. Eltes, F. et al. An integrated optical modulator operating at cryogenic temperatures. *Nat. Mater.* **19**, 1164–1168 (2020).
17. Wang, X., Valdez, F., Mere, V. & Mookherjea, S. Monolithic integration of 110 GHz thin-film lithium niobate modulator and high-Q silicon microring resonator for photon-pair generation. In *2022 Conference on Lasers and Electro-Optics (CLEO)* 1–2 (IEEE, 2022).
18. Wang, X., Mere, V., Valdez, F. & Mookherjea, S. Integrated electro-optic control of biphoton generation using hybrid photonics. *Opt. Quantum* **1**, 19–25 (2023).

19. Pernice, W. H. et al. High-speed and high-efficiency travelling wave single-photon detectors embedded in nanophotonic circuits. *Nat. Commun.* **3**, 1325 (2012).

20. Akhlaghi, M. K., Schelew, E. & Young, J. F. Waveguide integrated superconducting single-photon detectors implemented as near-perfect absorbers of coherent radiation. *Nat. Commun.* **6**, 8233 (2015).

21. Najafi, F. et al. On-chip detection of non-classical light by scalable integration of single-photon detectors. *Nat. Commun.* **6**, 5873 (2015).

22. Carolan, J. et al. Scalable feedback control of single photon sources for photonic quantum technologies. *Optica* **6**, 335–340 (2019).

23. Caspani, L. et al. Integrated sources of photon quantum states based on nonlinear optics. *Light Sci. Appl.* **6**, e17100 (2017).

24. Savanier, M., Kumar, R. & Mookherjea, S. Photon pair generation from compact silicon microring resonators using microwatt-level pump powers. *Opt. Express* **24**, 3313–3328 (2016).

25. Silverstone, J. W. et al. Qubit entanglement between ring-resonator photon-pair sources on a silicon chip. *Nat. Commun.* **6**, 7948 (2015).

26. Faruque, I. I., Sinclair, G. F., Bonneau, D., Rarity, J. G. & Thompson, M. G. On-chip quantum interference with heralded photons from two independent micro-ring resonator sources in silicon photonics. *Opt. Express* **26**, 20379–20395 (2018).

27. Lu, L. et al. Three-dimensional entanglement on a silicon chip. *npj Quantum Inf.* **6**, 30 (2020).

28. Llewellyn, D. et al. Chip-to-chip quantum teleportation and multi-photon entanglement in silicon. *Nat. Phys.* **16**, 148–153 (2020).

29. Arrazola, J. M. et al. Quantum circuits with many photons on a programmable nanophotonic chip. *Nature* **591**, 54–60 (2021).

30. Wang, J. et al. Multidimensional quantum entanglement with large-scale integrated optics. *Science* **360**, 285–291 (2018).

31. Bao, J. et al. Very-large-scale integrated quantum graph photonics. *Nat. Photon.* **17**, 573–581 (2023).

32. Yard, P. et al. On-chip quantum information processing with distinguishable photons. *Phys. Rev. Lett.* **132**, 150602 (2024).

33. Horikawa, T. et al. Resonant wavelength variation modelling for microring resonators based on fabrication deviation analysis. In *2017 European Conference on Optical Communication (ECOC)* 1–3 (IEEE, 2017).

34. Jayatilleka, H. et al. Post-fabrication trimming of silicon photonic ring resonators at wafer-scale. *J. Lightwave Technol.* **39**, 5083–5088 (2021).

35. Dinu, M., Quochi, F. & Garcia, H. Third-order nonlinearities in silicon at telecom wavelengths. *Appl. Phys. Lett.* **82**, 2954–2956 (2003).

36. Soref, R. A. & Bennett, B. R. Electrooptical effects in silicon. *IEEE J. Quantum Electron.* **23**, 123–129 (1987).

37. Almeida, V. R. & Lipson, M. Optical bistability on a silicon chip. *Optics Lett.* **29**, 2387–2389 (2004).

38. Priem, G. et al. Optical bistability and pulsating behaviour in silicon-on-insulator ring resonator structures. *Opt. Express* **13**, 9623–9628 (2005).

39. Sun, C. et al. A 45 nm CMOS-SOI monolithic photonics platform with bit-statistics-based resonant microring thermal tuning. *IEEE J. Solid-State Circuits* **51**, 893–907 (2016).

40. Guo, K. et al. Nonclassical optical bistability and resonance-locked regime of photon-pair sources using silicon microring resonator. *Phys. Rev. Appl.* **11**, 034007 (2019).

41. Xu, Q. & Lipson, M. Carrier-induced optical bistability in silicon ring resonators. *Opt. Lett.* **31**, 341–343 (2006).

42. Johnson, T. J., Borselli, M. & Painter, O. Self-induced optical modulation of the transmission through a high-Q silicon microdisk resonator. *Opt. Express* **14**, 817–831 (2006).

43. Chen, S., Zhang, L., Fei, Y. & Cao, T. Bistability and self-pulsation phenomena in silicon microring resonators based on nonlinear optical effects. *Opt. Express* **20**, 7454–7468 (2012).

44. Stojanović, V. et al. Monolithic silicon-photonic platforms in state-of-the-art CMOS SOI processes. *Opt. Express* **26**, 13106–13121 (2018).

45. Orcutt, J. S. et al. Open foundry platform for high-performance electronic-photonic integration. *Opt. Express* **20**, 12222–12232 (2012).

46. Sun, C. et al. Single-chip microprocessor that communicates directly using light. *Nature* **528**, 534–538 (2015).

47. Sun, C. et al. TeraPHY: an O-band WDM electro-optic platform for low power, terabit/s optical I/O. In *2020 IEEE Symposium on VLSI Technology* 1–2 (IEEE, 2020).

48. Wade, M. et al. TeraPHY: a chiplet technology for low-power, high-bandwidth in-package optical I/O. *IEEE Micro* **40**, 63–71 (2020).

49. Wade, M. et al. An error-free 1 Tbps WDM optical I/O chiplet and multi-wavelength multi-port laser. In *Optical Fiber Communication Conference (OFC) 2021* F3C.6 (Optica Publishing Group, 2021).

50. Gentry, C. M. et al. Quantum-correlated photon pairs generated in a commercial 45 nm complementary metal-oxide semiconductor microelectronic chip. *Optica* **2**, 1065–1071 (2015).

51. Gentry, C. M. et al. Monolithic source of entangled photons with integrated pump rejection. In *Conference on Lasers and Electro-Optics, OSA Technical Digest* JTh4C.3 (Optica Publishing Group, 2018).

52. Wade, M. T. et al. 75% efficient wide bandwidth grating couplers in a 45 nm microelectronics CMOS process. In *2015 IEEE Optical Interconnects Conference (OI)* 46–47 (IEEE, 2015).

53. Notaros, J. et al. Ultra-efficient CMOS fiber-to-chip grating couplers. In *2016 Optical Fiber Communications Conference and Exhibition (OFC)* 1–3 (IEEE, 2016).

54. Atabaki, A. H., Meng, H., Alloatti, L., Mehta, K. K. & Ram, R. J. High-speed polysilicon CMOS photodetector for telecom and datacom. *Appl. Phys. Lett.* **109,** 111106 (2016).

55. Hosseini, E. S., Yegnanarayanan, S., Atabaki, A. H., Soltani, M. & Adibi, A. Systematic design and fabrication of high-Q single-mode pulley-coupled planar silicon nitride microdisk resonators at visible wavelengths. *Opt. Express* **18**, 2127–2136 (2010).

56. Shainline, J. M. et al. Depletion-mode carrier-plasma optical modulator in zero-change advanced CMOS. *Opt. Lett.* **38**, 2657–2659 (2013).

57. Grillanda, S. & Morichetti, F. Light-induced metal-like surface of silicon photonic waveguides. *Nat. Commun.* **6**, 8182 (2015).

58. Alloatti, L. & Ram, R. J. Resonance-enhanced waveguide-coupled silicon-germanium detector. *Appl. Phys. Lett.* **108**, 071105 (2016).

59. Ong, J. R., Kumar, R., Aguinaldo, R. & Mookherjea, S. Efficient CW four-wave mixing in silicon-on-insulator micro-rings with active carrier removal. *IEEE Photon. Technol. Lett.* **25**, 1699–1702 (2013).

60. Savanier, M., Kumar, R. & Mookherjea, S. Optimizing photon-pair generation electronically using a p-i-n diode incorporated in a silicon microring resonator. *Appl. Phys. Lett.* **107**, 131101 (2015).

61. Gray, D. et al. Thermo-optic multistability and relaxation in silicon microring resonators with lateral diodes. *Phys. Rev. Appl.* **14**, 024073 (2020).

62. Xie, Y. et al. Thermally-reconfigurable silicon photonic devices and circuits. *IEEE J. Sel. Topics Quantum Electron.* **26**, 3600220 (2020).

63. Sun, C., Timurdogan, E., Watts, M. R. & Stojanović, V. Integrated microring tuning in deep-trench bulk CMOS. In *2013 Optical Interconnects Conference* 54–55 (IEEE, 2013).

64. Collins, M. J. et al. Integrated spatial multiplexing of heralded single-photon sources. *Nat. Commun.* **4**, 2582 (2013).

65. Milanizadeh, M., Aguiar, D., Melloni, A. & Morichetti, F. Canceling thermal cross-talk effects in photonic integrated circuits. *J. Lightwave Technol.* **37**, 1325–1332 (2019).

66. Gurses, B. V., Fatemi, R., Khachaturian, A. & Hajimiri, A. Large-scale crosstalk-corrected thermo-optic phase shifter arrays in silicon photonics. *IEEE J. Sel. Topics Quantum Electron.* **28**, 6101009 (2022).

67. Seok, T. J., Kwon, K., Henriksson, J., Luo, J. & Wu, M. C. Wafer-scale silicon photonic switches beyond die size limit. *Optica* **6**, 490–494 (2019).

68. Jin, W., Feshali, A., Paniccia, M. & Bowers, J. E. Seamless multi-reticle photonics. *Opt. Lett.* **46**, 2984–2987 (2021).

69. Lau, J. H. Recent advances and trends in advanced packaging. *IEEE Trans. Compon. Packag. Manuf. Technol.* **12**, 228–252 (2022).

70. Shekhar, S. et al. Roadmapping the next generation of silicon photonics. *Nat. Commun.* **15**, 751 (2024).

71. Mahajan, R. et al. Embedded multidie interconnect bridge—a localized, high-density multichip packaging interconnect. *IEEE Trans. Compon. Packag. Manuf. Technol.* **9**, 1952–1962 (2019).

72. Bienfang, J. C. et al. Single-photon sources and detectors dictionary (US Department of Commerce, National Institute of Standards and Technology, 2023).

73. Beck, M. Comparing measurements of $g^{(2)}(0)$ performed with different coincidence detection techniques. *J. Opt. Soc. Am. B* **24**, 2972–2978 (2007).

74. Cabanillas, J. F. et al. Monolithically integrated high-order vernier filters and tuning circuits for electronic-photonic quantum system-on-chip. In *Conference on Lasers and Electro-Optics, Technical Digest Series* STh4H.4 (Optica Publishing Group, 2022).

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Author contributions

I.W. and J.M.F.C. designed the photonic components. D.K. and I.W. designed the electronic–photonic system layout. D.K., S.B., C.A. and P.Z. designed the on-chip electronic circuits. S.B. created and supported the electronic–photonic chip design infrastructure and tool flow. D.K. performed the system integration; package design, control firmware and software development; and initial hardware bring-up. D.K., A.R. and Ð.G. collected and analysed the classical electro-optical characterization data. A.R. developed and performed the quantum characterization experiments, and D.K. contributed the data analysis code. A.R. and D.K. conceptualized and conducted the system-level demonstrations. I.W., Ð.G., D.K. and A.R. developed and validated the photon-pair source device model. The paper was prepared by D.K., A.R., I.W. and Ð.G. D.K., A.R. and I.W. created the figures. All authors contributed to the review of the paper. M.A.P., P.K. and V.M.S. supervised and conceptualized the project. These authors contributed equally: D.K., I.W. and A.R.

Competing interests

The authors declare no competing interests.

Additional information

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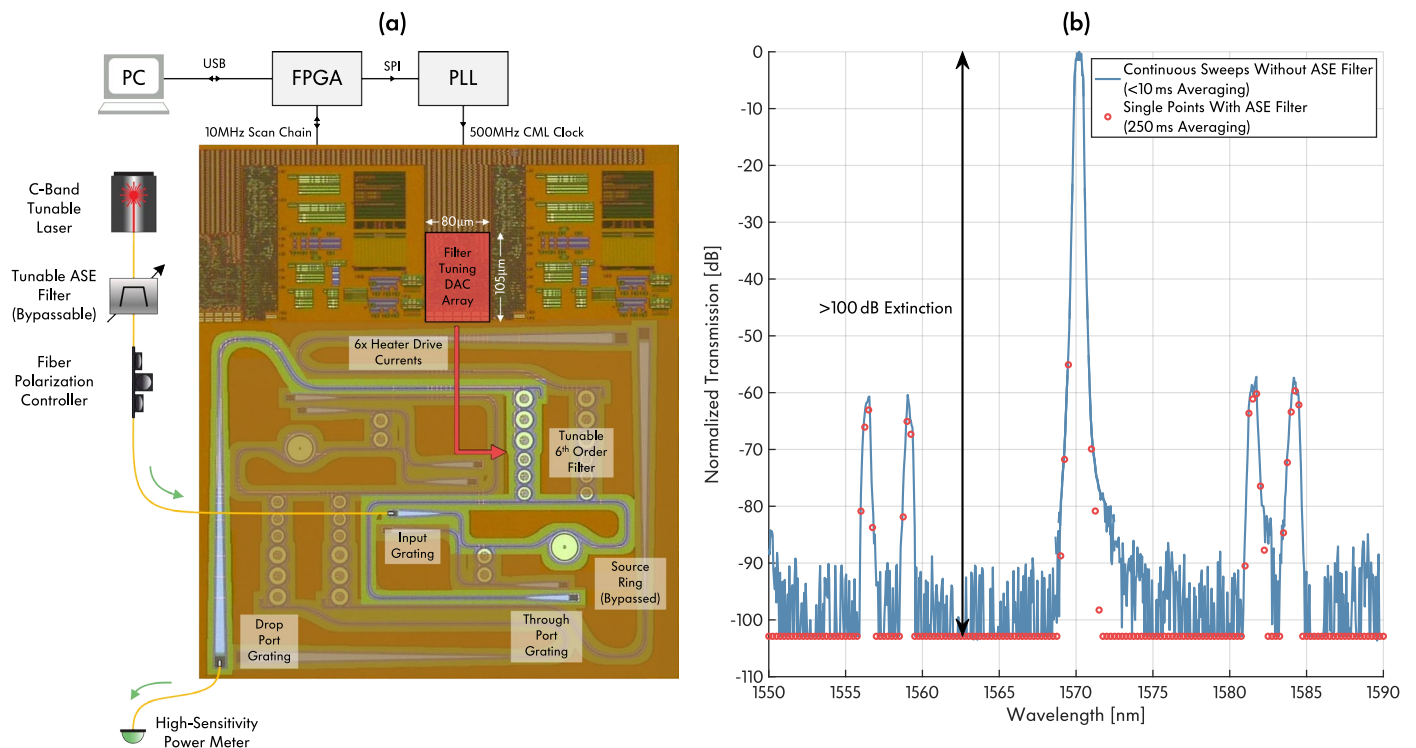
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Extended Data Fig. 1 | High-Extinction Pump Rejection Filter. (a) Measurement setup for characterizing the extinction ratio of the integrated pump rejection filters. The filters are aligned by using an EDFA in place of the tunable laser to intentionally generate broadband ASE noise, and then maximizing the drop port power meter readings using a Nelder-Mead optimization algorithm. The tunable laser is then swapped back in to take a transmission spectrum. **(b)** Normalized transmission spectrum of input to drop port response of the aligned filter using a series of stitched continuous sweeps with varying power meter range settings (blue curve) showing ~ 95 dB extinction that is limited by ASE noise of the laser source passing through the aligned passband. When an external ASE filter is enabled and the integration time is increased, the noise floor falls below the minimum detectable level of the power meter, indicating > 100 dB extinction at an offset wavelength of one FSR of the photon-pair source, which is required

for fully on-chip pump filtering (red points). The filter uses a Vernier scheme to extend the FSR, resulting in less extinction (~ 60 dB) at the FSRs of the cascaded sub-filters, which are selected not to align with either the pump laser or other single-photon channel when the pump rejection filter is aligned to a particular signal or idler output wavelength. Limited heater tuning range prevented the on-chip filters from being aligned to a photon-pair source resonance wavelength on all tested chips, which is correctable by improving the source and filter heater designs and slightly adjusting the microring radii to target specific resonance wavelengths, reducing the initial error between the source and filter resonances. We have characterized the insertion loss of this filter to be < 1 dB using measurements at a separate test site with through port and drop port grating couplers oriented in the same direction, allowing the same fiber to measure both ports one at a time[74].