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Epitaxial growth of antiphase boundary free GaAs layer on 300 mm Si(001) substrate by metalorganic chemical vapour deposition with high mobility

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Metal organic chemical vapor deposition of GaAs on standard nominal 300 mm Si(001) wafers was studied. Antiphase boundary (APB) free epitaxial GaAs films as thin as 150 nm were obtained. The APB-free films exhibit an improvement of the room temperature photoluminescence signal with an increase of the intensity of almost a factor 2.5. Hall effect measurements show an electron mobility enhancement from 200 to 2000 cm^2/V s. The GaAs layers directly grown on industrial platform with no APBs are perfect candidates for being integrated as active layers for nanoelectronic as well as optoelectronic devices in a CMOS environment. © *2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).* [http://dx.doi.org/10.1063/1.4945586]

In the last decade, a growing research interest is again observed on III-V materials integration on silicon. Indeed, the electronic and optoelectronic properties of arsenides and phosphides semiconductors make them interesting to boost the performances of integrated circuits.[1–3] In the past, GaAs was probably one of the most studied materials as it has demonstrated abilities for high-speed and high power applications,[4,5] laser diodes and RF devices for optical network and communications[4,6,7] thanks to high mobility and direct bandgap properties. Co-integration of these functionalities with Si CMOS logic will open up the route of designing new systems. For a monolithic integration, direct epitaxy of GaAs on Si(001) is required. However, despite 3 decades of research to grow a high quality III-V layer on silicon substrates, there are still challenges to be solved. The first challenge is the lattice mismatch between silicon and gallium arsenide (4.1%), which induces the formation of crystalline defects to accommodate the strain in the material. To reduce crystalline defects density, various smart improvements have been investigated like post-growth thermal cycle annealing,[2,8] insertion of dislocation filter layer,[9] selective growth in trenches using aspect ratio trapping (ART) method[10–12] or Ge/GeSi buffer layer.[13] The second challenge is the difference of thermal expansion coefficients between Si and III-V (6.6×10^{-6} K^{-1} and 2.3×10^{-6} K^{-1} for GaAs and Si, respectively), which limits the film thickness before crack appears. The third one is the emergence of anti-phase domains at the interface between III-V and Si substrate. Anti-phase boundaries (APBs) come from polar material (III-V) epitaxy on non-polar material (silicon). This hurdle has been tackled by using Si(001) substrates with a misorientation of 4°–6° towards the [110] direction[14,15] or Si(211) substrates.[1] Antiphase boundaries are charged structural defects in polar

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semiconductor forming disordered bond structures.[2] APBs are formed at the Si/GaAs interface and nucleate at the step edge of single Si atomic steps present at nominal Si(001) surface. Thus, homo-atomic bonds (Ga–Ga and As–As) are formed and propagates inside the whole epilayer. Because of the variation in bond strength between Ga–Ga,[16] As–As,[16] and Ga–As[16] bonds, the crystal lattice is locally distorted and elastic stress takes place at APBs position. Moreover, the Ga–Ga bonds present an electron deficiency and so they could act as acceptors, whereas As–As bonds have excess electrons and so they could act as donors. These bonds are doubly charged defects and usually As–As and Ga–Ga bonds are in equal number in GaAs layer allowing an electronic neutrality. Hence, the layer behaves like a highly compensated semiconductor degrading its electronic properties.[2]

In this paper, we show that APB-free GaAs thin layers can be grown on microelectronics standard nominal Si(001) 300 mm substrates. The APB-free epitaxial layer as thin as 150 nm was achieved using conventional microelectronics substrates with 0.15° misorientation in the [110] direction. We show that these APB-free layers exhibit improved optical and electronic properties compared to the layers with APBs.

The growths were performed in a 300 mm Applied Materials metalorganic chemical vapour deposition (MOCVD) reactor using hydrogen (H_2) as carrier gas, trimethylgallium (TMGa) as group-III precursor, tertiarybutylarsine (TBAs) as group-V precursor and disilane (Si_2H_6) for the n-type doping. For all the studies, microelectronics standard nominal Si(001) 300 mm wafers were used. Before the growth, the Si substrate was desoxidized in a SiConi™ chamber using a NF_3/NH_3 remote plasma. The wafers were then transferred into the MOCVD chamber where the GaAs layers were grown using a classical two-step process:[14,15] a nucleation layer was first deposited at low temperature (400-500 °C) measured by optical pyrometer followed by a high temperature step (600-700 °C) to grow high quality material. The typical V/III ratio is in the range of 5-30. For the electrical characterizations, doped GaAs:Si ($n = 7 \times 10^{17}$ cm^{-3}) layers were grown on top of non-intentionally doped GaAs buffer layer ($n = 3 \times 10^{16}$ cm^{-3}). This way the electrical conduction preferentially occurred in the doped layer located far from the defective Si/GaAs interface.

The surface morphology of the layers was investigated by atomic force microscopy (AFM) with standard tapping mode to get 2×2 and 5×5 μm^2 pictures. The structural properties were characterized in cross-section and plane view by *in situ* scanning transmission electron microscopy (STEM) across thin lamellas prepared with a focused ion beam-scanning electron microscope (FIB-SEM) tool (Helios NanoLab 450S from FEI) combining focused ion and electron beams. STEM images were directly realized under the SEM column at 30 keV to get less than 1 nm resolution images based on a field-emission-gun electron source. Additional observations have been performed with a JEOL transmission electron microscope (TEM) operating at 200 keV. Optical properties were measured by micro-photoluminescence (µPL) done in single point or as a map on the whole 300 mm wafers with a 532 nm laser diode focused by a microscope objective to a spot size of about 80 μm^2 presenting a power density of about 5 kW/cm^2. Hall effect measurements were carried out at room temperature to measure the carrier concentration and mobility. As the deposition is very uniform across the whole 300 mm wafers, five different zones along a diameter have been tested for Hall effect measurements and photoluminescence study.

Figure 1(a) shows an AFM image of a 400 nm thick GaAs layer obtained with the process described above. Thanks to their typical V groove shapes, randomly oriented APBs can be observed with a linear density of 3.7 μm^{-1}, leading to a high surface roughness of 1.6 nm. To decrease this surface roughness as well as the APBs density, all the process steps should be optimized.

We select Si(001) substrates presenting a 0.15° misorientation in the [110] direction because it corresponds to standard microelectronic substrates used in production unlike the 4°-6° offcut used normally to avoid APB formation.[8,14,15] Before the growth, an annealing (1 min–10 min) at high temperature (800 °C-950 °C) under H_2 is added to promote structuring of the 2×1 surface.[17–27] The Si surface presents mainly double steps (Figure 1(b)) with a width of about 100 nm, and few monoatomic islands remains at the step edges (not clearly visible from the AFM image). Despite theoretical thermodynamic considerations do not predict double step formation for quasi-nominal Si(001) substrate, this anomalous behavior (formation of double steps at low miscut angle) has already been observed by other groups.[17,28]
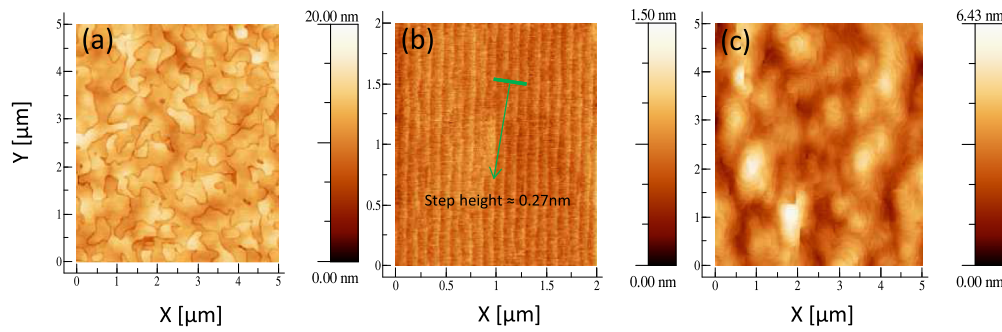
FIG. 1. (a) 5×5 μm^2 AFM image of a 400 nm thick GaAs growth on un-optimized Si(001): High density of randomly oriented APBs. RMS roughness = 1.6 nm. (b) 2×2 μm^2 AFM image of 0.15° Si(001) after optimized preparation (800 °C–950 °C annealing under H$_2$). The surface is therefore mainly double-stepped. (c) 5×5 μm^2 AFM image of an APBs-free 150 nm thick GaAs growth on optimized 0.15° Si(001). RMS roughness is 0.8 nm.

The two-step process was then used to grow a GaAs layer on this optimized Si surface. The AFM image of a 150 nm thick GaAs layer is shown in Figure 1(c). The surface roughness is improved with a 0.8 nm RMS value. This roughness is similar to the lowest one reported for 1 μm thick GaAs grown on 4°-6° offcut Si(001) substrate,[8,29,30] whereas we only grow 150 nm GaAs on quasi nominal substrates. Second, no V-groove feature is observed and indicating that an APBs-free surface is formed thanks to the Si surface preparation (SiConi + annealing) leading to the formation of double steps. Moreover, the APBs which should have formed from the few monoatomic silicon islands remaining at the surface (Figure 1(a)) are not visible at the GaAs surface (Figure 1(c)). The APB planes that nucleate at these monoatomic step edges have intersected pairwise during the growth and thus self-annihilated. This observation is similar to those previously reported by Stolz *et al.* on the MOCVD epitaxy of GaP on silicon.[17,31,32] In their experiment, they have to grow first a thick Si-buffer and anneal it at high temperature to be able to obtain the right Si surface preparation and reconstruction prior to GaP heteroepitaxy. Our process is simpler and better suited for industrial purpose as it eliminates the Si buffer growth and annealing to obtain an APB-free material.

To confirm the absence of APBs on top of the GaAs layer, we also performed STEM in cross section (Figure 2(a)). The STEM image took in the [110] direction shows a dark zone at the bottom of the GaAs layer due to the highly defective Si/GaAs heterointerface. The defective area is a combination of multiple crystalline defects such as dislocations, stacking faults due to the nucleation layer, APBs due to the monoatomic silicon islands. However, beyond about 70 nm, no more APB planes propagate toward the surface because APBs intersect pairwise and self-annihilate. APB-free GaAs top layer is confirmed by the absence of topological V-groove shape defect.
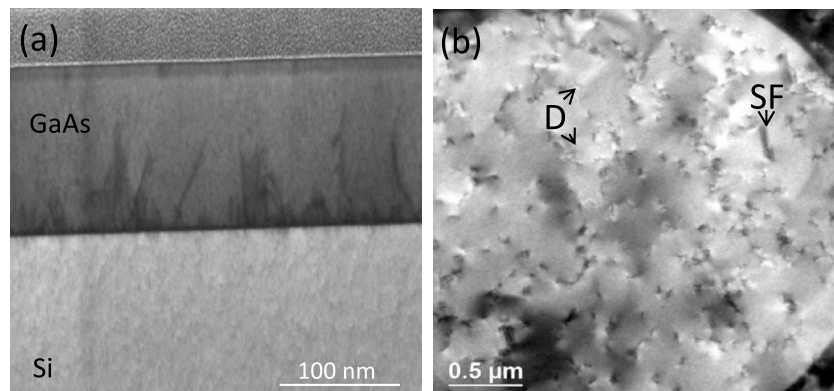

FIG. 2. (a) Cross section STEM image of the 150 nm GaAs layer with APBs-free top-surface. (b) TEM image realized in [001] direction. Dislocations and stacking faults are indicated on the image by "D" and "SF," respectively.
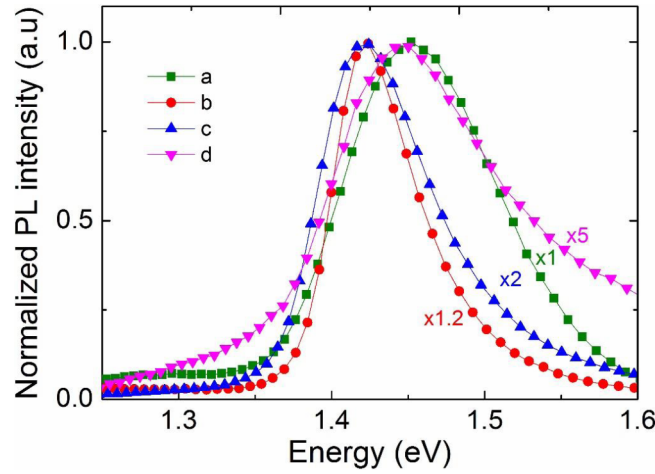
FIG. 3. Room temperature normalized PL spectra of: (a) a Si-doped GaAs substrate (doping concentration is 3×10^{18} cm^{-3}), a 400 nm GaAs:Si (doping concentration is 7×10^{17} cm^{-3}) (b) grown on a GaAs substrate, (c) without APBs grown on a Si substrate (d) with APBs grown on a Si substrate.

To characterize the crystalline quality of the GaAs top layer, plan-view TEM analysis is realized from a 400 nm thick optimized GaAs layer. For such an analysis, the challenge is to take only the material coming from the top part. We have developed a specific process thanks to a FIB-SEM tool to etch locally the silicon substrate and lift a large area of GaAs layer, which is placed on a TEM grid. This layer was then thinned down to 100 nm by ion etching from the backside. Figure 2(b) shows TEM image achieved in the [001] direction. Dislocations and stacking faults presenting a trapezoid shape are observed. The dislocations and stacking faults densities are estimated by counting the number of defects per unit area around 3×10^9 cm^{-2} and 7×10^7 cm^{-2}, respectively. Such dislocation density is in agreement with Tachikawa and Yamaguchi results.[33] Nevertheless, this value is still high and must be reduced in the future. Several methods are possible to decrease the threading dislocation density down to 10^5-10^6 cm^{-2}: Thermal Cycling Annealing (TCA) of the layer,[2,8] Ge/SiGe buffer layer,[13] ART,[10–12] superlattices,[2] InAs quantum dots insertion in the layer.[9]

Then, the influence of APBs on the optical and electrical properties has been studied. Figure 3 compares the photoluminescence of (a) a n-type GaAs substrate (n = 3×10^{18} cm^{-3} supplied by AXT) with a 400 nm thick GaAs:Si (7×10^{17} cm^{-3}) layers (b) grown on a GaAs substrate (c) without APBs grown on a Si substrate (d) with APBs grown on a Si substrate. The room temperature normalized μPL spectra obtained under the same experimental conditions are shown in Figure 3. The main extracted PL characteristics are reported in Table I.

As expected, the GaAs substrate and the GaAs:Si/GaAs(001) have the strongest and comparable PL intensity, which is two and five times higher than the GaAs:Si/Si(001) without and with APB, respectively. GaAs near band-edge emission is centered at 1.42 eV (samples b and c), 1.44 eV (sample d), and 1.45 eV (sample a) for APB-free GaAs, APBs GaAs, and GaAs substrate, respectively. For GaAs substrate, this 0.03 eV blue shift with respect to the room temperature GaAs band

TABLE I. μPL room temperature characteristics of a (a) GaAs substrates and GaAs:Si layers (b) grown on a GaAs substrate (c) without APBs grown on a Si substrate (d) with APBs grown on a Si substrate.

Sample	Center (eV)	FWHM (meV)	Maximum PL intensity	Intensity PL multiplicator factor
n-type GaAs substrate (a)	1.45	111	25 000	1
GaAs/GaAs substrate (b)	1.42	64	21 000	1.2
GaAs without APB on Si (c)	1.42	85	13 000	2
GaAs with APB on Si (d)	1.44	141	5 300	5

TABLE II. Hall effect measurements at room temperature for GaAs thin films grown on (i) GaAs substrate taken from literature, (ii) Si with and without APB in our MOCVD, and (iii) grown on GaAs substrate in our MOCVD.

Sample	Doping level (cm^{-3})	Electron mobility ($cm^2/V\,s$)	Resistivity (Ω/cm)
GaAs/GaAs substrate[36,37] literature	7×10^{17}	5000	2×10^{-3}
GaAs without APB on Si	7×10^{17}	2000	4×10^{-3}
GaAs with APB on Si	7×10^{17}	200	2×10^{-2}
GaAs/GaAs substrate grown in our MOCVD	7×10^{17}	2500	3×10^{-3}

gap of 1.42 eV is known as the Burstein-Moss shift and has been extensively studied in the past for heavily Si-doped GaAs.[34,35] This shift towards higher energies results from the filling of the conduction band by free carrier concentration. Moreover, the broadening of the PL peak in Si-doped GaAs with increasing the electron concentration has also been reported and is explained by band to band optical transitions with and without momentum conservation between the conduction and valence bands. On the other hand, it is important to notice that the optimized GaAs layer with no APBs has a stronger PL intensity (almost three times higher) with a narrower peak (FWHM of 85 meV) than the APBs GaAs layer (FWHM of 141 meV). This is definitively correlated with the role of APBs that act as non-radiative recombination centers.[13]

In order to study the role of APBs on the electrical properties, a 250 nm thick Si-doped GaAs layer with a doping level of n = 7×10^{17} cm^{-3} was grown on a GaAs substrate and on 400 nm thick GaAs buffer layers (n = 3×10^{16} cm^{-3}) with and without APBs. Hall effect measurements in the Van der Pauw configuration are reported in Table II.

For the APB-free Si-doped GaAs layer, the mean electron mobility (μ_e) was evaluated by taking 5 points across whole 300 mm wafer to be 2000 ± 60 $cm^2/V\,s$, while the one measured for the sample containing APBs was only 200 $cm^2/V\,s$, which represent an improvement of one decade. For the same doping level, electron mobility $\mu_e \sim 2500$ $cm^2/V\,s$ was determined for n-type homoepitaxial n-GaAs/GaAs(001) grown in our MOCVD reactor. Hageman *et al.* reported a value of $\mu_e \sim 5000$ $cm^2/V\,s$ for homoepitaxial GaAs layer with a comparable doping level.[37] In the eighties, Akiyama *et al.*[14,38] have grown GaAs directly on Si(001) substrates. They claimed that they were able to grow APB-free materials with film thickness about 3 μm and that they obtained a mobility of 5200 $cm^2/V\,s$. This mobility decreases to 2000 $cm^2/V\,s$ in presence of APB showing their detrimental effect. APBs have to be suppressed to improve μ_e but also the dislocation density should be reduced (in our layer: 10^9 cm^{-2}). Nevertheless, we could compare for the same doping level μ_e in Si(001) (~ 200 $cm^2/V\,s$),[39] with μ_e in our thin GaAs films directly grown on Si(001) (2000 $cm^2/V\,s$). A gain of a factor 10 is reached, opening a way to realize GaAs based devices on a Si CMOS platform with expected improved electrical characteristics in comparison with Si based devices.

In conclusion, we have demonstrated the possibility to grow a very thin GaAs layer (150 nm) on 300 mm nominal Si(001) substrates used as a standard in the microelectronics industry, with no anti-phase domains. We compared the electronic and optical properties of the GaAs films with and without APBs. The electronic properties are considerably improved as (i) a FWHM narrowing of the μPL signal is observed concomitant with an increase of the intensity and (ii) an increase of the electron mobility to a value of 2000 $cm^2/V\,s$. Moreover, in comparison with Hall mobility value for bulk silicon where $\mu_e = 200$ $cm^2/V\,s$, it represents also an increase of one decade. These improved properties could open a route for elaboration and integration of GaAs as active layer of nanoelectronic and optoelectronic devices on a Si CMOS platform.

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