علی بنی هاشمی 810100245
محمدکاوه عسگری 810100274
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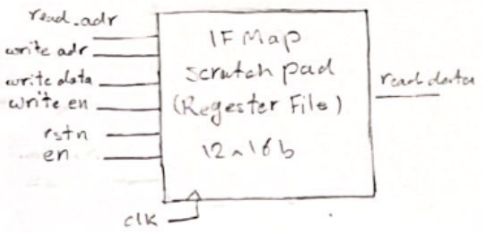
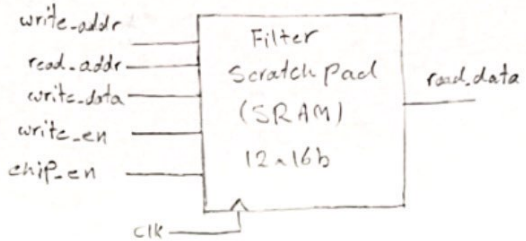
1, Regester Scratch pad:



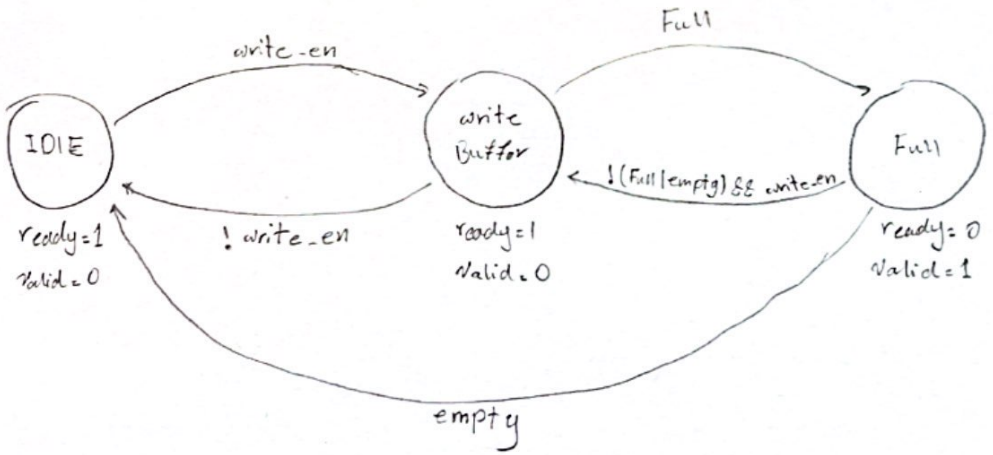
A single port regester array scratch pad memory that allows read and write operations in single clock cycle.

2, SRAM Scratch pad:



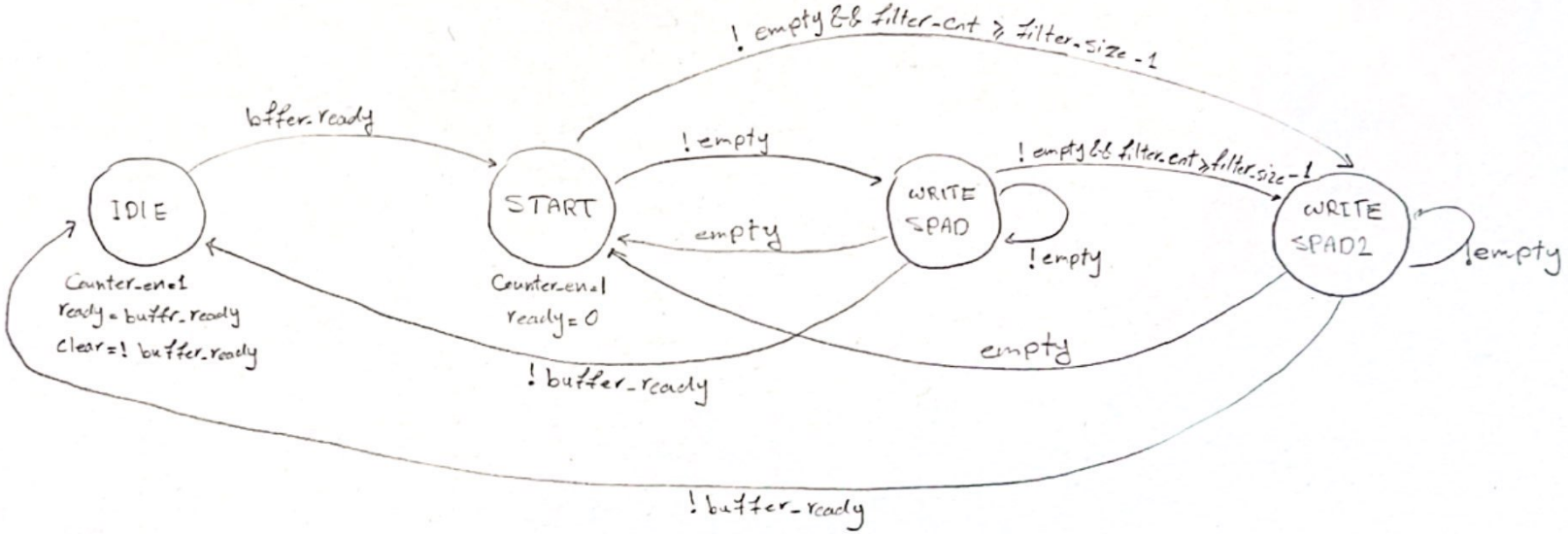
A synchronous SRAM scratch pad designed to allow read and write operation within a single clock cycle.

3, Buffer Controller: buffer should have 2 signals, one showing the buffer is not filled and can still get new values. (ready). Ones show now it h value and outher Components like Spads can read from that (valid).



Data Spad Controller: module is responsible for managing the communication between the data buffer and the scratch pad (spads) memory.

It controls the state transition bais on the buffer readiness and the FIFO status, ensuring data is properly written to spads.



→ waiting for the buffer to be ready (IDLE).

→ preparing to write data when the buffer is ready (START).

→ Actively writing data to the SPAD when the FIFO is not empty (write_SPAD).

→ Compliting the write operation and signaling readiness (write_SPAD2).

→ Actively writing data to the SPAD when the FIFO is not empty (write_SPAD).

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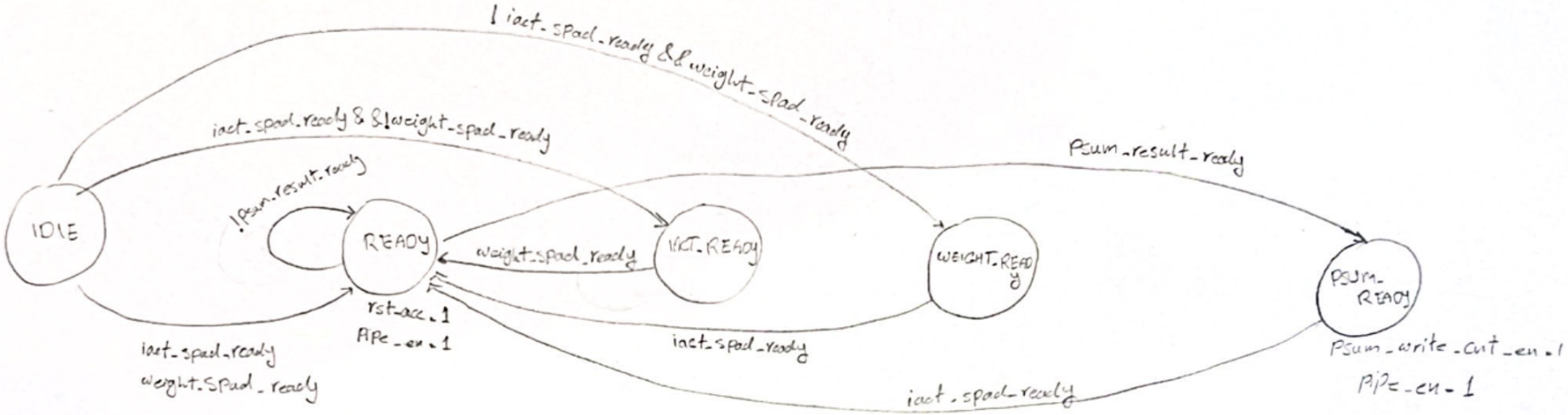
5, main Controller (PE Controller) is responsible for manging the Control signal for the processig elements (PEs) in the system.



→ waiting for both input activation and weight SPAD controllers to be ready (IDLE).

→ Enabling the processing pipe line when both controllers are ready (Redy).

→ managing the Counter clear signal and pipeline enable signal based on the state transition.

port name	type	width	Description
clk	input	1	clock signal.
rstn	input	1	reset signal (Active low).
iact_spad_Controller_ready	input	1	signal indicating IACT SPad Controller is ready.
weight_spad_Controller_ready	input	1	signal indicating weight SPad Controller is ready.
pipe_en	output	1	Enable signal to start pipeline process.

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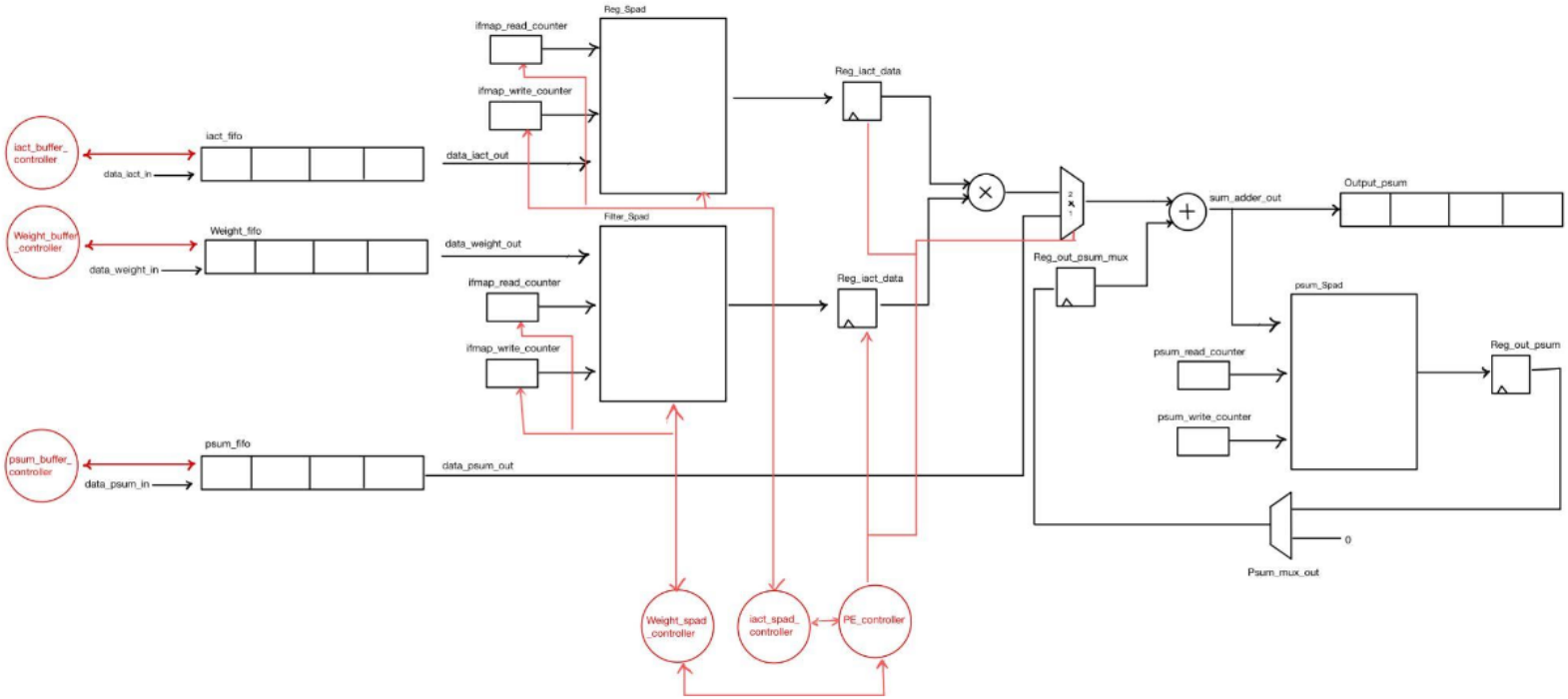
Reg_Spad
ifmap_read_counter
ifmap_write_counter
Reg_iact_data
iact_buffer_
controller
iact_fifo
data_iact_in
data_iact_out
Weight_buffer
_controller
Weight_fifo
data_weight_in
data_weight_out
Filter_Spad
ifmap_read_counter
ifmap_write_counter
Reg_iact_data
2
x
1
Reg_out_psum_mux
sum_adder_out
Output_psum
psum_Spad
psum_read_counter
psum_write_counter
Reg_out_psum
psum_buffer_
controller
psum_fifo
data_psum_in
data_psum_out
0
Psum_mux_out
Weight_spad
_controller
iact_spad_
controller
PE_controller