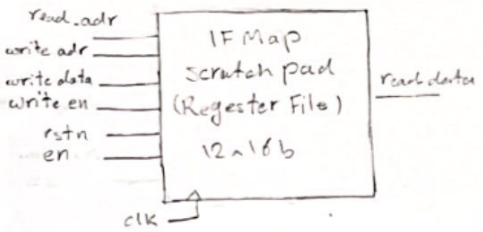
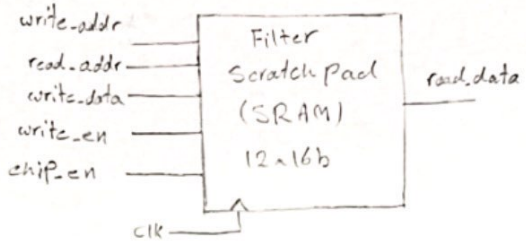
علی بنی هاشمی 810100245
محمدمهدی عسگری 810100274
محمدمهدی داورزنی 810100140

1, Regester Scratch pad:



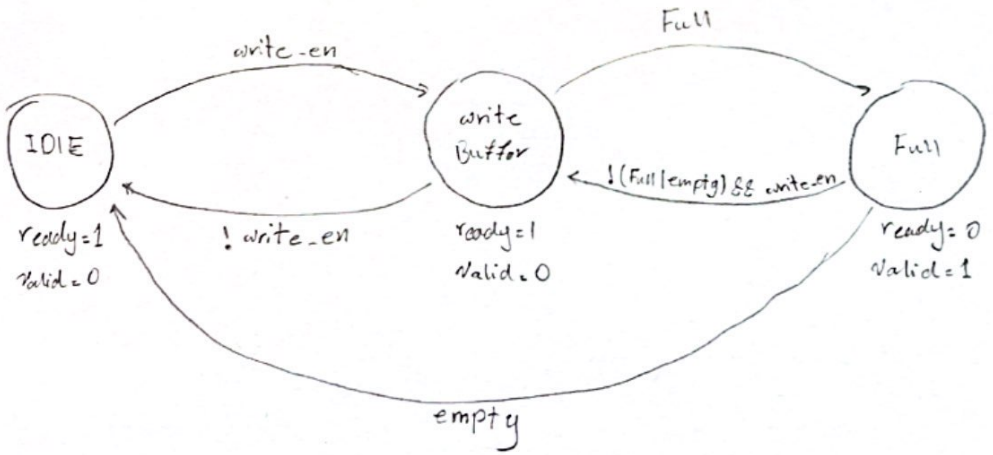

A single port regester array scratch pad memory that allows read and write operations in single clock cycle.

2, SRAM Scratch pad:



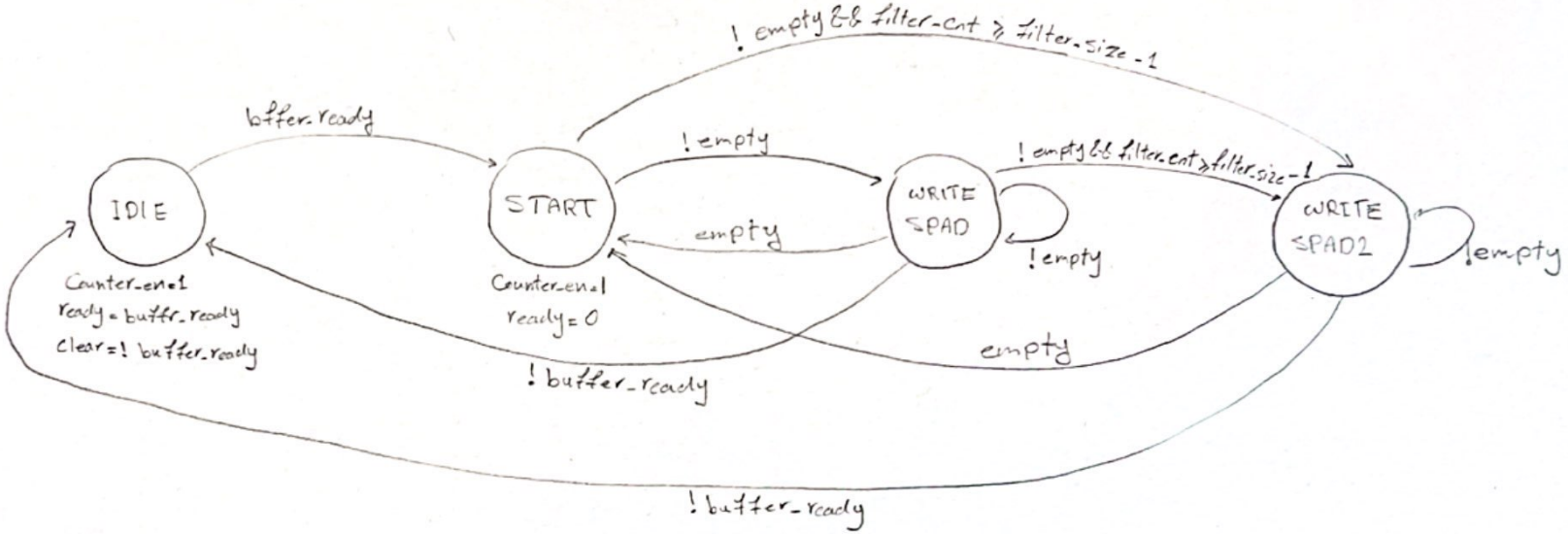

A synchronous SRAM scratch pad designed to allow read and write operation within a single clock cycle.

3, Buffer Controller: buffer should have 2 signals, one showing the buffer is not filled and can still get new values. (ready). Ones show now it has value and outher Components like SPads can read from that (Valid).



Data Spad Controller: module is responsible for managing the communication between the data buffer and the scratch pad (spads) memory.

It controls the state transition bais on the buffer readiness and the FIFO status, ensuring data is properly written to spads.




→ waiting for the buffer to be ready (IDLE).

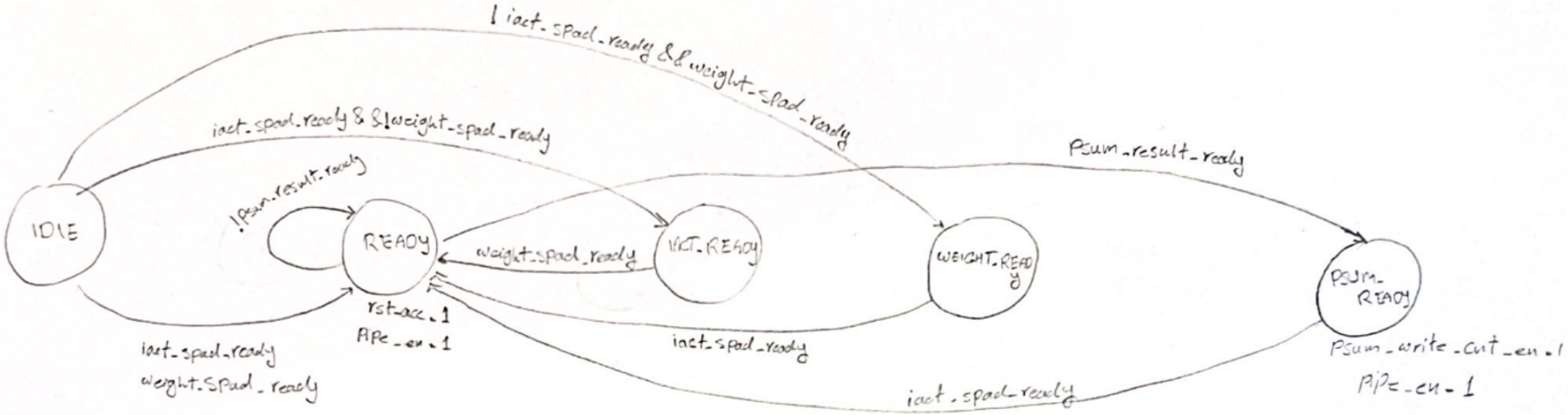
→ preparing to write data when the buffer is ready (START).

→ Actively writing data to the SPAD when the FIFO is not empty (write_SPAD).

→ Compliting the write operation and signaling readiness (write_SPAD2).

→ Actively writing data to the SPAD when the FIFO is not empty (write_SPAD).

5, main Controller (PE Controller) is responsible for manging the Control signal for the processig elements (PEs) in the system.




→ waiting for both input activation and weight SPAD controllers to be ready (IDLE).

→ Enabling the processing pipe line when both controllers are ready (Redy).

→ managing the Counter clear signal and pipeline enable signal based on the state transition.

| port name | type | width | Description |
|---|---|---|---|
| clk | input | 1 | clock signal. |
| rstn | input | 1 | reset signal (Active low). |
| iact_spad_Controller_ready | input | 1 | signal indicating IACT SPad Controller is ready. |
| weight_spad_Controller_ready | input | 1 | signal indicating weight SPad Controller is ready. |
| pipe_en | output | 1 | Enable signal to start pipeline process. |