Experiment 1 - Clock and Periodic Signal Generation

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Abstract— **This document is a report for experiment #1 of Digital Logic Design Laboratory at ECE department, University of Tehran. The purpose of this experiment is to provide different methods for clock generation.**

Keywords—

I. CLOCK GENERATION USING ICS AND ANALOG COMPONENTS

A. Ring Oscillator

By connecting odd number of these gates and connecting the output of the last inverter to the first one, output of each inverter will oscillate.

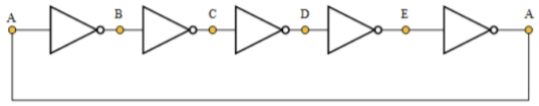

Fig.1: Ring oscillator circuit [1]

A 74LS04 has 6 inverters. As it was said, we need odd number of inverters to have the oscillation. By connecting five inverters of 74LS04 we will have a ring oscillator with a frequency of about 26 KHz.

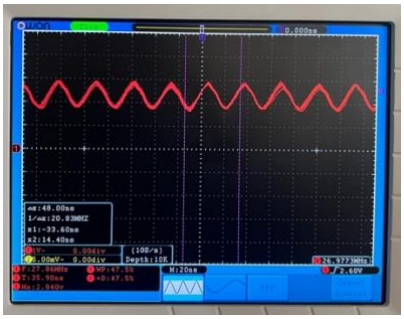

Fig. 2: Ring oscillator output

As we know we can calculate the delay of a single inverter using ring oscillator, to measure propagation delay of the chain, we should measure the time from the 50% point of input to the 50% point of output. This period is equal to half of period time of the output, that is about 38 ns (T = 1/f).

Using ring oscillator period time formula, we can have the delay of a single inverter:

$$T_{ring\ oscillator} = 2N\Delta \ ; \quad \Delta: Inverter\ delay$$

$$\rightarrow \Delta = 3.8\ ns$$

B. LM555 Timer

This IC is among the devices that can be used for generating clock signal or delays. It has three modes: Monostable, Bistable and Astable, which in astable mode it operates as an oscillator.

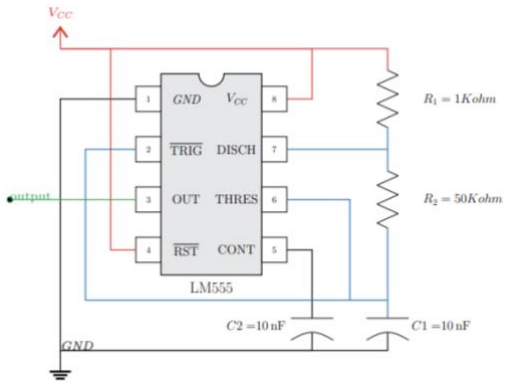

Fig. 3: LM555 in astable mode [1]

In this IC we have two Op-Amps that their positive pin is connected to a fraction of Vcc. The outputs of these two are connected to a FF with a reset and preset. At first capacitor C1 is empty and starts to charge. In this state the FF reset to 0, Then output is 1 (duo to inverter at FF output). When C1 charges until %66 of Vcc FF sets to 1 and output is 0. Then the base voltage of the BJT transistor is 1 (logically) and C1 discharges through it, And this cycle repeats. C1 charges from R1+R2 and discharges through R2. Therefor the charge period is more than discharge period and we have a duty cycle above %50.

We can change R1, R2, C1 values to reach desired frequency and duty cycle. By default, values of R1, R2, C1 we have:

$$T = 0.69(R_1 + 2R_2)C_1 \rightarrow \ T = 699.93\ \mu s$$

$$f = \frac{1}{T} \rightarrow f = 1.428\ KHz$$

$$duty\ cycle = \frac{R_1 + R_2}{R_1 + 2R_2} = 0.50 = \%50$$

Then we have the output:

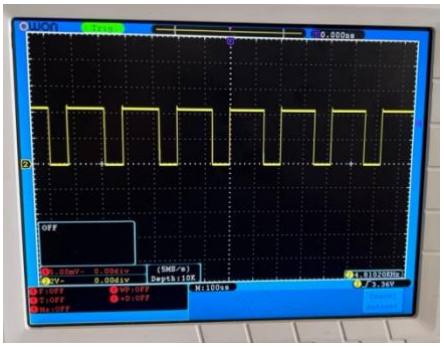

Fig. 4: LM555 output waveform

As we see in waveform above, Output has a 4.8102KHz frequency and about %50.3 duty cycle. There is a little bit difference between real life and calculations. That's because of circuit disturbance and oscilloscope accuracy. By changing R2 value, we will have different frequencies and duty cycles according to calculations above:

Table I. LM555 freq. and duty cycle change duo to R2 value

Resistor (KΩ)	1	10	100
Frequency (KHz)	46.1	6.8	0.71
Duty cycle	%66.6	%52.1	%50.2

As we see the more R2 increases the less frequency and duty cycle we have.

The results that were calculated are also attached in the following.

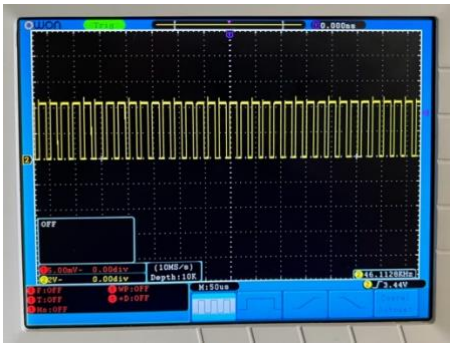

Fig. 5: LM555 output with 1KΩ resistor

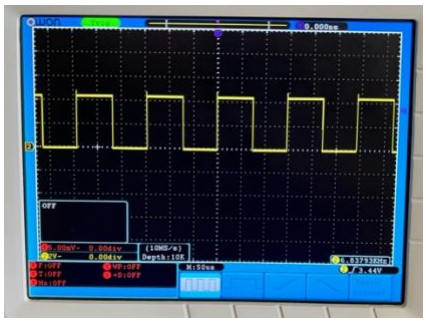

Fig. 6: LM555 output with 10KΩ resistor

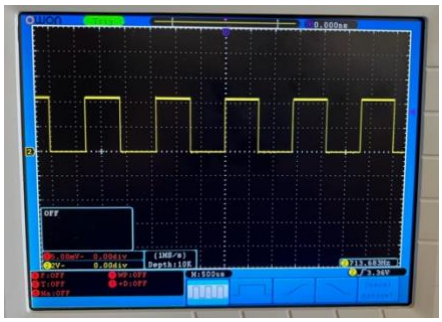

Fig. 7: LM555 output with 100KΩ resistor

Note that the difference between calculations and real life is due to circuit disturbance and oscilloscope accuracy.

C. Schmitt Trigger Oscillator

Schmitt trigger is a comparator circuit that can be implemented by an Op-amp. Connecting a few resistors to it, allows us to design an element which has such an IO characteristic.

The main advantage of this design is that there is a margin between threshold levels, so the output won't be affected by unwanted noises.

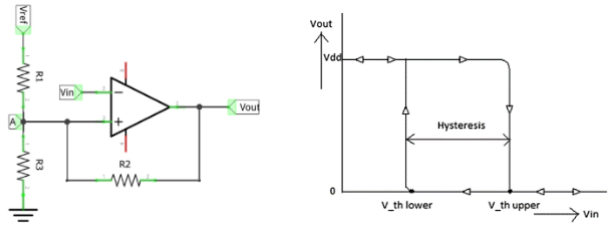

Fig. 8: Schmitt trigger circuit [?]

If we connect the output and the input of the Schmitt trigger by a resistor and it's input to the ground using a capacitor, V_{out} should oscillate.

Let's consider the capacitor has no charge at first. V_{in} would be zero and V_{out} must be equal to V_{cc}. Then the capacitor starts to charge until its voltage becomes V_{Th+}. At this point V_{out} will become zero and the capacitor starts to discharge. It will continue till its charge gets to V_{Th-}. This process would repeat and repeat and as we expected, we'll see a square wave at V_{out}.

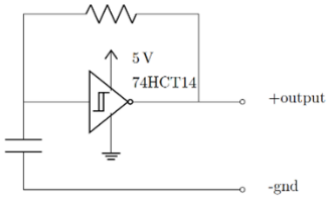

Fig. 9: Schmitt inverter oscillator circuit [1]

The function of this circuit is based on charging and discharging of the capacitor. The more it's time constant (τ) is, the more it takes to oscillate. It can be concluded that frequency is proportional to 1/τ and this can turn into an equation by considering a constant such as α which represents the structure of the Schmitt trigger.

Using a 74HCT14 we assembled the circuit which was mentioned in figure 4 and by changing the resistors, we measured the frequencies and α. The results can be seen in the table below.

Table II. measurement of α

Resistor (Ω)	**470**	**1000**	**2200**
Frequency (KHz)	153.5	73.1	27.7
α	0.72	0.73	0.65

The results that were observed are also attached in the following.

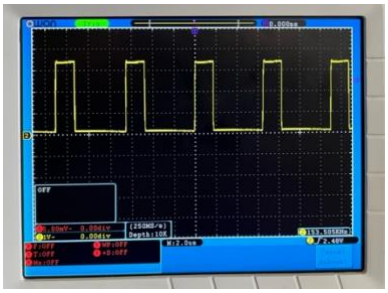

Fig. 10: Schmitt trigger with 470Ω resistor

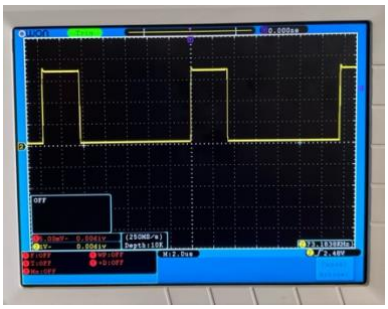

Fig. 11: Schmitt trigger with 1000Ω resistor

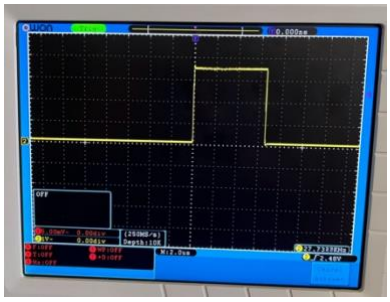

Fig. 12: Schmitt trigger with 2200Ω resistor

D. Synchronous Counter as a Frequency Divider

By cascading two 4-bit counters, the maximum value that can be reached is $2^8 - 1 = 256 - 1 = 255$. Therefrom we are supposed to build a divide-by-200 frequency divider, we must put $255 - 200 = 55$ which is 00110111 on parallel inputs. As it was said in the manual, we assembled the circuit and connected corresponding inputs to gnd and V_{cc}. For the primary initialization, using a 74HC08 IC, we added an AND gate to the load pin to have a preset pin. By connecting the output of the Ring Oscillator to the input of the first counter, the carry out pin of the first counter to the clock input of the second counter and the carry out pin of the second counter to both load inputs, the circuit will divide the frequency by the given value.

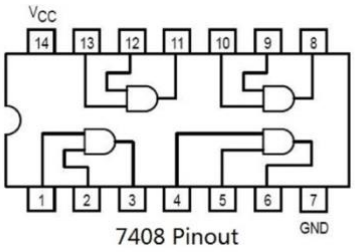

Fig. 13: 7408 Logic gate chip datasheet

As we saw in the first part, the frequency of the Ring Oscillator was about 26MHz. It can be seen that the output frequency is about 122KHz. As we expected the frequency was divided by 200. However, the duty cycle is still about $\frac{199}{200} \approx 1$ which is not desired. In the next part, by adding a T-Flip Flop, we'll see it can be easily solved.

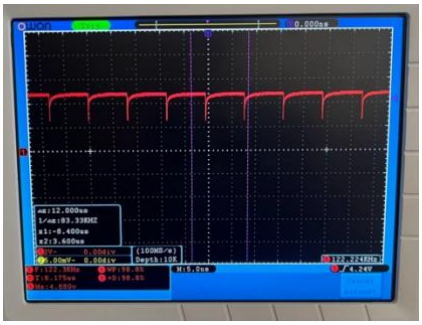

Fig. 14: Waveform of carry out pin of the MSB counter

E. T Flip-Flop

By converting a D flip-flop to T flip-flop and connect the output of frequency divider to the TFF input we can reach %50 duty cycle in the output.

Using a 74HC74 and wire pin2 and pin6 we will have TFF operation via DFF. At positive edge of clock, Q1bar toggles until next edge. Therefore, we have a %50 duty cycle at the output.

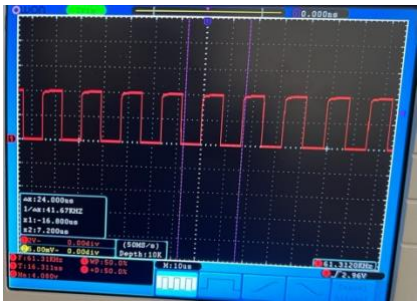

Fig. 15: TFF output with %50 duty cycle

Note that using a TFF will halves the frequency (from 122KHz to 61KHz).

F. Final circuit picture

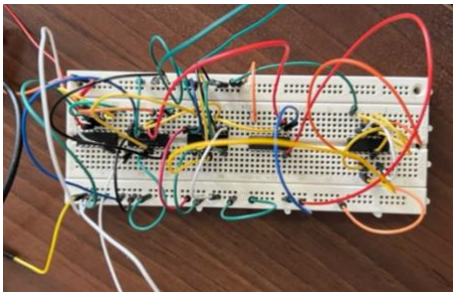

Fig. 16: Final circuit wiring

II. CONCLUSIONS

In this experiment, we learnt different clock generating methods, 74 Series Basic Logic Gates (Inverter, DFF, etc.), Frequency division with counters, And use T flip-flop to generate %50 duty cycle.

III. REFERENCES

This lab manual was prepared and developed by Katayoon Basharkhah, Ph.D. student of Digital Systems at the University of Tehran, under the supervision of Professor Zain Navabi. This manual has been revised and edited by Zahra Jahanpeima, PHD student of Digital Systems at University of Tehran.