

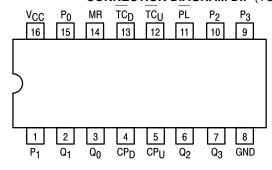
# PRESETTABLE BCD/DECADE UP/DOWN COUNTER PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

The SN54/74LS192 is an UP/DOWN BCD Decade (8421) Counter and the SN54/74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load (PL) and the Master Reset (MR) inputs asynchronously override the clocks.

- Low Power . . . 95 mW Typical Dissipation
- High Speed . . . 40 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Master Reset and Parallel Load
- Individual Preset Inputs
- Cascading Circuitry Internally Provided
- Input Clamp Diodes Limit High Speed Termination Effects

# **CONNECTION DIAGRAM DIP (TOP VIEW)**



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOADING (Note a)

# **PIN NAMES**

		HIGH	LOW
CPU	Count Up Clock Pulse Input	0.5 U.L.	0.25 U.L.
CPD	Count Down Clock Pulse Input	0.5 U.L.	0.25 U.L.
<u>MR</u>	Asynchronous Master Reset (Clear) Input	0.5 U.L.	0.25 U.L.
PL	Asynchronous Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
$P_n$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
<u>Q</u> n	Flip-Flop Outputs (Note b)	10 U.L.	5 (2.5) U.L.
<u>TC</u> D	Terminal Count Down (Borrow) Output (Note b)	10 U.L.	5 (2.5) U.L.
TCU	Terminal Count Up (Carry) Output (Note b)	10 U.L.	5 (2.5) U.L.

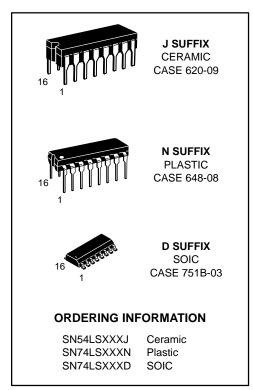
a. 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

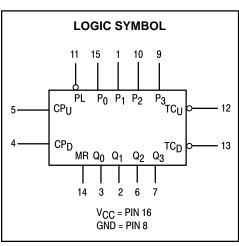
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

# SN54/74LS192 SN54/74LS193

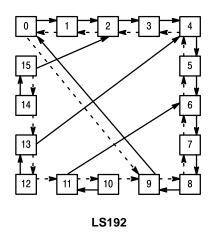
PRESETTABLE BCD/DECADE
UP/DOWN COUNTER
PRESETTABLE 4-BIT BINARY
UP/DOWN COUNTER

LOW POWER SCHOTTKY





### STATE DIAGRAMS



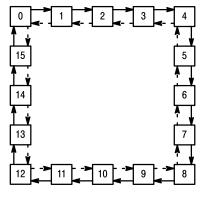
# LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{ \frac{TC}{TC}_U} = \underline{Q_0} \cdot \underline{Q_3} \cdot \overline{\underline{CP_U}}$$

$$\overline{TC_D} = \underline{Q_0} \cdot \underline{Q_1} \cdot \underline{Q_2} \cdot \underline{Q_3} \cdot \overline{\underline{CP_D}}$$

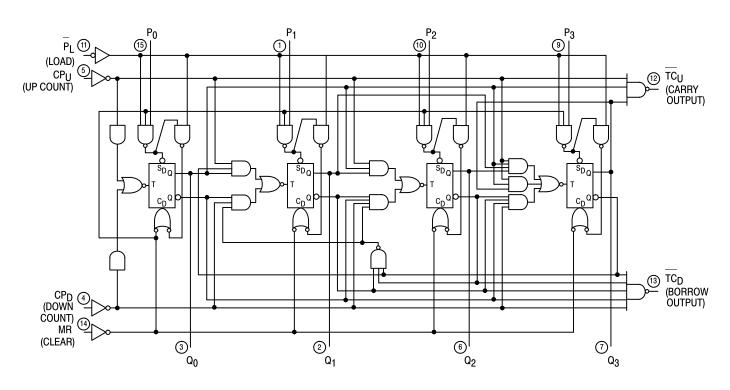
# LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

$$\begin{array}{l} \overline{\underline{TC}}_U = \underline{Q_0} \cdot \underline{Q_1} \cdot \underline{Q_2} \cdot \underline{Q_3} \cdot \overline{\underline{CP_U}} \\ TC_D = \underline{Q_0} \cdot \underline{Q_1} \cdot \underline{Q_2} \cdot \underline{Q_3} \cdot \underline{CP_D} \end{array}$$



# LS193

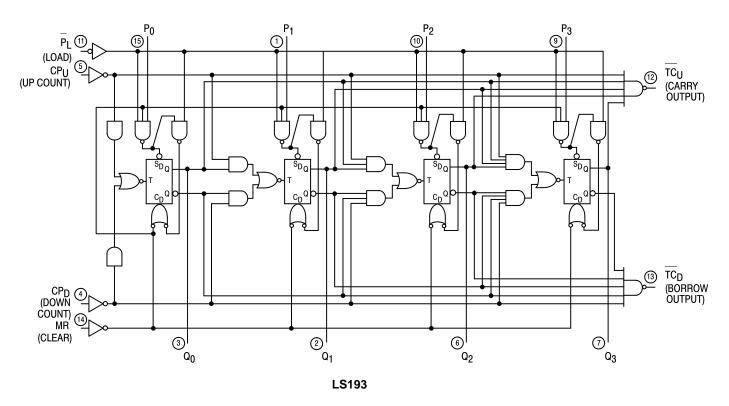
# **LOGIC DIAGRAMS**



LS192

 $V_{CC}$  = PIN 16 GND = PIN 8  $\bigcirc$  = PIN NUMBERS

# **LOGIC DIAGRAMS (continued)**



V<sub>CC</sub> = PIN 16 GND = PIN 8

### **FUNCTIONAL DESCRIPTION**

The LS192 and LS193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous UP/DOWN (Reversable) Counters. The operating modes of the LS192 decade counter and the LS193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up (TC<sub>U</sub>) and Terminal Count Down (TC<sub>D</sub>) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the LS192, 15 for the LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause TC<sub>U</sub> to go LOW. TC<sub>U</sub> will stay LOW until CP<sub>U</sub> goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the TC<sub>D</sub> output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability <u>per</u>mitting the counter to be preset. When the Parallel Load (PL) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs ( $P_0$ ,  $P_3$ ) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

## **MODE SELECT TABLE**

MR	PL	СР	CPD	MODE
Н	Х	Х	Х	Reset (Asyn.)
L	L	Х	Х	Preset (Asyn.)
L	Н	Н	Н	No Change
L	Н	J	Н	Count Up
L	Н	Н		Count Down

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

# **GUARANTEED OPERATING RANGES**

Symbol	Parameter		Min	Тур	Max	Unit
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I <sub>ОН</sub>	Output Current — High	54, 74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

# DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

			Limits					
Symbol	Parameter		Min	Тур	Max	Unit	Tes	st Conditions
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
\/	Input I OW Voltage	54			0.7	V	Guaranteed Input	LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
Vari	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC}$ = MIN, $I_{OH}$ = MAX, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table	
VOH	Output HIGH voltage	74	2.7	3.5		V		
V	Output I OW/ Valtage	54, 74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN},$ $V_{IN} = V_{IL} \text{ or } V_{IH}$	
VOL	Output LOW Voltage	74		0.35	0.5	V	I <sub>OL</sub> = 8.0 mA	per Truth Table
1	Innut I II CI I Current				20	μΑ	$V_{CC} = MAX, V_{IN}$	= 2.7 V
l ¹IH	Input HIGH Current				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>I</sub> L	Input LOW Current				-0.4	mA	$V_{CC} = MAX$ , $V_{IN} = 0.4 V$	
IOS	Short Circuit Current (Note 1)		-20		-100	mA	V <sub>CC</sub> = MAX	
ICC	Power Supply Current				34	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# AC CHARACTERISTICS $(T_A = 25^{\circ}C)$

		Limits				
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
f <sub>MAX</sub>	Maximum Clock Frequency	25	32		MHz	
<sup>t</sup> PLH <sup>t</sup> PHL	CP <sub>U</sub> Input to TC <sub>U</sub> Output		17 18	26 24	ns	
<sup>t</sup> PLH <sup>t</sup> PHL	CP <sub>D</sub> Input to TC <sub>D</sub> Output		16 15	24 24	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
<sup>t</sup> PLH <sup>t</sup> PHL	Clock to Q		27 30	38 47	ns	C <sub>L</sub> = 15 pF
<sup>t</sup> PLH <sup>t</sup> PHL	PL to Q		24 25	40 40	ns	
<sup>t</sup> PHL	MR Input to Any Output		23	35	ns	

# AC SETUP REQUIREMENTS ( $T_A = 25$ °C)

		Limits				
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
tW	Any Pulse Width	20			ns	
t <sub>S</sub>	Data Setup Time	20			ns	V 50V
t <sub>h</sub>	Data Hold Time	5.0			ns	V <sub>CC</sub> = 5.0 V
t <sub>rec</sub>	Recovery Time	40			ns	

# **DEFINITIONS OF TERMS**

SETUP TIME  $(t_S)$  is defined as the minimum time required for the correct logic level to be present at the logic input prior to the PL transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

 $\underline{HQLD}$  TIME ( $t_h$ ) is defined as the minimum time following the PL transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recogni-

tion. A negative HOLD TIME indicates that the correct logic level may be released prior to the PL transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME ( $t_{\text{rec}}$ ) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

# **AC WAVEFORMS**

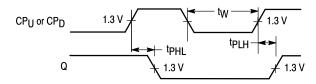


Figure 1

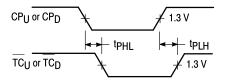


Figure 2

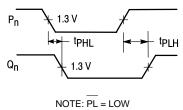


Figure 3

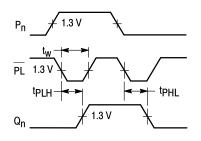


Figure 4

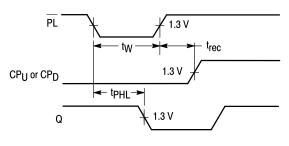
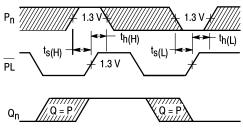


Figure 5



\* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 6

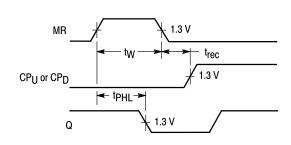
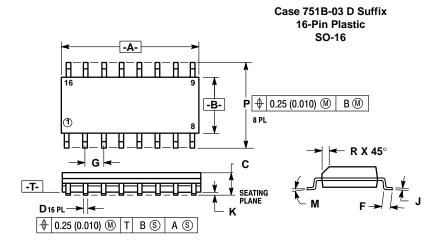
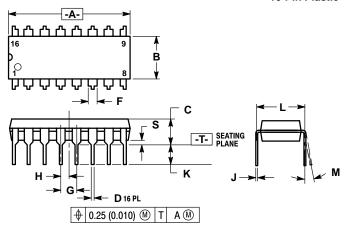
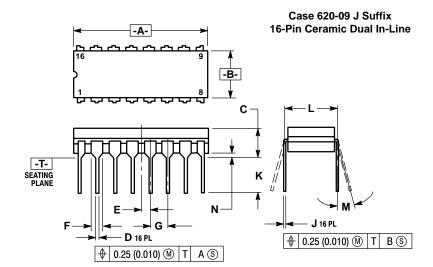


Figure 7



# Case 648-08 N Suffix 16-Pin Plastic





### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
  DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- PER SIDE.
  751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

	MILLIM	ETERS	INC	HES	
DIM	MIN MAX		MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050 BSC		
J	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
M	0°	7°	0°	7°	
Р	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- TO THE STATE OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD
- ROUNDED CORNERS OPTIONAL. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

	MILLIM	ETERS	INC	HES	
DIM	MIN	MIN MAX		MAX	
Α	18.80	19.55	0.740	0.770	
В	6.35	6.85	0.250	0.270	
С	3.69	4.44	0.145	0.175	
D	0.39	0.53	0.015	0.021	
F	1.02	1.77	0.040	0.070	
G	2.54	BSC	0.100 BSC		
Н	1.27	BSC	0.050 BSC		
J	0.21	0.38	0.008	0.015	
K	2.80	3.30	0.110	0.130	
L	7.50	7.74	0.295	0.305	
M	0°	10°	0°	10°	
S	0.51	1.01	0.020	0.040	

- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L'TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
  5. 620-01 THRU-08 OBSOLETE, NEW STANDARD 620-09.

	MILLIM	ETERS	INC	HES	
DIM	MIN MAX		MIN	MAX	
Α	19.05	19.55	0.750	0.770	
В	6.10	7.36	0.240	0.290	
С	_	4.19	_	0.165	
D	0.39	0.53	0.015	0.021	
E	1.27	BSC	0.050 BSC		
F	1.40	1.77	0.055	0.070	
G	2.54	BSC	0.100	BSC	
J	0.23	0.27	0.009	0.011	
K	_	5.08	_	0.200	
L	7.62 BSC		0.300	BSC	
M	0°	15°	0°	15°	
N	0.39	0.88	0.015	0.035	

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