Stephen Singh

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Education

University of Florida — Gainesville, FL

MS in Electrical & Computer Engineering — 01/2022 - 12/2024

- Courses: Hardware/Software Co-Design for ML, SoC Architecture, Computer Architecture, Hardware Security & Trust, Digital Logic Design using HDL, RF Analog Filter Design, Low Power VLSI

University of Georgia — Athens, GA

BS in Electrical & Electronics Engineering — 05/2019 - 05/2021

Experience

Motorola Solutions — Florida, US

Presales System Engineer — 2018 - Present

- Working closely with the Sales Team to deliver customer-driven, end-to-end solutions that rise to the challenges of first responder, government, utility, transportation, and enterprise customers.
- Perform RF coverage and interference predictions.
- Prepare systems diagrams, detailed rack layouts and site floor plans.
- Build and sustain relationships with cross-functional teams to achieve customer satisfaction, orders, and revenue goals.
- Guided consultation in wireless solutions, emphasizing ASTRO25, APCO P25, LTE, and 3G/4G technologies.
- Architected RF front-ends with a focus on noise, IM distortion, harmonic suppression, and ERP according to FCC Rules.

Projects

Lane-Following RC Car SoC Development — 2023 - 2025

PYNQ Z2 | Zynq-7000 SoC | Verilog/Vivado | Python/OpenCV | AXI4 | I²C | UART | PWM

- Designed and implemented a real-time lane-following self-driving RC car on the **PYNQ Z2** platform (ARM Cortex-A9 + FPGA).
- Developed **custom Verilog IP cores** for camera preprocessing (grayscale, 7×7 convolution) using **AXI4-Stream** interfacing.
- Controlled steering and throttle through **hardware PWM** using **AXI GPIO** and **MMIO**, enabling dynamic servo adjustments based on lane curvature.
- Tested and tuned real-time **lane detection algorithm** (Canny edge + Hough Transform) on ARM core using Python/OpenCV.

AES-128 Encryption/Decryption SoC — 2024 - 2025

Verilog | Vivado | Vitis C | AXI4-Lite | UART | GPIO | FSM Design | RTL Simulation

- Engineered **AES-128 cryptographic system** on the **Xilinx Zynq-7020 SoC**, covering RTL design, testbenches, and **hardware/software co-design**.
- Developed **Vitis C drivers** to control the AES IP over AXI-Lite and interact with users via **UART console** and **AXI-GPIO (buttons/switches/LEDs)**.
- Created RTL cores for **AES encryption, decryption, and key expansion**, using Verilog and modular FSM control.

5-Stage Pipelined RISC-V CPU — 2024 - 2025

Verilog | Vivado | BRAM | Pipelining | MMIO | PYNQ-Z2 | ILA Debug

- Designed and deployed a custom **32-bit 5-stage pipelined RISC-V processor** on the **PYNQ-Z2 FPGA.**
- Integrated **instruction and data BRAM** with memory-mapped I/O for switches and LEDs using custom address decoding.
- Verified RTL via **Vivado testbenches** and waveform analysis, achieving **functional and branch coverage** with no assertion failures.
- Packaged the design into a custom IP for **Vivado block diagram**, wiring the RISC-V core, BRAMs, and I/O interfaces.

HDMI Pong Game on PYNQ-Z2 with CPU-Controlled Opponent — 2023 - 2025

SystemVerilog | Vivado | Vitis C | TMDS/HDMI | AXI-Lite | BRAM | FSM | Video Timing

- Full 1280×720@60Hz **Pong game engine** on the **Zynq-7020 SoC**, combining **FPGA-rendered HDMI output** with **bare-metal C AI control** via AXI-Lite.
- Engineered full game logic: ball physics, paddle collisions, score tracking, and a "GAME OVER" splash loaded from BRAM-initialized **bitmap ROM**.

Skills

Programming Languages: · Verilog · VHDL · System Verilog · C/C++ · MATLAB · VITIS HLS · OpenCL · TCL · Perl · Bash

Embedded Platforms: · Xilinx PynqZ2 (Zynq-7000) · Digilent Basys3 (Artix-7) · Xilinx MicroBlaze · Arduino (ESP8266) · Raspberry Pi 4

Software: · Xilinx Vivado · Xilinx Vitis HLS · PetaLinux · Cadence Virtuoso · Intel Quartus · ModelSim · Git · Simulink · GEM5 · AWS