14nm Process Flow Final Project

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***Abstract*— This research paper will go into detail about he process flow for a 14nm FinFET. It will detail each and every step of the process which includes deposits and etching methods of different sorts. For example, lithography etching and RIE. We will use an automated tool flow in a CMOS fin shaped transistor.**

Keywords—FinFET, Etching, Deposit, RIE, LIT, Coventor

I. Introduction

When it comes to creating advanced technology nodes for transistors, a very detailed process and number of steps is involved. Transistors have very fine nanometer characteristics that are optimized and designed for particular circuits. To be able to do this on such a small scale in a factory takes a process flow that is unique and lengthy and one that uses multiple techniques to accomplish this. One of the biggest challenges faced by designers is to factor accurately a devices variability during the process flow and orientation of the gates, drain and sources. Each design has different widths and lengths that create a wide variety of changes that affect the electrical properties. Some are due to different phenomena such short channel effects. To ensure that each transistor is made to specification, a factory's process flow is precise and done in a certain way each time. Scaling of a planar CMOS below 14 nm would be significantly more difficult, but not impossible due to electrostatics, excessive leakage currents, and mobility degradation. Not to mention fabrication issues involved with it. Throughout this paper, these steps will be listed and described in detail as to how a 14nm FinFET is made step by step and will also highlight the complexity of different techniques. The tool used to create the FinFET and steps is Coventor Simulator 3D.

II. Step 1: Wafer Setup

A. Silicon Foundation

To start with, a small block of material is used as the basic foundation of the finFET process. This material is known as silicon. The pure form of silicon is the best use as of right now in semiconductor technology due to its atomic structure and its conductive properties. It has properties which is consistent of a conductive metal while simultaneously acts like an insulator which can block electricity. In short, this unique ability of silicon makes it the perfect switching material which is what is needed for an ideal semiconductor. Of course, there is no such thing as ideal, but it comes very close. Below in Fig 1 we can see the starting block of silicon used in step one of the process flow for the finFET.

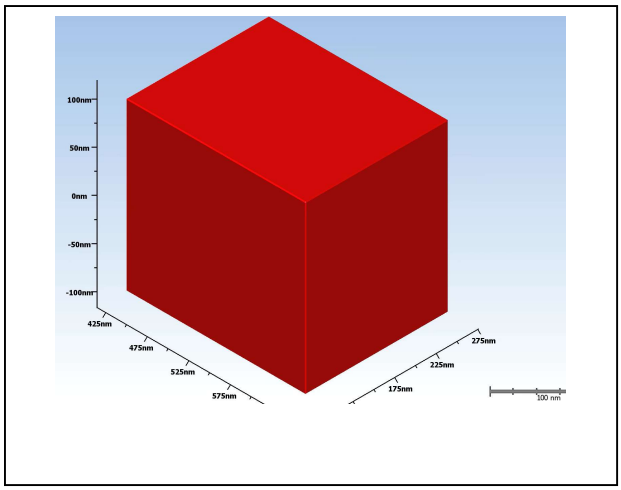

Fig 1: Silicon Foundation

III. Step 2: Front End of Line

This step is known as step 2 of the process flow and is mostly dealing with the fins of the FinFET. Not only will almost all techniques occur in this step, but we will also get to see more than just the creation of the fins. This is where the gates, sources, and each of the drains will come into creation. The reason is due to the proximity of the fins and the facts that each of these pieces that make up a semiconductor is directly in contacts with material around the fins. Some of the focus areas will be around the process used such as deposits, etching, and lithography techniques to create each of the items listed above. This entire step is most commonly referred to as Front End of Line in the process flow integration

A. Step 2.1: FINS

The fins in a finFET is arguably the most important part of the semiconductor design. This is the biggest difference between the planar design and the finFET. Overtime, as the fins get designed better and better, the industry comes closer to overcoming the worst short channel effects of submicron transistors some of which includes the drain induced barrier lowering. Because of these effects, it was difficult to get voltage to deplete under the channel and stop the flow of carriers turning off a transistor. When the industry adopted fins that were above the channel, they were able to add tri-gates which wrapped around the sides and thus, increased the control of carriers with it.

One of the main key points to the design of the finFET fins, was its ability to choose the drive strength of the device. This is important as the device gets smaller and reaches minimum sizes because then the options of how to approach getting the desired drive strength are easy depending on application needed. For

example, changing the height of the fin was one option that was easily attained by depositing more material. The second option was to increase the width of the fin which was also as easy as depositing more material and etching to finish. A third option was to add more fins to the device and while that adds more surface area, it was still an option due to self-alignment techniques.

To create the fins in the finFET, Coventor has two main steps in the process flow. The first step, is the creation of the fins, mostly through deposits, as seen below in Fig 2.

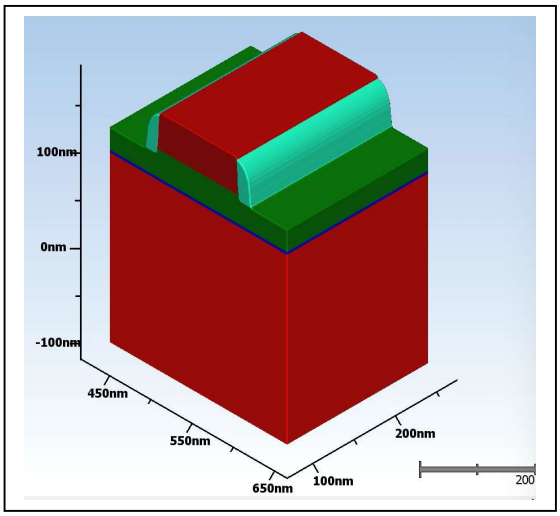

Fig 2: Fin Creation

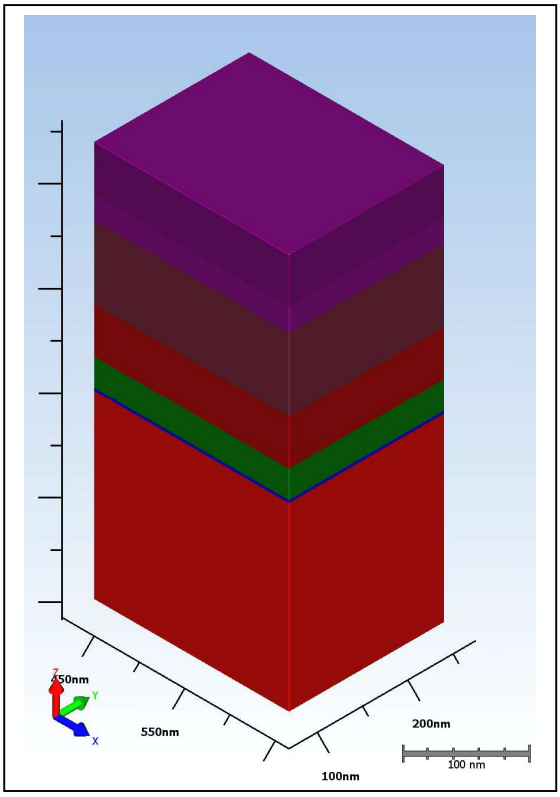

Fig 3: Stacked Deposit Layers

The fins are made through an eleven sub step process. The first of these sub steps is done through deposits of different materials. Layer one is to deposit an even layer of oxides and silicon on top of the silicon foundation. Then, after that, a deposit of nitride is padded and layered evenly over the oxide and silicon. The reason for the materials used, silicon and nitride, is to use them as a metal diffusion barrier that stops the chemical mechanical planarization of metals.

The next steps in the fin making process flow is to make the mandrels. Mandrels are used both as spacers and supports of the fins while they are being cut. It starts with the another depositing layer of silicon that is flat. The next deposit is an ODL mandrel layer that stands for Optical Dispersive Layer. This layer acts to refract portions of light which will become important during the etching phase that is used to cut the fins out later. This layer is also flat along with the next deposit layer of Si-ARC. This is a special silicon layer that has ARC, or anti-reflection coating that is important to be paired with ODL layers before. When this material is used as a secondary mask that is patterned, it forms new shapes and openings to the nitride layer. This is also paired with another light resistive organic material that is layered flat on top of the ARC layer. This stacked deposit of layers is easily shown in Fig 3 below in order from bottom to top, starting with the thin blue layer to the darker purple layer on top.

Now, we can move on to the light etching processes to etch away the mandrel portions of the deposited layers to ensure a clean cut process for etching the actual fins of the semiconductor. The first process is known as lithography. This is where a highly complex and precise machine will draw circuit patterns on a photomask and exposed on a silicon substrate wafer. To do this task, a lithography system must have three key components to be able to get to 20 nm or less. The first key component is the projection lens that a machine uses. This lens must have the best resolution possible if more intricate circuits are to be patterned onto the wafer. The more power to the lens, the better the performance of the optically transferred pattern. The second component is the alignment sensors of the machine that aligns each mask and substrate. This is especially important because the silicon wafers and photomasks are swapped multiple times throughout the pattern process that any mis-alignment would ruin the design completely as the process is irreversible. The last major component of the lithography system is the exposure rate. This is also important as this plays into the time factor of making the patterns. Since the patterning is done multiple times over, the quantity of wafers that get exposed faster is critical to production. Fig 4 below shows the lithography machine and each critical component.

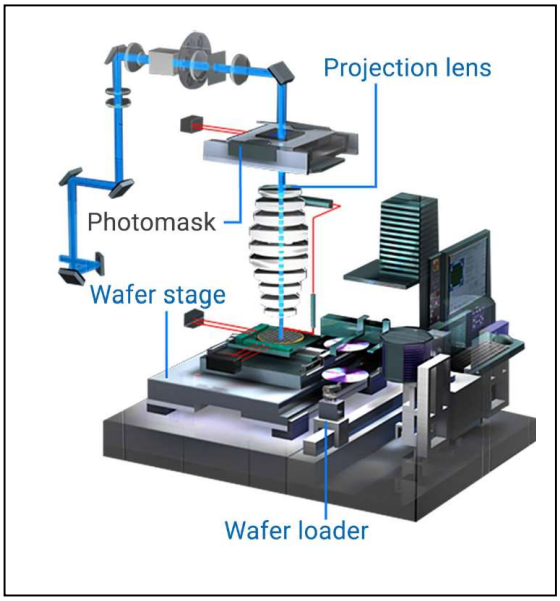

Fig 4: Lithography Machine

The next technique that will be used in the etching process is known as RIE which is also known more commonly as Reactive Ion Etching. This is a unique process that consists of plasma etching technology. How it works is it uses a chemically reactive ions that are accelerated at the silicon substrate to remove specific deposited materials from the previous steps. With RIE technology, a variety of raw materials can be etched away. Dielectric materials such as silicon dioxide and silicon nitride for the gates. Silicon materials such as poly silicon, which is heavily used in semiconductor manufacturing. Even metals such as aluminum, copper, and titanium can be etched away. It is also useful in etching gallium arsenide which is gaining attraction in the industry as a silicon substitute due to its charge carriers being faster. Fig 5 below shows the machine that applies a RF power to a vacuum unit to create an electric field which ionizes gas molecules.

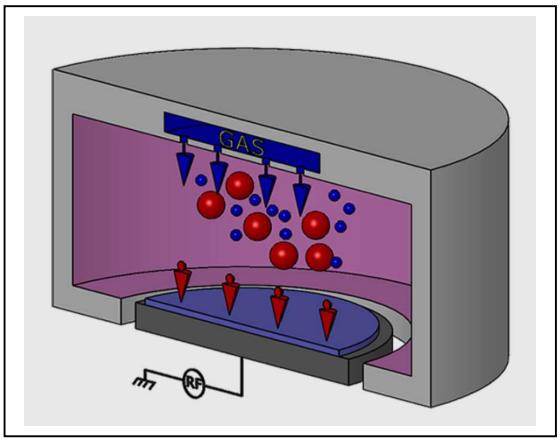

Fig 5: RIE Machine

To start the etching of the mandrel layers, the lithography technique is used to remove part of the top deposited resistive layer. Then, the RIE technique is applied to remove both the Mandrel resistive layer along with the silicon ARC and ODL layers. This leaves behind a desired shape and portion of the silicon in the middle to be used as a base for the fins. Finally, a small layer of oxide is deposited as a spacer for the desired space between the fins and etched away using RIE. The final result is the same as Fig 2 above which is the creation of the fins before it is cut into shape.

B. Step 2.2: Fin Cuts

The second step in the FEOL is to cut the created fins into their geometrically named shape. This step will etch away the material until the fin has its desired pitch and height. For the simulation, coventor has made two fins during the etching process. The first step in the cutting process actually begins with depositing a a resistive layer of material to pattern out where should be cut for each fin. The next step with use a Lithography technique to etch way the depth for the first fin. The second step is to use a RIE etching to take away the spacer oxide layer deposited from the previous steps. From here on out, RIE will be the main technique for etching away material until the fins are finally cut. The mandreals will be all taken away. Following that, the padded nitride deposits will be etched away. Then the padded active resistive material will be etched away along with the padded oxides layers which leaves behind the fins. This final fin cut result is viewed easily in Fig 6 below.

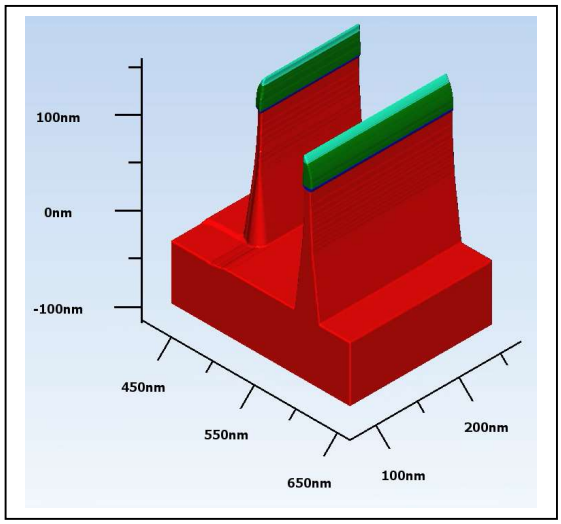

Fig 6: Fully Etched Fins

As you can see, the height of the fin is roughly 155nm tall and the pitch between the two fins is around 120nm. The thickness of the fin directly correlates to its short channel behavior. The height controls current flow between the source and drain through the channel beneath them and increases proportionally with the fin's height. The sum of a fins height and the width of the fin are multiplied by a factor of two gives the electrical width of the finFET design.

C. Step 2.3: Wells

The wells are a very important part of making the CMOS transistors. To achieve a CMOS where you have both NMOS and PMOS on the same type of wafer, we can use wells that will be diffused on a different substrate. For example, diffusing a N-well on top of the P-well substrate. For Coventor modeling, the simulation uses a P-substrate with an N-well and P-well. To do this procedure of making wells, we start by depositing a screening oxide layer over the fins and silicon. Usually done with silicon dioxide barrier to act as a diffusion of n-type impurities and protect against portions of the wafer against contaminates. Another protective PSPD layer is also deposited on top of the oxide layer. A photo sensitive emulsion layer for the P-well is then deposited to allow selective etching of the P-well. A final layer of masking and open stencil is then applied to the surface of the resistive layers and exposed to UV light. This is where the lithography technique will etch away part of the P-well resist layer to create the N-well. From here, the RIE etching process will be used to remove the PSPD poly layer along with the rest of the P-well photoresist layer. The step following this is the deposit of the NSPD poly layer immediately followed by etching it away with the RIE technique. A rapid thermal process, or RTP for short hand, is then used to create the well drive and dopant activation as well as thermal oxidation and silicide barrier forming. Once that process is done and the thermal heating is cooled slowly to prevent shock and breakage, the RIE etches away the remaining SPD poly layer to leave behind the wells and fins of a finFET seen in Fig 7 below.

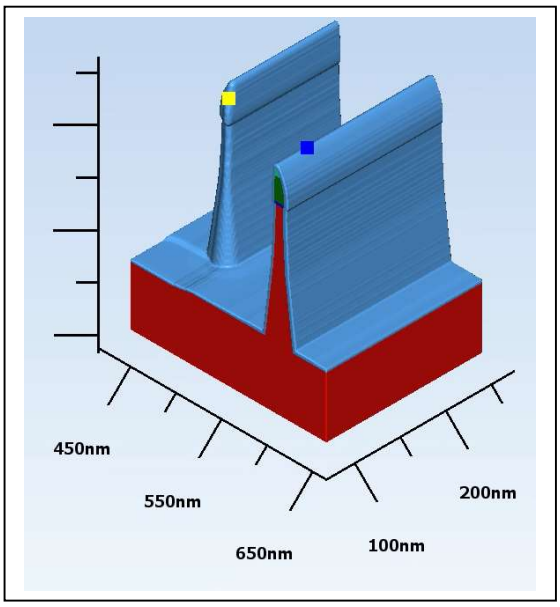

Fig 7: Wells Added to FinFET

D. Step 2.4: STI

STI is what is known as Shallow Trench Isolation and has been a key factor in the making of FETs below 100nm. The reason why STI is so important is because of how it can prevent electric current leakage between two semiconductor devices. This became an important achievement due to the limitations of the manufacturing process as designers tried to make smaller and smaller components. As the surface area was being reduced, too many components were causing issues due to being so close with other components. As designers developed this trench, they also filled it with a nonconductive layer that would further help prevent leakage. .Although the process of making an STI sounds simple, the reality of it is that it is a very difficult process to pull off at the sub-micron level during manufacturing. The fist step in the Coventor simulation for making an shallow trench isolation well is to deposit an STI HDP layer. The HDP is high density plasma which can also be a chemical vapor deposition. This will help with the etching process done by chemical mechanical planarization or CMP for short. The CMP is a process that etches away material by using chemicals and abrasives along with a physical metal polishing ring that is about the same size as the wafer. The reason that this polishing is necessary is because after the planarization is done and the surface area is flat and free of irregularities, the wafer can now be within the field of vision for lithography. This setup and increased surface area can allow for more circuits on top. From here, RIE is used to reduces and etch away a small excess amount of the deposited STI HDP so that it is below the tips of the finFET fins. Then, a more broad technique of etching, known as wet etching, is used to clean the HDP. It will also be used to clean and strip away the padded nitride that sits on top of the fins for the finFET. The final result is a shallow trench isolation that will help prevent leakage of electricity due to excellent dielectric protection. This is very important to have this feature at 14nm node and will help with the relative position of each component such as the gate, source, and drain. The final result of the STI process flow steps can be seen in Fig 8 below.

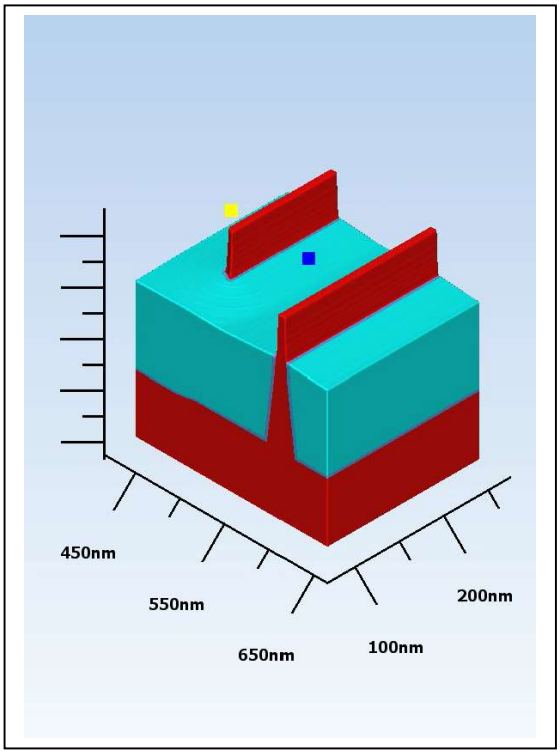

Fig 8: Shallow Trench Isolation

E. Step 2.5: Gates

The gate is one of the three most essential parts that makes up a transistor right alongside the source and the drain. In finFETs, it is a long task to make the gates due to the amount of steps alone in this part of the process. This is mainly because of how the gate is placed due to the addition of a fin vs the planar transistor where the fin is flat and flush with the source and drain. In a finFET, the gate is wrapped around the fins and oriented in a way that is perpendicular to the fins. The gate is placed and layered over the entire channel and between the drain and the source. The result of this is that finFETs can now have multiple gates surround the very slim channel and deplete charge carriers much more efficiently. This is a major accomplishment because it can help control electrostatic problems much better inside of the channel. This, along with low threshold voltage and reduced power dissipation, is the main benefits of using a finFET over the planar transistors.

For the purpose of the process flow, the simulation done in Coventor has wrapped the gate around the two fins in the 14nm finFET model. The steps start off with multiple depositing layers of different oxides. The first deposits are self-aligned contacts oxide and the self-aligned contacts silicon for the gate. Self-aligned contacts, or SAC for short, is a technique used in the process flow that adds a dielectric layer over the gate of the transistor and is a protective element to prevent contact to gate shorts. Recently, with how small the area of contacts is getting and the gate length does not scale, the total working spaces for the landing area length is not meeting the requirement for the contacted poly pitch. However, with SAC, the contacts can now land extremely close or even on the top of the gate without causing a short. This means the scaling of the contacted poly pitch can increase which will minimize the yield loss of misaligned contacts over the gate. However, a downside of using SAC is that the lack of distance between the contacts and gate make for a situation where the contact capacitance increases considerably.

Once the SAC material layers are deposited, they are etched out by RIE to make a smooth surface layer again. Again, More oxides and nitrides are layered, but this time it is for the creation of the gate caps. The caps are protective layers from the contacts that separate them from the gates. This is then planarized and an ODL, or organic dielectric layer, is placed on top to create an isolation layer that will prevent the contacts from shorting with the gate. Finally, the gate material is deposited on top which consists of a silicon ARC and a photoresist masking layer that will have the pattern so that the lithography can etch away the undesired parts. We can see the layers reach above 400nm and that they are stacked before any etching is done is Fig 9 below.

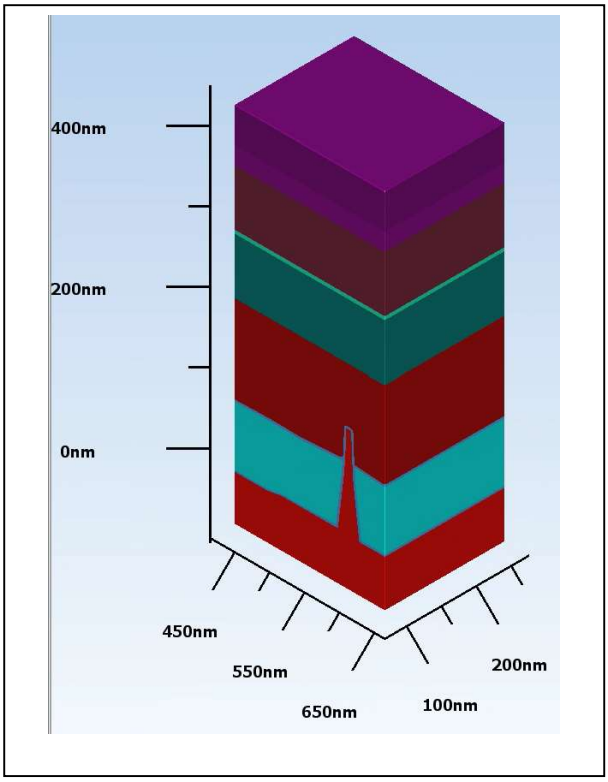

Fig 9: Stacked Gate Deposits

The next steps to come is all of the etching steps that will take place. The first is the lithography process that will etch away material rom the photoresist layer into the desired gate shape pattern. After that, the RIE technique will be utilized to remove most of the hard mask that could not come off with lithography. It will also remove the layer of resistive material that masks more of the gates shape in the oxide and nitride. Again, this is a long process and making the shape of the gates is no easy task. To continue further, deposits of more ODL and silicon ARC layers are placed and another photoresist

mask is made into pattern. This is needed for the final Gate cuts to make sure that they do not destroy the fins which are underneath the newly formed gates. The lithography will again, take the ODL material off while RIE removes and etches away the harder resist masks and materials. Finally, a WET abrasion and etching process is used to clean up the surfaces and polish the material to remove impurities. The final gate wrap around fin cut can be seen in Fig 10 which shows it being reduce back down to a max height of around 315 nm.

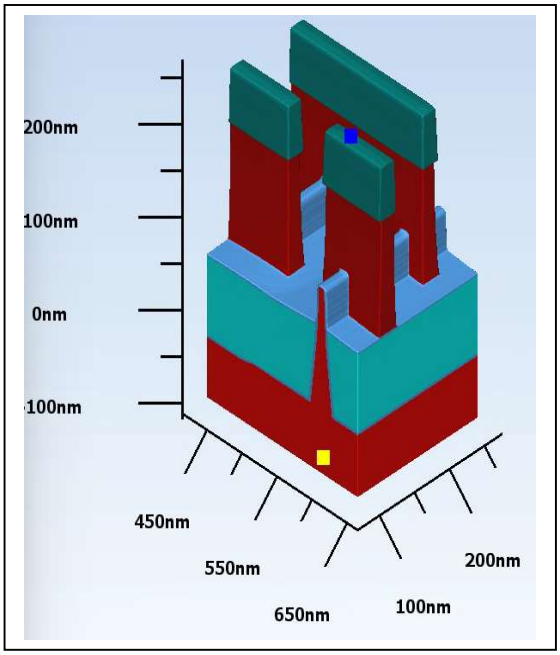

Fig 10: Final Gate Creation

F. Step 2.6: Source and Drain

The Source is the second part of the important trio that comes after the gate in terms of creation in the process flow. The primary goal of the MOSFET is to control the flow of voltage and current that goes from the source and drain terminals. An almost ideal capacitor is formed at the gat and is a vital part of this process. When a small voltage is applied to the pseudo capacitor and the gate is positive voltage, a depletion region is created. This formation attracts electrons from the source, drain, and N-well. This forms an electron reach channel and current will flow between the source and drain if current is applied. The gate will control the magnitude of electrons also known as Vg. If a negative voltage is applied, what is known as a hole channel will be created underneath the oxide layer and the properties of how the source and drain change. The source to the gate voltage is now in charge of conduction of the current from the source to the drain and only if the voltage exceeds the threshold does the conduction begin.

To create the source and drain through process flow, there has to be two parts. The first part is to create the positive source and drain region. The second part is to create a negative source and drain region. The first step of part one is to always begin with the deposit layer steps. Here, we will deposit a spacer oxide, a spacer nitride, and a spacer photoresist layer for the pattern mask etching in that order. This will then be followed by using lithography to remove and etch the pattern left by the resist mask. The RIE etching process will then remove the remaining undesired spacer oxide and nitride layers and leave a small recess where masked off. This will also be followed by a WET etching as to smoothen out the surface and remove any impurities as the next step will be very important. In this next step. EPI is done with silicon germanium. EPI is what is known as epitaxy and is a high temperature process used to deposit the silicon germanium in selected areas for the source, drain, and channel. The silicon germanium is used specially for this because of how it offers high speed and high frequency for digital electronics and IC. The silicon in epitaxy is strained and have their atoms stretched beyond the regular structure of the atom. This longer stretch gives a channel higher electron mobility and thus results in a transistor having faster switching speeds at low power. This is the finish part of actually making one part of the source and drain regions which can be seen in Fig 11 below.

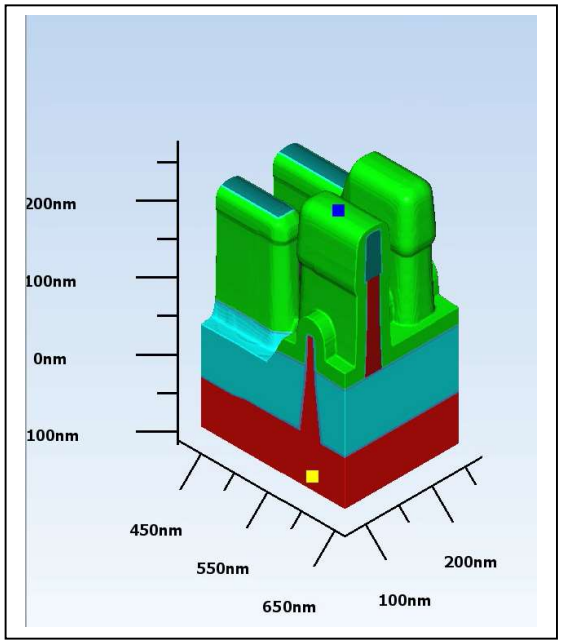

Fig 11: PSD

Making the second part, which is the NSD, is the same process as before in part one. This is just done on the other half of the fins. The first steps again are to start with the deposit of materials for spacers. This includes depositing spacers of nitride and the resistive photomask that will have the new pattern. There is no oxide layer this time because there was some left over that was deposited from the first part of this process. The lithography will etch away the circuit design and remove that part of the resistive layer. RIE will then etch away the rest of the not wanted layers leaving only a small recess behind again. WET will do a fine abrasion and polishing to

remove irregularities and even the surface of the remaining layers. Finally EPI will be used to selectively place silicon carbide this time. The reason silicon carbide instead of the SiGe is due to it having properties that include a voltage rating of over 600 volts and a wider temperature rating. The final Source drain creation can be seen below in Fig 12.

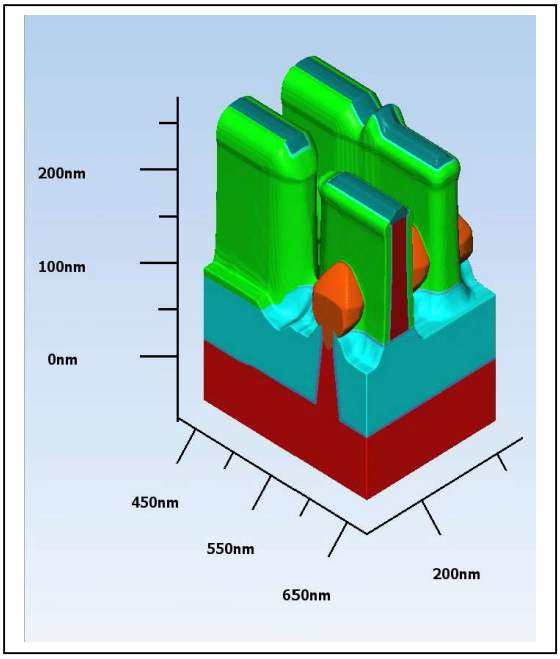

Fig 12: Full Source/Drain Creation

G. Step 2.7: Replacement Metal Gates

Replacement metal gates have become an industry standard after the 45nm node and smaller were created and are exactly what they sound like. RMG is a process that has many advantages like preventing damage from various etches to the gate underneath and providing more stability to all the materials it surrounds. It also gives better thermal protection from thermal processes and it improves the overall performance of device. The negatives of RMG technology is that it relies heavily on CMP which can have defects the more times it is used. It can incorrectly adjust final gate heights, metal flakes, etc. All of which can cause adverse effects like leakage in the channel or incorrect carrier current or resistance.

To start off with, a deposit of interlayer dielectric layer is formed to fill opening or sometimes go over a sacrificial layer which consists of many silicon oxides. Below is Fig 13: which shows the Coventor starting point after the deposited oxide layers in a light blue color.

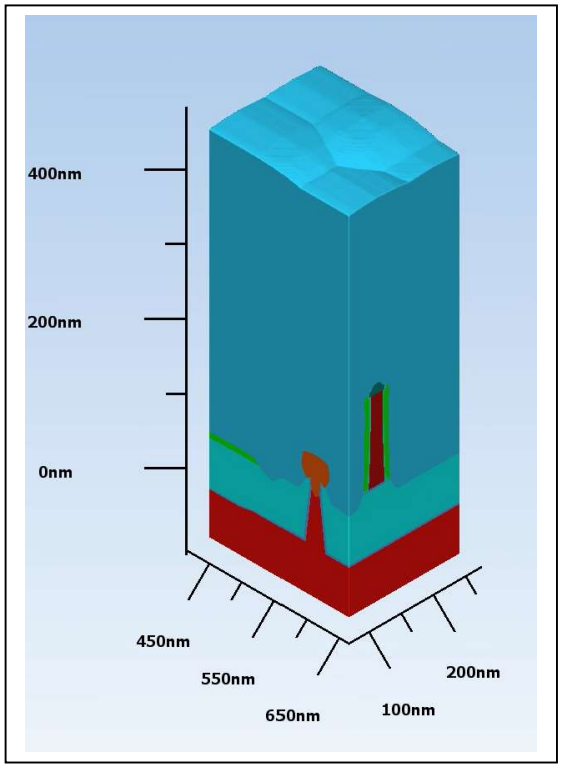

Fig 13: Replacement Metal Gate Deposit

From here, multiple etching process will be used between the RIE techniques and CMP for additional etching of the metal and also polishing. First is a CMP process to remove the bulk of the oxides and metals so that it is just over the surface of the gates for exact height measurements as this is critical it does not remove more than necessary. In this case, the height of the gate is 120nm and can also be seen in Fig 14 below.

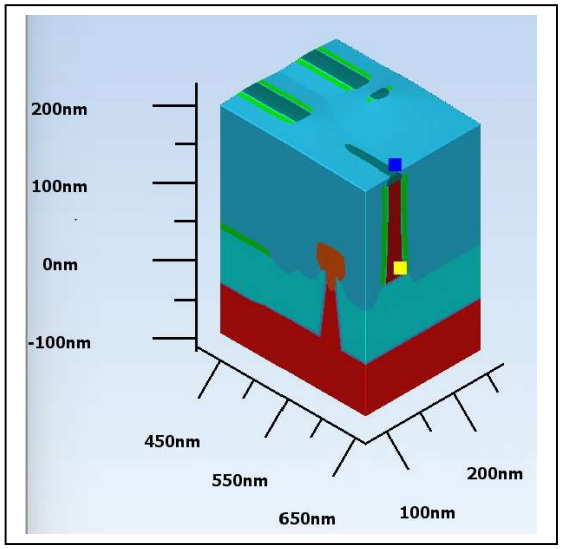

Fig 14: Selective CMP Removal

RIE is then used to remove the selected and non- selected patterns from multiple masks to create spaces for the next step which is the WET etching of the sacrificial gate. It will also remove whatever oxides are remaining inside the gate trenches and polish off that area for the next set of deposits. The first deposit is a dielectric material with a high K, or kappa, value which is also a high dielectric constant. This is some material that is better than silicon dioxide. The next step is to deposit a titanium nitride layer which is a ceramic material good for physical vapor deposition. Following that, is a deposition of tantalum nitride which will act as a diffusion layer between a masking photoresist layer. Lithography will etch away the required pattern to be left behind and then RIE will remove the material completely. Now, another deposit of metal, specifically titanium aluminum will be layered first along with tungsten. The final CMP etching will take place and remove undesired materials and polish the surfaces of the metals to remove any imperfections and irregularities on the surface. Finally, a gate plug, made of nitride, will be placed in the trenches and RIE will remove material until it is level again. The final RMG result is shown in Fig 15 and is an amazing transformation from what was started with in Fig 14.

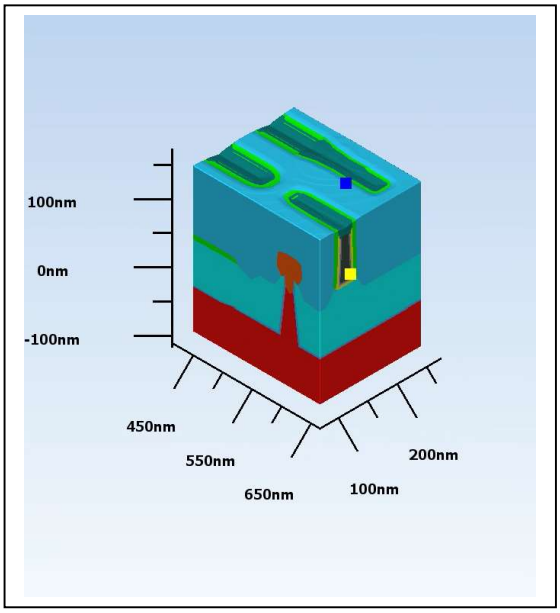

Fig 14: Replacement Metal Gate Creation

IV. Step 3: Middle of Line

Middle of the line is the third step of the process flow for creating a finFET. This step always comes after Step 2 which is the Front End of Line and is generally considered to be the hardest of the three parts. This is due to the many defects and limitations placed on the process from FEOL and BEOL. The first step in the process is the metallization of the contacts. This is critical to make sure that the contact resistance does not lower to make a short. To ensure that this does not happen, designers have made a two step process to add contacts. The first is contact to active or trench silicide. This is an interference space material of silicide that is deposited over the entire source, drain, and gate. On top of that is the deposit of titanium nitride and then tungsten. These are then etched away using RIE and WET etching processes along with CMP for polishing the trench. The second layer is then filled with a tungsten plug that is sandwiched between the titanium liners and the titanium nitride barrier layer. Using this overlay strategy is important because it determines the overall performance of the wafer and measurements can be taken to send feedback where wafers are worse. These wafers can then be corrected based on more exposure and overlaying techniques to mitigate any contact resistance. The final result if done correctly is shown in Fig 15 below. This is the final finFET and the end of he process flow for the 14nm node. A full list of steps can be shown below in Fig 16.

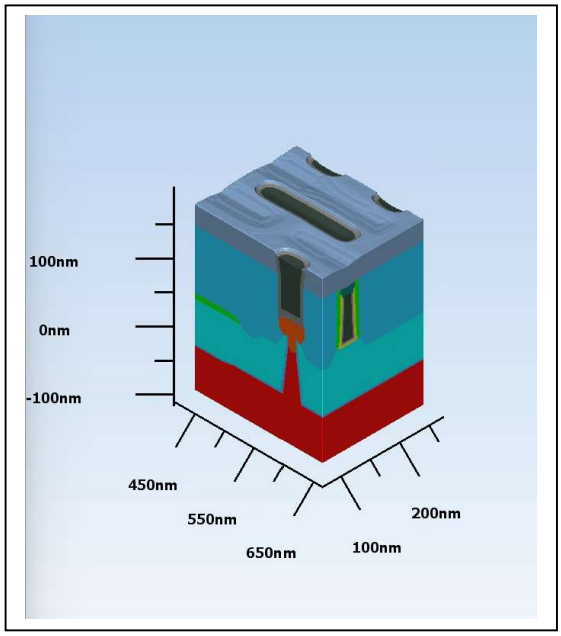

Fig 15: Final FinFET

Fig 16: Coventor Simulation Process Flow

CONCLUSION

To conclude the process flow, all that is left to do it extract the devices if it was successfully made. This will then move on to bulk production and yield. Overall, there are many different techniques that can be used and as time goes on, most of these process will change to accommodate the challenges that arise for smaller and smaller nodes. The process is ever changing and if Moore's law holds true, there will be many more challenges to overcome in the FET process flow.

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