Assignment 5: 4x4 Multiplier (LUNA-CiM)

Stephen Singh
Herbert Wertheim College of Engineering
University of Florida, Gainesville, USA
Email: singhstephen@ufl.edu

***Abstract*—This report presents the design and optimization of a 4×4 multiplier using the Divide and Conquer (D&C) method, specifically tailored for low energy consumption and minimal area overhead. The proposed design, termed LUNA-CiM (Low-energy and area-efficient Unified Multiplier Architecture with Carry-in Memory), focuses on optimizing the number of Static Random Access Memory (SRAM) storage cells to achieve enhanced performance metrics. Leveraging previously crafted circuits including full adders, half adders, buffers, and inverters, the LUNA-CiM multiplier aims to provide superior efficiency in terms of both energy consumption and area utilization compared to traditional Lookup Table (LUT) based multipliers. Through a comprehensive exploration of the D&C method and subsequent optimization strategies, this report demonstrates the effectiveness of the proposed approach in achieving significant improvements in performance metrics.**

***Index Terms*—4x4 multiplier, LUT-based multiplier, gpdk045, Cadence Virtuoso, power consumption, timing analysis**

I. Introduction

Multiplication operations are fundamental in various digital signal processing (DSP) and arithmetic applications, ranging from image processing to cryptography. However, conventional multiplier architectures often suffer from high energy consumption and significant area overhead, limiting their applicability in energy-constrained environments. To address these challenges, this report introduces the design and optimization of a 4×4 multiplier using the Divide and Conquer (D&C) method.

The D&C method is a powerful algorithmic technique that breaks down complex problems into smaller, more manageable subproblems, facilitating efficient computation with reduced resource requirements. By leveraging the inherent parallelism and modularity offered by the D&C approach, we aim to design a multiplier architecture that not only meets stringent energy and area constraints but also offers competitive performance compared to conventional LUT designs.

The proposed architecture, named LUNA-CiM, integrates optimization techniques to minimize the number of SRAM storage cells while maintaining high computational efficiency. This optimization is crucial for reducing both energy consumption and area utilization, making the LUNA-CiM multiplier suitable for a wide range of applications where resource efficiency is paramount.

In this report, we detail the design methodology of the LUNA-CiM multiplier, including the utilization of previously crafted circuits such as full adders (FA), half adders (HA), buffers (BUF), and inverters (INV). Finally, we present a comparative evaluation of the LUNA-CiM multiplier against traditional LUT-based multipliers, showcasing its efficiency and effectiveness in practical scenarios.

II. Methodology

A. Expanding 2x1 MUX to 6-bit

To accommodate 6 bits in a 2x1 MUX, we replicate the 2x1 MUX six times, each taking its own bit as input and outputting its own bit. Subsequently, we create a symbol representing this arrangement and utilize Wide Wire and Buses notation to enable a single symbol to accept multiple bits.

B. Creating 4x1 MUX 6-bit

We transform the 6-bit 2x1 MUX into a 4-input, 1-output MUX (4x1 MUX) using the formula $N - 1$, where N is the number of inputs. In this case, for a 4-input MUX, we require $N - 1$, 2:1 MUXes which means a grand total of 3 MUXs. For visual representation, refer to Figure 1 for the schematic diagram of the 4x1 MUX 6-bit.

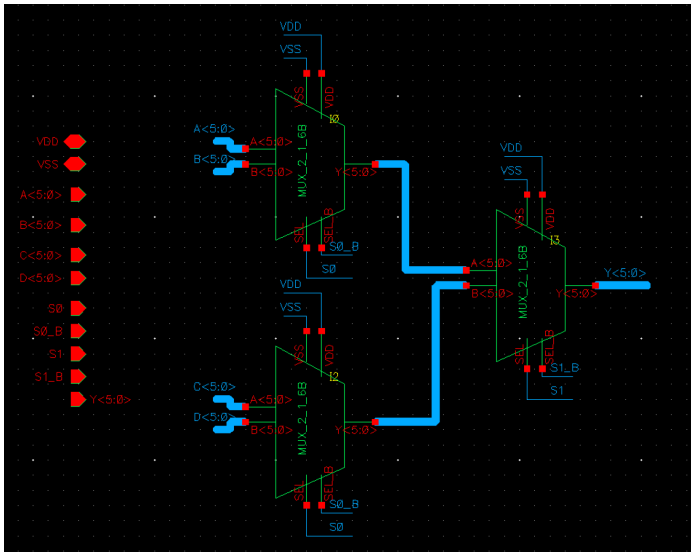

Fig. 1: Schematic diagram of the 4x1 MUX 6-bit

C. Component Design

1) NOT Block: The NOT block takes input from operand Y and employs multiple inverters to produce signals for the two 4:1, 6-bit multiplexers. For instance, LS0 represents the original signal from Y¡0¿, while $LS0_B represents its inverse. This goes for each of the other three Y inputs.$

2) Multiplication Block: The multiplication block constitutes the 4x4 Multiplier, an optimized version of LUNA-CiM, comprising several key components previously designed in other assignments. These components include 3 full adders, 3 half adders, 2 buffers, 2 4x1 MUX 6-bit, and the NOT Block. To enable seamless integration of these components, we utilize Buses and array format along with Wide Wire to facilitate the passage of multiple inputs and outputs through each block. The NOT block was made in the previous step and serves as the inputs for the 4X1 Muxs and will use the wire names L and M, such as LS0 and MS0.

3) 4x4 LUT Multiplier (LUNA-CiM Version): The LUNA-CiM version of the 4x4 Look-Up Table (LUT) multiplier utilizes the Divide and Conquer (D&C) method for low energy and area overhead. It optimizes the number of SRAM storage cells to enhance performance metrics. We will refer to the multiplication block here which has its 8 6-bit inputs, 4 Y inputs, and an 8 bit Output. From the assignment, we will be using a fixed weight of "1010" and then calculate the values of Wx00 to Wx11 and store them in storage elements. The storage elements are also previously created circuit designs known as TIE-HI and TIE-LO cells which can output a value of digital 1 or 0. The setup of the Vpulse which will give us our input of Y is seen below.

1) Y<3>:
   - Implemented as a pulse waveform with:
     - Minimum voltage: 0V
     - Maximum voltage: 1V
     - Period: 80 ns
     - Duty cycle: 50%
     - Rise time: 20 ps
     - Fall time: 20 ps
2) Y<2>:
   - Implemented as a pulse waveform with:
     - Minimum voltage: 0V
     - Maximum voltage: 1V
     - Period: 40 ns
     - Duty cycle: 50%
     - Rise time: 20 ps
     - Fall time: 20 ps
3) Y<1>:
   - Implemented as a pulse waveform with:
     - Minimum voltage: 0V
     - Maximum voltage: 1V
     - Period: 20 ns
     - Duty cycle: 50%
     - Rise time: 20 ps
     - Fall time: 20 ps
4) Y<0>:
   - Implemented as a pulse waveform with:
     - Minimum voltage: 0V
     - Maximum voltage: 1V
     - Period: 10 ns
     - Duty cycle: 50%
     - Rise time: 20 ps
     - Fall time: 20 ps

III. Results

A. Power Consumption

1) Static Power: The static power consumption of the 4x4 LUNA-CiM multiplier was measured to be 57.37 μW. Refer to Figure 2 for a graphical representation.

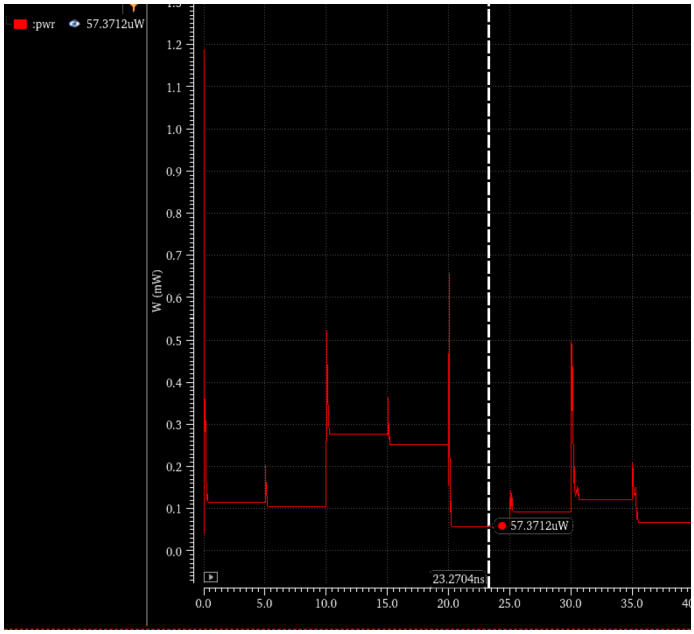

Fig. 2: Static power consumption

2) Average Power: The average power consumption of the 4x4 LUNA-CiM multiplier was recorded as 146.7 μW. For a visual representation, see Figure 3.

	Expression	Value
1	average(getData...	146.7E-6

Fig. 3: Average power consumption

3) Energy per Calculation: The energy consumed per calculation by the 4x4 LUNA-CiM multiplier, considering 16 inputs, was calculated to be 676fJ. Refer to Figure 4 for visualization.

	Name/Signal/Expr	Value
1	Y<3:0>	
2	OUT<7:0>	
3	Energy Per Calc	676.987f

Fig. 4: Energy per calculation

B. Input and Output Waveforms

The input waveforms consist of Y<3:0>generated using the Vpulse function, while the output waveforms correspond to

the signals OUT<7:0>from the multiplication block. Figure 5 illustrates the comparison between the input and output waveforms.

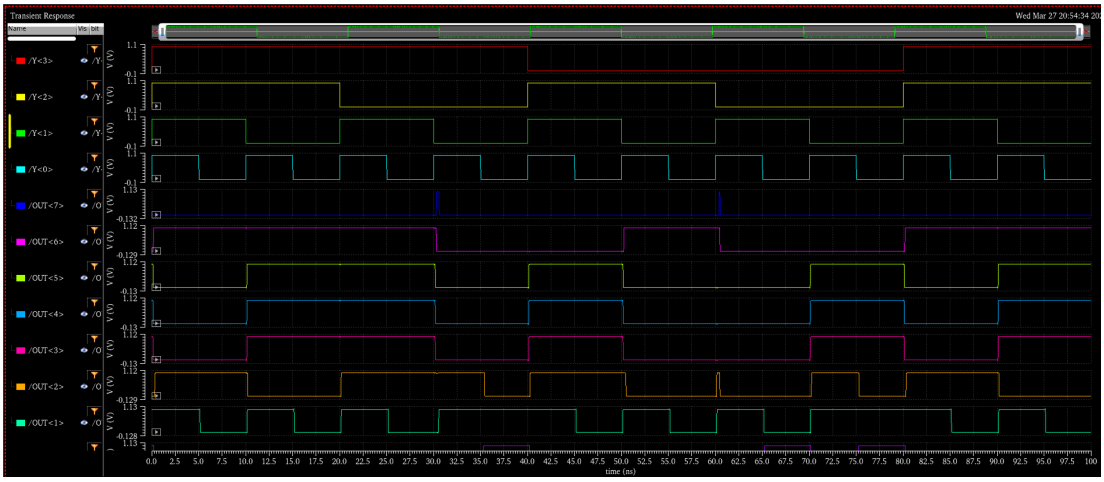

Fig. 5: Multiplier input and output waveforms

As depicted in Figure 5, the multiplication block, named "Stephen Multiplication," processes the input signals Y<3:0>to generate the output signals OUT<7:0>. The waveform pattern of the outputs resembles previous assignments' LUT-based multipliers, with similar characteristics. However, it is notable that one of the output signals exhibits higher spikes in this new multiplier compared to the previous designs.

IV. Conclusion

In this study, we designed and optimized a 4x4 multiplier using the Divide and Conquer (D&C) method, termed LUNA-CiM (Low-energy and area-efficient Unified Multiplier Architecture with Carry-in Memory). The methodology involved the integration of various components such as full adders, half adders, buffers, multiplexers, and inverters to achieve an efficient multiplier architecture.

The results indicate that the LUNA-CiM multiplier exhibits competitive performance metrics compared to traditional Lookup Table (LUT) based multipliers. The static power consumption was measured at 57.37 μW, with an average power consumption of 146.7 μW. Additionally, the energy per calculation was determined to be 676fJ units for 16 inputs.

Furthermore, the input and output waveforms comparison showcased the functionality of the multiplication block, labeled "Stephen Multiplication." While the waveform patterns of the outputs resembled those of previous LUT-based multipliers, it was observed that one of the output signals exhibited higher spikes in the LUNA-CiM multiplier.

In conclusion, the LUNA-CiM multiplier demonstrates promising efficiency and effectiveness in terms of power consumption and waveform generation. Future research could focus on further optimization techniques to mitigate the observed spikes in output signals and enhance overall performance.

APPENDIX

A. Part 2 4x1 MUX 6B Schematic

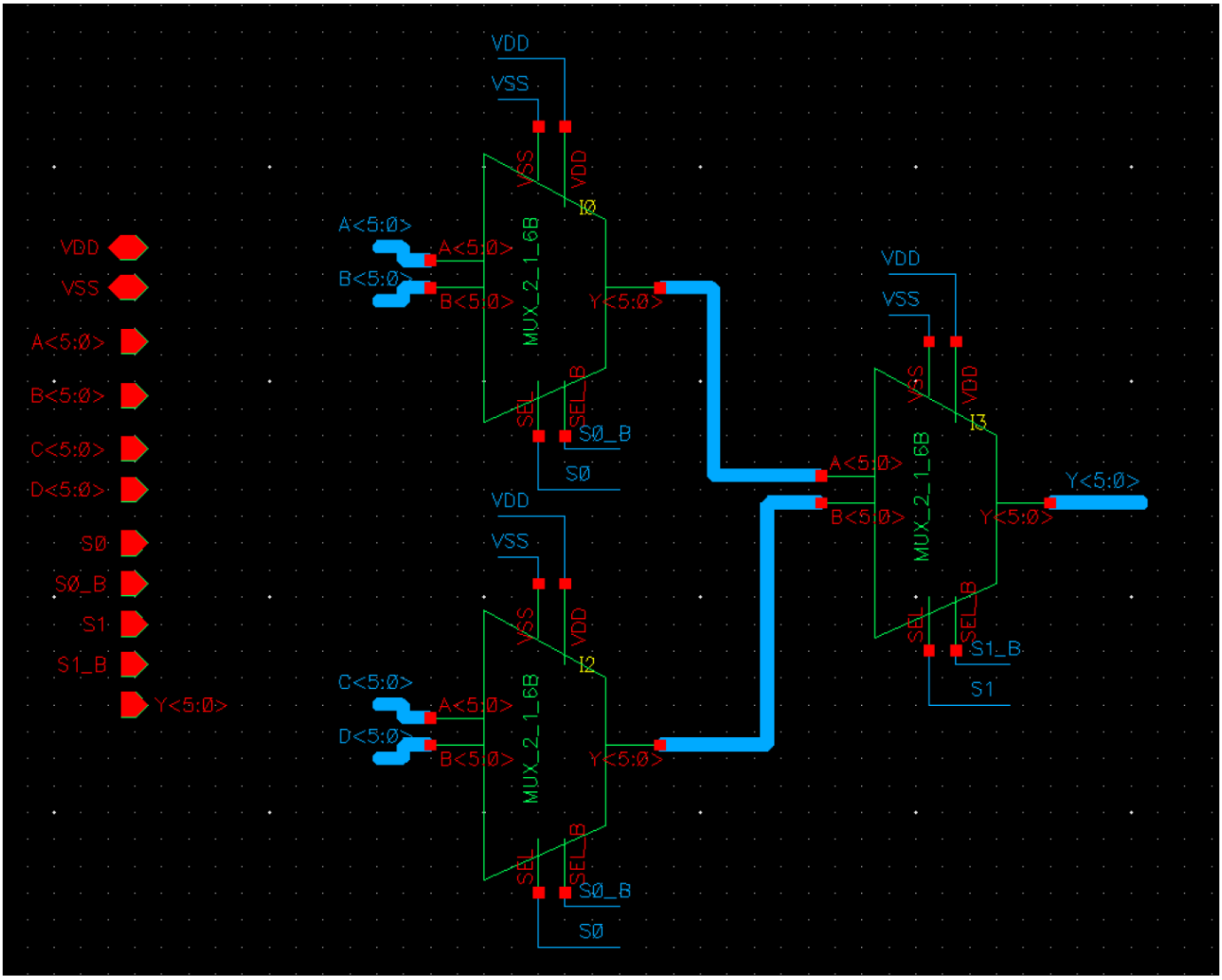

Fig. 6: Schematic of the 4:1 MUX 6B

B. Part 3 Average Power

	Expression	Value
1	average(getData...	146.7E-6

Fig. 7: Measured average power consumption

C. Part 3 Energy Per Calc

	Name/Signal/Expr	Value
1	Y<3:0>	
2	OUT<7:0>	
3	Energy Per Calc	676.987f

Fig. 8: Energy consumption per calculation per 16 inputs

D. Part 3 Input and Output Waveforms

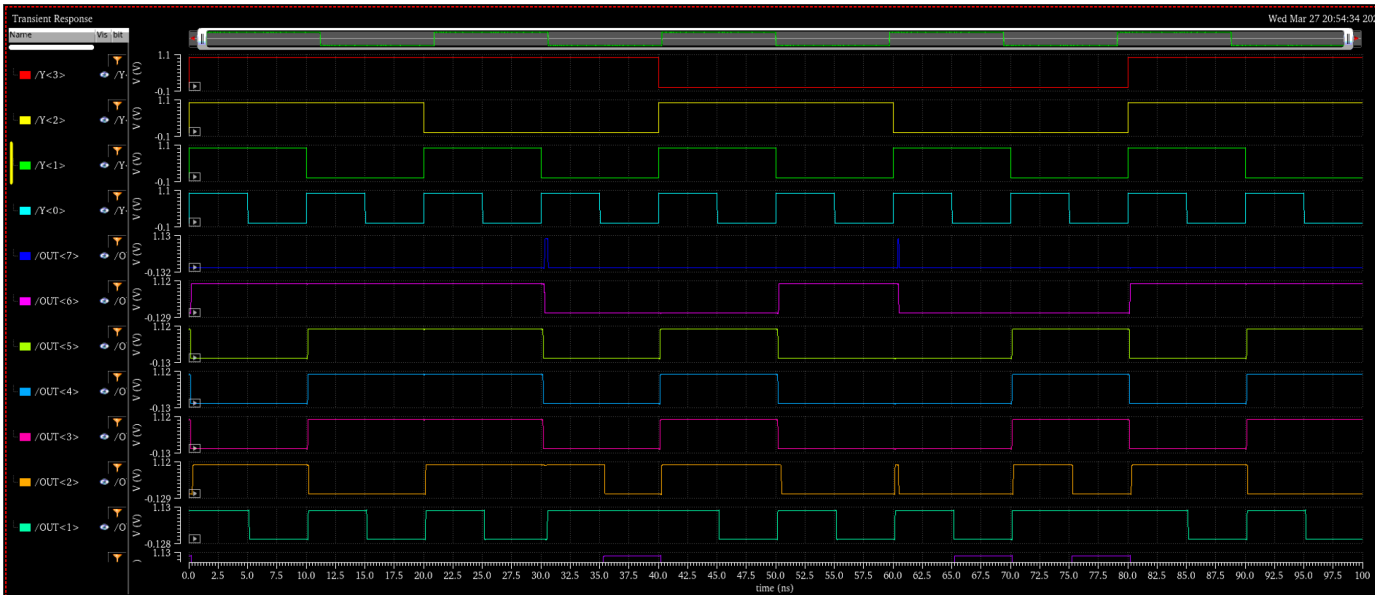

Fig. 9: Analysis Results Inputs and Outputs

E. Part 3 Static Power

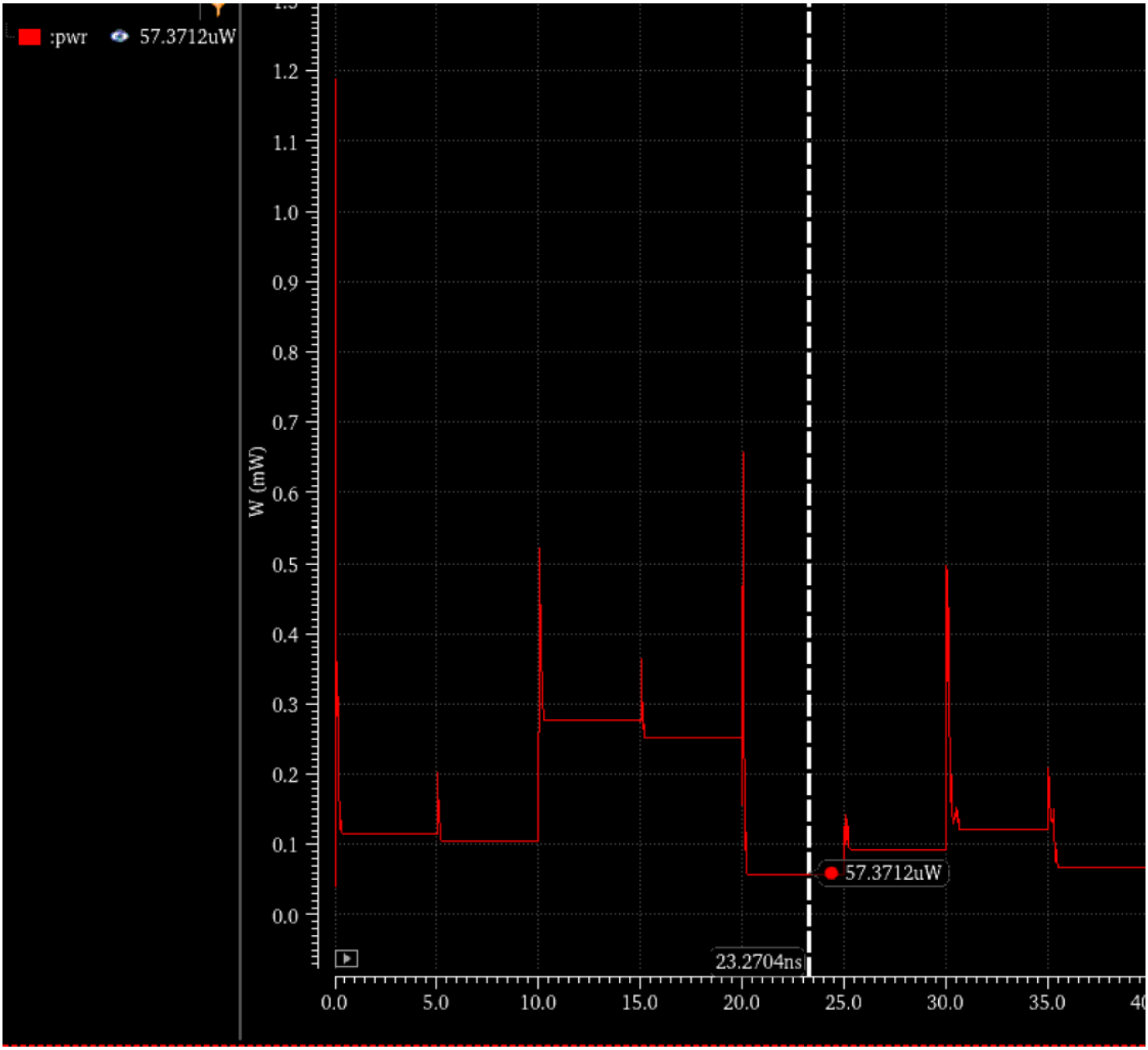

Fig. 10: Measured static power consumption

F. Part3 Schematic

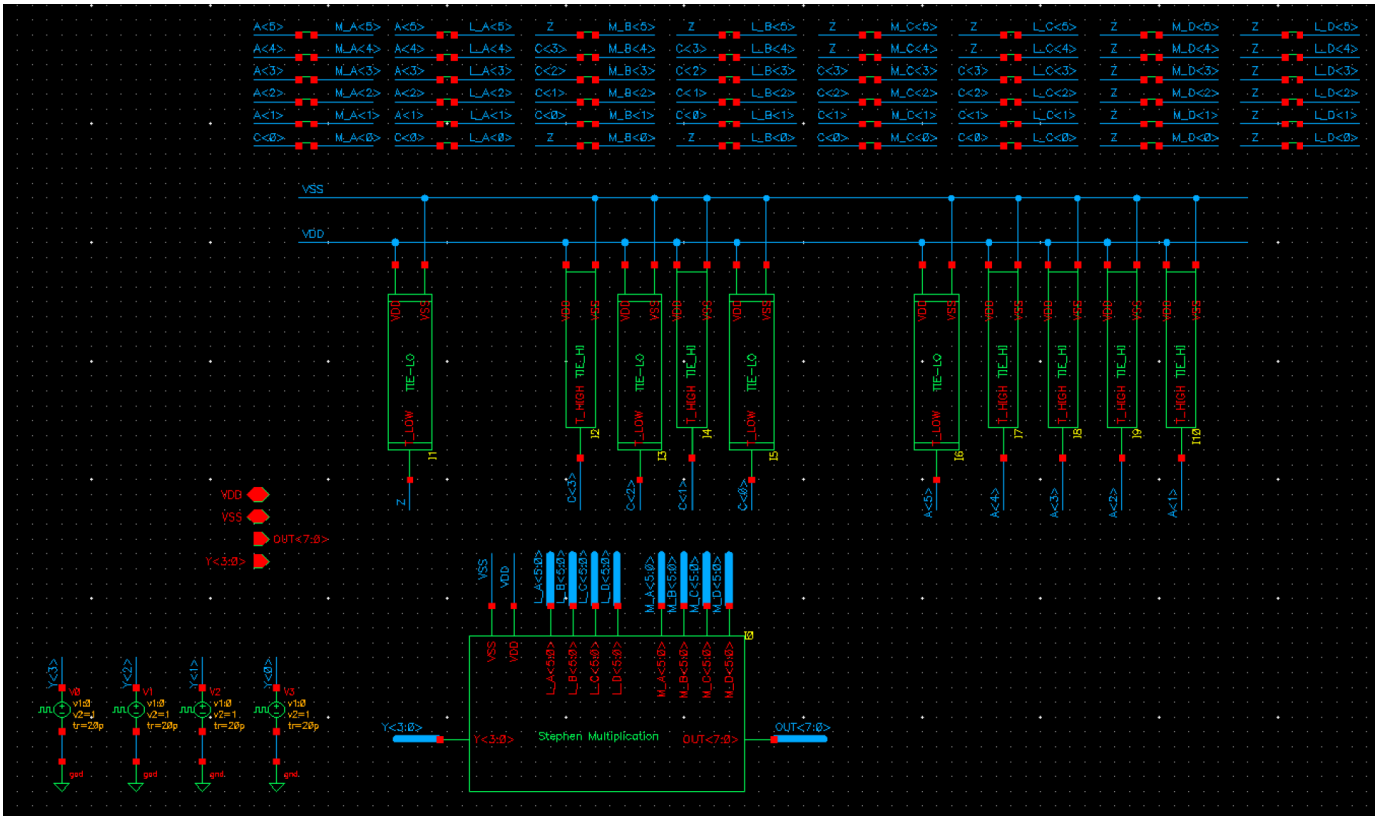

Fig. 11: Final Schematic of the LUT Based 4x4 Multiplier (Optimized version of LUNA-CiM)

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