

SRAM Design Project

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Abstract—The use of Static Random Access Memory (SRAM) has become standard in a variety of applications due to the low power and quick access time as well as coming in large densities. Such applications include SoCs for the competitive smartphone and laptop markets. Many of these applications require designs that fit in smaller and smaller IC footprints.

This paper will discuss all the transistor circuit components that make up an SRAM cell. It will then explore the custom 8-by-4 SRAM cell using the 45nm node technology. Cadence schematics and layouts will be shown and discussed as well as simulation results.

Index Terms—CMOS, SRAM, Decoders, 6T SRAM cell, Sense Amplifier

I. INTRODUCTION

The SRAM design is split up into several different components. Each of these components plays a role in the overall function of SRAM. An overall block diagram for the SRAM design in this paper can be found in Fig. 1 below.

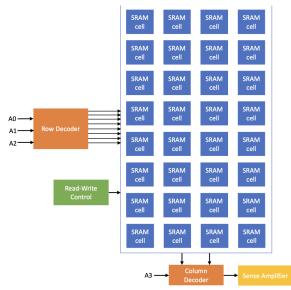


Fig. 1. Basic SRAM design

Fig. 1. Basic SRAM Design

The main building block for an SRAM is the SRAM cell, which stores a single bit of data. This bit of data can be accessed using the Row and Column Decoders. These circuits allow the bits stored to be read out or written two when the address inputs A0-A3 correspond to the row and column line for a particular cell. During a read operation, the column decoder will look at the change in voltage between the column lines of a selected cell. That potential is usually in the range of a couple of hundred millivolts. The sense amplifier will take that delta voltage and amplify that signal to be read out.

II. SRAM DESIGN COMPONENTS

A. SRAM Cell

A typical SRAM cell is made up of a certain number of transistors to create a certain number of cross-connected inverters. This SRAM design used six transistors. The 6T

SRAM cell for this design can be found in Fig. 2 above. The SRAM array is comprised of 8 rows where each made up of 4 6t SRAM cells. A single SRAM cell represents 1 bit of data that can be read or written to. Each bit is also accessed by 2-bit lines that are complemented.

The SRAM cell acts as a latch to store a single bit into the SRAM cell to be accessed later. The two inverters feedback to each other to store the bit as long as power is applied to the die. The pair of transistors on either side are the access transistors. The control of the access transistors is left to the bit lines and word lines. The word lines enable the access transistors and the bitlines sense the voltage difference between the inverters.

B. B. Row and Column Decoder

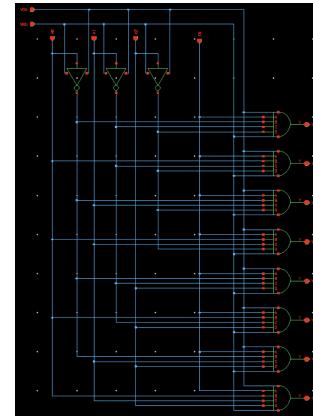


Fig. 3. Row Decoder Schematic

The SRAM chip set divides all memory locations into addressable locations. These locations can be accessed by any external application. The row and column decoders take the address input and translate them to bit line and word line configurations. The row decoder for this SRAM design has a 3-to-8 decoding scheme.

The row decoder is designed to trigger the word lines of the SRAM cell. The decoder can be designed with several basic logic gates. The schematic design for the row decoder can be found in Fig 3. above.

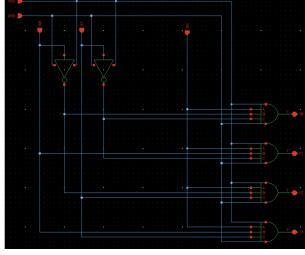


Fig. 4. Column Decoder Schematic

The row decoder is designed to trigger the word lines of the SRAM cell. The decoder can be designed with several basic logic gates. The schematic design for the row decoder can be found in Fig 4. above.

The column decoder schematic controls the bit lines for the SRAM cell.

C. Read and Write Control

The read-and-write control allows an external controller to either read or write to the SRAM cell. This is usually controlled by enable signals. These allow signals to change how the SRAM cell is used. The read enable will enable the sense amplifier and pre-charge the bit lines to pull down the addresses SRAM cell. The write will put a voltage on the SRAM cell to change the bits stored in the SRAM cell inverter. The read-and-write control design can be found in Fig. 5.

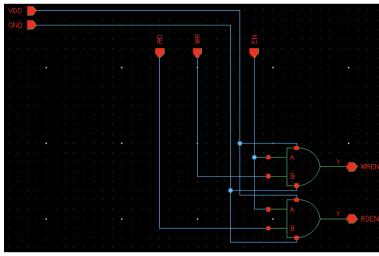


Fig. 5. Read or Write Control Schematic

The read/write control circuit contains two AND gates along with an enable port for both logic gates.

D. Sense Amplifier

Due to the small voltage difference between SRAM cell bit lines, a sense amplifier is needed. The sense amplifier measures the change in voltage between SRAM cell bit lines and amplifies the voltage. The sense amplifier for this design can be found in Fig 6.

III. SIMULATIONS

Several simulations were run to verify the functionality of the SRAM circuit. The simulations included verifying SRAM setup, pre-charge, writing, and reading transactions.

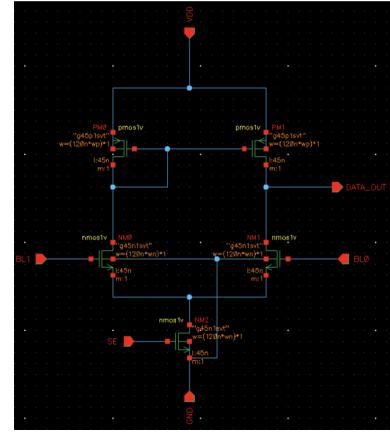


Fig. 6. Sense Amplifier Schematic

A. Setup

The simulations completed for this design were done using the Cadence ADE L simulation tool. Each component was simulated individually before fully assembling the SRAM array.

The simulations' stimuli included pulsing the read and write enable, changing address bits, and driving a clock. All transient simulations were plotted and checked for timing on reads and writes as well as correct signal transitions and edges.

B. Pre-charge

Before a read can occur, the bit lines for the addressed SRAM cell needs to be pulled up to the source voltage, VDD. This is done to reduce the time for a read voltage to transition between the logic '0' and logic '1' voltage thresholds. The bit line pre-charge is achieved by an enable signal that turns on the two bit line transistors. A schematic view of the pre-charge function can be found in Fig 7.

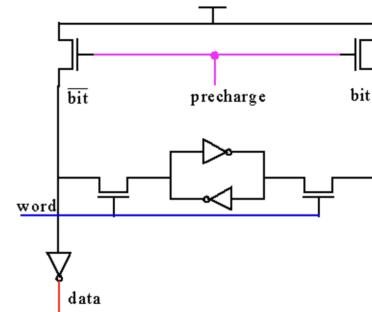


Fig. 7. SRAM Pre-charge behavior

The pre-charge for some SRAM circuits is implemented with a clock signal. This allows for external controllers to reliably pre-charge regularly. The clock signal pre-charge simulation can be found in Fig. 7.

C. SRAM Read and Write

SRAM write operations are used to overwrite the current bit stored in a particular address SRAM cell. The SRAM cell

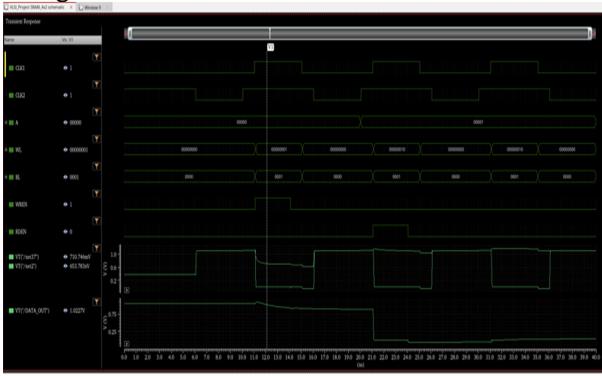


Fig. 8. SRAM Pre-charge simulation

can be written to with the following steps:

- Drive either bit line to VDD and the other to the ground.
- Word line goes to VDD.
- The SRAM cell inverter will be overwritten by a new bit line value.

For the SRAM cell design, those steps can be observed for a write of logic ‘1’ and logic ‘0’ at multiple addresses. This behavior can be found in Fig. 8.

SRAM read operations are used to read the current bit stored in a particular address SRAM cell. The SRAM cell can be read with the following steps:

- Pre-charge both bit lines.
- Word line goes to VDD.
- One of the bit lines will be pulled to ground.
- The change in voltage is read out of sense amplifier.

For the SRAM cell design, those steps can be observed for a read of logic ‘1’ and logic ‘0’ at multiple addresses. This behavior can be found in Fig. 9.

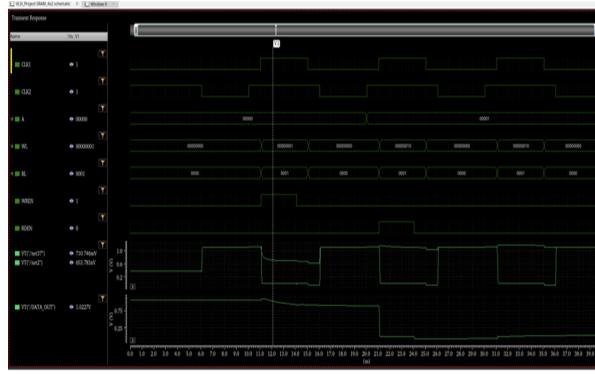


Fig. 9. SRAM Simulation

IV. LAYOUT

After the simulation was complete, all of the components were laid out using Cadence. The layout was done using the gpdk045 node library and followed the design rules for that technology node. These design rules are all found in the GPDK

45nm Mixed Signal GPDK Spec. Design verification using DRC and LVS checks were used for each layout.

A. SRAM Cell

The layout for the entire SRAM cell is done in a hierarchy method. The layout was broken into smaller design blocks and individually tested before integrating into the main design. The main design uses metal for the rails which include the power VDD and ground or VSS rails. Bit lines are also represented using metal-1. The gates of the transistors are connected using polySi material layers.

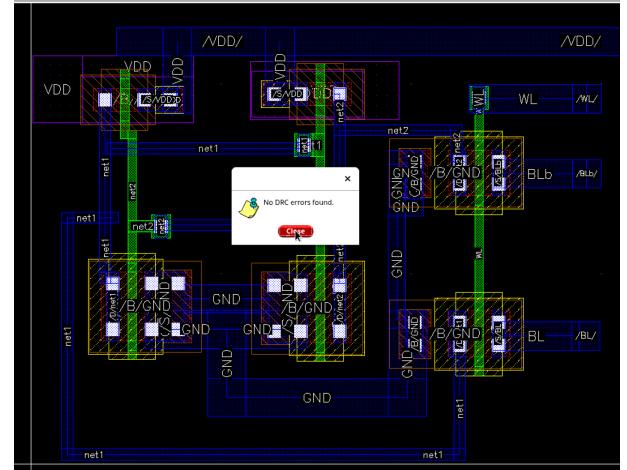


Fig. 10. SRAM bitcell Layout

B. Row Decoder

The overall row decoder layout can be found in Fig. 10. First, the NAND has to be designed along with the inverter. Once that is completed, they can be added to the decoder layout. Although we had similar patterns of keeping power rails at the top and ground rails at the bottom, it would have been a better design to make the decoder have common rails to halve the area required.

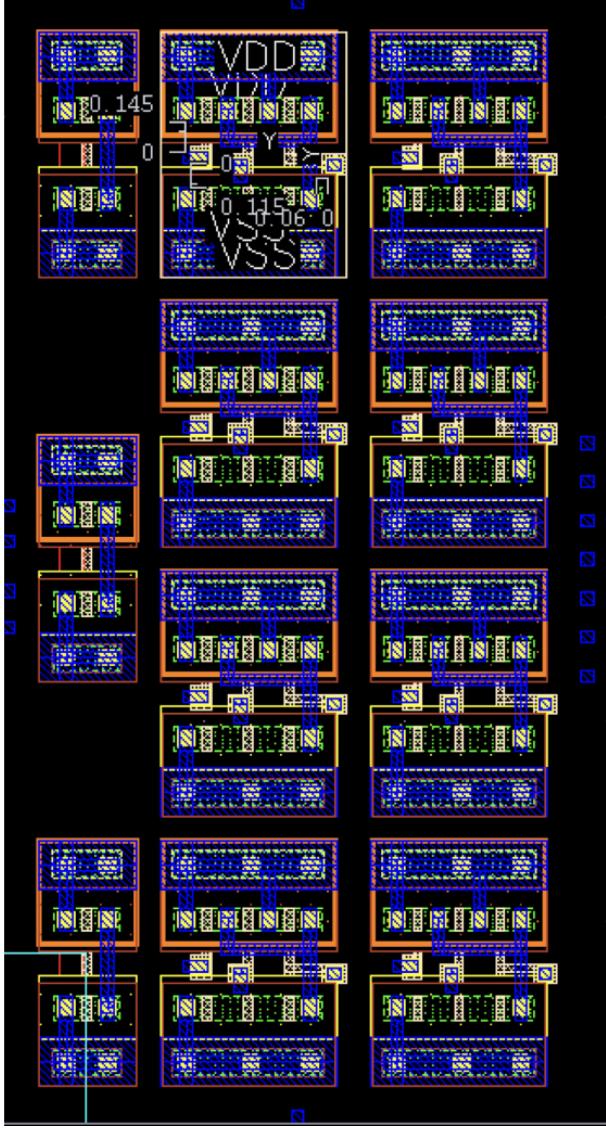


Fig. 11. Row Decoder Layout

This layout shows the AND gates and the inverters that make up the row decoder. An AND gate layout for this decoder can be found in Fig. 12. This layout is used throughout the SRAM design.

C. Column Decoder

The layout for the Column Decoder is similar, which a different number logic AND gates and inverters. The same AND and inverter layouts were used for those designs again. The column decoder layout can be found in Fig. 13.

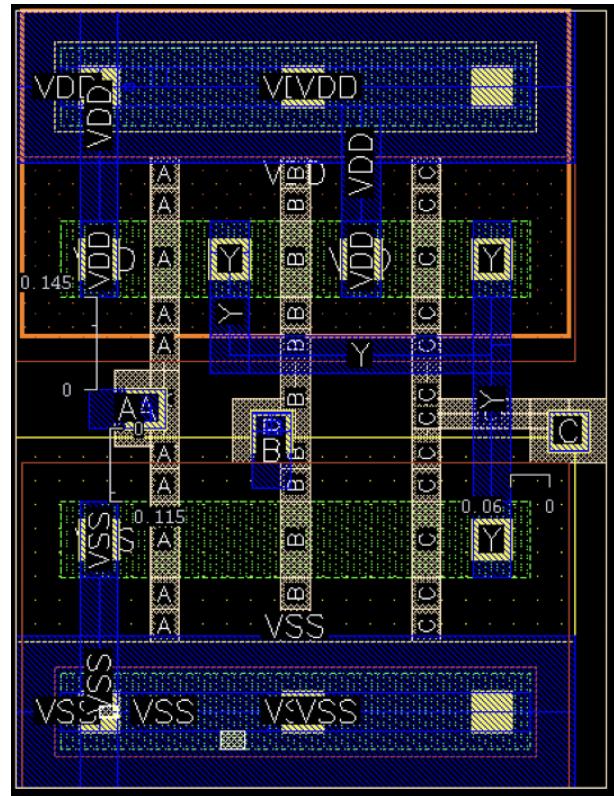


Fig. 12. AND Layout

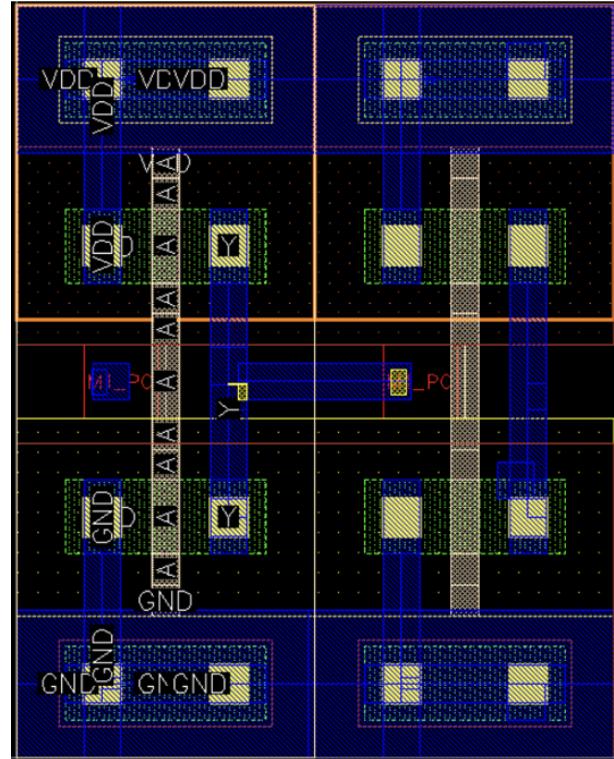


Fig. 13. Column Decoder Layout

D. Sense Amplifier

The sense amplifier layout design can be shown below in Fig. 14.

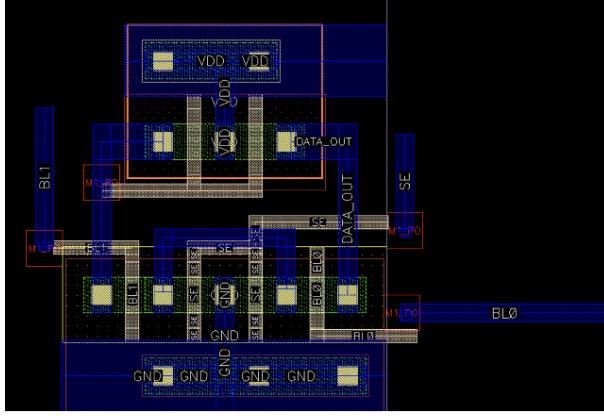


Fig. 14. Sense Amplifier Layout

V. CONCLUSION

The presented work introduces the working design and full layout of a 3 to 8 row decoder. This was accomplished using the 45nm technology design rules from TSMC CMOS technology. In conclusion, even though the current design is operational, improvements can be made to increase efficiency. For example, increasing the storage capacity or increasing the operating frequency of the design. Additional sense amplifiers can be added to the bit line which would be helpful due to capacitance increase from additional rows and a lowered voltage on the read of the SRAM cell.

VI. REFERENCES

- [1] J. IMP, VLSI Memory. [Online]. Available: http://ece-research.unm.edu/jimp/vlsi/slides/chap8_2.html. [Accessed : 08 – Dec – 2022].

VII. APPENDIX

A. Full SRAM circuit (8x4)

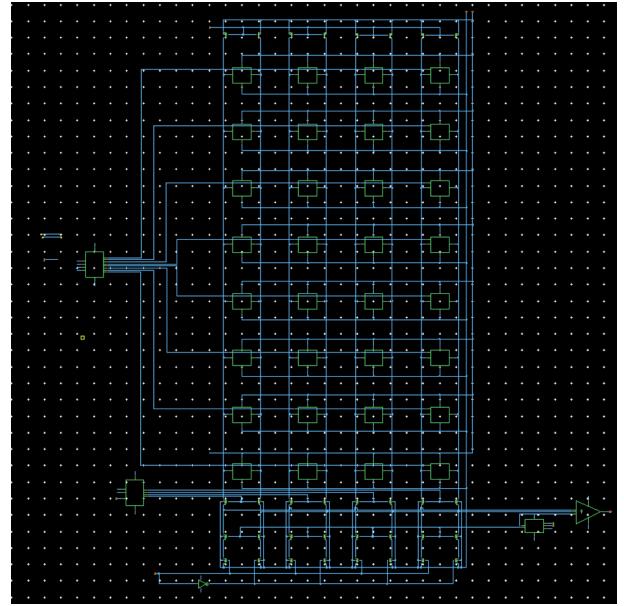


Fig. 15. 8x4 SRAM Schematic

B. SRAM cell DRC and LVS

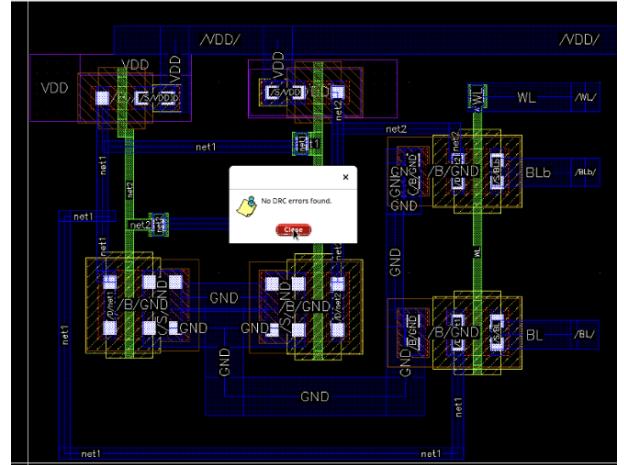


Fig. 16. SRAM bitcell layout clean DRC

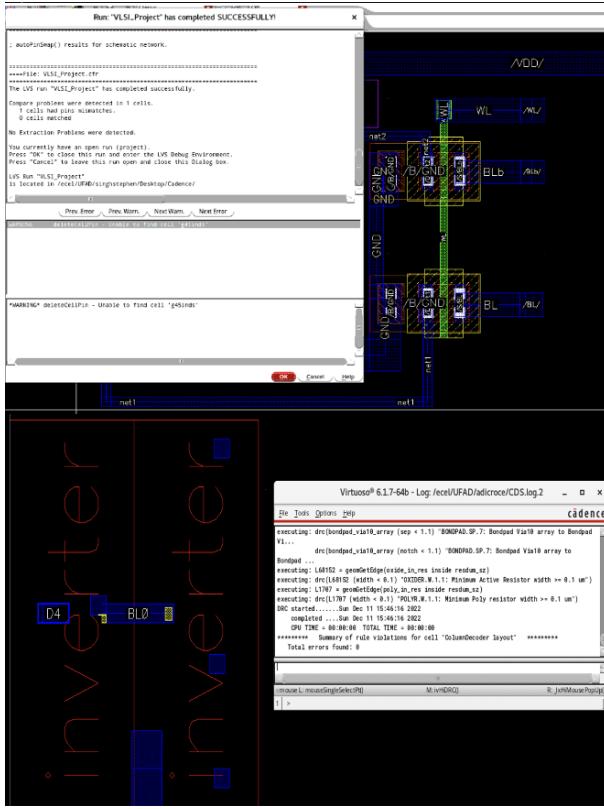


Fig. 17. SRAM bitcell layout clean LVS

C. Sense Amplifier DRC and LVS

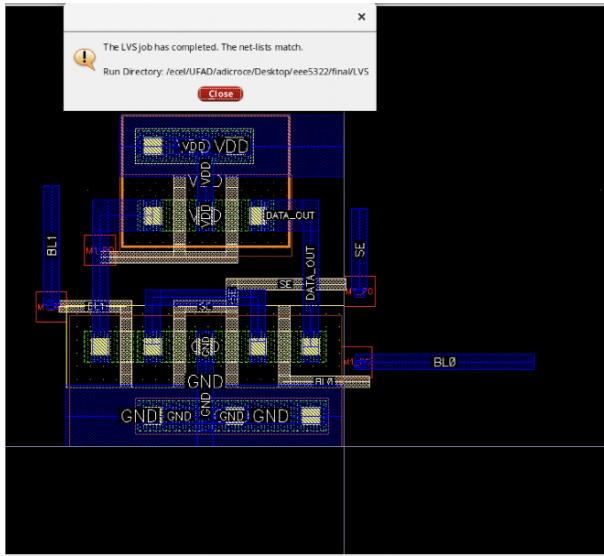


Fig. 18. Sense Amplifier layout clean DRC and LVS

D. Column Decoder DRC and LVS

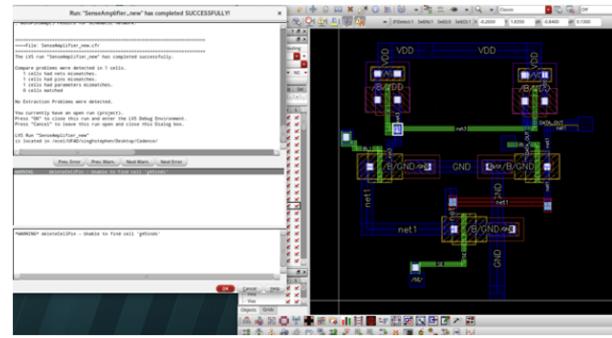


Fig. 19. Column Decoder layout clean DRC and LVS

E. Row Decoder DRC and LVS

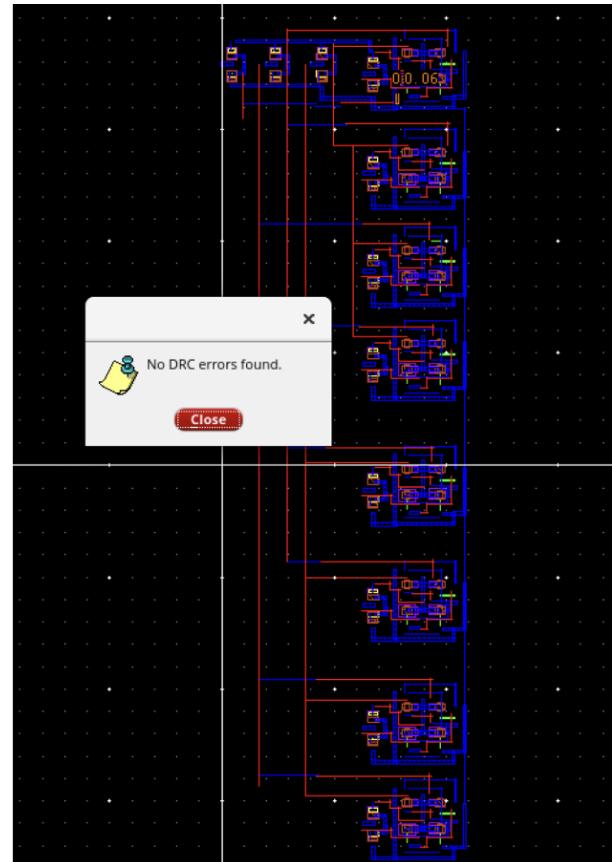


Fig. 20. Row Decoder layout clean DRC and LVS

F. Read and Write DRC and LVS

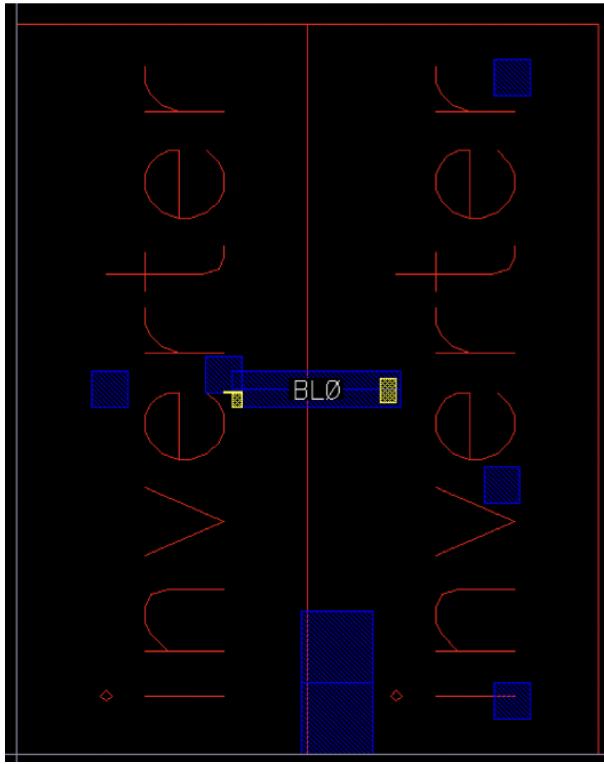


Fig. 21. Read and Write layout

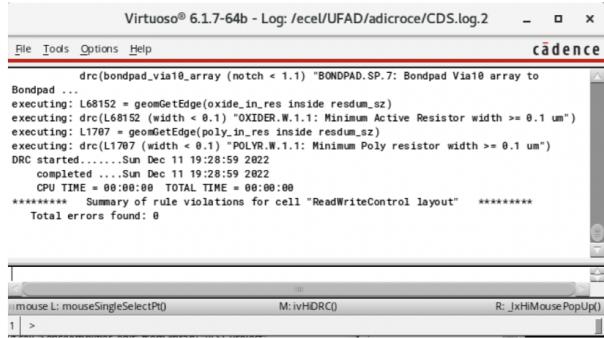


Fig. 22. Read and Write layout clean DRC and LVS

G. 8x4 SRAM DRC and LVS

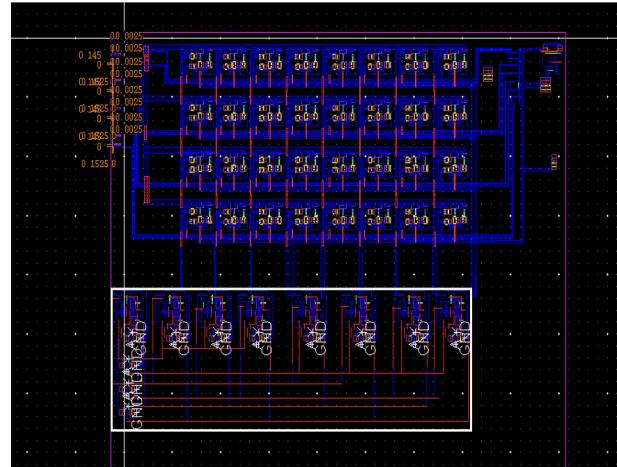


Fig. 23. 8x4 SRAM layout

VIII. WORK CONTRIBUTION

- **Aishwarya Bommireddipalli:** All the schematics, verified the 8x4 SRAM and Sense Amplifier Layout.
- **Albert DiCroce:** Column Decoder Layout and Report.
- **Alexandra Wright:** Completed the 8x4 SRAM Layout.
- **Stephen Singh:** Layout of SRAM Bitcell, DRC and LVS verification of rule violations for cell "ReadWriteControl layout" ***** Total errors found: 8