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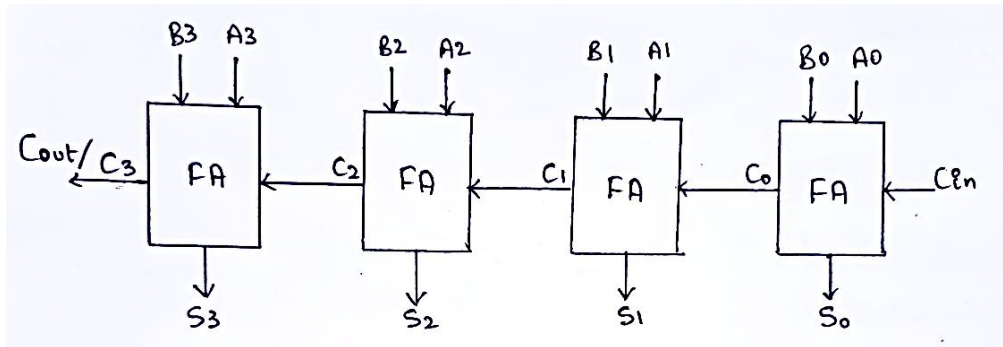
Experiment-2

Design a 4-bit full adder and subtractor and simulate the same using basic gates.

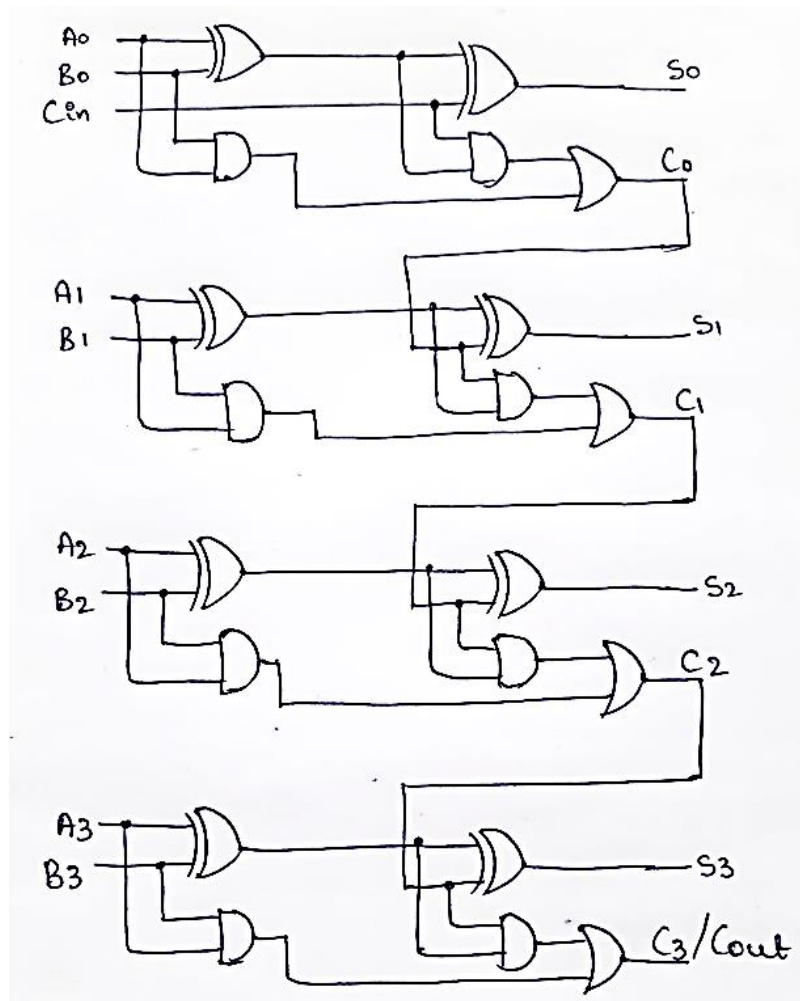
Aim: To design 4-bit adder, 4-bit subtractor and 4-bit adder-subtractor and to simulate the same using logic gates.

4-bit adder

Block diagram



Logic diagram



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1

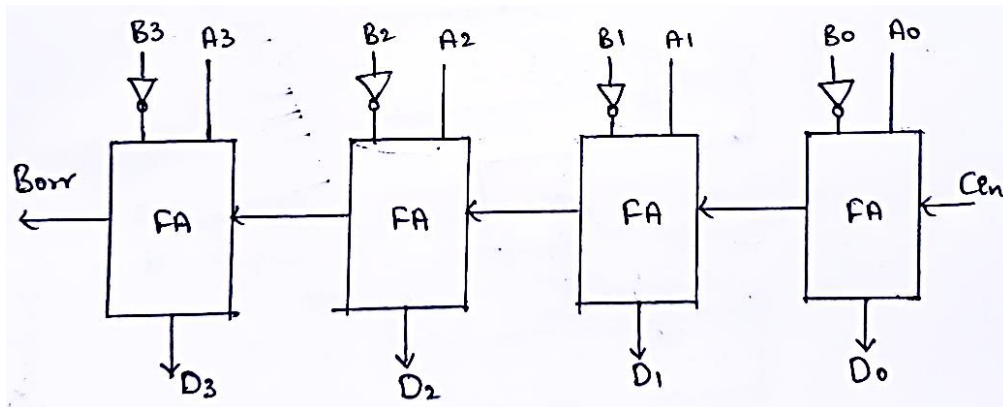
A -> 1 0 0 1

B -> + 0 0 0 1

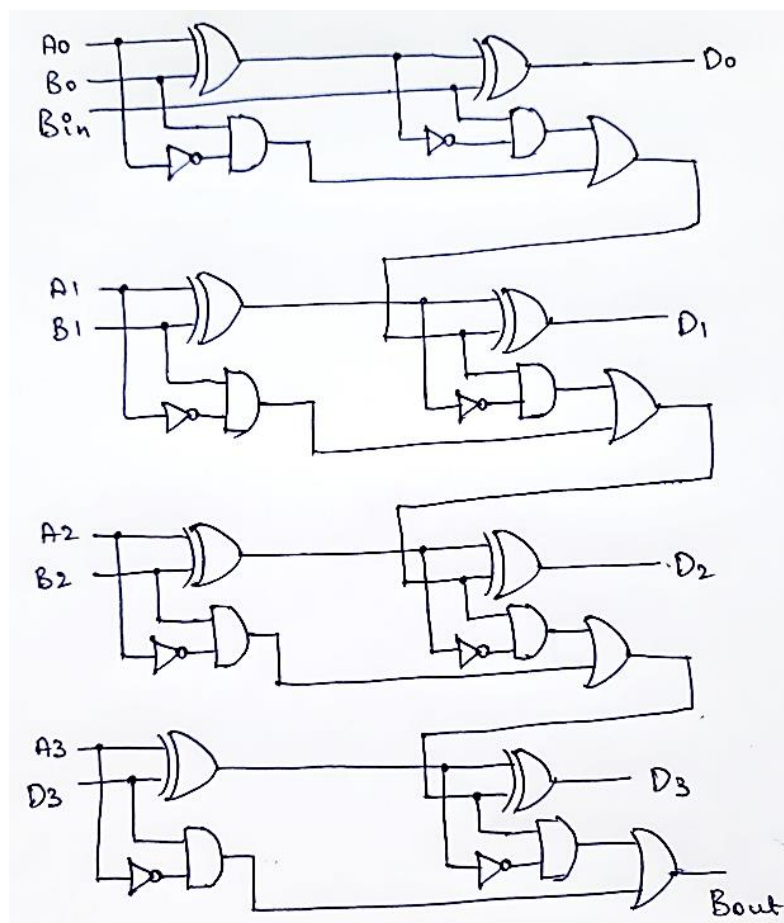
0 1 0 1 0

4-bit subtractor

Block diagram



Logic diagram



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A -> 1 0 0 1

B -> 0 0 0 1

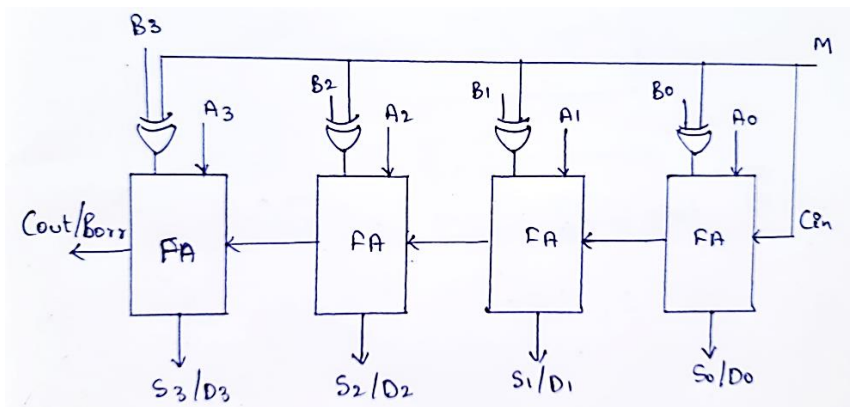
1's Complement of B -> 1 1 1 0

2's Complement of B -> 1's Complement of B + 1 -> 1 1 1 1

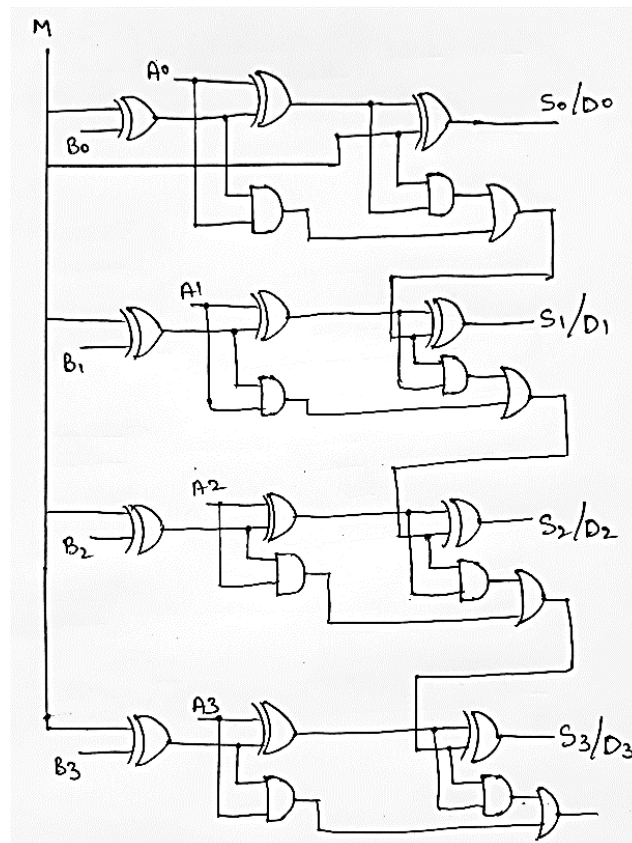
$$\begin{array}{r}
 A \rightarrow \quad \quad \quad 1\ 0\ 0\ 1 \\
 2's\ Complement\ of\ B \rightarrow +\ 1\ 1\ 1\ 1 \\
 \hline
 \quad \quad \quad 1\ 1\ 0\ 0\ 0
 \end{array}$$

4-bit adder-subtractor

Block diagram



Logic diagram





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M=0, Adder

M=1, Subtractor

Result: 4-bit adder, 4-bit subtractor and 4-bit adder-subtractor circuits are designed and simulated using logic gates.