KREATRYX

KNotes

ANALOG CIRCUITS

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Contents

Manual for K-Notes

Why K-Notes?

Towards the end of preparation, a student has lost the time to revise all the chapters from his / her class notes / standard text books. This is the reason why K-Notes is specifically intended for Quick Revision and should not be considered as comprehensive study material.

What are K-Notes?

A 40 page or less notebook for each subject which contains all concepts covered in GATE Curriculum in a concise manner to aid a student in final stages of his/her preparation. It is highly useful for both the students as well as working professionals who are preparing for GATE as it comes handy while traveling long distances.

When do I start using K-Notes?

It is highly recommended to use K-Notes in the last 2 months before GATE Exam (November end onwards).

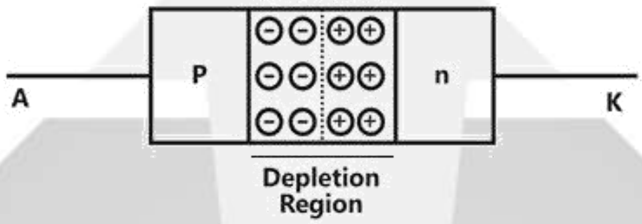
How do I use K-Notes?

Once you finish the entire K-Notes for a particular subject, you should practice the respective Subject Test / Mixed Question Bag containing questions from all the Chapters to make best use of it.

Diodes

Representation:

A: Anode K : Cathode



- The voltage at which the charged particles start crossing the junction is called as cut – in voltage or Threshold voltage.
  It is represented as $V_{AK} = V_{\gamma}$.

- When $V_{AK} < V_{\gamma}$, depletion region exists and no charge carriers cross the junction, therefore $I_D = 0$
- When $V_{AK} > V_{\gamma}$, number of charged particles crossing the junction increases & the current through the diode increase, non – linearly or exponentially.
- Diode in the condition is said to be forward biased.

$$I_D = I_S \left[e^{V_{AK}/\eta V_T} - 1 \right]$$

I_S = reverse saturation current

V_T = Thermal voltage = $\frac{KT}{q}$

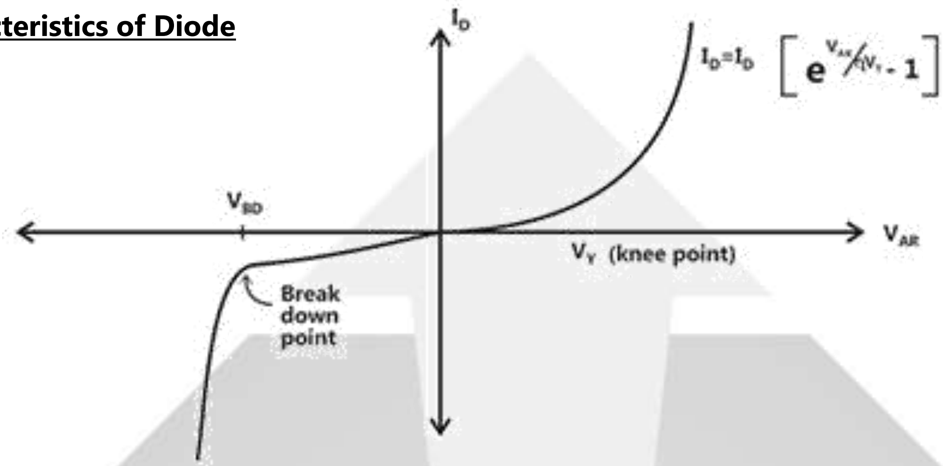
K = Boltzmann constant
T = Temp. in k
q = charge of one e^{-}

V_T = 26mv at room temperature

η = intrinsic factor

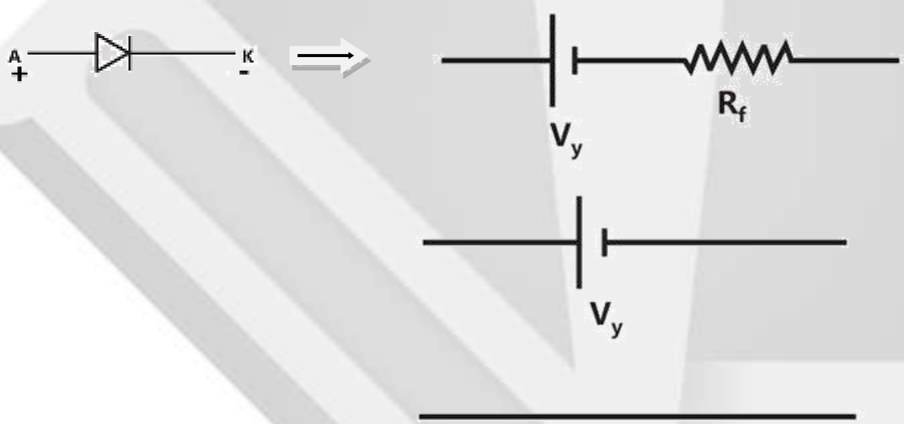
- When $V_{AK} < 0$, diode is said to be in reverse biased condition & no majority carriers cross the depletion region, hence $I_D = 0$

Characteristics of Diode



Equivalent circuit of diode

- Forward Bias



when V_γ & R_f given

when V_γ given

when both are not given

- Reverse Bias

open circuit

Diode Resistance

1) State or DC Resistance

$$R_{DC} = \frac{V_{AK}}{I_D}$$

2) Dynamic or AC Resistance

$$R_{AC} = \frac{dV_D}{dI_D} = \frac{\eta V_T}{I_D}$$

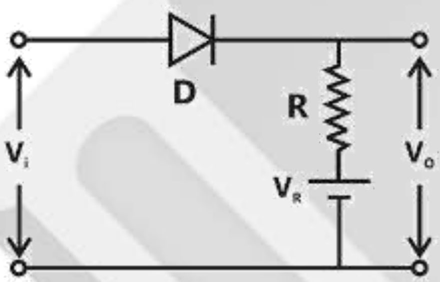
Diode Applications

Clippers

It is a transmission circuit which transmits a part of i/p voltage either above the reference voltage or below the reference voltage or b/w the two reference voltages.

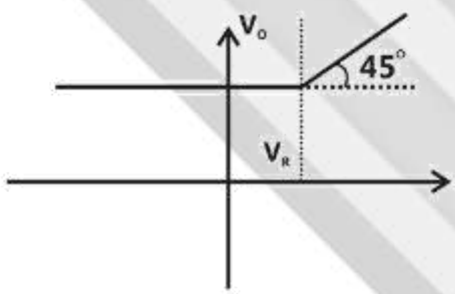
- **Series Clippers**

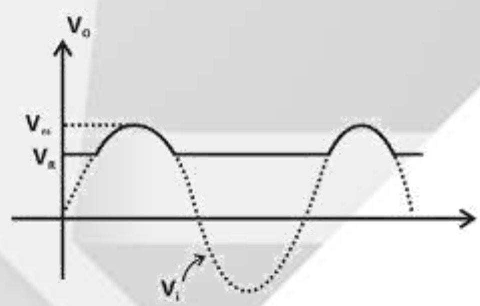
i) Positive Clippers



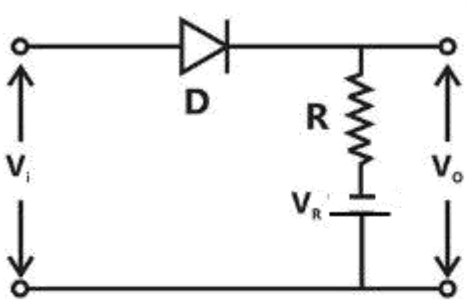
$V_i = V_m \sin\omega t$: When $V_i < V_R \Rightarrow V_O = V_R$

$V_m > V_R$ When $V_i > V_R \Rightarrow V_O = V_i$



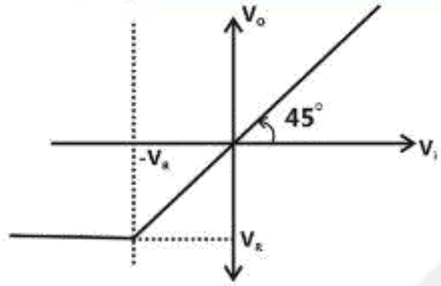


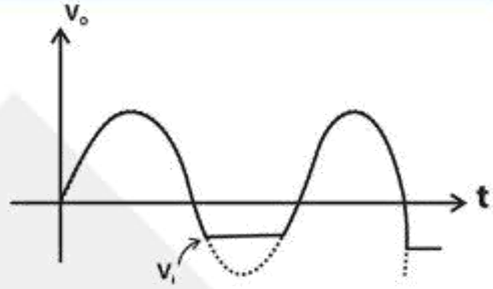
ii) Negative Clipper



$V_i = V_m \sin\omega t$: When $V_i < -V_R \Rightarrow V_o = -V_R$

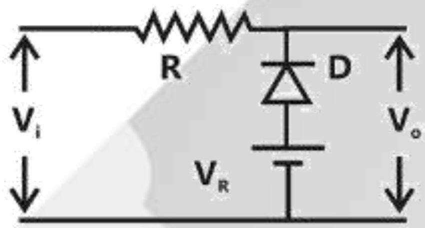
$V_m > -V_R$ When $V_i > -V_R \Rightarrow V_o = V_i$





- **Shunt Clipper**

i) Positive Clipper



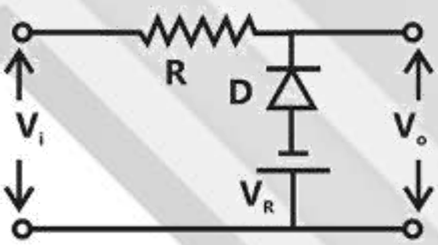
When $V_i < V_R$, D is ON

$V_o = V_R$

When $V_i > V_R$, D is OFF

$V_o = V_i$

ii) Negative Clipper



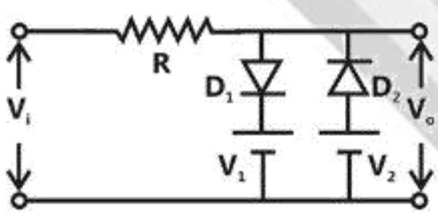
When $V_i < -V_R$, D is ON

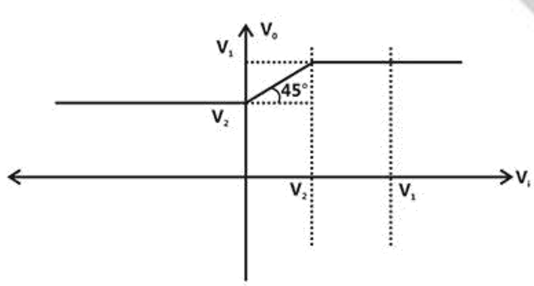
$V_o = -V_R$

When $V_i > -V_R$, D is OFF

$V_o = V_i$

- **Two level Clipper**





When $V_i < V_2$, D_1 is OFF & D_2 is ON

$V_0 = V_2$

When $V_i \geq V_2$ & $V_i < V_1$, D_2 is OFF & D_1 is OFF

$V_o = V_i$

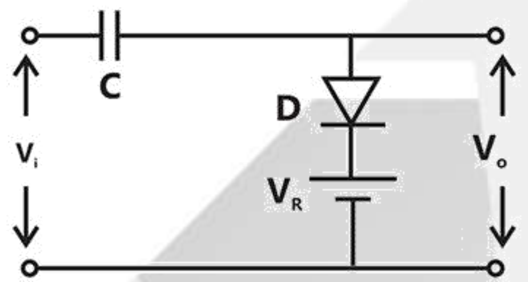
When $V_i > V_1$, D_2 is OFF D_I is ON

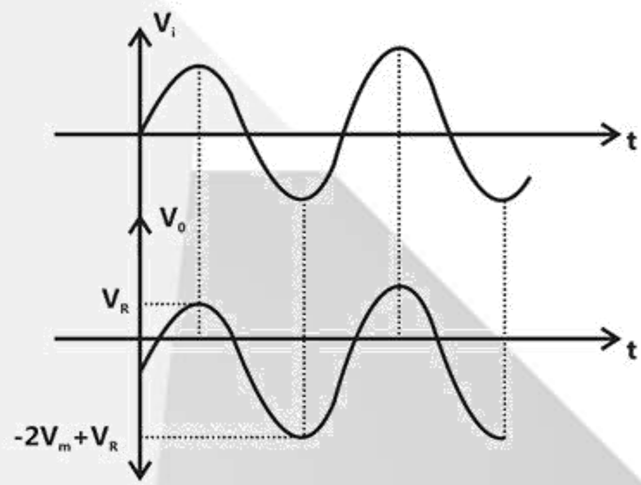
$V_o = V_1$

CLAMPERS

These circuits are used to shift the signal either up words or down words.

- **Negative Clampers**





When $V_R = 0$

+ve peak is shifted to 0

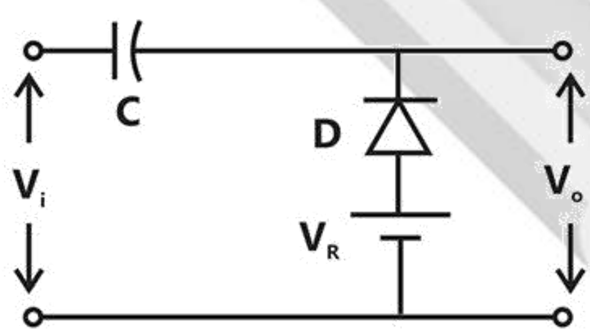
-ve peak is shifted to $-2V_m$

When $V_R \neq 0$

+ve peak is shifted to V_R

-ve peak is shifted to -2 $V_m + V_R$

- **Positive Clampers**



When $V_R = 0$

-ve peak is shifted to 0

+ve peak is shifted to $2V_m$

When $V_R \neq 0$

-Ve peak is shifted to V_R

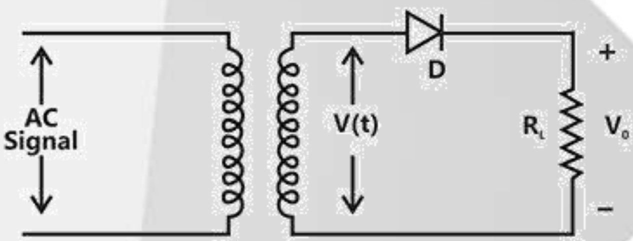
+ve peak is shifted to $2V_m + V_R$

Rectifier

It converts AC signal into pulsating DC.

1) **Half wave rectifier**

During positive half wave cycle



$$V_0 = V_m \sin\omega t\left[\frac{R_L}{R_f + R_L}\right]$$

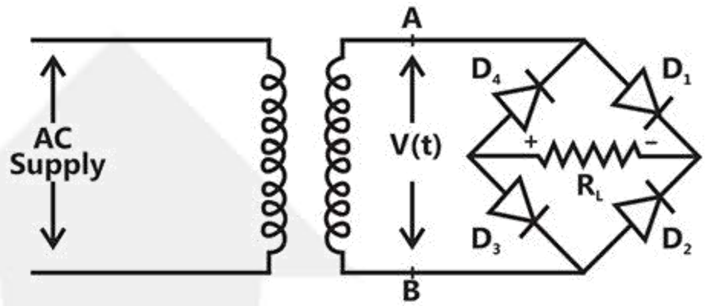
R_f = diode resistance

During negative half cycle

$V_0 = 0$

- $(V_0)_{avg} = \frac{V_m}{\pi}$
- $\eta = \frac{4}{\pi^2}\left(\frac{R_L}{R_f + R_L}\right) \times 100\%$
- $(V_0)_{RMS} = \frac{V_m}{2}$
- Form Factor = $\frac{V_{RMS}}{V_{avg}} = \pi/2$
- Ripple factor = $\sqrt{FF^2 - 1}$
- PIV = V_m

Bridge full wave rectifier



When +ve half wave cycle

$$V_o = V(t) \times \frac{R_L}{R_L + 2R_f}$$

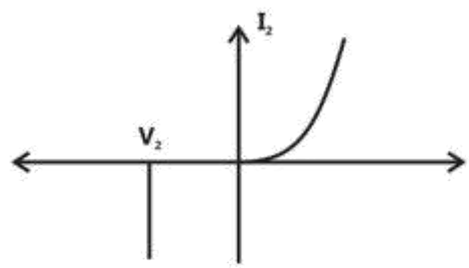
When –ve half wave cycle

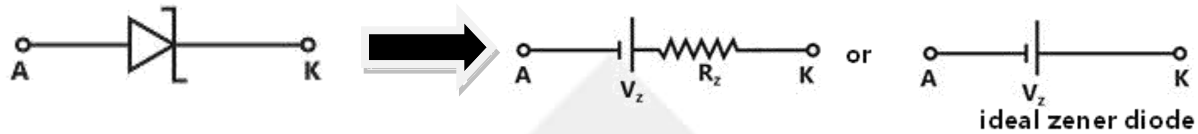
$$V_o = -V(t) \times \frac{R_L}{R_L + 2R_f}$$

- $(V_o)_{avg} = \frac{2V_m}{\pi}$
- $\eta = \frac{8}{\pi^2}\left(\frac{1}{1 + 2\frac{R_f}{R_L}}\right) \times 100\%$
- $(V_o)_{RMS} = \frac{V_m}{\sqrt{2}}$
- $FF = \frac{\pi}{2\sqrt{2}}$
- $PIV = V_m$

Zener Diode

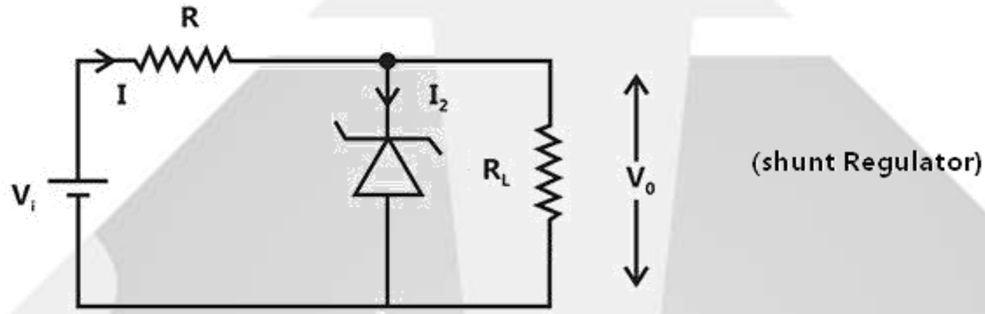
- A heavily doped a si diode which has sharp breakdown characteristics is called Zener Diode.
- When Zener Diode is forward biased, it acts as a normal PN junction diode.
- For an ideal zener diode, voltage across diode remains constant in breakdown region.
- If $I_{z(min)}$ is not given, then consider $I_{z(min)} = 0$





Voltage Regulator

Regulators maintains constant output voltage irrespective of input voltage variation.



Zener must operate in breakdown region so $\boxed{V_i > V_z}$

$$I = I_z + I_L$$

$$I_L = \frac{V_z}{R_L}$$

$$\therefore I_{max} = I_{z(max)} + I_L$$

$$I_{min} = I_{z(min)} + I_L$$

$$\therefore I_{z(max)} = I_{(max)} - I_L$$

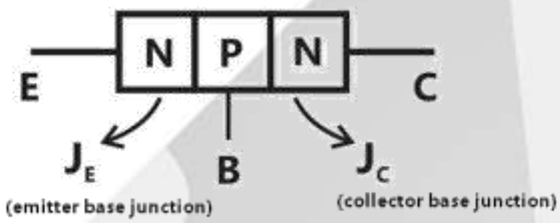
$$I_{z(min)} = I_{min} - I_L$$

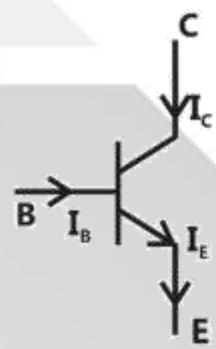
Transistor Biasing

Bipolar Junction Transistor

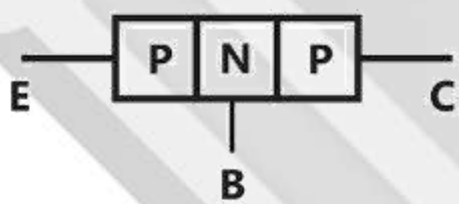
- Current conduction due to both e- & holes
- It is a current controlled current source.

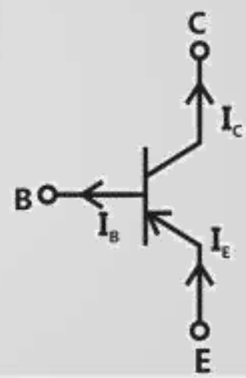
NPN Transistor





PNP Transistor





Region of Operation

	Junctions	Region of operations	Applications
i)	$J_E = RB$ $J_C = RB$	cut – off	Switch
ii)	$J_E = FB$ $J_C = RB$	active	amplifier
iii)	$J_E = FB$ $J_C = FB$	saturation	Switch
iv)	$J_E = RB$ $J_C = FB$	reverse active	Attenuation

Current gain (α) (common base)

$I_C = I_{nc} + I_o$

I_{nc} : injected majority carrier current in collector

$\alpha = \frac{I_{nc}}{I_E}$

$I_C = \frac{\alpha I_B + I_o}{(1-\alpha)}$; $I_E = \frac{I_B}{(1-\alpha)} + \frac{1}{(1-\alpha)} I_o$

Current gain β (common emitter)

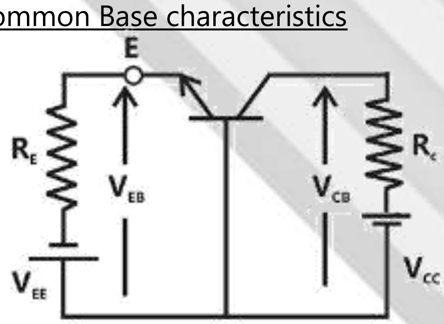
$I_c = \beta I_B + (1+\beta) I_o$

$\alpha = \frac{\beta}{1+\beta}$; $\beta = \frac{\alpha}{(1-\alpha)}$

- These relations are valid for active region of operations.

Characteristics of BJT

- Common Base characteristics

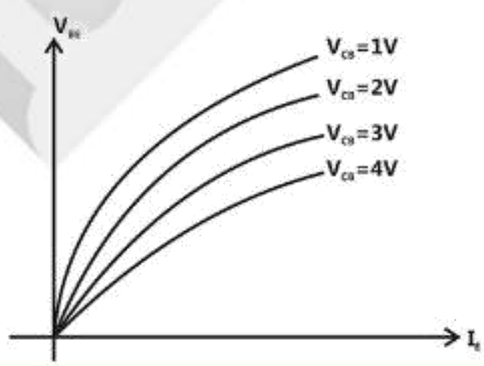


input = V_{BE}, I_E

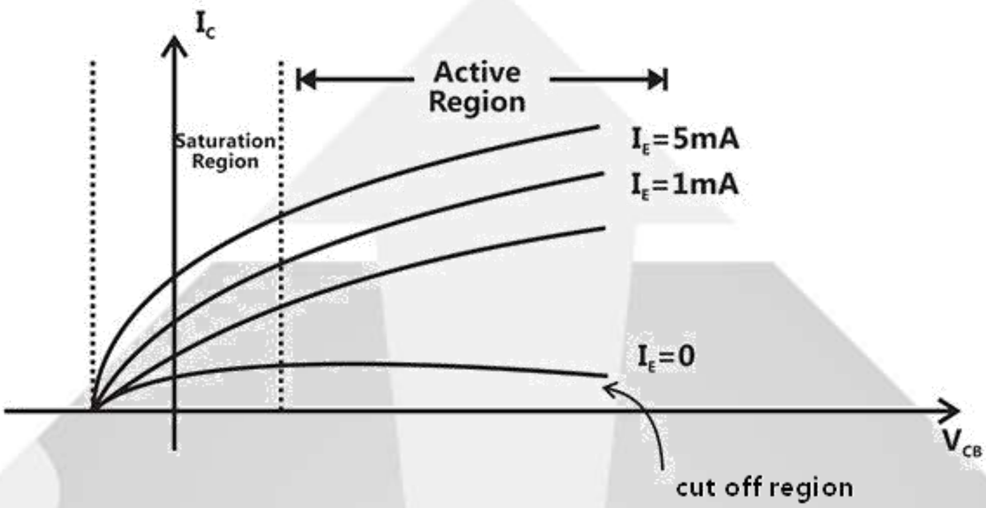
output = V_{CB}, I_C

Input characteristics

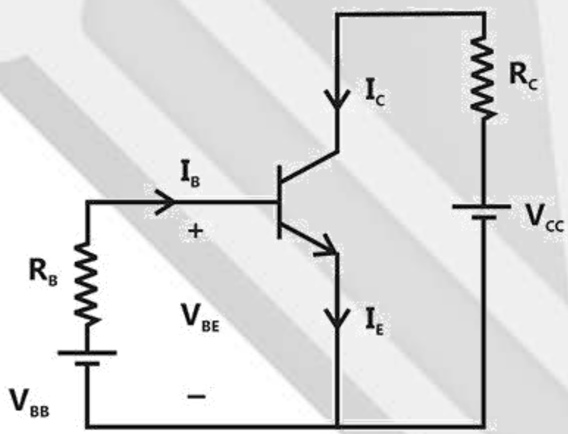
V_{BE} vs I_E when V_{CB} = constant



Output characteristics



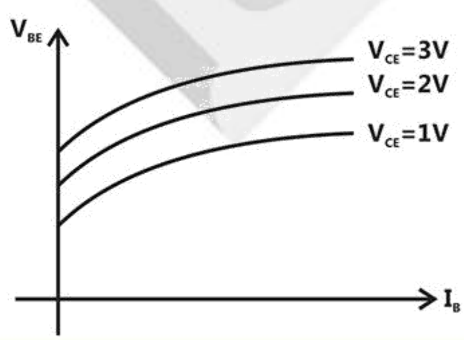
- Common emitter characteristics



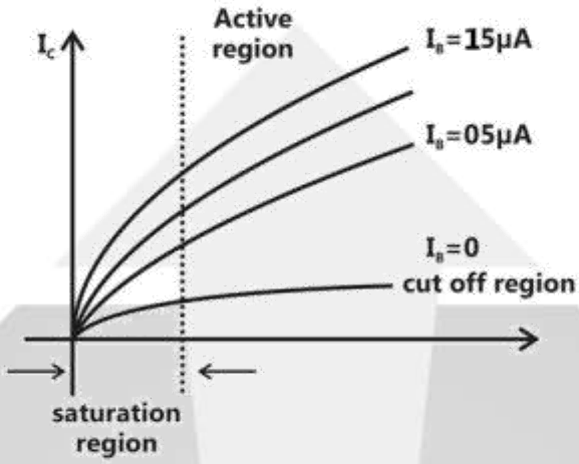
inputs$\left(V_{BE}, I_B\right)$

outputs$\left(V_{CE}, I_C\right)$

Input characteristics

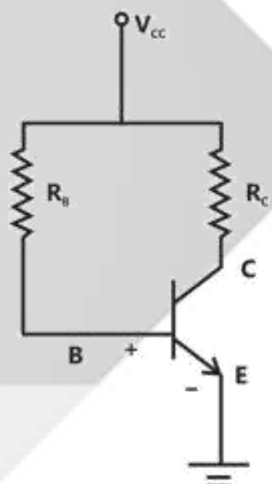


<u>Output characteristics</u>



<u>Transistor Biasing</u>

1) **<u>Fixed Bias method</u>**



$$V_{cc} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

Assuming active region of operation

$$I_c = \beta I_B$$

$$V_{CE} = V_{CC} - I_C R_C$$

<u>Verification</u>

- If $V_{CE(sat)} < V_{CE} < V_{CC} \rightarrow \text{Active Region}$

  If not ; then saturation region

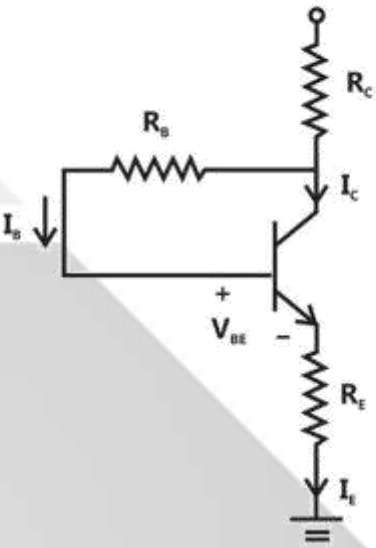
- For saturation region , $V_{CE} = V_{CE(sat)}$

$$I_C = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

- In saturation region , $I_B \geq \frac{I_C}{\beta_{min}}$

2) Feedback Resistor Bias Method

By KVL



$$V_{CC} - \left(I_C + I_B\right)R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - \left(I_C + I_B\right)R_C - I_B R_B - V_{BE} - \left(I_C + I_B\right)R_B = 0$$

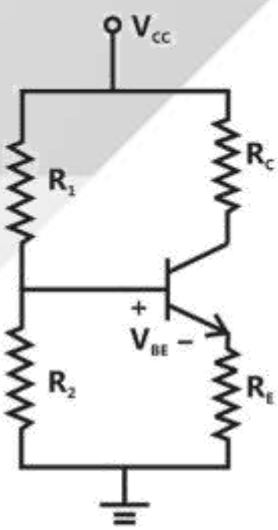
Assuming active region

$$I_C = \beta I_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)\left(R_C + R_E\right)} \quad ; \quad I_C = \beta I_B$$

$$V_{CE} = V_{CC} - \left(I_C + I_B\right)\left(R_C + R_E\right)$$

3) Voltage divider bias or self-bias



By thevenin's theorem across R_2

$$V_{TH} = V_{CC}\frac{R_2}{R_1 + R_2}$$

$$R_{TH} = \frac{R_2 R_1}{R_1 + R_2}$$

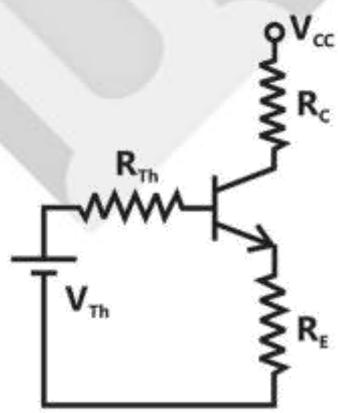
Apply KVL

$$V_{TH} - V_{BE} = I_B R_{TH} + \left(I_B + I_C\right)R_E$$

Assuming active region $I_C = \beta I_B$

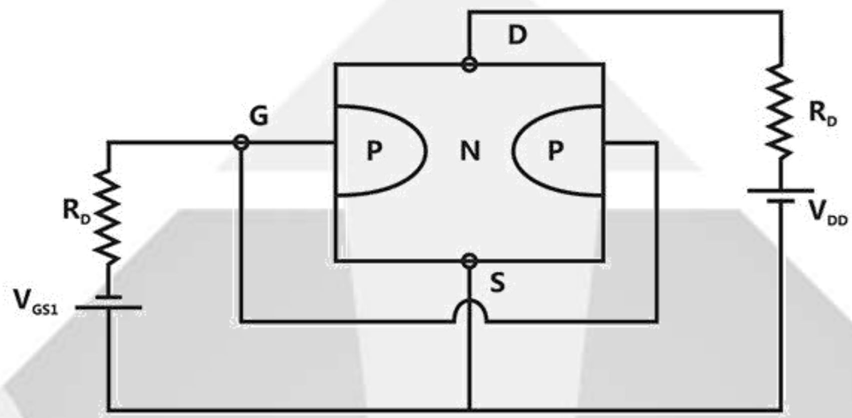
$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta)R_E}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$



FET Biasing

JFET



- When V_{GS} is negative, depletion layer is created between two P – region and that pinches the channel between drain & source.
- The voltage at which drain current is reduce to zero is called as pinch off voltage.
- Transfer – characteristics of JFET is inverted parabola

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(OFF)}}\right]^2$$

When $V_{GS} = 0,\ I_D = I_{DSS}$

When $V_{GS} = V_{GS(OFF)},\ I_D = 0$

Pinch of voltage, $V_p = \left|V_{GS(OFF)}\right|$

- For a N – channel JFET, pinch off voltage is always positive

$V_p > 0\ \&\ V_{GS} < 0$

JFET Parameters

1) **Drain Resistance**

$$r_d = \frac{\Delta V_{DS}}{\Delta I_{DS}}$$

It is very high, of the order of $M\Omega$.

2) **Trans conductance**

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{dI_D}{dV_{GS}}$$

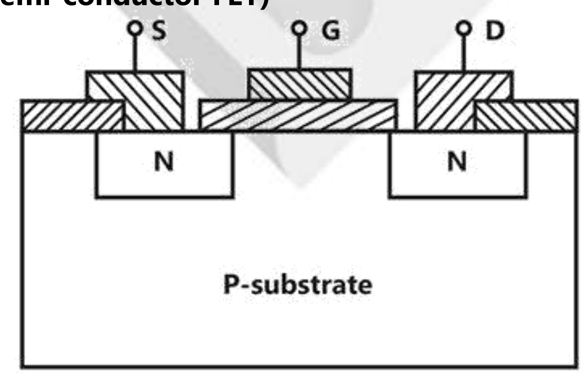
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(OFF)}}\right]^2$$

$$\frac{dI_D}{dV_{GS}} = g_m = \frac{-2I_{DSS}}{V_{GS(OFF)}}\left[1 - \frac{V_{GS}}{V_{GS(OFF)}}\right]$$

3) **Amplification factor**

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = g_m r_d$$

MOSFET (Metal Oxide Semi-conductor FET)



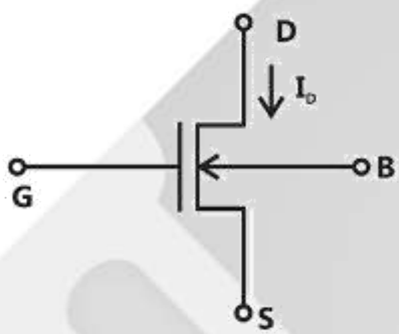
Enhancement Type MOSFET

- No physical channel between source & drain
- To induce a channel Gate – source voltage is applied.

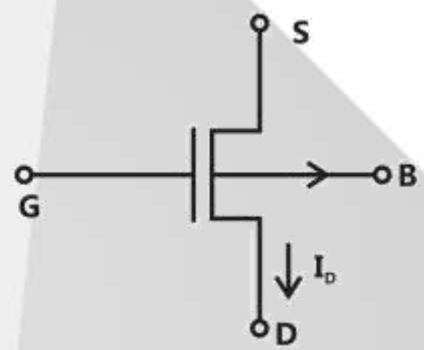
Depletion MOSFET

- Physical channel present between source & drain.

Types of MOSFET



n-channel MOSFET



P-channel MOSFET

Operating characteristics

1. **For n – channel MOSFET**

- $I_D = 0 \quad \text{for } V_{GS} < V_T$ (cut – off region)
- $I_D = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$ (linear region)

  $V_{GS} \geq V_T$ and $V_{DS} < \left(V_{GS} - V_T\right)$
- $I_D = \mu_n C_{ox} \frac{W}{L}\frac{\left(V_{GS} - V_T\right)^2}{2}$ (saturation region)

  $V_{GS} \geq V_T$ and $V_{DS} \geq \left(V_{GS} - V_T\right)$

2. For p – channel MOSFET

- $I_D = 0 \text{ for } V_{GS} > V_T$ (cut – off region)
- $I_D = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$ (linear region)

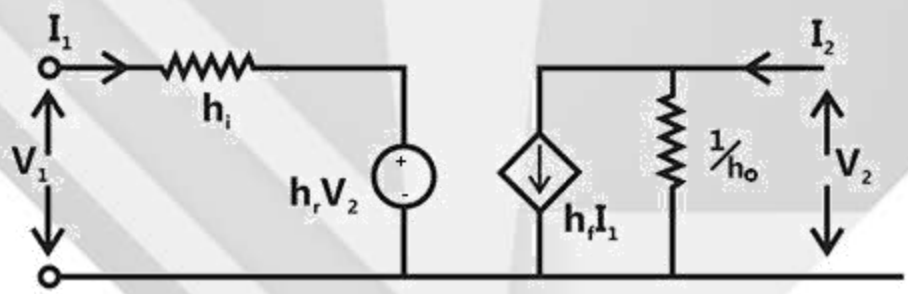
  $V_{GS} \le V_T$ and $V_{DS} > V_{GS} - V_T$
- $I_D = \mu_n C_{ox} \frac{W}{L}\frac{\left(V_{GS} - V_T\right)^2}{2}$ (saturation region)

  $V_{GS} \le V_T$ and $V_{DS} \le V_{GS} - V_T$

Transistor Amplifier

Small signal analysis for BJT

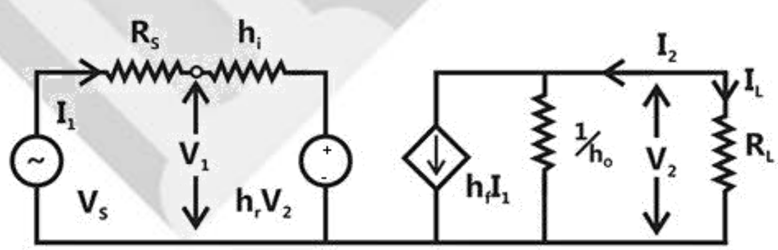
- h – parameter model of BJT



$V_1 = h_i I_1 + h_r V_2$

$I_2 = h_f I_1 + h_o V_2$

- current gain, $A_I = -\frac{I_2}{I_1}$

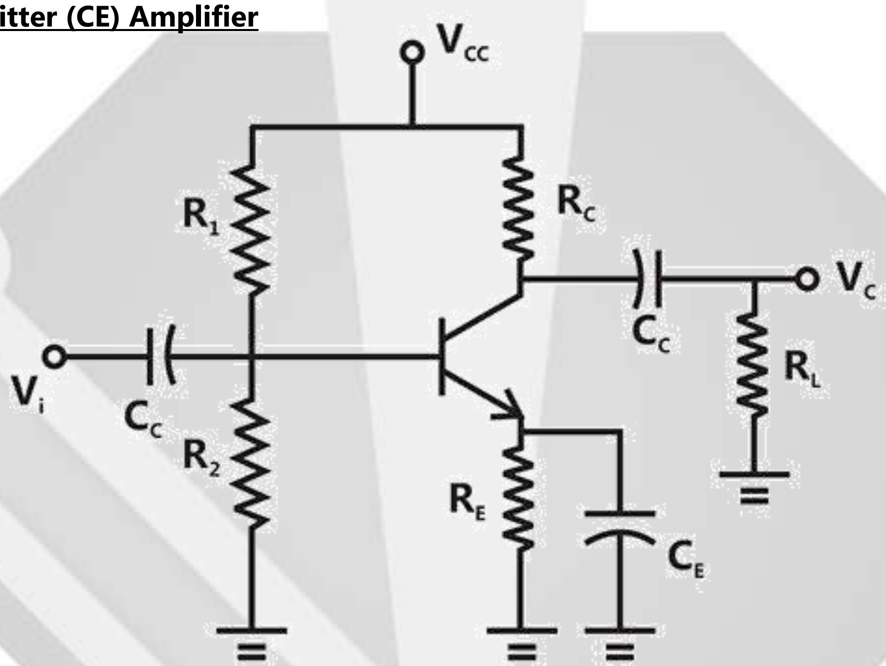


$$A_I = \frac{-h_f R_L}{1 + h_o R_L}$$

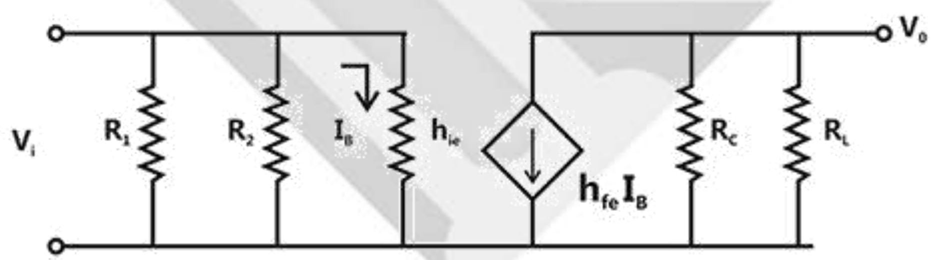
- Input Impedance, $Z_i = \frac{V_1}{I_I} = h_i + h_r A_I R_L$

- Voltage gain, $A_V = \frac{A_I R_L}{Z_i}$
- Output impedance, $Z_o = \frac{1}{\left(h_o - \frac{h_f h_r}{h_i + R_s}\right)}$

Common Emitter (CE) Amplifier

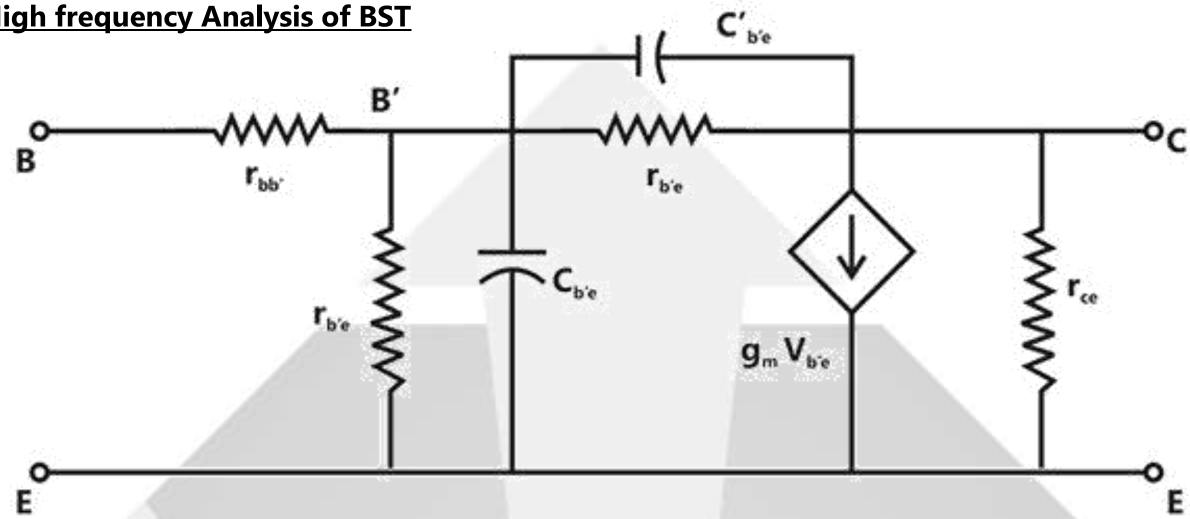


Small signal model



Voltage gain $A_V = \frac{V_o}{V_i} = \frac{-h_f e}{h_i e}\left(R_C \parallel R_L\right)$

High frequency Analysis of BST



$r_{bb'}$ = base spreading resistance.

$r_{b'e}$ = input resistance.

$r_{b'c}$ = feedback resistance.

r_{ce} = output resistance.

$C_{b'e}$ = diffraction capacitance.

$C_{b'c}$ = Transition capacitance.

g_m = Transconductance.

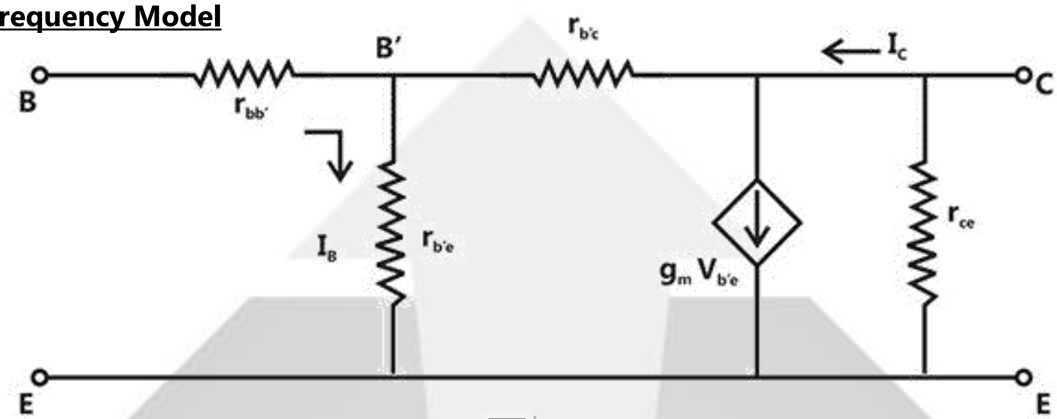
Hybrid π - parameters

1) $g_m = \frac{(I_c)_Q}{V_T}$; $V_T = \frac{KT}{q}$,

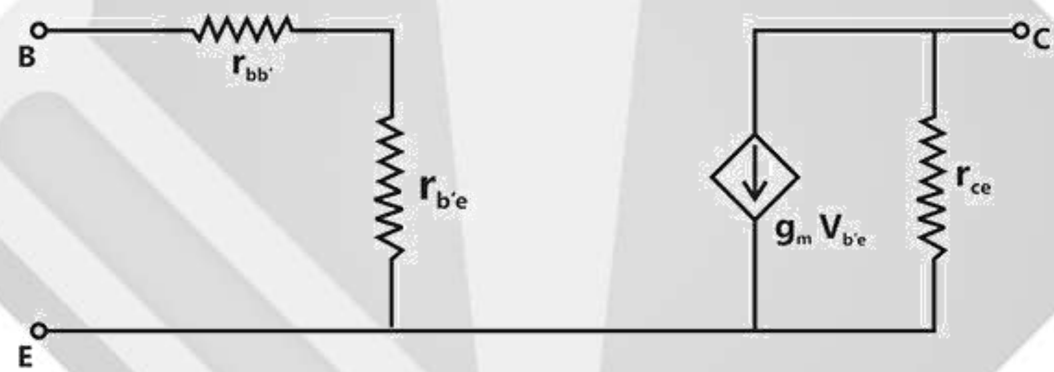
I_{CQ} = dc bias point collector current.

2) $r_{b'e} = \frac{h_{fe}}{g_m}$

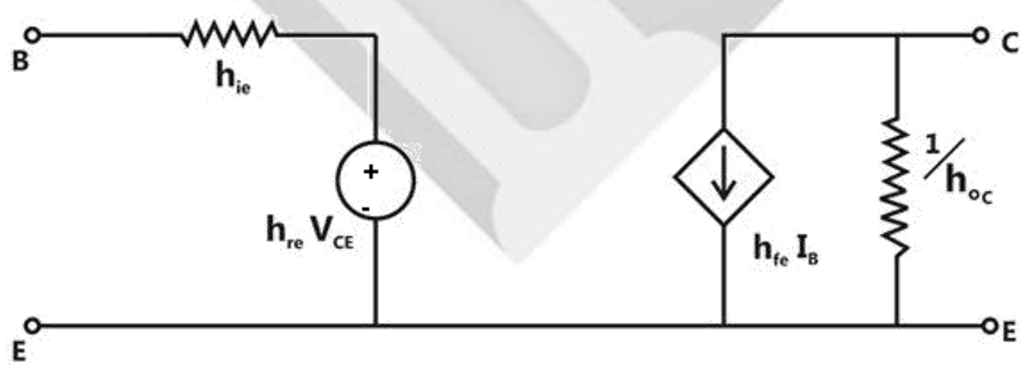
High Frequency Model



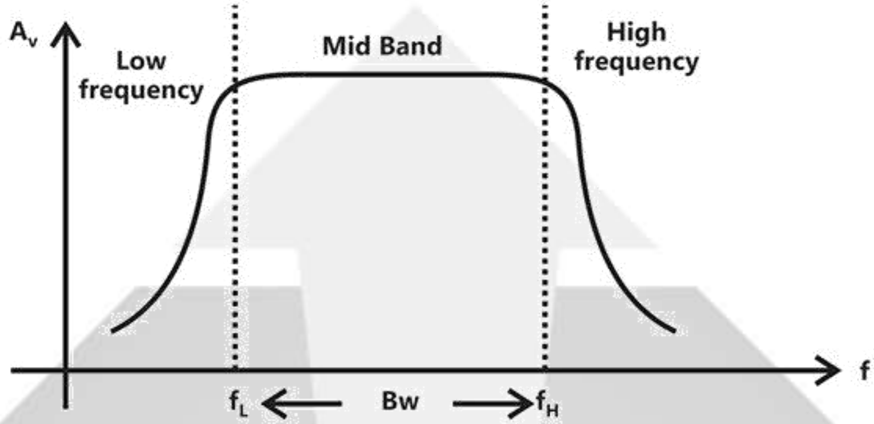
$r_{b'c}$ = open circuited.

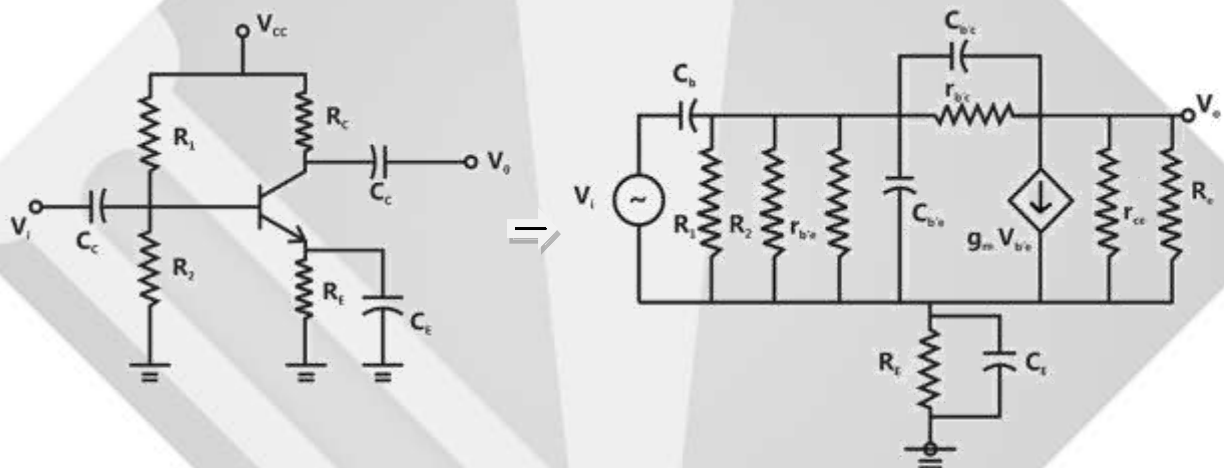


Low Frequency Model



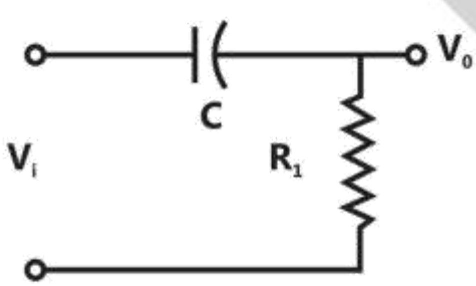
Voltage gain as frequency





Low Frequency Range

- External capacitor C_E and C_C are short circuited.
- Internal capacitor $C_{b'c}$ and $C_{b'e}$ are open circuited.
- Circuit becomes like.



= acts as high pass filter.

High frequency range

- External capacitors C_b, C_c and C_E are short circuited.
- $C_{b'c}$ is open circuited.
- Equivalent circuit behaves as a low pass filter with cut-off frequency f_L.

Mid – band range

- All internal and external capacitance are neglected, so gain is independent of frequency.

FET Small Signal parameters

Trans conductance, $g_m = \dfrac{\partial I_D}{\partial V_{GS}}$

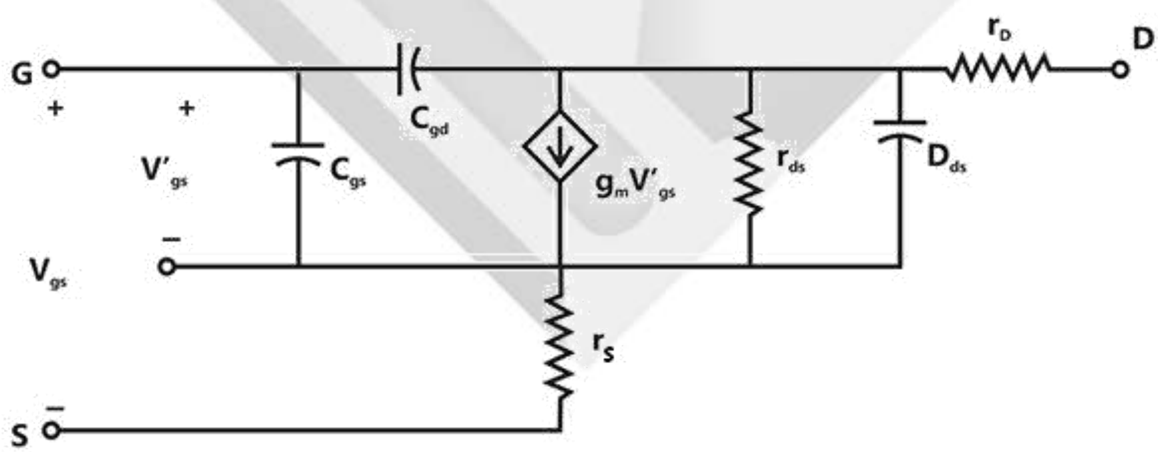
In non – saturation region

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} . V_{DS}$$

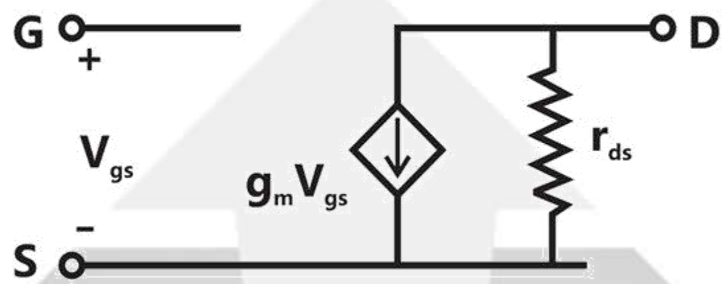
In saturation region

$$g_{ms} = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_T\right)$$

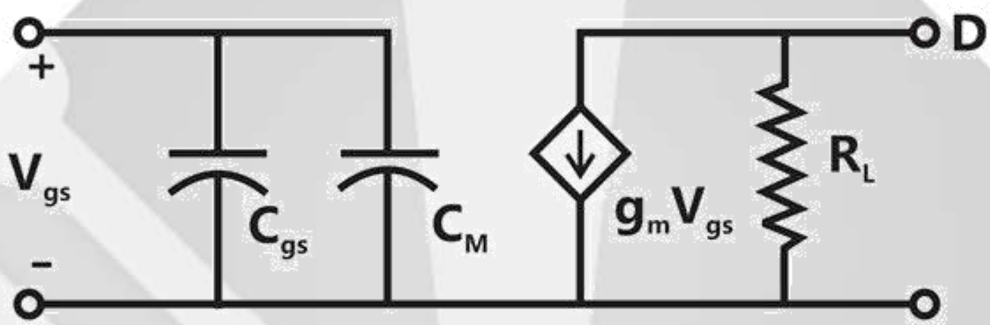
Small Signal equivalent circuit



For low frequency



For high frequency



Feedback Amplifiers

Ideal Amplifier

$Z_{in} = \infty$

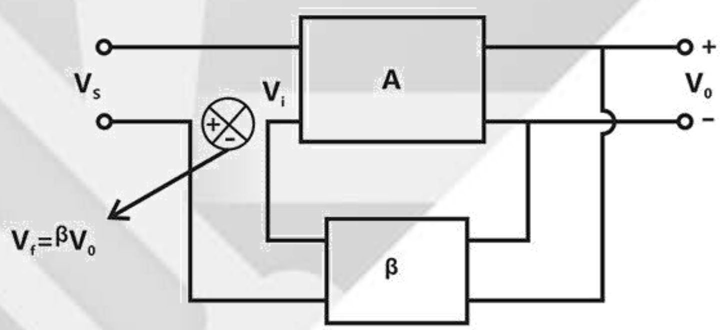
$Z_o = 0$

Positive feedback : $V_i = V_s + V_f$

Negative Feedback : $V_i = V_s - V_f$

For negative feedback, $\frac{V_o}{V_s} = \frac{A}{1 + A\beta}$

For positive feedback, $\frac{V_o}{V_s} = \frac{A}{1 - A\beta}$



- Positive feedback is used for unstable system like oscillators.

Effects of Negative Feedback

i) Sensitivity

Without feedback = $\frac{\delta A}{A}$

With feedback = $\frac{\delta A_f}{A_f}$

$$\boxed{\frac{\delta A_f}{A_f} = \frac{1}{(1 + A\beta)} \frac{\delta A}{A}}$$

ii) Input Impedance

Without feedback = Z_i

With feedback = Z_{if}

$Z_{if} = Z_i (1 + A\beta)$

iii) Output impedance

Without feedback = Z_o

With feedback = Z_{of}

$Z_{of} = Z_o / (1 + A\beta)$

- Negative feedback also leads to increase in band width

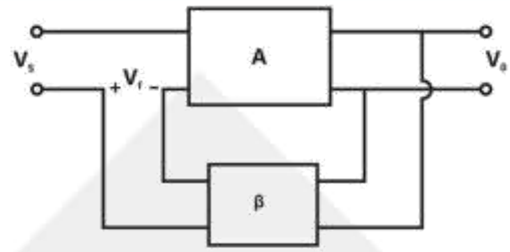
.

Topologies of Negative feedback

Output	Input
Voltage	Series
Voltage	Shunt
Current	Series
Current	Shunt

1) **Voltage Series Topologies**

$V_f = \beta V_o$

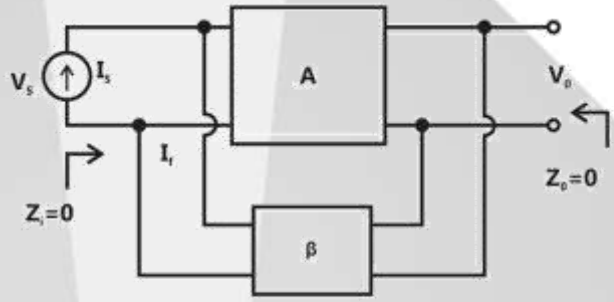


It is called as series shunt feedback or voltage - voltage feedback.

In this case, input impedance increases & output impedance decreases.

2) **Voltage shunt topologies**

$I_f = \beta V_o$



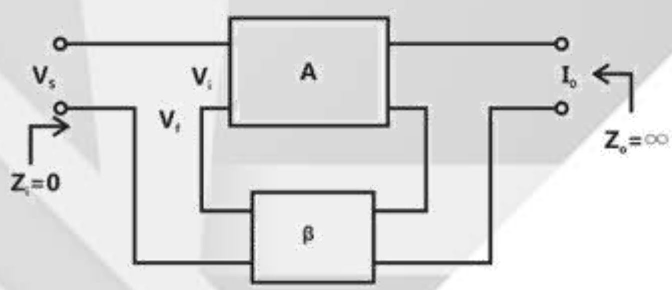
β = Trans conductance

It is called as shunt-shunt or voltage current feedback.

3) **Current series Topologies**

$V_f = \beta I_o$

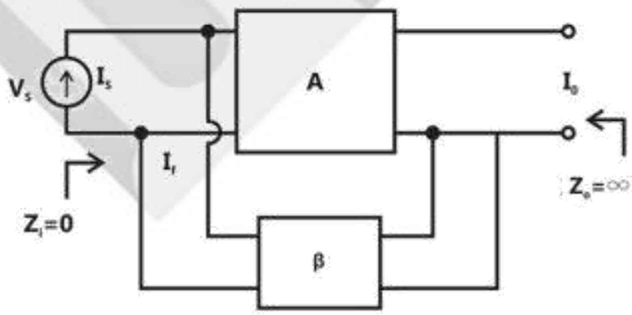
β = resistance



It is called as shunt – shunt or voltage current feedback.

4) **Current shunt Topologies**

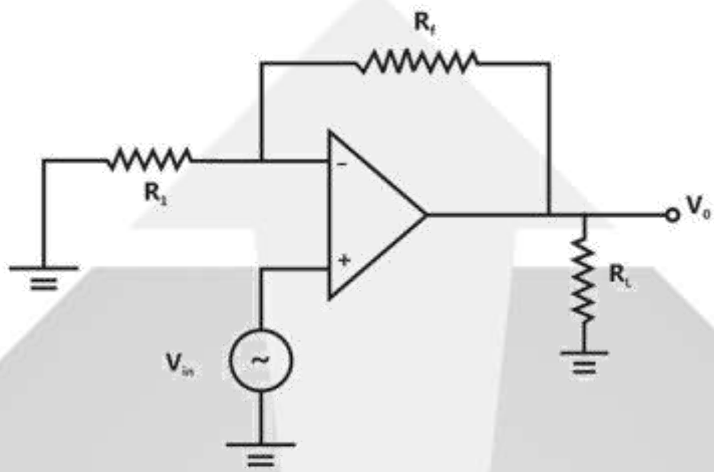
$I_f = \beta I_o$



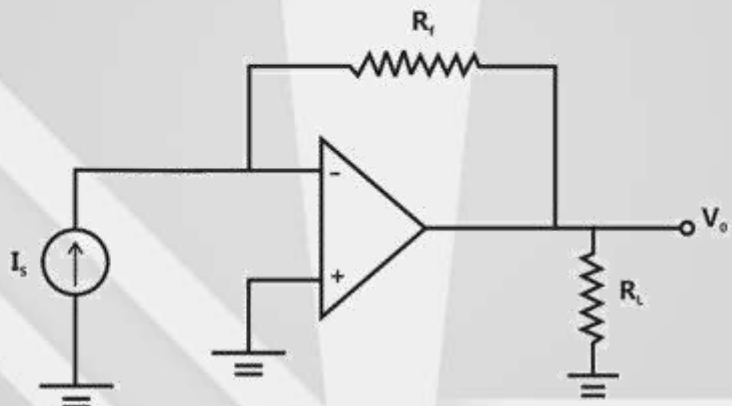
It is also called as shunt – series or current – current feedback.

Circuit Topologies

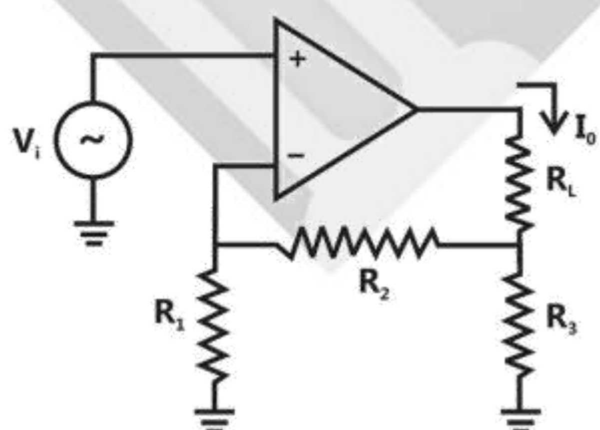
1) Voltage series



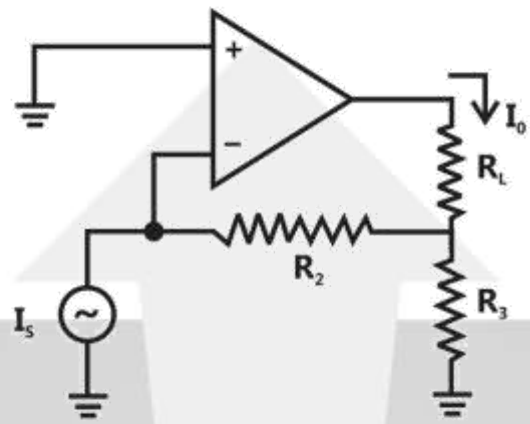
2) Voltage shunt



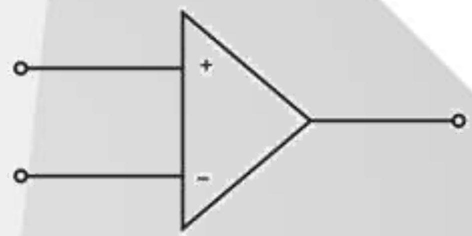
3) Current – series



4) Current – shunt



Operational Amplifiers (OP-AMP)



+ → Non – inverting terminal

- → inverting terminal

Parameters of OP–AMP

1) Input offset voltage

Voltage applied between input terminals of OP – AMP to null or zero the output.

2) Input offset current

Difference between current into inverting and non – inverting terminals of OP – AMP.

3) Input Bias Current

Average of current entering the input terminals of OP – AMP.

4) Common mode Rejection Ratio (CMRR)

Defined as ratio of differential voltage gain A_d to common mode gain (A_{cm}).

$$CMRR = \frac{A_d}{A_{cm}}$$

5) Slew Rate

Maximum rate of change of output voltage per unit time under large signal conditions.

$$SR = \left.\frac{dV_o}{dt}\right|_{max} \quad V/\mu s$$

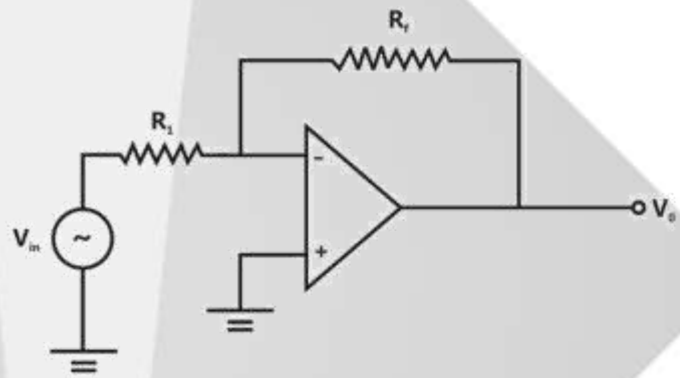
Concept of Virtual ground

In an OP – AMP with negative feedback, the potential at non – inserting terminals is same as the potential at inverting terminal.

Applications of OP –AMP

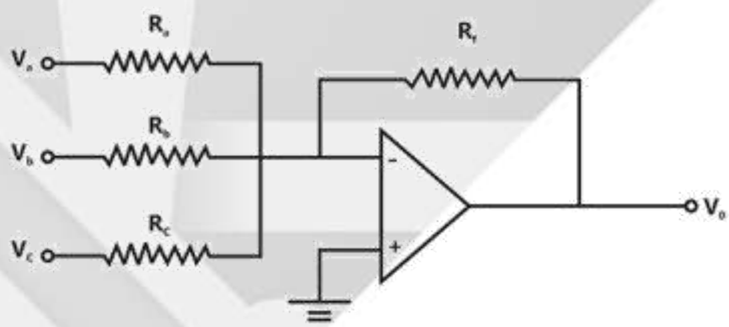
1) Inverting Amplifier

$$V_o = \frac{-R_f}{R_1} V_{in}$$



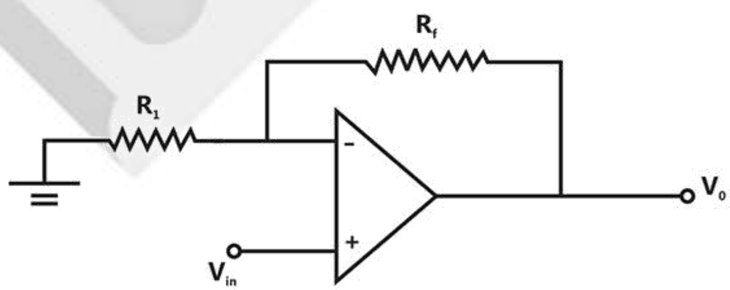
2) Inverting Summer

$$V_o = -R_f\left(\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c}\right)$$



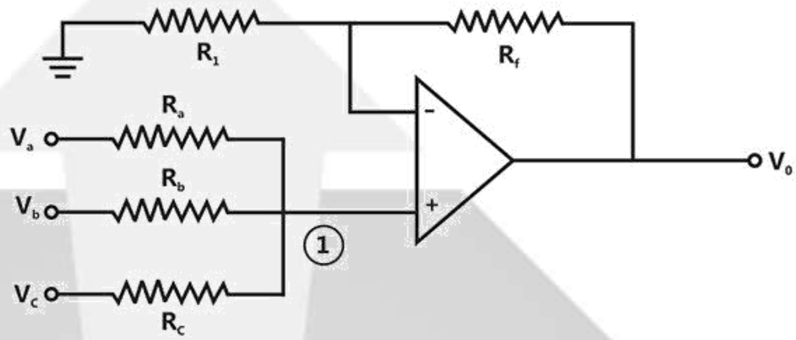
3) Non – inverting Amplifier

$$V_o = \left(1 + \frac{R_f}{R_1} V_{in}\right)$$



4) <u>Non – inverting summer</u>

If $R_a = R_b = R_c = R$



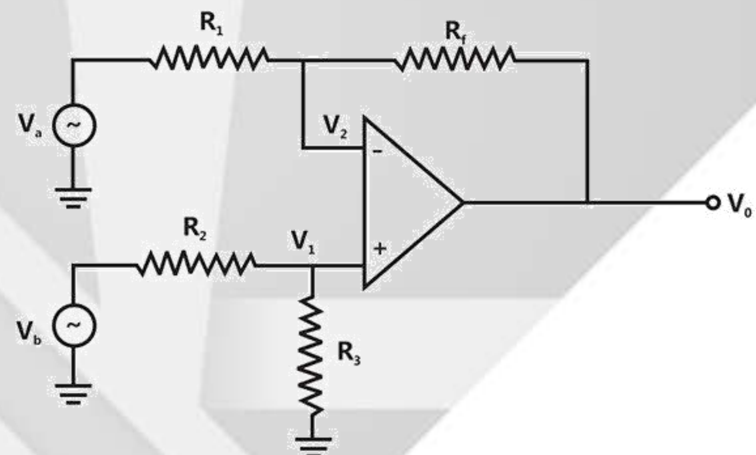
$$V_1 = \frac{V_a\left(R/2\right)}{R + R/2} + \frac{V_b\left(R/2\right)}{R + R/2} + \frac{V_c\left(R/2\right)}{R + R/2}$$

$$V_1 = \frac{\left(V_a + V_b + V_c\right)}{3}$$

$$V_o = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{V_a + V_b + V_c}{3}\right)$$

5) <u>Differential Amplifier</u>

By Super position

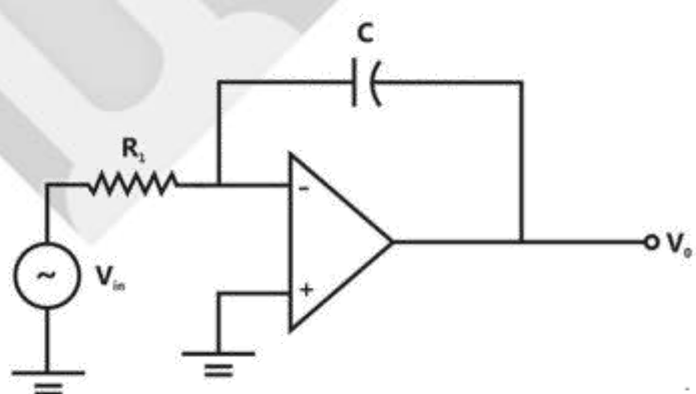


$$V_{ob} = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{R_3}{R_2 + R_3}\right)V_b$$

$$V_{oa} = \frac{-R_f}{R_1}V_a$$

$$V_o = V_{oa} + V_{ob}$$

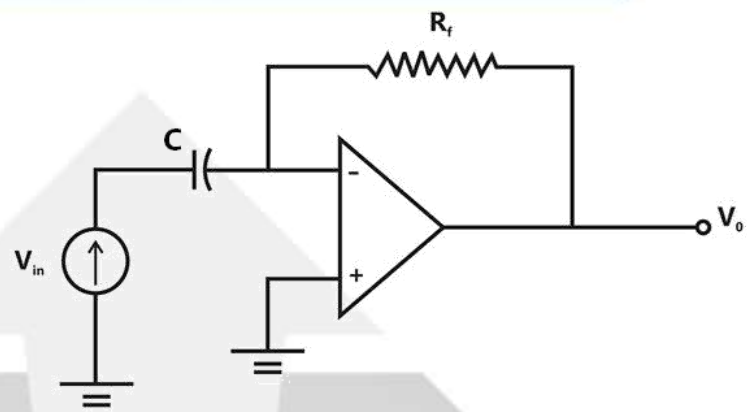
6) <u>Integrator</u>



$$V_o = \frac{-1}{RC}\int_o^t V_{in} dc$$

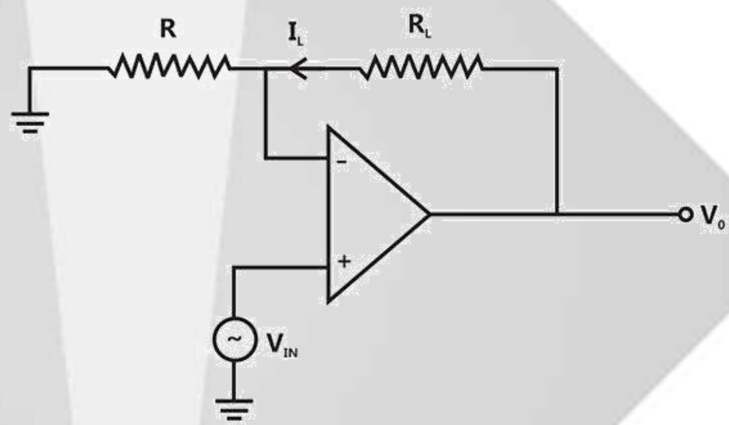
7) <u>Differentiator</u>

$$V_o = -RC\frac{dV_{in}}{dt}$$



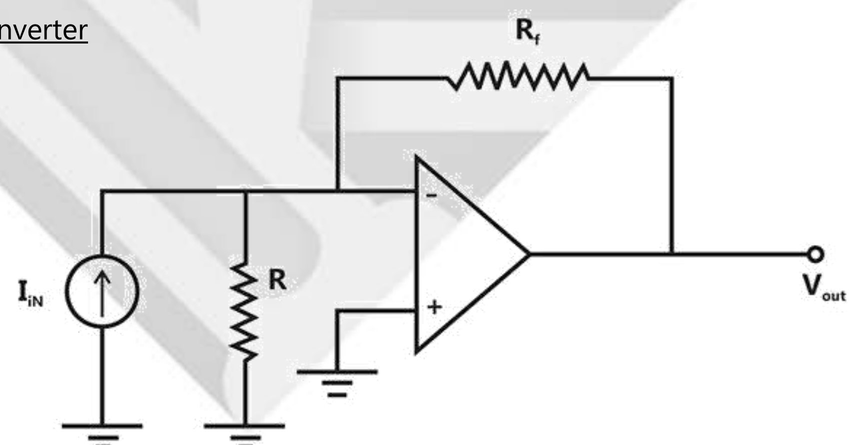
8) <u>Voltage to current converter</u>

$$I_L = \frac{V_{in}}{R}$$

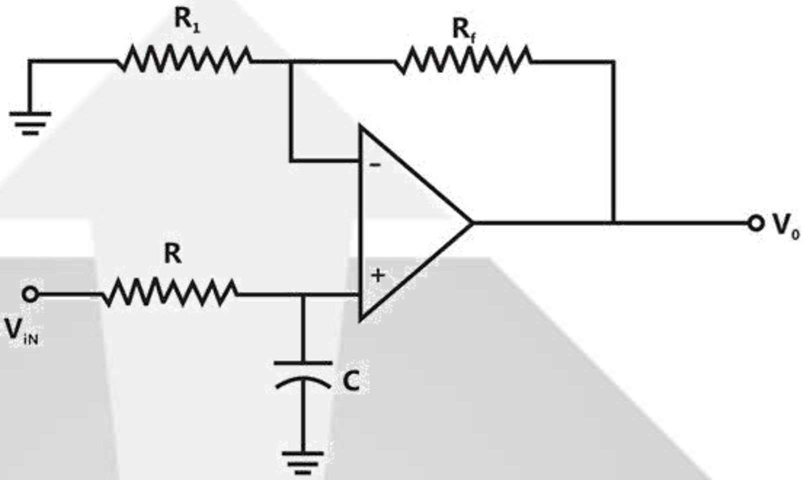


9) <u>Current to voltage Converter</u>

$$V_{out} = -R_p I_{IN}$$



10) Butter – worth Low Pass Filter

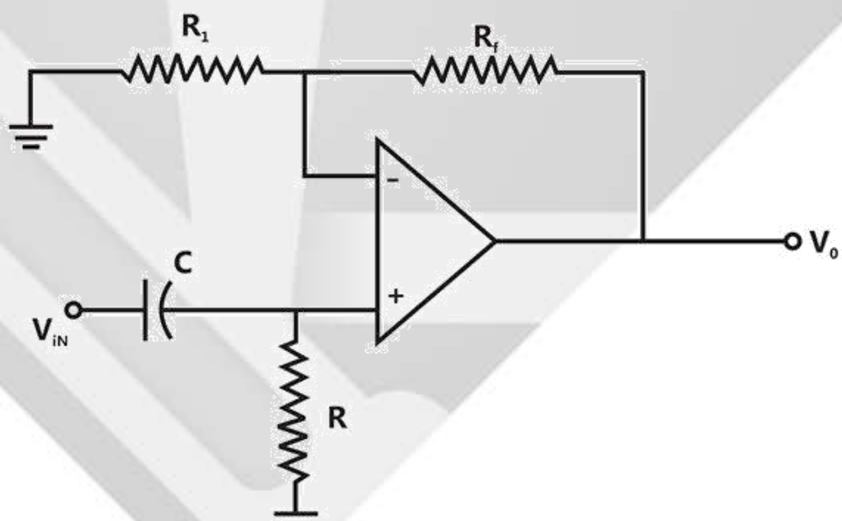


$$V_o = \left(1+\frac{R_f}{R_1}\right)\frac{V_{in}}{(1+j2\pi fRC)}$$

$$\frac{V_o}{V_{in}} = \frac{A_f}{1+j\left(\frac{f}{f_H}\right)}$$

$$A_f = \left(1+\frac{R_f}{R_1}\right) \; ; \; f_H = \frac{1}{2\pi RC}$$

11) Butter – worth High Pass Filter



$$\frac{V_o}{V_{in}} = \left(1+\frac{R_f}{R_1}\right)\left(\frac{j2\pi fRc}{1+j2\pi fRC}\right)$$

$$= A_f\left[\frac{j\left(\frac{f}{f_L}\right)}{1+j\left(\frac{f}{f_L}\right)}\right]$$

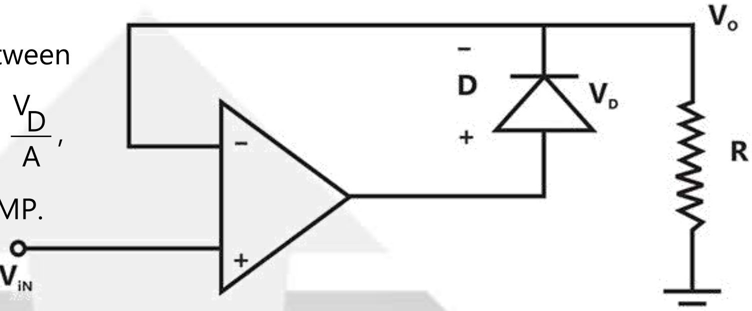
$$A_f = 1+\frac{R_f}{R_1}$$

$$f_L = \frac{1}{2\pi RC}$$

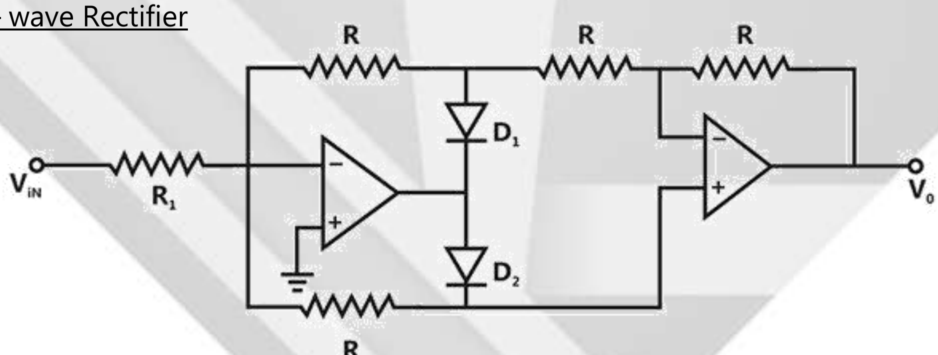
12) Active Half – wave rectifier

In this circuit, diode voltage drop between input & output is not V_D but rather $\frac{V_D}{A}$, where A = open loop gain of OP – AMP.

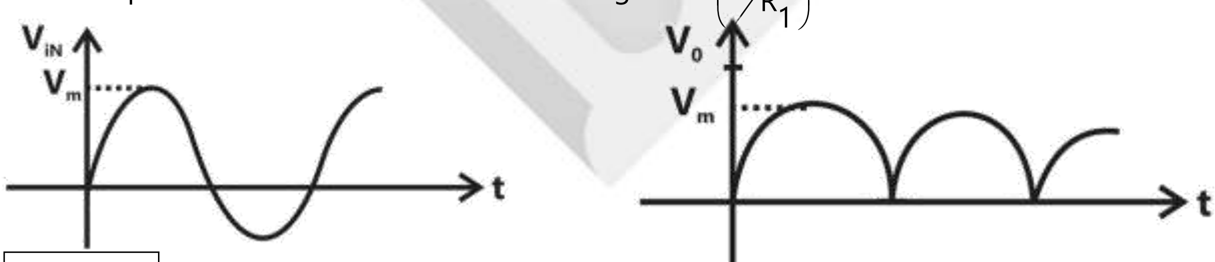
$\therefore V_{in} \approx V_o$



13) Active Full – wave Rectifier

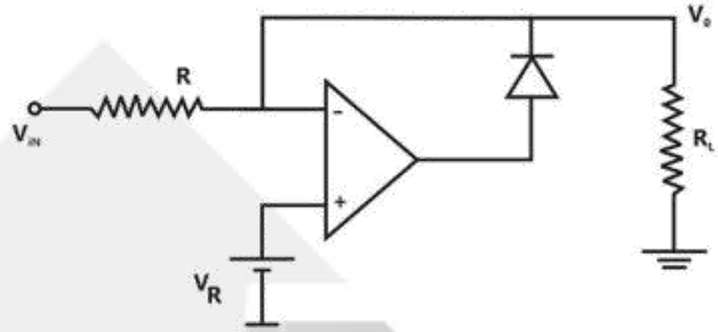


This circuit provides full wave rectification with a gain of $\left(\frac{R}{R_1}\right)$



$$\boxed{V'_m = \frac{R}{R_1} V_m}$$

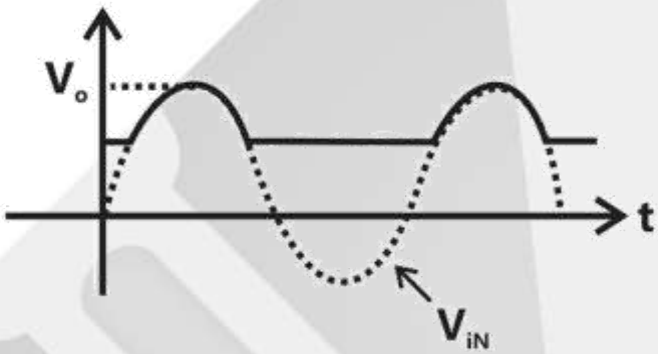
14) <u>Active Clipper</u>



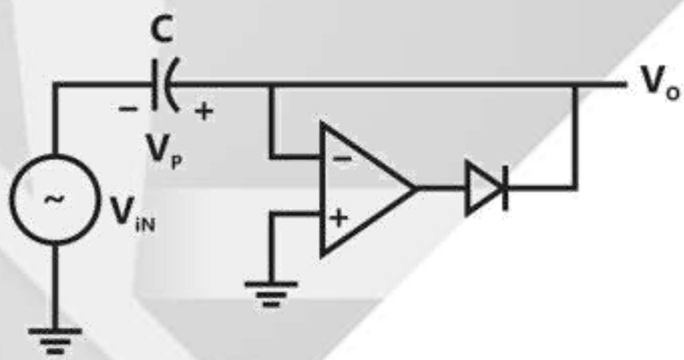
$V_{IN} < V_R$, Diode conducts and $V_o = V$

And when $V_{IN} > V_R$ Diode is OFF

$\therefore V_o = V_{IN}$

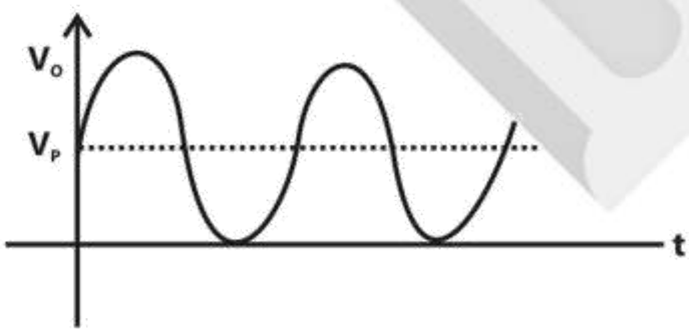


15) <u>Active Clamper</u>

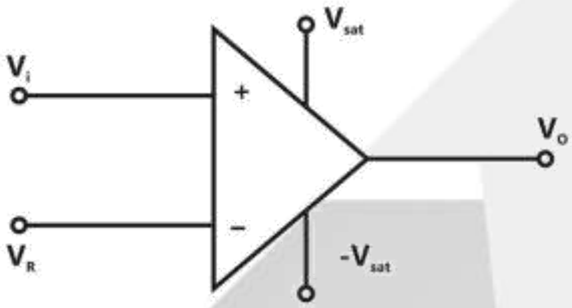


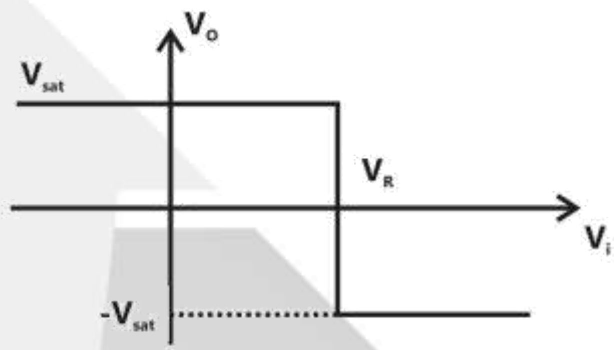
$V_o = V_{IN} + V_p$

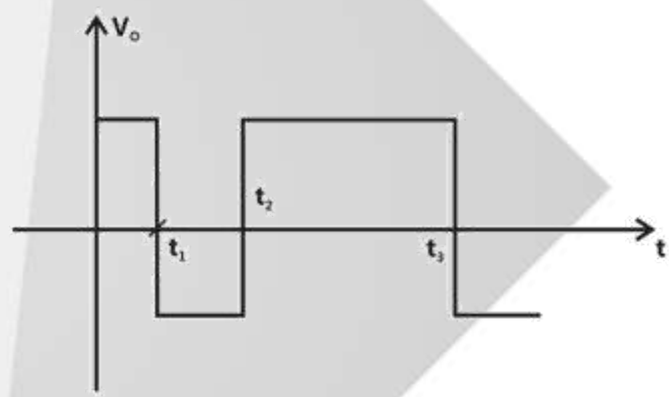
V_p = peak value of V_{IN}

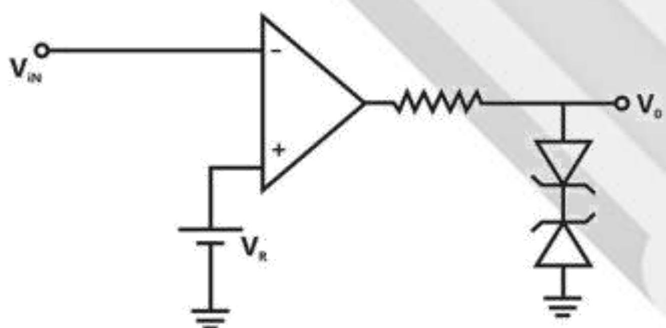


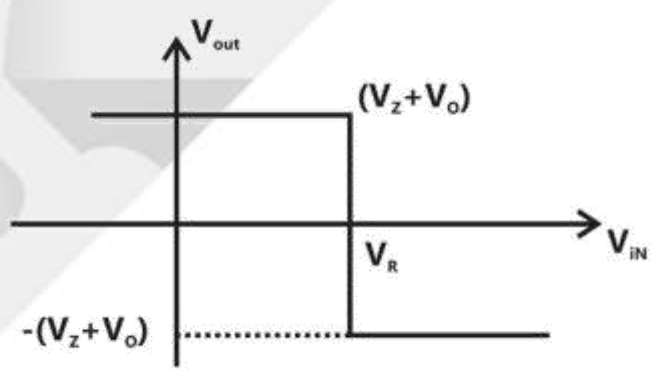
16) Comparators





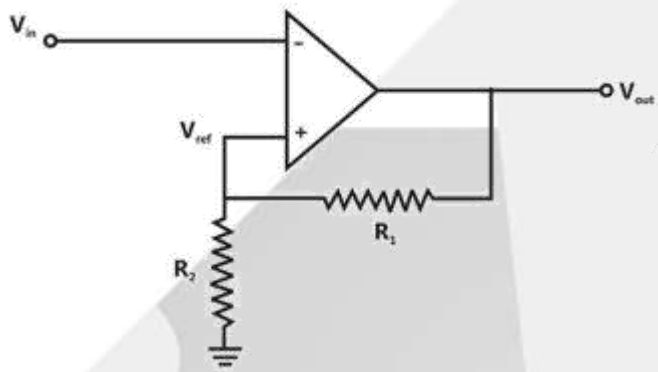


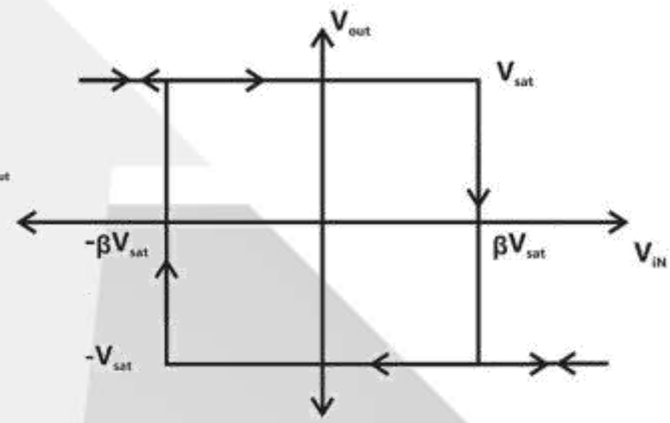




17) Schmitt Trigger

Inverting Schmitt Trigger





- When output is $+V_{sat}$, then $V_{ref} = \beta V_{sat}$
- When output is $-V_{sat}$, then $V_{ref} = -\beta V_{sat}$

  When $\beta = \dfrac{R_2}{R_1 + R_2}$

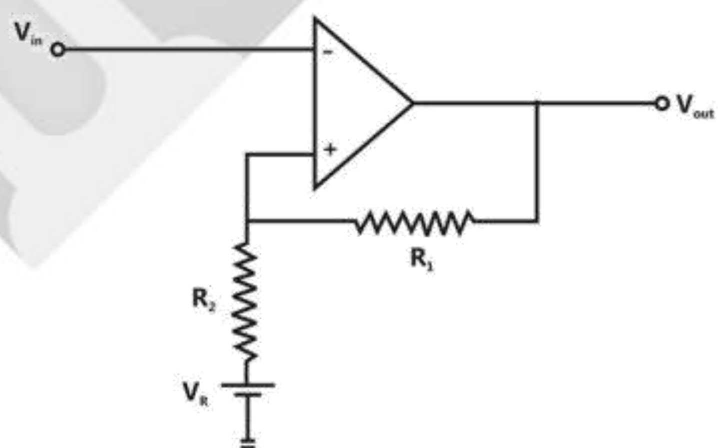
- Upper triggering point $(utp) = \beta V_{sat}$

  Lower triggering point $(Ltp) = -\beta V_{sat}$

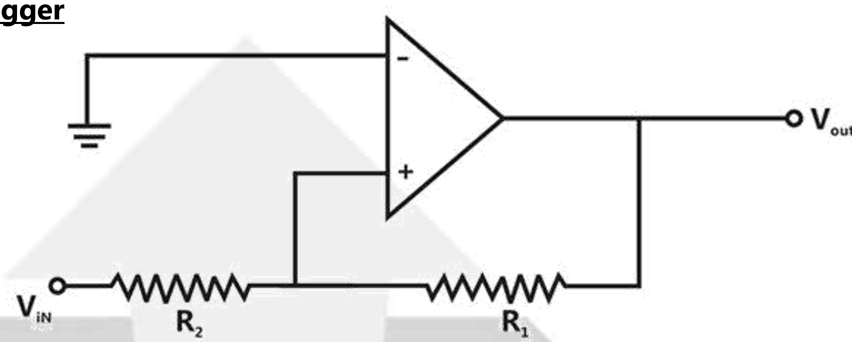
- Hystersis voltage = $UTP - LTP = 2\beta V_{sat}$

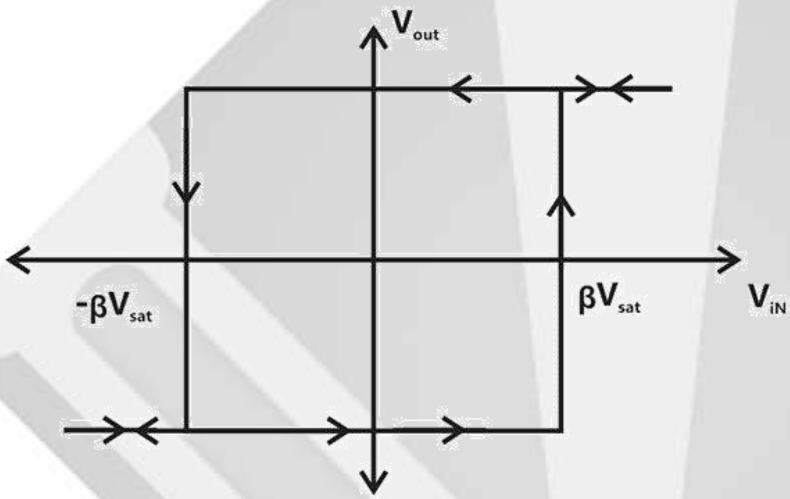
$$UTP = \beta V_{sat} + \frac{R_1}{R_1 + R_2} V_R$$

$$LTP = -\beta V_{sat} + \frac{R_1}{R_1 + R_2} V_R$$



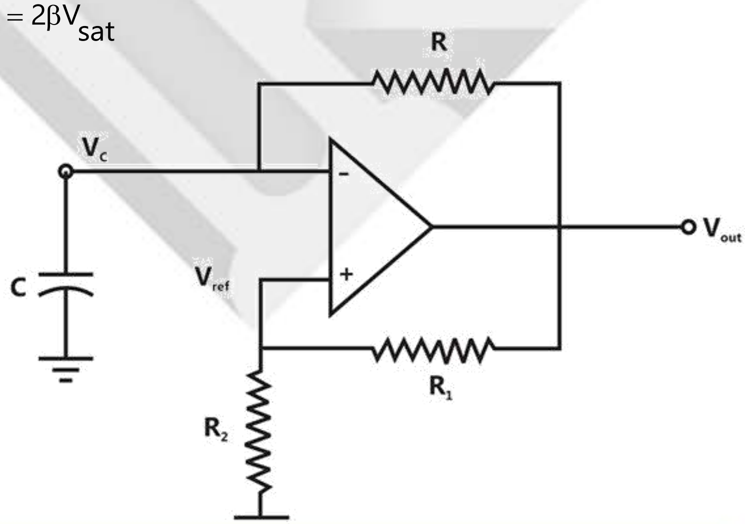
Non – Inverting Schmitt Trigger

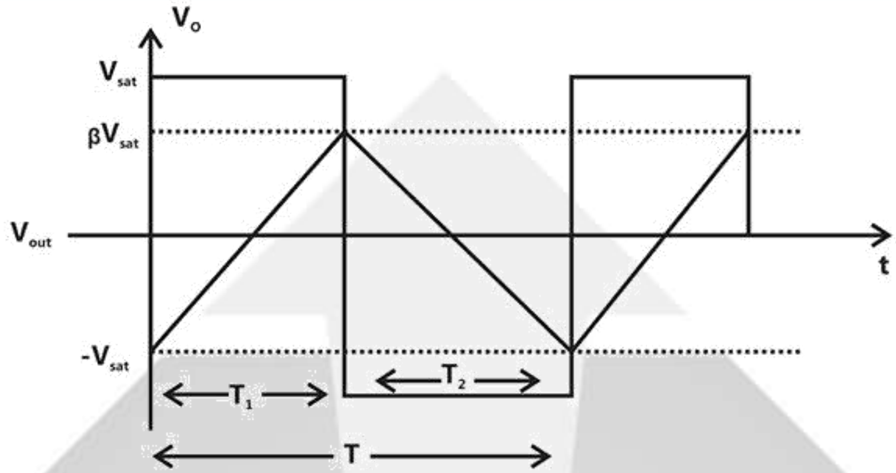




- Upper trigger Point $(UTP) = \frac{R_2}{R_1} V_{sat}$, Lower triggering point $(LTP) = \frac{-R_2}{R_1} V_{sat}$, $\boxed{\beta = \frac{R_2}{R_1}}$
- Hysteric voltage = $UTP - LTP = 2\beta V_{sat}$

18) Relaxation Oscillator





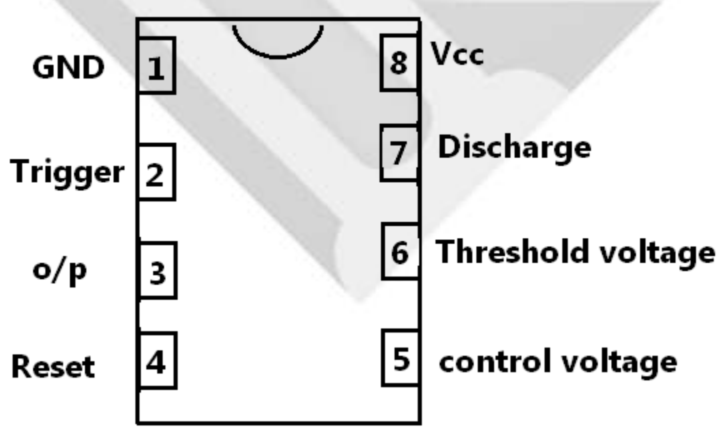
$$\beta = \left(\frac{R_2}{R_1 + R_2}\right)$$

$$T = 2RC\ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$f = \frac{1}{T} = \frac{1}{2RC\ln\left(\frac{1+\beta}{1-\beta}\right)}$$

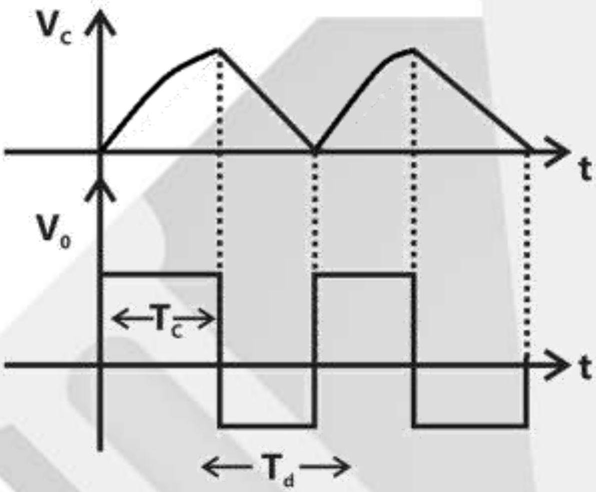
555 Timer

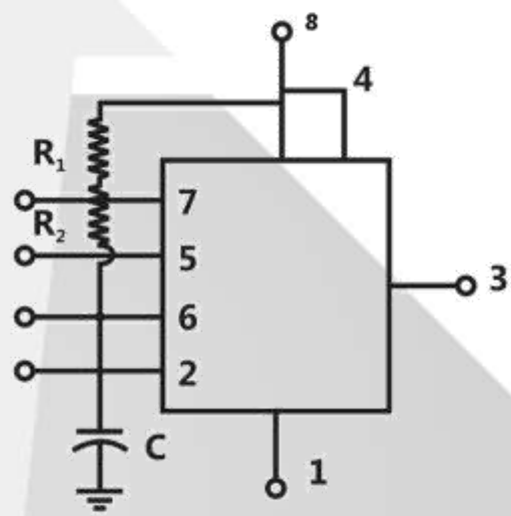
Pin Diagram



- Bistable multi vibrator acts as a FF.
- Monostable Multi vibrator produces pulse output.
- Bistable Multi vibrator acts as free running oscillator.

A stable Multi vibrator





$$T_c = 0.69(R_1 + R_2)c$$

$$T_d = 0.69R_2c$$

$$T = T_c + T_d = 0.69(R_1 + 2R_2)C$$

$$f = \frac{1}{T} = \frac{1}{0.69(R_1 + 2R_2)C}$$

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info@kreatryx.com
kreatryx.thegateguru@gmail.com
+91 7406144144 +91 9819373645 0120-4326333
Address - SE 617, Shastri Nagar, Ghaziabad, U.P (201002)

www.kreatryx.com