Digital Electronics Project 9 – Full Custom Final Project

Due: 23:59, June 8, 2023

In our final full custom IC design project, you are required to complete (A) a 2-input NAND gate implementation and (B) a 2-input NOR gate implementation from the front-end schematic to the back-end layout. Please design your own simulation stimuli for each gate so that the circuit behavior can be completely verified (tested).

Please submit your design project files according to the following rules:

1- The font size of your report is 12 in PDF format.
2- The filename is your team ID (e.g., T12.pdf).
3- List the names and student IDs of all team members.
4- Post the screenshot of your schematic.
5- Post the screenshot of your symbolic shape (symbol).
6- Post the screenshot of your layout.
7- Post the screenshot of your DRC and LVS reports.
8- Post the front-end SPICE file under simulation.
9- Post the back-end SPICE file under simulation.
10- Report the front-end and back-end slew rate and the propagation delay.
11- Post screenshots of your front-end and back-end waveforms.
12- Upload a tarball (e.g., T12.tgz) of your sp file, mt0 file, st0 file, and tr0 file from both "front-end schematic" and "back-end layout" simulations.