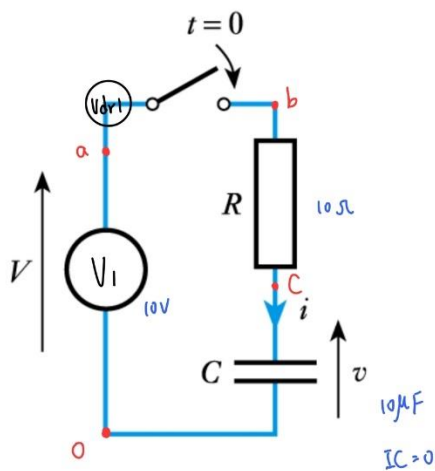
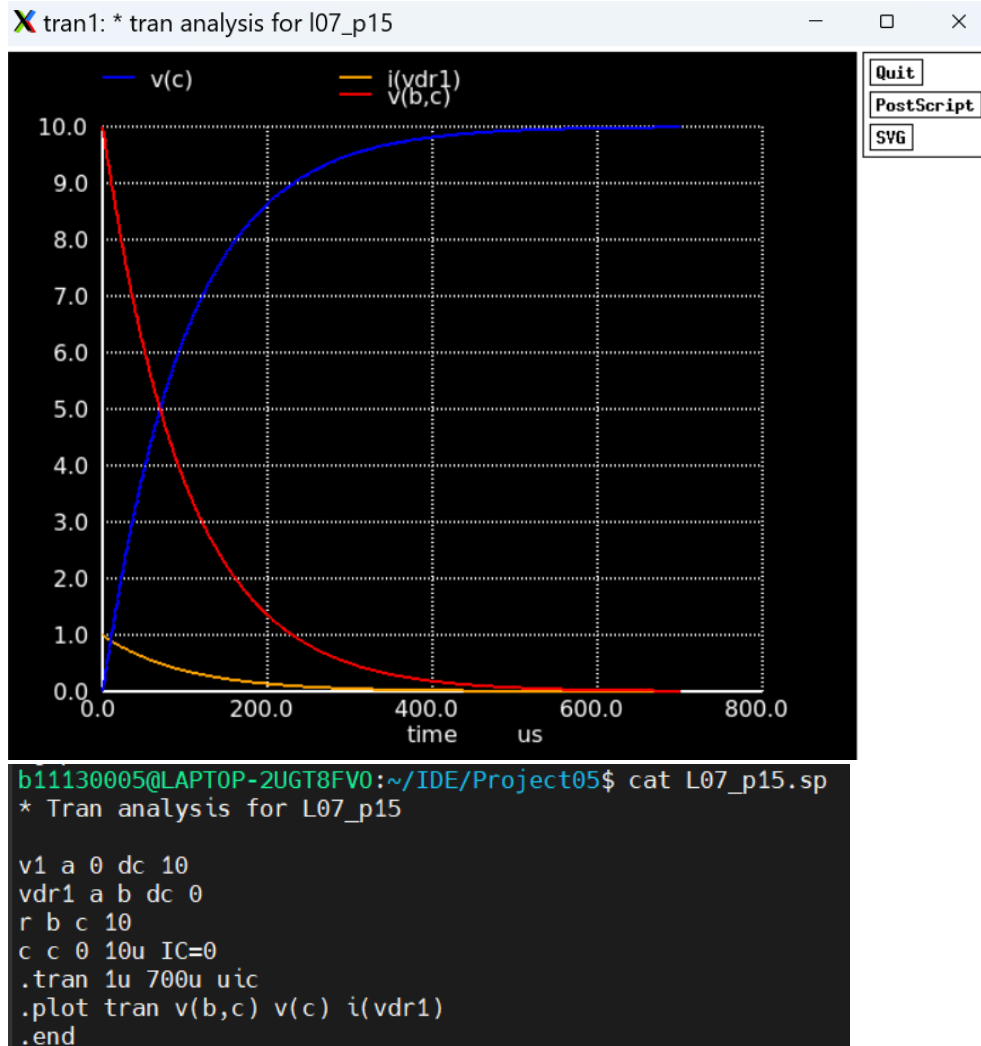
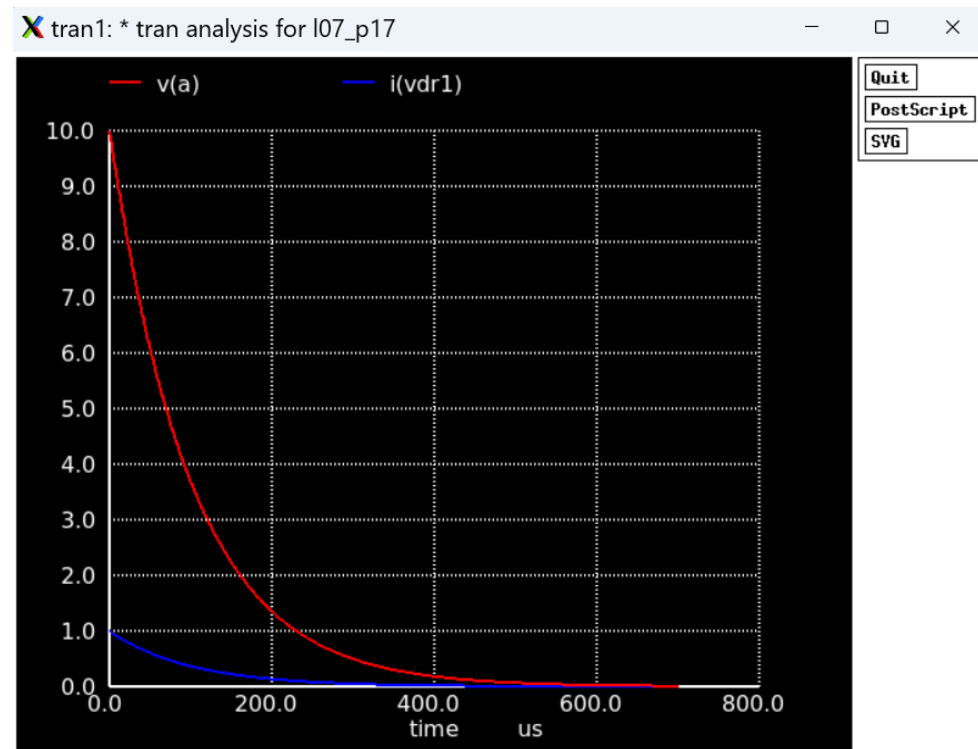


Project05

L07_p15

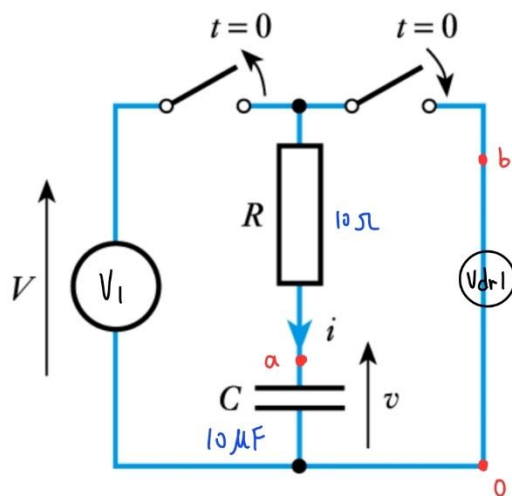


L07_p17

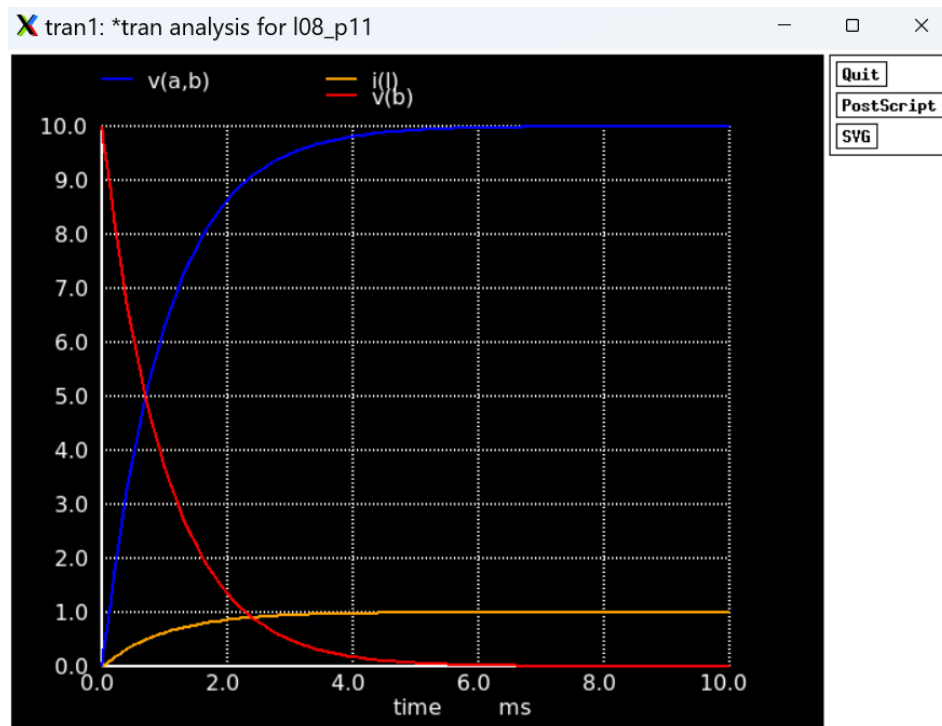


```
b11130005@LAPTOP-2UGT8FV0:~/IDE/Project05$ cat L07_p17.sp
* Tran analysis for L07_p17

vdr1 b 0 dc 0
r a b 10
c a 0 10u IC=10
.tran 1u 700u uic
.plot v(a) i(vdr1)
.end
```

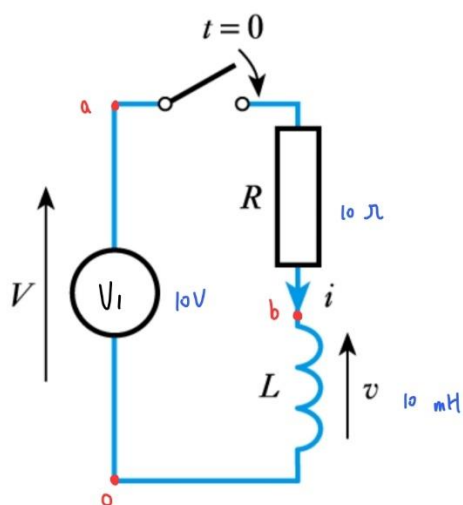


L08_p11

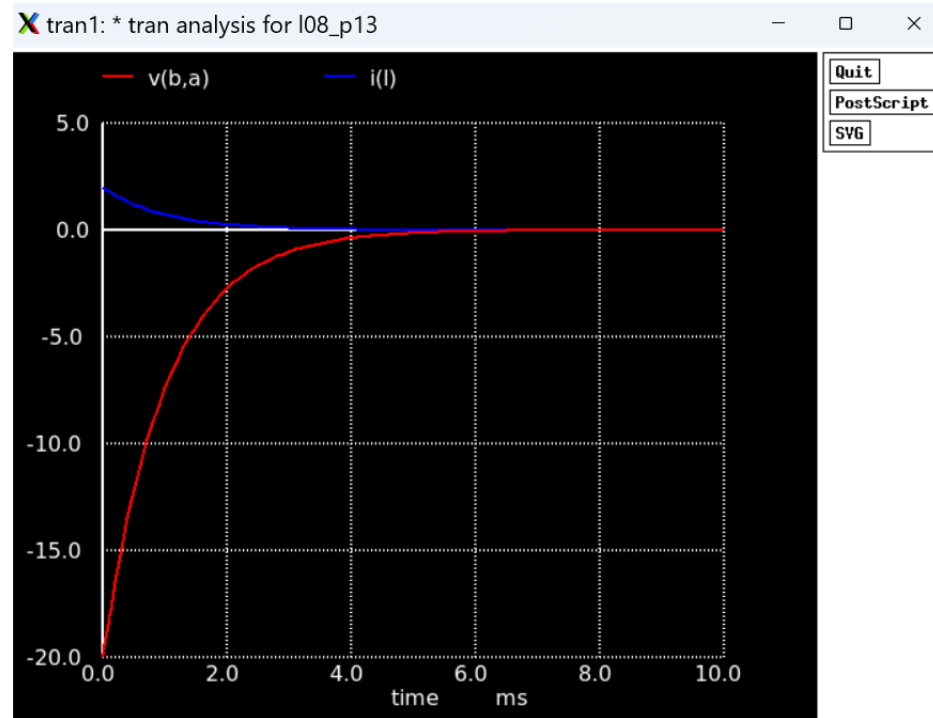


```
b11130005@LAPTOP-2UGT8FV0:~/IDE/Project05$ cat L08_p11.sp
*Tran analysis for L08_p11

v1 a 0 dc 10
r a b 10
l b 0 10m IC=0
.tran 0.1m 10m uic
.plot v(b) v(a,b) i(l1)
.end
```



L08_p13



```
b11130005@LAPTOP-2UGT8FV0:~/IDE/Project05$ cat L08_p13.sp
* Tran analysis for L08_p13

vdr1 a 0 dc 0
r b 0 10
l b a 10m IC=2
.tran 0.1m 10m uic
.plot v(b,a) i(l)
.end
```

