Digital Electronics Project 7 – Transistor Schematic

Due: 23:59, May 25, 2023

Full custom IC design is a bottom-up approach to construct a circuit from scratch based on transistor-level behaviors. In the beginning, IC designers specify the transistor schematic (front-end design) of their target circuit. Once the circuit schematic is completed, transistor-level simulation upon intended stimuli are required to ensure functional correctness before conducting the layouts (back-end design) at the geometrical level. We have demonstrated the front-end design flow for an inverter gate with two state-of-the-art industry commercial tools, Cadence Virtuoso schematic editor and Synopsys HSPICE circuit simulator. In this warm-up project, you are required to go through the inverter design yourself.

Please submit your design project files according to the following rules:

1- The font size of your report is 12 in PDF format.
2- The filename is your team ID (e.g., T01.pdf).
3- List the names and student IDs of all team members.
4- Post the screenshot of your schematic.
5- Post the screenshot of your symbolic shape (symbol).
6- Post the SPICE file under simulation.
7- Report the slew rate (rise/fall time) and the propagation delay (rising/falling).
8- Post the screenshot of your waveform.
9- Upload a tarball (e.g., T01.tgz) of your sp file, mt0 file, st0 file, and tr0 file from the front-end schematic simulation.