Digital Electronics Project 8 – Transistor Layout

Due: 23:59, June 1, 2023

Full custom IC design is a bottom-up approach to construct a circuit from scratch based on transistor-level behaviors. After completing the transistor schematics of a target design, the IC designer is required to conduct the corresponding circuit layout at the geometrical level. Once the circuit layout is completed, verifications – design rule check (DRC), layout versus schematic (LVS), and parasitic extraction (PEX) – and post-layout simulation are performed to ensure functional correctness before sign-off for final circuit tape out. We have demonstrated the back-end design flow for an inverter gate with three state-of-the-art industry commercial tools, Cadence Virtuoso layout editor, Siemens Calibre DRC/LVS/PEX layout verifier, and Synopsys HSPICE circuit simulator. In this project, you are required to go through the inverter design yourself.

Please submit your design project files according to the following rules:

1- The font size of your report is 12 in PDF format.
2- The filename is your team ID (e.g., T01.pdf).
3- List the names and student IDs of all team members.
4- Post the screenshot of your layout.
5- Post the screenshot of your DRC and LVS reports.
6- Post the SPICE file under simulation.
7- Report the slew rate (rise/fall time) and the propagation delay (rising/falling).
8- Post the screenshot of your waveform.
9- Upload a tarball (e.g., T01.tgz) of your sp file, mt0 file, st0 file, and tr0 file from the back-end layout simulation.