MLIR, CIRCT, and AHA

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Overview

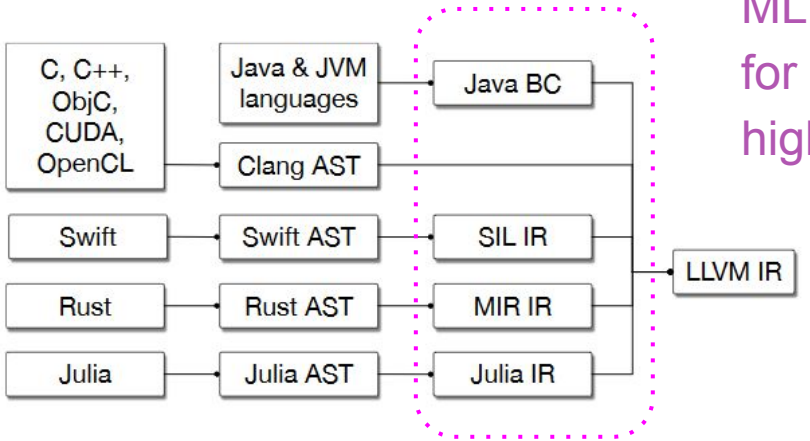
MLIR - Multi-level IR, a toolkit for creating domain-specific IRs (dialects)

CIRCT - Circuit IR Compilers and Tools

How AHA tools might interface with MLIR/CIRCT

MLIR

Motivation: common infrastructure for multi-/mid-level IRs



MLIR is a framework for developing higher-level IRs.

MLIR: A Compiler Infrastructure for the End of Moore's Law
https://arxiv.org/abs/2002.11054v2

MLIR Dialects

A custom IR with its own operations, attributes, and types

Mixable, composable for progressive lowering and expressivity

Dialects declaratively specified using
Operation Definition Specification (ODS)

MLIR Affine dialect operation

```
func @body(index) -> ()

func @simple_loop() {
  affine.for %i = 1 to 42 {
    call @body(%i) : (index) -> ()
  }
  return
}
```

Can mix dialects

```
func @body(index) -> ()

func @simple_loop() {
  affine.for %i = 1 to 42 {
    call @body(%i) : (index) -> ()
  }
  %c1 = constant 1 : index
  %c42 = constant 42 : index
  %c1_0 = constant 1 : index
  scf.for %arg0 = %c1 to %c42 step %c1_0 {
    call @body(%arg0) : (index) -> ()
  }
  return
}
```

Existing Dialects (not exhaustive)

affine - affine operations and analyses / polyhedral stuff
linalg - linear algebra
quant - quantization constraints and transformations
tf - tensorflow
tfl - tensorflow lite
xla - XLA
fir - Fortran
std - standard dialect
scf - structured control flow
pdl - high level abstraction for rewrite patterns
pdl_interp - lower level abstraction for rewrite patterns
llvm - wraps the LLVM IR types and instructions into MLIR
omp - OpenMP
acc - OpenACC
async - modeling asynchronous execution
avx512 - SIMD
vector - abstract SIMD
gpu - middle-level abstractions for launching GPU kernels
nvvm - wraps the NVVM IR (Nvidia)
rocdl - analogous to nvvm dialect but for AMD GPUs

What MLIR provides

Large community of users
Rich ecosystem of dialects
Reduced cost of building a compiler
Target-specific dialect operations
IR specification

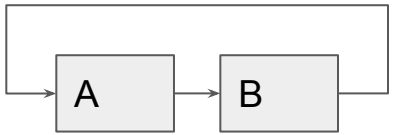
What MLIR won’t provide

Lowering/conversion passes
Type conversion (custom types)
Low level machine code generation
Dialects are not a source language

CIRCT

LLVM incubator project
Goal: MLIR/LLVM development methodology for hardware design tools

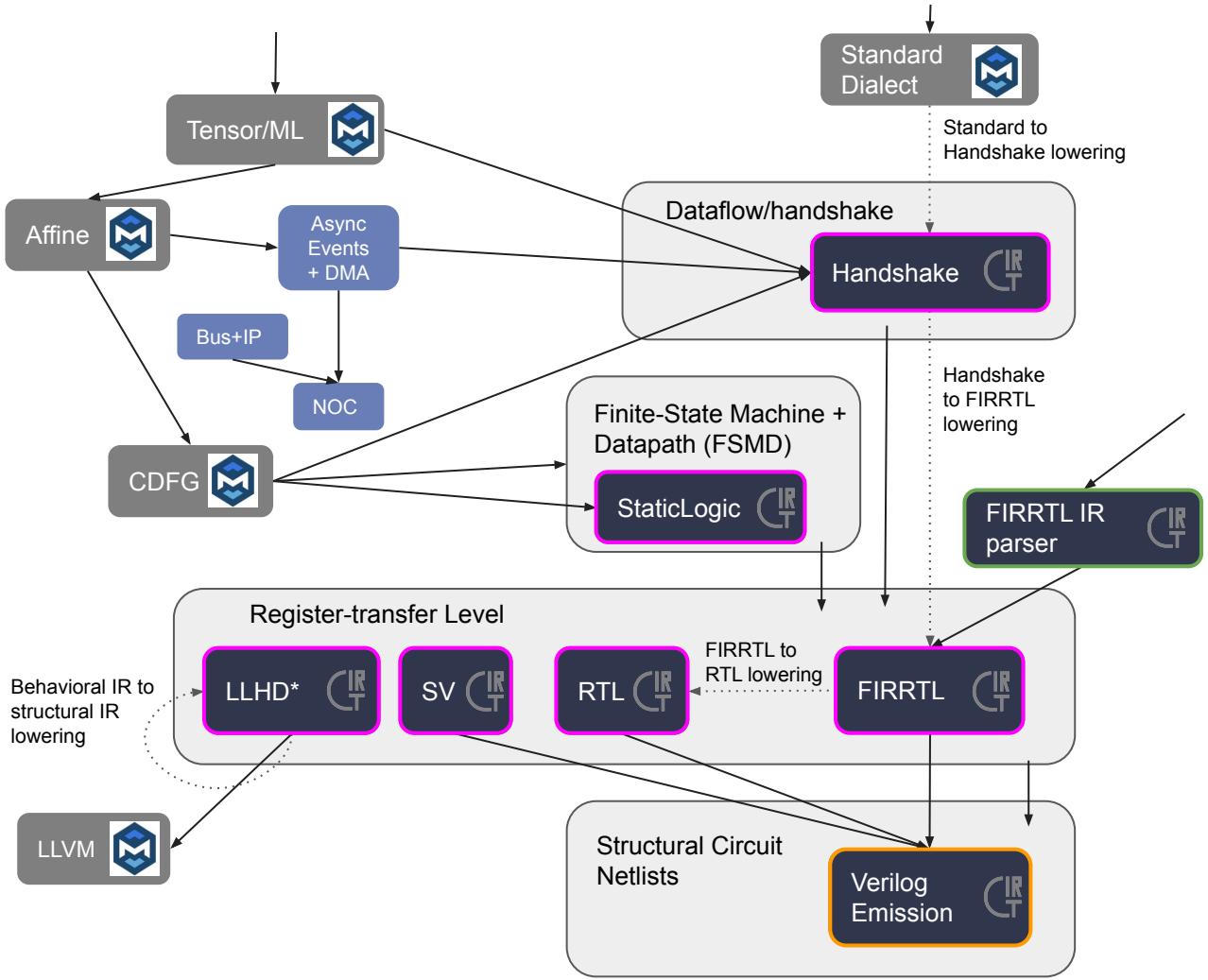
Parallel Compilation => Reduced design time
Multiple Abstractions/Dialect => Improved predictability
Unified Framework => Better integration between high/low level tools
Cyclic SSA graphs (from CIRCT folks) => hardware-oriented semantic models



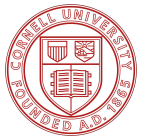

```
func @arbitrary() {
  %0 = foo.bar(%1)
  %1 = foo.baz(%0)
  return
}
```

Cyclic SSA!

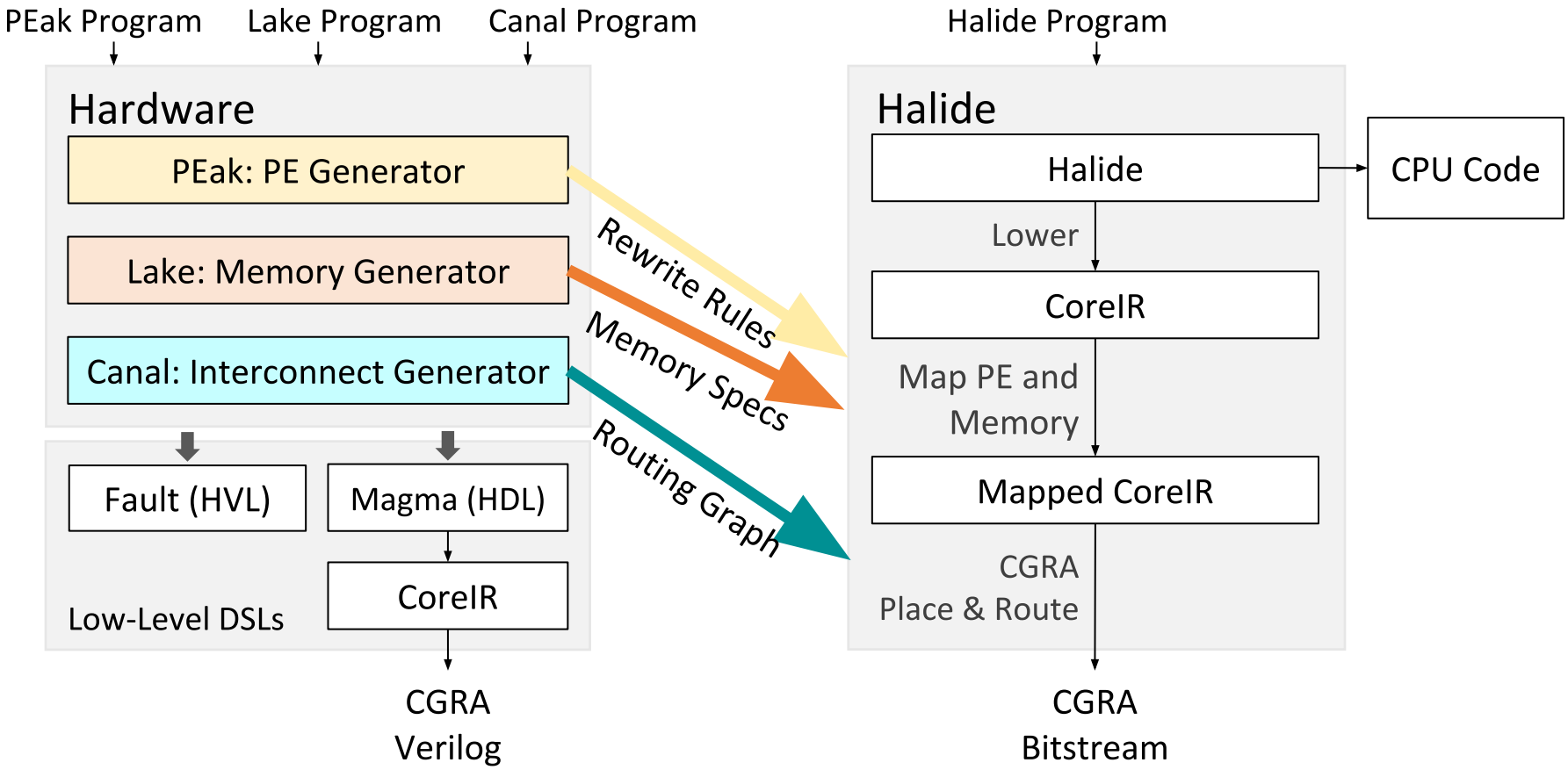
CIRCT


Standard Dialect
Standard to Handshake lowering
Tensor/ML
Affine
Async Events + DMA
Bus+IP
NOC
Dataflow/handshake
Handshake
Handshake to FIRRTL lowering
CDFG
Finite-State Machine + Datapath (FSMD)
StaticLogic
FIRRTL IR parser
Register-transfer Level
Behavioral IR to structural IR lowering
LLHD*
SV
RTL
FIRRTL to RTL lowering
FIRRTL
LLVM
Structural Circuit Netlists
Verilog Emission

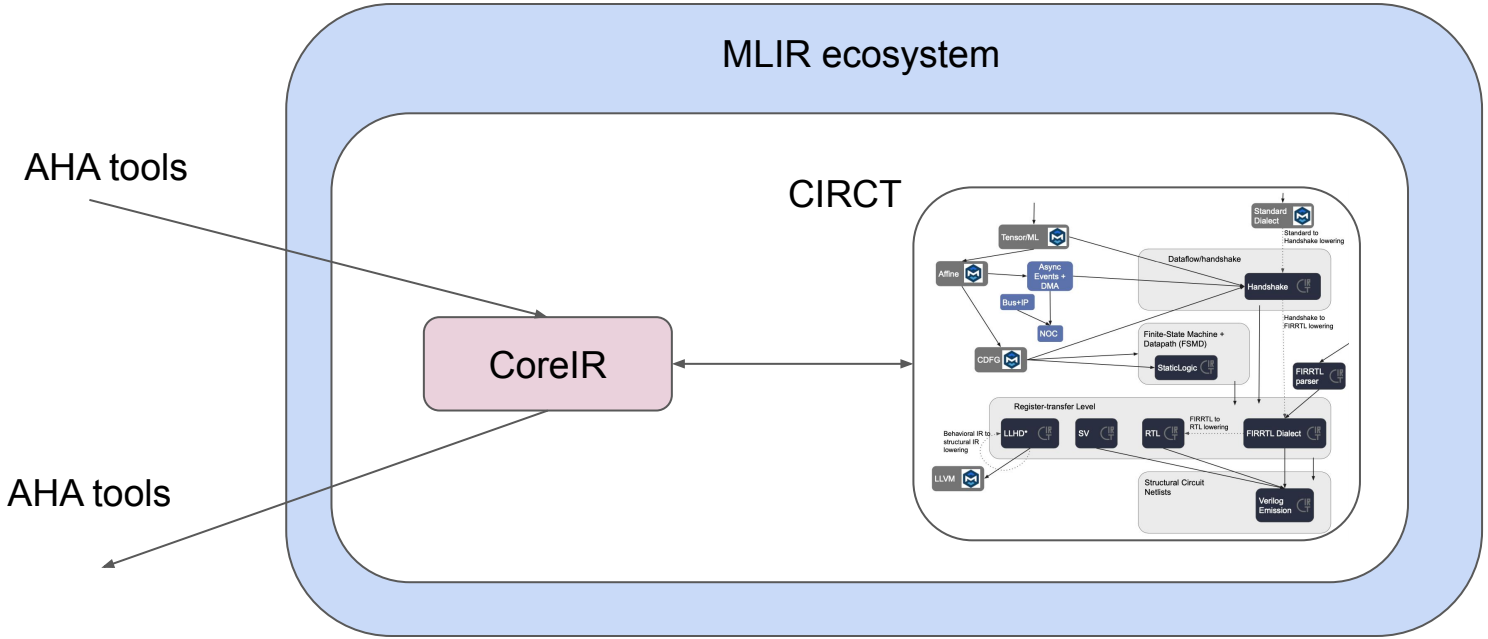
Who is involved with CIRCT and MLIR?



Hardware-Software Compiler Interaction in AHA

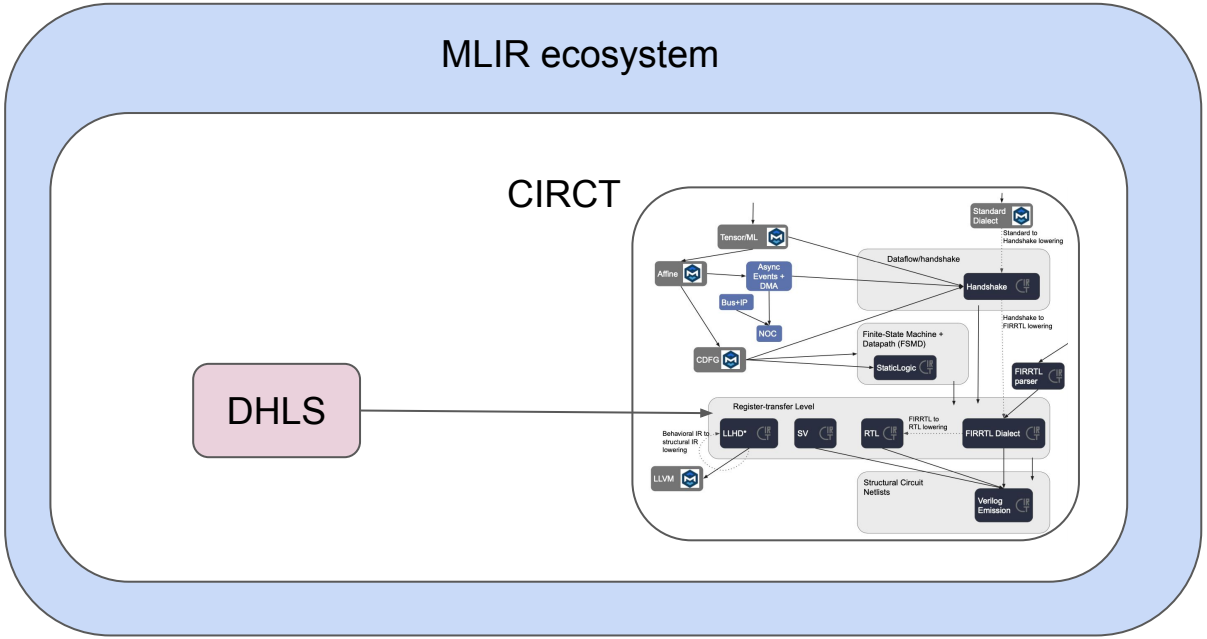


CoreIR and MLIR



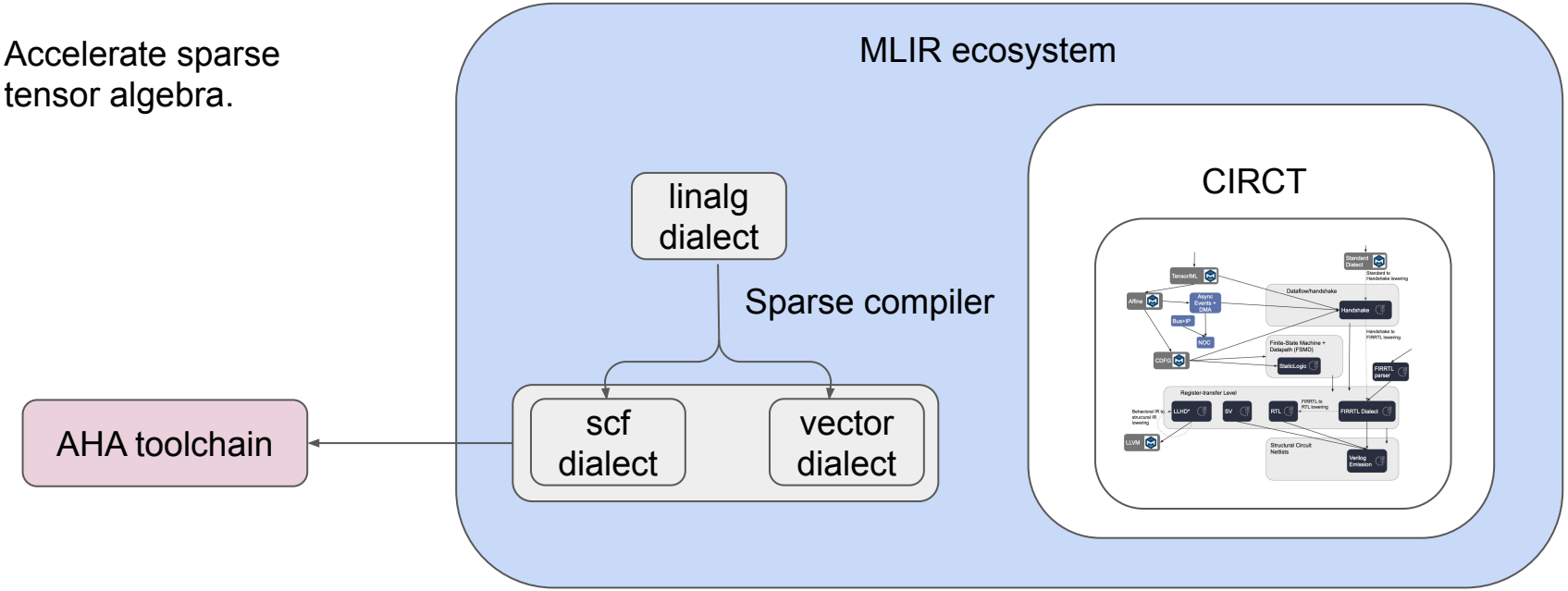
HLS and MLIR

Create an HLS tool designed from the ground up to be used by other compilers as a codegen backend.

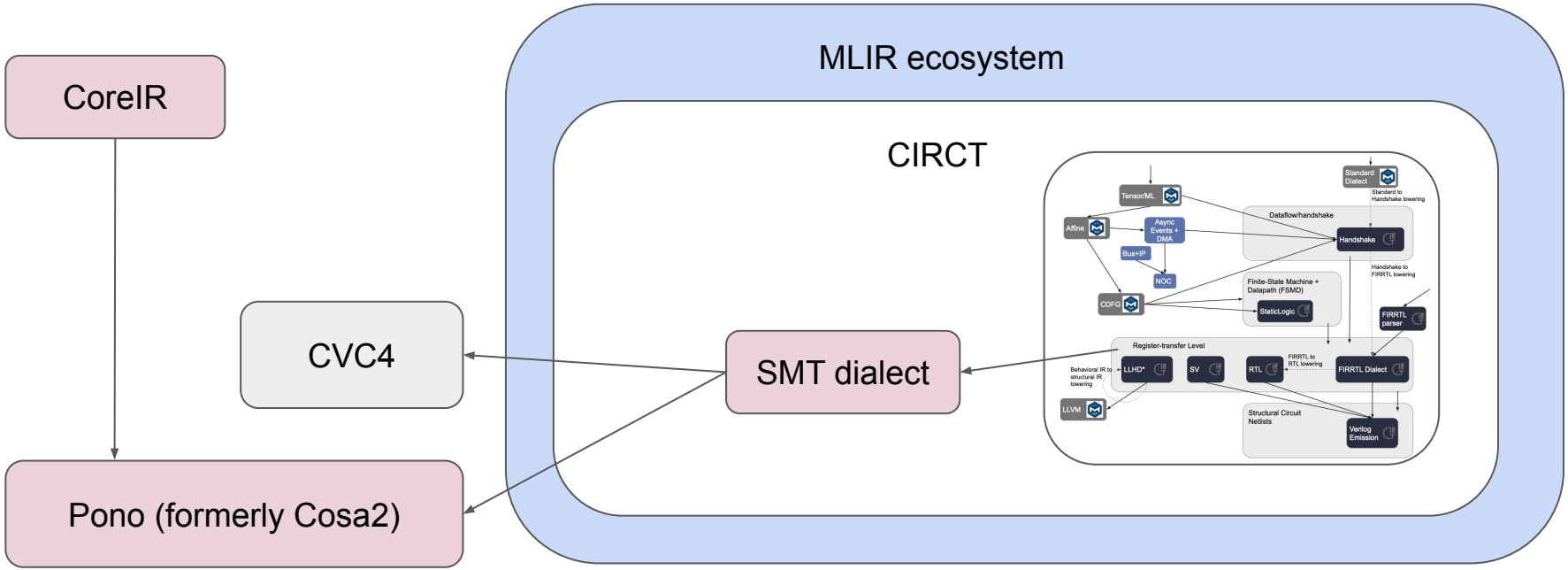


Sparsity and MLIR

Accelerate sparse tensor algebra.



SMT and MLIR


CoreIR
MLIR ecosystem
CIRCT
CVC4
SMT dialect
Pono (formerly Cosa2)
Standard Dialect
Standard to Handshake lowering
Tensor/ML
Affine
Async Events + DMA
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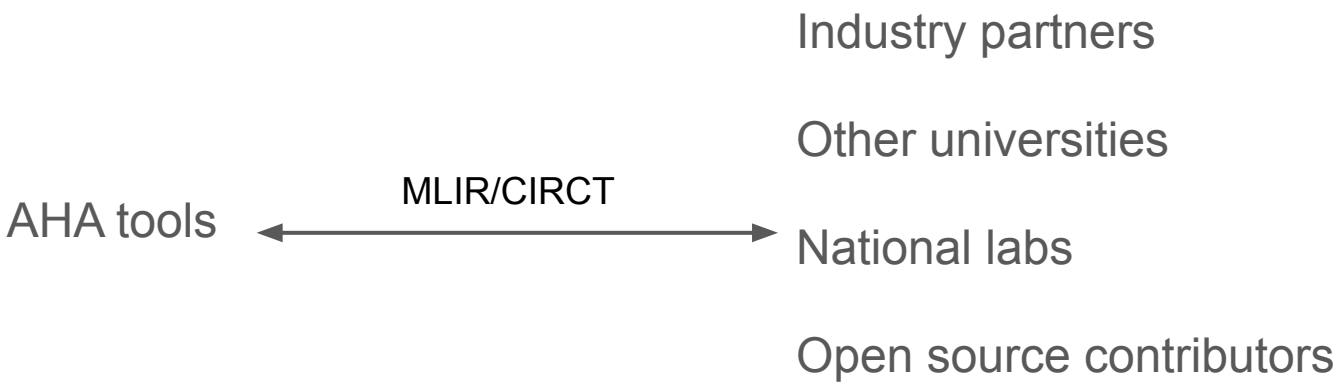
Conclusion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