Next-Generation CGRA Architecture

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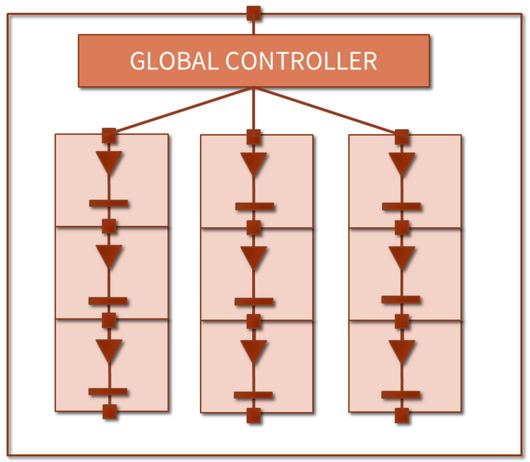
AGILE HW ARCHITECTURE GOAL

- Incremental high value additions to the complex HW system
- Two part process
  - Build CGRA – Build base array, add key features, repeat
  - Build SoC – Integrate CGRA with processor, IO devices etc.
- Next-Generation CGRA Effort
  - Fix the issues with last tapeout
  - New features to improve support for broader class of apps
  - Improve chip's PPA (Power-Performance-Area)
- Broader HW Development Effort: DL and modem processing apps

#1: FIX ISSUES WITH LAST TAPEOUT

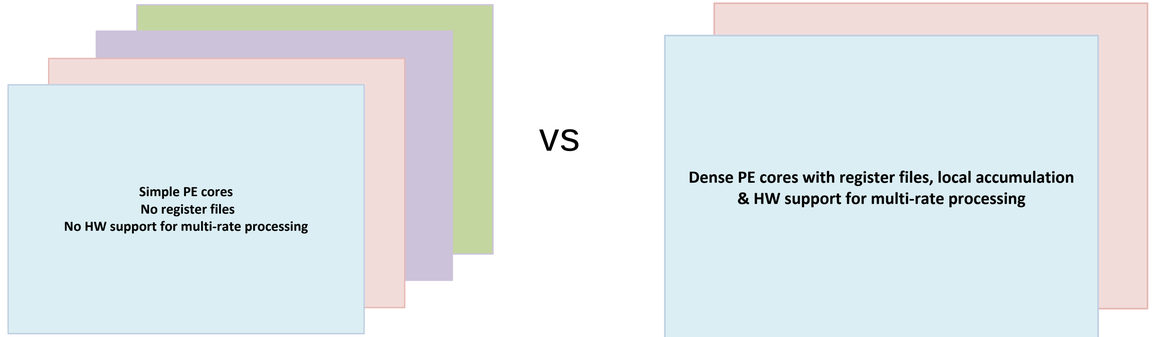
- Avoid global wiring problem due to high fanout synthesis in backend
- Build a modular design to embed wires in the block itself
- Mesochronous clocking network: same frequency, unknown phases
- Column based global signal distribution through tiles



New Global Signal Architecture

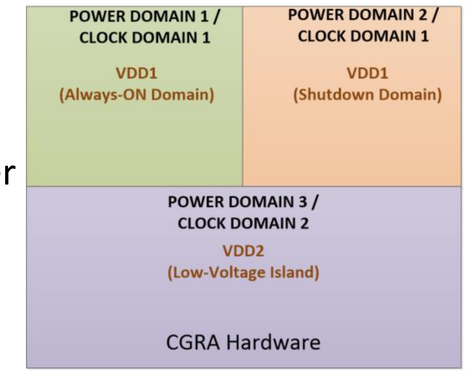
#2: ADD NEW FEATURES

- New PE operations and operand types (covered separately)
- CGRA HW virtualization: Enable re-use when app > HW resources
  - Fast reconfiguration techniques for rapid swapping of apps
  - Extend to enable FSM based design & multi-rate operations



#3: IMPROVE PPA

- Reduce power using clock and power domains: No performance impact
- Bring-up using agile approach
  - Power gate part of the chip not used - Use only AON domain to map apps
  - Need support from P&R, but not mapper
- Special handling on the boundary tiles for inserting isolation cells on output signals
- Generator for supporting power domains



Multi-Island CGRA

ISTC Agile