

AHA (Agile Hardware): Visual Computing

Planning Meeting

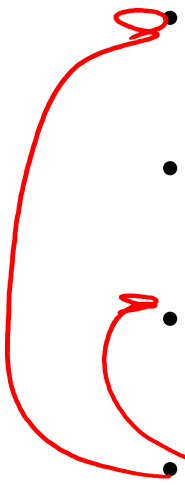
1/14/2021

Stanford | ENGINEERING
Electrical Engineering

Need to Set Goals For the Quarter

- Try something new this year
 - ▣ Throw out ideas of potential projects
 - ▣ Collect people who are interested in that idea
- We will seed the discussion with some potential projects
 - ▣ Feel free to add projects, if yours isn't listed

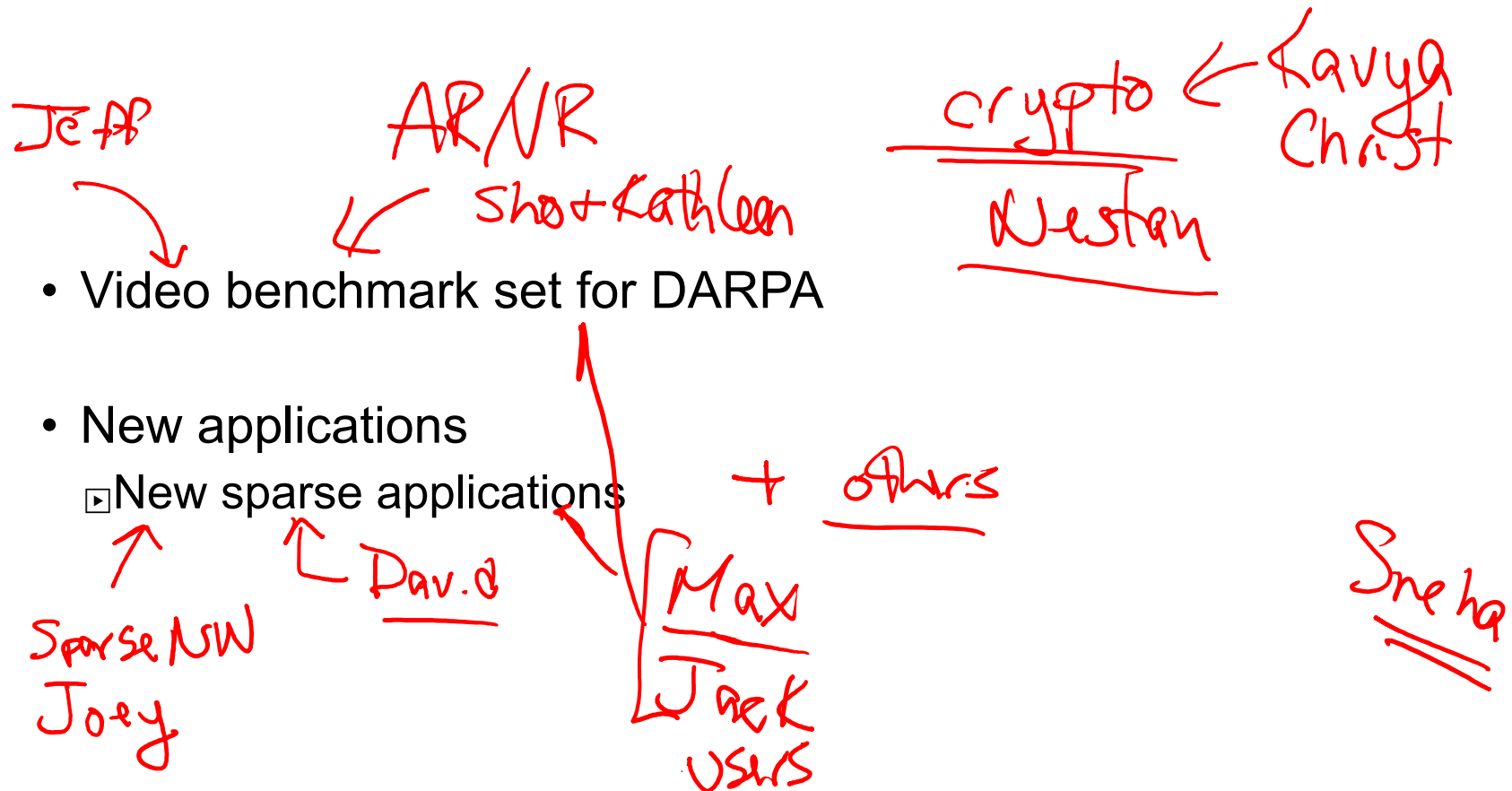
Bigger Picture Questions:

- Chip Bring-up
 - What is the goal of our next SoC?
 - New Applications we want to support
 - How to make our tool flow more robust
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- A red hand-drawn arrow starts from the 'Chip Bring-up' item and points to the 'New Applications we want to support' item. Another red hand-drawn arrow starts from the 'New Applications we want to support' item and points to the 'How to make our tool flow more robust' item. A third red hand-drawn arrow starts from the 'How to make our tool flow more robust' item and points back to the 'Chip Bring-up' item, forming a loop.

Main Areas

- Applications
- Compiler
- Validation
- Tools
- Hardware

Applications



Compiler

Jeff

Gedeon

Dillon

auto scheduling
Kalhan

Treyang

- Make the current Halide compiler chain more robust

- Support other memory uses

- ▣ Mapping / histograms

MAX

- Support sparsity

- ▣ Back end for Taco

- ▣ Generalize programming model Taco -> sparse numPy

auto scheduling

Ross (meta-flow)
Jack

Validation

- Bring formal into AHA
- Pono
- Model checking engines
- Source level hardware debugging

Ross → Using SMT auto debugging

Tools

Chris, Alex, Caleb, Keyi

- Creating/using “symbol table information” from Magma

- ▣ For test / debug, and physical design

Raj, Lenny, Ross

- DSE – more feature, more robust

Jack, Ross, Caleb

- CoreIR flow integration

- Lake

David, Kavya, Max, Taeyang, Ankita, Joey

Ankur + Ross → CoreIR ↔ MLIR

Ross → ROM

Hardware / Tools

- Improved:

- ▣ mflowgen

→ Chris, Gideon

- ▣ Magma

- “Smart” components

- ▣ Dealing with hardware generated at last moment

Lenny, Ross, Gideon, Kayva, Raj, Alex
Caleb, Nestor

- Power modeling framework (energy dictionary)

Kalhan, Kathleen, Raj, Max,

→ better agile Energy dictionary
↳ Joel,

SoC \Rightarrow Reg Seg Lang
Gedeon

Hardware

Zach, Kathleen, Gedeon, Keyi, Kalhan, Charles, Max
Treyang

- Creating chip testing environment

- Virtualization Treyang, Keyi, Kalhan, Gedeon

- Physical design aware hardware design

- Cypto hardware ✓

Jack

- Extended unified buffer (sparsity)

Joel, Max, Tim

Alex, Raj, Keyi

(Intersection units)

Quick query
How Hardware DL
can encode
more information