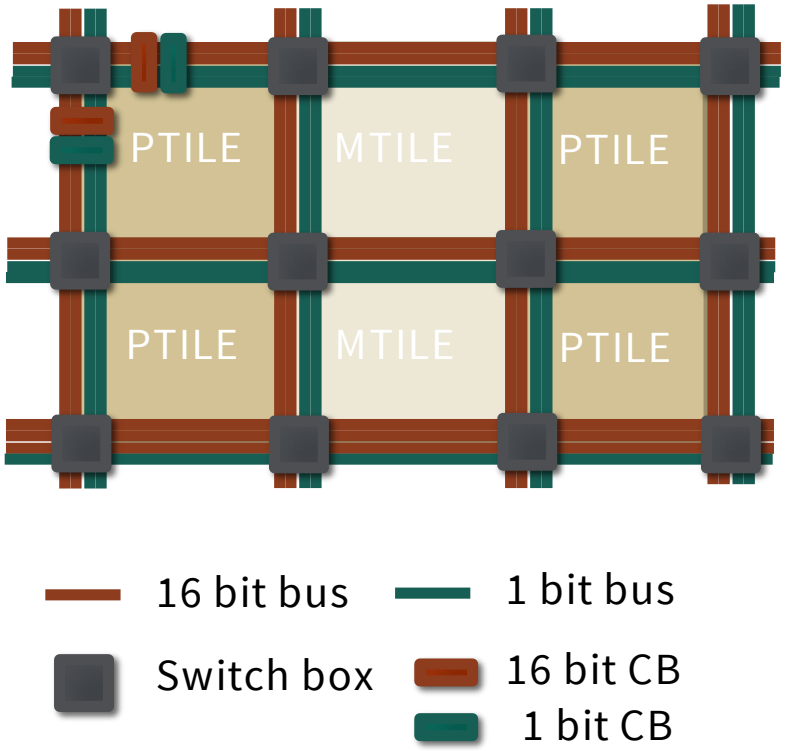
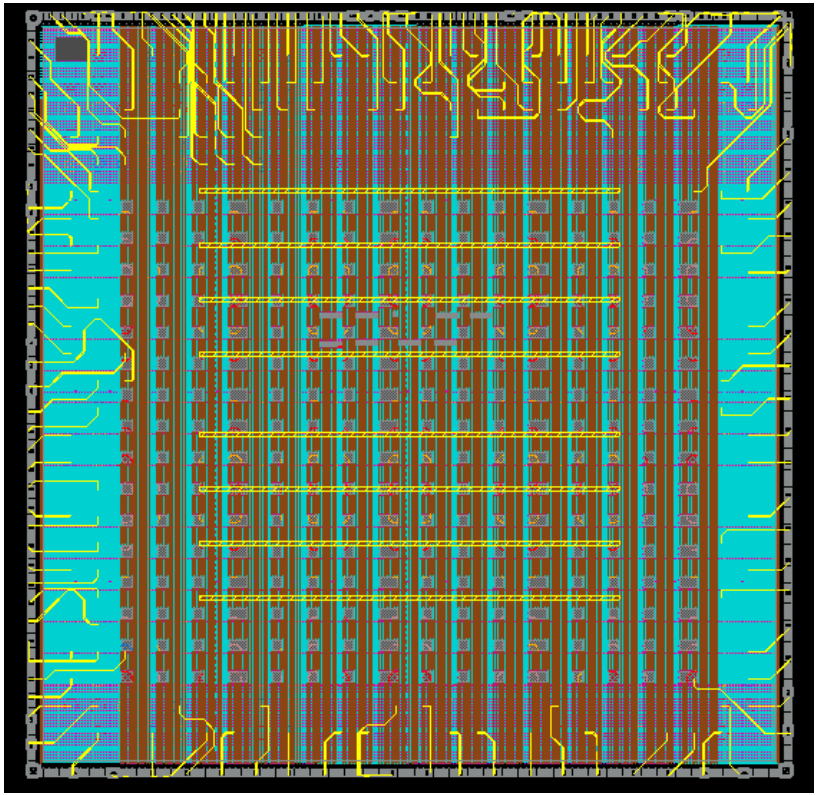
CGRA Architecture



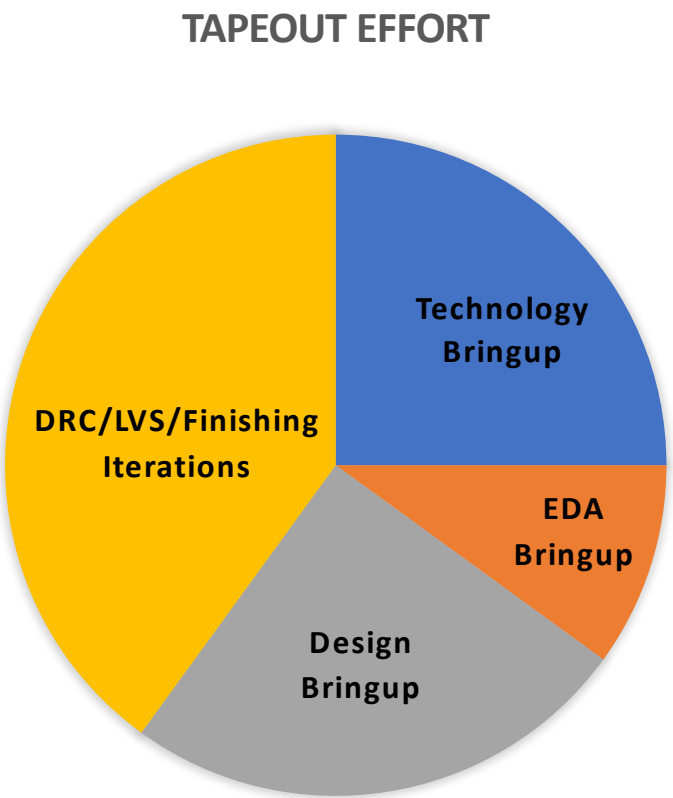
CGRA Specifications



CGRA Final Layout

- TSMC 16nm FFC PODE 10 ML
- 5mm x 5mm ; Flip Chip ; PIO
- 16x16 CGRA grid (192 PE : 64 Mem)
- 64 programmable IOs
- Tile addressable JTAG configuration
- 2KB per tile, 128KB total on-chip memory
- Single, always-on, power domain
- Uni-clock architecture
- Four 1-bit programmable global signals

Automating Physical Design

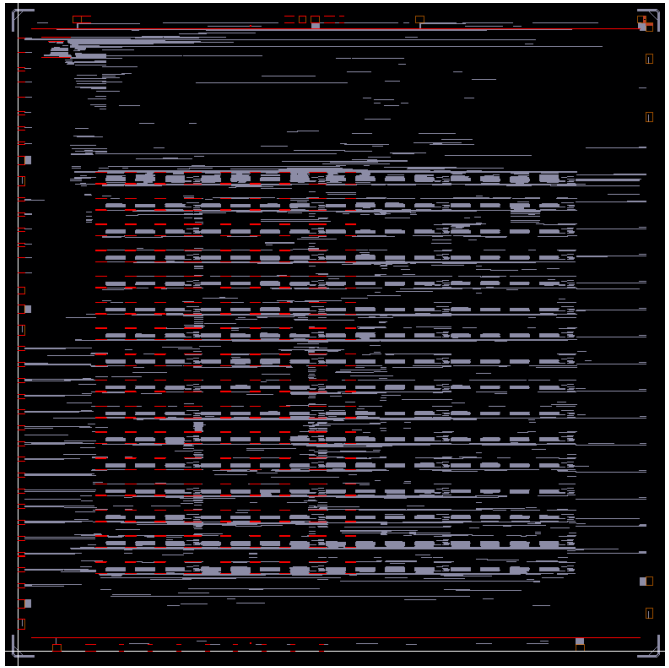


- Eight weeks from RTL to Tapeout
- Significant effort spent in getting a DRC clean PAD ring and core area
- PnR challenges when routing global signals across a die with non-boundary tile macros and long narrow channels
- Regular grid structure can be exploited to simplify PnR
- CGRA Verilog generator can also generate collateral for directing the PnR tool (UPF/CTS/etc.)

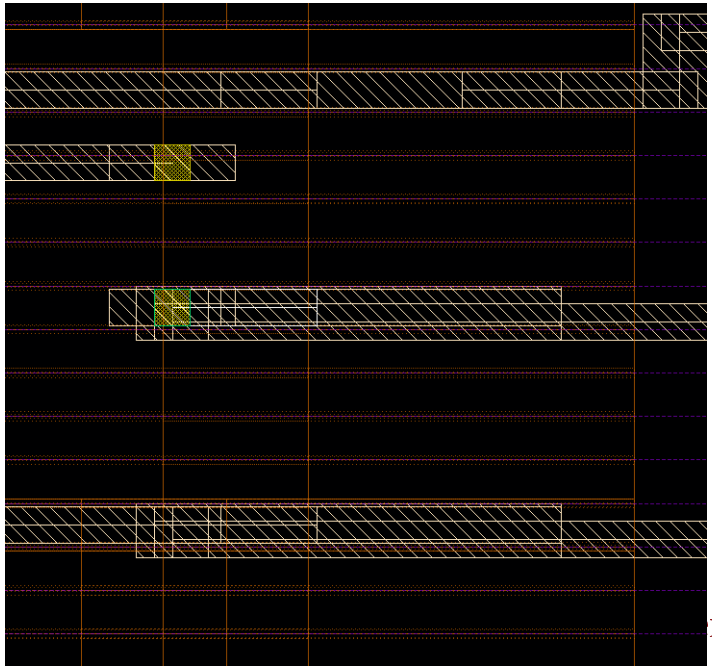
Innovus - Calibre Mismatch

- There were many issues in recent Tape-out(16nm FinFET) when running Full-Chip DRC
- All these errors ***couldn't be detected in Innovus***
- Examples

1) FIN / OD off-grid error (> # 1M)

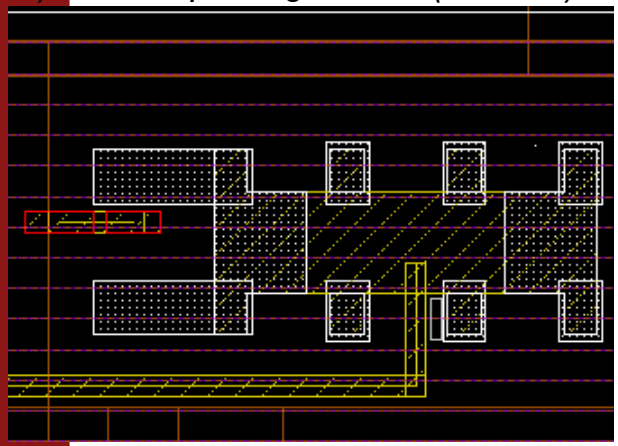
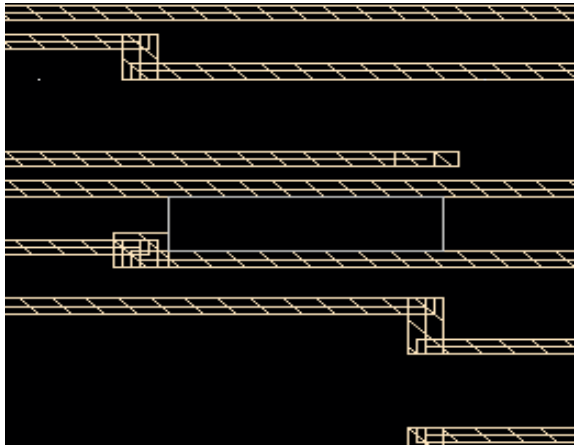
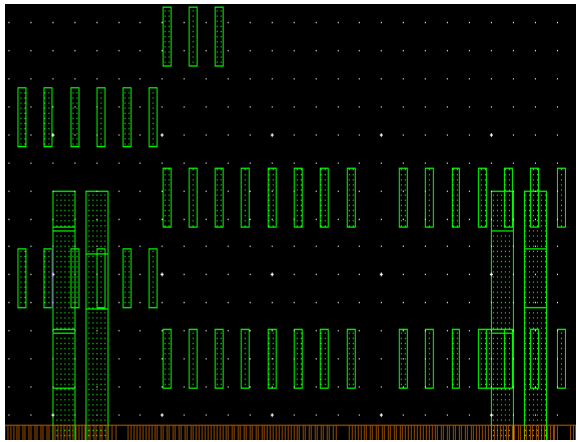
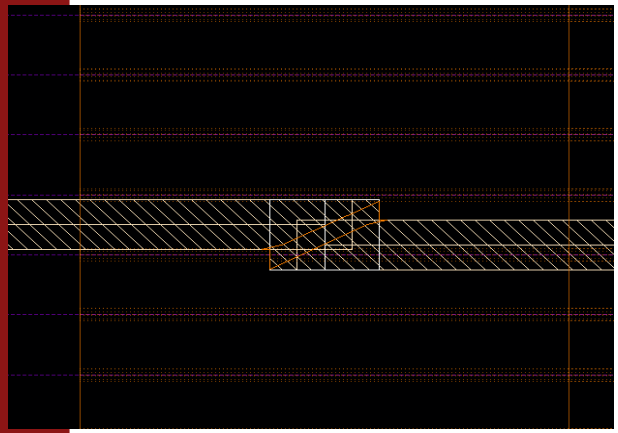
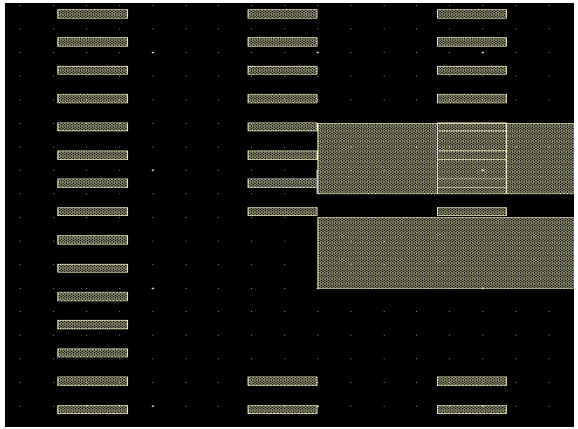
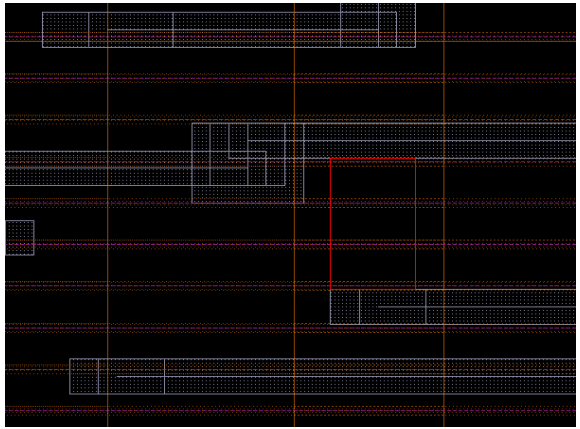


2) Pin off-grid error (~ #100)



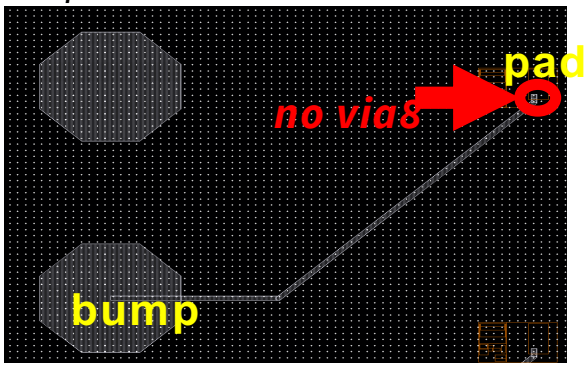
Innovus - Calibre Mismatch

3) Metal spacing errors (~ #200)

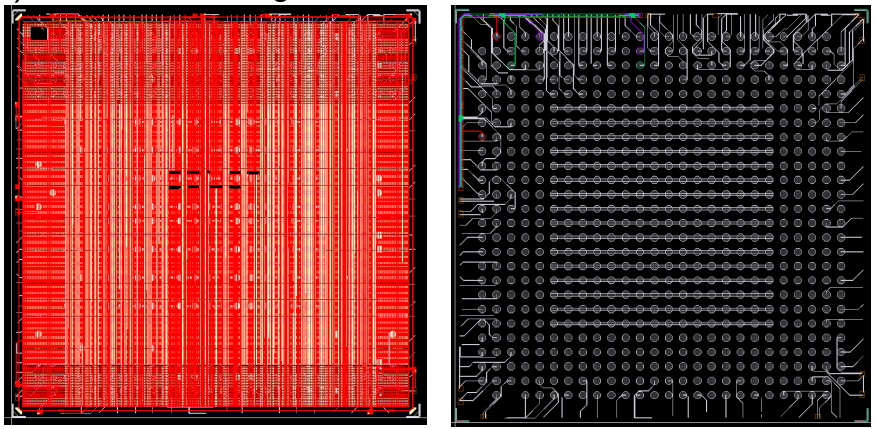







Innovus - Calibre Mismatch

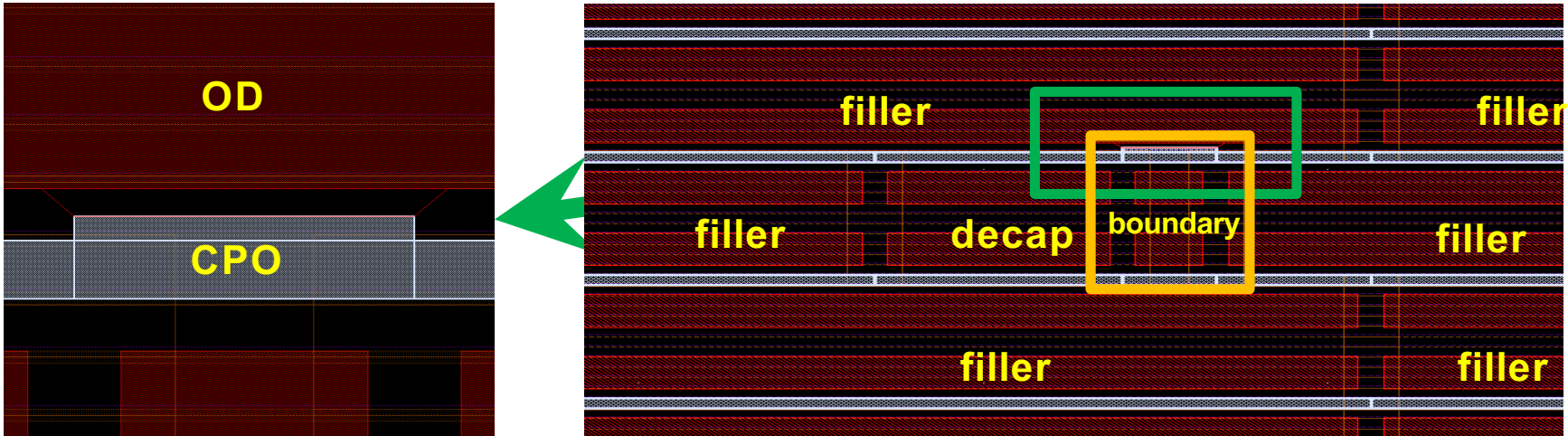
4) Bumps are not connected to PADs (~ #150)



5) Power shortage

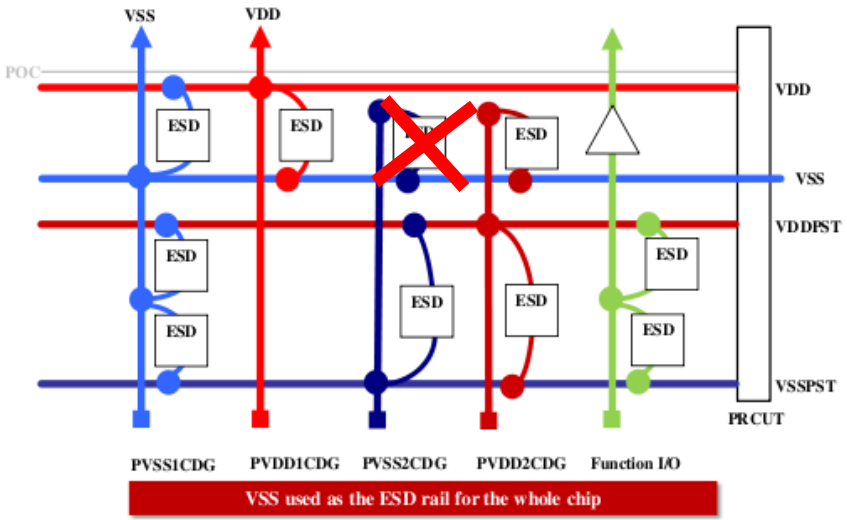


6) Cell misplacements

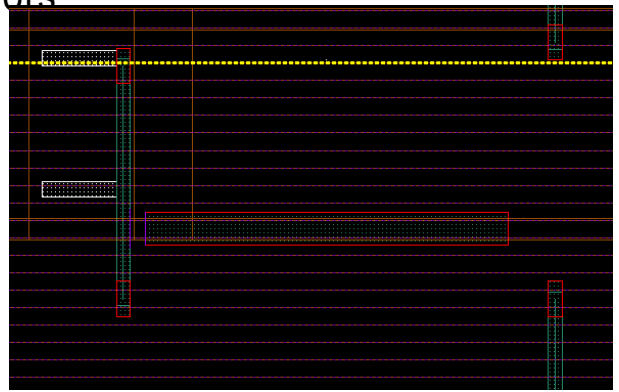


Innovus - Calibre Mismatch

7) Voltage dependent metal spacing / ESD (> #300M)



→ Absence of back-to-back diode between two grounds causes ***ESD errors*** and ***voltage dependent metal spacing*** errors



- Innovus cannot detect all DRC errors
- More than 3 weeks are taken to fix these errors by manual layout revision