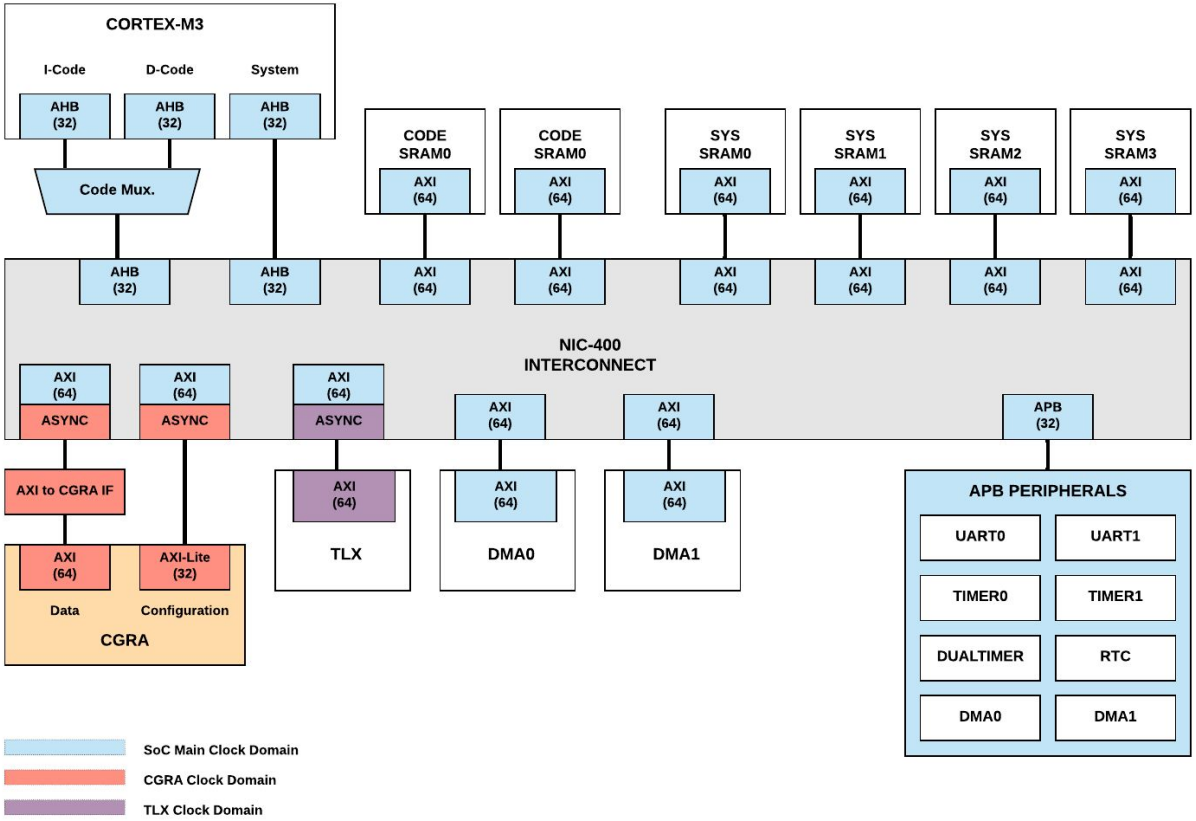
Garnet SoC

Hardware Architecture

System-Level Diagram

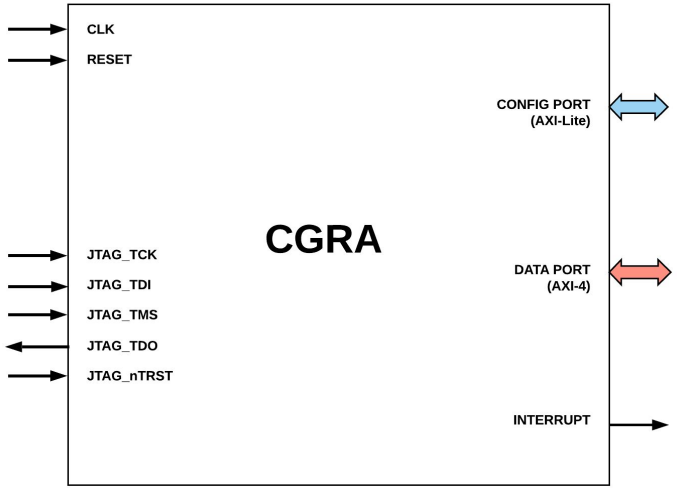


Garnet SoC

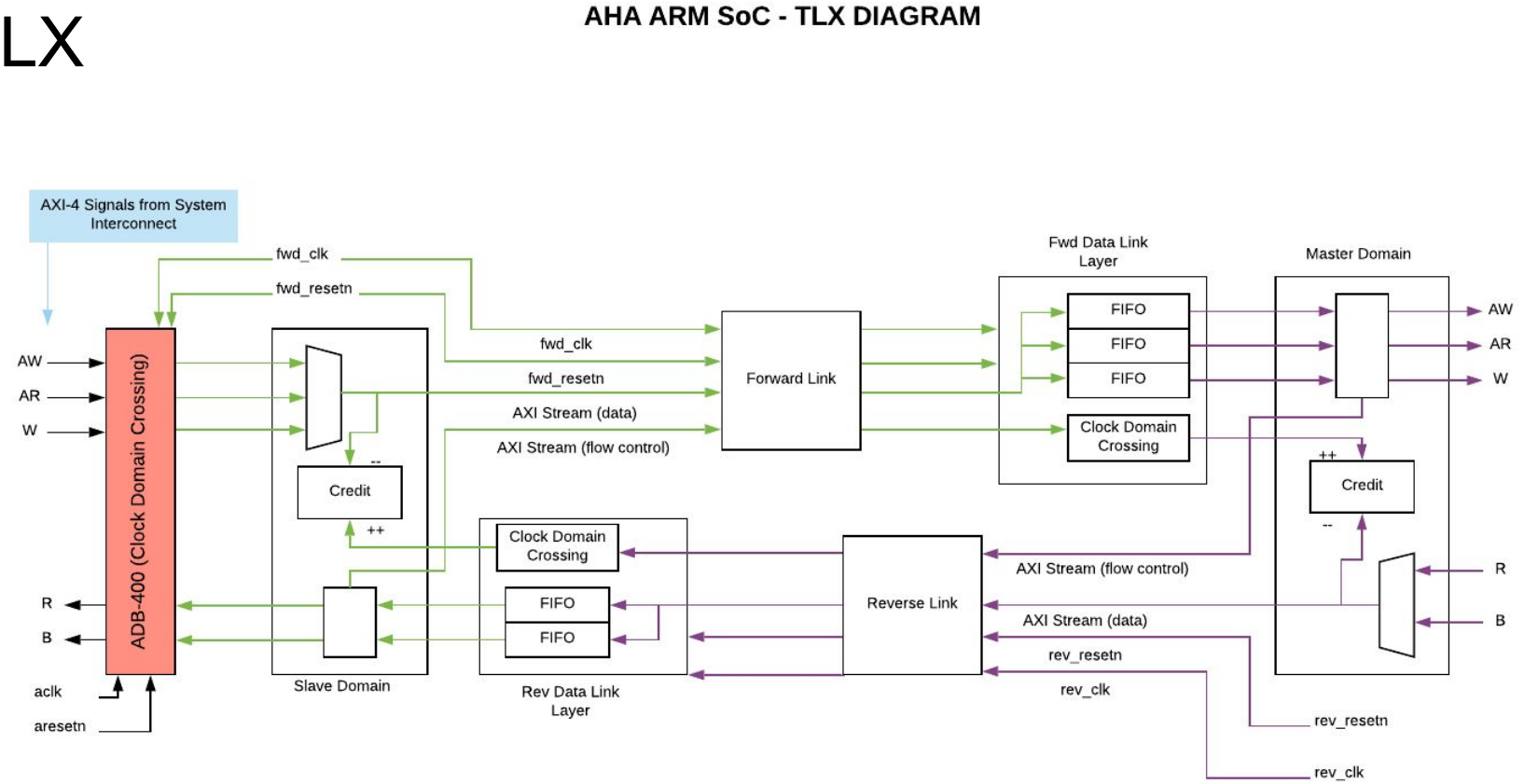
Key Components

CGRA (Coarse-Grain Reconfigurable Array)

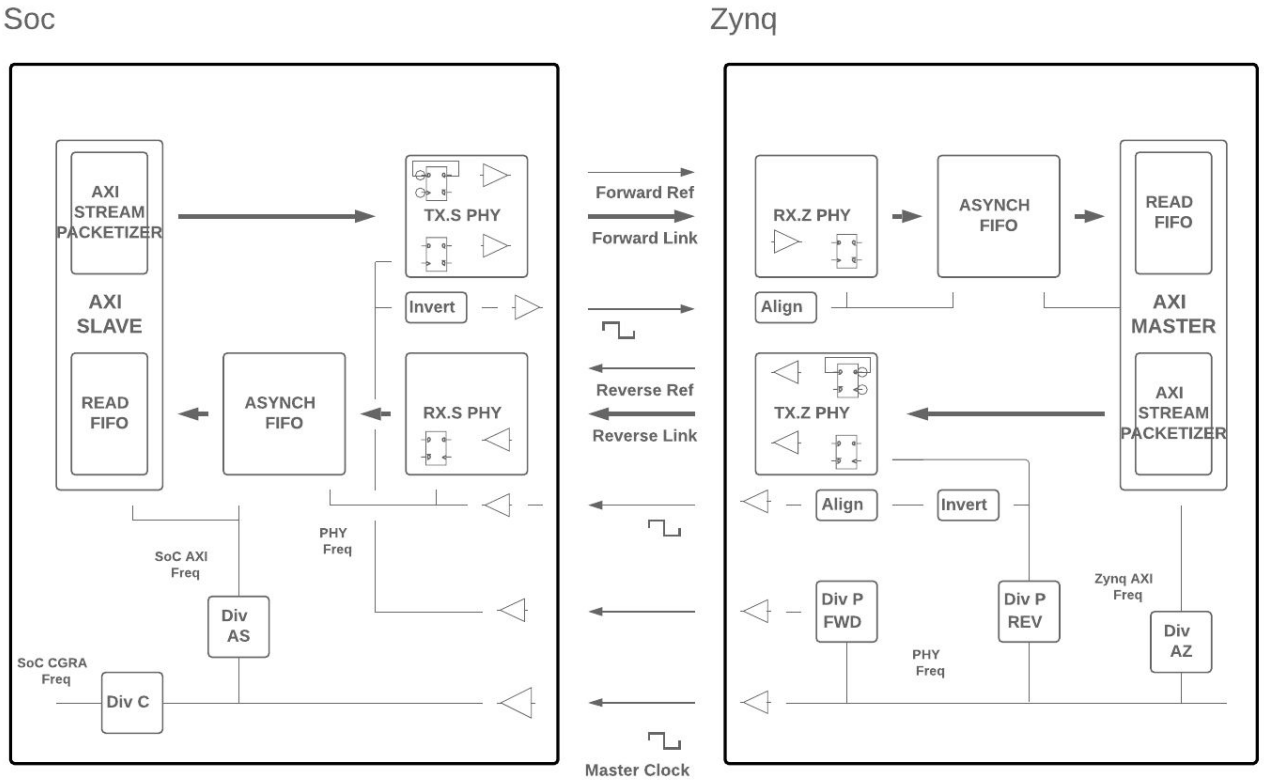
- 2 ports: Data and Configuration
- Data Port: 32-bit Address, 64-bit Data
- Config Port: 32-bit Address, 32-bit Data
- 1 Interrupt Line
- JTAG Debug Interface



TLX


AHA ARM SoC - TLX DIAGRAM
AXI-4 Signals from System Interconnect
fwd_clk
fwd_resetn
AW
AR
W
R
B
aclk
aresetn
ADB-400 (Clock Domain Crossing)
Credit
--
++
Slave Domain
fwd_clk
fwd_resetn
AXI Stream (data)
AXI Stream (flow control)
Forward Link
Fwd Data Link Layer
FIFO
FIFO
FIFO
Clock Domain Crossing
Master Domain
AW
AR
W
Credit
++
--
R
B
Clock Domain Crossing
FIFO
FIFO
Rev Data Link Layer
Reverse Link
AXI Stream (flow control)
AXI Stream (data)
rev_resetn
rev_clk
rev_resetn
rev_clk

TLX - Continued



TLX - continued

- TLX-400 ARM IP
- Forward Link (SoC to Zynq)
  - 40-bit data (multiplexing **AW**, **W**, **AR**, and control info)
  - Forward bandwidth percentage: 34%
- Reverse Link (Zynq to SoC)
  - 80-bit data (multiplexing **R**, **B**, and control info)
  - Reverse bandwidth percentage: 100%
- Pin Count: 137 pins

AW = AXI Write Address Channel
W = AXI Write Data Channel
AR = AXI Read Address Channel
R = AXI Read Data Channel
B = AXI Write Response Channel

DMA

- PL-330 ARM IP
- 2 DMA engines with 2 Channels per engine
- 32-bit Address, 64-bit Data
- Internal buffers implemented using registers (32 x 64-bit buffers)
- Instruction cache: 4 Lines with 8 instructions per line (total 32 instructions)
- Write issuing capability: 4 active write transactions
- Read issuing capability: 8 active transactions

System Interconnect

- NIC-400 IP
- 32-bit Address, 64-bit Data
- Multi-Layer AXI Interconnect
- Asynchronous Boundary for CGRA and TLX
- 3 Masters: Cortex-M3, DMA0, DMA1
- Peripheral APB Port

CoreSight Integration (Debug)

- CGRA and Processor connected in a chain
- ***Full Access*** (CGRA and Processor) in JTAG mode
- ***Isolated Access*** (processor-only) In SWD Mode
- Complete System Debug through Processor