AHA (Agile Hardware): Visual Computing

Planning Meeting

1/14/2021

Stanford | ENGINEERING
Electrical Engineering

Need to Set Goals For the Quarter

- Try something new this year
  - Throw out ideas of potential projects
  - Collect people who are interested in that idea
- We will seed the discussion with some potential projects
  - Feel free to add projects, if yours isn't listed

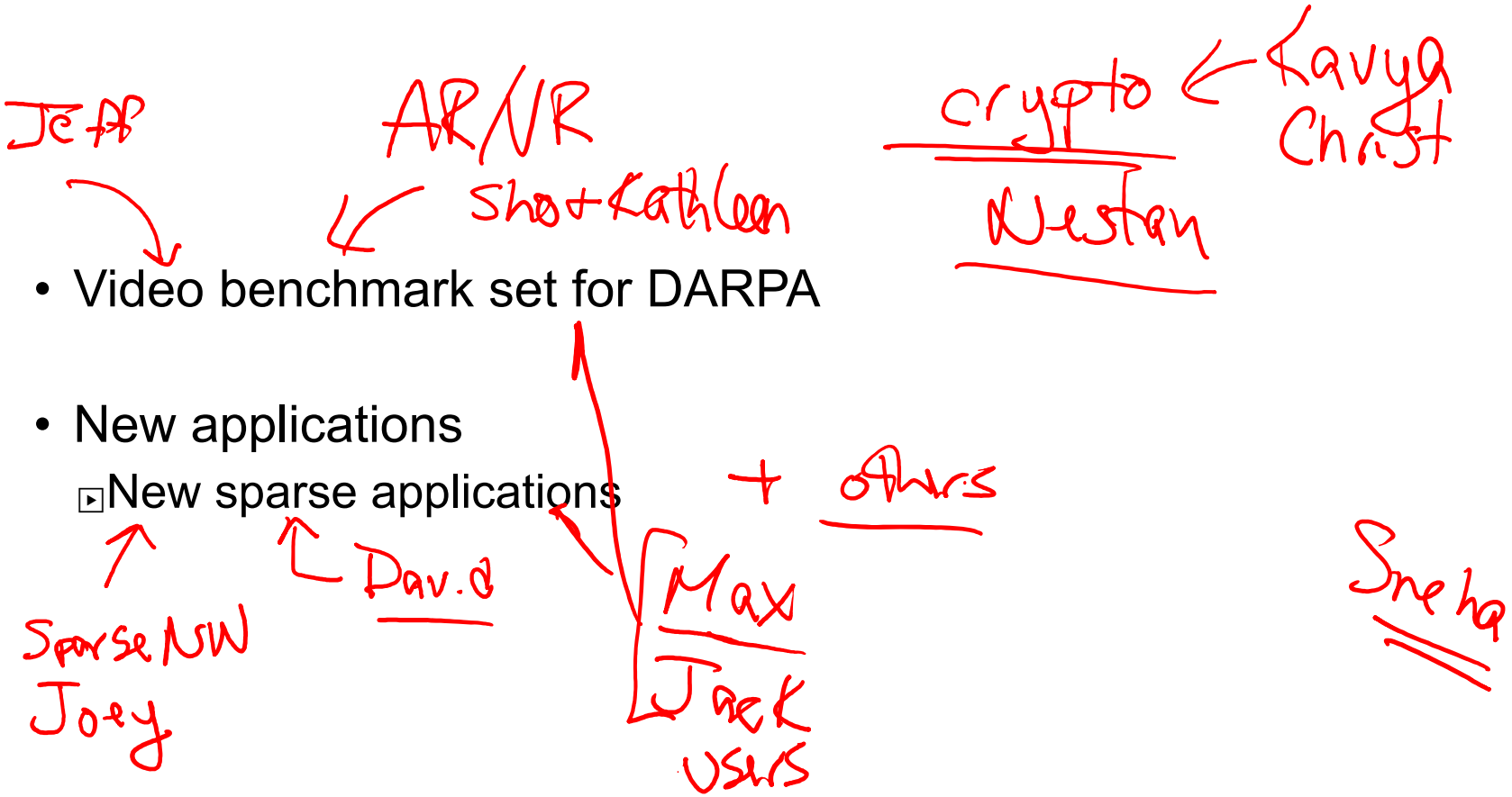
Bigger Picture Questions:

- Chip Bring-up
- What is the goal of our next SoC?
- New Applications we want to support
- How to make our tool flow more robust

Main Areas

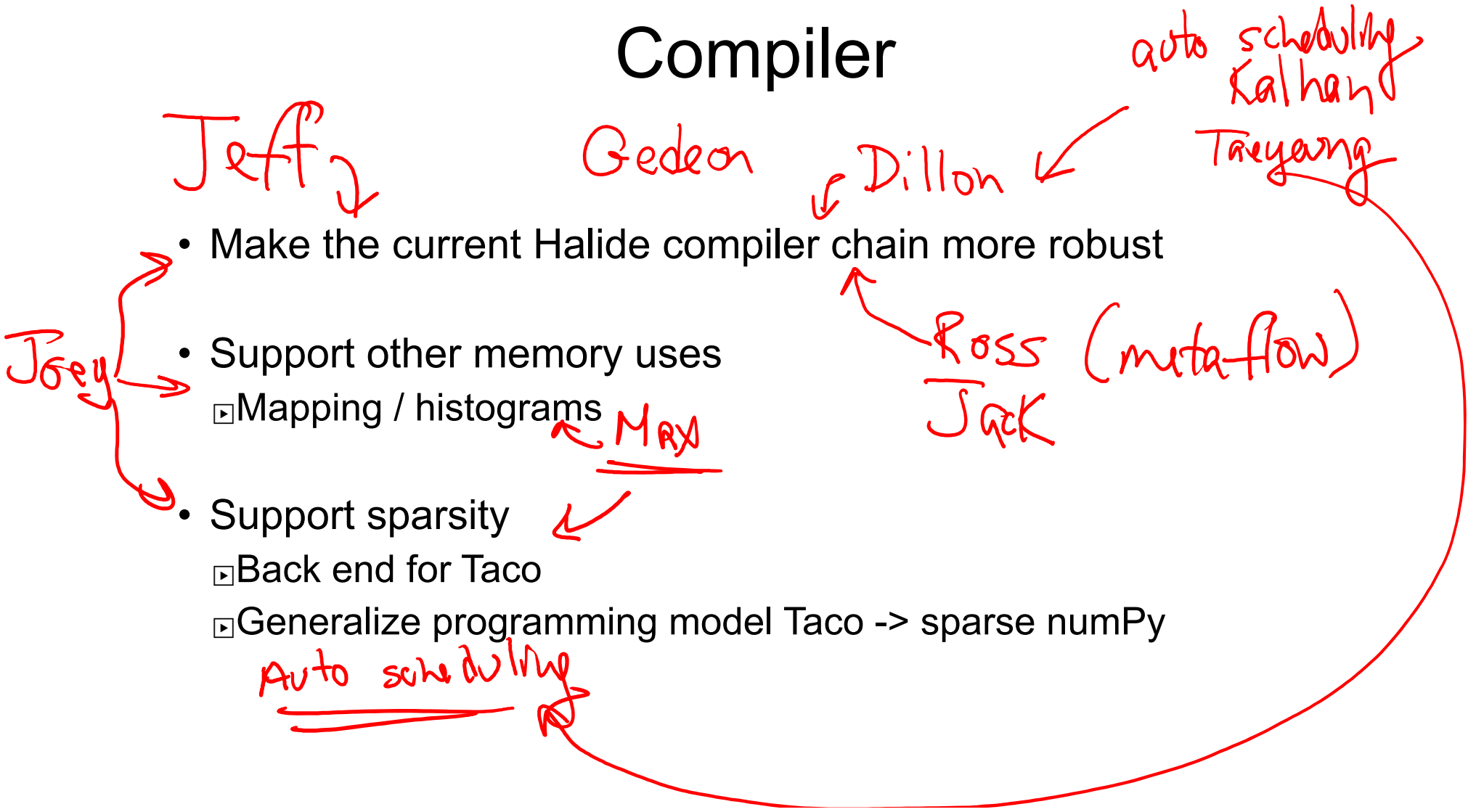
- Applications
- Compiler
- Validation
- Tools
- Hardware

Applications



Compiler

- Make the current Halide compiler chain more robust
- Support other memory uses
  - Mapping / histograms
- Support sparsity
  - Back end for Taco
  - Generalize programming model Taco -> sparse numPy



Validation

- Bring formal into AHA
- Pono
- Model checking engines
- Source level hardware debugging

Ross → Using SMT auto debugging

Tools

Chris, Alex, Caleb, Keyi

- Creating/using “symbol table information” from Magma
  - For test / debug, and physical design — Raj, Lenny, Ross
- DSE – more feature, more robust — Jack, Ross, Caleb
- CoreIR flow integration
- Lake — David, Kavya, Max, Taeyoung, Ankita, Joey

Ankita + Ross → CoreIR ⇔ MLIR

Ross → ROM

Hardware / Tools

- Improved:
  - mflowgen
  - Magma
- "Smart" components
  - Dealing with hardware generated at last moment
- Power modeling framework (energy dictionary)

Hardware

- Creating chip testing environment
- Virtualization
- Physical design aware hardware design
- Cypto hardware
- Extended unified buffer (sparsity)