



Compile Halide to CoreIR

- Examples from travis <https://travis-ci.org/StanfordAHA/CGRAFlow/builds/393575195>
- Halide_CoreIR https://github.com/jeffsetter/Halide_CoreIR.git
 - Halide => coreir_design_top
 - Halide + img_in => img_out_x86

```
1652: make -C Halide_CoreIR/apps/coreir_examples/onebit_bool/ clean design_top.json out.png
```

Generate the CGRA

- CGRAGenerator <https://github.com/StanfordAHA/CGRAGenerator.git>
 - Genesis2 => verilog

```
1904:
Here is what I built (it's supposed to look like an array of tiles).
... .. i02 i03 i04 i05 i06 i07 i08 i09 i0A i0B i0C i0D i0E i0F i10 i11 ... ..
... .. io16_12 ... .. ... .. ... .. ... .. ... .. ... ..
i13 io16_14 p15 p16 p17 m18 p19 p1A p1B m1C p1D p1E p1F m20 p21 p22 p23 m24 io16_25 i26
i27 ... p28 p29 p2A ... p2B p2C p2D ... p2E p2F p30 ... p31 p32 p33 ... ... i34
i35 ... p36 p37 p38 m39 p3A p3B p3C m3D p3E p3F p40 m41 p42 p43 p44 m45 ... i46
i47 ... p48 p49 p4A ... p4B p4C p4D ... p4E p4F p50 ... p51 p52 p53 ... i54
i55 ... p56 p57 p58 m59 p5A p5B p5C m5D p5E p5F p60 m61 p62 p63 p64 m65 ... i66
i67 ... p68 p69 p6A ... p6B p6C p6D ... p6E p6F p70 ... p71 p72 p73 ... i74
i75 ... p76 p77 p78 m79 p7A p7B p7C m7D p7E p7F p80 m81 p82 p83 p84 m85 ... i86
i87 ... p88 p89 p8A ... p8B p8C p8D ... p8E p8F p90 ... p91 p92 p93 ... i94
i95 ... p96 p97 p98 m99 p9A p9B p9C m9D p9E p9F pA0 mA1 pA2 pA3 pA4 mA5 ... iA6
iA7 ... pA8 pA9 pAA ... pAB pAC pAD ... pAE pAF pB0 ... pB1 pB2 pB3 ... iB4
iB5 ... pB6 pB7 pB8 mB9 pBA pBB pBC mBD pBE pBF pC0 mC1 pC2 pC3 pC4 mC5 ... iC6
iC7 ... pC8 pC9 pCA ... pCB pCC pCD ... pCE pCF pD0 ... pD1 pD2 pD3 ... iD4
iD5 ... pD6 pD7 pD8 mD9 pDA pDB pDC mDD pDE pDF pE0 mE1 pE2 pE3 pE4 mE5 ... iE6
iE7 ... pE8 pE9 pEA ... pEB pEC pED ... pEE pEF pF0 ... pF1 pF2 pF3 ... iF4
iF5 ... pF6 pF7 pF8 mF9 pFA pFB pFC mFD pFE pFF p100 m101 p102 p103 p104 m105 ... i106
I107 ... p108 p109 p10A ... p10B p10C p10D ... p10E p10F p110 ... p111 p112 p113 ... i114
... .. io16_115 .. ... .. ... .. ... .. ... .. ... ..
... .. i116 i117 i118 i119 i11A i11B i11C i11D i11E i11F i120 i121 i122 i123 i124 i125 ... ..
```

Map, Place and Route App Onto CGRA

- CGRAMapper <https://github.com/StanfordAHA/CGRAMapper.git>
 - coreir_design_top => coreir_mapped

```
1728: ./CGRAMapper/bin/mapper build/onebit_bool_design_top.json build/onebit_bool_mapped.json
```

- smt-pnr <https://github.com/cdonovick/smt-pnr.git>
 - coreir_mapped => bitstream (pointwise, conv{12, 21, 31, bw})

```
2420: smt-pnr/run_pnr.py  
      build/pointwise_mapped.json build/cgra_info_16x16.txt  
      --bitstream build/pointwise_pnr_bitstream ...
```

- OR serpent-pnr <https://github.com/StanfordAHA/CGRAGenerator.git>
 - coreir_mapped => bitstream (onebit_bool)

```
1764:  
json2dot.py < build/onebit_bool_mapped.json > build/onebit_bool_mapped.dot  
serpent.py   build/onebit_bool_mapped.dot -o build/onebit_bool.bsb  
bsbuilder.py < build/onebit_bool.bsb          > build/onebit_bool.bsa
```

Final Correctness Check x86 vs. CGRA

- Verilator testbench <https://github.com/StanfordAHA/TestBenchGenerator.git>
 - (img_in, bitstream, verilog) => img_out_CGRA

2276:

build/onebit_bool_halide_out.raw looks like this:

```
od -t u1 build/onebit_bool_halide_out.raw
```

0000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0000020	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0000040	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0000060	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0000100	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0000120	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0000140	1	1	1	1												

build/onebit_bool_CGRA_out1.raw looks like this:

```
od -t u1 build/onebit_bool_CGRA_out1.raw
```

0000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0000020	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0000040	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0000060	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0000100	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0000120	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0000140	1	1	1	1												

TEST RESULT onebit_bool PASSED