Introduction to UCIe™ (Universal Chiplet Interconnect Express™)

Building an open ecosystem of chiplets for on-package innovations

Presentation to Stanford AHA Agile Hardware Project
Nov 1st, 2023

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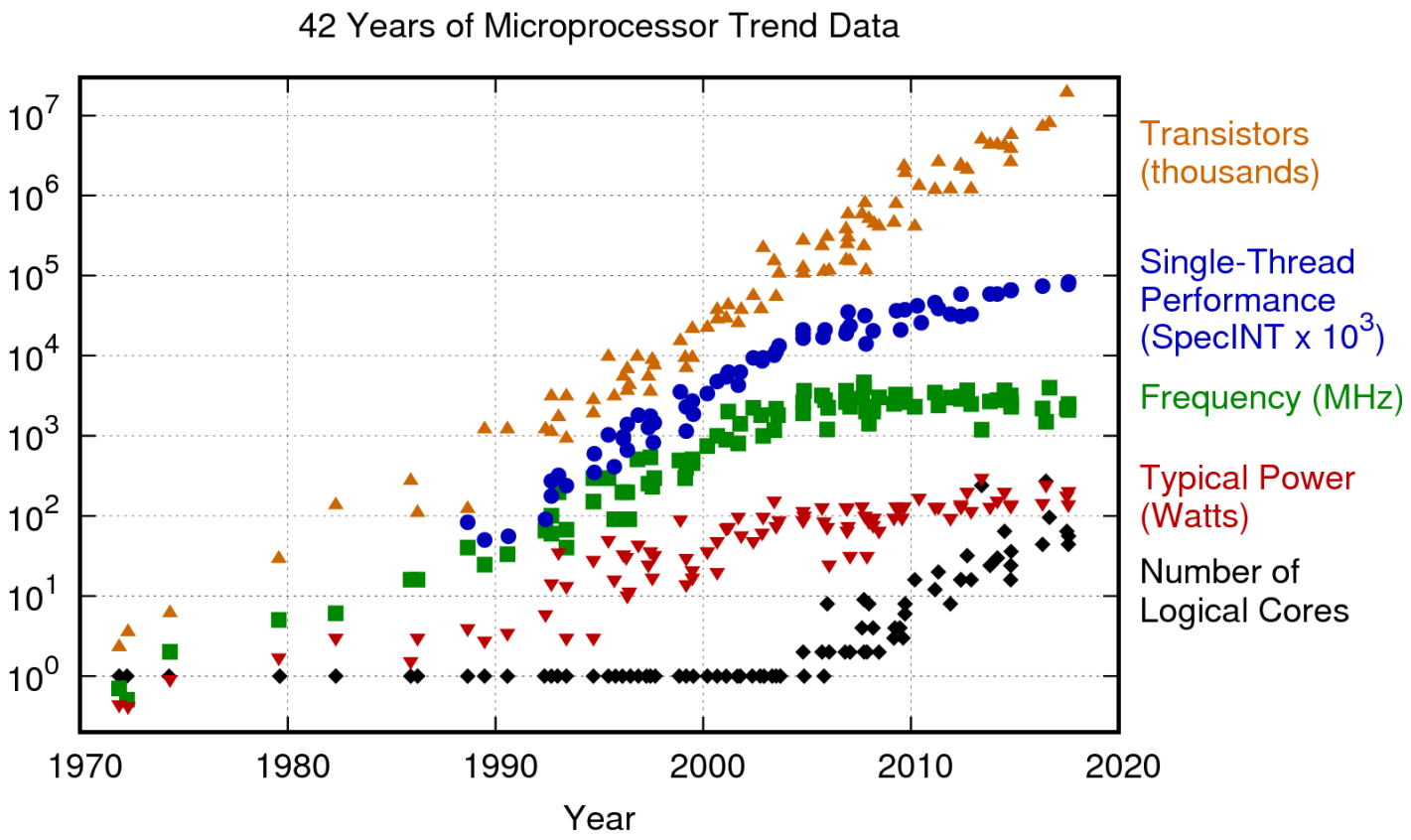
Moore's Law and "Day of Reckoning" Prediction



Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2017 by K. Rupp

Electronics, Vol 38, No 8, April 19, 1965

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

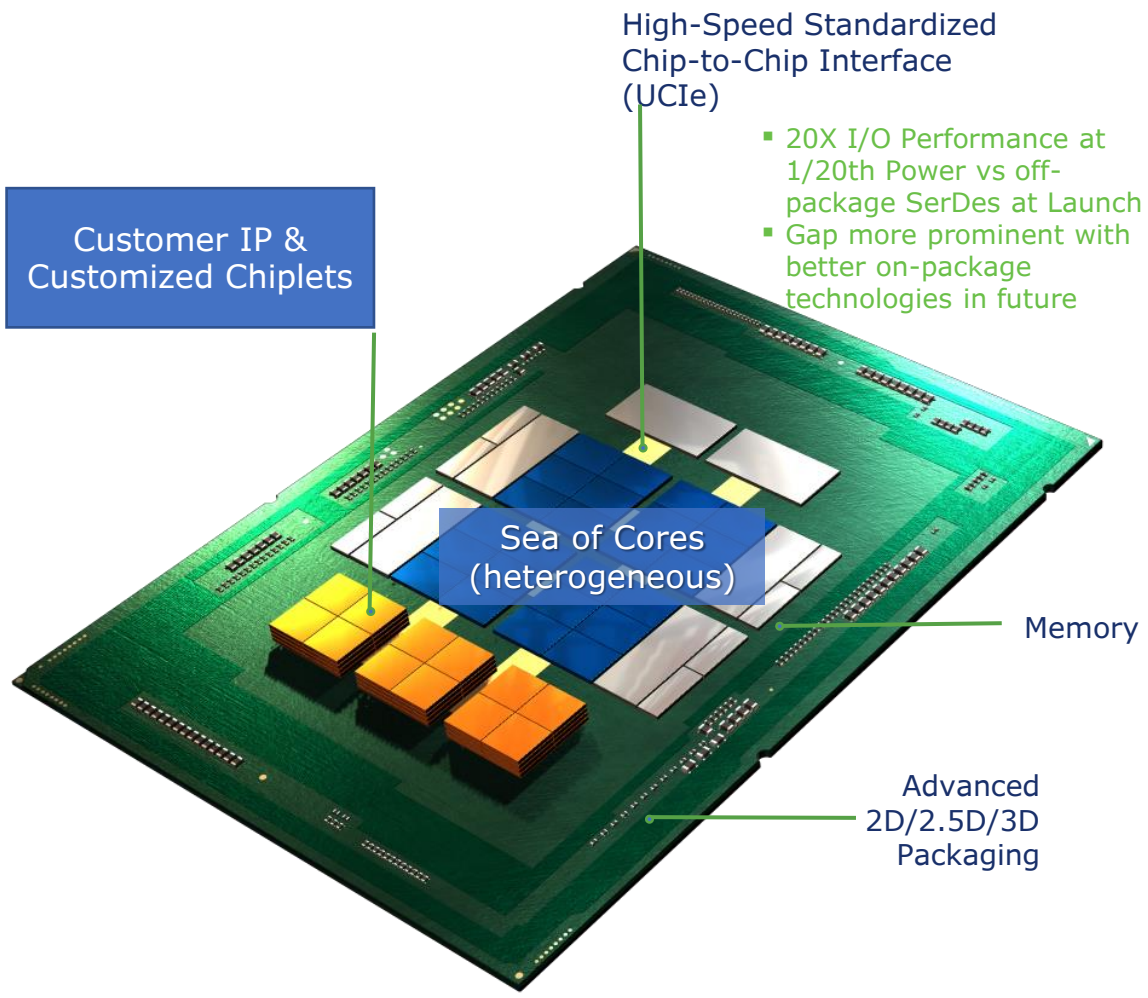
Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

Paper predicted "day of reckoning" :

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected"

Creation of UCIe

OPEN CHIPLET: PLATFORM ON A PACKAGE



On March 2nd 2022 leaders in semiconductors, packaging, IP suppliers, foundries and cloud service providers join forces to standardize chiplet ecosystem

UCIe
Universal Chiplet Interconnect Express

August 8, 2023 – Beaverton, OR – Today, the UCIe Consortium announced the public release of UCIe™ (Universal Chiplet Interconnect Express™) 1.1 Specification to deliver valuable improvements in the chiplet ecosystem, extending reliability mechanisms to more protocols and supporting broader usage models. Additional enhancements are included for automotive usages – such as predictive failure analysis and health monitoring – and enabling lower-cost packaging implementations. The specification also details architectural specification attributes to define system setups and registers that will be used in test plans and compliance testing to ensure device interoperability. The UCIe 1.1 Specification is fully backward compatible with the UCIe 1.0 Specification.

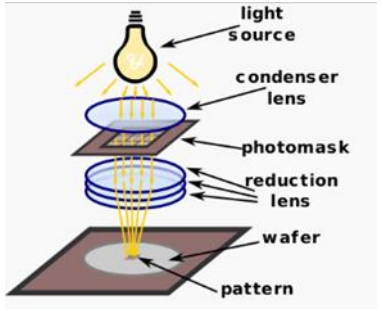
130+ Member Companies and growing!

Board Members

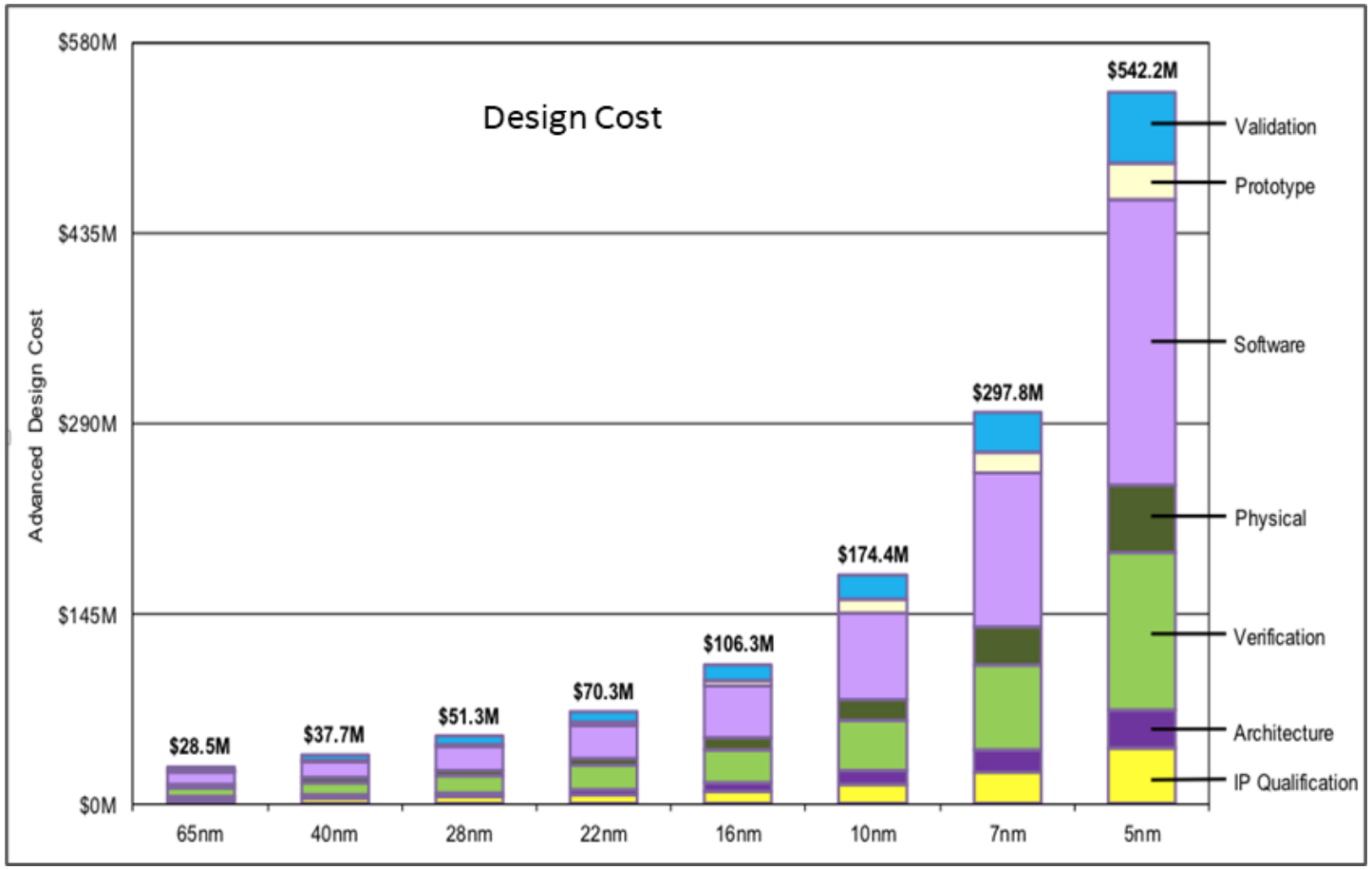
Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive
The open chiplet ecosystem.

JOIN US!

Drivers for On-Package Chiplets

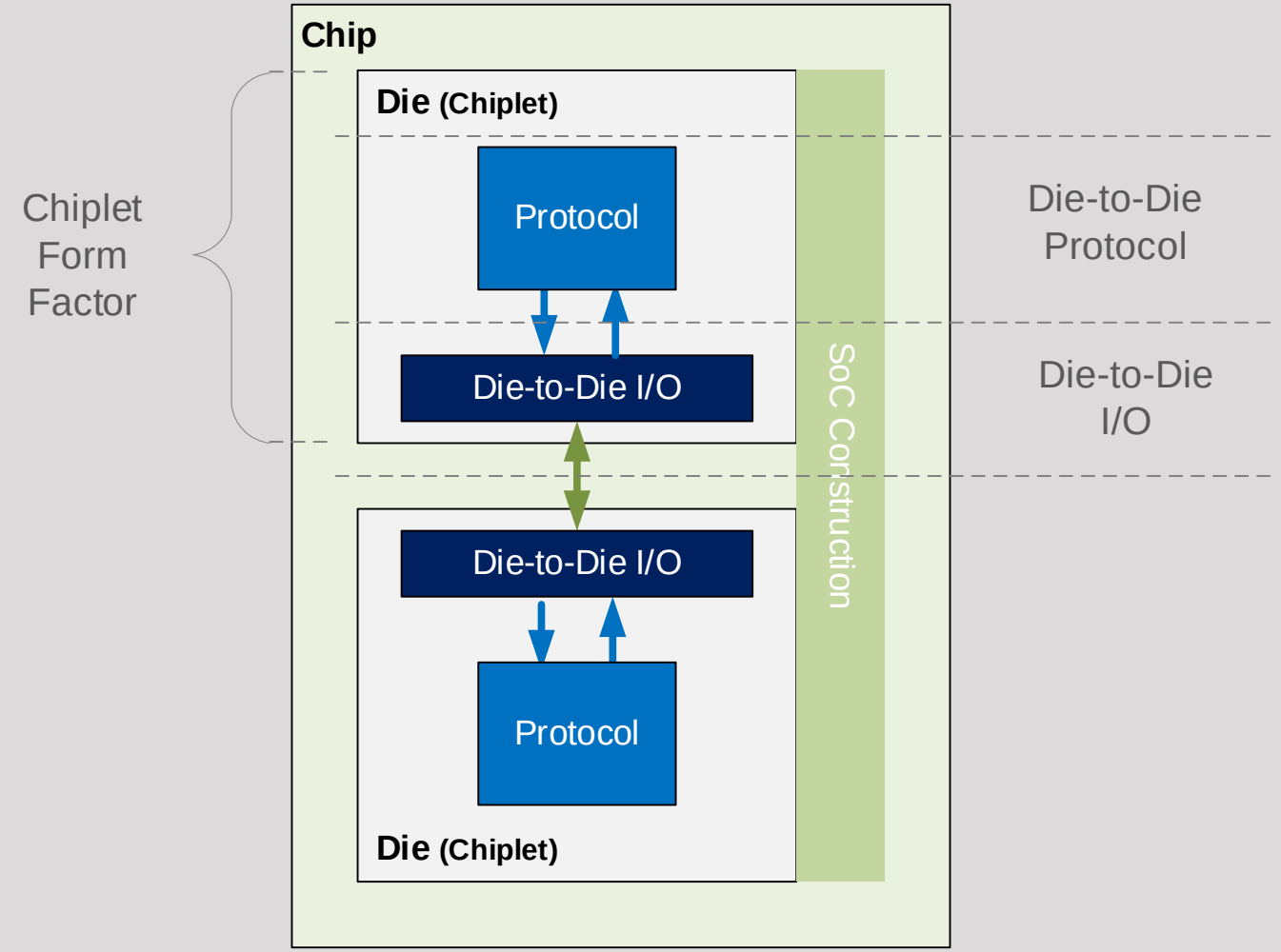


- Reticle Limit, yield optimization, scalable performance
  - → Same dies on package (Scale-up)
- Increasing design costs at leading edge process nodes
  - → Disaggregate dies across different nodes
  - → Deploy latest process node for advanced functionality
- Time to Market (Late binding)
- Easily enables Custom silicon for different customers leveraging a common base product
  - → E.g., Different acceleration functions with common compute
- Different process nodes optimized for different functions
  - → E.g., Memory, logic, analog, co-packaged optics
- Enables high, power-efficient bandwidth with low-latency access (e.g., HBM memory)



Source: IBS (as cited in IEEE Heterogeneous Integration Roadmap)

Components of Chiplet Interoperability

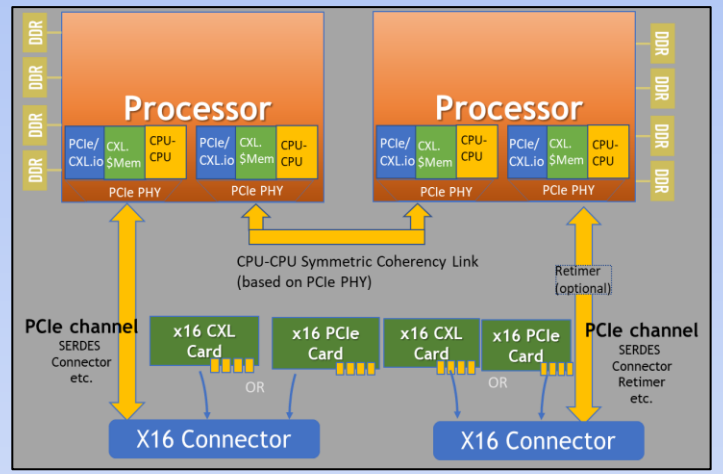


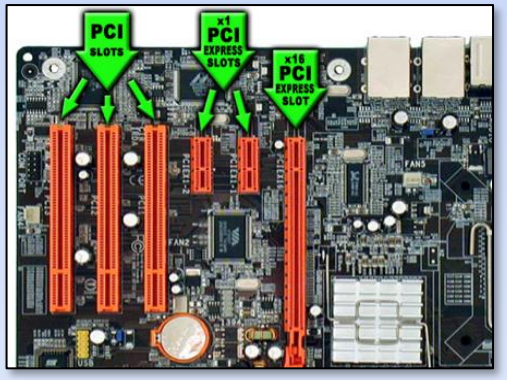
(Example SoC showing two chiplets only)

- **Chiplet Form Factor**
  - Die Size / bump location
  - Power delivery
- **SoC Construction** (Application Layer)
  - Reset and Initialization
  - Register access
  - Security
- **Die-to-Die Protocols** (Data Link to Transaction Layer)
  - PCIe/ CXL/ Streaming
  - Plug and play IPs
- **Die-to-Die I/O** (Physical Layer)
  - Electrical, bump arrangement, channel, reset, initialization, power, latency, test repair, technology transition

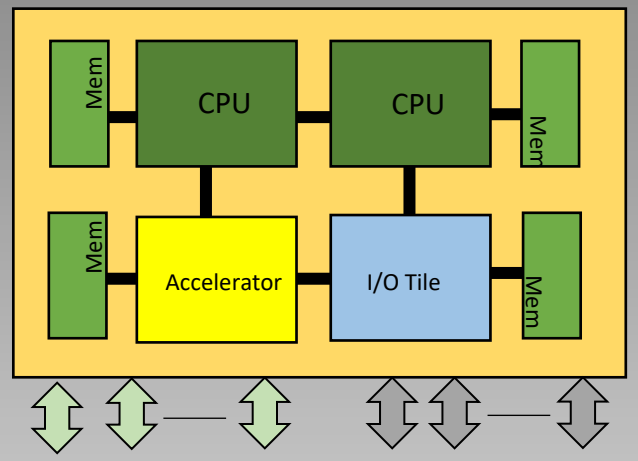
Design Choice: Seamless Integration from Node → Package → On-die

Enables Reuse, Better User Experience

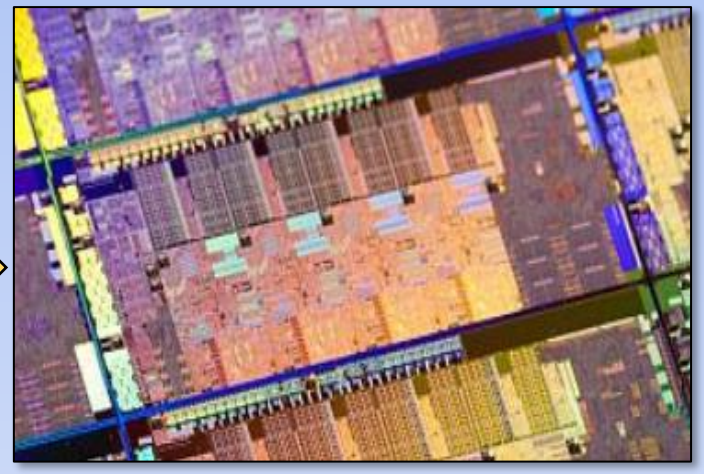




Node / Board Level Integration



Package Level Integration (with on-package interconnects)



On-die Integration

Same Software, IP, and Subsystem to build scalable solutions offers economies of scale , time to market advantage, and seamless user experience. Innovations at the open slot in board level needs to migrate to package level for multiple usages!

Key Metrics and Adoption Criteria

Key Technology Metrics

- Bandwidth density (linear & area)
  - Data Rate & Bump Pitch
- Energy Efficiency (pJ/b)
  - Scalable energy consumption
  - Low idle power (entry/exit time)
- Latency (end-to-end: Tx+Rx)
- Channel Reach
- Technology, frequency, & BER
- Reliability & Availability
- Cost (Standard vs advanced packaging)

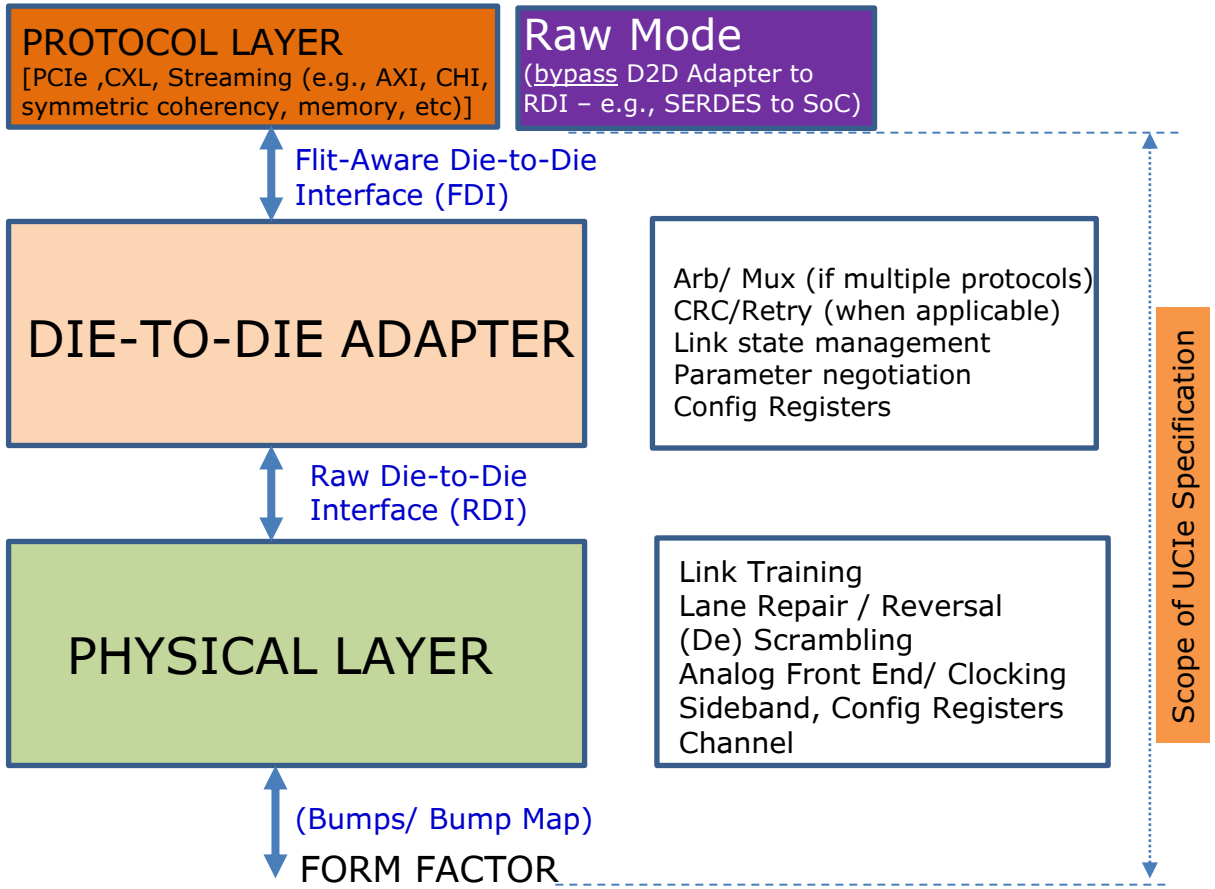
Factors Affecting Wide Adoption

- Interoperability
- Full-stack, plug-and-play with existing s/w is+
- Different usages/segments
- Technology
  - Across process nodes & packaging options
  - Power delivery & cooling
  - Repair strategy (failure/yield improvement)
  - Debug – controllability & observability
- Broad industry support / Open ecosystem
  - Learnings from other standards efforts

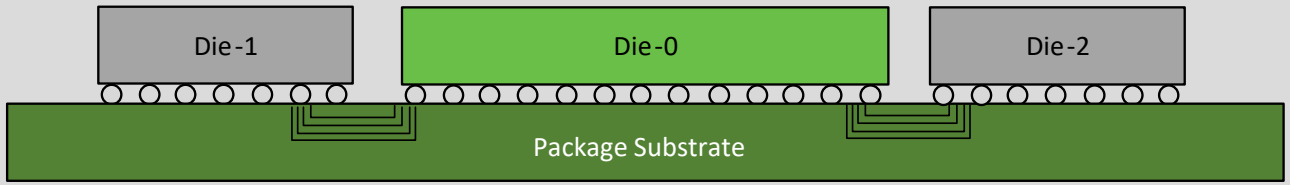
UCIe - Architected and specified from the ground-up to deliver the best KPIs while meeting wide adoption criteria to drive innovations at package level

UCIe 1.1 Specification

- **Layered Approach with industry-leading KPIs**
- **Physical Layer:** Die-to-Die I/O
- **Die to Die Adapter:** Reliable delivery
  - Support for multiple protocols: bypassed in raw mode
- **Protocol:** CXL/PCIe and Streaming
  - **CXL™/PCIe® for volume attach and plug-and-play**
    - SoC construction issues are addressed w/ CXL/PCIe
    - CXL/PCIe addresses common use cases
      - I/O attach, Memory, Accelerator
  - **Streaming for other protocols**
    - Scale-up (e.g., CPU/ GP-GPU/Switch from smaller dies)
    - Protocol can be anything (e.g., AXI/CHI/SFI/CPI/ etc)
- **Well defined specification**: interoperability and future evolution
  - Configuration register for discovery and run-time
    - control and status reporting in each layer
    - transparent to existing drivers
  - Form-factor and Management
  - Compliance for interoperability
  - Plug-and-play IPs with RDI/ FDI interface



UCIe 1.1: Supports Standard and Advanced Packages

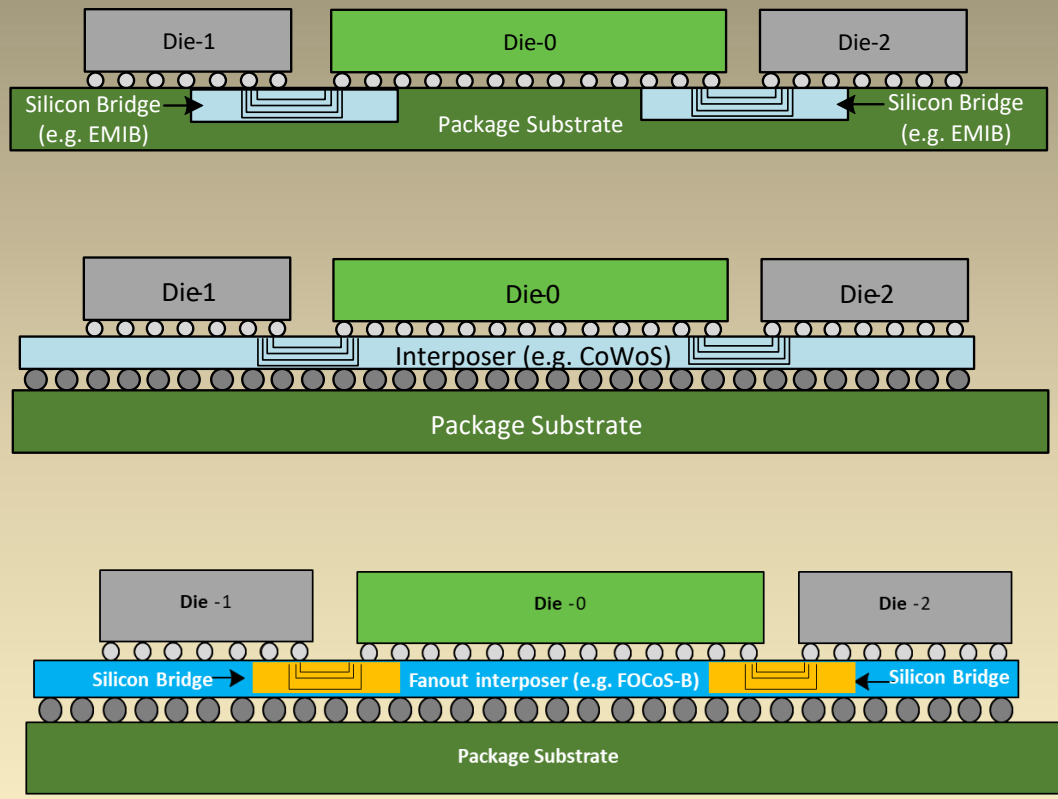


(Standard Package)

Standard Package: 2D – cost effective, longer distance

Advanced Package: 2.5D – power-efficient, high bandwidth density

Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package – Flexibility for SoC designer

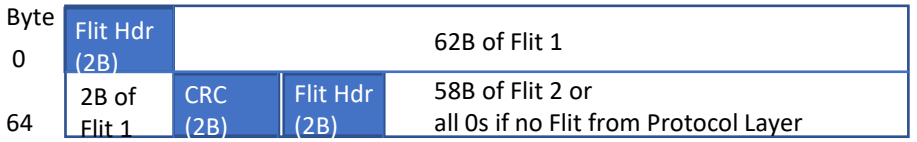


(Multiple Advanced Package Choices)

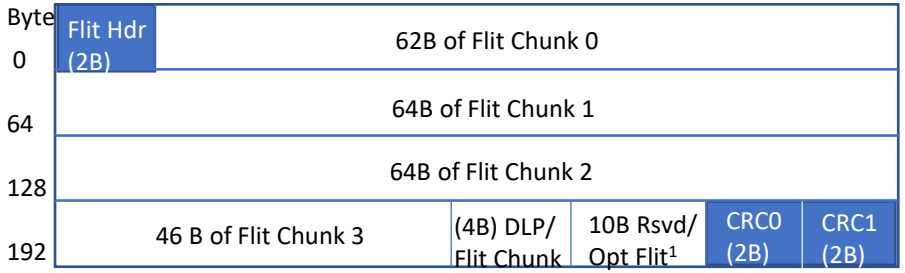
One UCIe 1.1 spec supports different flavors of packaging options to build an open ecosystem

D2D Adapter and Flit Mapping through FDI

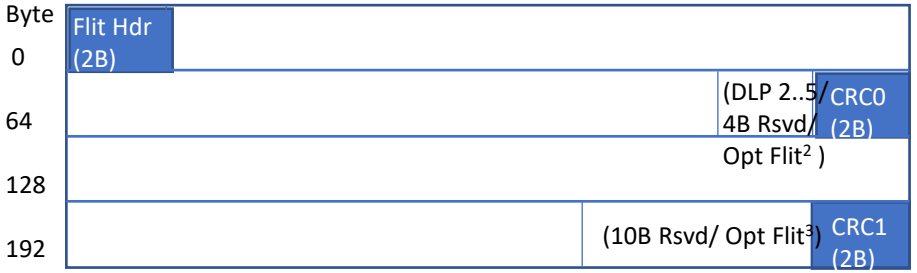
- Responsible for packetization
  - Adds Flit Header (2B) and CRC (2B)
- Supported Flit Sizes: 68B and two flavors of 256B
  - Decided at negotiation
- Flit Hdr (2B): Protocol ID (3b), Credit (1b), Flit Ack/Nak management (2b command + 8b sequence number), Rsvd (2b)
- CRC: Covers 128B payload (smaller payloads are 0-extended)
  - Triple bit flip detection guarantee with 16 bits
  - Replay if CRC fails
  - Sample RTL code for CRC provided in the spec



(a. 68-Byte Flit – usage CXL 2.0/ PCIe Non-Flit Mode/ Streaming)



(b. 256-Byte Flit – usage CXL 3.0/ PCIe 6.0)

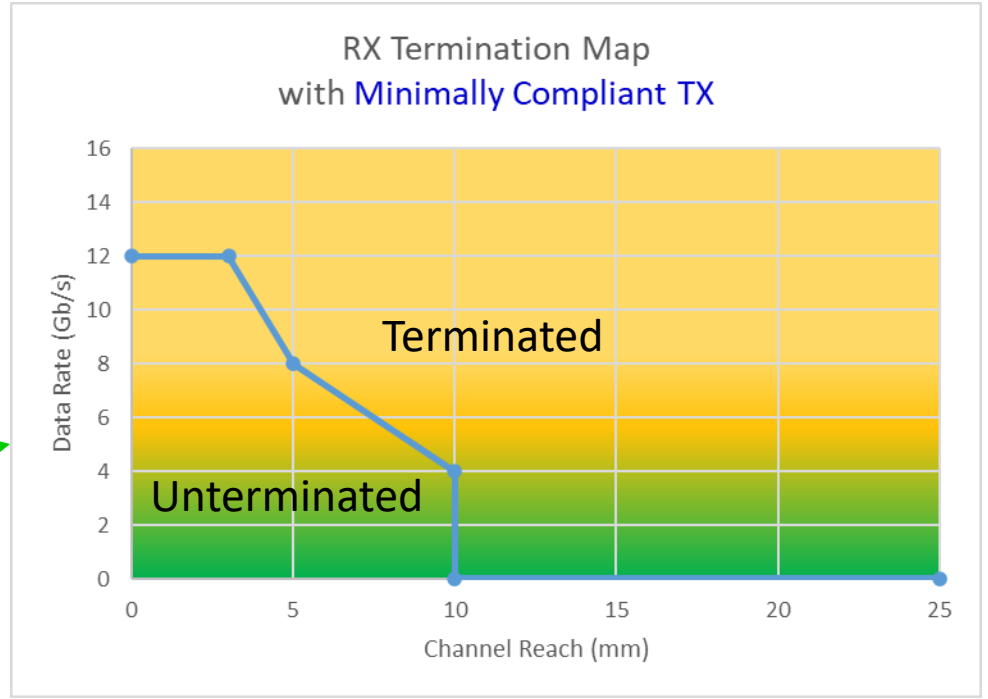


(c. 256-Byte Latency-Optimized Flit – usage CXL 3.0/ Streaming)

(Opt Flit is for better link efficiency to use the unused CRC/ FEC bytes in PCIe/ CXL)

Data Rate, BER, and Channel Reach

- Signaling: Unidirectional NRZ
- Data Rate: 4, 8, 12, 16, 24, 32 Gb/s.
- Channel Reach:
  - Advanced Package (25-55um bump pitch):
    - Up to 2mm and 32Gb/s, TX drive control.
    - No RX Termination
  - Standard Package (100-130um bump pitch):
    - TX Termination
    - RX Termination Map
- BER:



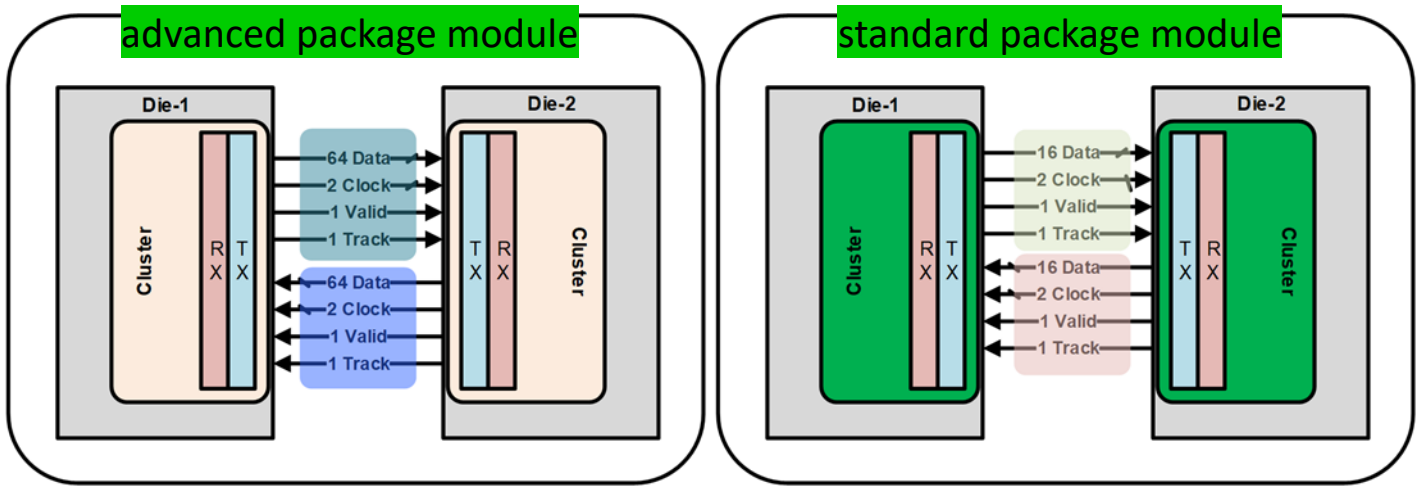
Reach for unterminated RX can be increased with higher swing TX

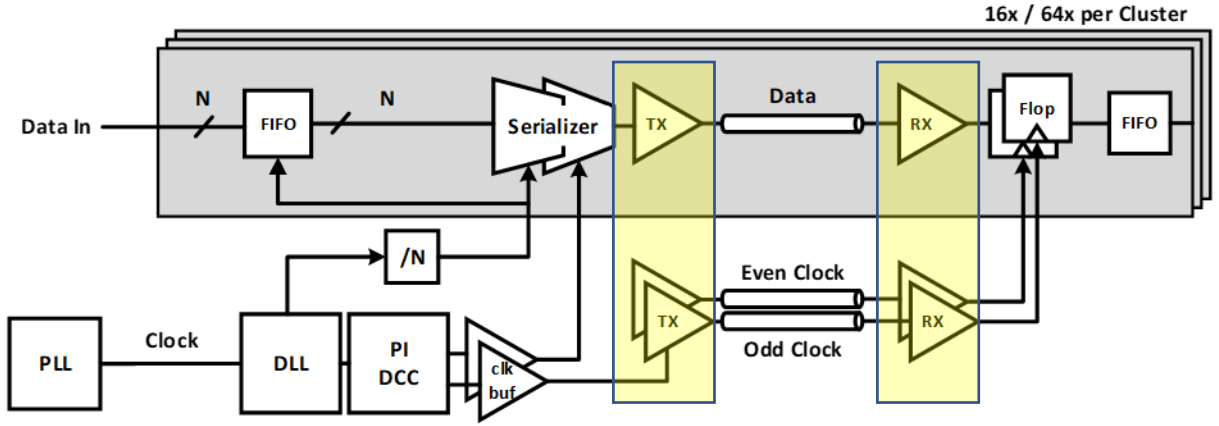
Data Rate (Gb/s)	4	8	12	16	24	32
Advanced Package	1.00E-27	1.00E-27	1.00E-27	1.00E-15	1.00E-15	1.00E-15
Standard Package	1.00E-27	1.00E-27	1.00E-15	1.00E-15	1.00E-15	1.00E-15

CRC and Retry for BER 1E-15 to achieve FIT rate <<1

PHY Architecture

- Basic module data width:
  - x64 for advanced packaging
  - x16 for standard packaging
- Differential Forwarded Clock, Single-Ended Data.
- "Matched" Architecture
  - Better tolerance to power supply noise
- Matched Interconnect Channels
  - Significant power reduction in clock recovery
- SSC allowed, 0 ppm TX to RX
  - Refclk: < 5ns transport delay difference ➔ < 1 cycle phase drift due to SSC

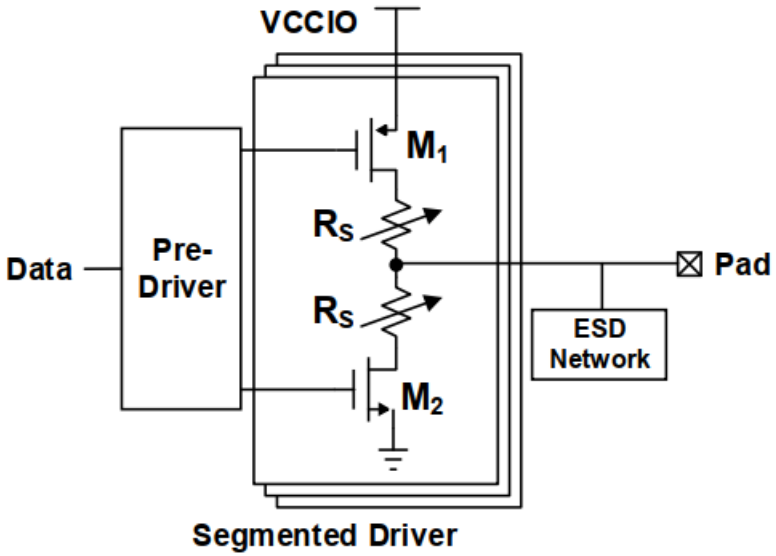




Driver and Input Buffer

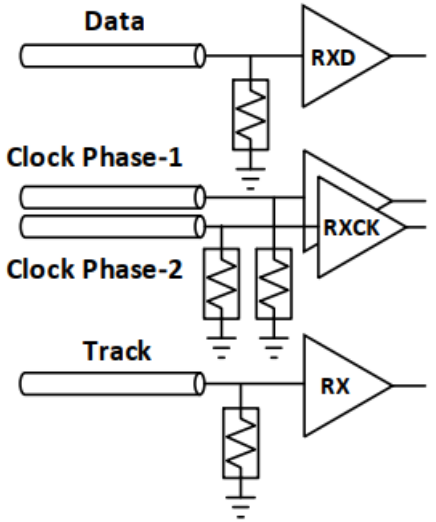
TX Driver

- Typical segmented driver
- CMOS implementation shown. NN driver and other structure possible.
- Target source impedance based on optimal eye open, not necessary matching T-Line impedance.
- BW and rise/fall time defined by Rterm and Cpad spec
- **TXLE** (1-tap de-emphasis) required at 24G+
  - Trained at link-initialization, no real time adaptation



RX Input Buffer

- Termination (when applicable) is to ground, and matching T-Line impedance.
- Spec does not mandate a specific input buffer design. If RX amplifier is used, recommend BW of > 0.75x data rate (1.5x Nyquist).
- Optional RX CTLE



TX and RX Voltage Compatibility

- Minimum TX swing 0.4V
- Strongly recommend max TX voltage < 0.85V for compatibility with future process nodes

Transmitter V_{OH} and Receiver VCC compatibility guidelines				
Die 1 TX output maximum V_{OH} (V)	V_{OH}	V_{OH}	V_{OH}	V_{OH}
Die 2 RX AFE VCC level (V)	V_{OH} - VCC < 0mV	V_{OH} - VCC = 0mV	V_{OH} - VCC < 100mV	V_{OH} - VCC > 100mV
Compatibility	Safe	Safe	Safe	Not Safe*

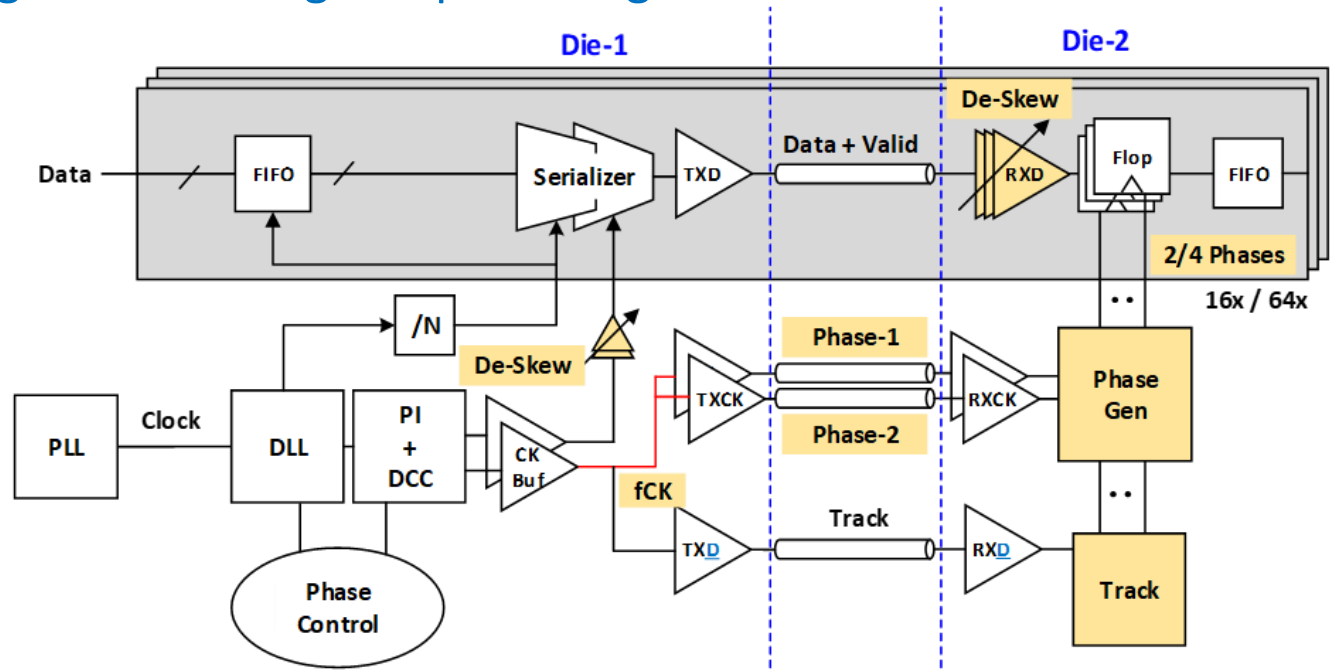
- Cross Process Reliability and Electrical Overstress (EOS) concerns
  - To avoid reliability issues (voltage overstress above allowable process limits: EOS), recommend limiting the TX output high (V_{OH}) to a maximum of 100mV above the RX supply rail.
  - When the TX V_{OH} is equal to or lower than the RX AFE supply rail, within ranges in the spec, there won't be reliability concerns.

- In the case of "Not Safe*", RX AFE overstress protection circuitry can be used to mitigate the issue, at cost of area and power consumption.

PHY Clocking Architecture

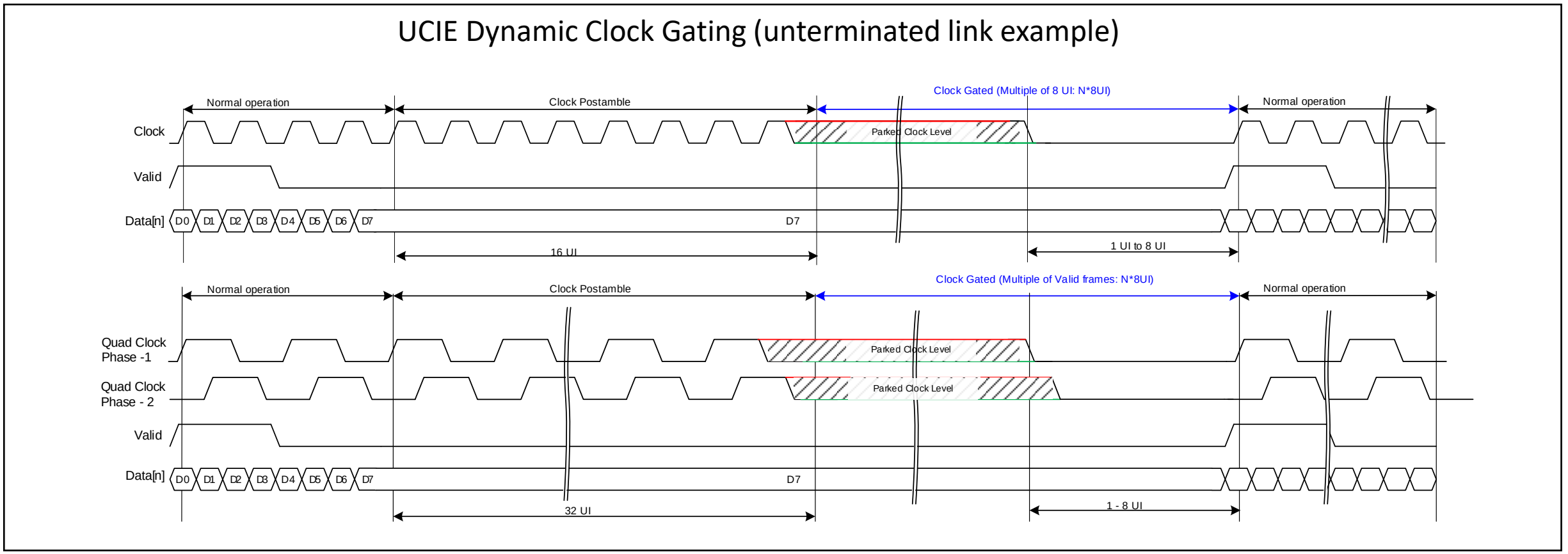
- Supports 2-way and 4-way interleaving TRX
- Independent even/odd phase control
- Global TX, local TX, local RX phase adjustments depending on data rate.
- Data Valid bit to gate clock distribution (also for data framing)
- Track bit for background training and phase alignment

Data rate (GT/s)	Clock freq. (fCK) (GHz)	Phase -1	Phase-2	De-skew (Req/Opt)
32	16	90	270	Required
	8	45	135	Required
24	12	90	270	Required
	6	45	135	Required
16	8	90	270	Required
12	6	90	270	Required
8	4	90	270	Optional
4	2	90	270	Optional



Dynamic Clock Gating

- Clock gated if Valid remains low after providing postamble
  - No clock gating if free running clock mode is negotiated
- Clock parked Hi/Low during alternate clock gating events; 8 UI boundary

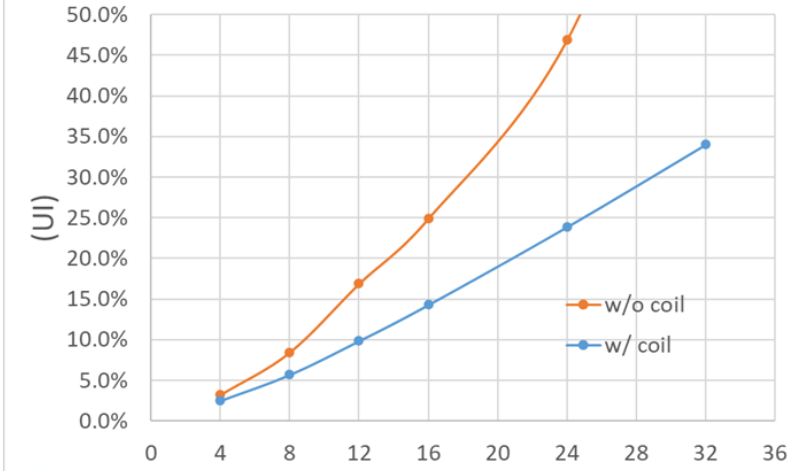


Pad Capacitance and ESD

- Cpad has 1st order performance impact
- Aggressive targets on Cpad and ESD
- UCIe 1.1 ESD spec: **30V CDM,** further scaling in future, align with Industry Council on ESD Targets**.**
- **T-coil** to reduce effective pad capacitance
  - T-coil widely used by serial I/O across industry
  - T-coil size expected to be on the order of 20um x 20um x2

TX/RX Pad Capacitance	250/200	fF	Advanced Package Mode
TX/RX Pad Capacitance (8Gb/s capable design)	300	fF	Standard Package Mode
TX/RX Pad Capacitance (16Gb/s capable design)	200	fF	Standard Package Mode Effective Cpad
TX/RX Pad Capacitance (32Gb/s capable design)	125	fF	Standard Package Mode Effective Cpad

T-coil impact to standard package channel



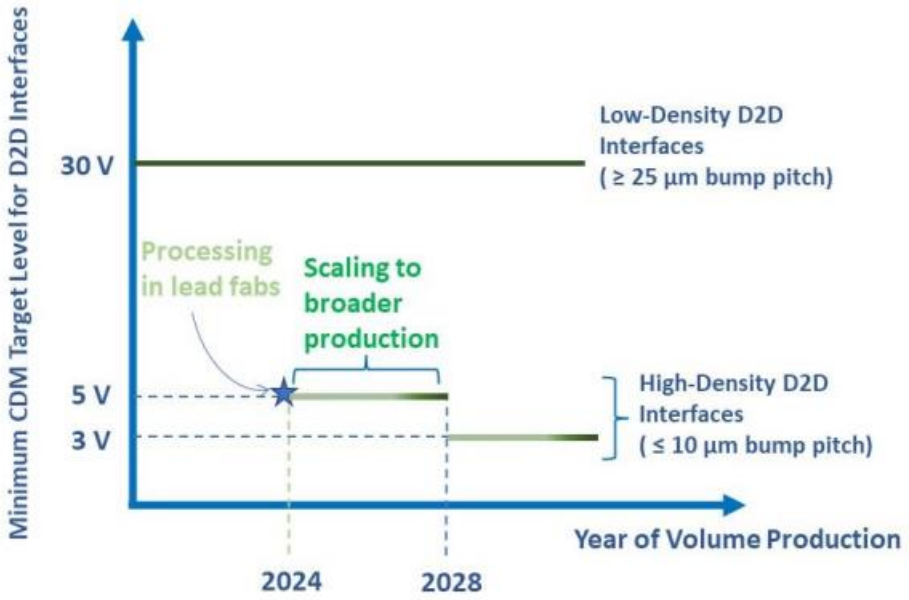
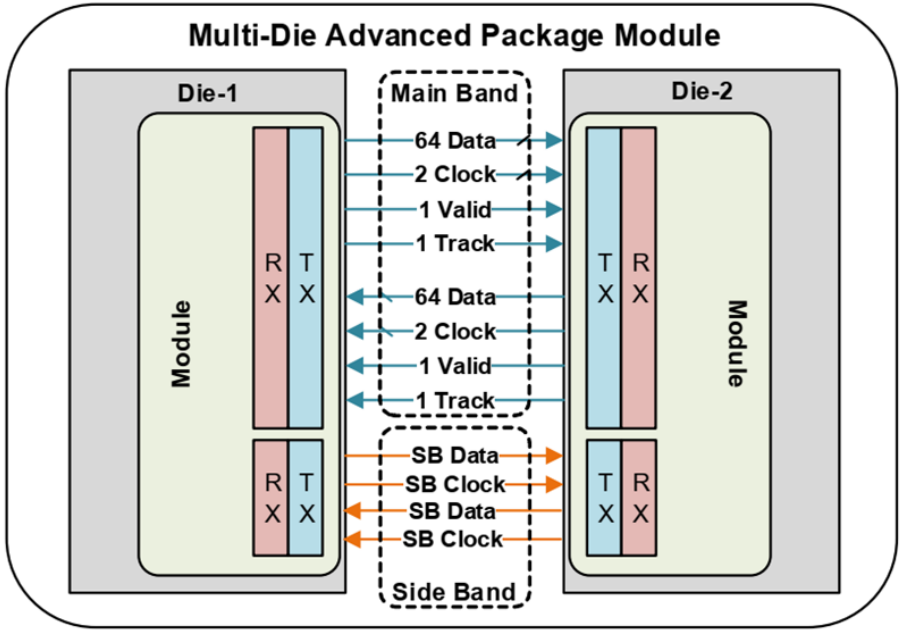


Figure 1: Roadmap of CDM Targets of Die-to-Die Interfaces

Source: White Paper (Aug 2023) from the Industry Council on ESD

Additional PHY Features

- 800MT/s 2-wire sideband per module
- Global signals (DFX etc.)
- Low Datapath Latency: 12 UI up to 16Gb/s, 16 UI 24-32Gb/s.
- Ultra Fast Idle Exit (L0-idle) through Data Valid Clock gating
- Valid Framing and Re-timer support, Hamming distance 4 encoding to improve reliability.
- L1 power state (options for further power down)
- Redundancy & Repair for Advanced Package
  - Two per 32 bits
- Data Scrambling to mitigate power supply noise
  - Does not require extra pin as DBI would



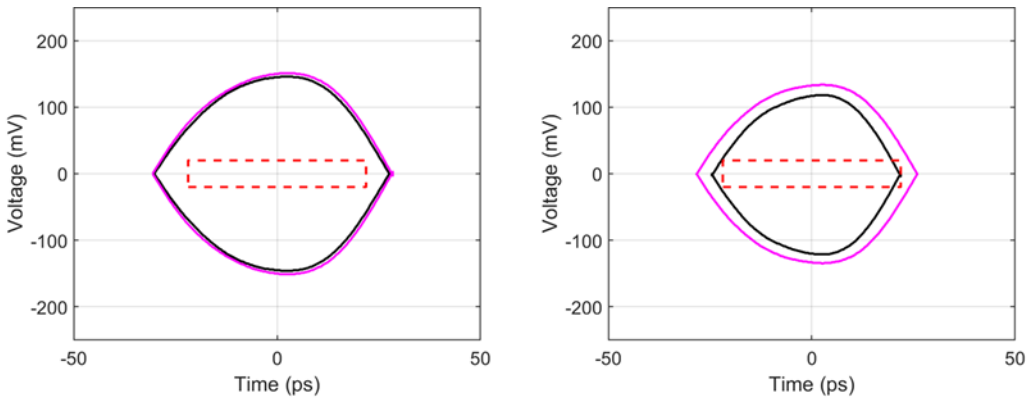
Sideband used for training, debug, management…
Figure is logical illustration
Physically sideband leverages depopulated bumps
No impact to shoreline / die edge BW density

Channel Specification

- Channel needs to meet minimum eye mask under channel compliance simulation with noiseless jitter-less behavioral TX and RX models

Data Rate	4-16Gb/s	24-32Gb/s
Overall (Eye Closure due to Channel)		
Eye Height	40mV	40mV
Eye Width (rectangular eye mask with specified eye height)	0.75 UI	0.65 UI with Equalization Enabled

Pass/fail eye mask example



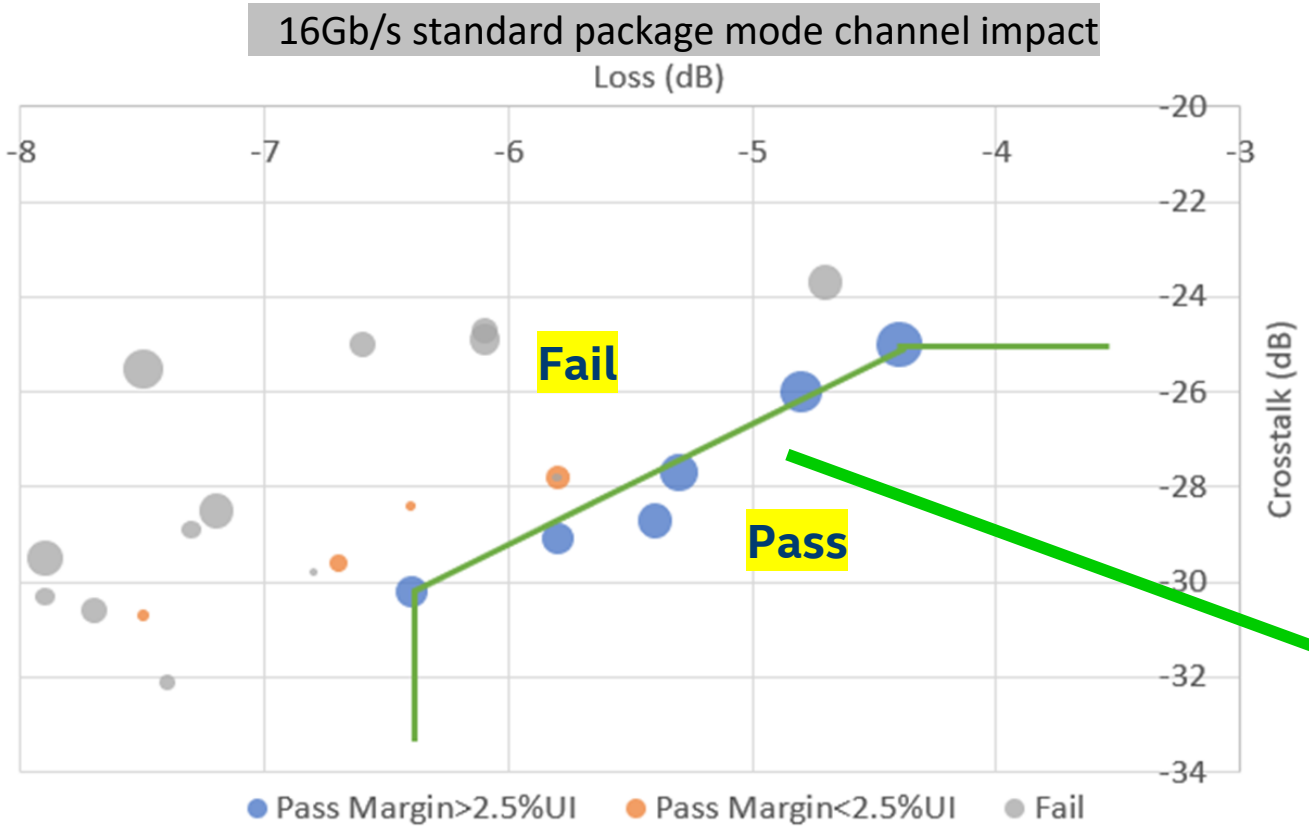
Insertion loss and Crosstalk spec defined based on the criteria using Voltage Transfer Function (VTF) method

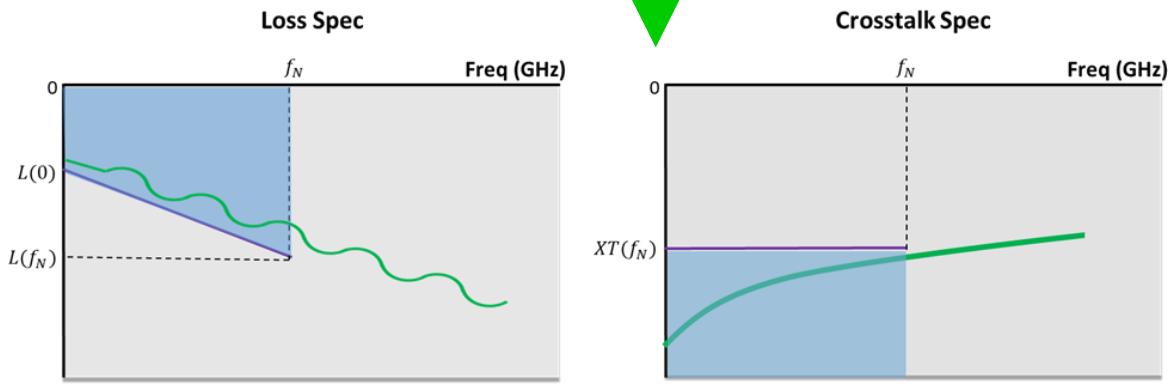
  - Due to short transmission line, VTF is more practical than S-parameter based method.

Specify Insertion Loss, Crosstalk & Tradeoff

Example of 16Gb/s standard package shown: 2D map of L(8) and XT(8) pass/fail region

- Linear and flat mask for Loss and Crosstalk respectively, not a single frequency spec.



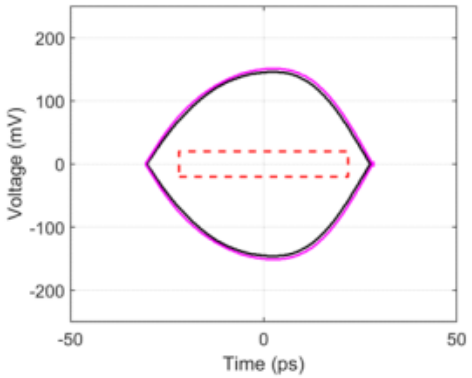


- f_N is the Nyquist frequency in GHz
- Loss from DC to f_N needs to be above the spec line
- Crosstalk from DC to f_N needs to be below the spec line

$L(0) > -4.5$ $L(f_N) > -6.5$
$XT(f_N) < 3 * L(f_N) - 11.5$ and $XT(f_N) < -25$

Tightly Coupled Mode

- Both Conditions must be met:
  - Shared Power Supply or Forwarded Power Supply
  - Channel supports larger eye mask
- Rationale / Advantages:
  - Further Optimization of PHY Circuits to lower power. For example, inverter-based RX, no front amplifier.
  - Reduced Training Complexity, such RX reference voltage training.
  - Preparation for higher density D2D



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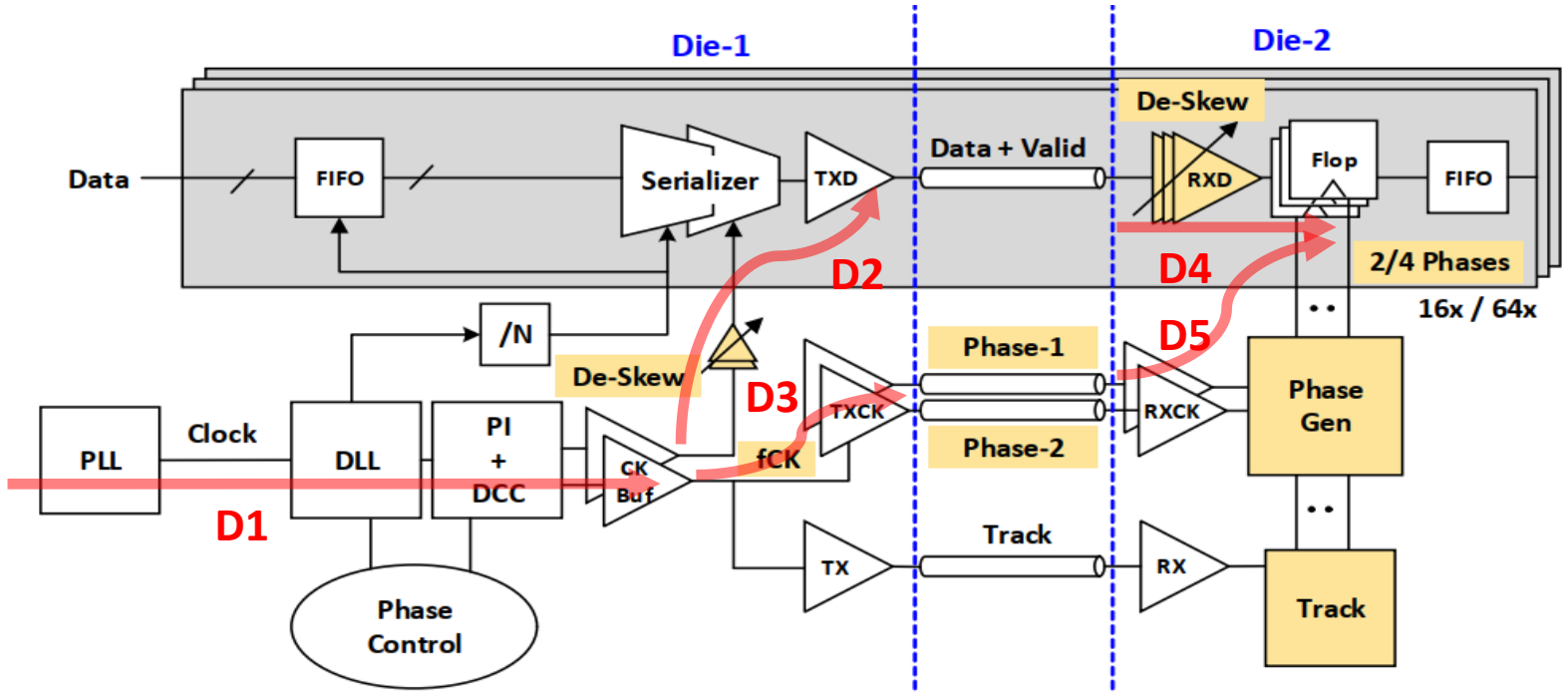
Eye mask for channel changes to

250mV / 0.7UI for TX swing 0.75V

Up to 16Gb/s

TX and RX Jitters

Specify 1-UI TX jitter, data/clock differential TX jitter, and data/clock differential RX jitter.



D1: Tx Common clock delay
D2: Tx Data path clock delay
D3: Tx FWD clock path delay
D4: Rx Data path delay
D5: Rx Clock path delay

E(D3) = E(D2) + nT, E is the mean, n = 0.5 for matched arch

Jitter = D1(t-nT) – D1(t) + D3(t-nT) – D2(t) – nT + D5(t) – D4(t)

➔ Jitter = $D(t-nT) - D(t) + \delta D_T(t) - nT + \delta D_R(t)$

where $D = D1+D3$ (total delay), $\delta D_T = D3-D2$, $\delta D_R(t) = D5-D4$

Link Timing Analysis

Timing parameters

	Name	Note
Eye Closure due to Channel	Ch	from SI analysis
Channel Mismatch	Chm	
n-UI TX Total Jitter	Tjnui	specified at BER
TX Data/Clock Differential Jitter	Tjtx	specified at BER
TX Duty Cycle Error	Dce	post correction
TX Lane-to-lane Skew Correction Range	Rstx	
TX Lane-to-Lane Skew	Stx	post correction
Clock to Mean Data Training Accuracy	Eckd	including static and tracking error
RX Data/Clock Differential Jitter	Tjrx	specified at BER
Max RX Lane-to-Lane Skew	Msrx	if exceeding limit, requires RX lane-to-lane deskew
RX Phase Error	Eph	including duty cycle and I/Q mismatch
Sampling Aperture	Ap	

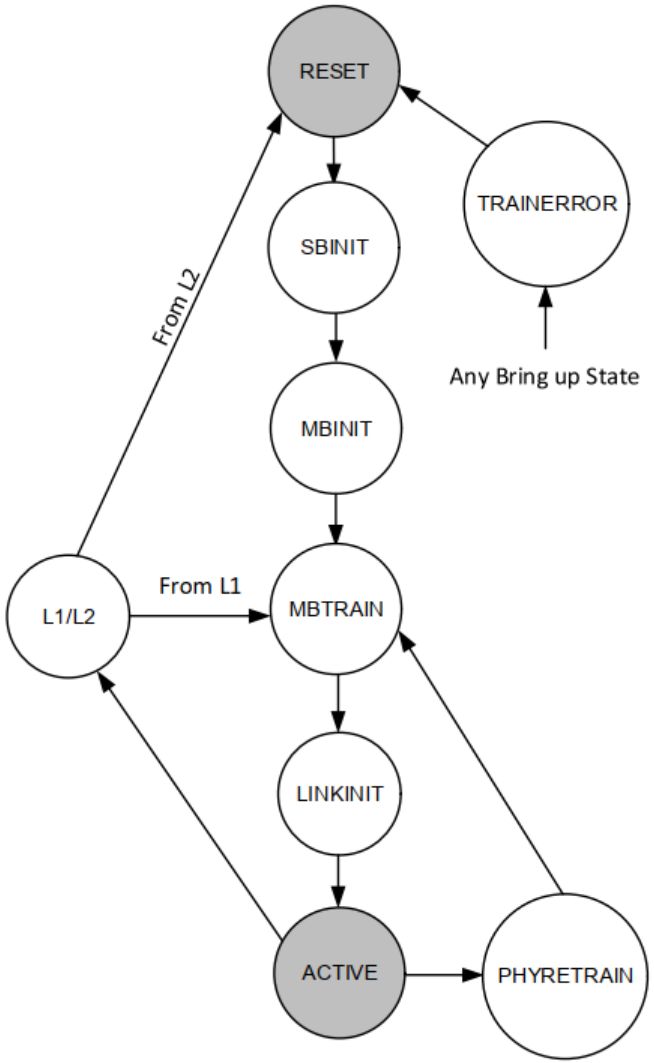
- Need to meet the following conditions (range defined as peak-to-peak)

$$C_h + T_{jnui} + D_{ce} + S_{tx} + E_{ckd} + T_{jrx} + E_{ph} + A_p \leq 1\text{UI}$$

$$C_{hm} \leq R_{stx} - M_{srx}$$

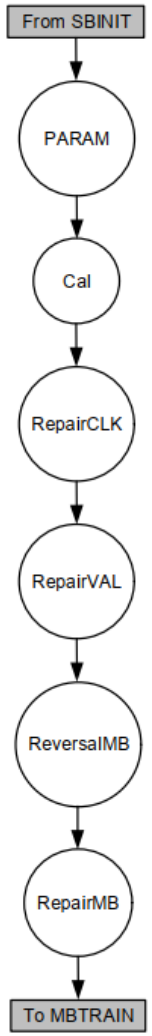
- Detailed numbers at different data rates are in the spec and WG discussions

Link Training and Status State Machine



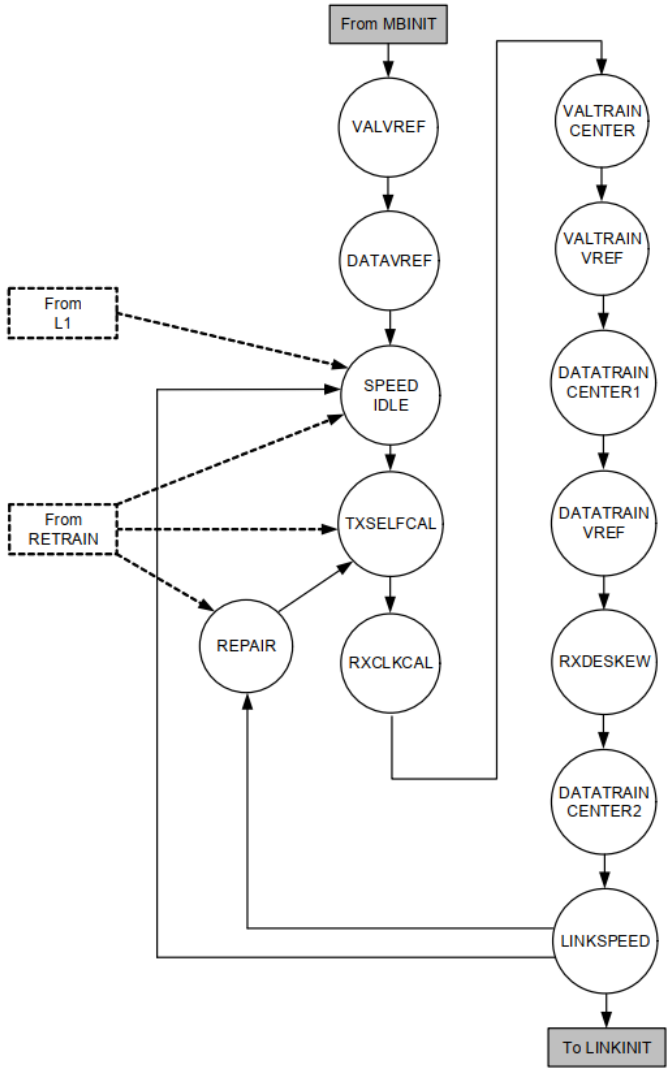
- Sideband (SB) initialization
  - Initialization and repair (advanced interface) of SB
- Main band (MB) initialization
  - Parameter exchange, CLK, Valid & MB repair & MB reversal
- Main band training
  - Data training, at speed repair/degrade and speed degrade
- Link init
  - Exchange RDI Link management messages
- PHYRETRAIN: Retrain based on Link errors
  - Allow infield repair and degrade
- L1/L2: Lower power state
- Train error: For uncorrectable internal errors and Link down conditions //state timeouts and SB timeouts
- Active: Transactions are sent and received

Main band Initialization



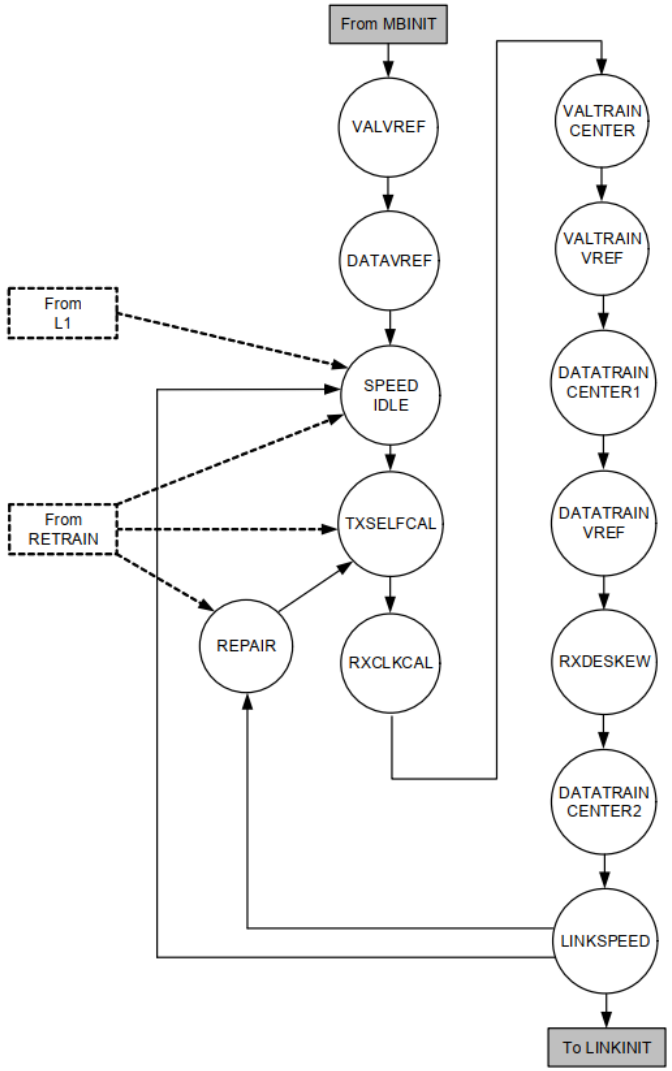
- Data rate set to 4GT/s for main band
- Param
  - Exchange of parameters required to setup maximum speed and other PHY settings
- Cal
  - Perform any required calibration (ex: Tx Duty Cycle, Rx Vref etc.)
- RepairCLK
  - Detect and apply repair (if needed) to clock and track Lanes for Advanced Pkg
  - Functional check of clock and track Lanes for Standard Pkg
- RepairVAL
  - Detect and apply repair (if needed) to Valid Lane for Advanced Pkg
  - Functional check of Valid for Standard Package interface.
- ReversalMB
  - Detect and apply Lane reversal (both Standard and Advanced package)
- RepairMB
  - Detect and apply repair (if needed) for Advanced Pkg interface
  - Functional check and width degrade (if needed) for Standard Pkg interface.

Main band Training



- VALVREF
  - Receiver reference voltage (Vref) to sample the incoming Valid
  - Performed through Rx initiated point tests or sweep using Valtrain pattern
- DataVref
  - Receiver reference voltage (Vref) to sample the incoming Data
  - Performed through Rx initiated point tests or sweep using LFSR pattern
- Speed Idle
  - Frequency changed to highest negotiated Data rate
- TxSelfCal
  - UCIe Module calibrates its circuit parameters independent of the UCIe Module Partner
- RxClkCal
  - Perform calibration on Clock receive path and align Clock/Track alignment
- ValTrainCenter
  - Valid to clock centering and ensure Valid functionality

Main band Training [2]



- ValTrainVref
  - Optional operation within the state to allow at speed Vref training on Valid signal
- DataCenter1
  - Full Data to clock training with correct Valid framing
  - Tx initiated point tests or eye width sweep with LFSR pattern
- DataTrainVref
  - Optional operation within the state to allow at speed Vref training on Data
- RxDeSkew
  - Optional Operation within the state to allow Lane-to-Lane skew correction on Rx if needed
- DataCenter2
  - Recentering if Rx performs Deskew
- LinkSpeed
  - Link stability check; direct Link to repair or speed degrade if needed
- Repair
  - Apply repair for Advanced pkg and Width degrade for Standard pkg

Electrical Summary

	Standard Package	Standard Package	Standard Package	Standard Package	Advanced Package	Advanced Package	Advanced Package
Data Width	16	16	16	16	64	64	64
Data Rate (Gb/s)	4-16	4/8/12	16	24/32	4/8/12	16	24/32
Power Efficiency Target (pJ/b)	0.25-0.5	0.5-1	0.5-1	0.75-1.25	0.25-0.5	0.3-0.6	0.3-0.6
Latency Target (TX+RX) (UI)	12	12	12	16	12	12	16
Idle Power (% of peak)	15%	15%	15%	15%	15%	15%	15%
Channel Reach (mm)	2-10	25	25	25	2	2	2
Die Edge BW Density (GByte/s/mm)	28-112	28-84	112	168/224	165-494	658	988/1317
BW Area Density (GByte/s/mm²)	21-85	21/42/64	85	109/145	158/316/473	631	710/947
PHY dimension Width (um)	571.5	571.5	571.5	571.5	388.8	388.8	388.8
PHY dimension Depth (um)	1320	1320	1320	1540	1043	1043	
ESD	**30V CDM (Further scaling in future, align with Industry Council on ESD Targets)**						

Conservative estimate, 800/1000+ GB/s/mm^2 latest proposal, PHY depth ~1200 um

Advanced package PHY depth depends on bump pitch, number based on 45um

UCIe-S: Standard Package Bump Maps

- Two options: x16 and x32 bump arrangements for BW/mm flexibility
  - 4-2-4 recommended package stack-up for x16 (two topside stripline routing layers)
  - 8-2-8 recommended package stack-up for x32 (4 topside stripline routing layers) for doubled BW/mm

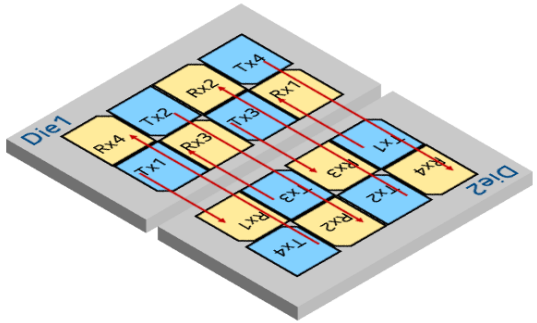
x16 module

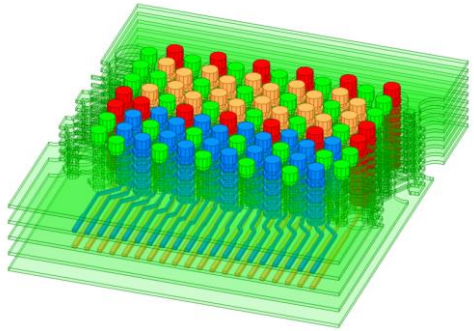
Column 0	Column 1	Column 2	Column 3	Column 4	Column 5	Column 6	Column 7	Column 8	Column 9	Column 10	Column 11
	txdatasb		txcksb		vccaon		vccaon		rxcksb		rxdatasb
vccio		vccio		vccio		vccio		vccio		vccio	
	vss		vss		vss		vss		vss		vss
vccio		txdata7		txdata9		vccio		rxdata8		rxdata6	
	txdata5		txckn		txdata11		rxdata10		rxckp		rxdata4
vss		vss		vss		vss		vss		vss	
	txdata4		txckp		txdata10		rxdata11		rxckn		rxdata5
vss		txdata6		txdata8		vss		rxdata9		rxdata7	
	vss		vss		vss		vss		vss		vss
vccio		txdata3		txdata13		vccio		rxdata12		rxdata2	
	txdata1		txvld		txdata15		rxdata14		rxtrk		rxdata0
vccio		vss		vss		vccio		vss		vss	
	txdata0		txtrk		txdata14		rxdata15		rxvld		rxdata1
vss		txdata2		txdata12		vss		rxdata13		rxdata3	
Die Edge											

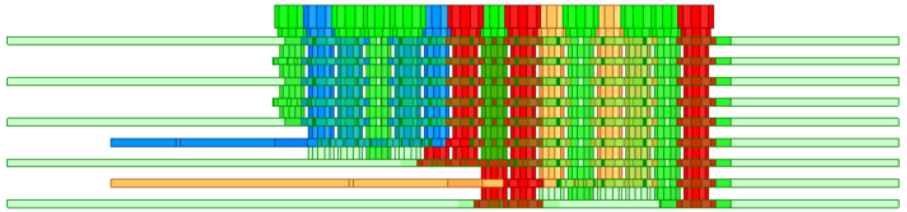
x32 module

Column 0	Column 1	Column 2	Column 3	Column 4	Column 5	Column 6	Column 7	Column 8	Column 9	Column 10	Column 11
	m2rxdatasb		m2rxcksb		vccaon		m2txcksb		m2txdatasb		vccaon
m1txdatasb		m1txcksb		vccaon		vccaon		m1rxcksb		m1rxdatasb	
	vccio		vccio		vccio		vccio		vccio		vccio
vss		vss		vss		vss		vss		vss	
	m2rxdata6		m2rxdata8		vss		m2txdata9		m2txdata7		vss
m2rxdata4		m2rxckp		m2rxdata10		m2txdata11		m2txckn		m2txdata5	
	vss		vss		vss		vss		vss		vss
m2rxdata5		m2rxckn		m2rxdata11		m2txdata10		m2txckp		m2txdata4	
	m2rxdata7		m2rxdata9		vss		m2txdata8		m2txdata6		vss
vss		vss		vss		vss		vss		vss	
	m2rxdata2		m2rxdata12		vss		m2txdata13		m2txdata3		vss
m2rxdata0		m2rxtrk		m2rxdata14		m2txdata15		m2txvld		m2txdata1	
	vss		vss		vss		vss		vss		vss
m2rxdata1		m2rxvld		m2rxdata15		m2txdata14		m2txtrk		m2txdata0	
	m2rxdata3		m2rxdata13		vccio		m2txdata12		m2txdata2		vccio
vccio		vccio		vccio		vccio		vccio		vccio	
	vss		vss		vccio		vss		vss		vccio
vccio		m1txdata7		m1txdata9		vccio		m1rxdata8		m1rxdata6	
	m1txdata5		m1txckn		m1txdata11		m1rxdata10		m1rxckp		m1rxdata4
vss		vss		vss		vss		vss		vss	
	m1txdata4		m1txckp		m1txdata10		m1rxdata11		m1rxckn		m1rxdata5
vss		m1txdata6		m1txdata8		vss		m1rxdata9		m1rxdata7	
	vss		vss		vss		vss		vss		vss
vccio		m1txdata3		m1txdata13		vccio		m1rxdata12		m1rxdata2	
	m1txdata1		m1txvld		m1txdata15		m1rxdata14		m1rxtrk		m1rxdata0
vccio		vss		vss		vccio		vss		vss	
	m1txdata0		m1txtrk		m1txdata14		m1rxdata15		m1rxvld		m1rxdata1
vss		m1txdata2		m1txdata12		vss		m1rxdata13		m1rxdata3	
Die Edge											

UCIe-S: Arrangement & Channel Characteristics





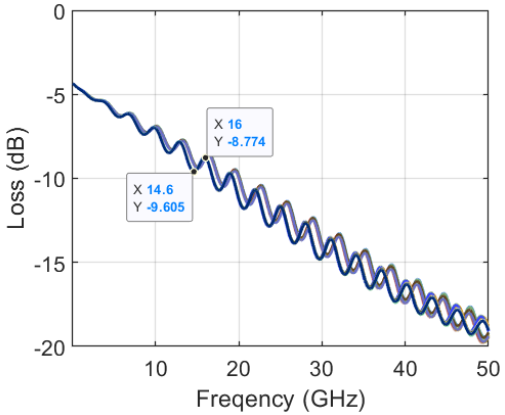


- 2-module stacking

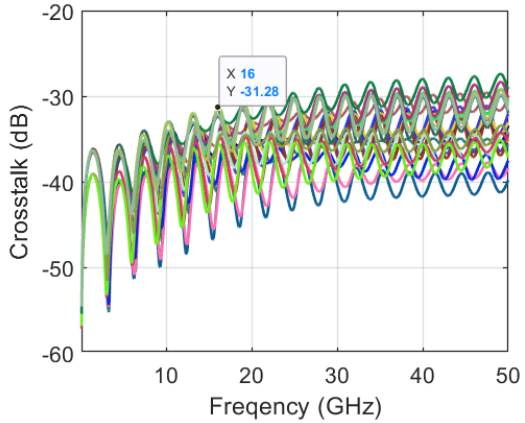
- 18 IO/mm/layer
- 2 routing layers for each module
- 4 routing layers for 2 modules

- power
- ground
- signals on L8
- signals on L6
- signals on L4 and L2 not shown

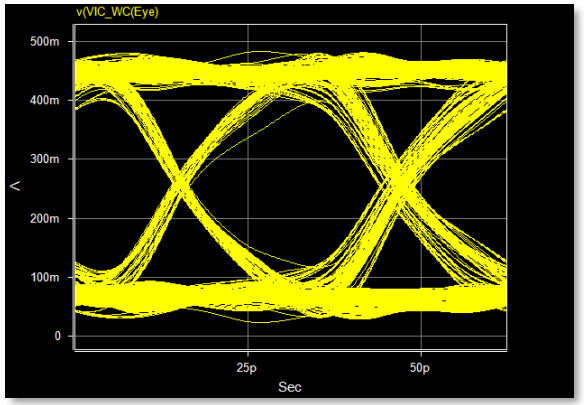
VTF Loss



Cumulative VTF Crosstalk



32Gb/s Eye Diagram



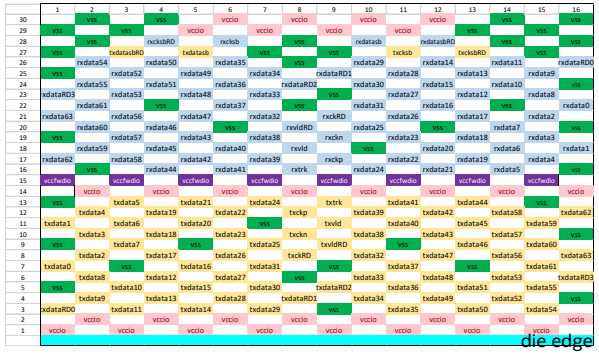
25mm length

Voltage Transfer Function (VTF)

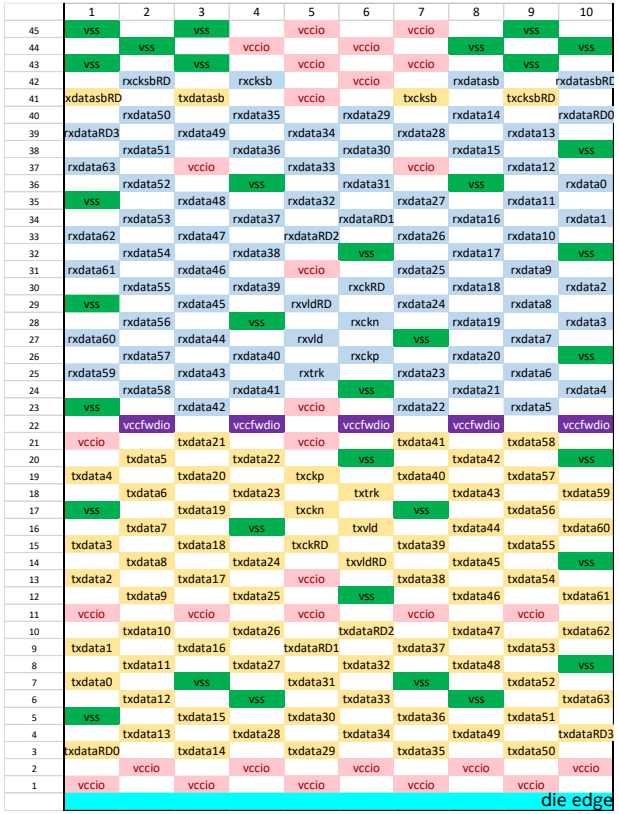
UCIe-A Bump Maps

- Bumpout configurations for maintaining optimized BW/mm^2 across allowable bump pitch range
  - 8, 10 and 16-columns
  - Suggested usage guideline:

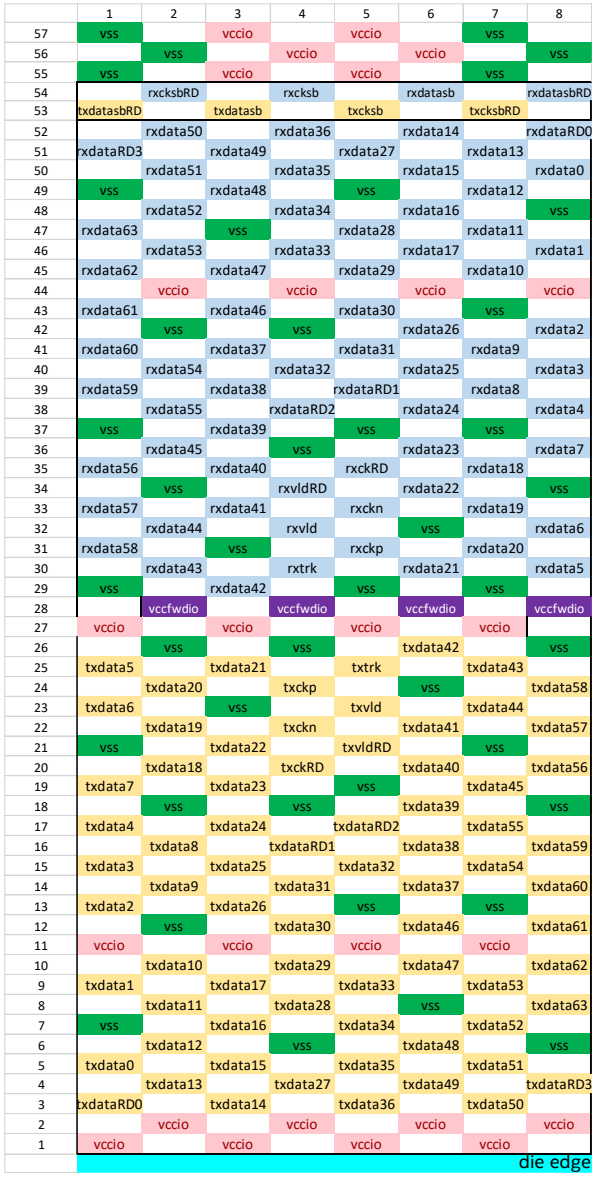
BP	Max Data Rate by Spec	Columns within 388.8 shoreline
25-30	12	16
31-37	16	
38-44	24	10
45-50	32	
51-55	32	8



16Col
Recommended for
25-37um bump pitch

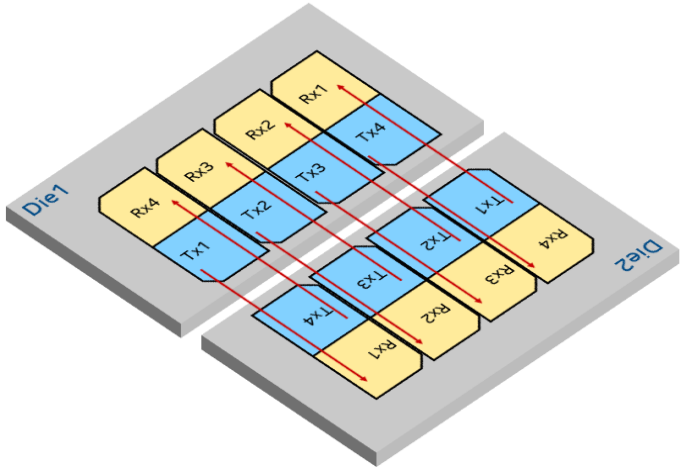


10Col
Recommended for
38-50um bump pitch

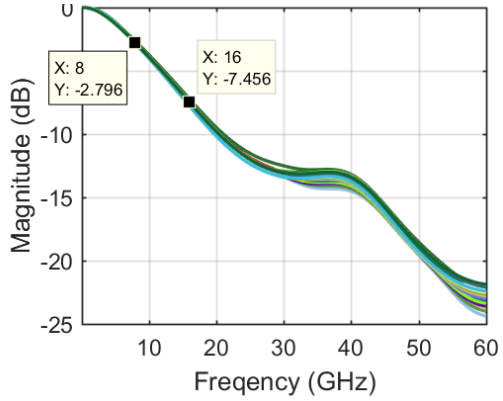


8Col
Recommended for
51-55um bump pitch

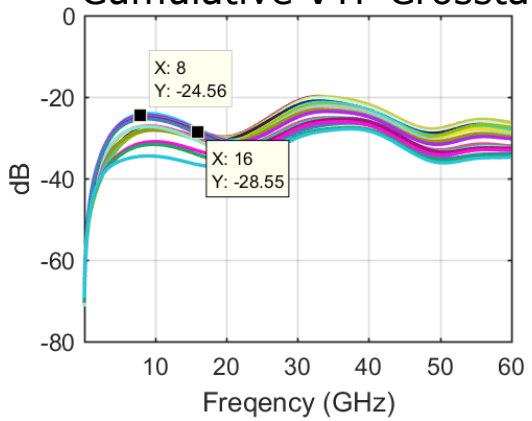
UCIe-A: Arrangement & Channel Characteristics



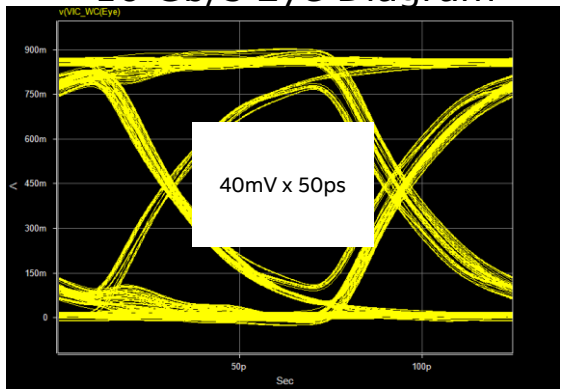
VTF Loss



Cumulative VTF Crosstalk



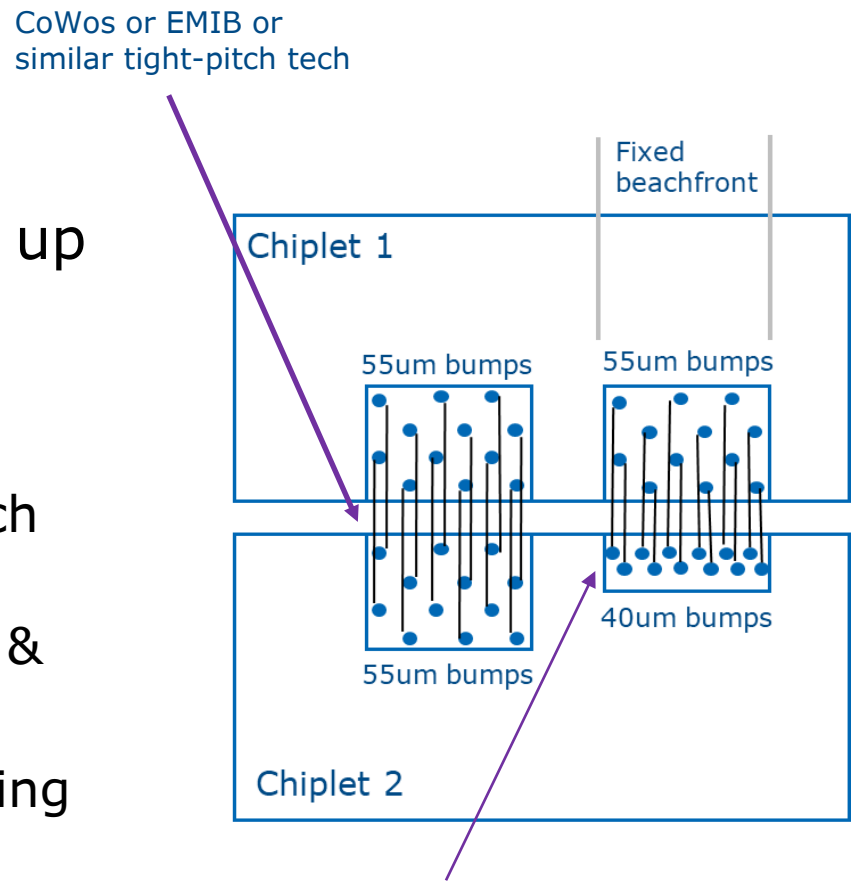
16 Gb/s Eye Diagram



Voltage Transfer Function (VTF)

UCIe-A Interoperability

- Advanced package planning of key parameters up front for interop across IDMs/OSATs:
  - PHY beachfront must be spec to balance BW/mm capability and mechanical compatibility
  - Inter-generational compatibility across bump pitch range
    - Fixed beachfront (388.8um) per PHY module &
    - Signal ordering rules
  - Comprehensive PHY placement & rotation/mirroring rules



- With the reduction of bump pitch, the number of rows decrease while the number of columns increase
- Interop is enabled by a fixed beachfront & following signal ordering rules

UCIe 1.1 delivers the best KPIs while meeting the projected needs for the next 5-6 years across the compute continuum

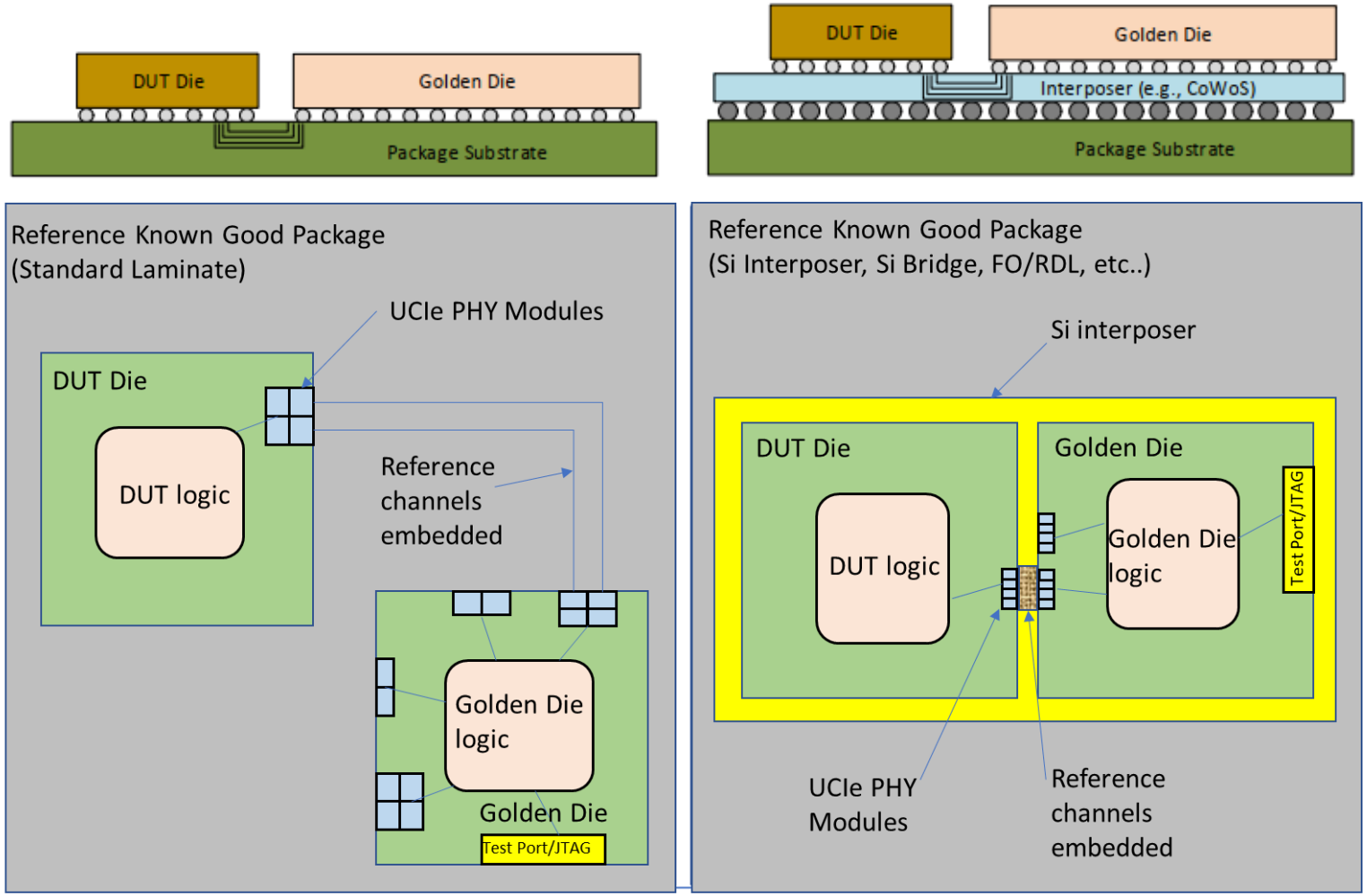
Compliance Overview

- The goal of Compliance testing
  - To validate the **main-band** supported features of a Device Under Test (DUT) against a known good reference UCIe implementation (Golden-Die)
    - Electrical compliance (Device and Channel)
    - Protocol layer compliance
    - Adapter layer
- UCIe PHY register read/write and status access
  - The UCIe **side-band link** plays a critical role for enabling compliance testing by allowing compliance software to access registers from different UCIe components (e.g. Physical Layer, D2D Adapter, etc.) for setting up tests as well as monitoring status
- **Compliance Test Document** to be published
  - Golden Die details, including form factor, and system-level behavior
  - Compliance test setup, such as the channel model and package level details
  - Compliance test content details (what and how)

Compliance Setup

Consist of:

- Reference UCIe implementation across all layers of the UCIe stack (Golden UCIe)
- DUT: to be tested with reference design
  - Required to have cleared die sort/pre-bond testing
- For Advanced Package, a known good silicon bridge or interposer.



Protocol and Adapter Compliance

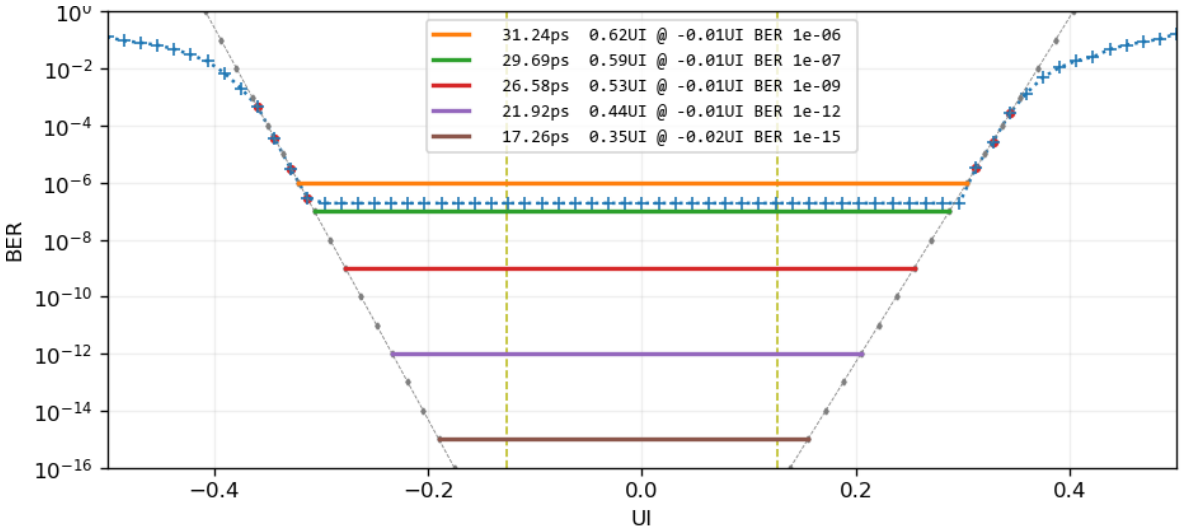
- Protocol Layer Compliance
  - For **PCIe and CXL Protocol** Layers, UCIe leverages the protocol compliance defined in those specs
  - For **Streaming protocols**, Protocol interop is specific to the protocol being streamed and is beyond scope of the UCIe spec
- Adapter Compliance:
  - **Golden Die Adapter** must have all the capabilities defined in UCIe spec and must have the capability to inject both consistent and inconsistent sideband messages to test DUT for various error scenarios
  - **DUT** must have Control and Status registers for:
    - Ability to Inject Test or NOP Flits
    - Injection of Link State Request or Response sideband messages
    - Retry injection control

PHY Compliance

- Golden Die must support capabilities to force timeouts on all applicable sideband messages as well as state residence timers
- Electrical Compliance Features:
  - Lane-to-Lane skew for a given module at both RX and TX
  - TX Equalization
  - Eye Margining
    - Horizontal Eye Margining - Timing
    - Vertical Eye Margining - Voltage (when supported)
  - BER measurement
    - Various power states/mode transitions (TBD)
    - Frequency and Vccio shmoo test (TBD)

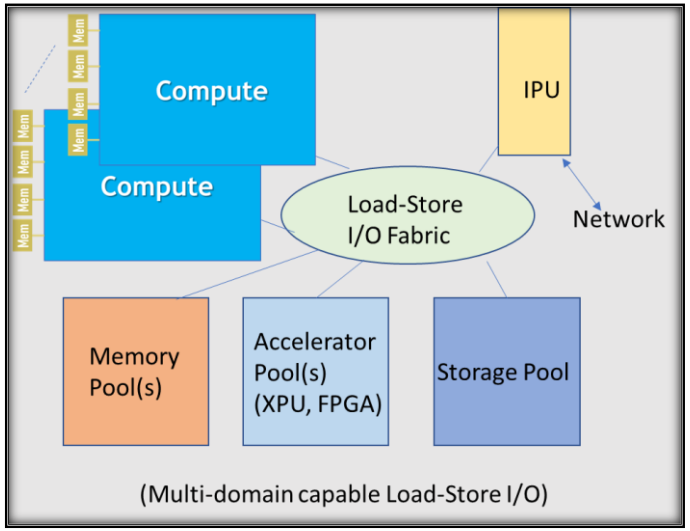
- BER Extrapolation to 1E-15 and 1E-27
- Total Jitter = $DJ_{pkpk} + 2*Q*\sigma_{RJ}$

$$Q = \sqrt{2}\ \mathrm{erfc}^{-1}\left(\frac{BER}{\rho_T}\right)$$

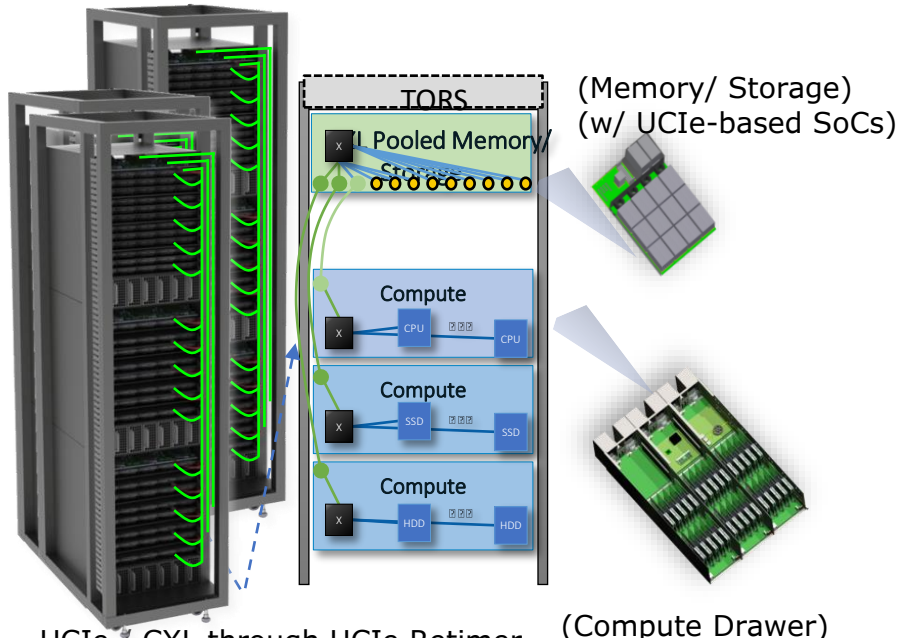


Example Figure courtesy of Teradyne

UCIe Usage: Off-package Connectivity w/ Re-timers

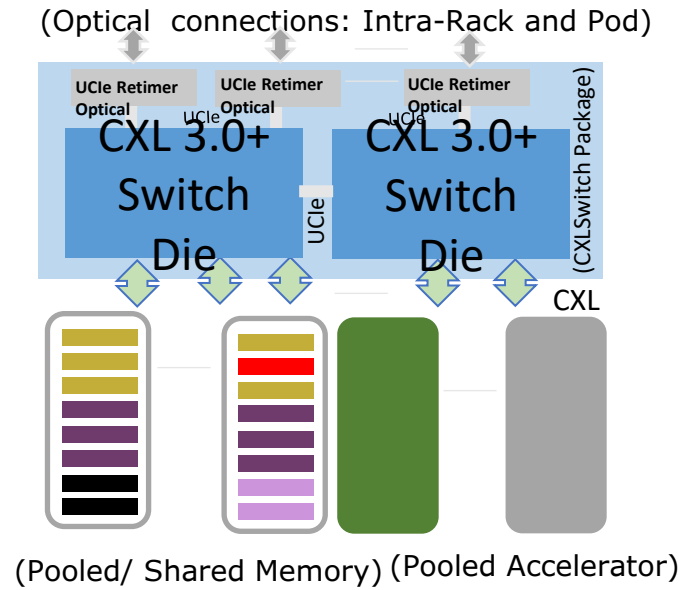


(Use Case: Load-Store I/O (CXL) as the fabric across the Pod providing low-latency and high bandwidth resource pooling/ sharing as well as message passing)



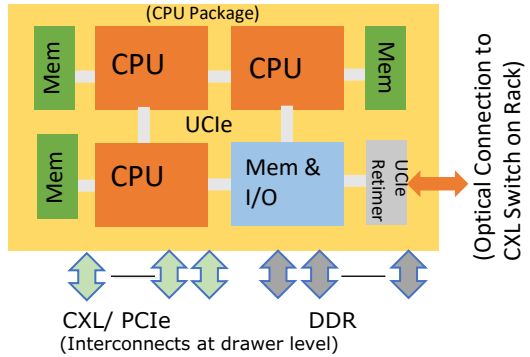
UCIe / CXL through UCIe Retimer

Provision to extend off-package with UCIe Retimers connecting to other media (e.g., optics)

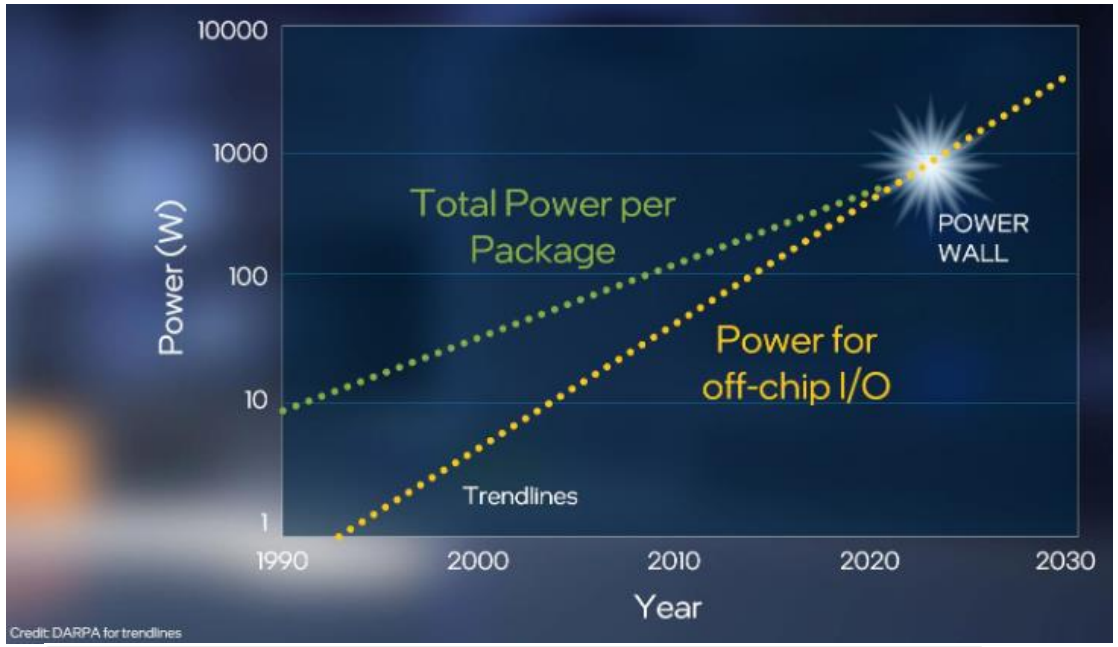


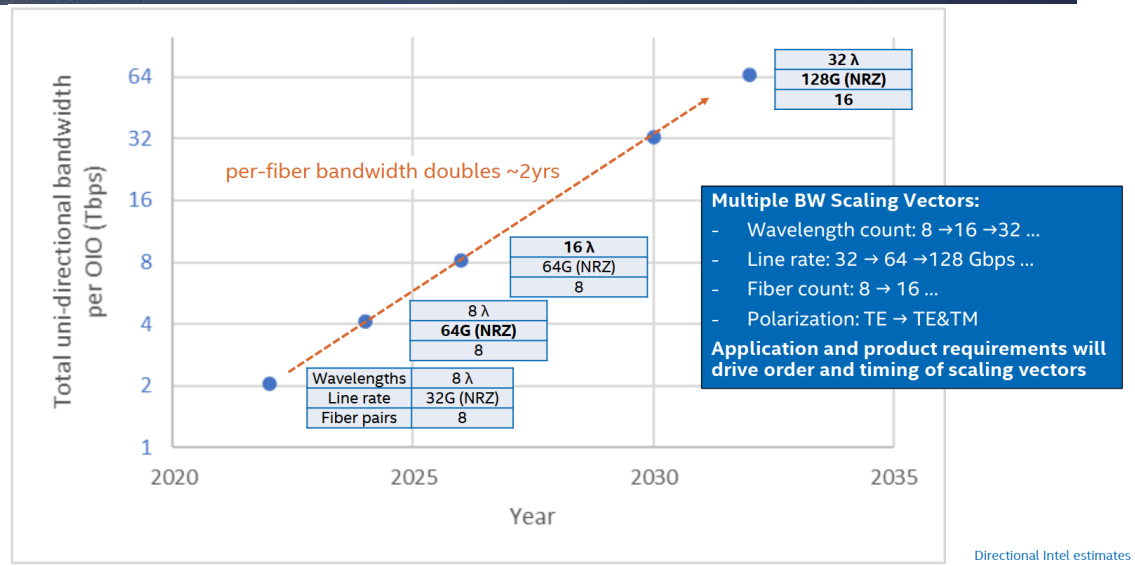
(Switch dies connected through UCIe PHY + Adapter Running a proprietary switch internal protocol)

(Another example can be multi-terabit networking switches Constructed from UCIe-based co-packaged optics and partitionable networking switch dies connected through UCIe on package



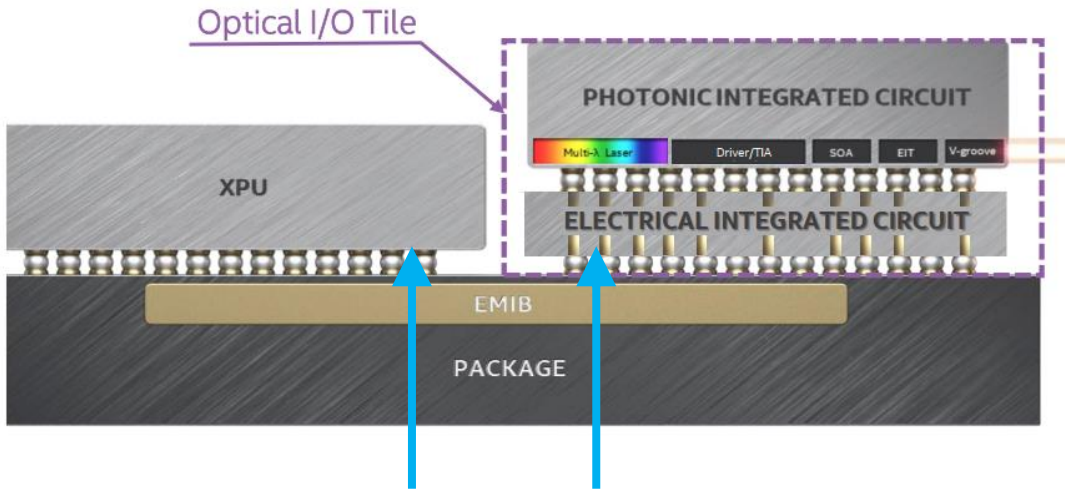
Electrical KPI and Optical I/O





Directional Intel estimates

- I/O consumes increasing percentage of system power ➔ Power Wall
- Scaling of Electrical I/O has slowed
  - Will continue to scale, but may not be able to keep up with the demand of some applications.
- Optical I/O offers a new scaling options:
  - Parallel optics: µLED, VCSEL
  - Si Photonics: with wavelength-division multiplexing
- UCIe's KPI enables full realization of optical potential



Short electrical link: UCIe

UCIe 1.1 delivers the best KPIs while meeting the projected needs for the next 5-6 years.

Wide industry leader adoption spanning semiconductor, manufacturing, assembly, & cloud segments.

UCIe 1.1: Characteristics and Key Metrics

CHARACTERISTICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<=2	

KPIs / TARGET FOR KEY METRICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm^2)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit latency	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ UCIe Flit Mode

UCIe™
Universal Chiplet
Interconnect Express

The First UCIe Silicon Interoperability:
Intel silicon on Intel Process with Synopsys silicon on TSMC process

Sept 19, 2023

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At today's Intel Innovation keynote, Pat Gelsinger showcased the first UCIe interoperable demo featuring technology from UCIe Consortium member companies Intel Corporation, Synopsys Inc and TSMC.

The Pike Creek test silicon contains an Intel UCIe IP chiplet fabricates on IFS Intel 3 and a Synopsys UCIe IP chiplet fabricated on a TSMC N3E process node and packaged using EMIB advanced packaging technology. This demo highlights the UCIe open standard-based chiplet ecosystem, and the future of chiplet interoperability.

Learn more from Tom's Hardware: https://bit.ly/3Lpzn5i
#UCIe #UCIeConsortium #chiplets