Artix_7A50T

Avnet Engineering Services

www.Artix50.org

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Artix_7A50T

19 Jun 2014

10:04:35 AM

AVNET Avnet Engineering Services		
Title: 01 - Avnet Lead Sheet_B.SchDoc		
Size: B	Project Name: Artix_7A50T	Rev: A
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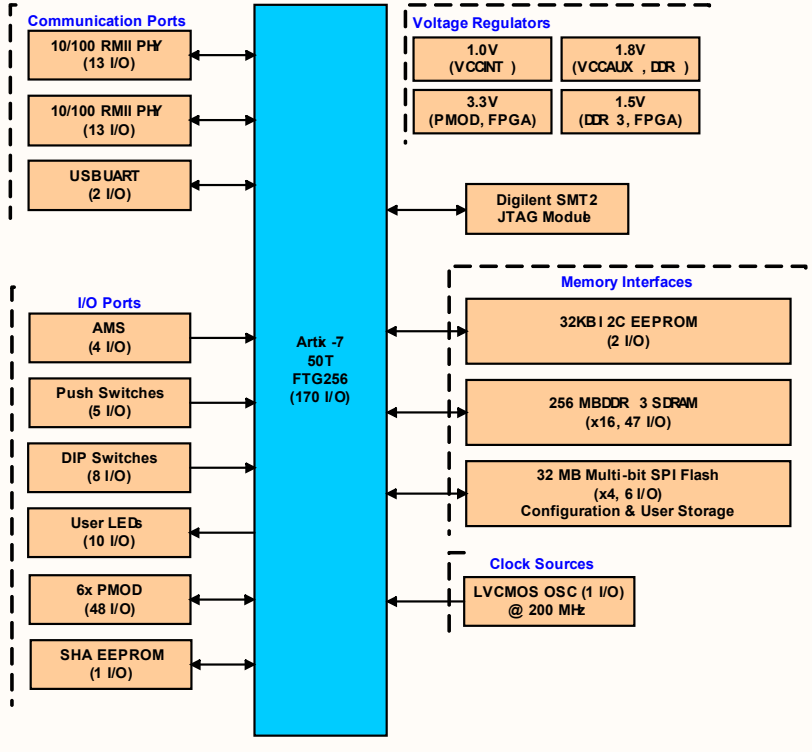
Topology



AVNET Avnet Engineering Services		
Title: 02 - Block Diagram.SchDoc		
Size: B	Project Name: Artix_7A50T	Rev: A
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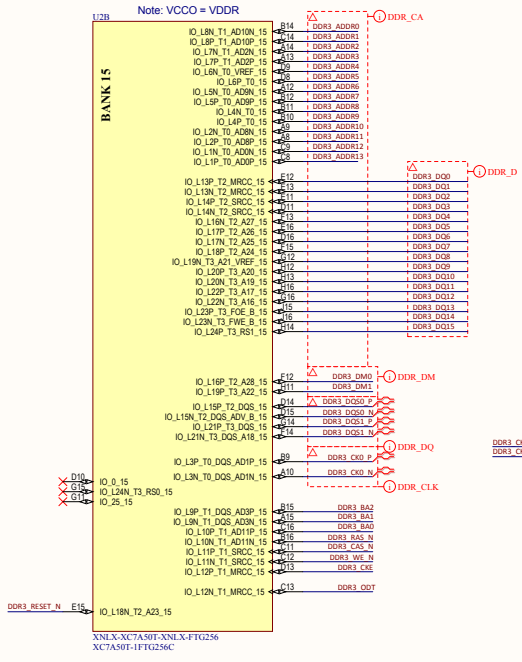
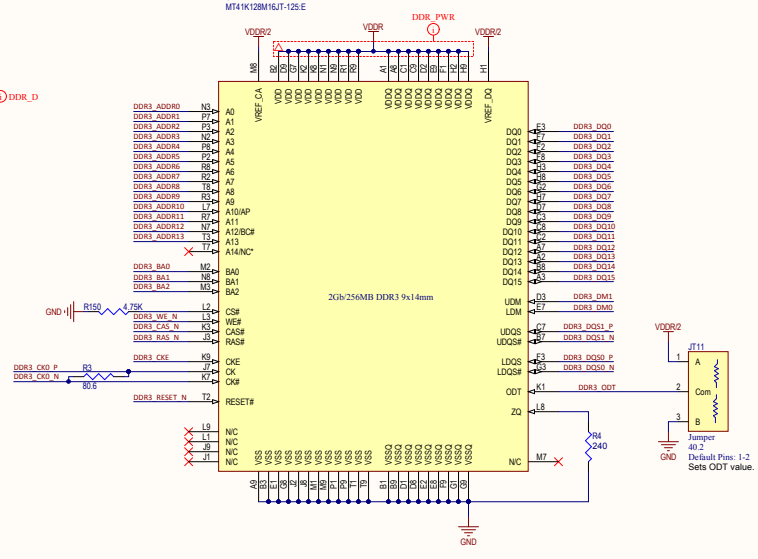
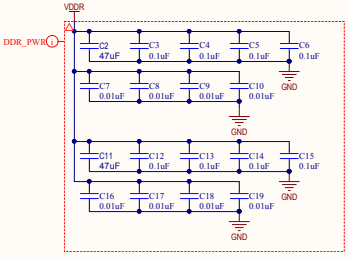
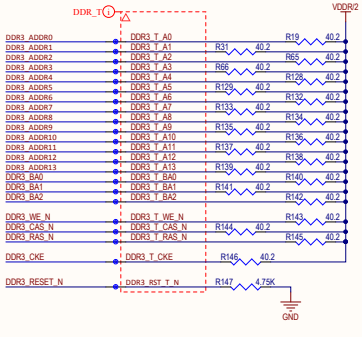


256MB DDR3 1600 MEMORY

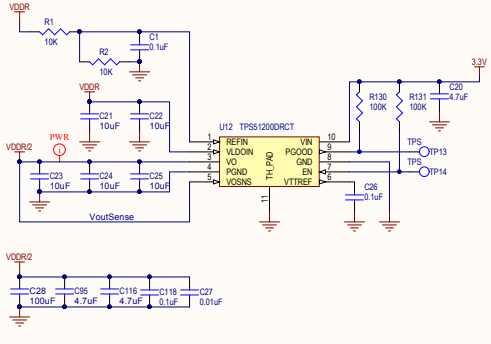




DDR3 ADDR & CNTRL TERMINATION RESISTORS



DDR3 TERMINATION REGULATOR



DDR3 single-ended traces are 40 Ohms impedance
DDR3 Differential traces are 80 Ohms differential impedance

All DDR RAM traces are matched length and less than 2540 mils (25 mm). The below information is general guidance and is pending the FR4 board material composition and stack up.

Address and command trace spacing is 10 mil min for short runs, 4 mils
clearance for parallel runs less than 500 mils.
Data trace spacing is 10 mil min for short runs, 4 mils clearance for parallel
runs less than 500 mils.

Place clock signals on internal layers to minimize EMI.
Match CK trace length to CK# trace length within +/- 20 mil.
Clock pairs should be equivalent within +/- 20 mil.
Clock and DQS should be length matched.
Clock to Address / Control should be matched within +/-400 mil.

For further information, see Micron's Tech Notes: TN4113 & TN-52-02

AVNET Avnet Engineering Services		
Title: 03 - BANK 15 DDR3 Memory.SchDoc		
Size: C	Project Name: Artix_7A50T	Rev: A
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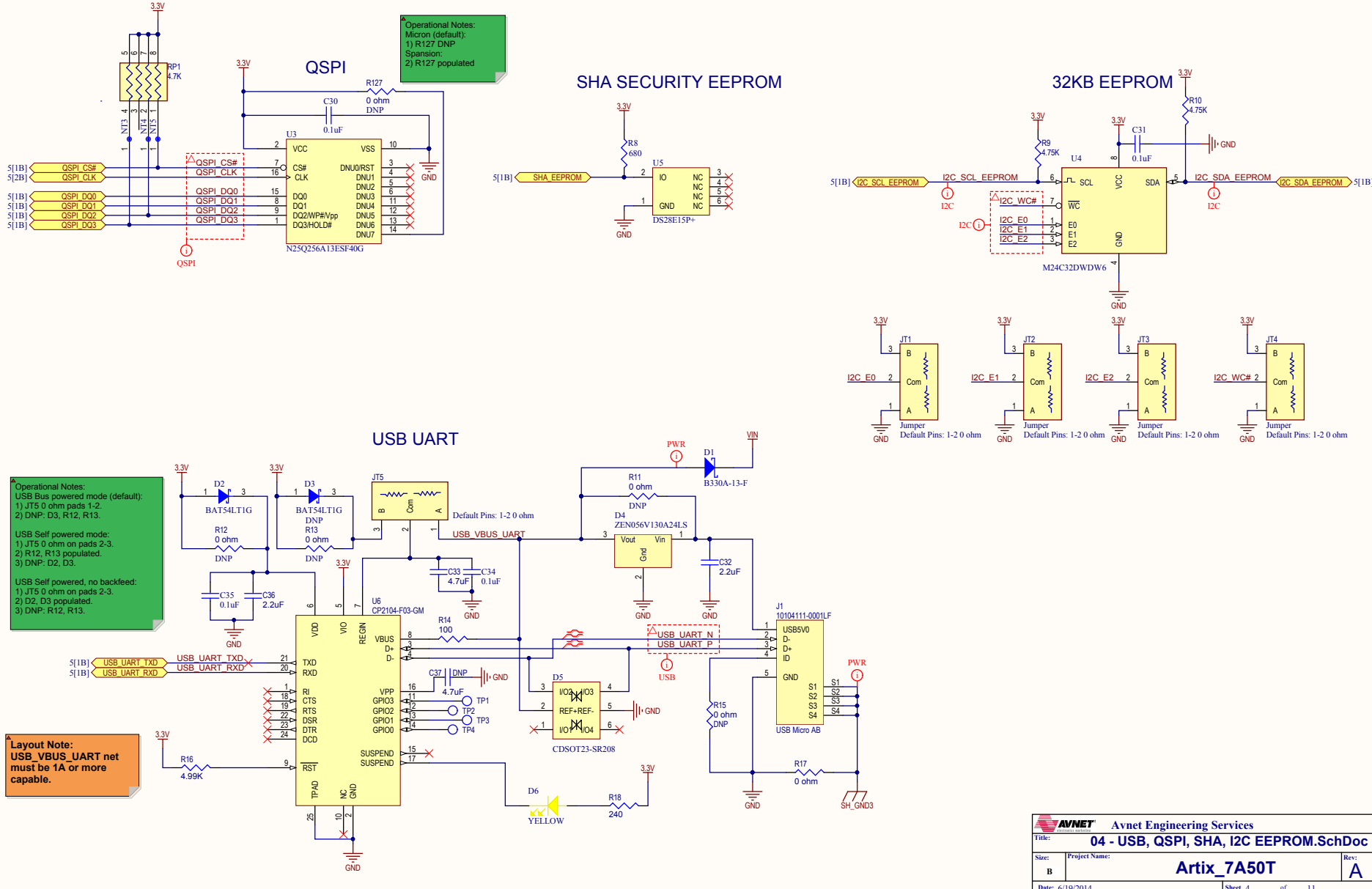
QSPI
Operational Notes:
Micron (default):
1) R127 DNP
Spansion:
2) R127 populated
SHA SECURITY EEPROM
32KB EEPROM
USB UART
Operational Notes:
USB Bus powered mode (default):
1) JT5 0 ohm pads 1-2.
2) DNP: D3, R12, R13.
USB Self powered mode:
1) JT5 0 ohm on pads 2-3.
2) R12, R13 populated.
3) DNP: D2, D3.
USB Self powered, no backfeed:
1) JT5 0 ohm on pads 2-3.
2) D2, D3 populated.
3) DNP: R12, R13.
Layout Note:
USB_VBUS_UART net must be 1A or more capable.
N25Q256A13ESF40G
DS28E15P+
M24C32DWDW6
CP2104-F03-GM
CDSOT23-SR208
B330A-13-F
ZEN056V130A24LS
10104111-0001LF
USB Micro AB
Jumper
Default Pins: 1-2 0 ohm
Avnet Engineering Services
Title: 04 - USB, QSPI, SHA, I2C EEPROM.SchDoc
Size: B
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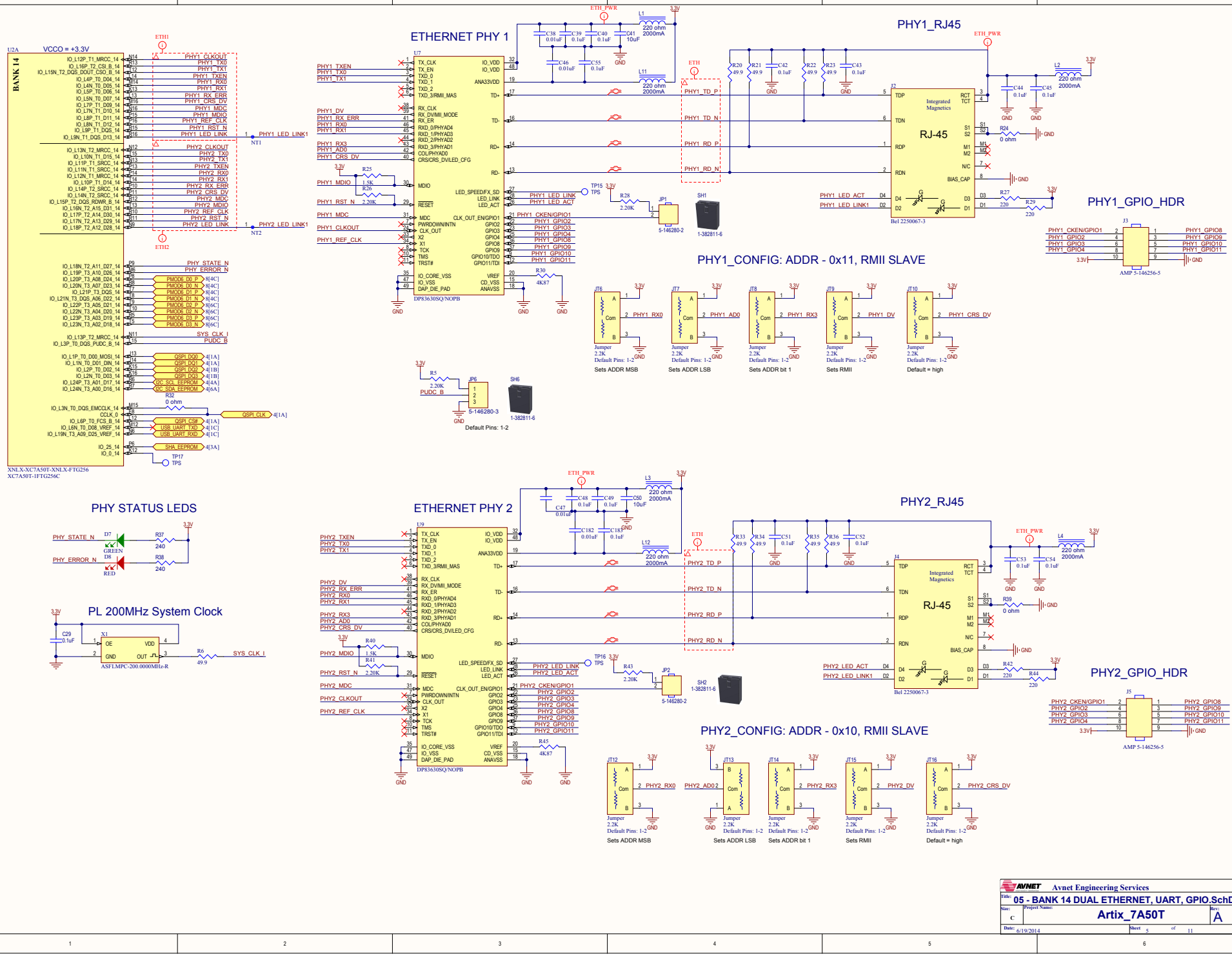
BANK 14
VCCO = +3.3V
XNLX-XC7A50T-XNLX-FTG256
XC7A50T-1FTG256C
PHY STATUS LEDS
PL 200MHz System Clock
ASFLMPC-200.0000MHz-R
ETHERNET PHY 1
DP83630SQ/NOPB
PHY1_RJ45
RJ-45
PHY1_GPIO_HDR
AMP 5-146256-5
PHY1_CONFIG: ADDR - 0x11, RMII SLAVE
Sets ADDR MSB
Sets ADDR LSB
Sets ADDR bit 1
Sets RMII
Default = high
ETHERNET PHY 2
PHY2_RJ45
PHY2_GPIO_HDR
PHY2_CONFIG: ADDR - 0x10, RMII SLAVE
Avnet Engineering Services
05 - BANK 14 DUAL ETHERNET, UART, GPIO.SchDoc
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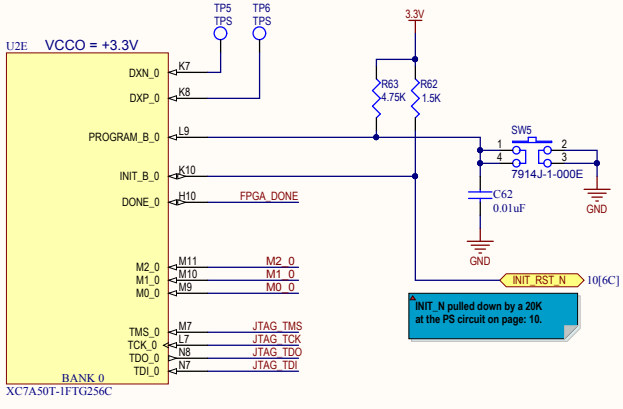
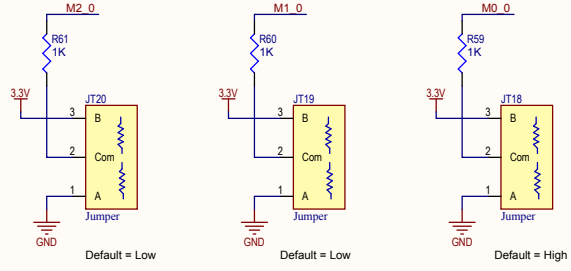
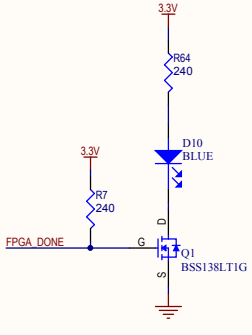
PROG_PB RESET



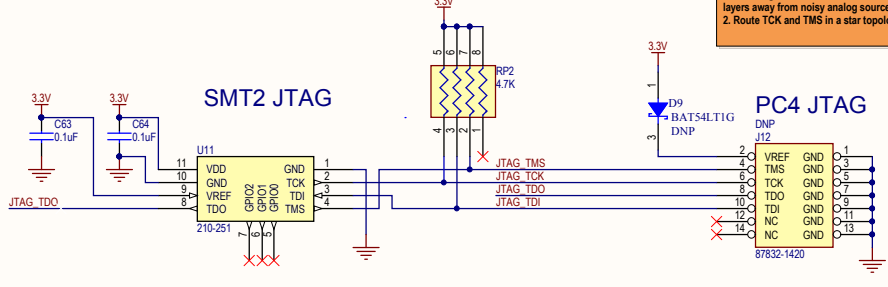
BOOT MODE SELECT



FPGA DONE LED



DUAL JTAG



Layout Note:

JTAG circuit routing should adhere to the following guidelines:
1. JTAG signals should be routed on the outer layers away from noisy analog sources
2. Route TCK and TMS in a star topology

Avnet Engineering Services		
Title: 06 - BANK 0, SMT2 JTAG, BOOT MODE.SchDoc		
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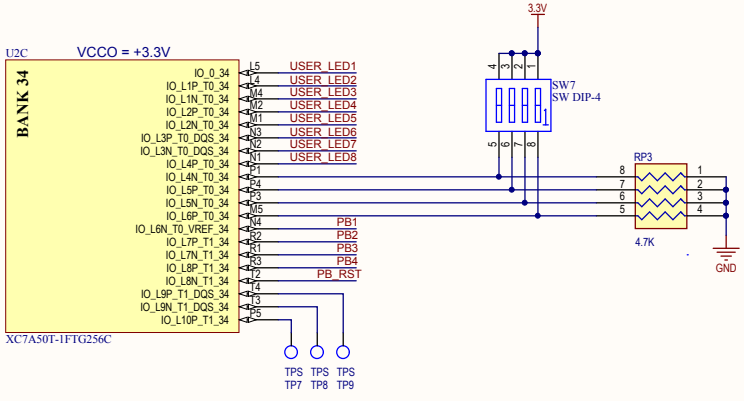
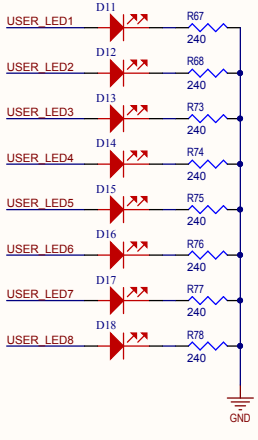
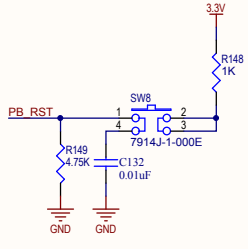
USER SLIDE SWITCHES



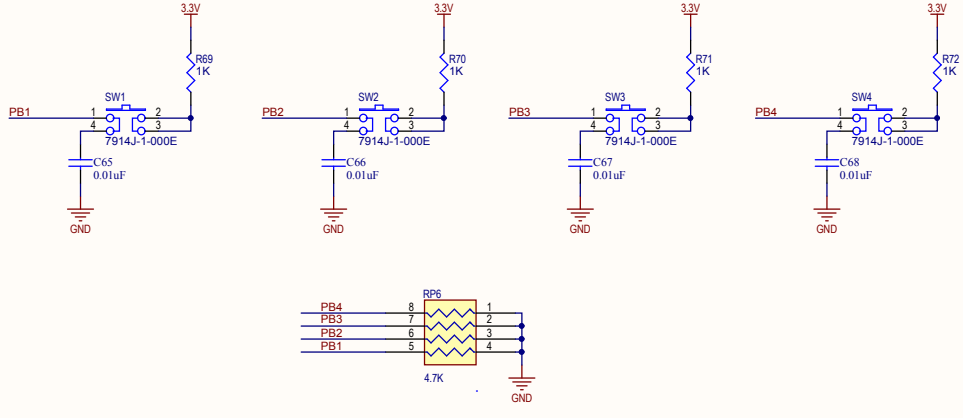
8 USER LEDS



CPU_RST



USER_PUSH_BUTTONS



AVNET Avnet Engineering Services		
Title: 07 - BANK 34 SWITCHES, LEDs.SchDoc		
Size: B	Project Name: Artix_7A50T	Rev: A
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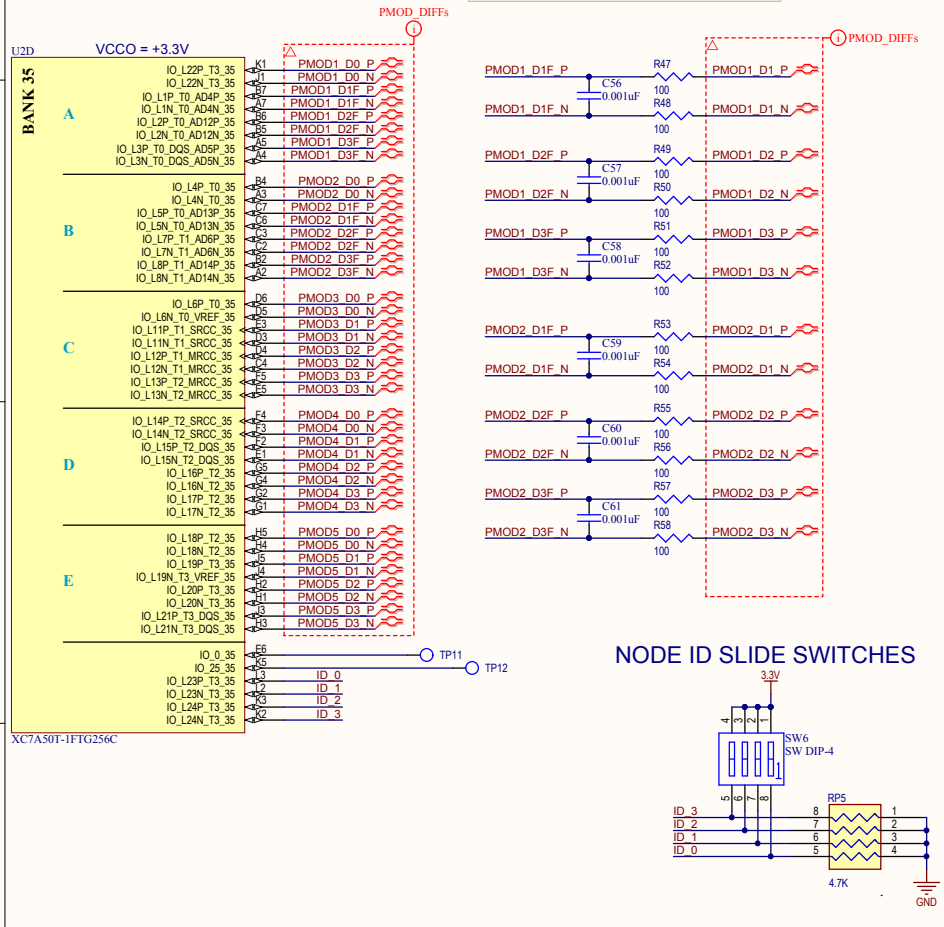
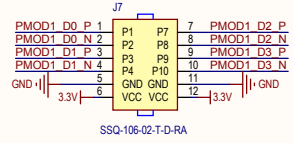
LAYOUT NOTE:
All PMOD signals routed differentially (P/N pairs) and length tuned to each other on each header.

LAYOUT NOTE:
Place resistors and capacitors as close as possible to FPGA.

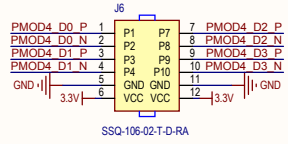


NODE ID SLIDE SWITCHES

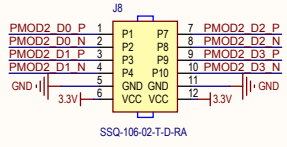
PMOD 1 Interface



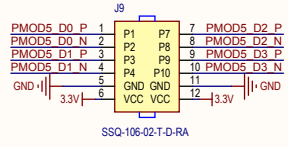
PMOD 4 Interface



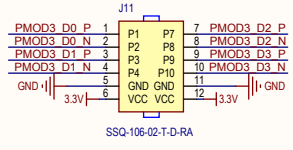
PMOD 2 Interface



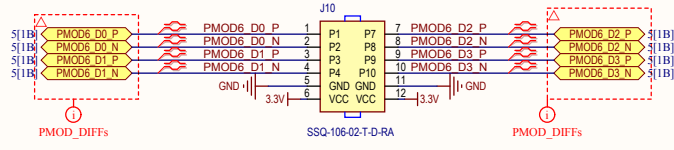
PMOD 5 Interface



PMOD 3 Interface



PMOD 6 Interface



AVNET Avnet Engineering Services		
Title: 08 - BANK 35 PMOD Interfaces.SchDoc		
Size: B	Project Name: Artix_7A50T	Rev: A
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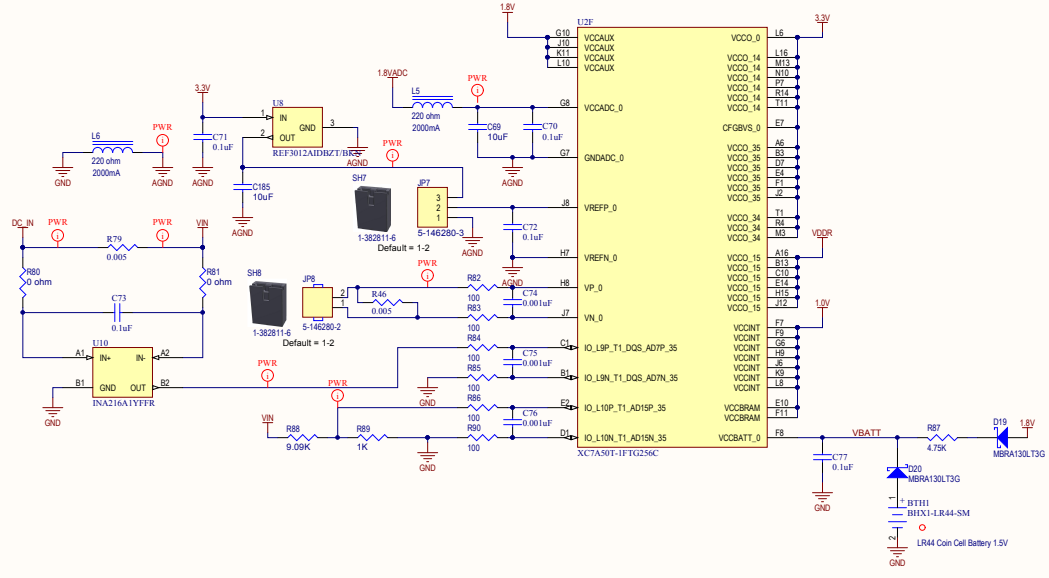
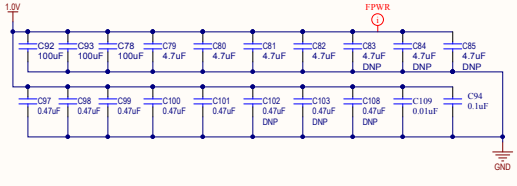
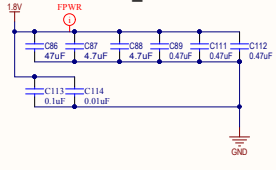


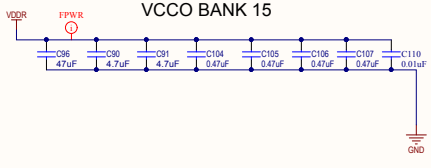
VCCINT



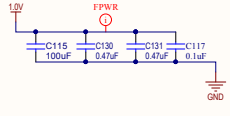
VCC_AUX



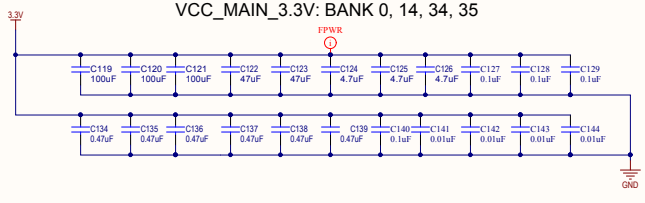
VCCO BANK 15



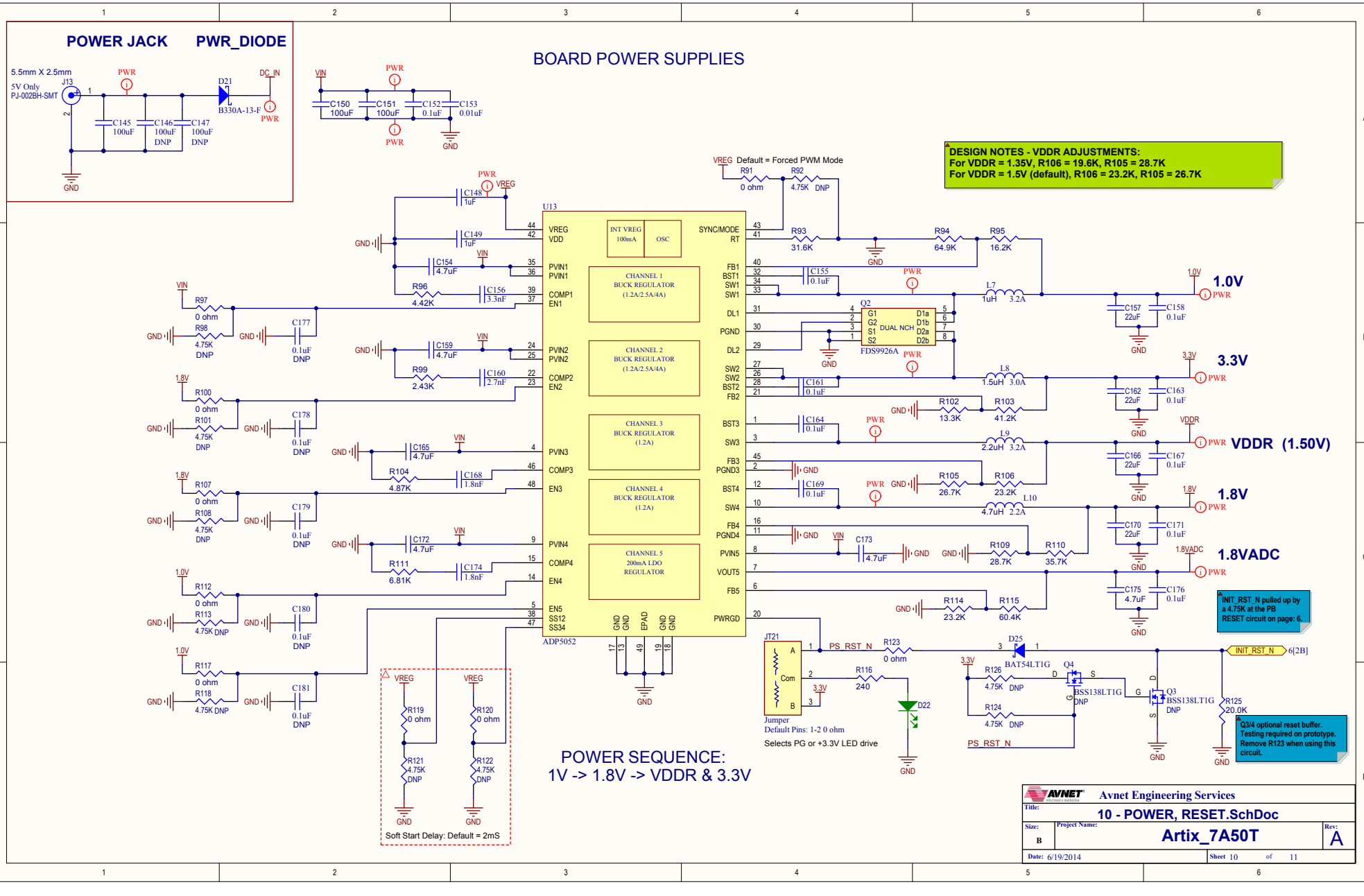
VCC_BRAM



VCC_MAIN_3.3V: BANK 0, 14, 34, 35



AVNET	Avnet Engineering Services	
Title:	09 - FPGA POWER.SchDoc	
Size: C	Project Name: Artix_7A50T	Rev: A
Date: 6/19/2014	Sheet 9 of 11	


POWER JACK
PWR_DIODE
5.5mm X 2.5mm
5V Only
PJ-002BH-SMT
J13
D21
B330A-13-F
DC_IN
PWR
GND
C145 100uF
C146 100uF DNP
C147 100uF DNP
C150 100uF
C151 100uF
C152 0.1uF
C153 0.01uF
VIN
BOARD POWER SUPPLIES
DESIGN NOTES - VDDR ADJUSTMENTS:
For VDDR = 1.35V, R106 = 19.6K, R105 = 28.7K
For VDDR = 1.5V (default), R106 = 23.2K, R105 = 26.7K
U13
ADP5052
INT VREG 100mA
OSC
CHANNEL 1 BUCK REGULATOR (1.2A/2.5A/4A)
CHANNEL 2 BUCK REGULATOR (1.2A/2.5A/4A)
CHANNEL 3 BUCK REGULATOR (1.2A)
CHANNEL 4 BUCK REGULATOR (1.2A)
CHANNEL 5 200mA LDO REGULATOR
VREG Default = Forced PWM Mode
R91 0 ohm
R92 4.75K DNP
R93 31.6K
R94 64.9K
R95 16.2K
1.0V
3.3V
VDDR (1.50V)
1.8V
1.8VADC
Q2
FDS9926A
DUAL NCH
L7 1uH 3.2A
L8 1.5uH 3.0A
L9 2.2uH 3.2A
L10 4.7uH 2.2A
INIT_RST_N pulled up by a 4.75K at the PB RESET circuit on page: 6.
INIT_RST_N 6[2B]
D25
BAT54LT1G
Q4
BSS138LT1G
DNP
Q3
BSS138LT1G
DNP
Q3/4 optional reset buffer. Testing required on prototype. Remove R123 when using this circuit.
JT21
Jumper
Default Pins: 1-2 0 ohm
Selects PG or +3.3V LED drive
D22
PS_RST_N
Soft Start Delay: Default = 2mS
POWER SEQUENCE:
1V -> 1.8V -> VDDR & 3.3V
AVNET
Avnet Engineering Services
Title: 10 - POWER, RESET.SchDoc
Size: B
Project Name: Artix_7A50T
Rev: A
Date: 6/19/2014
Sheet 10 of 11

Revision Notes:

Revision A:
1) Initial design

Mechanicals:

PCB
A7MB-7A50T-PCB-A

PCB Mounting Holes

MTG1
0
MOUNTING HOLE 125mil

MTG2
0
MOUNTING HOLE 125mil

MTG3
0
MOUNTING HOLE 125mil

MTG4
0
MOUNTING HOLE 125mil

Bumper Standoffs

BMPR1
0
SJ61A4
7.9mm Bumper

BMPR2
0
SJ61A4
7.9mm Bumper

BMPR3
0
SJ61A4
7.9mm Bumper

BMPR4
0
SJ61A4
7.9mm Bumper

AVNET Avnet Engineering Services		
Title: 11 - Back Page.SchDoc		
Size: B	Document Number: Artix_7A50.PrjPcb	Rev: A
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