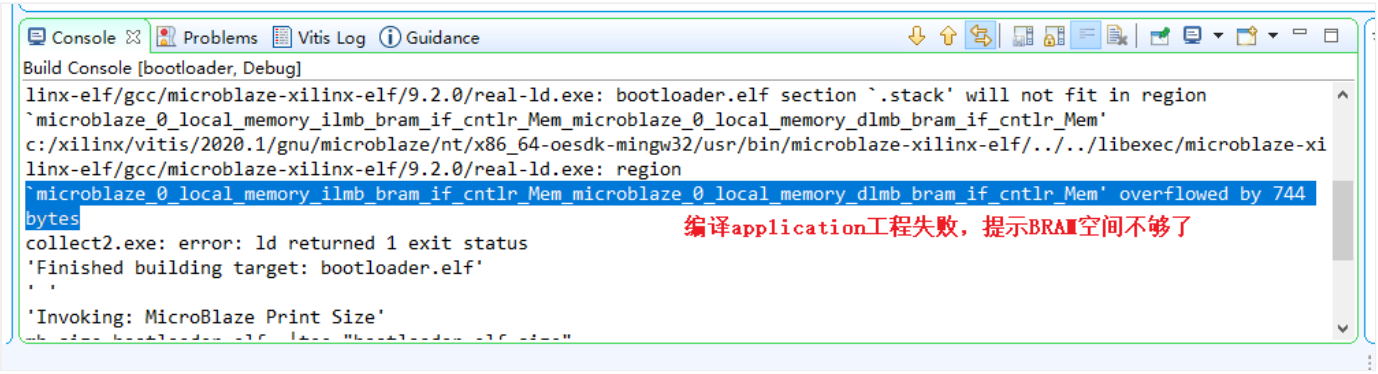
Xilinx Vitis 2020.1 method to modify the size of BRAM memory occupied by the project

tags: FPGA Vitis BRAM Microblaze Xilinx

After modifying the code and compiling the project, sometimes the compilation fails due to insufficient BRAM space, and the following error message appears:

TOP



'Invoking: MicroBlaze gcc linker'

mb-gcc -Wl,-T -Wl,../src/lscript.ld -LE:/fpga_projects/test4/microblaze_test/export/microblaze_test/sw/microblaze_test/standalone_domain/bsplib/lib -mlittle-endian -mcpu=v11.0 -mxl-soft-mul -Wl,--no-relax -Wl,--gc-sections -o "bootloader.elf" ./src/bootloader.o ./src/platform.o ./src/srec.o -Wl,--start-group,-lxil,-lgcc,-lc,--end-group -Wl,--start-group,-lxilisf,-lxil,-lgcc,-lc,--end-group c:/xilinx/vitis/2020.1/gnu/microblaze/nt/x86_64-oesdk-mingw32/usr/bin/microblaze-xilinx-elf/../../libexec/microblaze-xilinx-elf/gcc/microblaze-xilinx-elf/9.2.0/real-ld.exe: bootloader.elf section `.stack' will not fit in region `microblaze_0_local_memory_ilmb_bram_if_cntlr_Mem_microblaze_0_local_memory_dlmb_bram_if_cntlr_Mem' c:/xilinx/vitis/2020.1/gnu/microblaze/nt/x86_64-oesdk-mingw32/usr/bin/microblaze-xilinx-elf/../../libexec/microblaze-xilinx-elf/gcc/microblaze-xilinx-elf/9.2.0/real-ld.exe: region `microblaze_0_local_memory_ilmb_bram_if_cntlr_Mem_microblaze_0_local_memory_dlmb_bram_if_cntlr_Mem' overflowed by 744 bytes

collect2.exe: error: ld returned 1 exit status

'Finished building target: bootloader.elf'

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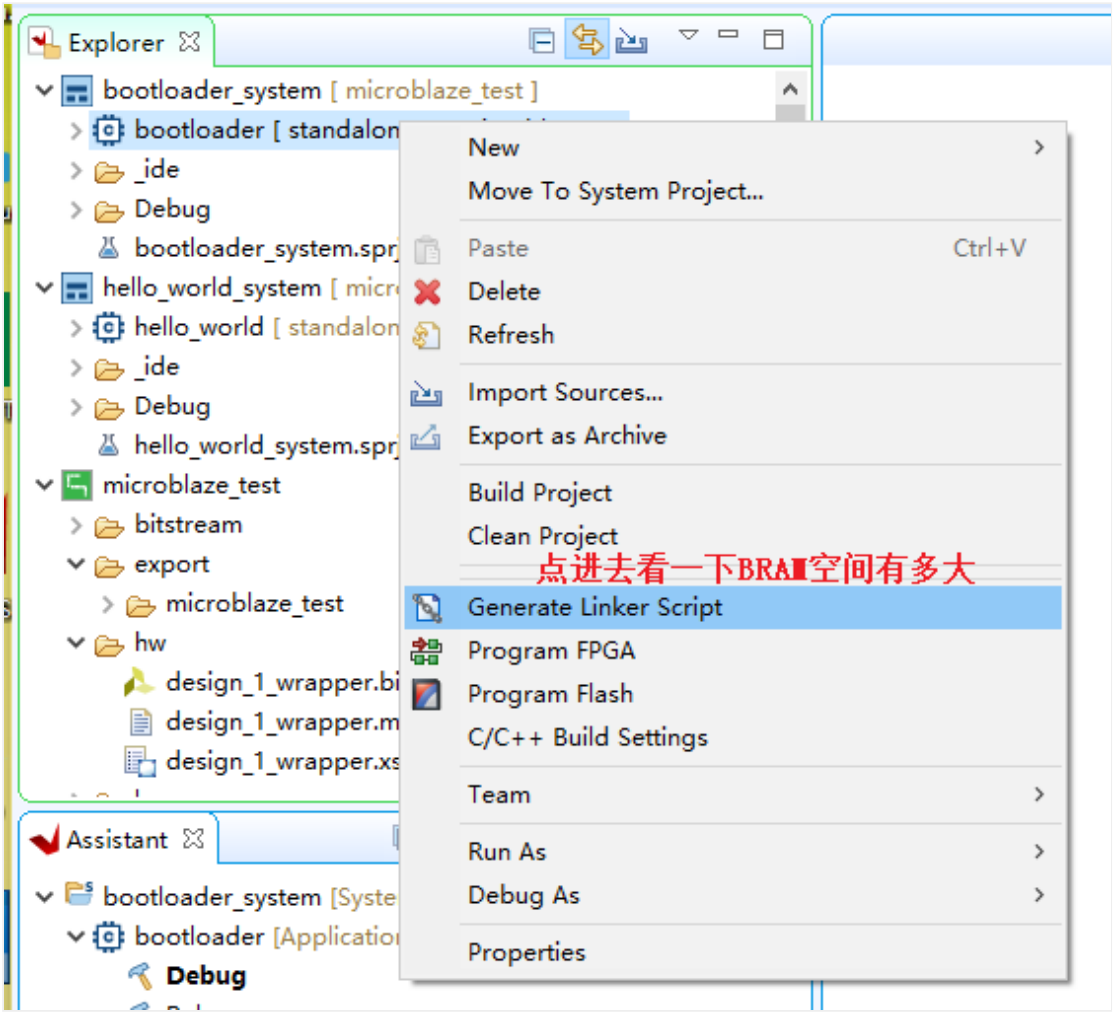
Explorer
bootloader_system [microblaze_test]
bootloader [standalon
_ide
Debug
bootloader_system.spr
hello_world_system [micr
hello_world [standalon
_ide
Debug
hello_world_system.spr
microblaze_test
bitstream
export
microblaze_test
hw
design_1_wrapper.bi
design_1_wrapper.m
design_1_wrapper.xs
Assistant
bootloader_system [Syste
bootloader [Applicatio
Debug
New
Move To System Project...
Paste Ctrl+V
Delete
Refresh
Import Sources...
Export as Archive
Build Project
Clean Project
点进去看一下BRAM空间有多大
Generate Linker Script
Program FPGA
Program Flash
C/C++ Build Settings
Team
Run As
Debug As
Properties

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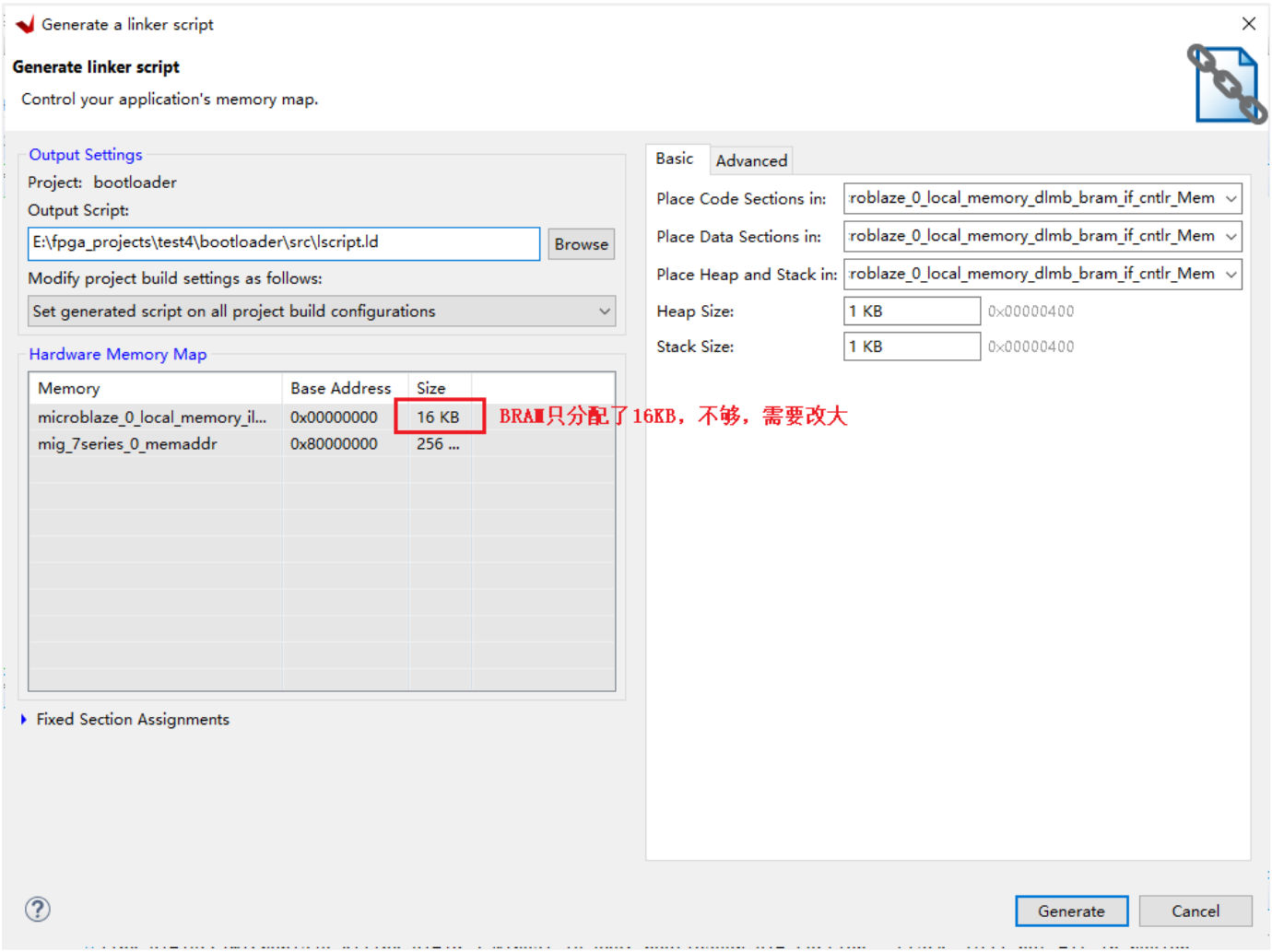

At this time, you need to go back to the Vivado project and increase the size of the allocated BRAM space in Block Design. The specific method is as follows.

Enter the Address Edditor of IP INTEGRATOR:

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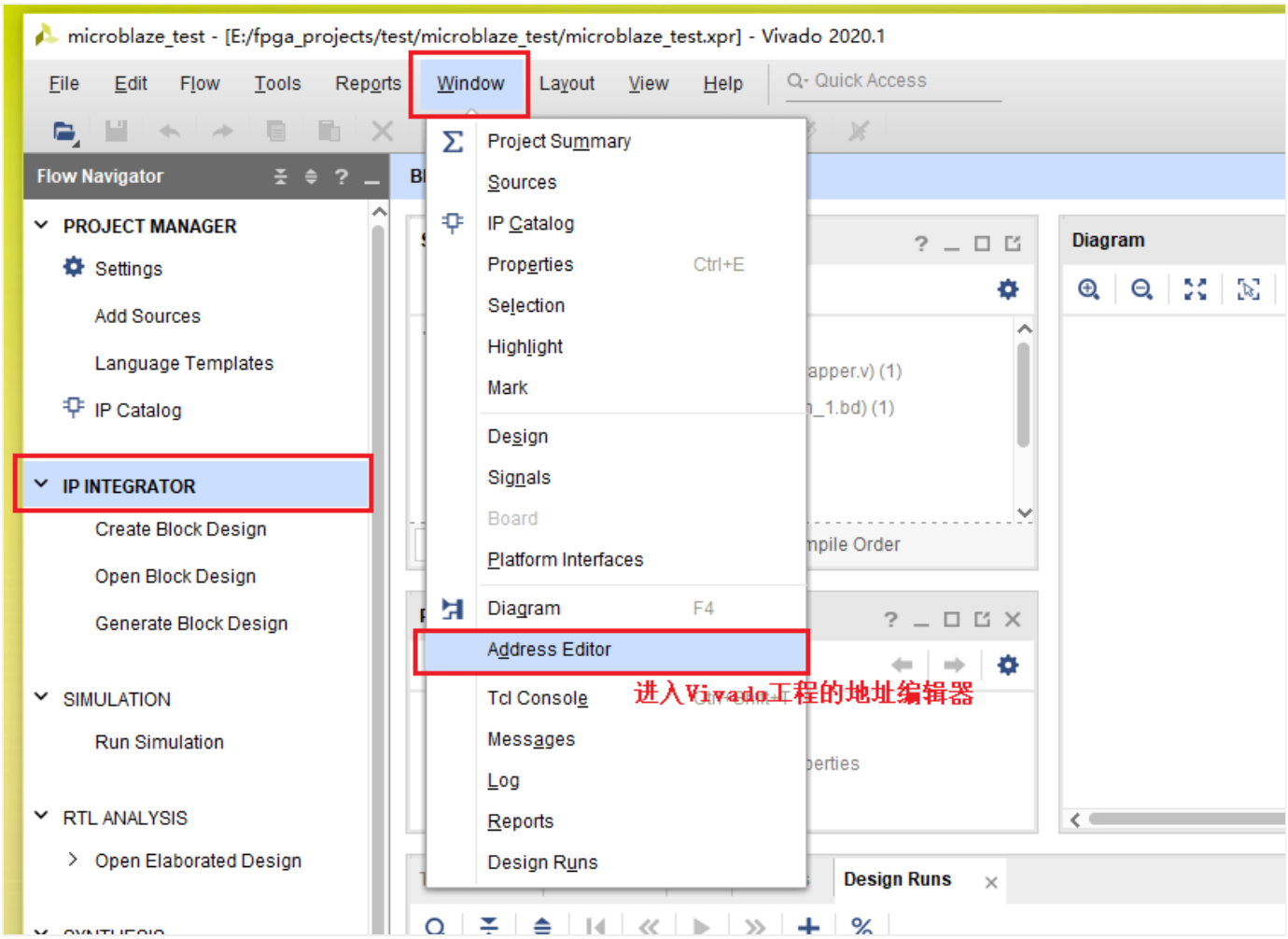
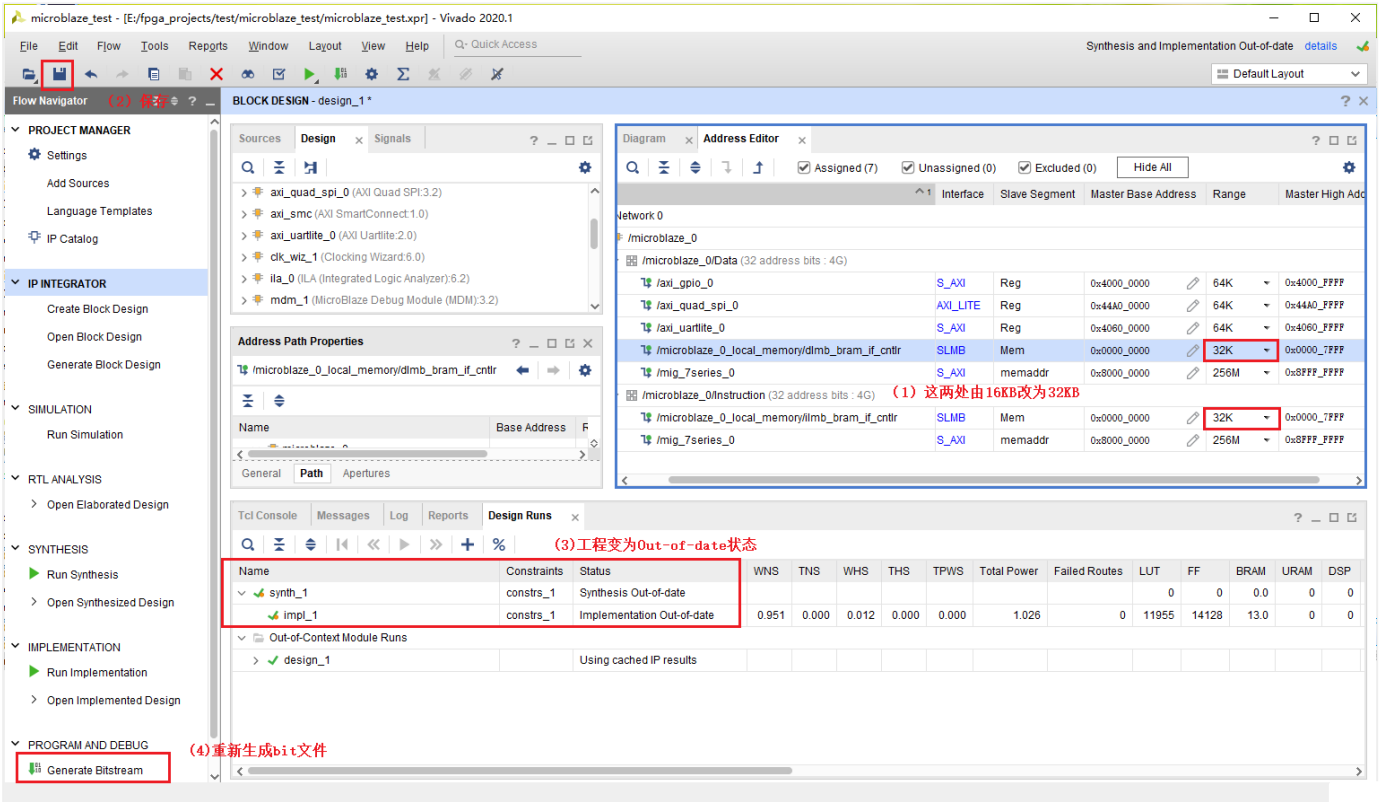


Modify the BRAM space size from 16KB to 32KB, save, and then regenerate the bit file.



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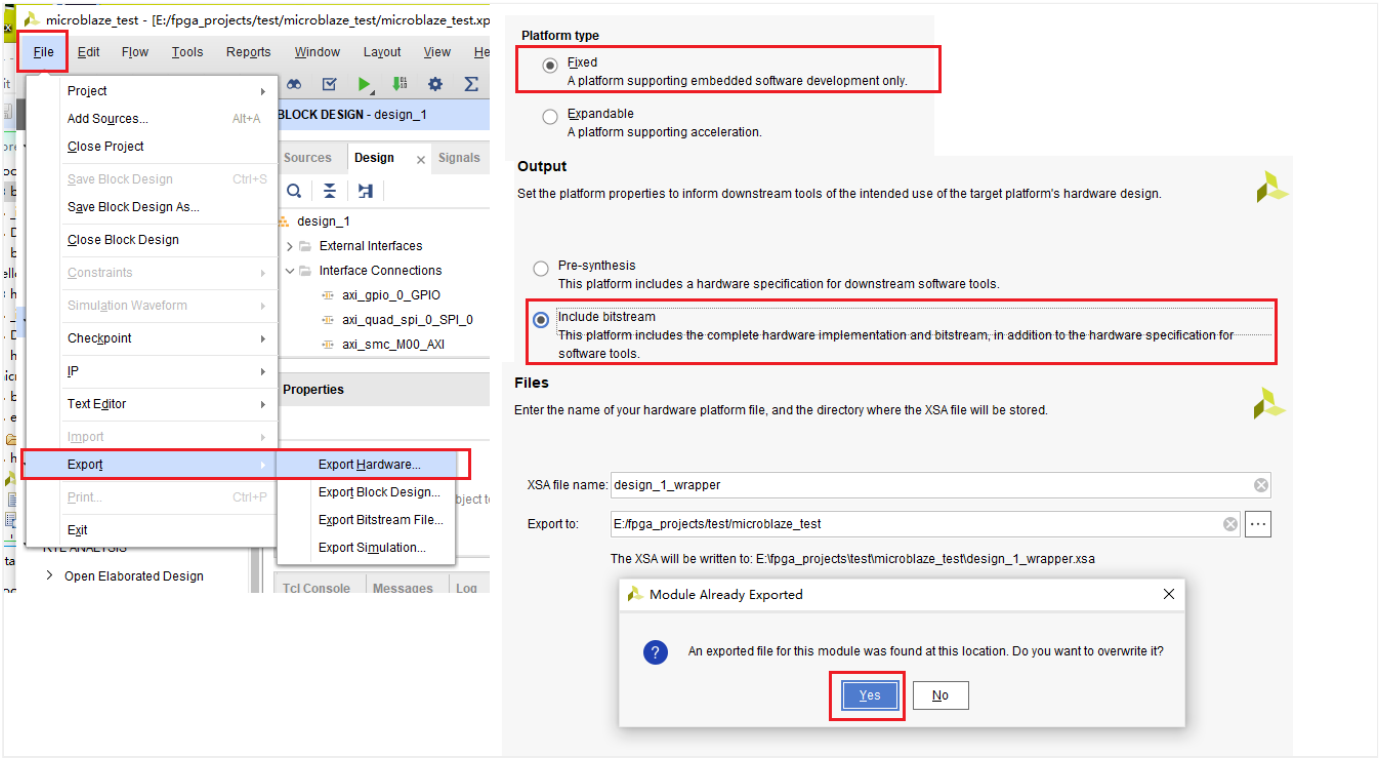
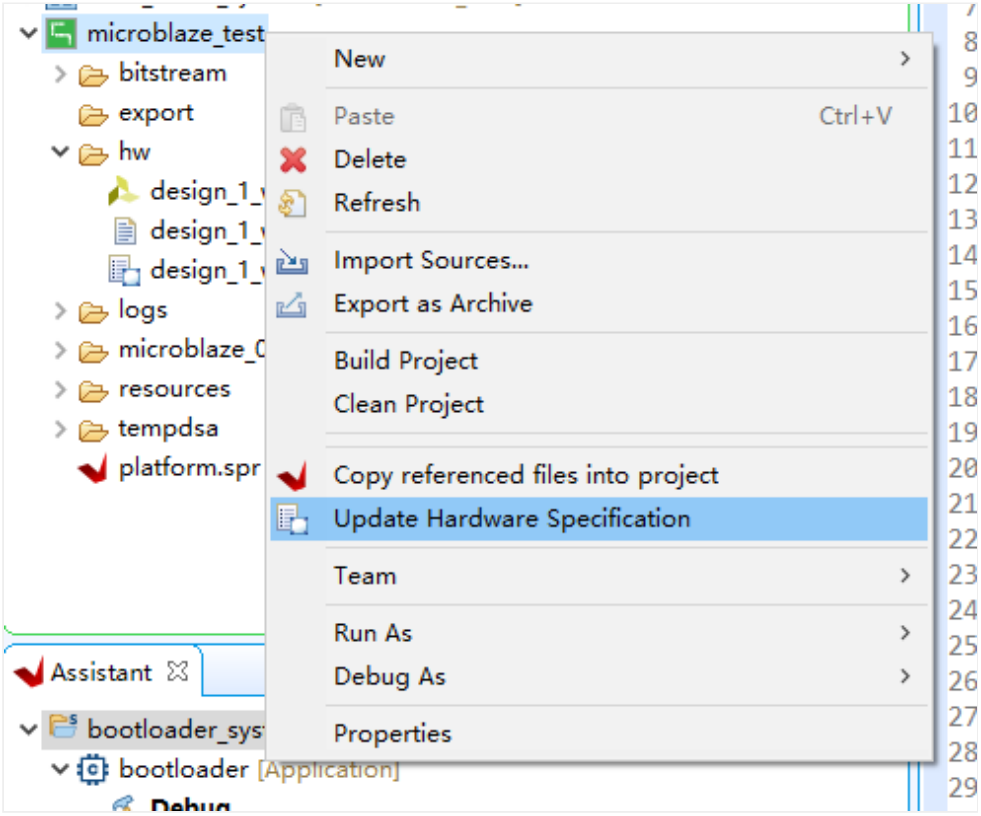
After generating the bit file, export the xsa file again:



Go back to Vitis and re-import the xsa file:



Take a closer look at the path of the xsa file here. Sometimes the path here is wrong and you need to select the correct file again.

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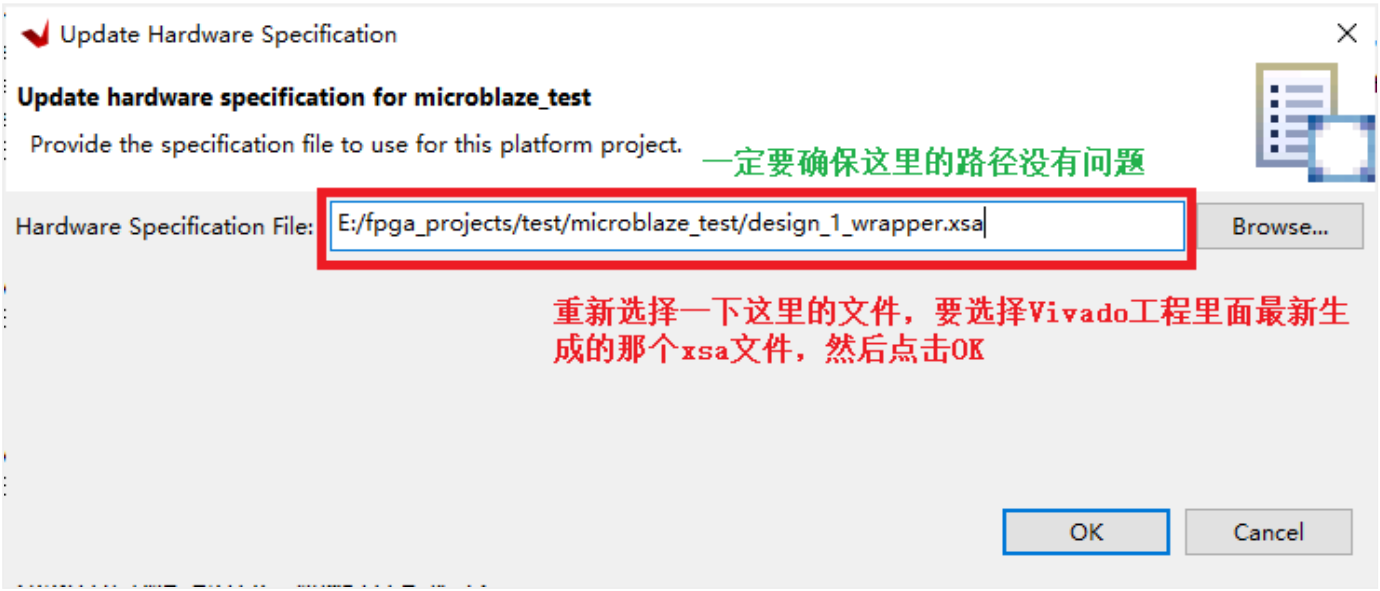
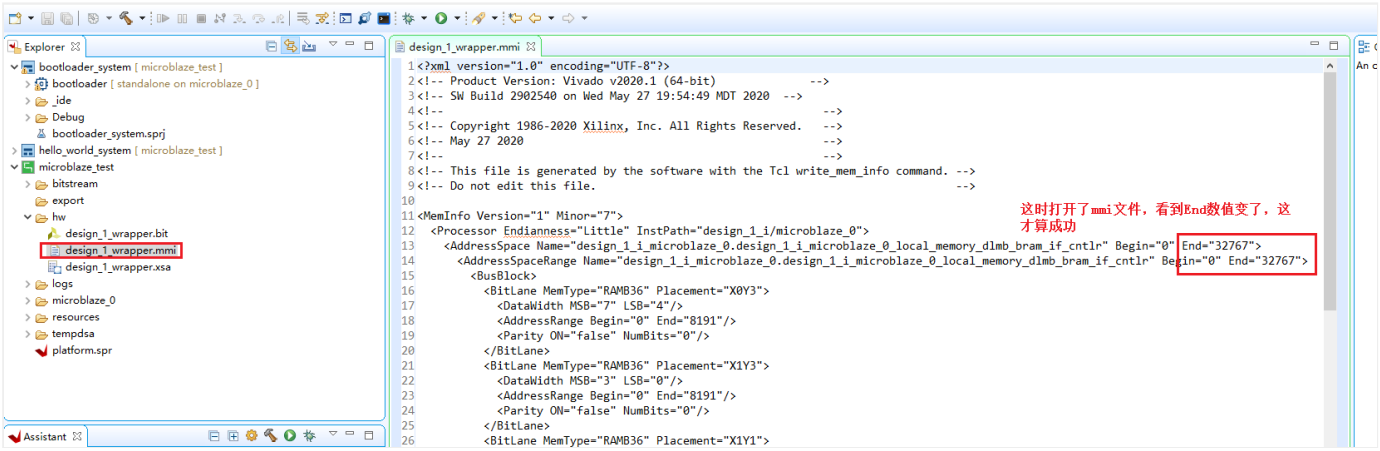
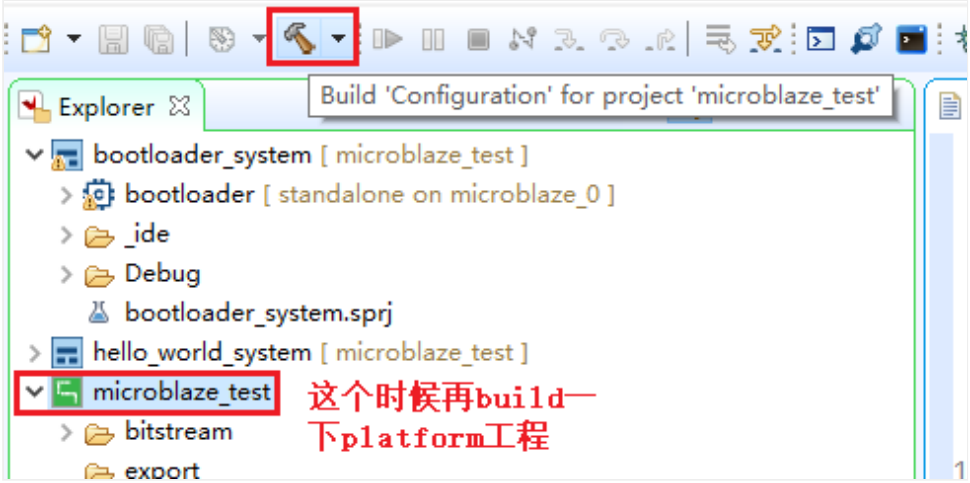


After clicking OK to close the dialog box, open the mmi file and take a look to see if the modified BRAM size really takes effect. If it does not take effect, the path of the xsa file you just selected is wrong.



After confirming that the size is correct, you must build the platform project (the green project) at this time.



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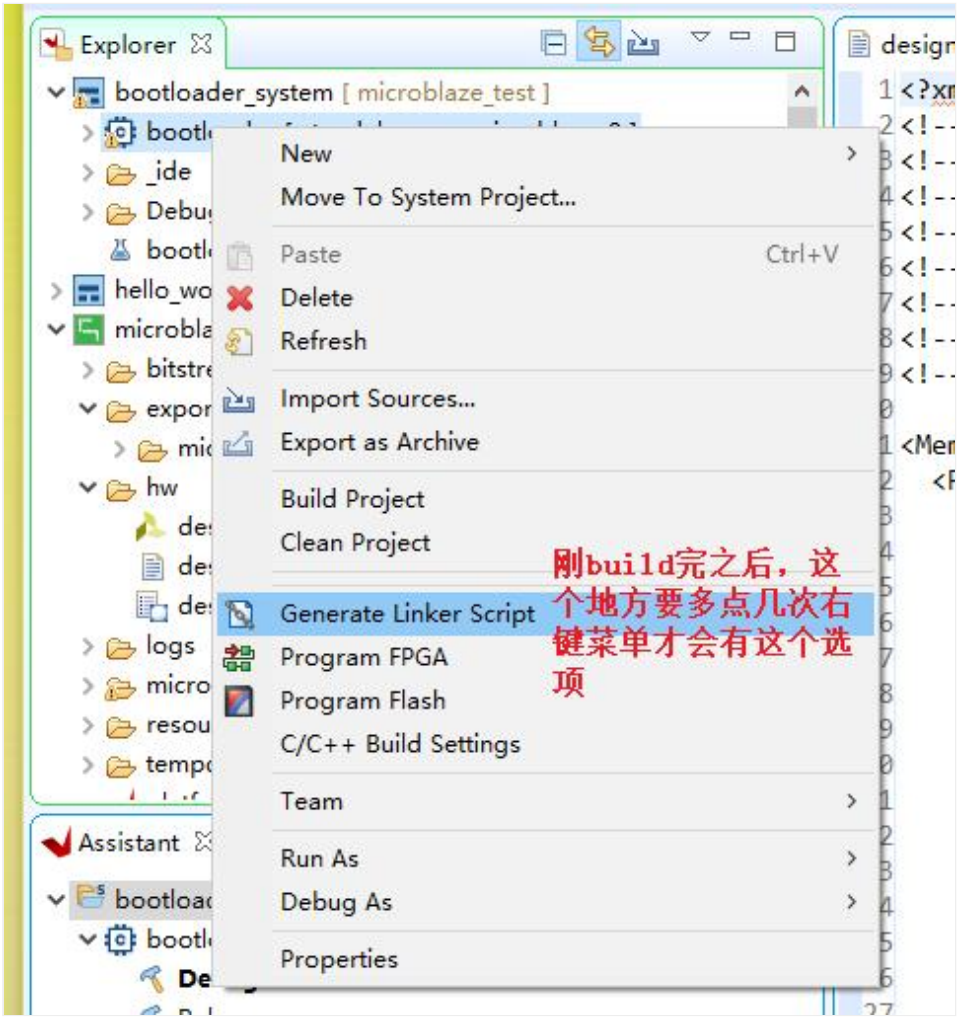
After the build is completed, check whether the BRAM size in the application project is effective. Here, the right-click menu usually pops up several times before the Generate Linker Script menu item comes out.



You can see that the size of BRAM has taken effect and has become 32KB. At this time, click the Generate button to update the lscript.ld file.

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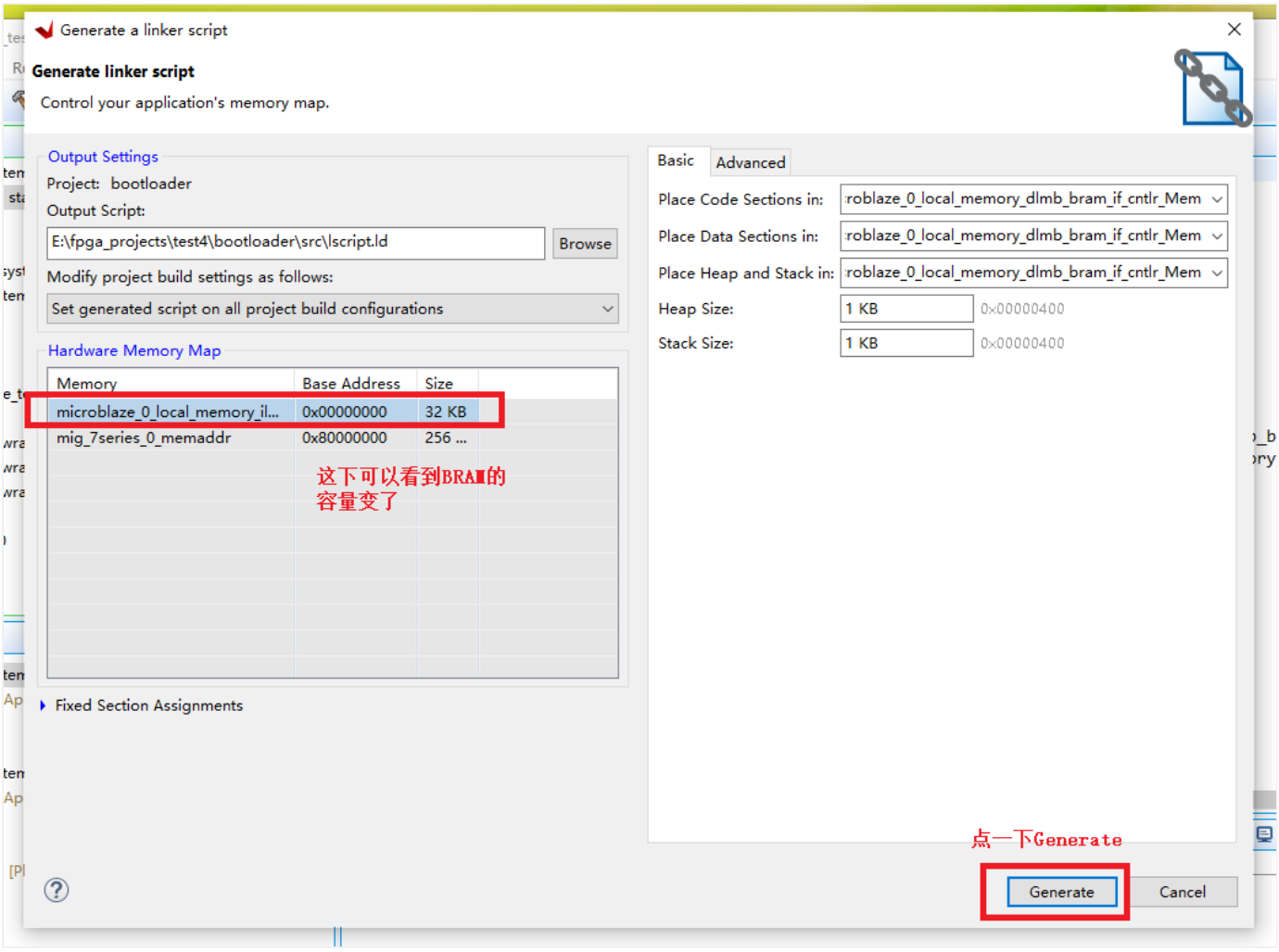

BRAM space is enough, the project can be compiled and passed:

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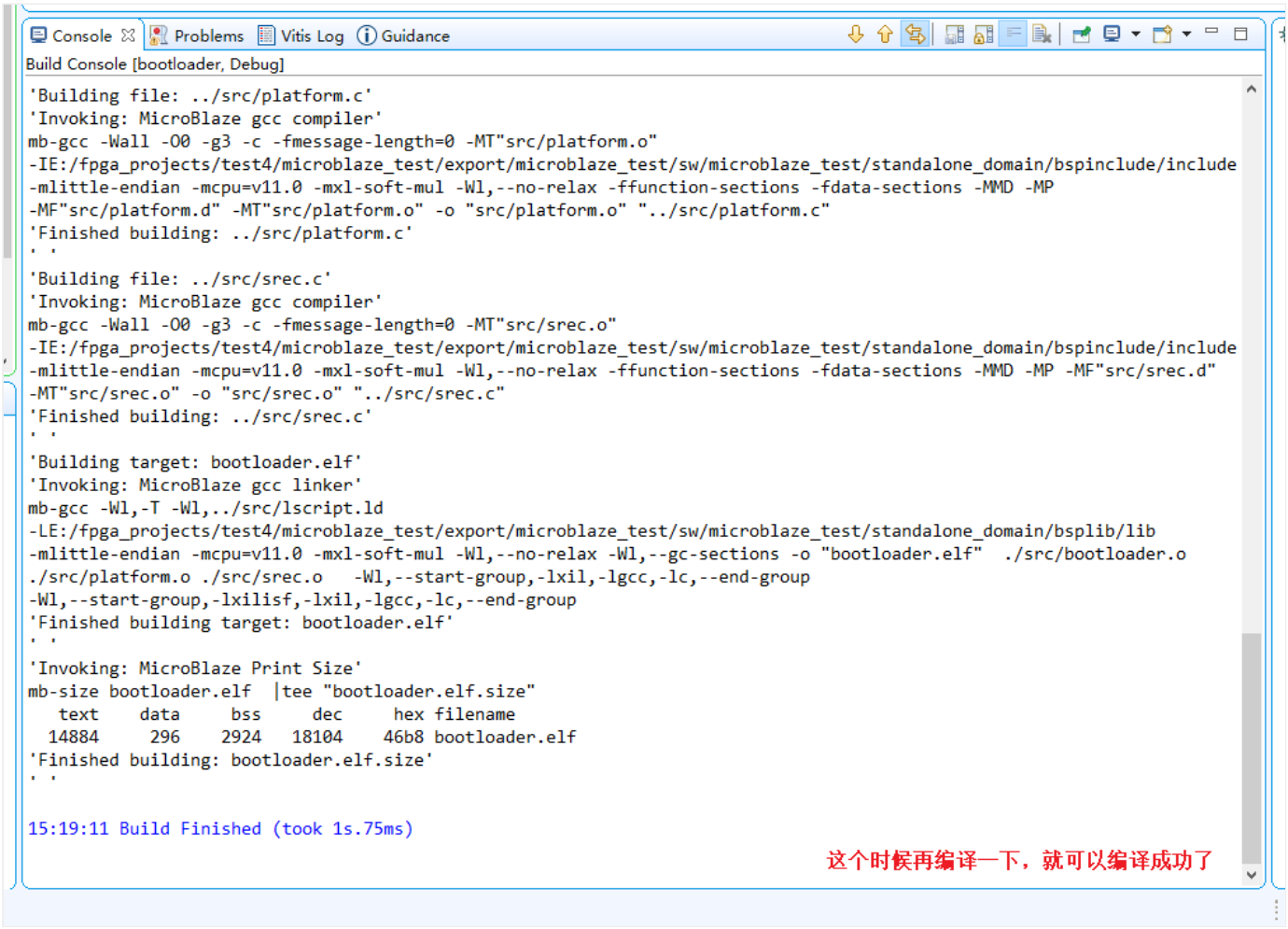

The above are the complete steps to modify the project BRAM size. As long as the above steps are wrong, the modification will be unsuccessful. The whole process is quite complicated.

Zabbix disk performance for use (the iostat) monitoring the linux

Intelligent Recommendation

Xilinx FPGA BRAM study notes

Chip model: XC7A100T Camera model: OV5640 Resolution: 320*240 BRAM type: single dual port bram The thing to do is to display the camera data on a VGA monitor. The solution is to first put the r...

C++--The size of the memory occupied by the structure

Structure occupied memory size In vs2010, use sizeof to display 80 bytes of memory occupied. The essence of the structure in memory size is: byte alignment The offset of each member of the structure r...

A JPG's memory size occupied in Android

2019 Unicorn Enterprise Heavy Recruitment Python Engineer Standard >>> A JPG file, is displayed, it is to be converted into Bitmap, then how much memory space is this BitAmp takes up? The fol...

Xilinx Vitis Petalinux installation and use

ubuntu16.04.6 Install Vitis, execute, According to the default settings, the desktop shortcut installation failed, it should be my Chinese version of ubuntu, the desktop shortcut installation error, j...

Xilinx Vitis Shortcut Binds and View

Shortcut key settings & views Learning to develop Zynq Ultrascale +, VITIS is numerous, and there are many shortcuts.

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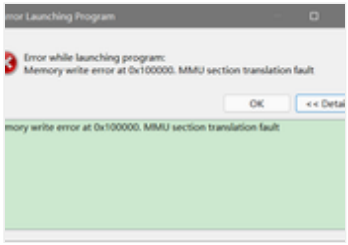
You can modify the shortcut key settings in Window-> Preferences-> Keys ...

More Recommendation

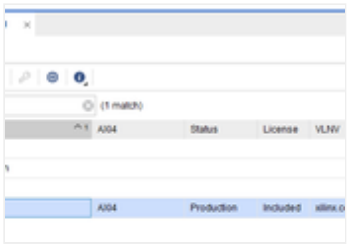
Install Vivado Vitis Petalinux 2020.1 on Ubuntu18.04

The latest version of the Xilinx tool has been updated to 2020.2, I installed 2020.1 mainly because Pynq latest version V2.6 support 2020.1, this year will do some Pynq related development. 1 New virt...



Xilinx Vitis Error Launching Program: Memory write error MMU section translation fault

An error is reported at Run As -> Launch Hardware (Single Application Debug (GDB)): Error while launching program: Memory write error at 0x100000. MMU section translation fault The reason is that t...



Xilinx 2020.1 MIG Nuclear Read Write DDR3 Memory, Configuring MIG Nucleus When New Engineering

This paper uses this chip in XC7A35TFGG484-2 as an example, using the MILE FPGA development board, drive DDR3 memory with MIG core. FPGA external crystal size is 50 MHz, the drive frequency of DDR3 me...

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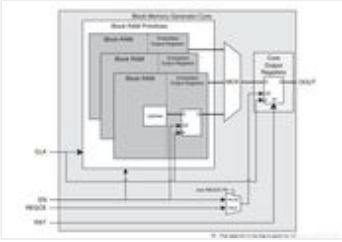

Xilinx BlockRam (Bram) structure and read logic interpretation

As shown in the figure, bram consists of a lot of blocks and registers of ram blocks, through the Mux data selector, the data is sent to the output register, and finally output. As can be seen from th...

Xilinx Bram IP core operating instructions

1. What is BRAM Search ram in vivado2018.3, configure IPcore according to the following figures, here first use simple dual-port ram, use native interface The configuration data width is 8 bits...

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