Artix_7A50T	
Avnet Engineering Services	
www.Artix50.org	
Function	Sheet Number
LEAD SHEET	1
BLOCK DIAGRAM	2
BANK 15 DDR3 Memory	3
USB, QSPI, SHA, I2C, EEPROM	4
BANK 14 DUAL ETHERNET, UART, GPIO	5
BANK 0, SMT2 JTAG, BOOT MODE	6
BANK 34 SWITCHES, LEDS	7
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Artix_7A50T

7 APR 2015

11:50:39 AM

AVNET Avnet Engineering Services		
Title: 01 - Avnet Lead Sheet_C.SchDoc		
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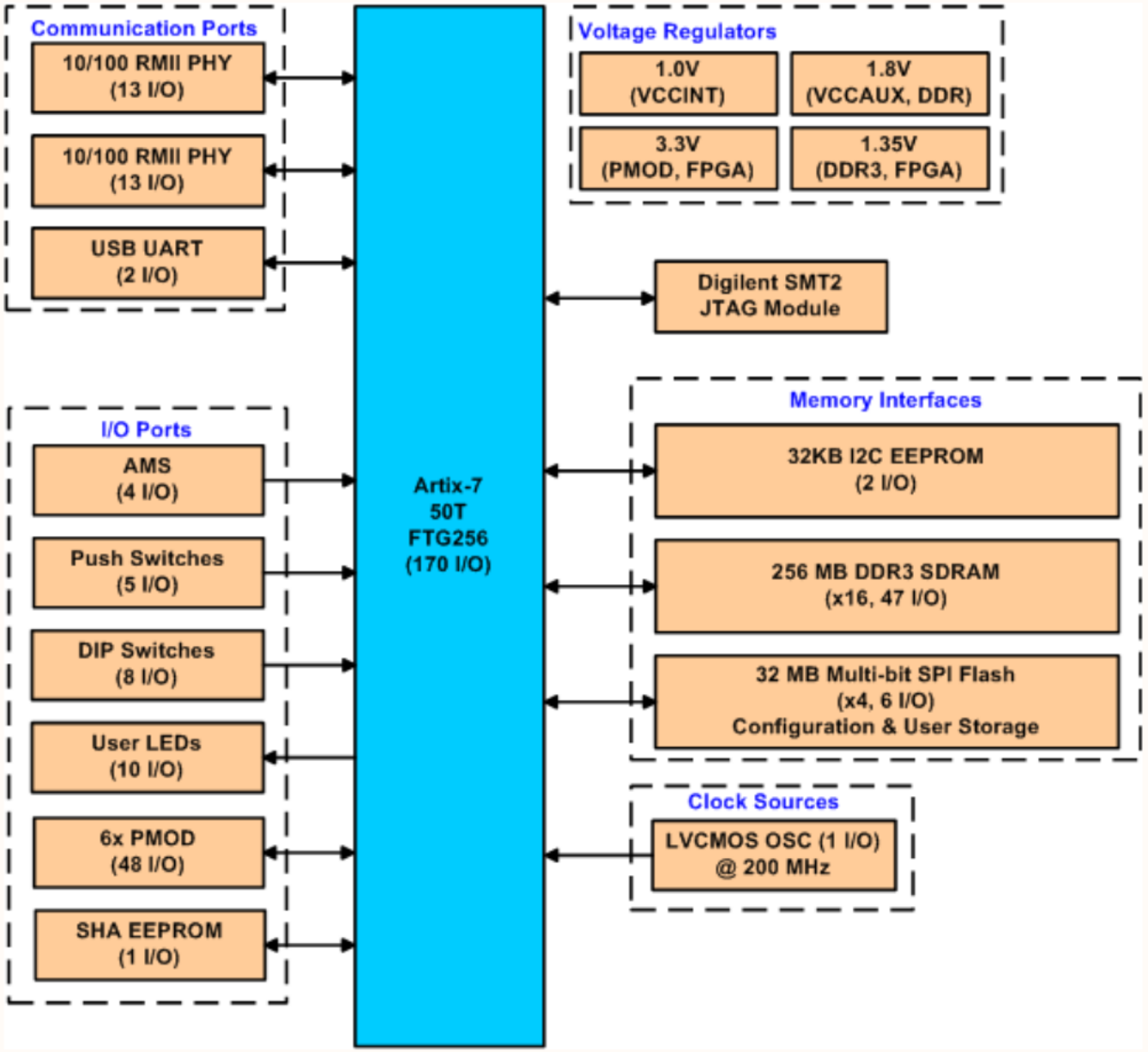
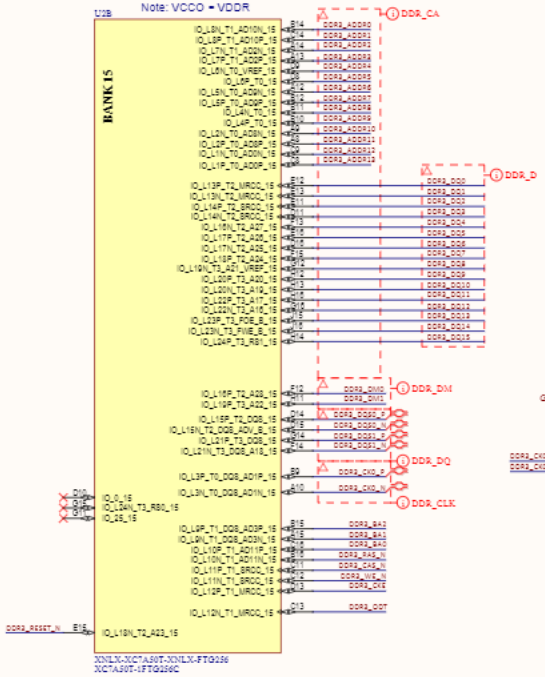
Date: 4/7/2015	Sheet 1 of 11	

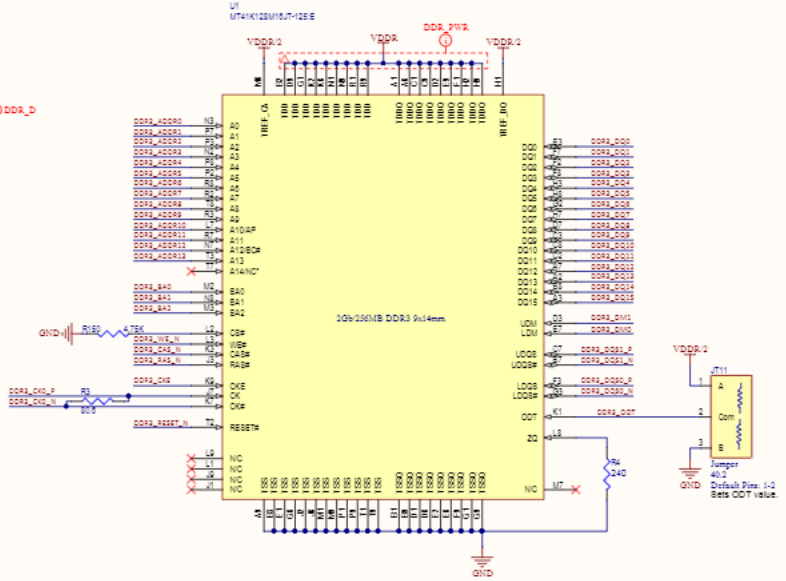
Topology

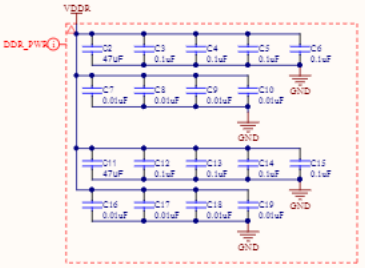


AVNET Avnet Engineering Services		
Title: 02 - Block Diagram.SchDoc		
Size: C	Project Name: Artix_7A50T	Rev: C
Date: 4/7/2015	Sheet 2 of 11	

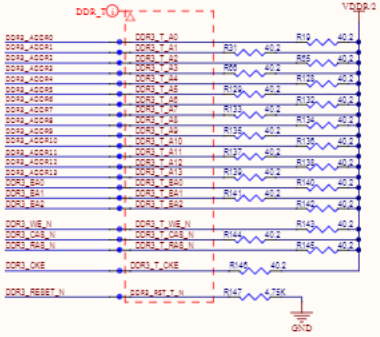


256MB DDR3 1600 MEMORY

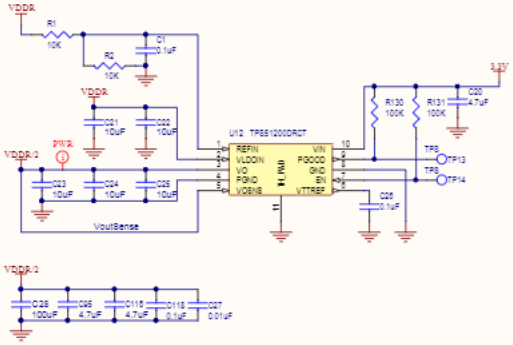




DDR3 ADDR & CNTRL TERMINATION RESISTORS



DDR3 TERMINATION REGULATOR



DDR3 single-ended traces are 40 Ohms impedance
DDR3 Differential traces are 80 Ohms differential impedance

All DDR RAM traces are matched length and less than 2540 mils (25 mm). The below information is general guidance and is pending the FR4 board material composition and stack up.

Address and command trace spacing is 10 mil min for short runs, 4 mils
clearance for parallel runs less than 500 mils.
Data trace spacing is 10 mil min for short runs, 4 mils clearance for parallel
runs less

AVNET Avnet Engineering Services		
Title: 03 - BANK 15 DDR3 Memory.SchDoc		
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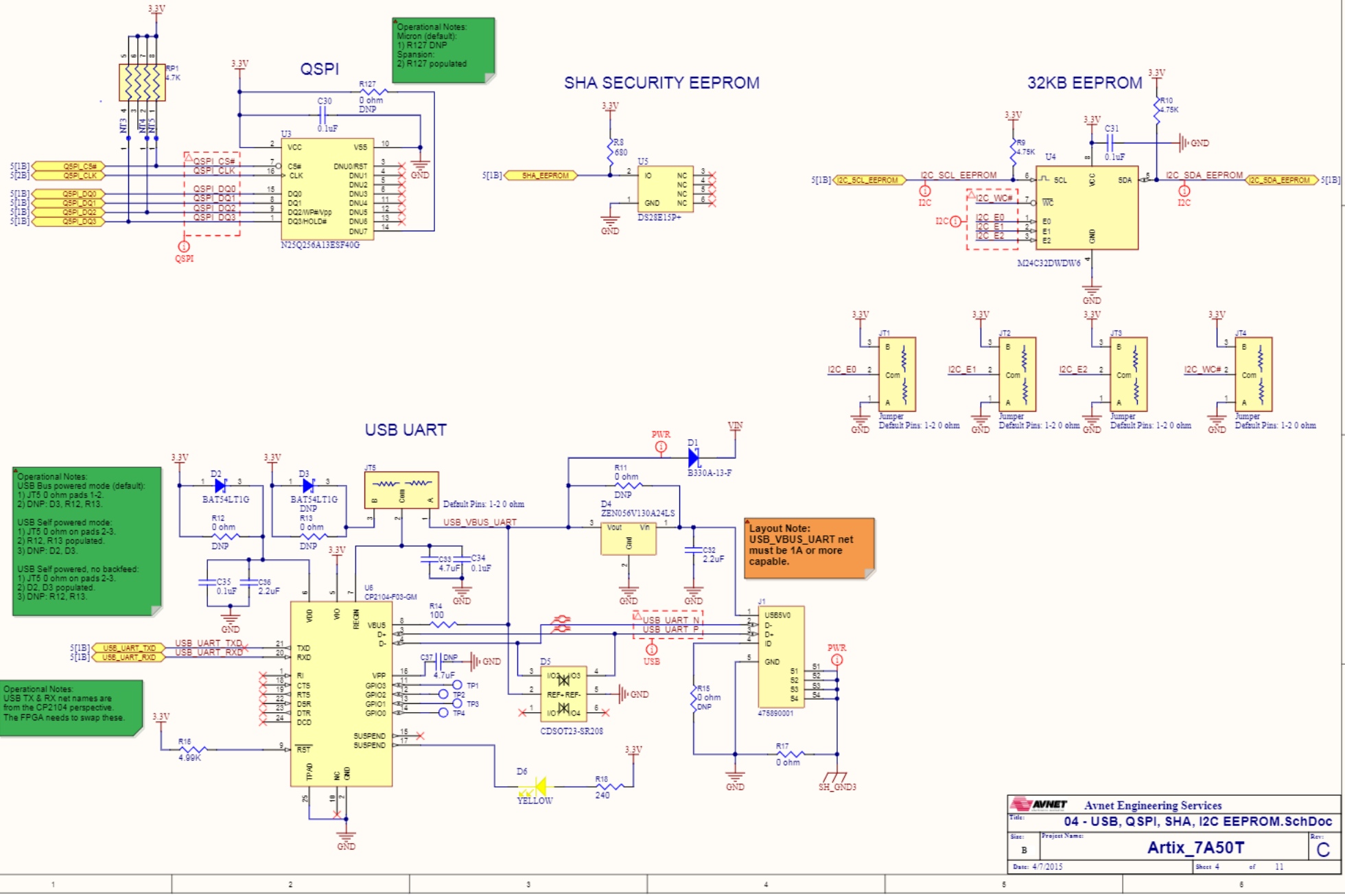
QSPI
SHA SECURITY EEPROM
32KB EEPROM
USB UART
Operational Notes:
Micron (default):
1) R127 DNP
Spansion:
2) R127 populated
N25Q256A13ESF40G
DS28E15P+
M24C32DWDW6
Operational Notes:
USB Bus powered mode (default):
1) JT5 0 ohm pads 1-2.
2) DNP: D3, R12, R13.
USB Self powered mode:
1) JT5 0 ohm on pads 2-3.
2) R12, R13 populated.
3) DNP: D2, D3.
USB Self powered, no backfeed:
1) JT5 0 ohm on pads 2-3.
2) D2, D3 populated.
3) DNP: R12, R13.
Operational Notes:
USB TX & RX net names are from the CP2104 perspective. The FPGA needs to swap these.
Layout Note:
USB_VBUS_UART net must be 1A or more capable.
CP2104-F03-GM
CDSOT23-SR208
Avnet Engineering Services
04 - USB, QSPI, SHA, I2C EEPROM.SchDoc
Artix_7A50T
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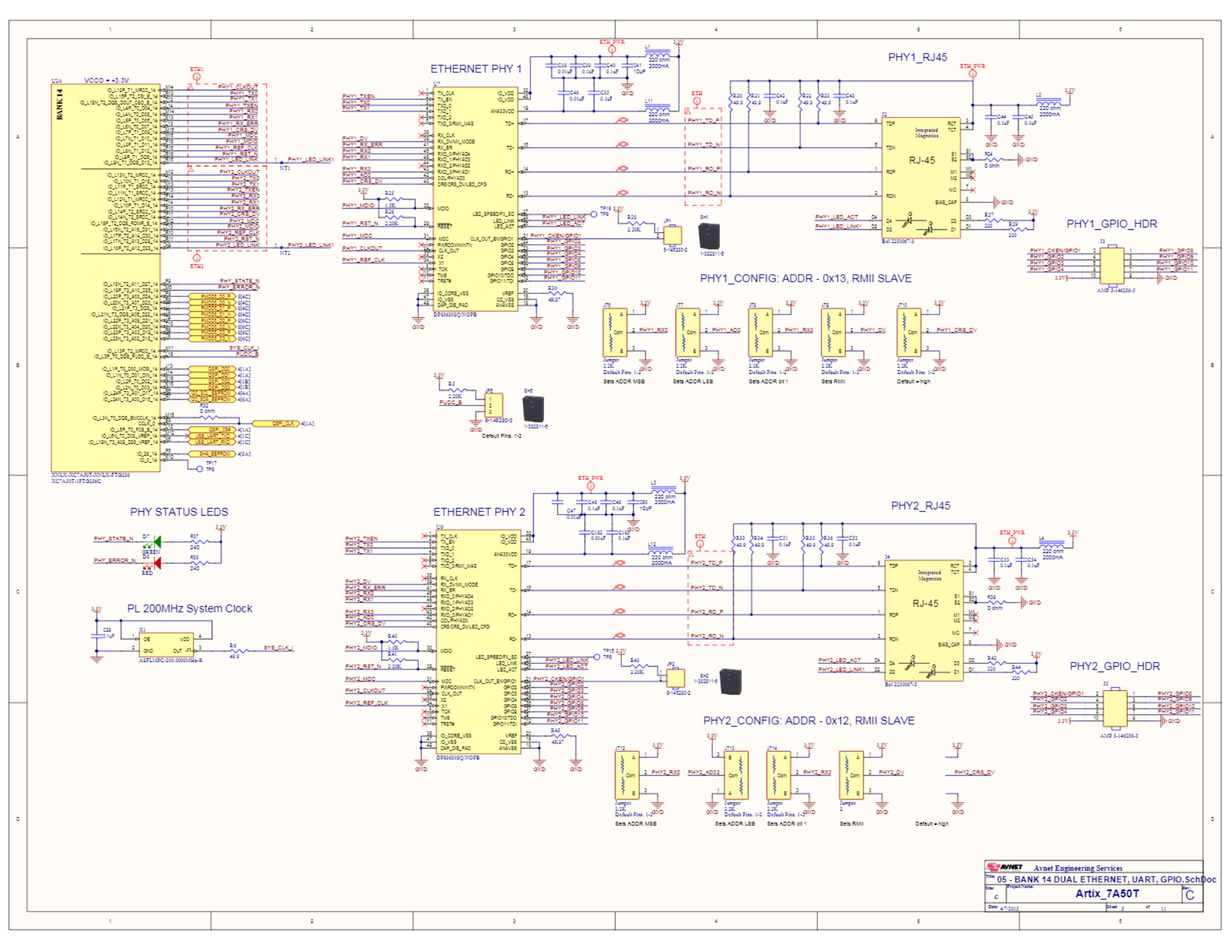
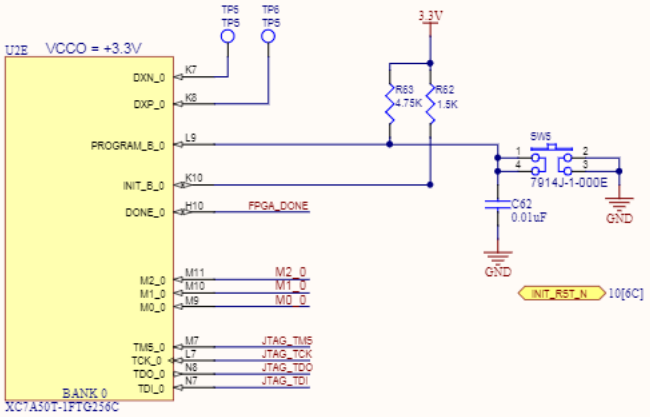
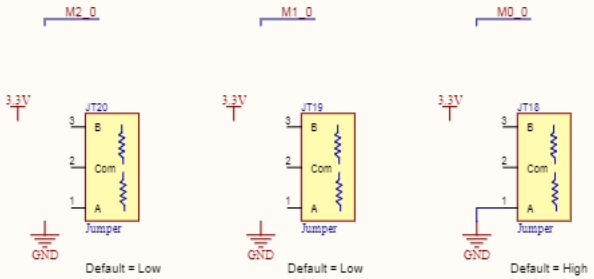

BANK 14
VCCO = +3.3V
XNLX-XC7A50T-XNLX-FTG256
XC7A50T-1FTG256C
ETHERNET PHY 1
PHY1_RJ45
PHY1_GPIO_HDR
PHY1_CONFIG: ADDR - 0x13, RMII SLAVE
ETHERNET PHY 2
PHY2_RJ45
PHY2_GPIO_HDR
PHY2_CONFIG: ADDR - 0x12, RMII SLAVE
PHY STATUS LEDS
PL 200MHz System Clock
RJ-45
Integrated Magnetics
DP83630SQ/NOPB
ASFLMPC-200.0000M-R
Sets ADDR MSB
Sets ADDR LSB
Sets ADDR bit 1
Sets RMII
Default = high
Avnet Engineering Services
05 - BANK 14 DUAL ETHERNET, UART, GPIO.SchDoc
Artix_7A50T

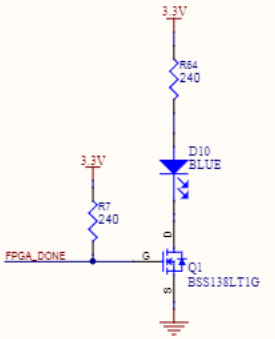
PROG_PB RESET



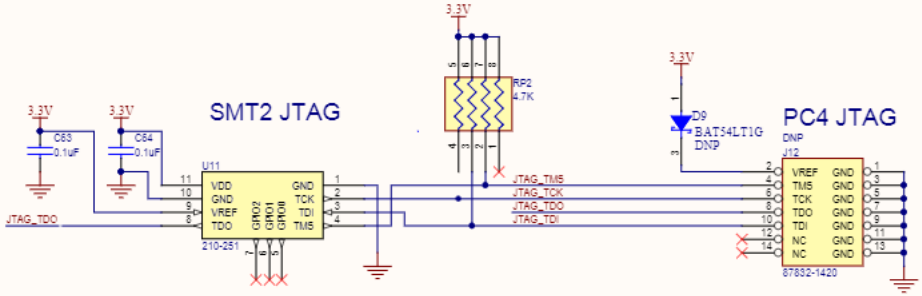
BOOT MODE SELECT



FPGA DONE LED



DUAL JTAG



Avnet Engineering Services	
Title: 06 - BANK 0, SMT2 JTAG, BOOT MODE.SchDoc	
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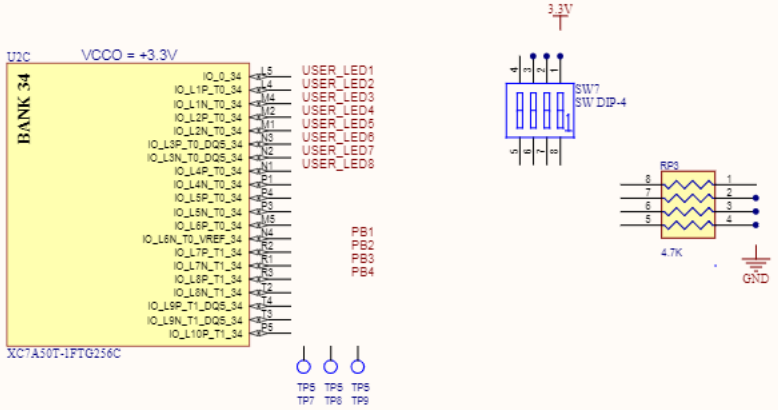
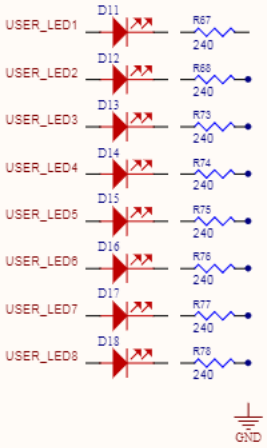
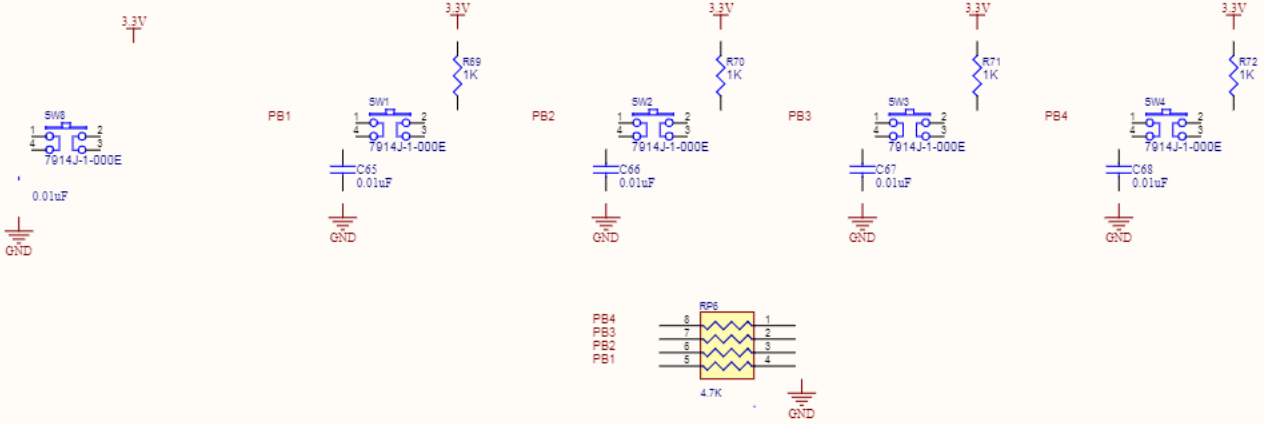
USER SLIDE SWITCHES



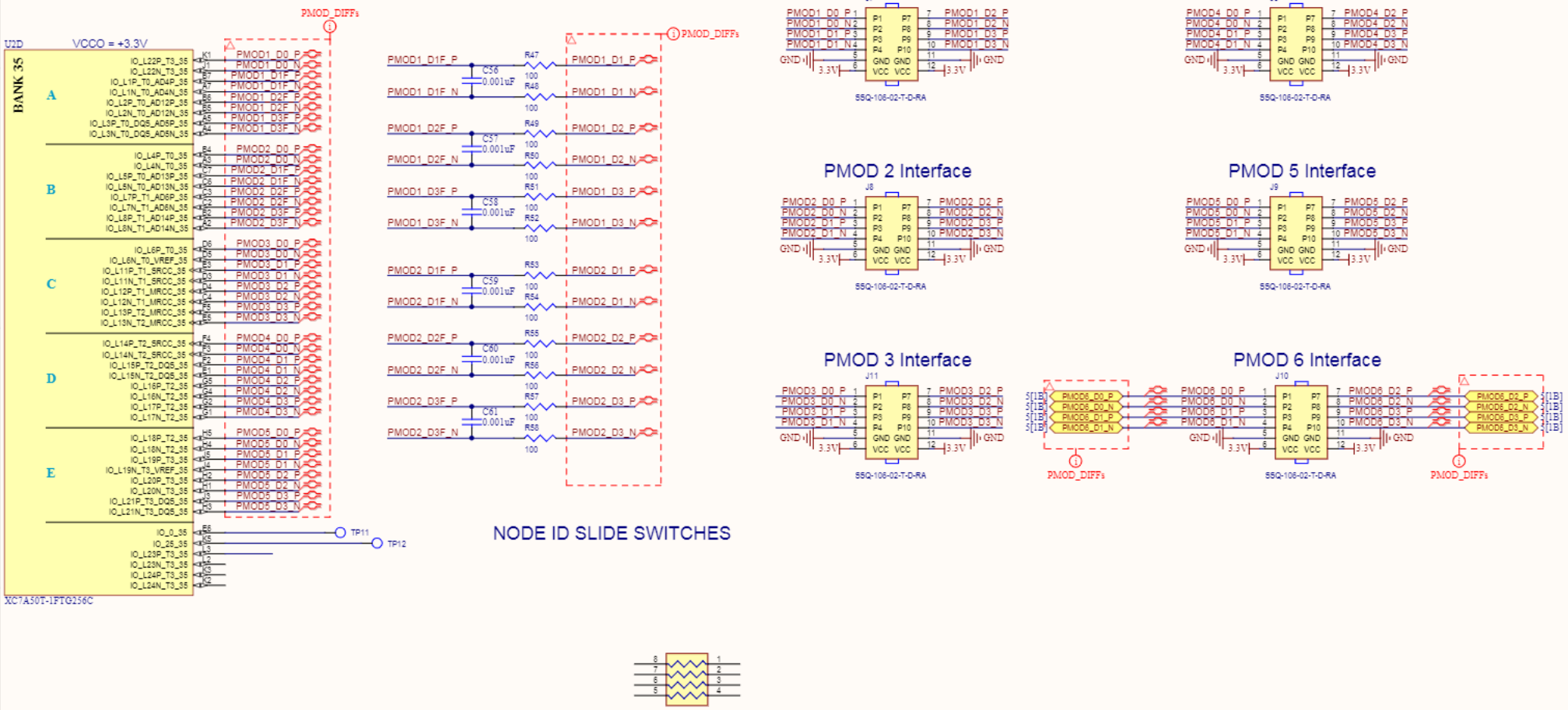
8 USER LEDS



USER_PUSH_BUTTONS



Avnet Engineering Services		
Title: 07 - BANK 34 SWITCHES, LEDs.SchDoc		
Size: B	Project Name: Artix_7A50T	Rev: C
Date: 4/7/2015	Sheet 7 of 11	



Title:	08 - BANK 35 PMOD Interfaces.SchDoc
Size: B	Project Name: Artix_7A50T
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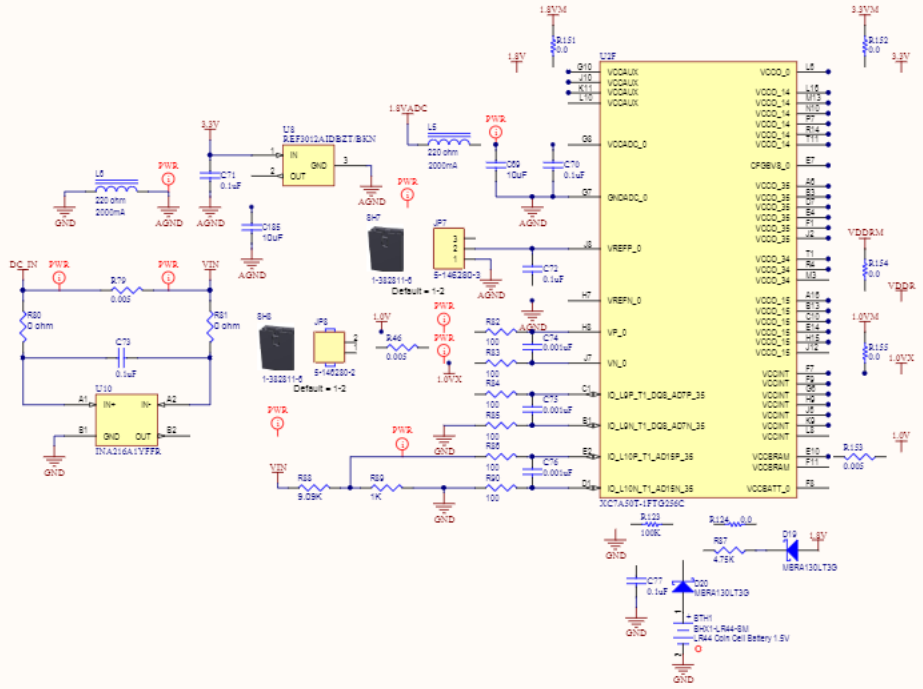
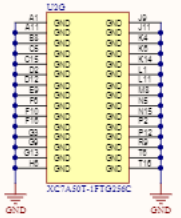
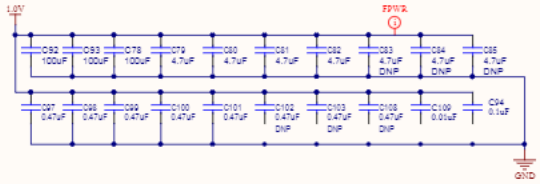
Avnet Engineering Services

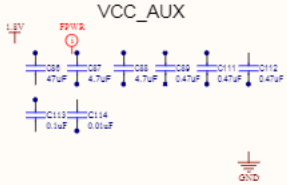




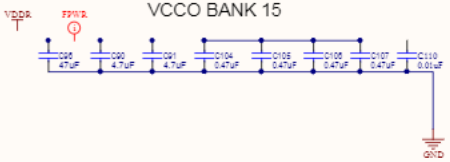
VCCINT



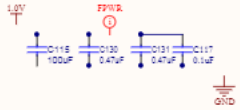
VCC_AUX



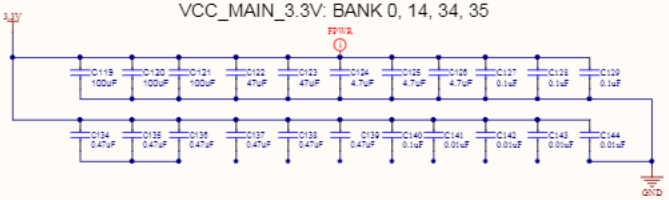
VCCO BANK 15



VCC_BRAM



VCC_MAIN_3.3V: BANK 0, 14, 34, 35



AVNET Avnet Engineering Services		
Title: 09 - FPGA POWER.SchDoc		
Size: C	Project Name: Artix_7A50T	Rev: C
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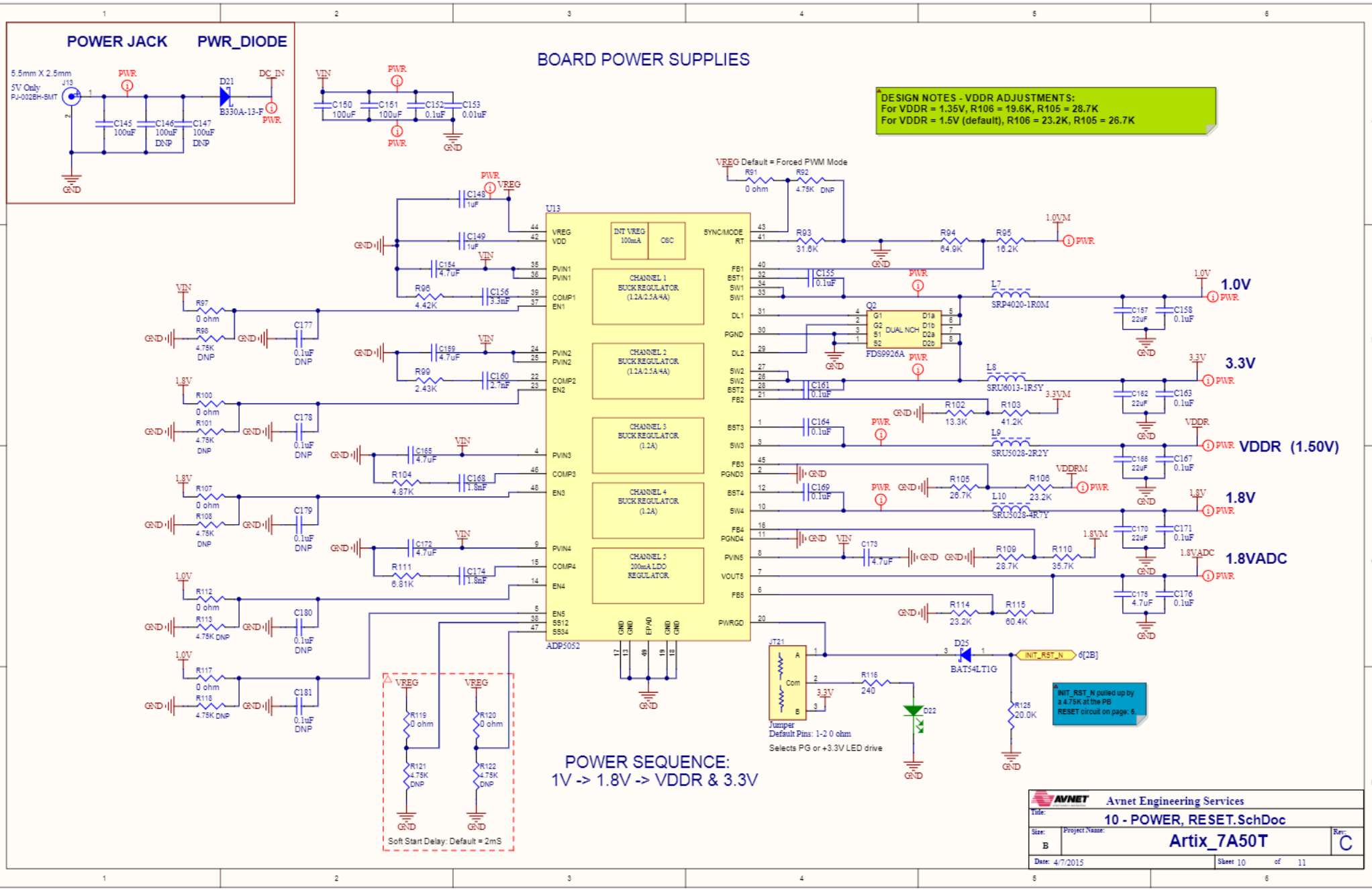
POWER JACK
PWR_DIODE
5.5mm X 2.5mm
5V Only
PJ-002BH-SMT
J13
D21
B330A-13-F
DC_IN
PWR
GND
C145 100uF
C146 100uF DNP
C147 100uF DNP
C150 100uF
C151 100uF
C152 0.1uF
C153 0.01uF
VIN
BOARD POWER SUPPLIES
DESIGN NOTES - VDDR ADJUSTMENTS:
For VDDR = 1.35V, R106 = 19.6K, R105 = 28.7K
For VDDR = 1.5V (default), R106 = 23.2K, R105 = 26.7K
VREG Default = Forced PWM Mode
U13
ADP5052
INT VREG 100mA
OSC
CHANNEL 1 BUCK REGULATOR (1.2A/2.5A/4A)
CHANNEL 2 BUCK REGULATOR (1.2A/2.5A/4A)
CHANNEL 3 BUCK REGULATOR (1.2A)
CHANNEL 4 BUCK REGULATOR (1.2A)
CHANNEL 5 200mA LDO REGULATOR
VREG
VDD
PVIN1
COMP1
EN1
PVIN2
COMP2
EN2
PVIN3
COMP3
EN3
PVIN4
COMP4
EN4
EN5
SS12
SS34
SYNC/MODE
RT
FB1
BST1
SW1
DL1
PGND
DL2
SW2
BST2
FB2
BST3
SW3
FB3
PGND3
BST4
SW4
FB4
PGND4
PVIN5
VOUT5
FB5
PWRGD
EPAD
1.0V
1.0VM
3.3V
3.3VM
VDDR
VDDRM
1.8V
1.8VM
1.8VADC
L7 SRP4020-1R0M
L8 SRU6013-1R5Y
L9 SRU5028-2R2Y
L10 SRU5028-4R7Y
Q2 DUAL NCH
FDS9926A
JT21
Jumper
Default Pins: 1-2 0 ohm
Selects PG or +3.3V LED drive
D25
BAT54LT1G
INIT_RST_N
6[2B]
INIT_RST_N pulled up by a 4.75K at the PB RESET circuit on page: 6.
POWER SEQUENCE:
1V -> 1.8V -> VDDR & 3.3V
Soft Start Delay: Default = 2mS
AVNET
Avnet Engineering Services
Title:
10 - POWER, RESET.SchDoc
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Mechanicals:

PCB
A7MB-7A50T-PCB-B

PCB Mounting Holes

MTG1
0
MOUNTING HOLE 125mi

MTG4
0
MOUNTING HOLE 125mi

Avnet Engineering Services		
Title: 11 - Back Page.SchDoc		
Size: B	Document Number: Artix_7A50_C.PrjPcb	Rev: C
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