ProgrammerSought



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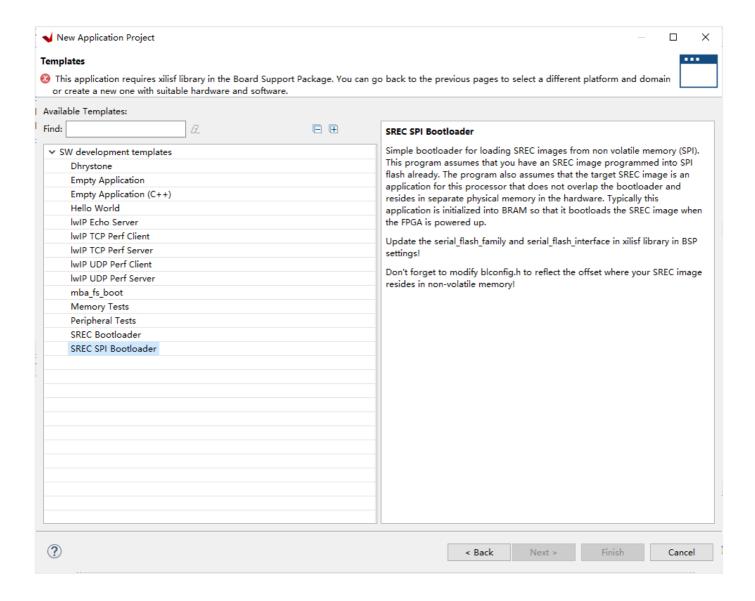
Xilinx Vitis 2020.1 cannot create SREC SPI Bootloader projec t, prompting the solution of lack of Xilisf library

tags: FPGA Xilinx Vitis Vivado SREC

[Error message]

This application requires xilisf library in the Board Support Package. You can go back to the previous pages to select a different platform and domain or create a new on Top

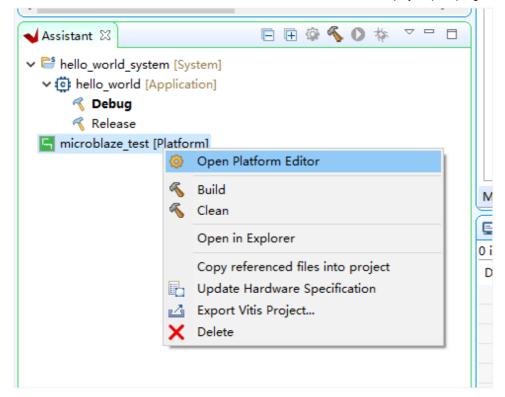
with suitable hardware and software.



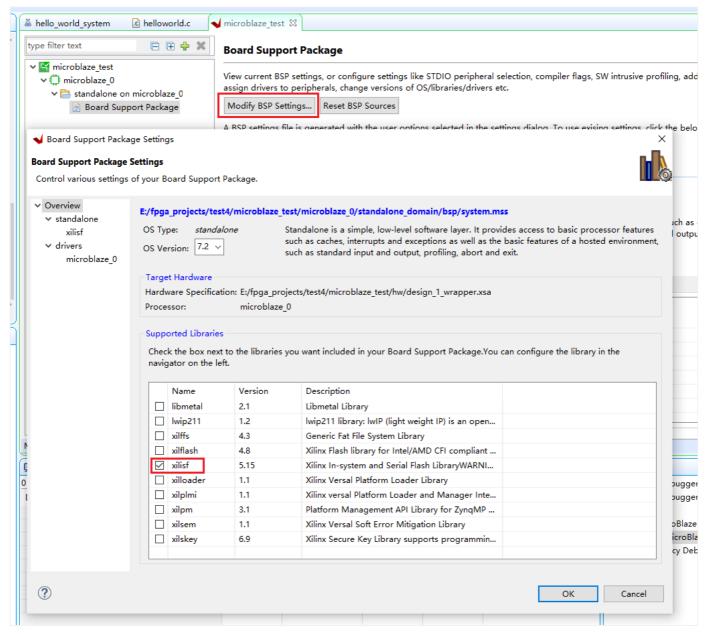
[Solution]

In the BSP settings, manually add a reference to the xilisf library.

First, click the right mouse button on the Platform project (here, microblaze_test) and select the "Open Platform Editor" command.



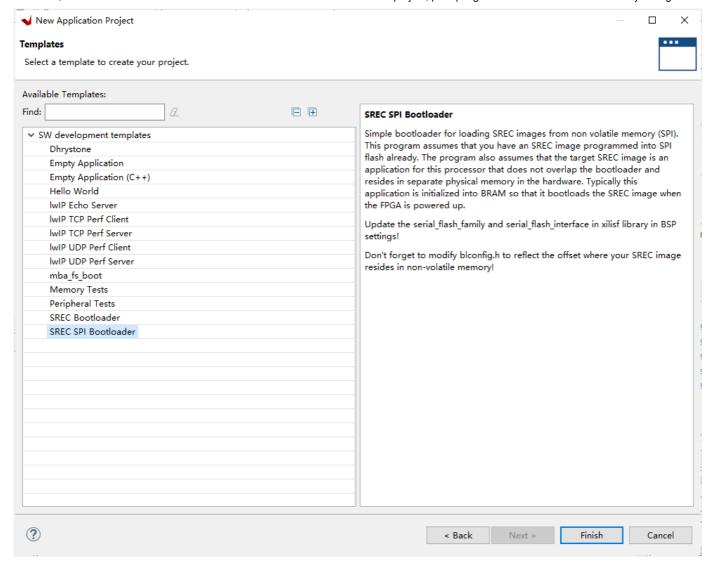
In the Board Support Package, click the Modify BSP Settings button, check the xilisf check box, and then click OK.



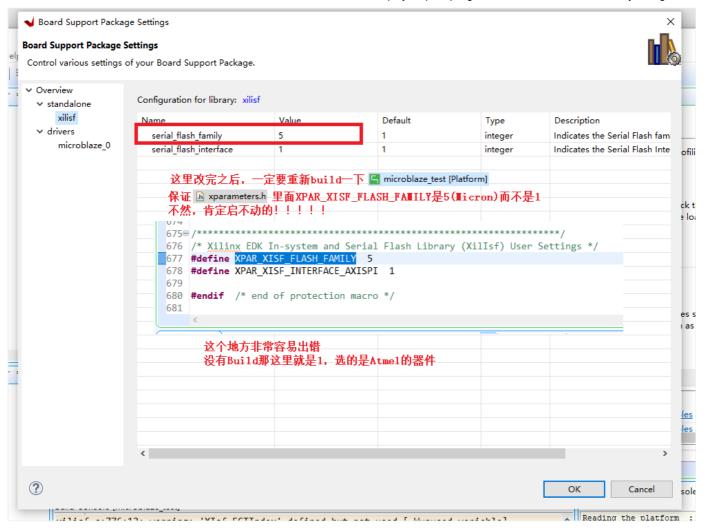
After checking, be sure to remember to Build Platform Project, otherwise the setting will not take effect!



Now you can successfully create the SREC SPI Bootloader project:



After creating the project, we need to modify the serial_flash_family number. After the modification, you must build the platform project again, otherwise the settings will not take effect, XPAR_XISF_FLASH_FAMILY in xparameters.h is still 1. Debugging the bootloader project will find that he entered the ATMEL branch and made an error.



After the modification is completed, compiling the SREC project will find that the compilation fails, indicating that the BRAM space is insufficient:

'Invoking: MicroBlaze gcc linker'
mb-qcc -Wl,-T -Wl,../src/lscript.ld -

LE:/fpga_projects/test4/microblaze_test/export/microblaze_test/sw/microblaze_t est/standalone_domain/bsplib/lib -mlittle-endian -mcpu=v11.0 -mxl-soft-mul -Wl,--no-relax -Wl,--gc-sections -o "bootloader.elf" ./src/bootloader.o ./src/platform.o ./src/srec.o -Wl,--start-group,-lxil,-lgcc,-lc,--end-group -Wl,--start-group,-lxilisf,-lgcc,-lc,--end-group

c:/xilinx/vitis/2020.1/gnu/microblaze/nt/x86_64-oesdk-mingw32/usr/bin/microblaze-xilinx-elf/../../libexec/microblaze-xilinx-elf/g.c/microblaze-xilinx-elf/g.2.0/real-ld.exe: bootloader.elf section `.stack' will not

fit in region

`microblaze_0_local_memory_ilmb_bram_if_cntlr_Mem_microblaze_0_local_memory_dlmb_bram_if_cntlr_Mem'

c:/xilinx/vitis/2020.1/gnu/microblaze/nt/x86_64-oesdk-

mingw32/usr/bin/microblaze-xilinx-elf/../../libexec/microblaze-xilinx-

elf/gcc/microblaze-xilinx-elf/9.2.0/real-ld.exe: region

`microblaze_0_local_memory_ilmb_bram_if_cntlr_Mem_microblaze_0_local_memo

ry_dlmb_bram_if_cntlr_Mem' overflowed by 744 bytes

collect2.exe: error: ld returned 1 exit status

'Finished building target: bootloader.elf'

At this time, we have to go back to Vivado and increase the BRAM space of Microblaze.

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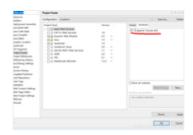
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Golang tcp forwarding remoteAddr error

Intelligent Recommendation

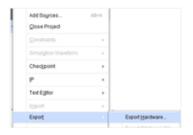


eclipse ----- The solution to the lack of To mcat library package in web project

Select the project-right click-properties-select project facetsselect Apache Tomcat-apply in the Runtimes option on the right side of the window and click OK to add the Tomcat library package to the ...

Solve 2020.1 Idea Create a problem in the Spring project

Solve 2020.1 Idea Create a problem in the Spring project During this time, after the influence of a theoretical knowledge, it began the construction of the Spring project. But the programmed path is a...



Vivado quickly create a Vitis project (no ne ed to create a Platform Project)

Most of the Internet is to create a Platform Project and then create Application Projet, and then import the platform files in Application Projet. In fact, an easy way is to directly create

Applicatio...

Xilinx Vitis Petalinux installation and use

ubuntu16.04.6 Install Vitis, execute, According to the default settings, the desktop shortcut installation failed, it should be my Chinese version of ubuntu, the desktop shortcut installation error, j...



Xilinx Vitis Shortcut Binds and View

Shortcut key settings & views Learning to develop Zynq Ultrascale +, VITIS is numerous, and there are many shortcuts. You can modify the shortcut key settings in Window-> Preferences-> Keys ...

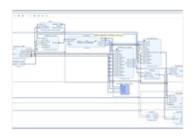
More Recommendation



Install Vivado Vitis Petalinux 2020.1 on Ubu ntu18.04

The latest version of the Xilinx tool has been updated to 2020.2, I installed 2020.1 mainly because Pynq latest version V2.6 support 2020.1, this year will do some Pynq related

development. 1 New virt...



vivado SPI bootloader bootloader creation

introduction Generally speaking, Xilinx Microblaze will be used to do some auxiliary work of control classes and simple interfaces in the system, such as running low-speed interface drivers such as II...

FreeRTOS OpenAmp uses the project created by Vitis, and the task cannot be dispatched

Frertos OpenAmp uses the project created by Vitis, and the task cannot be scheduled. FreeRTOS Openamp uses the project created by Vitis. In the task, VTASKDELAY (1000) is directly stuck and cannot be ...



The solution to the lack of dependencies in the Maven project

I just started to learn the framework recently, and every time I configure it in the pom.xml file, the corresponding file will not appear in the "External Libraries" on the left. Having been...

Solution for prompting that WordPress cannot connect to F TP server

TOP

In the past few days when building the main station, I could not connect to the FTP server when updating wordpress The solution is as follows: inWordPressFound under the directorywp-config.phpEdit the...

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 the Hello World C language program (do not use external DDR3 memory), and
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- Xilinx Vitis 2020.1 method to modify the size of BRAM memory occupied by the project
- [Tutorial] Xilinx Vivado / Vitis 2020.1 Create a MicroBlaze project to run the Hello World C language program (using external DDR3 memory)
- Xilinx vitis unsweefence solution when starting
- Xilinx Vitis
- Questions about the Sleep function card of the MicroBlaze soft core in Xilinx
 VITIS 2020.1

- I can't find MicroBlaze_0 when running a C program in Xilinx Vitis 2020.1
- Solve the problem that Xilinx Vitis IDE 2019.2 cannot start
- The AXI Interrupt Controller in Xilinx Vivado 2020.1 cannot select the number of interrupts

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tm use Coast

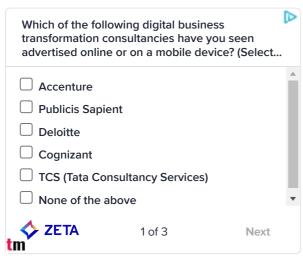
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