Vivado Board Definition Files
For the
Artix-7 50T Evaluation Board

Vivado version 2014.2
Document version 1.0
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AVNET electronics marketing

Table of Contents

Introduction

This document describes installing the Vivado board definition files for the 7A50T Evaluation board so that the board appears in the menu list of available target boards when creating a new Vivado project.

Objectives

This tutorial will demonstrate the following with the supplied files.

- Installation of the board definition files into the proper Vivado folder in your installation of the Vivado tools.
- Use of the board definition files ot create a new Vivado project targeting the 7A50T Evaluation board.

Installation Requirements

The following items are required for proper completion of this install guide.

Software

The software requirements for this reference design are:

- Linux, Windows XP, Windows 7, Windows 8.1 (ug973-vivado-release-notes-install-license.pdf)
- Xilinx Vivado Design Edition software
    - Version 2014.2 is used for this design

Hardware

The hardware setup used by this reference design includes:

- Computer with 1 GB RAM and 1 GB virtual memory (recommended) (www.xilinx.com/design-tools/vivado/memory.htm)
- Avnet Artix-7 50T Evaluation board Kit
    - Avnet Artix-7 50T Evaluation board
    - USB-A to USB-micro B cables (UART and JTAG)

Supplied Files

The following directory structure is included with this reference design:

board_xml: Contains the folder of board definition files to be copied to the Vivado install folders.

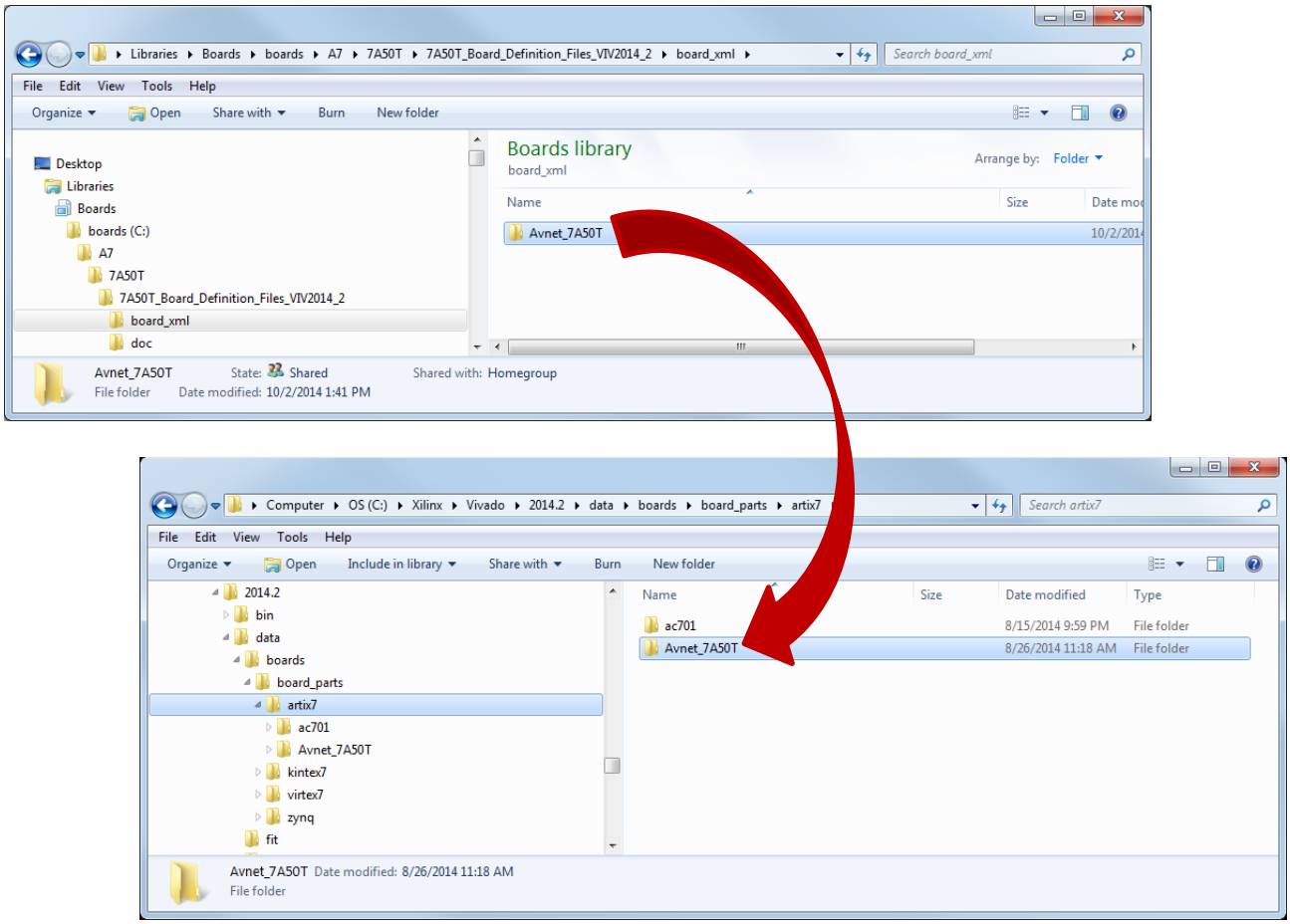
doc: Contains documentation for this design:
7A50T_Board_Definition_Files_Install_Notes_VIV2014_2_v1_0.pdf: This document.

xdc: Contains the master constraints file for the Rev. A 7A50T Evaluation board.
7A50T_Master_XDC_PCB_Rev_A_v1_0.xdc

Installation of Board XML Files

Many Avnet evaluation boards can now be targeted directly in the Xilinx Vivado tools. This greatly simplifies the task of building the MicroBlaze processor system and integrating system peripherals and board interfaces into your own custom designs. Follow the instructions below to install the board XML files for the 7A50T board into your Vivado 2014.2 installation folders:

1. Using Windows Explorer, copy the **Avnet_7A50T** folder from the **<installation>\board_xml** folder to **<Vivado_install>\Xilinx\Vivado\2014.2\data\boards\board_parts\artix7**:



Known Issues

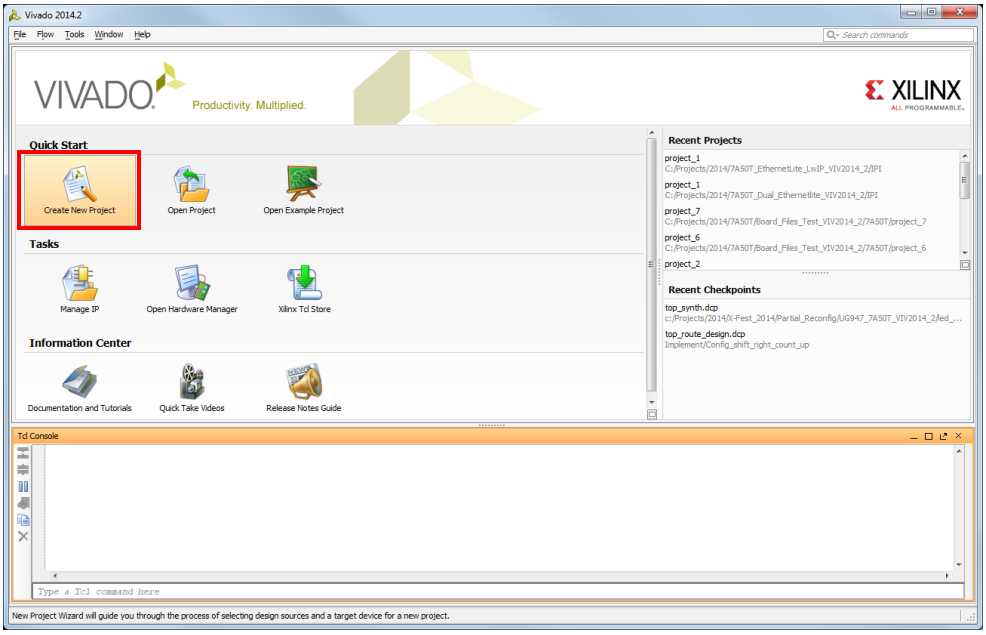
There are some known issues with the board XML files for the 7A50T board when creating a design from scratch for the 7A50T Evaluation board:

- Double-clicking on 'ddr3_sdram' in the 'Board Part Interfaces' tab instantiates MIG for the DDR3 interface, but the 'sys_rst' and 'sys_clk' interfaces do not get connected correctly. The 'sys_rst' does not get connected at all, and MIG creates an external port called 'sys_clk_i' instead of connecting to the 'sys_clk'. The user must manually connect the 'sys_rst' using 'Run Connection Automation' and manually change the 'sys_clk_i' to 'sys_clk' and change the frequency in 'External Port Properties'.
- The 'eth<0|1>_mdio' interfaces are always grayed-out in the 'Board Part Interfaces' tab, but will be connected when 'Run Connection Automation' is selected for the axi_ethernetlite instances.
- The 'eth<0|1>_phy_rst_n' interfaces in the 'Board Part Interfaces' tab only want to connect to an AXI_Ethernet peripheral. This interface needs to connect to the 'phy_rst_n' port of the AXI Ethernetlite peripheral AND be driven off-chip as an external port to the Ethernet PHY on the board.
- The 'ref_clk' port of the 'mii_to_rmii' IP wants to connect to 'sys_clk' when running 'Run Connection Automation'. This is not correct. This IP port needs to be connected to a 50Mhz clock output from the 'clocking wizard' IP AND be driven off-chip (through another 'clocking wizard' and phase shifted 45 degrees) to the clock input of the Ethernet PHY.
- Some board interface ports do not get identified and constrained correctly for I/O locations and I/O standards. Open the synthesized design and expand the hierarchy of I/O ports and you will see the errors/missing constraints. **The supplied master XDC constraints file (7A50T_Master_XDC_PCB_Rev_A_v1_0.xdc) can be used to identify the correct location and I/O constraints for the I/O ports outlined below.** The known problems are as follows:
  - The MDC/MDIO interfaces for each of the Ethernet ports do not get constrained correctly. The user must manually constrain the I/O locations and I/O standards for these signals.
  - The Ethernet PHY reset and 50MHz ref clock for each of the Ethernet ports do not get constrained correctly. The user must manually add these ports to the IPI block diagram and edit the I/O standard and location constraints.
  - The QSPI SCK signal does not get properly constrained. The user must manually constrain the I/O location and I/O standard for this signal.
  - The system clock input does not get properly constrained. The user must manually constrain the I/O location and I/O standard for this signal.

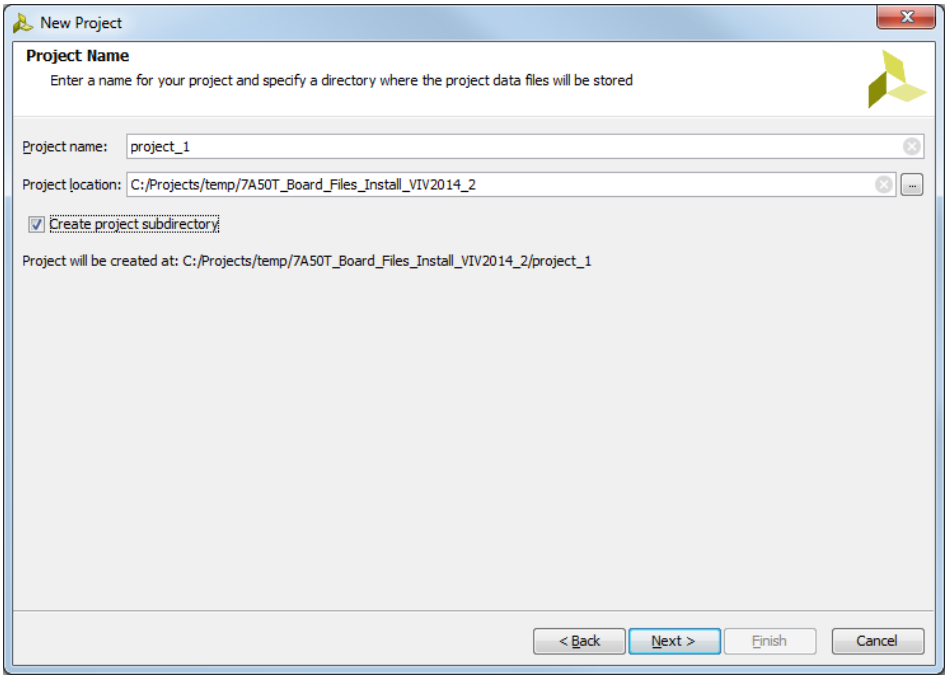
Using the Avnet 7A50T Board Files in Vivado 2014.2

Once the Avnet board files for the 7A50T Evaluation board are installed, they can be used to generate a MicroBlaze based design. Please follow the steps shown below to generate an example design using the Avnet 7A50T board files in Vivado 2014.2 tool.

1. Open Vivado and select **Create New Project**.



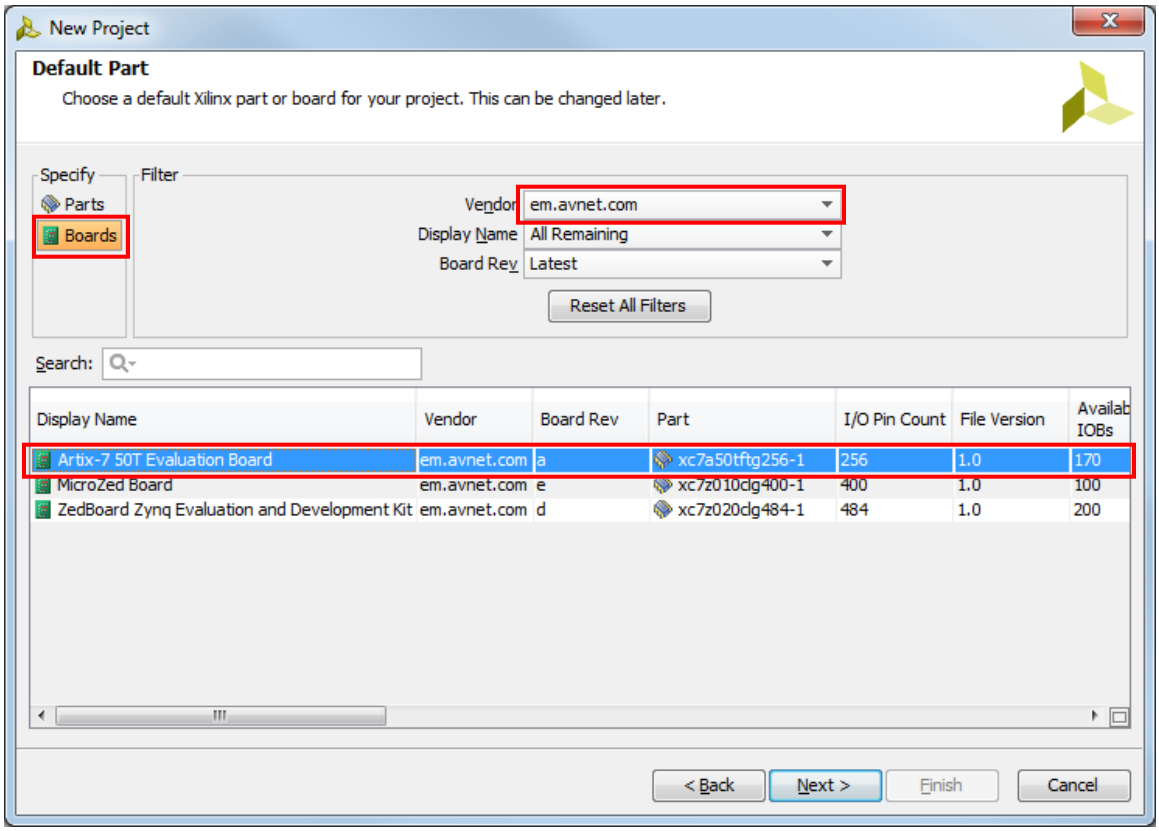
2. Click **Next** at the first window and at the next window navigate to a folder of your choice to store the Vivado project. Click **Next** to continue.



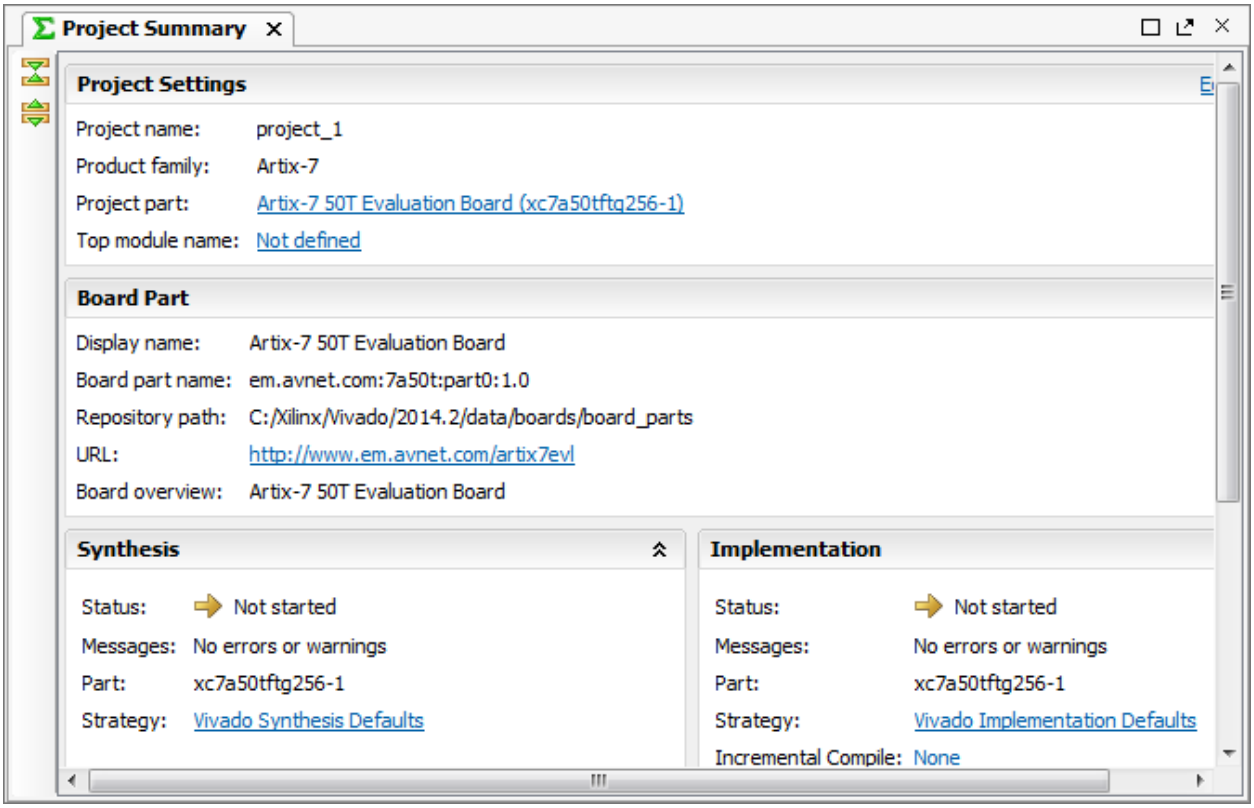
3. Click **Next** to create an RTL project (without sources).

4. Click **Next** at the following four windows to skip the addition of HDL sources, existing IP, and constraints.

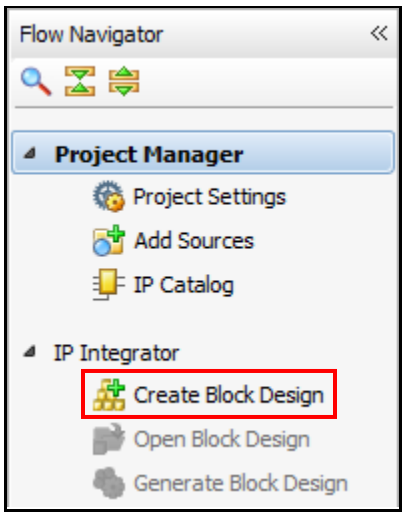
5. Rather than just specifying a target FPGA device we will select the **Artix-7 50T Evaluation Board** as the target. Click on **Boards,** then in the **Filter** section select **em.avnet.com** in the drop list. This will display the list of Avnet boards that have board definition files installed in the Vivado tools. Select the **Artix-7 50T Evaluation Board** and click **Next** and then click **Finish** at the **New Project Summary** window.



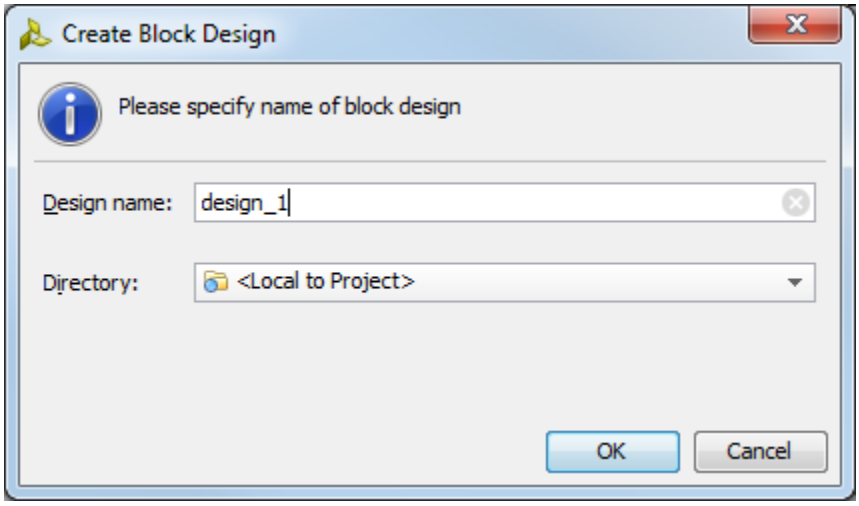
6. The **Project Summary** pane should resemble the screenshot below:



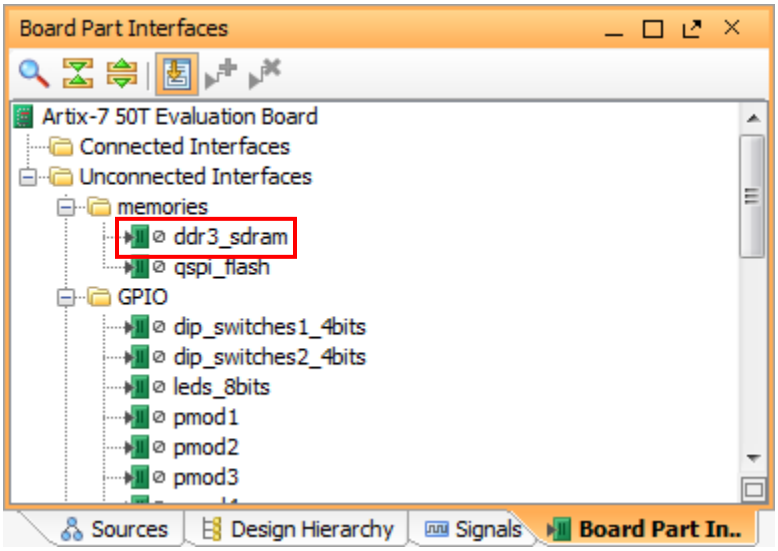
7. Go to the **Flow Navigator** pane in and under **IP Integrator** select **Create Block Diagram.**



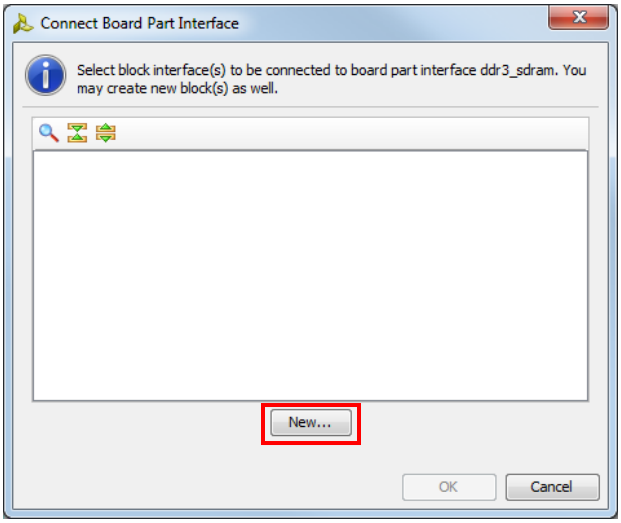
8. Choose a name for the block diagram design (or accept the default) then click **OK** to continue.

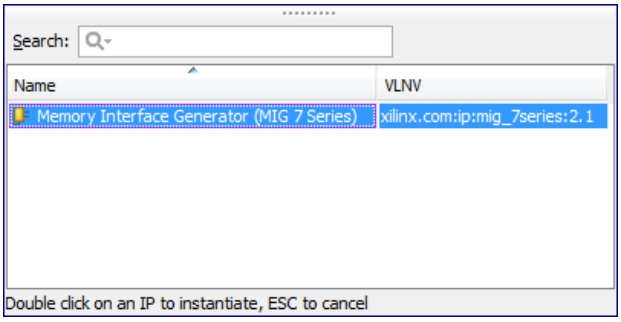


9. Navigate to the **Board Part Interfaces** tab and double-click on the **ddr3_sdram** memory interface.

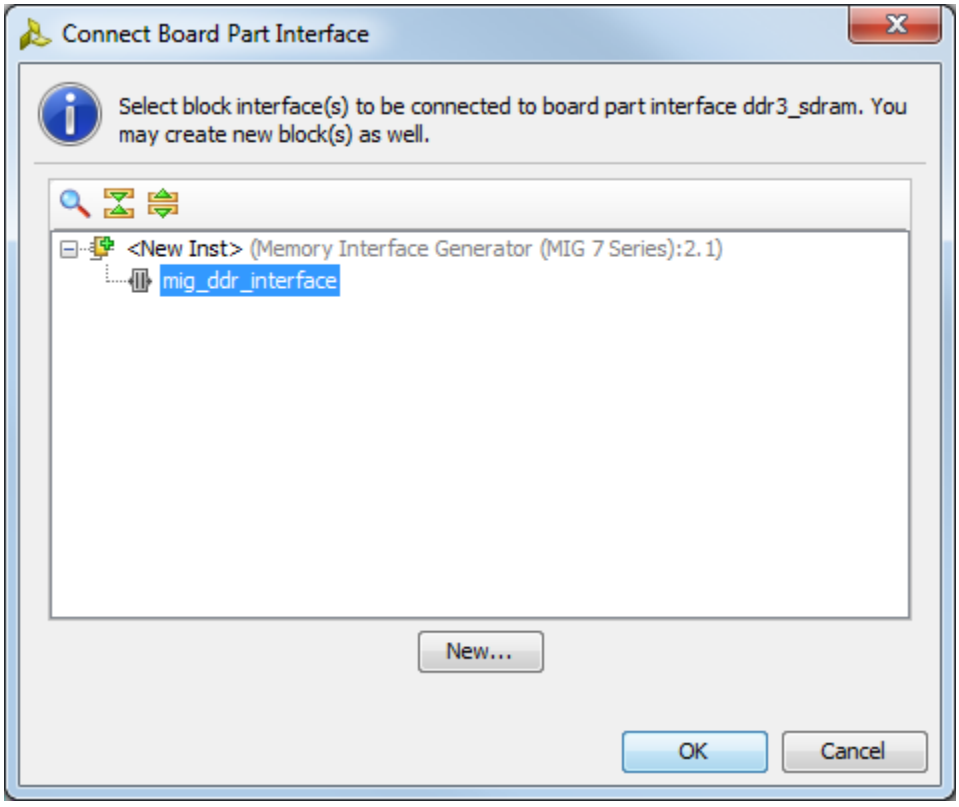


10. Click on **New** and then double-click on **Memory Interface Generator (MIG 7 Series)**.

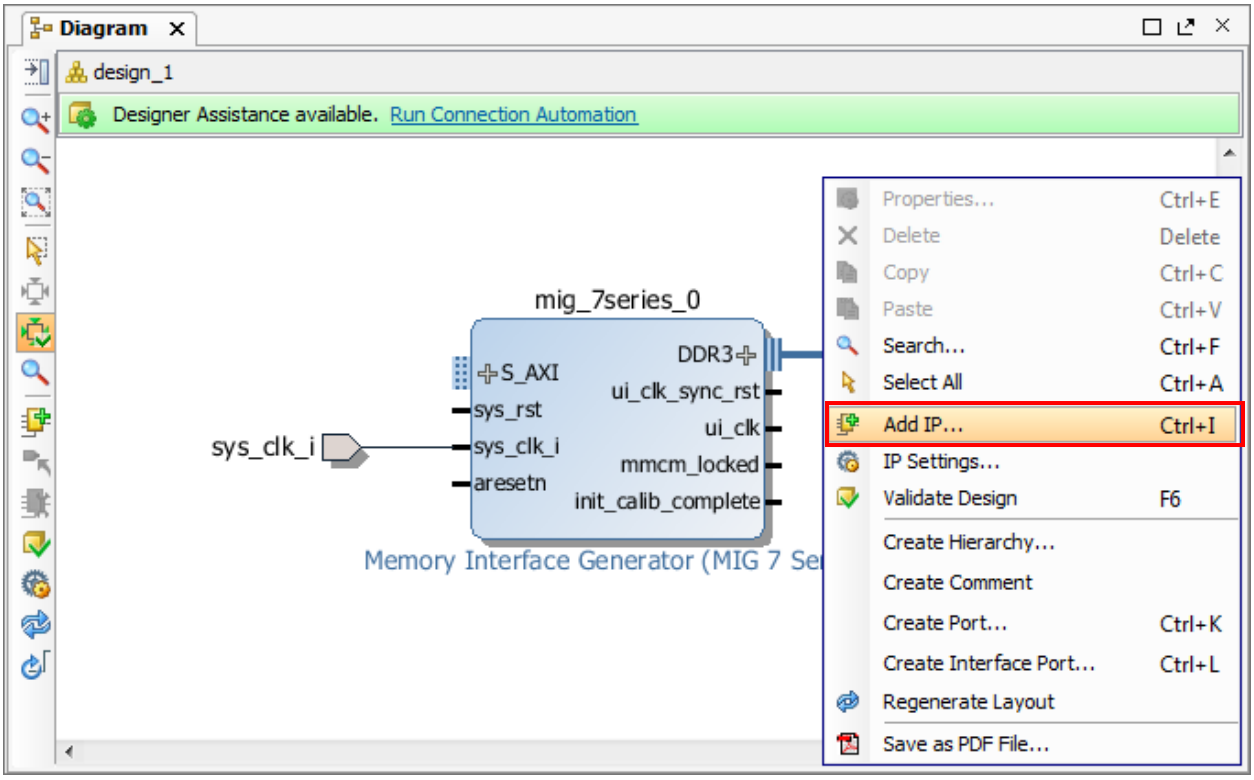




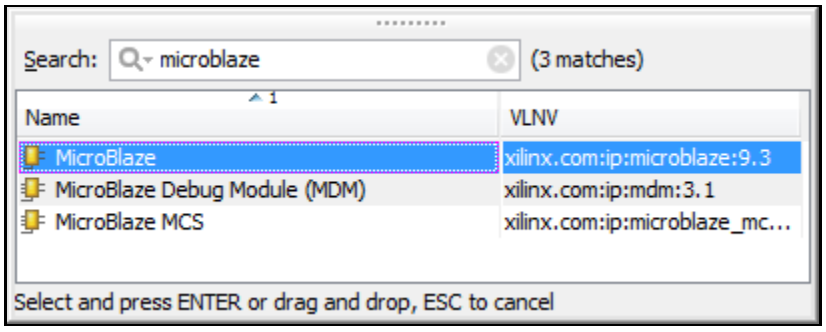
11. Click **OK** to continue. The DDR3 interface will be added to the block diagram.



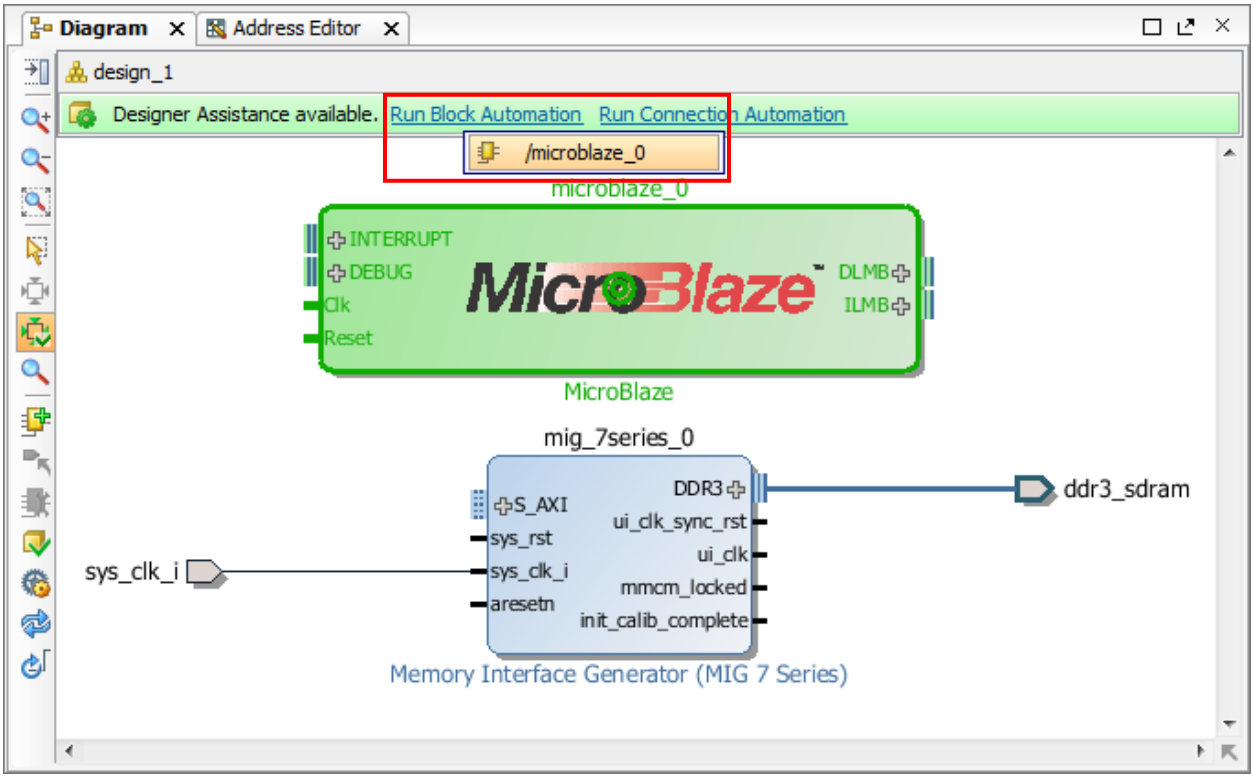
12. Right-click anywhere in the white space of the **design_1** block diagram pane and select **Add IP**.



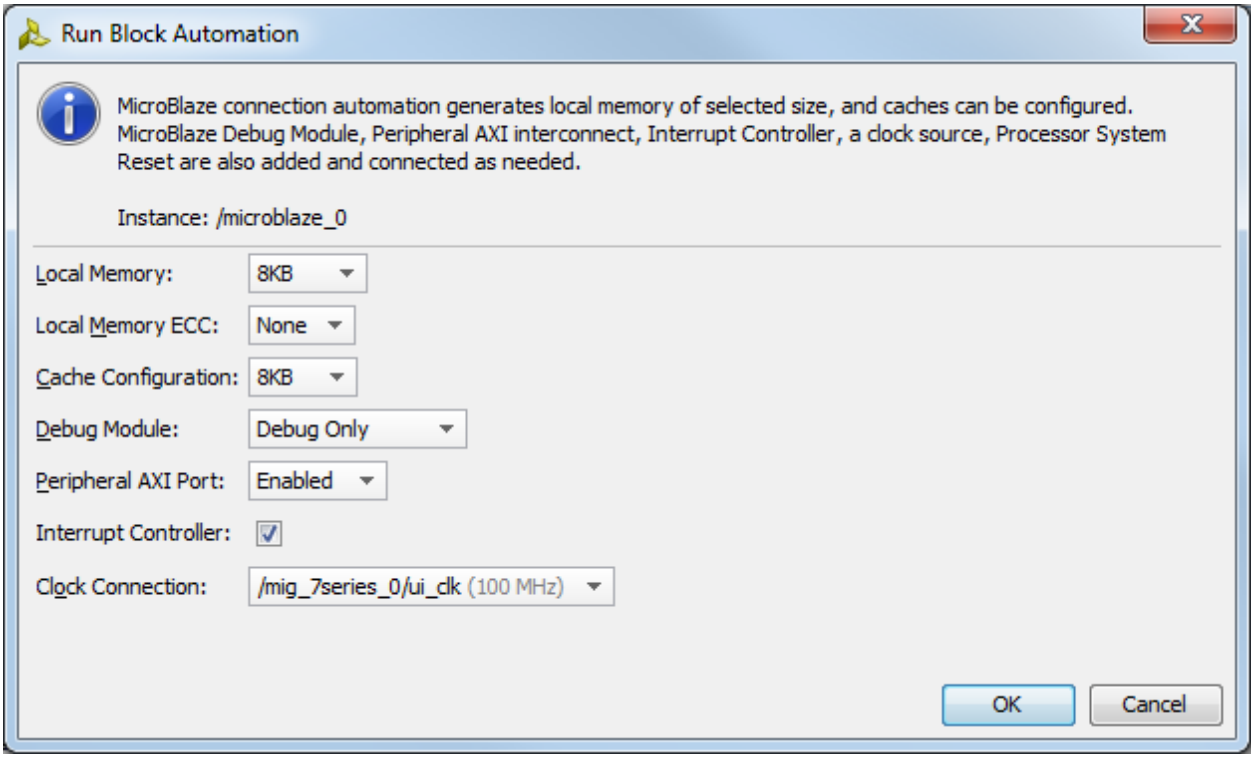
13. Search for and double-click on **MicroBlaze**.



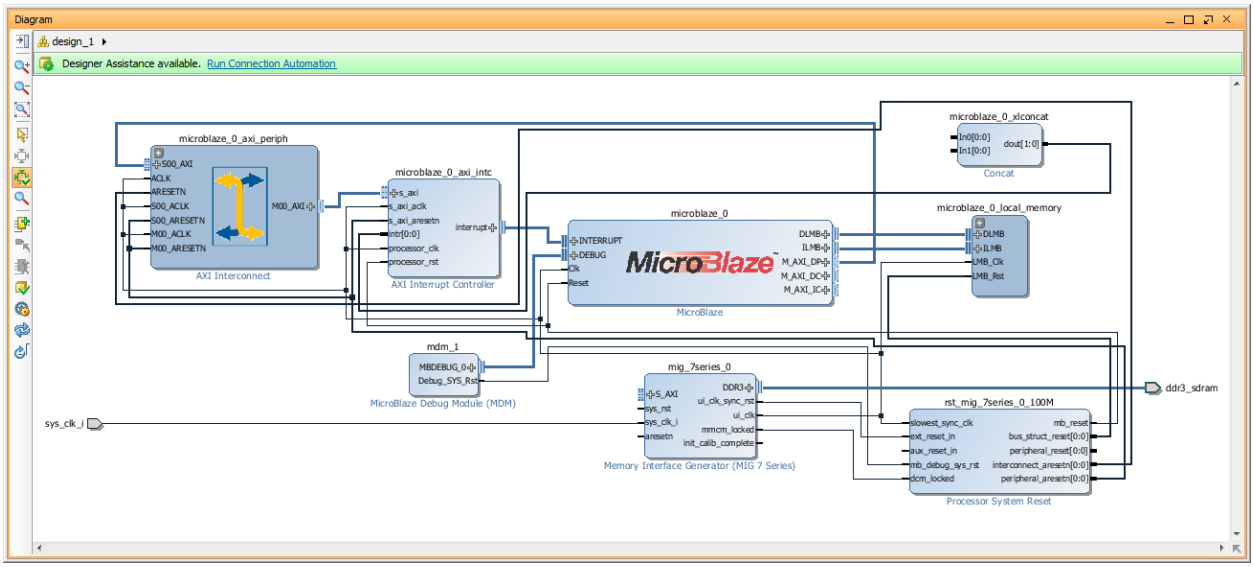
14. The MicroBlaze soft processor will be added to the block diagram. Click on **Run Block Automation** and select **microblaze_0** to customize the MicroBlaze instance and automate key system connections for its use in the processor system.



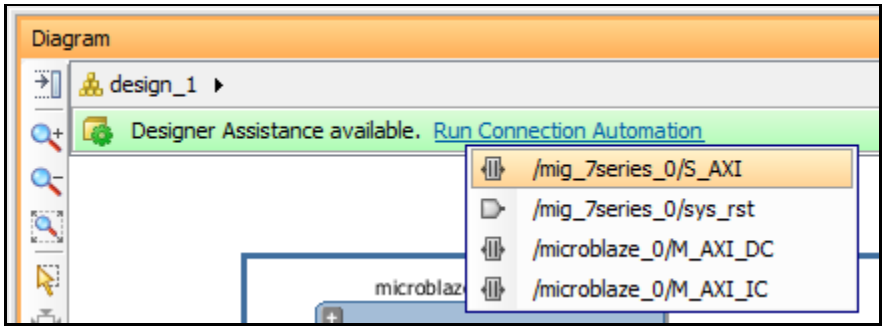
15. Below are the default MicroBlaze options with the **Interrupt Controller enabled**. Note the **Clock Connection** by default is set to **/mig_7series_0/ui_clk (100 MHz)**. This is convenient as it allows us to use the user interface clock output (ui_clk) of the MIG DDR3 interface to be the MicroBlaze processor and system clock for the AXI interconnect and peripherals that will be added later. This saves the steps of manually adding and connecting clocking resources in the block diagram. This, coincidentally, is why we added the DDR3 interface to the block diagram first, so this connection would be available to choose once the MicroBlaze processor has been added to the design. Click **OK** to continue.



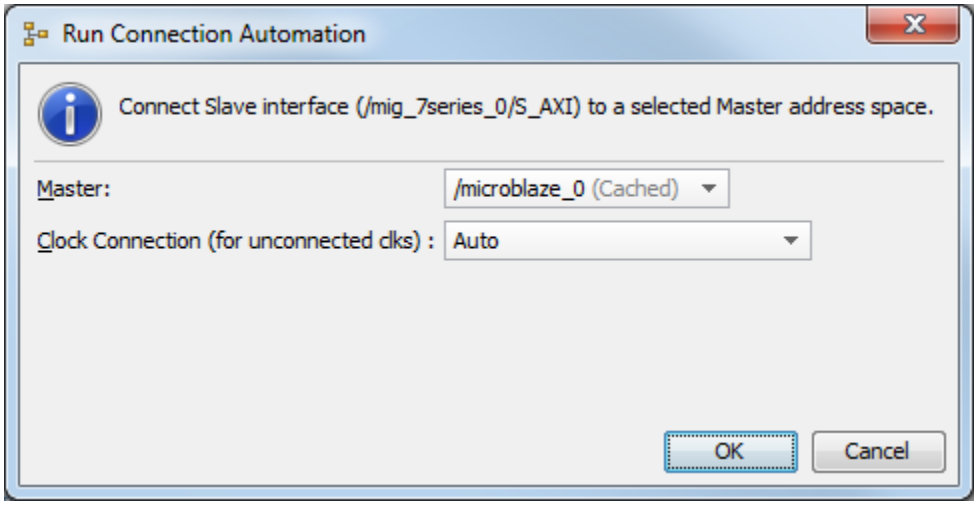
16. Notice the new connections and IP additions Block Automation added to the design.



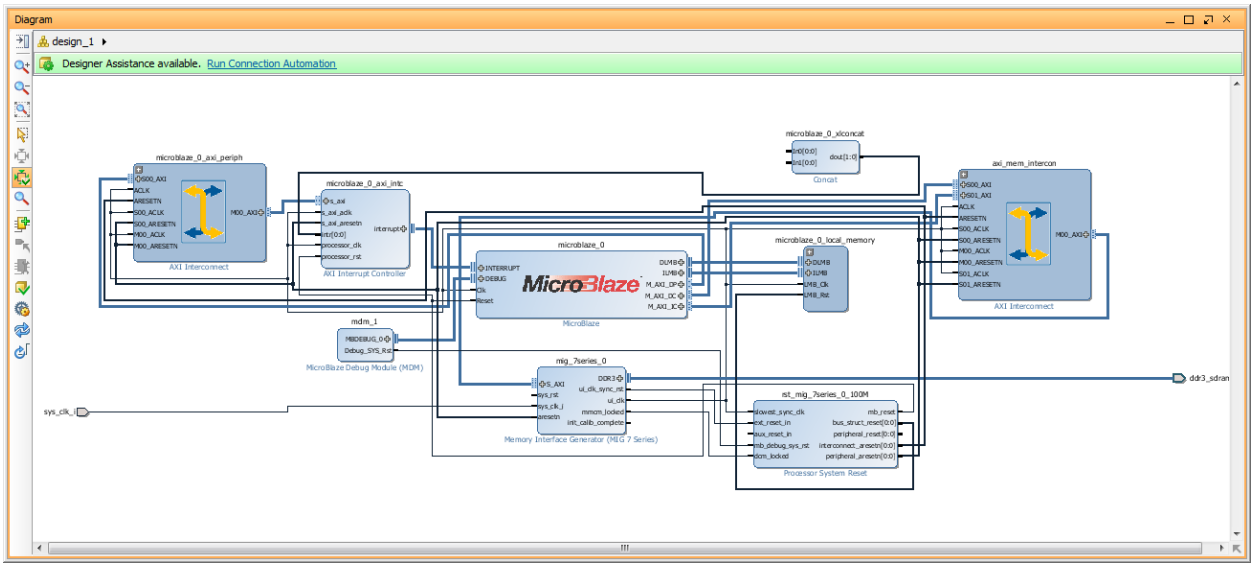
17. Now click on **Run Connection Automation** and select **/mig_7series_0/S_AXI**.



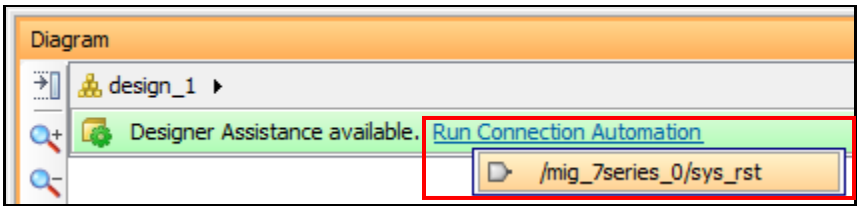
18. Click **OK** to accept the default connections.



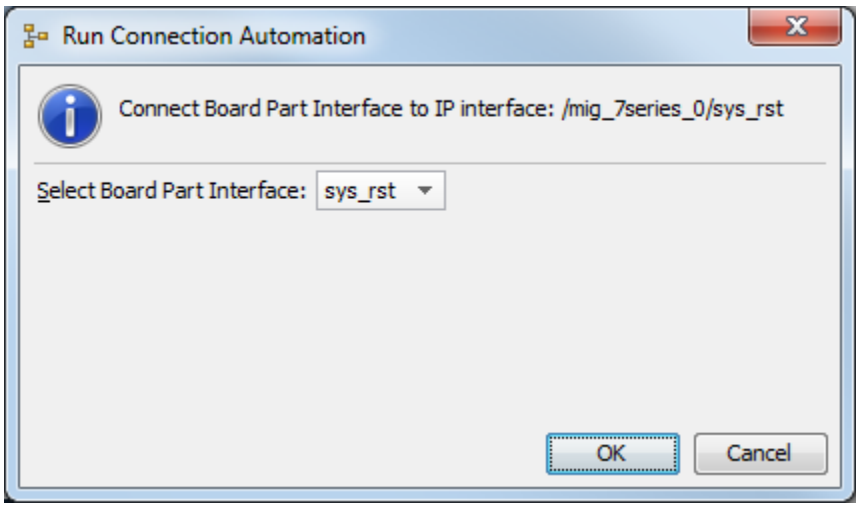
19. Notice now another **AXI Interconnect** block has been added and connected to **the Instruction Cache (IC)** and **Data Cache (DC) ports** of the MicroBlaze instance and the **S_AXI** port of the MIG DDR3 controller is connected to the **MO0_AXI** port of the new AXI Interconnect block.



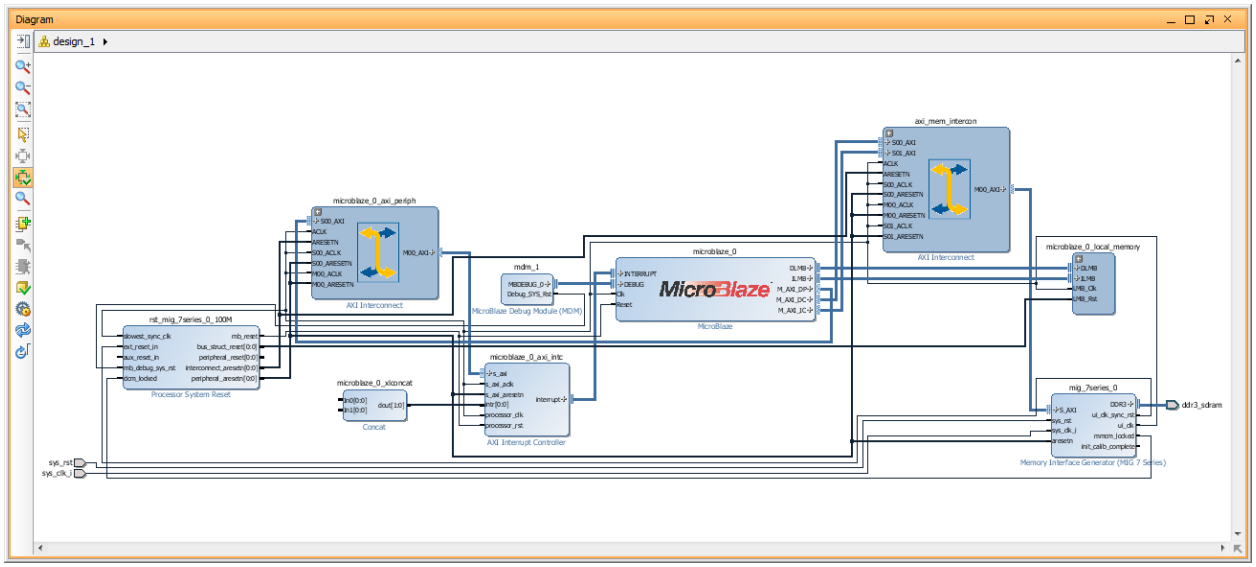
20. Click again on **Run Connection Automation** and select **/mig_7series_0/sys_rst.**



21. Accept the default connection to the **sys_rst** port.



22. At this point the essentials of the processor system have been added to the design and you can use this as the basis for your own custom designs by adding other board interfaces to the system via the **Board Part Interfaces** tab similar to how we added the DDR3 memory interface earlier.



23. Please refer to this following short video for more information on using the board definition files in Vivado. This video will show how to add other IP cores and board interfaces to the design. http://www.xilinx.com/training/vivado/using-vivado-with-xilinx-evaluation-boards.htm

This concludes this installation guide.

Getting Help and Support

Evaluation Kit home page with Documentation and Reference Designs

http://em.avnet.com/artix7evl

For Xilinx technical support, you may contact your local Avnet/Silica FAE or Xilinx Online Technical Support at www.support.xilinx.com. On this site you will also find the following resources for assistance:

- Software, IP, and Documentation Updates
- Access to Technical Support Web Tools
- Searchable Answer Database with Over 4,000 Solutions
- User Forums
- Training - Select instructor-led classes and recorded e-learning options

Contact Avnet Support for any questions regarding the Artix-7 50T Evaluation board reference designs, kit hardware, or if you are interested in designing any of the kit devices into your next design.

- http://www.em.avnet.com/techsupport

You can also contact your local Avnet/Silica FAE.

Recommended Reading

- The hardware used on the Artix-7 50T Evaluation board is described in detail in Avnet document *Avnet Artix-7 50T Evaluation board, Rev. A - User Guide*.

- Details on the Artix-7 FPGA family are included in the following Xilinx documents:
  - *Artix-7 Family Overview (DS180)*
  - *Artix-7 FPGA Data Sheet (DS181)*
  - *Artix-7 FPGA Configuration User Guide (UG470)*

Revision History

Version	Date	Author	Details
1.0	October 2, 2014	TC	Xilinx Vivado 2014.2. Release to web.