

		•						Note (1)
Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	M301	DQS for X8
Number					Channel			
GXB_L1		REFCLK1Ln					E20	
GXB_L1		REFCLK1Lp					E21	
GXB_L1		GXB_TX_L5n					G21	
GXB_L1		GXB_TX_L5p					H21	
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					F18	
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					G18	
GXB_L0		GXB_TX_L2n					K21	
GXB_L0		GXB_TX_L2p					L21	
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					J18	
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					K18	
GXB_L0		GXB_TX_L1n					N21	
GXB_L0		GXB_TX_L1p					P21	
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					M18	
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					N18	
GXB_L0		GXB_TX_L0n					T21	
GXB L0		GXB TX L0p					U21	
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					R18	
GXB L0		GXB RX L0n,GXB REFCLK L0n					T18	
GXB_L0	Ì	REFCLK0Lp					U19	1
GXB_L0		REFCLK0Ln					V20	1
3A		TDO		TDO	+	<u> </u>	Y21	†
3A	1	nCSO		DATA4			W19	1
3A	<u> </u>	TMS		TMS	+	1	Y20	+
3A		AS_DATA3		DATA3			W20	
3A		TCK		TCK			V19	
3A		AS_DATA2		DATA2			Y19	
3A		TDI		TDI			AA21	
3A		AS_DATA1		DATA1			W21	
3A		DCLK		DCLK			AA20	-
3A		AS_DATA0,ASDO		DATA0			AA20 AA19	-
	VREFB3AN0			DATA6	DIFFIO RX B1n	DIFFOUT B1n	AA18	DQ1B
3A		10						DQTB
3A	VREFB3AN0	10		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	V17	2012
3A	VREFB3AN0	10		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	AA17	DQ1B
3A	VREFB3AN0	10		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	V16	DQ1B
3A	VREFB3AN0	10		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	Y16	DQSn1B
3A	VREFB3AN0	10		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	V15	DQ1B
3A	VREFB3AN0	10		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AA16	DQS1B
3A	VREFB3AN0	10		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	W16	
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	Y15	DQ1B
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	V9	DQ1B
3A	VREFB3AN0	Ю		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	AA15	DQ1B
3A	VREFB3AN0	10		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V10	DQ1B
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	W14	
3A	VREFB3AN0	10		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	V11	DQ1B
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	Y14	
3A	VREFB3AN0	10			DIFFIO_TX_B8p	DIFFOUT_B8p	V12	DQ1B
3B	VREFB3BN0	10			DIFFIO_RX_B10n	DIFFOUT_B10n	Y13	
3B	VREFB3BN0	10			DIFFIO_RX_B11p	DIFFOUT_B11p	W13	
3B	VREFB3BN0	10			DIFFIO_RX_B14n	DIFFOUT_B14n	AA13	
3B	VREFB3BN0	10	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	AA12	
3B	VREFB3BN0	10			DIFFIO_RX_B18n	DIFFOUT_B18n	AA11	DQ3B
3B	VREFB3BN0	10			DIFFIO_TX_B17p	DIFFOUT_B17p	W4	DQ3B
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	AA10	DQ3B
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	Y10	DQSn3B
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	V5	DQ3B
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	Y11	DQS3B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	U5	DQ3B
3B	VREFB3BN0	IO	<u>LL_DL_OLIGOTI, IT LL_DL_OLIGOTII</u>		DIFFIO_TX_B2111	DIFFOUT_B22n	W6	DQ3B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	VV6	DQ3B
<u>зв</u> 3В	VREFB3BN0	IO	LL_DL_GLNOUTU,FFLL_BL_GLNOUTP,FFLL_BL_FB	<u> </u>	DIFFIO_TX_B21p	DIFFOUT_B22p	V4 V6	DQ3B
3B 3B	VREFB3BN0 VREFB3BN0	lio	CLK1n	-	DIFFIO_RX_B22p DIFFIO_RX_B23n	DIFFOUT_B23n	U4	סמאס
3B 3B	VREFB3BN0 VREFB3BN0		CLK1n	-			V7	DQ3B
		10	OLIVA-		DIFFIO_TX_B24n	DIFFOUT_B24n		ספאת
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	U3	1



								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M301	DQS for X8
B	VREFB3BN0	10			DIFFIO_TX_B24p	DIFFOUT_B24p	W7	DQ3B
A	VREFB4AN0	10	RZQ 0		DIFFIO TX B25n	DIFFOUT B25n	T2	
A	VREFB4AN0	10			DIFFIO_RX_B26n	DIFFOUT_B26n	R3	
A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	T3	
A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT B26p	R4	
A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	Y8	
Α	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	Y9	
Α	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AA8	
IA	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AA7	
IA	VREFB4AN0	10	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	AA6	
Α	VREFB4AN0	10	СЕКЕР		DIFFIO_RX_B34n	DIFFOUT_B34n	Y6	
IA	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34II	AA5	
IA	VREFB4AN0				DIFFIO_RX_B34p	DIFFOUT B35n	_	
		10		-			Y5	
IA.	VREFB4AN0	10			DIFFIO_RX_B35p	DIFFOUT_B35p	Y4	
A	VREFB4AN0	10			DIFFIO_RX_B38n	DIFFOUT_B38n	Y3	
łA .	VREFB4AN0	10			DIFFIO_RX_B38p	DIFFOUT_B38p	AA3	
A	VREFB4AN0	10	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	AA2	
ŀΑ	VREFB4AN0	10			DIFFIO_RX_B43n	DIFFOUT_B43n	AA1	
A	VREFB4AN0	10			DIFFIO_RX_B43p	DIFFOUT_B43p	Y1	
ŀΑ	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	W1	
IA.	VREFB4AN0	10			DIFFIO_RX_B46p	DIFFOUT_B46p	W2	
1A	VREFB4AN0	10			DIFFIO_RX_B47n	DIFFOUT_B47n	V1	
1A	VREFB4AN0	10			DIFFIO_RX_B47p	DIFFOUT_B47p	V2	
5A	VREFB5AN0	10	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	M4	
iΑ	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	R1	
A	VREFB5AN0	IO		PR REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	M3	
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	P2	
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	J4	
iA	VREFB5AN0	10		11020	DIFFIO_RX_R4p	DIFFOUT_R4p	M2	
iA	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_RX_R4p	DIFFOUT R3n	J3	
				CVP_CONFIDONE				
5A	VREFB5AN0	10		DEV 05	DIFFIO_RX_R4n	DIFFOUT_R4n	L2	
5A	VREFB5AN0	10		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	G3	
5A	VREFB5AN0	10		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	N1	
5A	VREFB5AN0	10		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	H4	
5A	VREFB5AN0	10		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	N2	
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	K4	
5A	VREFB5AN0	Ю			DIFFIO_RX_R8p	DIFFOUT_R8p	P3	
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	K3	
5A	VREFB5AN0	10			DIFFIO_RX_R8n	DIFFOUT_R8n	N4	
iВ	VREFB5BN0	10	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	L1	
iB	VREFB5BN0	10			DIFFIO_TX_R18p	DIFFOUT_R18p	E4	
iB	VREFB5BN0	10	CLK6n		DIFFIO_RX_R17n	DIFFOUT R17n	K1	
iВ	VREFB5BN0	10			DIFFIO_TX_R18n	DIFFOUT_R18n	E3	
iB	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	H1	
SB	VREFB5BN0	IO	FPLL BR CLKOUT0,FPLL BR CLKOUTp,FPLL BR FB		DIFFIO_TX_R20p	DIFFOUT R20p	F3	
iB	VREFB5BN0	IO	oz.noo roj. r zz_on_oznoo rpj. r zz_on_r b	+	DIFFIO_RX_R19n	DIFFOUT_R19n	J2	+
iB	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn	1	DIFFIO_RX_R19II	DIFFOUT_R20n	G4	+
iB		IO	I I LL_DN_OLNOU I I,FFLL_DN_OLNOU III	+				+
	VREFB5BN0			+	DIFFIO_RX_R21p	DIFFOUT_R21p	H2	+
B .	VREFB5BN0	10		+	DIFFIO_RX_R21n	DIFFOUT_R21n	G2	+
В	VREFB5BN0	10		+	DIFFIO_TX_R22n	DIFFOUT_R22n	E5	+
В	VREFB5BN0	10			DIFFIO_RX_R23p	DIFFOUT_R23p	F1	1
iB	VREFB5BN0	10			DIFFIO_TX_R24p	DIFFOUT_R24p	E1	1
В	VREFB5BN0	10			DIFFIO_RX_R23n	DIFFOUT_R23n	F2	1
		GND					D2	
'A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	C1	
'A	VREFB7AN0	10			DIFFIO_RX_T17n	DIFFOUT_T17n	C2	
'A	VREFB7AN0	10			DIFFIO_RX_T19p	DIFFOUT_T19p	A1	
'A	VREFB7AN0	10			DIFFIO_RX_T19n	DIFFOUT_T19n	B2	
'A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	A2	
A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT T23n	A3	
A	VREFB7AN0	IO		1	DIFFIO_RX_T27p	DIFFOUT_T27p	B3	+
Ά	VREFB7AN0	IO		+	DIFFIO_RX_T27p	DIFFOUT_T27n	C4	+
7A	VREFB7AN0	IO		1	DIFFIO_RX_T31p	DIFFOUT_T31p	A5	1
A	VINEFE/AINU	IIO		1	IDILLIO KY 191b	DILLOGI 1916	(A)	1



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M301	DQS for X8
A	VREFB7AN0	IO			DIFFIO RX T31n	DIFFOUT T31n	B4	+
À	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	C5	+
·	VREFB7AN0	10			DIFFIO_TX_T34n	DIFFOUT_T34n	D6	+
\ \	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	B5	+
<u>. </u>	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	C6	1
<u>, </u>	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	A6	+
, ,	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	D7	+
Α .	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	A7	+
Α	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	B7	+
Α	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	D9	+
4	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	A8	+
Ä	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT T40p	C7	+
4	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T39n	B8	+
4	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	D8	4
4						DIFFOUT T41p		4
	VREFB8AN0	10	CLK9p		DIFFIO_RX_T41p		C12	DOOT
١	VREFB8AN0	IO	1		DIFFIO_TX_T42p	DIFFOUT_T42p	D14	DQ6T
١	VREFB8AN0	10	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	D11	
١	VREFB8AN0	IO		_	DIFFIO_TX_T42n	DIFFOUT_T42n	D13	DQ6T
١	VREFB8AN0	10		_	DIFFIO_RX_T43p	DIFFOUT_T43p	C10	DQ6T
١	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	C17	DQ6T
4	VREFB8AN0	10			DIFFIO_RX_T43n	DIFFOUT_T43n	B11	DQ6T
4	VREFB8AN0	10	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	D17	DQ6T
4	VREFB8AN0	10			DIFFIO_RX_T45p	DIFFOUT_T45p	A10	DQS6T
4	VREFB8AN0	10			DIFFIO_RX_T45n	DIFFOUT_T45n	B10	DQSn6T
Ą	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	D16	DQ6T
١	VREFB8AN0	10			DIFFIO_RX_T47p	DIFFOUT_T47p	B12	DQ6T
١	VREFB8AN0	10			DIFFIO_TX_T48p	DIFFOUT_T48p	C16	DQ6T
Ą	VREFB8AN0	10			DIFFIO_RX_T47n	DIFFOUT_T47n	A13	DQ6T
Ą	VREFB8AN0	10	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	A11	
A	VREFB8AN0	10	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	A12	
A	VREFB8AN0	10			DIFFIO_RX_T51p	DIFFOUT_T51p	B13	
A	VREFB8AN0	10			DIFFIO_RX_T53n	DIFFOUT_T53n	B14	
Α	VREFB8AN0	10			DIFFIO_RX_T55p	DIFFOUT_T55p	A15	
A	VREFB8AN0	10			DIFFIO_RX_T55n	DIFFOUT_T55n	B15	1
Ą		MSEL0		MSEL0			A17	+
Α.		CONF_DONE		CONF_DONE			A16	1
A		MSEL1		MSEL1			A19	+
Α		nSTATUS		nSTATUS			A18	1
<u>.</u>		nCE		nCE			A20	1
Α		MSEL2		MSEL2			A21	+
À A		MSEL3		MSEL3			B20	+
Ä		nCONFIG		nCONFIG			D19	+
A		MSEL4		MSEL4			B19	+
1	1	GND		WOLL4	1		C19	+
	1	GND	1		1	+	M21	+
	1	GND				+		+
	1					+	M9 A9	+
	1	GND						+
	1	GND					D10	+
	1	GND		_			J19	+
	1	GND		_			K13	+
	ļ	GND		_			J10	
		GND					M11	
		GND					G20	
		GND					F19	4
		GND					A4	
		GND					J12	
		GND					W5	
		GND					U18	
		GND					H20	
		GND					P18	
		GND					V13	T
		GND					N12	



lank lumber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M301	DQS for X8		
		GND					R19			
		GND					L4			
		GND					K11			
		GND					P20			
		GND					D15			
		GND		İ			N10			
		GND					L18			
		GND		1			F4			
		GND		1			M13			
		GND		1			B16			
		GND		1			W10			
		GND						-		
		GND		ļ			E2			
							U20			
		GND					L20			
		GND					H18			
		GND					B1			
		GND					K9			
		GND					E18			
		GND					D21			
		GND					H3			
		GND					R21			
		GND					K19			
		GND					G19			
		GND		1			F21	+		
		GND		1			U1			
		GND		 			J21	+		
				<u> </u>			J21			
		GND		<u> </u>			T19			
		GND					M19			
		GND					D5			
		GND					V21			
		GND					T4			
		GND					V8			
		GND					C18			
		GND					AA14			
		GND					T20			
		GND					V3			
		GND					N20			
		GND					N19			
		GND		1			K20	+		
		GND					B21			
		VCC		 			L9	1		
				ļ						
		VCC		<u> </u>			N11			
		VCC					L13			
	1	VCC				1	J9	1		
		VCC					J11			
		VCC					M10			
		VCC					L12	1		
		VCC					M12			
		VCC					K10			
		VCC					N13			
		VCC					L10			
		VCC				İ	K12			
	1	VCC					N9			
	1	VCC					L11	1		
	1	VCC		1	1	1	J13	1		
	}	DNU					C20	+		
	1						020	1		
	1	DNU				1	D20	1		
		DNU					D4			
		DNU					D12	1		
		VCCPGM					Y18			
		VCCPGM					T1			
		VCCPGM					B17			
		VCCBAT					D18			



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		VCCIO3A					W15	
		VCCIO3A					Y17	
		VCCIO3B					AA9	
		VCCIO3B					Y12	
		VCCIO4A					Y2	
		VCCIO4A					AA4	
		VCCIO4A					Y7	
		VCCIO5A					R2	
		VCCIO5A					N3	
		VCCIO5B					G1	
		VCCIO5B					K2	
		VCCIO7A					C8	
		VCCIO7A					B6	
		VCCIO7A					C3	
		VCCIO8A					A14	
		VCCIO8A					C13	
		VCCPD3A					W17	
		VCCPD3B4A					V14	
		VCCPD3B4A		İ			W9	
		VCCPD5A		İ			P1	
		VCCPD5B					J1	
		VCCPD7A8A					C14	
		VCCPD7A8A		1			B9	
	VREFB3AN0	VREFB3AN0					V18	
	VREFB3BN0	VREFB3BN0		1			W12	
		VREFB4AN0		1			W8	
	VREFB5AN0	VREFB5AN0		1			P4	
·	VREFB5BN0	VREFB5BN0		1			L3	
\	VREFB7AN0	VREFB7AN0					C9	
\	VREFB8AN0	VREFB8AN0		1			C15	
	VICEI DO/1140	VCCH_GXBL					M20	
		VCCH_GXBL		1			E19	
		VCCL_GXBL					J20	
		VCCL_GXBL					R20	
		RREF_TL					C21	
		VCCA_FPLL					U17	
		VCCA_FPLL					E17	
		VCCA_FPLL		1			U2	
		VCCA_FPLL VCCA_FPLL		1			D1	
		VCC_AUX					B18	
		VCC_AUX					W18	
		VCC_AUX					C11	
	-	VCC_AUX VCC_AUX			 		W11	+
	-	VCC_AUX			 		D3	1
	-	VCC_AUX VCC_AUX			 		W3	1
					 			_
		VCCE_GXBL VCCE_GXBL			 		P19 L19	_
	-				<u> </u>			
		VCCE_GXBL VCCE_GXBL		+	1		F20 H19	

Note

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.

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										Note (1)
Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin	HMC Pin
Number					Channel				Assignment for	Assignment for
									DDR3/DDR2 (2)	LPDDR2
GXB_L1		REFCLK1Ln					G23			
GXB_L1		REFCLK1Lp					H24			
GXB_L1		GXB_TX_L5n					F25			
GXB_L1	1	GXB_TX_L5p					G25			
GXB_L1 GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p GXB_RX_L5n,GXB_REFCLK_L5n					E22 F22			
GXB_L1	 	GXB_TX_L4n					J25			+
GXB_L1		GXB_TX_L4p					K25			1
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					H22			1
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					J22			
GXB_L1		GXB_TX_L3n					M25			
GXB_L1	1	GXB_TX_L3p					N25 L22			
GXB_L1 GXB_L1	1	GXB_RX_L3p,GXB_REFCLK_L3p GXB_RX_L3n,GXB_REFCLK_L3n				+	M22		+	+
GXB_L0	1	GXB_TX_L2n					R25		1	+
GXB_L0		GXB_TX_L2p					T25			
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					P22			
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R22			
GXB_L0		GXB_TX_L1n				ļ	V25		_	
GXB_L0	+	GXB_TX_L1p	 	1	1		W25	1	+	+
GXB_L0	+	GXB_RX_L1p,GXB_REFCLK_L1p		 	-	 	U22 V22	 	+	+
GXB_L0 GXB_L0	1	GXB_RX_L1n,GXB_REFCLK_L1n GXB_TX_L0n		 	1	 	AA25	†	†	+
GXB_L0	1	GXB_TX_L0p		1		İ	AB25	1	1	†
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p		İ		İ .	Y22		1	1
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AA22			
GXB_L0	1	REFCLK0Lp			ļ		AC24			4
GXB_L0		REFCLK0Ln		TD0	ļ	1	AC23	.	1	
3A 3A		nCSO		TDO DATA4			AD25 AD24			
3A		TMS		TMS			AE25			
3A	1	AS_DATA3		DATA3			AE24		1	+
3A		TCK		TCK			AC22			
3A		AS_DATA2		DATA2			AB21			
3A		TDI		TDI			AD23			
3A		AS_DATA1		DATA1			AE21			
3A	1	DCLK		DCLK			AE22			
3A 3A	VREFB3AN0	AS_DATA0,ASDO		DATA0 DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	AE23 AE18	DQ1B	+	+
3A	VREFB3AN0	10		DATA6 DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	AE20	DQIB		+
3A	VREFB3AN0	10		DATAS DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	AD19	DQ1B	1	+
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	AD21	DQ1B		
3A	VREFB3AN0	Ю		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	AD18	DQSn1B		
3A	VREFB3AN0	Ю		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB20	DQ1B		
3A	VREFB3AN0	10		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AC17	DQS1B		
3A 3A	VREFB3AN0 VREFB3AN0	10		DATA11 DATA14	DIFFIO_TX_B4p DIFFIO_RX_B5n	DIFFOUT_B4p DIFFOUT_B5n	AB19 AF17	DO1B		
3A	VREFB3AN0			DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AC19	DQ1B		
3A	VREFB3AN0	10		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	AD16	DQ1B	1	+
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	AC18	DQ1B		
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	AE16			1
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AB17	DQ1B		1
3A	VREFB3AN0	10		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	AE15	L		
3A	VREFB3AN0	10	-	 	DIFFIO_TX_B8p DIFFIO_RX_B10n	DIFFOUT_B8p	AA17	DQ1B	+	+
3B 3B	VREFB3BN0 VREFB3BN0	IIO		1	DIFFIO_RX_B10n DIFFIO_RX_B11p	DIFFOUT_B10n DIFFOUT_B11p	AA16 AC16	1	1	+
3B	VREFB3BN0	IO		1	DIFFIO_RX_B14n	DIFFOUT_B14n	AB15	1	1	†
3B	VREFB3BN0	10	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	AD15	1	1	1
3B	VREFB3BN0	10	CLK0p,FPLL BL FBp		DIFFIO_RX_B15p	DIFFOUT B15p	AD14			
3B	VREFB3BN0	Ю			DIFFIO_TX_B17n	DIFFOUT B17n	AB14			1
3B	VREFB3BN0	Ю			DIFFIO_RX_B18n	DIFFOUT_B18n	AE13	DQ2B	1	4
3B	VREFB3BN0	10		!	DIFFIO_TX_B17p	DIFFOUT_B17p	AA14	DQ2B	1	
3B 3B	VREFB3BN0 VREFB3BN0	10	-	 	DIFFIO_RX_B18p DIFFIO_RX_B19n	DIFFOUT_B18p DIFFOUT_B19n	AE12 AE11	DQ2B DQSn2B	+	+
3B 3B	VREFB3BN0 VREFB3BN0	IO		 	DIFFIO_RX_B19n DIFFIO_TX_B20n	DIFFOUT_B19n DIFFOUT_B20n	AE11 AD13	DQSn2B DQ2B	+	+
3B	VREFB3BN0	10	<u> </u>	1	DIFFIO_TX_B2011 DIFFIO_RX_B19p	DIFFOUT_B19p	AE10	DQS2B	1	+
3B	VREFB3BN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AC14		1	1
3B	VREFB3BN0	10	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB12	DQ2B		
3B	VREFB3BN0	Ю			DIFFIO_RX_B22n	DIFFOUT_B22n	AD11	DQ2B	1	1
3B	VREFB3BN0	10	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AA12	DQ2B		
3B 3B	VREFB3BN0	10	CLK1n	1	DIFFIO_RX_B22p DIFFIO_RX_B23n	DIFFOUT_B22p DIFFOUT_B23n	AC12	DQ2B	1	+
3B 3B	VREFB3BN0 VREFB3BN0	10	CLAIN	 	DIFFIO_RX_B23n DIFFIO_TX_B24n	DIFFOUT_B23n DIFFOUT_B24n	AD10 AB11	DQ2B	+	+
3B	VREFB3BN0	lio	CLK1p		DIFFIO_TX_B24fi	DIFFOUT_B23p	AD9	DQZD	†	+
3B	VREFB3BN0			İ	DIFFIO_TX_B24p	DIFFOUT_B24p	AA11	DQ2B	İ	1
4A	VREFB4AN0	10	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AB10			1
4A	VREFB4AN0	Ю			DIFFIO_RX_B26n	DIFFOUT_B26n	AE8	DQ3B	1	1
4A	VREFB4AN0	10		<u> </u>	DIFFIO_TX_B25p	DIFFOUT_B25p	AA9	DQ3B	<u> </u>	
4A	VREFB4AN0	IO		1	DIFFIO_RX_B26p	DIFFOUT_B26p	AD8	DQ3B	1	+
4A 4A	VREFB4AN0	10		 	DIFFIO RX B27n	DIFFOUT B27n	AC9	DQSn3B	 	+
475	VREFB4AN0	IIO		1	DIFFIO_TX_B28n	DIFFOUT_B28n	AB9	DQ3B	1	1



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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for	HMC Pin Assignment for
umber					Channel				DDR3/DDR2 (2)	LPDDR2
									DD.1.0/DD.1.2 (2)	L. DDILL
١	VREFB4AN0	10			DIFFIO_RX_B27p	DIFFOUT_B27p	AC8	DQS3B	1	1
١	VREFB4AN0	10			DIFFIO_TX_B28p	DIFFOUT_B28p	AA8		1	
	VREFB4AN0				DIFFIO_TX_B29n	DIFFOUT_B29n	AC7	DQ3B	1	
١	VREFB4AN0	10			DIFFIO_RX_B30n	DIFFOUT_B30n	AE6	DQ3B		
4	VREFB4AN0	10			DIFFIO_TX_B29p	DIFFOUT_B29p	AC6	DQ3B		
4	VREFB4AN0				DIFFIO_RX_B30p	DIFFOUT_B30p	AD6	DQ3B		
١	VREFB4AN0		CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	AE5			
A	VREFB4AN0	10			DIFFIO_TX_B32n	DIFFOUT_B32n	AC4	DQ3B		
١	VREFB4AN0		CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	AD5			
١	VREFB4AN0	10		ļ	DIFFIO_TX_B32p	DIFFOUT_B32p	AB5	DQ3B		
١	VREFB4AN0	10			DIFFIO_TX_B33n	DIFFOUT_B33n	AC3			
	VREFB4AN0				DIFFIO_RX_B34n	DIFFOUT_B34n	AE3	DQ4B		
	VREFB4AN0				DIFFIO_TX_B33p	DIFFOUT_B33p	AB4	DQ4B		1
	VREFB4AN0	IO IO			DIFFIO_RX_B34p DIFFIO_RX_B35n	DIFFOUT_B34p	AE2	DQ4B		
	VREFB4AN0				DIFFIO_RX_B35n DIFFIO TX B36n	DIFFOUT_B35n	AD4	DQSn4B		
	VREFB4AN0 VREFB4AN0	10			DIFFIO_IX_B36n DIFFIO RX B35p	DIFFOUT_B36n	AA4	DQ4B		
		10		1		DIFFOUT_B35p	AD3	DQS4B	+	+
	VREFB4AN0	IO IO			DIFFIO_TX_B36p DIFFIO_TX_B37n	DIFFOUT_B36p	AA3 W3	DQ4B		
	VREFB4AN0 VREFB4AN0	ie				DIFFOUT_B37n				
					DIFFIO_RX_B38n	DIFFOUT_B38n	AE1	DQ4B		1
	VREFB4AN0 VREFB4AN0	IO IO			DIFFIO_TX_B37p DIFFIO_RX_B38p	DIFFOUT_B37p DIFFOUT_B38p	V4 AD1	DQ4B DQ4B	+	
			CLK2n	1				DQ4D	+	
	VREFB4AN0 VREFB4AN0	10	CLK3n		DIFFIO_RX_B39n DIFFIO_TX_B40n	DIFFOUT_B39n DIFFOUT_B40n	AC2	DQ4B	+	
	VREFB4AN0 VREFB4AN0	10	CLK3p	1	DIFFIO_IX_B40n DIFFIO_RX_B39p		Y3 AC1	DQ4D	+	
	VREFB4AN0 VREFB4AN0		OLNOP	1	DIFFIO_RX_B39p DIFFIO_TX_B40p	DIFFOUT_B39p DIFFOUT_B40p	W4	DOAR	+	
	VREFB4AN0 VREFB4AN0	10	+	1	DIFFIO_IX_B40p DIFFIO_RX_B43n	DIFFOUT B43n	W4 AB2	DQ4B	+	
	VREFB4AN0 VREFB4AN0	10		t			AB2 AB1	†	+	
	VREFB4AN0 VREFB4AN0			t	DIFFIO_RX_B43p DIFFIO_RX_B46n	DIFFOUT_B43p DIFFOUT_B46n	AA2	†	+	
	VREFB4AN0	IO		1	DIFFIO_RX_B460	DIFFOUT B460	Y2		+	+
	VREFB4AN0			1	DIFFIO_RX_B46p DIFFIO_RX_B47n	DIFFOUT_B47n	Y1		+	+
	VREFB4AN0	10		1	DIFFIO_RX_B47h	DIFFOUT_B47h	W1		+	+
	VREFB5AN0	10	RZQ 1	1	DIFFIO_RX_B47p	DIFFOUT_R1p	U2	DQ1R	+	+
	VREFB5AN0	IO IO	RZQ_I	INIT_DONE	DIFFIO_TX_R1p	DIFFOUT_R2p	V2	DQIK	+	+
	VREFB5AN0			PR_REQUEST	DIFFIO_RX_R2p	DIFFOUT_R1n	U1	DQ1R	+	+
	VREFB5AN0			CRC ERROR	DIFFIO_IX_RIII		V1	DQIK	+	+
	VREFB5AN0	10		nCEO	DIFFIO_RX_R2II DIFFIO_TX_R3p	DIFFOUT_R2n DIFFOUT_R3p	T4	DQ1R	+	+
	VREFB5AN0	IO		NCEO	DIFFIO_TX_R3p	DIFFOUT_R4p	R2	DQ1R DQ1R	+	+
	VREFB5AN0			CvP_CONFDONE	DIFFIO_RX_R4p	DIFFOUT_R3n	R3	DQ1R DQ1R	+	
	VREFB5AN0	10		CVP_CONFIDONE	DIFFIO_TX_R3fi	DIFFOUT_R4n	T2	DQ1R DQ1R	+	
	VREFB5AN0			DEV OE	DIFFIO_RX_R4fi	DIFFOUT_R5p	P3	DQIK	+	+
	VREFB5AN0			nPERSTL0	DIFFIO_TX_RSp	DIFFOUT_R6p	P1	DQS1R	+	
	VREFB5AN0	10		DEV CLRn	DIFFIO_KX_R6p	DIFFOUT R5n	N2	DQ3TK	+	
	VREFB5AN0			nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	R1	DQSn1R	+	
	VREFB5AN0	10		IIFERGIEI	DIFFIO_TX_R7p	DIFFOUT_R7p	N4	DQ1R	+	-
	VREFB5AN0	10			DIFFIO_RX_R8p	DIFFOUT_R8p	M1	DQ1R	+	-
	VREFB5AN0	10			DIFFIO_TX_R7n	DIFFOUT_R7n	N3	DQIK	+	-
	VREFB5AN0				DIFFIO_RX_R8n	DIFFOUT_R8n	N1	DQ1R	+	-
	VREFB5BN0		CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	L2	DQIK	+	-
	VREFB5BN0	10	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	M2		+	-
	VREFB5BN0		CERON	1	DIFFIO RX R19p	DIFFOUT R19p	K2		+	
	VREFB5BN0		FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	M4		†	
	VREFB5BN0	10	THE BROOM, THE BROOM, THE BROOM		DIFFIO_TX_R20p	DIFFOUT_R19n	K1		†	
	VREFB5BN0		FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_RX_R19II	DIFFOUT R20n	13		†	
	VREFB5BN0			1	DIFFIO_RX_R21p	DIFFOUT_R21p	H1	1	†	t
	VREFB5BN0	10		Ì	DIFFIO_TX_R22p	DIFFOUT_R22p	J4	1	1	1
	VREFB5BN0	10		İ	DIFFIO_RX_R21n	DIFFOUT_R21n	J1		†	1
	VREFB5BN0			İ	DIFFIO_TX_R22n	DIFFOUT_R22n	J3		†	1
	VREFB5BN0	10		İ	DIFFIO_RX_R23p	DIFFOUT R23p	H2		†	1
	VREFB5BN0	10		Ì	DIFFIO_TX_R24p	DIFFOUT_R24p	H4	İ	1	1
	VREFB5BN0	10			DIFFIO_RX_R23n	DIFFOUT_R23n	G1		T	
	VREFB5BN0	10			DIFFIO_TX_R24n	DIFFOUT_R24n	H3		1	1
		GND					F3			
	VREFB7AN0	10			DIFFIO_RX_T17p	DIFFOUT_T17p	E1		GND	GND
	VREFB7AN0				DIFFIO_RX_T17n	DIFFOUT_T17n	D1		GND	GND
	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	F2			
	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	E2			
	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	F4		T_RESET#	T_RESET#
	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	E3			
	VREFB7AN0				DIFFIO_RX_T23n	DIFFOUT_T23n	D3			
	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	C1			
	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C7	DQ1T	T_DM_1	T_DM_1
	VREFB7AN0		CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	B1			
	VREFB7AN0				DIFFIO_TX_T26n	DIFFOUT_T26n	C6	DQ1T	T_DQ_15	T_DQ_15
	VREFB7AN0	10			DIFFIO_RX_T27p	DIFFOUT_T27p	C3	DQ1T	T_DQ_13	T_DQ_13
	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	D4	DQ1T	T_DQ_14	T_DQ_14
	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	C2	DQ1T	T_DQ_12	T_DQ_12
	VREFB7AN0				DIFFIO_TX_T28n	DIFFOUT_T28n	C4	DQ1T	T_CKE_0	T_CKE_0
	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	B2	DQS1T	T_DQS_1	T_DQS_1
							1	1 -	T 01/F 4	
	VREFB7AN0	IO		<u> </u>	DIFFIO_TX_T30p	DIFFOUT_T30p	D8		T_CKE_1	T CKE 1

Pin List CM13



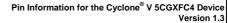
		T	T==						1	Note (1)
ank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin	HMC Pin
ımber					Channel				Assignment for	Assignment for
									DDR3/DDR2 (2)	LPDDR2
	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	C8	DQ1T	T_DQ_11	T_DQ_11
	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	A4	DQ1T	T_DQ_9	T DQ 9
	VREFB7AN0	10			DIFFIO_TX_T32p	DIFFOUT_T32p	B5	DQ1T	T_DQ_10	T_DQ_10
١	VREFB7AN0	10			DIFFIO_RX_T31n	DIFFOUT_T31n	A3	DQ1T	T_DQ_8	T_DQ_8
١	VREFB7AN0	10			DIFFIO_TX_T32n	DIFFOUT_T32n	B4		GND	GND
A	VREFB7AN0	10	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	B6			
١	VREFB7AN0				DIFFIO_TX_T34p	DIFFOUT_T34p	E8	DQ2T	T_DM_0	T_DM_0
Α	VREFB7AN0		CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	A5		T 00 T	T DO -
Α	VREFB7AN0				DIFFIO_TX_T34n	DIFFOUT_T34n	D9 B7	DQ2T	T_DQ_7	T_DQ_7
A	VREFB7AN0 VREFB7AN0				DIFFIO_RX_T35p DIFFIO_TX_T36p	DIFFOUT_T35p DIFFOUT_T36p	E10	DQ2T DQ2T	T_DQ_5 T_DQ_6	T_DQ_5 T_DQ_6
\ \	VREFB7AN0				DIFFIO_TX_T36p	DIFFOUT_T35n	A7	DQ2T	T_DQ_6	T_DQ_6
Δ.	VREFB7AN0	IO IO			DIFFIO_TX_T36n	DIFFOUT_T36n	D10	DQ2T	T_ODT_1	T_ODT_1
`	VREFB7AN0				DIFFIO_RX_T37p	DIFFOUT_T37p	A9	DQS2T	T_DQS_0	T_DQS_0
\	VREFB7AN0				DIFFIO_TX_T38p	DIFFOUT_T38p	E11		T_ODT_0	T_ODT_0
١	VREFB7AN0	Ю			DIFFIO_RX_T37n	DIFFOUT_T37n	A8	DQSn2T	T_DQS#_0	T_DQS#_0
١	VREFB7AN0	10			DIFFIO_TX_T38n	DIFFOUT_T38n	D11	DQ2T	T_DQ_3	T_DQ_3
١	VREFB7AN0				DIFFIO_RX_T39p	DIFFOUT_T39p	B9	DQ2T	T_DQ_1	T_DQ_1
١	VREFB7AN0				DIFFIO_TX_T40p	DIFFOUT_T40p	C11	DQ2T	T_DQ_2	T_DQ_2
	VREFB7AN0				DIFFIO_RX_T39n	DIFFOUT_T39n	A10	DQ2T	T_DQ_0	T_DQ_0
A	VREFB7AN0		RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	B10			
١	VREFB8AN0		CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	B12			L
١	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	E13	DQ3T	T_A_0	T_CA_0
4	VREFB8AN0		CLK9n	ļ	DIFFIO_RX_T41n	DIFFOUT_T41n	A12			<u> </u>
4	VREFB8AN0				DIFFIO_TX_T42n	DIFFOUT_T42n	D14	DQ3T	T_A_1	T_CA_1
Α	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	A14	DQ3T	T_A_4	T_CA_4
Α	VREFB8AN0		FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB	ļ	DIFFIO_TX_T44p	DIFFOUT_T44p	E15	DQ3T	T_A_2	T_CA_2
Α	VREFB8AN0		TOUR THOUSAND THE CHARLES		DIFFIO_RX_T43n	DIFFOUT_T43n	A13	DQ3T	T_A_5	T_CA_5
Α	VREFB8AN0 VREFB8AN0		FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn	 	DIFFIO_TX_T44n	DIFFOUT_T44n	D15	DQ3T	T_A_3 T_CK	T_CA_3
Α	VREFB8AN0 VREFB8AN0			1	DIFFIO_RX_T45p DIFFIO_TX_T46p	DIFFOUT_T45p DIFFOUT_T46p	C13 E17	DQS3T	T_A_6	T_CK T_CA_6
Α	VREFB8AN0				DIFFIO_TX_146p	DIFFOUT_146p	C12	DQSn3T	T CK#	T CK#
1	VREFB8AN0	10			DIFFIO_TX_T46n	DIFFOUT_T46n	E16	DQ3T3T	T_A_7	T_CA_7
`	VREFB8AN0				DIFFIO_TX_T4011	DIFFOUT_T47p	C14	DQ3T	T_BA_1	I_CA_/
`	VREFB8AN0				DIFFIO TX T48p	DIFFOUT_T48p	C16	DQ3T	T BA 0	+
`	VREFB8AN0	10			DIFFIO_RX_T47n	DIFFOUT_T47n	B14	DQ3T	T_BA_2	
À	VREFB8AN0	10			DIFFIO TX T48n	DIFFOUT T48n	B15	Dao.	GND	GND
A	VREFB8AN0	10	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	B16			1
Α.	VREFB8AN0	10			DIFFIO_TX_T50p	DIFFOUT_T50p	E18	DQ4T	T_CAS#	1
A	VREFB8AN0	10	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	A15			
A	VREFB8AN0				DIFFIO_TX_T50n	DIFFOUT_T50n	D19	DQ4T	T_RAS#	1
A	VREFB8AN0	10			DIFFIO_RX_T51p	DIFFOUT_T51p	B17	DQ4T	T_A_8	T_CA_8
A	VREFB8AN0	10			DIFFIO_TX_T52p	DIFFOUT_T52p	C19	DQ4T	T_A_10	
A	VREFB8AN0				DIFFIO_RX_T51n	DIFFOUT_T51n	A17	DQ4T	T_A_9	T_CA_9
A	VREFB8AN0				DIFFIO_TX_T52n	DIFFOUT_T52n	C18	DQ4T	T_A_11	
A	VREFB8AN0	10			DIFFIO_RX_T53p	DIFFOUT_T53p	A19	DQS4T	T_CS#_0	T_CS#_0
4	VREFB8AN0			Į.	DIFFIO_TX_T54p	DIFFOUT_T54p	C21		T_A_12	
Α	VREFB8AN0			ļ	DIFFIO_RX_T53n	DIFFOUT_T53n	A18	DQSn4T	T_CS#_1	T_CS#_1
Α	VREFB8AN0 VREFB8AN0				DIFFIO_TX_T54n	DIFFOUT_T54n	B20	DQ4T DQ4T	T_A_13	ļ
Α				1	DIFFIO_RX_T55p DIFFIO_TX_T56p	DIFFOUT_T55p	B19	DQ4T	T_A_14 T_WE#	+
Α	VREFB8AN0 VREFB8AN0	10		†	DIFFIO_TX_T55n	DIFFOUT_T56p DIFFOUT_T55n	D21 A20	DQ41 DQ4T	T_A_15	
Δ.	VINEE DOAINU	MSEL0	1	MSEL0	PILLIO VY 10011	Dii 1 001_100ii	A20 A23	DQHI	1_/_19	
Α.	 	CONF_DONE	1	CONF_DONE	†		A23 A22	1	-	+
Α	1	MSEL1	1	MSEL1	1	1	A24	1	1	t
Α	1	nSTATUS		nSTATUS			B22			1
A	1	nCE		nCE			A25			1
A		MSEL2		MSEL2	<u> </u>		B25			
4		MSEL3		MSEL3			B24			
Α		nCONFIG		nCONFIG			C23			
Α		MSEL4		MSEL4			C24			
		GND					C22			
		GND					A1			1
	ļ	GND			1		A11	1		ļ
	<u> </u>	GND		ļ	<u> </u>		AA1	1		
	ļ	GND					AA10			
	 	GND	1	1	1	+	AA15	+		
	 	GND GND		 			AA23 AB13	+	+	₩
	1	GND		-	 		AB13 AB24	+	-	
	1	GND GND		1	1	+		+	-	
	1	GND		1	1	+	AC10 P25	+	-	
	1	GND		†	+	<u> </u>	AC25	+	+	
	 	GND	1	1	†	<u>†</u>	AC25 AC5	1	1	
	1	GND			<u> </u>		AD17	+		t
	1	GND			<u> </u>		AD17	+		t
	1	GND		1	1	†	AE14	1	1	t
	1	GND		1			AE19			1
	i e	GND		İ	Ì		AE4	1	İ	
	1	GND					B13			1
		GND					B18			

Pin List CM13



ank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin	Note (
ımber			, , ,	_	Channel	•			Assignment for	Assignment fo
									DDR3/DDR2 (2)	LPDDR2
		GND					B23			
		GND					B8			
	1	GND GND				+	C25 C5	+		1
		GND					D12			
		GND					D17			
		GND					D2			
	1	GND GND			1	+	D22 D7	+		
		GND					E14			1
		GND					E23			
		GND					E25			
	_	GND GND					E4			
	+	GND			+		F24 G3	+		1
		GND					H25			
		GND					R23			
		GND					K4			
	+	GND GND			1		L1 L12	 	+	1
	+	GND			<u> </u>		L12 L14	+	+	†
		GND			İ		M11	İ		
-		GND					M13			
		GND GND			1		M15	1	+	
	+	GND GND	+		 		M23 P11	+	+	1
	1	GND	<u> </u>		1		P13	1	+	1
		GND					P15			
		GND					R12			
	1	GND GND			1	+	R14 R24	+		
		GND					T22			
		GND					T24			
		GND					U23			
	<u> </u>	GND GND					U25			
	1	GND					V23 V24			
		GND					V22			
		GND					Y25			
		GND					AB22			
	1	GND GND					F23			
	1	GND					AA24 G22			
	1	GND				İ	G24			1
		GND					H23			
		GND					J23			
	 	GND GND				+	J24			-
	1	GND			1		K22 K24			
		GND					L23			
		GND					L25			
	1	GND GND					M24 N22			
	1	GND				+	N22 N24	+		+
	1	GND			1		P23	1	1	
		GND					T1			
	1	GND					U3			
	 	GND			-		W22	1		1
	1	GND GND	<u> </u>		1		W24 Y4	1	+	t
		VCC			İ		L11			
		VCC					L13			
		VCC					L15			
	<u> </u>	VCC					M12 M14			
	1	VCC				†	N11			
		VCC					N12			
		VCC					N13	1		
		VCC			1		N14	1	+	
	+	VCC	+		 		N15 P12	+	+	1
	1	VCC	<u> </u>		1		P12	1	+	<u> </u>
		VCC			İ		R11	İ		
		VCC					R13			
	1	VCC			ļ		R15	1		
	+	DNU DNU			1		D24 E24	1		1
	+	DNU			 		G2	+	+	†
		DNU			<u> </u>		B11	İ		<u> </u>
		VCCPGM					AC21			

Pin List CM13



Note (1)

Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin	HMC Pin
Number			,	•	Channel				Assignment for	Assignment fo
									DDR3/DDR2 (2)	LPDDR2
									(-)	
		VCCPGM					D20			+
		VCCBAT					B21		1	+
		VCCIO3A					AB18			+
		VCCIOSA VCCIOSA				+	AC20			+
		VCCIO3A VCCIO3B					AC15			
										+
		VCCIO3B					AD12			
		VCCIO3B					AE9			
		VCCIO4A					AB3			
		VCCIO4A					AB8			
		VCCIO4A					AD2			
		VCCIO4A					AD7			
		VCCIO4A					W2			
		VCCIO5A					P2			
		VCCIO5A					R4			
		VCCIO5B				İ	J2		İ	
	1	VCCIO5B			1		M3		t	t
	† 	VCCIO3B VCCIO7A			1	†	A6	1	t	+
	1	VCCIO7A VCCIO7A	+	†	ł	1	B3	1	 	+
	+		-	<u> </u>					 	+
	 	VCCIO7A	ļ		ļ	ļ	C10		ļ	4
		VCCIO7A				1	E9		ļ	
		VCCIO7A					F1			
		VCCIO8A					A16			
		VCCIO8A					A21			
		VCCIO8A					C15			
		VCCIO8A					C20			
		VCCPD3A					AB16			1
		VCCPD3B4A					AB7			+
		VCCPD3B4A					AC13			+
		VCCPD5A					P4		1	+
	+	VCCPD5B					L4			+
		VCCPD7A8A					D13			+
										+
		VCCPD7A8A					D16			
		VCCPD7A8A					D6			
A	VREFB3AN0	VREFB3AN0					AD20			
В	VREFB3BN0	VREFB3BN0					AC11			
A	VREFB4AN0	VREFB4AN0					AE7			
A	VREFB5AN0	VREFB5AN0					V3			
В	VREFB5BN0	VREFB5BN0					K3			
A	VREFB7AN0	VREFB7AN0					C9			
A	VREFB8AN0	VREFB8AN0					C17			
•		VCCH_GXBL					L24		1	
	+	VCCH_GXBL		†			U24		†	†
		VCCL_GXBL		1	<u> </u>	1	K23			+
	+		-	<u> </u>			T23		 	+
	1	VCCL_GXBL			1				1	+
	 	RREF_TL	ļ		ļ	ļ	D25		ļ	4
		VCCA_FPLL				1	AB23		ļ	4
	1	VCCA_FPLL					D23			1
	1	VCCA_FPLL					U4		<u> </u>	1
		VCCA_FPLL					G4			
		VCC_AUX					AA13			
		VCC_AUX					AA18			
		VCC_AUX					AB6			
	İ	VCC_AUX			İ		D18			1
	1	VCC_AUX			1		D5		t	1
	1	VCC_AUX	+	†	ł	1	E12	1	 	+
	+		-	<u> </u>					 	+
	 	VCCE_GXBL	ļ		ļ	ļ	N23		ļ	4
		VCCE_GXBL				1	P24		ļ	
	1	VCCE_GXBL			Į		W23		1	1
		VCCE_GXBL		1	1	1	Y24	1	1	1

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.

(2) RESET pin is only applicable for DDR3 device.



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
GXB_L1		REFCLK1Ln					F5				
GXB_L1		REFCLK1Lp					G4				
GXB_L1		GXB_TX_L5n					D3				
GXB_L1		GXB_TX_L5p					D4				
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					C2				
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					C1				
GXB_L1		GXB_TX_L4n					E1				4
GXB_L1		GXB_TX_L4p					E2				
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2				
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					G1				
GXB_L1		GXB_TX_L3n					J1				
GXB_L1		GXB_TX_L3p					J2				
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p GXB_RX_L3n,GXB_REFCLK_L3n			-						
GXB_L1							L1				
GXB_L0 GXB_L0		GXB_TX_L2n GXB_TX_L2p					N1 N2				
				!							
GXB_L0 GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p GXB_RX_L2n,GXB_REFCLK_L2n					R2 R1				
	-										+
GXB_L0 GXB_L0	 	GXB_TX_L1n GXB_TX_L1p	+	 	 	 	U1 U2	1	1	1	+
	1	GXB_IX_L1p GXB_RX_L1p,GXB_REFCLK_L1p	+	<u> </u>	 	1		†	†	1	+
GXB_L0 GXB_L0	1	GXB_RX_L1p,GXB_REFCLK_L1p GXB_RX_L1n,GXB_REFCLK_L1n	+	<u> </u>	 	1	W2 W1	†	†	1	+
GXB_L0 GXB_L0	 	GXB_RX_L1n,GXB_REFCLK_L1n GXB_TX_L0n	+	+	+	1	W1 Y3	}	}	-	+
	-	GXB_TX_L00				+	13 Y4				+
GXB_L0 GXB_L0	1	GXB_IX_L0p GXB_RX_L0p,GXB_REFCLK_L0p	†	1	†	1	AA2	1	1	1	
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n			<u> </u>		AA1				+
GXB_L0		REFCLK0Lp		-			V4				+
GXB_L0		REFCLK0Ln		-			U4				
3A		TDO		TDO			M5				+
3A		nCSO		DATA4	<u> </u>		R4				+
3A		TMS		TMS	<u> </u>		P5				+
3A		AS_DATA3		DATA3			T4				+
3A		TCK		TCK			V5				+
3A		AS DATA2		DATA2			AA5				+
3A		TDI		TDI			W5				+
3A		AS_DATA1		DATA1			AB3				+
3A		DCLK		DCLK			V3				+
3A		AS_DATA0,ASDO		DATA0			AB4				+
34	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT B1n	R6	DQ1B			+
3A		10		DATA5	DIFFIO TX B2n	DIFFOUT B2n	U7	54.5			1
34		10		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	R5	DQ1B			+
3A		10		DATA7	DIFFIO_TX_B2p	DIFFOUT B2p	U8	DQ1B			†
3A		10		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	P6	DQSn1B			+
3A		10		DATA9	DIFFIO_TX_B4n	DIFFOUT B4n	W8	DQ1B			1
3A		10		DATA12	DIFFIO RX B3p	DIFFOUT B3p	N6	DQS1B			+
3A	VREFB3AN0			DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	W9				
3A	VREFB3AN0			DATA14	DIFFIO_RX_B5n	DIFFOUT B5n	T7	DQ1B			1
3A		10		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	U6	DQ1B			
3A	VREFB3AN0			CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T8	DQ1B			1
3A		10		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V6	DQ1B			
3A	VREFB3AN0			PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	M6				1
3A		IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	R7	DQ1B			
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	M7				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	P7	DQ1B			
3B		IO			DIFFIO_TX_B9n	DIFFOUT_B9n	AB6			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	V9	DQ2B		B_A_15	
3B	VREFB3BN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	AB5	DQ2B		B_WE#	
3B	VREFB3BN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	V10	DQ2B		B_A_14	
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	P8	DQSn2B		B_CS#_1	B_CS#_1
3B	VREFB3BN0	10			DIFFIO_TX_B12n	DIFFOUT_B12n	AA7	DQ2B		B_A_13	
3B	VREFB3BN0	10			DIFFIO_RX_B11p	DIFFOUT_B11p	N8	DQS2B		B_CS#_0	B_CS#_0
3B	VREFB3BN0	10			DIFFIO_TX_B12p	DIFFOUT_B12p	AB7			B_A_12	
3B	VREFB3BN0	10			DIFFIO_TX_B13n	DIFFOUT_B13n	AA8	DQ2B		B_A_11	1
3B	VREFB3BN0	10			DIFFIO_RX_B14n	DIFFOUT_B14n	T9	DQ2B		B_A_9	B_CA_9
3B	VREFB3BN0	10			DIFFIO_TX_B13p	DIFFOUT_B13p	AB8	DQ2B		B_A_10	
3B	VREFB3BN0	10			DIFFIO_RX_B14p	DIFFOUT_B14p	U10	DQ2B		B_A_8	B_CA_8
3B		10	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	M8				
3B		10			DIFFIO_TX_B16n	DIFFOUT_B16n	AA10	DQ2B		B_RAS#	
3B		10	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	M9				
3B	VREFB3BN0				DIFFIO_TX_B16p	DIFFOUT_B16p	AA9	DQ2B		B_CAS#	
3B	VREFB3BN0	10	1	1	DIFFIO TX B17n	DIFFOUT_B17n	Y10	1	1	GND	GND



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	T10	DQ3B		B_BA_2	
3B	VREFB3BN0	10			DIFFIO_TX_B17p	DIFFOUT_B17p	Y9	DQ3B		B_BA_0	
3B	VREFB3BN0	10			DIFFIO_RX_B18p	DIFFOUT_B18p	R9	DQ3B		B_BA_1	
3B	VREFB3BN0	10			DIFFIO_RX_B19n	DIFFOUT_B19n	U11	DQSn3B		B_CK#	B_CK#
3B	VREFB3BN0	10			DIFFIO_TX_B20n	DIFFOUT_B20n	R12	DQ3B		B_A_7	B_CA_7
3B	VREFB3BN0	10			DIFFIO_RX_B19p	DIFFOUT_B19p	U12	DQS3B		B_CK	B_CK
3B	VREFB3BN0	10			DIFFIO_TX_B20p	DIFFOUT_B20p	P12			B_A_6	B_CA_6
3B	VREFB3BN0	10	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB10	DQ3B		B_A_3	B_CA_3
3B	VREFB3BN0	10			DIFFIO_RX_B22n	DIFFOUT_B22n	R10	DQ3B		B_A_5	B_CA_5
3B	VREFB3BN0	10	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AB11	DQ3B		B_A_2	B_CA_2
3B	VREFB3BN0	10			DIFFIO RX B22p	DIFFOUT_B22p	R11	DQ3B		B_A_4	B_CA_4
3B	VREFB3BN0	10	CLK1n		DIFFIO RX B23n	DIFFOUT_B23n	P9				
3B	VREFB3BN0	10		1	DIFFIO TX B24n	DIFFOUT_B24n	Y11	DQ3B		B_A_1	B_CA_1
3B	VREFB3BN0	10	CLK1p	1	DIFFIO RX B23p	DIFFOUT B23p	N9				
3B	VREFB3BN0	10		1	DIFFIO TX B24p	DIFFOUT B24p	AA12	DQ3B		B_A_0	B_CA_0
4A	VREFB4AN0	10	RZQ 0	1	DIFFIO TX B25n	DIFFOUT B25n	AB13				
4A	VREFB4AN0	IO			DIFFIO RX B26n	DIFFOUT B26n	V13	DQ4B		B DQ 0	B DQ 0
4A	VREFB4AN0	IO			DIFFIO TX B25p	DIFFOUT B25p	AB12	DQ4B		B DQ 2	B DQ 2
4A	VREFB4AN0	10			DIFFIO RX B26p	DIFFOUT B26p	U13	DQ4B		B DQ 1	B DQ 1
4A	VREFB4AN0	lio	1	†	DIFFIO_RX_B26p	DIFFOUT B27n	T12	DQ4B DQSn4B	+	B_DQ_1 B DQS# 0	B_DQ_1 B DQS# 0
	VREFB4AN0	10	1	†	DIFFIO_RX_B27II	DIFFOUT_B28n	AA14	DQ3II4B DQ4B	+	B_DQ3#_0 B DQ 3	B_DQ3#_0 B DQ 3
411	VREFB4AN0 VREFB4AN0	10	+	1	DIFFIO_IX_B28n DIFFIO_RX_B27p	DIFFOUT_B28n DIFFOUT_B27p	T13	DQ4B DQS4B	+	B_DQ_3 B_DQS_0	B_DQ_3 B DQS 0
4M 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_RX_B27p DIFFIO_TX_B28p	DIFFOUT_B28p		DQ34B	+	B_DQS_0 B ODT 0	B_DQS_0 B ODT 0
4A		10		1			AA13	DOAD	+		
4A	VREFB4AN0	10			DIFFIO_TX_B29n	DIFFOUT_B29n	AB15	DQ4B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	10			DIFFIO_RX_B30n	DIFFOUT_B30n	Y14	DQ4B		B_DQ_4	B_DQ_4
4A	VREFB4AN0	10			DIFFIO_TX_B29p	DIFFOUT_B29p	AA15	DQ4B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	10			DIFFIO_RX_B30p	DIFFOUT_B30p	Y15	DQ4B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	10	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	V14				
4A	VREFB4AN0	10			DIFFIO_TX_B32n	DIFFOUT_B32n	AB17	DQ4B		B_DQ_7	B_DQ_7
4A	VREFB4AN0	10	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	V15				
4A	VREFB4AN0	10			DIFFIO_TX_B32p	DIFFOUT_B32p	AB18	DQ4B		B_DM_0	B_DM_0
4A	VREFB4AN0	10			DIFFIO_TX_B33n	DIFFOUT_B33n	AB20			GND	GND
4A	VREFB4AN0	10			DIFFIO_RX_B34n	DIFFOUT_B34n	Y16	DQ5B	DQ1B	B_DQ_8	B_DQ_8
4A	VREFB4AN0	10			DIFFIO_TX_B33p	DIFFOUT_B33p	AB21	DQ5B	DQ1B	B_DQ_10	B_DQ_10
4A	VREFB4AN0	10			DIFFIO RX B34p	DIFFOUT_B34p	Y17	DQ5B	DQ1B	B DQ 9	B_DQ_9
4A	VREFB4AN0	10			DIFFIO RX B35n	DIFFOUT_B35n	T14	DQSn5B	DQ1B	B_DQS#_1	B DQS# 1
4A	VREFB4AN0	10		1	DIFFIO_TX_B36n	DIFFOUT_B36n	AA17	DQ5B	DQ1B	B_DQ_11	B_DQ_11
4A	VREFB4AN0	IO		1	DIFFIO RX B35p	DIFFOUT B35p	U15	DQS5B	DQ1B	B_DQS_1	B DQS 1
4A	VREFB4AN0	IO			DIFFIO TX B36p	DIFFOUT B36p	AA18	Bucos	DQID	B CKE 1	B CKE 1
4A	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA19	DQ5B	DQ1B	B_CKE_0	B_CKE_0
4A	VREFB4AN0	10			DIFFIO_RX_B38n	DIFFOUT_B38n	V20	DQ5B	DQ1B	B_DQ_12	B_DQ_12
1Δ	VREFB4AN0	10			DIFFIO TX B37p	DIFFOUT_B37p	AA20	DQ5B	DQ1B	B DQ 14	B DQ 14
4A	VREFB4AN0	io			DIFFIO_RX_B38p	DIFFOUT_B38p	W19	DQ5B	DQ1B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	10	CLK3n	1	DIFFIO_RX_B39n	DIFFOUT_B39n	V16	DQJB	DQIB	D_DQ_13	D_DQ_13
40	VREFB4AN0	10	CERSII	1	DIFFIO_TX_B40n	DIFFOUT_B40n	AB22	DQ5B	DQ1B	B_DQ_15	B_DQ_15
4A		10	CLK3p	+		DIFFOUT_B39p	W16	DQSB	DQIB	B_DQ_13	B_DQ_13
4A	VREFB4AN0 VREFB4AN0	10	CLR3p		DIFFIO_RX_B39p		AA22	DQ5B	DQ1B	B DM 1	B DM 1
4A		10			DIFFIO_TX_B40p	DIFFOUT_B40p		DQSB	DQTB		
4A	VREFB4AN0	10		+	DIFFIO_TX_B41n	DIFFOUT_B41n	Y22	2002	2012	GND D. DO. 40	GND
4A	VREFB4AN0	10		+	DIFFIO_RX_B42n	DIFFOUT_B42n	Y20	DQ6B	DQ1B	B_DQ_16	B_DQ_16
4A	VREFB4AN0	10			DIFFIO_TX_B41p	DIFFOUT_B41p	W22	DQ6B	DQ1B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	10			DIFFIO_RX_B42p	DIFFOUT_B42p	Y19	DQ6B	DQ1B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	IO	1		DIFFIO_RX_B43n	DIFFOUT_B43n	P14	DQSn6B	DQSn1B	B_DQS#_2	B_DQS#_2
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	Y21	DQ6B	DQ1B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	10			DIFFIO_RX_B43p	DIFFOUT_B43p	R14	DQS6B	DQS1B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	IO		1	DIFFIO_TX_B44p	DIFFOUT_B44p	W21	1		B_RESET#	B_RESET#
4A	VREFB4AN0	10			DIFFIO_TX_B45n	DIFFOUT_B45n	U22	DQ6B	DQ1B	GND	GND
4A	VREFB4AN0	10			DIFFIO_RX_B46n	DIFFOUT_B46n	V19	DQ6B	DQ1B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	10			DIFFIO_TX_B45p	DIFFOUT_B45p	V21	DQ6B	DQ1B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	10			DIFFIO_RX_B46p	DIFFOUT_B46p	V18	DQ6B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	10			DIFFIO_RX_B47n	DIFFOUT_B47n	U16			GND	GND
4A	VREFB4AN0	10			DIFFIO_TX_B48n	DIFFOUT_B48n	U21	DQ6B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	10			DIFFIO RX B47p	DIFFOUT_B47p	U17	1		GND	GND
4A	VREFB4AN0	10			DIFFIO TX B48p	DIFFOUT B48p	U20	DQ6B	DQ1B	B DM 2	B DM 2
5A	VREFB5AN0	10	RZQ 1	1	DIFFIO TX R1p	DIFFOUT R1p	T19	DQ1R	24.2	5_56	
5A	VREFB5AN0	10	·	INIT_DONE	DIFFIO RX R2p	DIFFOUT_R2p	T18		+		+
5.A	VREFB5AN0	10	 	PR REQUEST	DIFFIO_RX_R2p	DIFFOUT R1n	T20	DQ1R	+	+	+
5.0	VREFB5AN0	10	<u> </u>	CRC ERROR	DIFFIO_TX_R1n	DIFFOUT R2n	T17	DOLK	+	+	+
JA E A		10						DO4B	+		+
)M	VREFB5AN0	10		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T22	DQ1R	+	-	+
AC	VREFB5AN0	IU	ļ	1	DIFFIO_RX_R4p	DIFFOUT_R4p	T15	DQ1R	-		4
iΑ	VREFB5AN0	10		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	R22	DQ1R			
5A	VREFB5AN0	10		1	DIFFIO_RX_R4n	DIFFOUT_R4n	R15	DQ1R			



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
A	VREFB5AN0	10		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	R21				
A	VREFB5AN0	IO		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R			
iΑ	VREFB5AN0	10		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	P22	DQ1R			
A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R			
A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	P19	DQ1R			
iΑ	VREFB5AN0	10			DIFFIO_RX_R8p	DIFFOUT_R8p	P16	DQ1R			
5A	VREFB5AN0	10			DIFFIO_TX_R7n	DIFFOUT_R7n	P18				
5A	VREFB5AN0				DIFFIO_RX_R8n	DIFFOUT_R8n	P17	DQ1R			<u> </u>
5B	VREFB5BN0	10	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	N16				
5B	VREFB5BN0	10			DIFFIO_TX_R18p	DIFFOUT_R18p	N20	DQ2R			
5B	VREFB5BN0	10	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	M16	DOOD			+
5B 5B	VREFB5BN0 VREFB5BN0	10			DIFFIO_TX_R18n DIFFIO_RX_R19p	DIFFOUT_R18n DIFFOUT_R19p	N21	DQ2R			+
5B	VREFB5BN0	10	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB	+	DIFFIO_TX_R20p	DIFFOUT_R20p	N19 M22	DQ2R			+
5B	VREFB5BN0	10	FFLL_BR_CLROUTO,FFLL_BR_CLROUTD,FFLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R19n	M18	DQ2R DQ2R			+
SB.	VREFB5BN0	10	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn	+	DIFFIO_TX_R20n	DIFFOUT_R20n	L22	DQ2R DQ2R			†
5B	VREFB5BN0	IO	TTEE_BIC_OEROOTI,TTEE_BIC_OEROOTII	+	DIFFIO_RX_R21p	DIFFOUT_R21p	K17	DQS2R			†
5B	VREFB5BN0	10			DIFFIO_TX_R22p	DIFFOUT_R22p	M20	DQOZIN			1
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT R21n	L17	DQSn2R			†
5B	VREFB5BN0	10			DIFFIO TX R22n	DIFFOUT R22n	M21	DQ2R			1
5B	VREFB5BN0	IO			DIFFIO RX R23p	DIFFOUT_R23p	L19	DQ2R			1
5B	VREFB5BN0	10			DIFFIO_TX_R24p	DIFFOUT_R24p	K21	DQ2R			1
5B	VREFB5BN0	10			DIFFIO_RX_R23n	DIFFOUT_R23n	L18	DQ2R			1
5B	VREFB5BN0	10			DIFFIO TX R24n	DIFFOUT R24n	K22				1
7A		GND					F17				
7A	VREFB7AN0	10			DIFFIO_RX_T1p	DIFFOUT_T1p	H21			GND	GND
7A	VREFB7AN0	10			DIFFIO_TX_T2p	DIFFOUT_T2p	E21	DQ1T	DQ1T	T_DM_4	T_DM_4
7A	VREFB7AN0	10			DIFFIO_RX_T1n	DIFFOUT_T1n	G21			GND	GND
7A	VREFB7AN0	10			DIFFIO_TX_T2n	DIFFOUT_T2n	D21	DQ1T	DQ1T	T_DQ_39	T_DQ_39
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	E19	DQ1T	DQ1T	T_DQ_37	T_DQ_37
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	C20	DQ1T	DQ1T	T_DQ_38	T_DQ_38
7A	VREFB7AN0	10			DIFFIO_RX_T3n	DIFFOUT_T3n	D19	DQ1T	DQ1T	T_DQ_36	T_DQ_36
7A	VREFB7AN0				DIFFIO_TX_T4n	DIFFOUT_T4n	B20	DQ1T	DQ1T	GND	GND
7A	VREFB7AN0				DIFFIO_RX_T5p	DIFFOUT_T5p	J21	DQS1T	DQS1T	T_DQS_4	T_DQS_4
7A	VREFB7AN0	10			DIFFIO_TX_T6p	DIFFOUT_T6p	B18			GND	GND
7A	VREFB7AN0				DIFFIO_RX_T5n	DIFFOUT_T5n	J22	DQSn1T	DQSn1T	T_DQS#_4	T_DQS#_4
7A	VREFB7AN0				DIFFIO_TX_T6n	DIFFOUT_T6n	B17	DQ1T	DQ1T	T_DQ_35	T_DQ_35
7A	VREFB7AN0	10			DIFFIO_RX_T7p	DIFFOUT_T7p	C21	DQ1T	DQ1T	T_DQ_33	T_DQ_33
7A	VREFB7AN0			_	DIFFIO_TX_T8p	DIFFOUT_T8p	G22	DQ1T	DQ1T	T_DQ_34	T_DQ_34
/A	VREFB7AN0	IO IO		_	DIFFIO_RX_T7n DIFFIO_TX_T8n	DIFFOUT_T7n	B21 F22	DQ1T	DQ1T	T_DQ_32 GND	T_DQ_32 GND
7.4	VREFB7AN0 VREFB7AN0	10			DIFFIO_TX_T8II DIFFIO_RX_T9p	DIFFOUT_T8n DIFFOUT_T9p	G20		-	GND	GND
7A	VREFB7AN0 VREFB7AN0	10		+	DIFFIO_RX_19p DIFFIO_TX_T10p	DIFFOUT_T10p	E22	DQ2T	DQ1T	T DM 3	T DM 3
7A	VREFB7AN0			+	DIFFIO_TX_T10p	DIFFOUT_T9n	H20	DQZI	DQTI	GND	GND
7A	VREFB7AN0	in			DIFFIO_TX_T10n	DIFFOUT_T10n	D22	DQ2T	DQ1T	T DQ 31	T DQ 31
7 A	VREFB7AN0	10			DIFFIO_TX_T10II	DIFFOUT T11p	C19	DQ2T	DQ1T	T DQ 29	T DQ 29
7A	VREFB7AN0	10			DIFFIO_TX_T12p	DIFFOUT_T12p	B22	DQ2T	DQ1T	T DQ 30	T DQ 30
7Δ	VREFB7AN0	in		+	DIFFIO RX T11n	DIFFOUT T11n	C18	DQ2T	DQ1T	T DQ 28	T DQ 28
7A	VREFB7AN0	10			DIFFIO TX T12n	DIFFOUT T12n	A22	DQ2T	DQ1T	GND	GND
7A	VREFB7AN0	IO		1	DIFFIO RX T13p	DIFFOUT_T13p	F19	DQS2T	DQ1T	T DQS 3	T DQS 3
7A	VREFB7AN0	10		1	DIFFIO_TX_T14p	DIFFOUT_T14p	E20		1	GND	GND
7A	VREFB7AN0	IO			DIFFIO RX T13n	DIFFOUT_T13n	F18	DQSn2T	DQ1T	T DQS# 3	T DQS# 3
7A	VREFB7AN0	10			DIFFIO_TX_T14n	DIFFOUT_T14n	F20	DQ2T	DQ1T	T_DQ_27	T_DQ_27
7A	VREFB7AN0	10			DIFFIO_RX_T15p	DIFFOUT_T15p	A18	DQ2T	DQ1T	T_DQ_25	T_DQ_25
7A	VREFB7AN0	10			DIFFIO_TX_T16p	DIFFOUT_T16p	A20	DQ2T	DQ1T	T_DQ_26	T_DQ_26
7A	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	A17	DQ2T	DQ1T	T_DQ_24	T_DQ_24
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A19			GND	GND
7A					DIFFIO_RX_T17p	DIFFOUT_T17p	K20			GND	GND
7A	VREFB7AN0				DIFFIO_TX_T18p	DIFFOUT_T18p	B16	DQ3T	DQ2T	T_DM_2	T_DM_2
7A	VREFB7AN0				DIFFIO_RX_T17n	DIFFOUT_T17n	K19			GND	GND
7A	VREFB7AN0	10			DIFFIO_TX_T18n	DIFFOUT_T18n	C16	DQ3T	DQ2T	T_DQ_23	T_DQ_23
7A	VREFB7AN0				DIFFIO_RX_T19p	DIFFOUT_T19p	D17	DQ3T	DQ2T	T_DQ_21	T_DQ_21
7A	VREFB7AN0	10			DIFFIO_TX_T20p	DIFFOUT_T20p	G17	DQ3T	DQ2T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	10			DIFFIO_RX_T19n	DIFFOUT_T19n	E16	DQ3T	DQ2T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	10			DIFFIO_TX_T20n	DIFFOUT_T20n	G16	DQ3T	DQ2T	GND	GND
7A	VREFB7AN0	10			DIFFIO_RX_T21p	DIFFOUT_T21p	G18	DQS3T	DQS2T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	10			DIFFIO_TX_T22p	DIFFOUT_T22p	J19		1	T_RESET#	T_RESET#
7A	VREFB7AN0	10			DIFFIO_RX_T21n	DIFFOUT_T21n	H18	DQSn3T	DQSn2T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	10			DIFFIO_TX_T22n	DIFFOUT_T22n	J18	DQ3T	DQ2T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	10			DIFFIO_RX_T23p	DIFFOUT_T23p	E15	DQ3T	DQ2T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	10			DIFFIO_TX_T24p	DIFFOUT_T24p	A15	DQ3T	DQ2T	T_DQ_18	T_DQ_18



Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin	HMC Pin
Number				garacon i unocoli	Channel					Assignment for DDR3/DDR2 (2)	Assignment for LPDDR2
7A	VREFB7AN0				DIFFIO_RX_T23n	DIFFOUT_T23n	F15	DQ3T	DQ2T	T_DQ_16	T_DQ_16
'A		IO		<u> </u>	DIFFIO_TX_T24n	DIFFOUT_T24n	A14			GND	GND
'A	VREFB7AN0		CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	H16				
'A	VREFB7AN0	10			DIFFIO_TX_T26p	DIFFOUT_T26p	J17	DQ4T	DQ2T	T_DM_1	T_DM_1
7A		10	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	H15				
7A	VREFB7AN0				DIFFIO_TX_T26n	DIFFOUT_T26n	K16	DQ4T	DQ2T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	10			DIFFIO_RX_T27p	DIFFOUT_T27p	C15	DQ4T	DQ2T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	10			DIFFIO_TX_T28p	DIFFOUT_T28p	G15	DQ4T	DQ2T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	10			DIFFIO_RX_T27n	DIFFOUT_T27n	B15	DQ4T	DQ2T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	10			DIFFIO_TX_T28n	DIFFOUT_T28n	F14	DQ4T	DQ2T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	10			DIFFIO_RX_T29p	DIFFOUT_T29p	H14	DQS4T	DQ2T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	Ю			DIFFIO_TX_T30p	DIFFOUT_T30p	B13			T_CKE_1	T_CKE_1
7A	VREFB7AN0	10			DIFFIO_RX_T29n	DIFFOUT_T29n	J13	DQSn4T	DQ2T	T_DQS#_1	T_DQS#_1
7A	VREFB7AN0	10			DIFFIO_TX_T30n	DIFFOUT_T30n	A13	DQ4T	DQ2T	T_DQ_11	T_DQ_11
7A		10			DIFFIO_RX_T31p	DIFFOUT_T31p	E14	DQ4T	DQ2T	T_DQ_9	T_DQ_9
7A		10			DIFFIO_TX_T32p	DIFFOUT_T32p	J11	DQ4T	DQ2T	T_DQ_10	T_DQ_10
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	F13	DQ4T	DQ2T	T_DQ_8	T_DQ_8
7A		10			DIFFIO_TX_T32n	DIFFOUT_T32n	H10			GND	GND
7A		10	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H13				
7A	VREFB7AN0				DIFFIO_TX_T34p	DIFFOUT_T34p	G11	DQ5T		T_DM_0	T_DM_0
7A	VREFB7AN0		CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G13				1
7A		10			DIFFIO_TX_T34n	DIFFOUT_T34n	F12	DQ5T		T_DQ_7	T_DQ_7
7A	VREFB7AN0				DIFFIO_RX_T35p	DIFFOUT_T35p	D13	DQ5T		T_DQ_5	T_DQ_5
7A		10			DIFFIO_TX_T36p	DIFFOUT_T36p	B12	DQ5T		T_DQ_6	T_DQ_6
7A		10			DIFFIO_RX_T35n	DIFFOUT_T35n	C13	DQ5T		T_DQ_4	T_DQ_4
7A		10			DIFFIO_TX_T36n	DIFFOUT_T36n	A12	DQ5T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	10			DIFFIO_RX_T37p	DIFFOUT_T37p	H11	DQS5T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	10			DIFFIO_TX_T38p	DIFFOUT_T38p	L8	↓		T_ODT_0	T_ODT_0
7A	VREFB7AN0	10			DIFFIO_RX_T37n	DIFFOUT_T37n	G12	DQSn5T		T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	10			DIFFIO_TX_T38n	DIFFOUT_T38n	K9	DQ5T		T_DQ_3	T_DQ_3
7A	VREFB7AN0	10			DIFFIO_RX_T39p	DIFFOUT_T39p	D12	DQ5T		T_DQ_1	T_DQ_1
7A	VREFB7AN0	10			DIFFIO_TX_T40p	DIFFOUT_T40p	C11	DQ5T		T_DQ_2	T_DQ_2
7A		10			DIFFIO_RX_T39n	DIFFOUT_T39n	E12	DQ5T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	10	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	B11				
8A		10	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	G10				
8A	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	L7	DQ6T		T_A_0	T_CA_0
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	F10				
8A	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	K7	DQ6T		T_A_1	T_CA_1
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	J7	DQ6T		T_A_4	T_CA_4
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	H8	DQ6T		T_A_2	T_CA_2
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	J8	DQ6T		T_A_5	T_CA_5
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	G8	DQ6T		T_A_3	T_CA_3
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	J9	DQS6T		T_CK	T_CK
8A	VREFB8AN0	10			DIFFIO_TX_T46p	DIFFOUT_T46p	A10			T_A_6	T_CA_6
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	H9	DQSn6T		T_CK#	T_CK#
8A		IO			DIFFIO_TX_T46n	DIFFOUT_T46n	A9	DQ6T		T_A_7	T_CA_7
8A	VREFB8AN0	10			DIFFIO_RX_T47p	DIFFOUT_T47p	B10	DQ6T		T_BA_1	
8A		10			DIFFIO_TX_T48p	DIFFOUT_T48p	A5	DQ6T		T_BA_0	
8A	VREFB8AN0	10			DIFFIO_RX_T47n	DIFFOUT_T47n	C9	DQ6T		T_BA_2	
8A	VREFB8AN0	10			DIFFIO_TX_T48n	DIFFOUT_T48n	B5			GND	GND
8A		10	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	E10				
8A	VREFB8AN0	10			DIFFIO_TX_T50p	DIFFOUT_T50p	B6	DQ7T		T_CAS#	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	F9				
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	B7	DQ7T		T_RAS#	
8A	VREFB8AN0	10			DIFFIO_RX_T51p	DIFFOUT_T51p	A8	DQ7T	T	T_A_8	T_CA_8
8A	VREFB8AN0	Ю			DIFFIO_TX_T52p	DIFFOUT_T52p	C6	DQ7T		T_A_10	
8A	VREFB8AN0	10			DIFFIO_RX_T51n	DIFFOUT_T51n	A7	DQ7T		T_A_9	T_CA_9
8A	VREFB8AN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	D6	DQ7T	T	T_A_11	T .
8A	VREFB8AN0	10			DIFFIO_RX_T53p	DIFFOUT_T53p	E9	DQS7T	T	T_CS#_0	T_CS#_0
8A	VREFB8AN0	Ю			DIFFIO_TX_T54p	DIFFOUT_T54p	D7			T_A_12	
8A	VREFB8AN0	10			DIFFIO_RX_T53n	DIFFOUT_T53n	D9	DQSn7T		T_CS#_1	T_CS#_1
8A	VREFB8AN0	10			DIFFIO TX T54n	DIFFOUT_T54n	C8	DQ7T	1	T A 13	1 -
8A	VREFB8AN0	10			DIFFIO RX T55p	DIFFOUT_T55p	G6	DQ7T	1	T A 14	1
8A	VREFB8AN0	10			DIFFIO_TX_T56p	DIFFOUT_T56p	F7	DQ7T	1	T WE#	1
8A	VREFB8AN0	10			DIFFIO_RX_T55n	DIFFOUT_T55n	H6	DQ7T	+	T A 15	†
8A	VREFB8AN0	10			DIFFIO_TX_T56n	DIFFOUT T56n	E7	 	+	GND	GND
9A	THE DOMEST	MSEL0		MSEL0	5 10_1X_100H	5 5510011	L6	+	+	CIAD	5.10
U/1	t	CONF DONE		CONF_DONE		+	K6	+	+	+	+
'QA			ļ			+		+	+		+
9A		MCEL 1	1	MCEL 1							
9A 9A		MSEL1 nSTATUS		MSEL1 nSTATUS		+	J6 H5	+	+		+





											Note (1)
Bank Number		Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
A.		MSEL2		MSEL2			A2				
9A		MSEL3		MSEL3			E5				
9A		nCONFIG		nCONFIG			A4				
9A		MSEL4		MSEL4			F3				
9A		GND					C5				
		GND					AB19				
		GND					AB14				
		GND					AB9				
		GND					AB2				
		GND					AB1				
		GND					AA11				
		GND					AA6				
		GND					AA4				
		GND					AA3	-			
	ļ	GND					Y18				
		GND					Y5				
		GND					Y2	-			
		GND					Y1	-			
	 	GND					W4	 		<u> </u>	+
	 	GND			1		W3	 		1	+
	-	GND			-		V22	_	-	-	+
	 	GND GND					V17	 		<u> </u>	+
	-				-		V12	_	-	-	+
		GND					V7	-			
		GND					V2				+
		GND					V1	-			
		GND					U9	-			
		GND					U5	-			
		GND					U3				
		GND					T21				
		GND					T16	-			
		GND					T2	-			
		GND					T1				
		GND					R13				
		GND					R3	-			
		GND					P10				
		GND					P4	-			
		GND GND					P2 P1	-			
	ļ	GND					P1				+
		GND					N22				
		GND GND					N17 N15	-			
		GND					N15				
		GND					N13 N11	-			
	ļ	GND					N11				+
	1	GND GND		-	-	-	N7	 	-	1	+
	1	GND		-	-	-	N5 N3	 	-	1	+
	1	GND		-	-	-	M14	 	-	1	+
	1	GND		-	-	-	M14 M12	 	-	1	+
	1	GND	 	 	1	+	M12 M10	 	1	1	+
	1	GND		-	-	-	M10 M4	 	-	1	+
	1	GND			1	+	M4 M2	 	1	1	+
	1	GND	 	 	1	+	M2 M1	 	1	1	+
	 	GND				1	L21	 		<u> </u>	+
	1	GND			1	+	L15	 	1	1	+
	1	GND	 	 	1	+	L15	 	1	1	+
	1	GND	 	 	1	+	L13	 	1	1	+
	1	GND	 	 	1	+	L5	 	1	1	+
	1	GND	 	 	1	+	L3	 	1	1	+
	1	GND	 	 	1	+	K14	 	1	1	+
	1	GND		 	1	1	K14 K12	† 	1	<u> </u>	+
	1	GND	 	 	1	+	K12 K10	 	1	1	+
		GND	 	 	1	+	K10 K8	 	1	1	+
		GND				1	K4	 		<u> </u>	+
		GND		-	-	-	K4 K2	 	-	1	+
		GND		-	-	-	K2 K1	 	-	1	+
		GND			-	-	J20	—	-	 	+
					1		J20 J15	 		1	+
	 	GND GND			1		J15 J5	 		1	+
	1			-	-	-	J5 J3	 	-	1	+
	1	GND		-	-	-		 	-	1	+
		GND		i	I		H22	1	1	1	I





							Note (1)				
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					H12				
		GND					H7				
		GND					H4				
		GND					H3				
		GND		İ			H2				
		GND					H1				
		GND					G19				
		GND					G9				
		GND					G3				
		GND					F16				
		GND					F6				
		GND					F2				-
		GND					F1				
		GND					E13				+
		GND					E4				
		GND					E3				ļ
		GND					D20				
		GND					D10				
		GND				1	D5		ļ		
		GND					D2				
		GND					D1				
		GND					C17				
		GND					C4				
		GND			İ	İ	C3	İ			
		GND			1		B14	1			1
		GND		1	†	†	B9	†	1	i e	1
		GND					B2				
		GND						+			
		GND					B1				+
		GND					A21				
		GND					A11				ļ
		VCC					P15				
		VCC					P13				
		VCC					P11				
		VCC					N14				
		VCC					N12				
		VCC					N10				
		VCC					M15				
		VCC		İ			M13				
		VCC					M11				
		VCC					L16				
		VCC					L14				
		VCC					L12				
		VCC					L12				-
											
		VCC					K15				
		VCC					K13				
	.	VCC	ļ		-	 	K11	-	ļ		4
		VCC			Ļ		J16				ļ
		VCC			Ļ		J14				ļ
		VCC			1		J12				ļ
		VCC				1	J10		ļ		
		DNU					B3				
		DNU]	B4				
		DNU					E17				
		DNU					L9				
	İ	VCCPGM			1	İ	V8	1			
		VCCPGM			İ		R19	1			1
	1	VCCPGM		1	†	†	F8	†	1	i e	1
	1	VCCBAT			 	1	A3	 			
		VCCIO3A	<u> </u>		t	1	T6	t	1		
	1	VCCIO3A VCCIO3A		 	+	 	Y8	+	1	1	1
	 				 			 	 		
	.	VCCIO3B	ļ		-	 	Y13	-	ļ		4
		VCCIO3B	ļ			ļ	W10		ļ		
		VCCIO3B			Ļ		T11				ļ
		VCCIO3B					R8				
		VCCIO4A					U19				
		VCCIO4A					AA21				
		VCCIO4A					AA16				
		VCCIO4A					W20	1			
	1	VCCIO4A VCCIO4A			†		W15	<u> </u>		1	t
		VCCIO4A VCCIO4A				1	U14		<u> </u>		
		VCCIO5A			 	1	R18	 			
		VOCIOUA	1	1	1		1/10	1	l	1	l



											,
Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin	HMC Pin
Number					Channel					Assignment for	Assignment for
										DDR3/DDR2 (2)	LPDDR2
		VCCIO5A					P20				
		VCCIO5B					M19				
		VCCIO5B					K18				
		VCCIO7A					B19				
		VCCIO7A					H17				
		VCCIO7A					G14				
		VCCIO7A					F21				
		VCCIO7A					F11				
		VCCIO7A					E18				
		VCCIO7A					D15				1
		VCCIO7A					C22				1
		VCCIO7A					C12				+
		VCCIO7A		†			A16				+
	†	VCCIO8A		+			A6	+		+	+
											+
		VCCI08A					G7				
		VCCIO8A			ļ	ļ	E8		ļ		
		VCCIO8A			ļ		C7	1		1	1
		VCCPD3A		ļ			W6	1		1	1
		VCCPD3B4A			<u> </u>		W17				
		VCCPD3B4A					W14				
		VCCPD3B4A					W12				
		VCCPD3B4A					W11				
		VCCPD5A					P21				
		VCCPD5B					N18				
		VCCPD5B					M17				+
		VCCPD7A8A		†			E11				+
											+
		VCCPD7A8A					D16 D14				+
		VCCPD7A8A									
		VCCPD7A8A					D8				
		VCCPD7A8A					C10				
3A	VREFB3AN0	VREFB3AN0					Y7				
3B	VREFB3BN0	VREFB3BN0					Y12				
4A	VREFB4AN0	VREFB4AN0					AB16				
5A	VREFB5AN0	VREFB5AN0					R20				
5B		VREFB5BN0					L20				
7A	VREFB7AN0	VREFB7AN0					C14				
8A	VREFB8AN0	VREFB8AN0					B8				
		NC					Y6				1
		NC					V11				1
		VCCH_GXBL		Ì	İ		M3	İ	1	İ	1
	 	VCCH_GXBL			1		T3	 	1	+	+
	-	VCCL_GXBL	<u> </u>		†	<u> </u>	P3	1	1	+	+
	1	VCCL_GXBL VCCL_GXBL	 	†	1	<u> </u>	K3	+	 	+	+
	-	RREF_TL			 		A1	+	+	+	+
	 				 			 	+	+	+
	1	VCCA_FPLL		 	 		T5	+	 	+	+
	!	VCCA_FPLL		ļ	ļ	-	F4	+	1	+	+
		VCCA_FPLL			ļ		U18	1		1	1
l		VCCA_FPLL		ļ			H19	1		1	1
		VCC_AUX					E6				
		VCC_AUX					D18				
		VCC_AUX					W18				
		VCC_AUX					W13				
		VCC_AUX					W7				
		VCC_AUX					D11				
	1	VCCE_GXBL			1		L4	1	1	1	1
	 	VCCE_GXBL			1		N4	 	1	+	+
 	1	VCCE_GXBL		1	†		K5	+	+	+	+
	 	VCCE_GXBL VCCE_GXBL	+	 	}	+	J4	+	+	+	+
		ACCE RYRE		1	1		J4		1		

Notes:

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.

(2) RESET pin is only applicable for DDR3 device.



											Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
SXB_L1		REFCLK1Ln					G4			DD110/DD112 (2)	L. DOILE
XB_L1		REFCLK1Lp					F5				
XB_L1		GXB_TX_L5n					D3				
XB_L1		GXB_TX_L5p					D4				
XB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					C2				
XB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					C1				
XB_L1		GXB_TX_L4n					E1				
XB_L1		GXB_TX_L4p					E2				
XB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2				
XB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					G1				
XB_L1		GXB_TX_L3n					J1				
XB_L1		GXB_TX_L3p					J2				
XB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					L2				
XB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					L1				
SXB_L0		GXB_TX_L2n					N1				+
XB_L0		GXB_TX_L2p					N2				
XB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					R2				+
XB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R1				+
XB_L0	 	GXB_TX_L1n		 			U1	<u> </u>	 	+	+
XB_L0	 	GXB_TX_L1p		 	1		U2	1	 	+	
XB_L0	-	GXB_RX_L1p,GXB_REFCLK_L1p		 	-		W2	1	 	-	
XB_L0 XB_L0	 	GXB_RX_L1n,GXB_REFCLK_L1n GXB_TX_L0n		 	1		W1 Y3	1	 	+	
							Y4				
XB_L0 XB_L0	}	GXB_TX_L0p GXB_RX_L0p,GXB_REFCLK_L0p		+	+	+	AA2	1	1	+	+
XB_L0 XB_L0	1	GXB_RX_L0p,GXB_REFCLK_L0p GXB_RX_L0n,GXB_REFCLK_L0n		<u> </u>	1	+	AA2 AA1	1	+	1	+
SXB_L0		REFCLK0Lp					V4				
SXB_L0		REFCLK0Lp REFCLK0Ln					V4 U4				
A A		TDO		TDO		+	V3				
Α		nCSO		DATA4			AB6				
Α		TMS		TMS			R4				
A .								+		-	-
A		AS_DATA3 TCK		DATA3		+	AA5 V5				
Α				TCK			T5				
A		AS_DATA2 TDI		DATA2 TDI			P5	+		-	-
Α		AS_DATA1		DATA1			W5				
Δ.		DCLK		DCLK		+	M5				
^		AS_DATA0,ASDO		DATA0		+	AB4				1
Δ.	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	P6	DQ1B			
A		10		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7	DQIB			
^		10		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	N6	DQ1B			
Α		10		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U6	DQ1B			
Λ.	VREFB3AN0	10		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	M6	DQSn1B			
A	VREFB3AN0			DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	R5	DQ1B			+
Δ.		in		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	M7	DQS1B			+
Λ	VREFB3AN0	10		DATA11	DIFFIO TX B4p	DIFFOUT B4p	R6	DQSTB			
Α	VREFB3AN0	10		DATA14	DIFFIO_TX_B4p	DIFFOUT_B5n	R7	DQ1B	1	1	1
Α		in		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	L7	DQ1B	1	1	†
Α	VREFB3AN0	10		CLKUSR	DIFFIO_TX_B6II	DIFFOUT_B5p	T7	DQ1B	1	1	†
A		10		DATA15	DIFFIO TX B6p	DIFFOUT_B6p	L8	DQ1B	†	1	1
Α		10		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	T8	- 4.5	1	1	1
Δ	VREFB3AN0	IO		PR_BONE PR_READY	DIFFIO TX B8n	DIFFOUT_B8n	P7	DQ1B	1	1	1
Α.		10		PR_ERROR	DIFFIO RX B7p	DIFFOUT B7p	T9	- 4.0	1	1	1
A		10			DIFFIO TX B8p	DIFFOUT B8p	P8	DQ1B	İ	i e	İ
B	VREFB3BN0	10		†	DIFFIO_TX_B0p	DIFFOUT B9n	V8	1	1	GND	GND
B		10			DIFFIO RX B10n	DIFFOUT B10n	N8	DQ2B	1	B A 15	1
В		10			DIFFIO_TX_B9p	DIFFOUT_B9p	W8	DQ2B	İ	B_WE#	İ
В		10			DIFFIO_RX_B10p	DIFFOUT_B10p	M8	DQ2B	1	B_A_14	1
В	VREFB3BN0				DIFFIO_RX_B11n	DIFFOUT_B11n	N9	DQSn2B	İ	B_CS#_1	B_CS#_1
3	VREFB3BN0				DIFFIO TX B12n	DIFFOUT_B12n	AA7	DQ2B	İ	B_A_13	1
3		10			DIFFIO_RX_B11p	DIFFOUT_B11p	N10	DQS2B	1	B_CS#_0	B CS# 0
В		10			DIFFIO TX B12p	DIFFOUT_B12p	AB7	1	İ	B_A_12	1
В		10			DIFFIO_TX_B13n	DIFFOUT_B13n	Y7	DQ2B	İ	B_A_11	1
В		10			DIFFIO_RX_B14n	DIFFOUT_B14n	U8	DQ2B	İ	B_A_9	B_CA_9
3		10		<u> </u>	DIFFIO_TX_B13p	DIFFOUT_B13p	W7	DQ2B	†	B_A_10	
	VREFB3BN0	10		†	DIFFIO_RX_B14p	DIFFOUT_B14p	V9	DQ2B	1	B_A_8	B_CA_8
3			ta	1	DIFFIO_RX_B15n	DIFFOUT_B15n	R9	- 4-0	1	1	
		IIO	ICLKOn.FPLL BL FBn								
3	VREFB3BN0	10	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15h			DQ2B		B RAS#	
B B	VREFB3BN0 VREFB3BN0	10			DIFFIO_TX_B16n	DIFFOUT_B16n	AB8	DQ2B		B_RAS#	
B B B	VREFB3BN0		CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15n DIFFIO_TX_B16n DIFFIO_RX_B15p DIFFIO_TX_B16p			DQ2B DQ2B		B_RAS# B_CAS#	



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
BB	VREFB3BN0	IO			DIFFIO RX B18n	DIFFOUT B18n	AA9	DQ3B		B BA 2	1
В	VREFB3BN0	10		İ	DIFFIO TX B17p	DIFFOUT_B17p	AA10	DQ3B		B BA 0	1
В	VREFB3BN0	10			DIFFIO RX B18p	DIFFOUT B18p	Y9	DQ3B		B BA 1	1
В	VREFB3BN0	10			DIFFIO RX B19n	DIFFOUT B19n	L9	DQSn3B		B CK#	B CK#
В	VREFB3BN0	10			DIFFIO TX B20n	DIFFOUT B20n	W11	DQ3B		B_A_7	B_CA_7
B	VREFB3BN0	10			DIFFIO RX B19p	DIFFOUT_B19p	M10	DQS3B		B CK	B CK
B	VREFB3BN0	IO			DIFFIO TX B20p	DIFFOUT_B20p	Y11			B A 6	B_CA_6
B	VREFB3BN0	10	FPLL BL CLKOUT1,FPLL BL CLKOUTn		DIFFIO TX B21n	DIFFOUT B21n	AB10	DQ3B		B A 3	B CA 3
BB	VREFB3BN0	10	THEE_BE_GENOGTH, TEE_BE_GENOGTH		DIFFIO RX B22n	DIFFOUT B22n	U10	DQ3B		B A 5	B CA 5
BB	VREFB3BN0	10	FPLL BL CLKOUTO,FPLL BL CLKOUTp,FPLL BL FB		DIFFIO TX B21p	DIFFOUT B21p	AB11	DQ3B		B A 2	B CA 2
B	VREFB3BN0	10	I FEE_BE_CEROOTO,I FEE_BE_CEROOTD,I FEE_BE_I B		DIFFIO RX B22p	DIFFOUT B22p	U11	DQ3B		B A 4	B CA 4
B	VREFB3BN0	10	CLK1n		DIFFIO_RX_B22p	DIFFOUT_B23n	T10	DQSB		D_A_4	B_CA_4
BB	VREFB3BN0	10	CENTI		DIFFIO_TX_B24n	DIFFOUT_B24n	R11	DQ3B		B_A_1	B_CA_1
RR.			011/4-				_	DQ3B			B_CA_I
BB BB	VREFB3BN0 VREFB3BN0	10	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	R10	DOOD		B_A_0	B_CA_0
IA	VREFB3BN0 VREFB4AN0	10	D70 0		DIFFIO_TX_B24p	DIFFOUT_B24p	P12	DQ3B		B_A_U	B_CA_U
" "		10	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AA13			2.20.0	
1A	VREFB4AN0	10			DIFFIO_RX_B26n	DIFFOUT_B26n	W12	DQ4B		B_DQ_0	B_DQ_0
1A	VREFB4AN0	10			DIFFIO_TX_B25p	DIFFOUT_B25p	AB13	DQ4B		B_DQ_2	B_DQ_2
1A	VREFB4AN0	10		!	DIFFIO_RX_B26p	DIFFOUT_B26p	Y12	DQ4B		B_DQ_1	B_DQ_1
4A	VREFB4AN0	10	ļ		DIFFIO_RX_B27n	DIFFOUT_B27n	U12	DQSn4B		B_DQS#_0	B_DQS#_0
4A	VREFB4AN0	10			DIFFIO_TX_B28n	DIFFOUT_B28n	R12	DQ4B		B_DQ_3	B_DQ_3
4A	VREFB4AN0	10			DIFFIO_RX_B27p	DIFFOUT_B27p	T12	DQS4B		B_DQS_0	B_DQS_0
4A	VREFB4AN0				DIFFIO_TX_B28p	DIFFOUT_B28p	T13	1		B_ODT_0	B_ODT_0
4A	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AB15	DQ4B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	10			DIFFIO_RX_B30n	DIFFOUT_B30n	W13	DQ4B		B_DQ_4	B_DQ_4
4A	VREFB4AN0	10			DIFFIO_TX_B29p	DIFFOUT_B29p	AB16	DQ4B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	10			DIFFIO_RX_B30p	DIFFOUT_B30p	V13	DQ4B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	10	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	T14				1
1A	VREFB4AN0	10			DIFFIO TX B32n	DIFFOUT B32n	AB18	DQ4B		B DQ 7	B DQ 7
4A	VREFB4AN0	10	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	U13				1
4A	VREFB4AN0	IO		İ	DIFFIO TX B32p	DIFFOUT_B32p	AA18	DQ4B		B DM 0	B DM 0
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AA19			GND	GND
4A	VREFB4AN0	IO		1	DIFFIO_RX_B34n	DIFFOUT_B34n	Y14	DQ5B	DQ1B	B DQ 8	B DQ 8
4A	VREFB4AN0				DIFFIO TX B33p	DIFFOUT_B33p	Y19	DQ5B	DQ1B	B DQ 10	B DQ 10
1Δ	VREFB4AN0	10			DIFFIO RX B34p	DIFFOUT B34p	W14	DQ5B	DQ1B	B DQ 9	B DQ 9
4A	VREFB4AN0	10			DIFFIO RX B35n	DIFFOUT B35n	P14	DQSn5B	DQ1B	B DQS# 1	B DQS# 1
4A	VREFB4AN0	10			DIFFIO_TX_B36n	DIFFOUT_B36n	AA20	DQ5B	DQ1B	B_DQ_11	B_DQ_11
4.0	VREFB4AN0	10			DIFFIO RX B35p	DIFFOUT_B35p	R14	DQS5B	DQ1B	B_DQS_1	B DQS 1
4A 4Δ	VREFB4AN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	Y20	DQSSB	DQIB	B_CKE_1	B_CKE_1
44	VREFB4AN0	10		1		DIFFOUT_B37n	AA15	DQ5B	DQ1B	B_CKE_0	B_CKE_0
4A		lio			DIFFIO_TX_B37n			DQ5B			
4A 4A	VREFB4AN0				DIFFIO_RX_B38n	DIFFOUT_B38n	U15		DQ1B	B_DQ_12	B_DQ_12
4A	VREFB4AN0	10			DIFFIO_TX_B37p	DIFFOUT_B37p	Y15	DQ5B	DQ1B	B_DQ_14	B_DQ_14
1A	VREFB4AN0	10			DIFFIO_RX_B38p	DIFFOUT_B38p	V15	DQ5B	DQ1B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	10	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	R15	ļ			
4A	VREFB4AN0	10			DIFFIO_TX_B40n	DIFFOUT_B40n	AB20	DQ5B	DQ1B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	10	CLK3p	ļ	DIFFIO_RX_B39p	DIFFOUT_B39p	T15			\bot	
4A	VREFB4AN0	10			DIFFIO_TX_B40p	DIFFOUT_B40p	AB21	DQ5B	DQ1B	B_DM_1	B_DM_1
4A	VREFB4AN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AB22	1		GND	GND
4A	VREFB4AN0	10			DIFFIO_RX_B42n	DIFFOUT_B42n	Y16	DQ6B	DQ1B	B_DQ_16	B_DQ_16
1A	VREFB4AN0	10			DIFFIO_TX_B41p	DIFFOUT_B41p	AA22	DQ6B	DQ1B	B_DQ_18	B_DQ_18
1A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	Y17	DQ6B	DQ1B	B_DQ_17	B_DQ_17
1A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	U16	DQSn6B	DQSn1B	B_DQS#_2	B_DQS#_2
4A	VREFB4AN0	10			DIFFIO_TX_B44n	DIFFOUT_B44n	AA17	DQ6B	DQ1B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	10			DIFFIO_RX_B43p	DIFFOUT_B43p	U17	DQS6B	DQS1B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	IO			DIFFIO TX B44p	DIFFOUT B44p	AB17			B RESET#	B RESET#
4A	VREFB4AN0	10		İ	DIFFIO TX B45n	DIFFOUT B45n	Y22	DQ6B	DQ1B	GND	GND
4A	VREFB4AN0	10			DIFFIO RX B46n	DIFFOUT_B46n	V18	DQ6B	DQ1B	B_DQ_20	B DQ 20
1A	VREFB4AN0	10		1	DIFFIO TX B45p	DIFFOUT B45p	Y21	DQ6B	DQ1B	B_DQ_22	B DQ 22
IA.	VREFB4AN0	10		1	DIFFIO_RX_B46p	DIFFOUT B46p	W18	DQ6B	DQ1B	B_DQ_21	B DQ 21
IA.	VREFB4AN0	10		<u> </u>	DIFFIO RX B47n	DIFFOUT B47n	W16	2400	DOID	GND	GND
1A	VREFB4AN0	IO	 	†	DIFFIO_RX_B47II	DIFFOUT_B48n	W21	DQ6B	DQ1B	B DQ 23	B DQ 23
IA	VREFB4AN0	10	<u> </u>	 	DIFFIO_TX_B46II	DIFFOUT_B47p	W17	2400	DQID	GND	GND
1A 1A				 				DOEB	DO4B	B DM 2	B DM 2
	VREFB4AN0	10	D70 4	 	DIFFIO_TX_B48p	DIFFOUT_B48p	W22	DQ6B	DQ1B	D_DIVI_2	D_UIVI_Z
5A	VREFB5AN0	10	RZQ_1	INIT BONE	DIFFIO_TX_R1p	DIFFOUT_R1p	U22	DQ1R		+	4
iΑ	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V20				
5A	VREFB5AN0	10		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	U21	DQ1R		+	
Α.	VREFB5AN0	10		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V19	1			
PA.		IO	1	nCFO	DIFFIO_TX_R3p	DIFFOUT_R3p	T19	DQ1R	1	1	1
A	VREFB5AN0	IU		HOLO	DII I IO_IX_R3p	Dil 1 OO1_Rop	110				
iA A	VREFB5AN0	10			DIFFIO_RX_R4p	DIFFOUT_R4p	T17	DQ1R			<u> </u>
5A 5A 5A		***		CvP_CONFDONE			1				



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
A	VREFB5AN0	10		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	T22				
5A	VREFB5AN0	10		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R			
5A	VREFB5AN0	10		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	R22	DQ1R			
5A	VREFB5AN0	10		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R			
5A	VREFB5AN0	10			DIFFIO_TX_R7p	DIFFOUT_R7p	R20	DQ1R			
5A	VREFB5AN0	10		İ	DIFFIO RX R8p	DIFFOUT_R8p	R19	DQ1R			1
5A	VREFB5AN0	IO			DIFFIO TX R7n	DIFFOUT_R7n	R21				
5A	VREFB5AN0	IO			DIFFIO RX R8n	DIFFOUT_R8n	P19	DQ1R			
5B	VREFB5BN0	IO	CLK7p,FPLL BR FBp		DIFFIO RX R9p	DIFFOUT R9p	M16				
5B	VREFB5BN0	IO			DIFFIO TX R10p	DIFFOUT_R10p	E21	DQ2R			+
5B	VREFB5BN0	IO	CLK7n,FPLL BR FBn		DIFFIO RX R9n	DIFFOUT R9n	M17	DOLLIN			+
5B	VREFB5BN0	10	OCIVITATI EC_DIV_1 DII		DIFFIO TX R10n	DIFFOUT R10n	D22	DQ2R	1		+
5B	VREFB5BN0	10			DIFFIO_RX_R11p	DIFFOUT_R11p	L19	DQ2R			+
5B	VREFB5BN0	10			DIFFIO_TX_R12p	DIFFOUT_R12p	K21	DQ2R			+
5B	VREFB5BN0	10			DIFFIO RX R11n	DIFFOUT R11n	L20	DQ2R	+	_	+
5B	VREFB5BN0	10			DIFFIO_RX_R11II	DIFFOUT_R12n	J21	DQ2R DQ2R			+
5B	VREFB5BN0	10			DIFFIO_TX_R12II	DIFFOUT R13p	L15		+	-	+
		10						DQS2R	-	_	+
5B	VREFB5BN0	10			DIFFIO_TX_R14p	DIFFOUT_R14p	G22	200 00	-	_	+
5B	VREFB5BN0	10	ļ		DIFFIO_RX_R13n	DIFFOUT_R13n	K15	DQSn2R	1	_	+
5B	VREFB5BN0	10	ļ		DIFFIO_TX_R14n	DIFFOUT_R14n	G21	DQ2R	1	_	+
5B	VREFB5BN0	10			DIFFIO_RX_R15p	DIFFOUT_R15p	L18	DQ2R	1	_	
5B	VREFB5BN0	10			DIFFIO_TX_R16p	DIFFOUT_R16p	G20	DQ2R			
5B	VREFB5BN0	10			DIFFIO_RX_R15n	DIFFOUT_R15n	K19	DQ2R			
5B	VREFB5BN0	10			DIFFIO_TX_R16n	DIFFOUT_R16n	H21	1			1
5B	VREFB5BN0	10	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	L17				
5B	VREFB5BN0	10			DIFFIO_TX_R18p	DIFFOUT_R18p	E20	DQ3R			
5B	VREFB5BN0	10	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	K17				
5B	VREFB5BN0	10			DIFFIO_TX_R18n	DIFFOUT_R18n	F20	DQ3R			
5B	VREFB5BN0	10			DIFFIO_RX_R19p	DIFFOUT_R19p	H20	DQ3R			
5B	VREFB5BN0	10	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	G18	DQ3R			
5B	VREFB5BN0	10		İ	DIFFIO RX R19n	DIFFOUT_R19n	H19	DQ3R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn	İ	DIFFIO TX R20n	DIFFOUT_R20n	G17	DQ3R			1
5B	VREFB5BN0	IO			DIFFIO RX R21p	DIFFOUT R21p	K16	DQS3R			
5B	VREFB5BN0	IO			DIFFIO TX R22p	DIFFOUT R22p	F19				
5B	VREFB5BN0	10			DIFFIO RX R21n	DIFFOUT R21n	J16	DQSn3R	1		
5B	VREFB5BN0	10			DIFFIO TX R22n	DIFFOUT R22n	F18	DQ3R	1		+
5B	VREFB5BN0	10			DIFFIO_RX_R23p	DIFFOUT_R23p	J17	DQ3R	+	_	+
5B	VREFB5BN0	10			DIFFIO_TX_R24p	DIFFOUT R24p	J19	DQ3R			_
5B	VREFB5BN0	io			DIFFIO_TX_R24p	DIFFOUT R23n	J18	DQ3R	+	+	+
5B		10						DQ3R	+	-	+
	VREFB5BN0				DIFFIO_TX_R24n	DIFFOUT_R24n	H18		-	_	
7A		GND					F17			O.U.D.	ONE
7A	VREFB7AN0	10			DIFFIO_RX_T17p	DIFFOUT_T17p	H16			GND	GND
7A	VREFB7AN0	10			DIFFIO_TX_T18p	DIFFOUT_T18p	C21	DQ1T	DQ1T	T_DM_2	T_DM_2
7A	VREFB7AN0	10			DIFFIO_RX_T17n	DIFFOUT_T17n	G16			GND	GND
7A	VREFB7AN0	10			DIFFIO_TX_T18n	DIFFOUT_T18n	C20	DQ1T	DQ1T	T_DQ_23	T_DQ_23
7A	VREFB7AN0	10			DIFFIO_RX_T19p	DIFFOUT_T19p	D18	DQ1T	DQ1T	T_DQ_21	T_DQ_21
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	B20	DQ1T	DQ1T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	10			DIFFIO_RX_T19n	DIFFOUT_T19n	E17	DQ1T	DQ1T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	10			DIFFIO_TX_T20n	DIFFOUT_T20n	B21	DQ1T	DQ1T	GND	GND
7A	VREFB7AN0	10			DIFFIO_RX_T21p	DIFFOUT_T21p	G15	DQS1T	DQS1T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	10			DIFFIO_TX_T22p	DIFFOUT_T22p	B22			T_RESET#	T_RESET#
7A	VREFB7AN0	10			DIFFIO_RX_T21n	DIFFOUT_T21n	G14	DQSn1T	DQSn1T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	10			DIFFIO_TX_T22n	DIFFOUT_T22n	A22	DQ1T	DQ1T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	10			DIFFIO_RX_T23p	DIFFOUT_T23p	E16	DQ1T	DQ1T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	10			DIFFIO TX T24p	DIFFOUT_T24p	A20	DQ1T	DQ1T	T DQ 18	T DQ 18
7A	VREFB7AN0	10			DIFFIO RX T23n	DIFFOUT_T23n	D17	DQ1T	DQ1T	T_DQ_16	T DQ 16
7A	VREFB7AN0	10			DIFFIO TX T24n	DIFFOUT_T24n	A19	T	1	GND	GND
'A	VREFB7AN0	10	CLK11p		DIFFIO RX T25p	DIFFOUT_T25p	G13	†	1	7	1
'Α	VREFB7AN0	10		1	DIFFIO_TX_T26p	DIFFOUT_T26p	C19	DQ2T	DQ1T	T_DM_1	T DM 1
'A	VREFB7AN0	10	CLK11n		DIFFIO RX T25n	DIFFOUT T25n	F14		2411		
7A	VREFB7AN0	io			DIFFIO_RX_125II	DIFFOUT_T26n	C18	DQ2T	DQ1T	T DQ 15	T DQ 15
7.0	VREFB7AN0	10			DIFFIO_TX_T26II	DIFFOUT_T27p	C16	DQ2T	DQ1T	T DQ_13	T DQ_13
7 A	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_12/p	DIFFOUT_127p DIFFOUT_T28p	B16	DQ2T	DQ1T DQ1T	T_DQ_13	T_DQ_13
7A		10									
'A	VREFB7AN0	10		ļ	DIFFIO_RX_T27n	DIFFOUT_T27n	C15	DQ2T	DQ1T	T_DQ_12	T_DQ_12
Ά	VREFB7AN0	10	ļ		DIFFIO_TX_T28n	DIFFOUT_T28n	B15	DQ2T	DQ1T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	G12	DQS2T	DQ1T	T_DQS_1	T_DQS_1
'A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	A18			T_CKE_1	T_CKE_1
Ά	VREFB7AN0	10			DIFFIO_RX_T29n	DIFFOUT_T29n	H12	DQSn2T	DQ1T	T_DQS#_1	T_DQS#_1
/A	VREFB7AN0	10			DIFFIO_TX_T30n	DIFFOUT_T30n	A17	DQ2T	DQ1T	T_DQ_11	T_DQ_11
/A	VREFB7AN0	10			DIFFIO_RX_T31p	DIFFOUT_T31p	F15	DQ2T	DQ1T	T_DQ_9	T_DQ_9
7A	VREFB7AN0	10			DIFFIO_TX_T32p	DIFFOUT_T32p	B18	DQ2T	DQ1T	T_DQ_10	T_DQ_10



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
A	VREFB7AN0	10			DIFFIO_RX_T31n	DIFFOUT_T31n	E14	DQ2T	DQ1T	T_DQ_8	T_DQ_8
A	VREFB7AN0	10			DIFFIO_TX_T32n	DIFFOUT_T32n	B17			GND	GND
A	VREFB7AN0	10	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H10				
A	VREFB7AN0	10			DIFFIO_TX_T34p	DIFFOUT_T34p	A15	DQ3T		T_DM_0	T_DM_0
Α	VREFB7AN0	10	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G11				
Α	VREFB7AN0	10			DIFFIO_TX_T34n	DIFFOUT_T34n	A14	DQ3T		T_DQ_7	T_DQ_7
Ά	VREFB7AN0	10			DIFFIO_RX_T35p	DIFFOUT_T35p	D13	DQ3T		T_DQ_5	T_DQ_5
Ά	VREFB7AN0	10			DIFFIO_TX_T36p	DIFFOUT_T36p	C14	DQ3T		T_DQ_6	T_DQ_6
'A	VREFB7AN0	10			DIFFIO_RX_T35n	DIFFOUT_T35n	C13	DQ3T		T_DQ_4	T_DQ_4
Ά	VREFB7AN0	10			DIFFIO_TX_T36n	DIFFOUT_T36n	D14	DQ3T		T_ODT_1	T_ODT_1
Ά	VREFB7AN0	10			DIFFIO RX T37p	DIFFOUT_T37p	H9	DQS3T		T_DQS_0	T DQS 0
Ά	VREFB7AN0	10			DIFFIO TX T38p	DIFFOUT_T38p	A13			T ODT 0	T ODT 0
Α	VREFB7AN0	10		Ì	DIFFIO RX T37n	DIFFOUT_T37n	G8	DQSn3T		T_DQS#_0	T_DQS#_0
A	VREFB7AN0	IO		1	DIFFIO TX T38n	DIFFOUT T38n	B13	DQ3T		T DQ 3	T DQ 3
Δ.	VREFB7AN0	10			DIFFIO RX T39p	DIFFOUT T39p	E12	DQ3T		T_DQ_1	T DQ 1
Ά.	VREFB7AN0	10			DIFFIO TX T40p	DIFFOUT_T40p	B12	DQ3T		T_DQ_2	T DQ 2
^	VREFB7AN0	lio		+	DIFFIO RX T39n	DIFFOUT T39n	F12	DQ3T		T DQ 0	T DQ 0
A		lio	D70 0	+				DQ31		I_DQ_0	1_DQ_0
A	VREFB7AN0	10	RZQ_2	-	DIFFIO_TX_T40n	DIFFOUT_T40n	A12				+
iA.	VREFB8AN0	10	CLK9p	1	DIFFIO_RX_T41p	DIFFOUT_T41p	G10	DO 17	4	T A C	T 04 2
A	VREFB8AN0	10			DIFFIO_TX_T42p	DIFFOUT_T42p	C11	DQ4T	1	T_A_0	T_CA_0
A	VREFB8AN0	10	CLK9n	1	DIFFIO_RX_T41n	DIFFOUT_T41n	F10	1			1
A	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	B11	DQ4T	1	T_A_1	T_CA_1
A	VREFB8AN0	10			DIFFIO_RX_T43p	DIFFOUT_T43p	D11	DQ4T		T_A_4	T_CA_4
A	VREFB8AN0	10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	A8	DQ4T		T_A_2	T_CA_2
Α	VREFB8AN0	10			DIFFIO_RX_T43n	DIFFOUT_T43n	E11	DQ4T		T_A_5	T_CA_5
A	VREFB8AN0	10	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	A7	DQ4T		T_A_3	T_CA_3
A	VREFB8AN0	10			DIFFIO_RX_T45p	DIFFOUT_T45p	J9	DQS4T		T_CK	T_CK
Λ.	VREFB8AN0	10		1	DIFFIO TX T46p	DIFFOUT T46p	F8	54011		T A 6	T CA 6
^	VREFB8AN0	10		†	DIFFIO_RX_T45n	DIFFOUT_T45n	J8	DQSn4T		T_CK#	T_CK#
Α		10		-			E7				T_CA_7
4	VREFB8AN0	10			DIFFIO_TX_T46n	DIFFOUT_T46n		DQ4T		T_A_7	I_CA_/
٩	VREFB8AN0	10		4	DIFFIO_RX_T47p	DIFFOUT_T47p	C10	DQ4T		T_BA_1	
A	VREFB8AN0	10			DIFFIO_TX_T48p	DIFFOUT_T48p	C6	DQ4T		T_BA_0	
A	VREFB8AN0	10			DIFFIO_RX_T47n	DIFFOUT_T47n	C9	DQ4T		T_BA_2	
A	VREFB8AN0	10			DIFFIO_TX_T48n	DIFFOUT_T48n	D7			GND	GND
A	VREFB8AN0	10	CLK8p,FPLL_TL_FBp		DIFFIO RX T49p	DIFFOUT_T49p	K7				
A	VREFB8AN0	10			DIFFIO_TX_T50p	DIFFOUT_T50p	A10	DQ5T		T_CAS#	
A	VREFB8AN0	10	CLK8n,FPLL_TL_FBn	Ì	DIFFIO_RX_T49n	DIFFOUT_T49n	J7				1
A	VREFB8AN0	IO		Ì	DIFFIO_TX_T50n	DIFFOUT_T50n	A9	DQ5T		T_RAS#	1
A	VREFB8AN0	IO			DIFFIO RX T51p	DIFFOUT_T51p	D9	DQ5T		T A 8	T CA 8
A	VREFB8AN0	10			DIFFIO_TX_T52p	DIFFOUT_T52p	B6	DQ5T		T_A_10	1_0/_0
A	VREFB8AN0	10		†	DIFFIO_RX_T51n	DIFFOUT_T51n	D8	DQ5T		T_A_9	T CA 9
Α.	VREFB8AN0	io		†	DIFFIO_TX_T52n	DIFFOUT T52n	B5	DQ5T		T A 11	1_0/(_5
A		lio		+						T_CS#_0	T_CS#_0
A	VREFB8AN0	10			DIFFIO_RX_T53p	DIFFOUT_T53p	H8	DQS5T			1_CS#_0
A	VREFB8AN0	10		4	DIFFIO_TX_T54p	DIFFOUT_T54p	C8			T_A_12	
A	VREFB8AN0	10	1		DIFFIO_RX_T53n	DIFFOUT_T53n	G7	DQSn5T		T_CS#_1	T_CS#_1
A	VREFB8AN0	10		1	DIFFIO_TX_T54n	DIFFOUT_T54n	B8	DQ5T		T_A_13	
A	VREFB8AN0	10			DIFFIO_RX_T55p	DIFFOUT_T55p	H6	DQ5T		T_A_14	1
A	VREFB8AN0	10			DIFFIO_TX_T56p	DIFFOUT_T56p	E6	DQ5T		T_WE#	
4	VREFB8AN0	10			DIFFIO_RX_T55n	DIFFOUT_T55n	G6	DQ5T		T_A_15	
A	VREFB8AN0	10			DIFFIO_TX_T56n	DIFFOUT_T56n	F7			GND	GND
A		MSEL0		MSEL0			L6				
ΙA		CONF DONE		CONF DONE			J6				
A.	İ	MSEL1		MSEL1		1	K6				
A		nSTATUS		nSTATUS			G5				1
Δ		nCE		nCE		1	H5	+	+	+	+
Δ	1	MSEL2	+	MSEL2	1	+	A2	+	+	+	+
1					1			-	+		+
4	-	MSEL3		MSEL3	ļ	1	E5	1	1		+
4		nCONFIG	1	nCONFIG		ļ	A4	-			
١		MSEL4		MSEL4			C5				
١	1	GND		1	1		F3		1		1
		GND					F21				
		GND					AB19				
		GND		1			AB2				1
		GND		1			AB1				1
		GND	 	1	1	1	AA16	+	+		+
		GND		1	1	-	AA16 AA11	+	+		+
				+				1	1	_	+
		GND	1			ļ	AA4	-			
		GND					AA3				
		GND					Y13				
		GND					Y8				
		GND					Y5				





Sank VRE		GND GND GND GND GND GND GND GND GND GND	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel		Y2 Y1 W20 W4 W3 V22 V17 V2 V1 U19 U14 U9 U5 U3 T11 T2 T1 R13	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND GND GND GND GND GND GND GND GND GND					Y1 W20 W4 W3 V22 V17 V2 V1 U19 U14 U9 U5 U3 T11 T2 T1				
		GND GND GND GND GND GND GND GND GND GND					Y1 W20 W4 W3 V22 V17 V2 V1 U19 U14 U9 U5 U3 T11 T2 T1				
		GND GND GND GND GND GND GND GND GND GND					W20 W4 W3 V22 V17 V2 V1 U19 U14 U9 U5 U3 T11 T2 T1				
		GND GND GND GND GND GND GND GND GND GND					W4 W3 V22 V17 V2 V1 U19 U14 U9 U5 U3 T11 T2 T1				
		GND GND GND GND GND GND GND GND GND GND					W3 V22 V17 V2 V1 U19 U14 U9 U5 U3 T11 T2 T1				
		GND GND GND GND GND GND GND GND GND GND					V22 V17 V2 V1 U19 U14 U9 U5 U3 T11 T2				
		GND GND GND GND GND GND GND GND GND GND					V17 V2 V1 U19 U14 U9 U5 U3 T11 T2				
		GND GND GND GND GND GND GND GND GND GND					V2 V1 U19 U14 U9 U5 U3 T11 T2				
		GND GND GND GND GND GND GND GND GND GND					V1 U19 U14 U9 U5 U3 T11 T2				
		GND GND GND GND GND GND GND GND GND GND					U19 U14 U9 U5 U3 T11 T2				
		GND GND GND GND GND GND GND GND GND GND					U14 U9 U5 U3 T11 T2				
		GND GND GND GND GND GND GND GND GND GND					U9 U5 U3 T11 T2 T1				
		GND GND GND GND GND GND GND GND GND GND					U5 U3 T11 T2 T1				
		GND GND GND GND GND GND GND GND GND GND					U3 T11 T2 T1				
		GND GND GND GND GND GND GND GND GND GND					T11 T2 T1				
		GND GND GND GND GND GND GND GND GND GND					T2 T1				
		GND GND GND GND GND GND GND GND GND GND					T1				
		GND GND GND GND GND GND GND GND GND GND									
		GND GND GND GND GND GND GND GND					R13				
		GND GND GND GND GND									
		GND GND GND GND				1	R3				
		GND GND GND					P10				
		GND GND GND					P4				
		GND GND					P2				
		GND					P1				
						İ	N22		İ		
		GND					N15		1		
		GND					N13		1		
		GND					N11				
	1	GND					N7				
		GND					N/C		+		
		GND					N5				
		GND					N3				
		GND					M19				
		GND					M14				
		GND					M12				
		GND					M9				
		GND					M4				
		GND					M2				
		GND					M1				
		GND					L16				
		GND					L13				
		GND					L11				
		GND					L5				
		GND					L3				
—— 		GND					K14				†
		GND					K12				
+		GND				1	K12 K10		t		
+			 		1	+	K10 K8	1	 		
$\longrightarrow \vdash$		GND GND			 		K8 K4		 		
\longrightarrow					ļ	 	N4	 	 		
		GND				1	K2	ļ	-		
\longrightarrow		GND			ļ	 	K1		-		↓
		GND				ļ	J20				
		GND					J15		ļ		ļ
		GND					J13				<u> </u>
		GND				1	J11				
		GND				1	J5				
		GND					J3				
	j	GND					H14				
	j	GND					H4				
+	t	GND			1	†	H3	l	†		1
+		GND	<u> </u>			†	H2		t		
+		GND	<u> </u>			†	H1		t		
+		GND				1	G9		 		
+		OND				-			-		
\longrightarrow		GND				-	G3	-	 		
\longrightarrow		GND			ļ	 	F16		-		
		GND					F11		Ļ		ļ
		GND					F6		ļ		1
		GND					F2				1
		GND				1	F1				
		GND					E13				
		GND					E4				
		GND					E3				
		GND					D20				





											Note (1)
Bank Number		Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					D10				
		GND					D5				
		GND					D2				
		GND					D1				
		GND					C22				
		GND					C17				
		GND					C7				4
		GND					C4				
		GND					C3				
		GND					B14				
		GND					B2 B1		-		
		GND GND					A21		-		+
							A21 A11				
		GND GND					A11				+
		VCC					J14				+
		VCC					P15				+
		VCC					P13		-		+
		VCC					P11				+
		VCC	 	t		1	N14		†	t	+
 		VCC	<u> </u>	†			N12		 	 	
		VCC		1			M15	1	1	t	1
		VCC		1			M13	1	1	t	1
		VCC		1			M11	İ	İ	İ	1
		VCC					L14				T .
		VCC					L12				1
		VCC					L10				1
		VCC					K13				
		VCC					K11				
		VCC					K9				
		VCC					J12				
		VCC					J10				
		VCC					H15				
		VCC					H13				
		VCC					H11				
		DNU					B3				4
		DNU					B4				
		DNU					D21				
		DNU					E10		-		
		VCCPGM					Y6				
		VCCPGM					U20		-		
		VCCPGM					B7 A3				
		VCCBAT VCCIO3A					T6				
		VCCIO3A VCCIO3A					AA6				+
		VCCIOSA VCCIOSB					V7		-		+
		VCCIO3B					AB9				+
		VCCIO3B					W10				+
		VCCIO3B					R8			1	
		VCCIO4A		1			T16	İ	İ	İ	1
		VCCIO4A		1			AB14	İ	İ	İ	1
		VCCIO4A					AA21				1
		VCCIO4A					Y18				1
		VCCIO4A					W15				
		VCCIO4A					V12				
		VCCIO5A					T21				
		VCCIO5A					R18				
		VCCIO5B					H22				
		VCCIO5B					P20				
		VCCIO5B					N17				
	, The state of the	VCCIO5B					L21				1
		VCCIO5B		ļ			K18		ļ	ļ	ļ
		VCCIO5B					G19				1
		VCCIO7A		ļ			B19		ļ	ļ	ļ
		VCCIO7A					H17				
		VCCIO7A					E18				
		VCCIO7A					D15				
		VCCIO7A					C12				
		VCCIO7A					A16				
		VCCIO8A VCCIO8A	<u> </u>	 		-	E8 H7	 	 	 	+
			1	18	1	1		i .	i	1	1

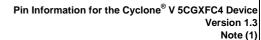


Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		VCCIO8A					B9			DDI(G/DDI(E (E)	LIDDICE
		VCCIOSA VCCIOSA			_		A6				+
	1	VCCPD3A			-		V6				+
											+
		VCCPD3B4A					V16				
		VCCPD3B4A					W9				
		VCCPD3B4A					V14				
		VCCPD3B4A					V10				
		VCCPD5A					P17				
		VCCPD5B					N19				
		VCCPD5B					M18				
		VCCPD7A8A					F13				1
		VCCPD7A8A					F9				1
		VCCPD7A8A					E15				+
		VCCPD7A8A			_		E9				+
24	VREFB3AN0			1	+				+		+
3A		VREFB3AN0					W6				
3B	VREFB3BN0	VREFB3BN0		ļ		ļ	AB12				
4A	VREFB4AN0	VREFB4AN0					AA14		1		
5A	VREFB5AN0	VREFB5AN0			ļ		V21				1
5B	VREFB5BN0	VREFB5BN0					K20				
7A	VREFB7AN0	VREFB7AN0					D16				
BA	VREFB8AN0	VREFB8AN0					B10				1
		NC					AB3				†
		NC					V11				+
		NC			_		P22				+
											+
		NC					P21				
		NC					P18				
		NC					P16				
		NC					N21				
		NC					N20				
		NC					N18				1
		NC					N16				
		NC					M22				†
		NC					M21				+
		NC					M20				+
	1	NC NC		1	+		L22		+		+
											+
		NC					K22				
		NC					J22				
		NC					F22				
		NC					E22				
		VCCH_GXBL					T3				
		VCCH_GXBL				<u> </u>	M3				
		VCCL_GXBL					P3				
		VCCL_GXBL					K3				1
	1	RREF_TL		1	1		A1		1	İ	1
	†	VCCA FPLL		<u> </u>	<u> </u>		T4				+
	1	VCCA_FPLL VCCA_FPLL		 	1	+	F4	1	+	+	+
	 			+	 				-		+
	ļ	VCCA_FPLL	1	ļ	ļ	<u> </u>	U18				4
		VCCA_FPLL					E19		1		
		VCC_AUX			ļ		D6				1
	<u> </u>	VCC_AUX					D12				<u> </u>
		VCC_AUX					D19				
		VCC AUX					W19				
		VCC_AUX		1			AA12			1	1
	1	VCC_AUX		1	1		AB5		1	İ	1
	1	VCCE_GXBL	+	 	1	+	L4	1	+	1	+
	 			+	 				-		+
	 	VCCE_GXBL		1	 		N4		 	+	+
		VCCE_GXBL		ļ		ļ	K5				
	1	VCCE_GXBL			1		J4				

Notes:

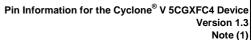
(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.

(2) RESET pin is only applicable for DDR3 device.





											Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
SXB_L1		REFCLK1Ln					P6			1,1	
XB_L1		REFCLK1Lp					N7				
XB_L1		GXB_TX_L5n					K1				
XB_L1		GXB_TX_L5p					K2				
XB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					M2				
SXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					M1				
XB_L1		GXB_TX_L4n					P1				
XB_L1		GXB_TX_L4p					P2				
SXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					T2				
SXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					T1				
SXB_L1		GXB_TX_L3n					W3				
XB_L1		GXB_TX_L3p					W4				
iXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					V2				
XB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					V1				
XB_L0		GXB_TX_L2n					AA3				
XB_L0		GXB_TX_L2p					AA4				
XB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					Y2				
XB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					Y1				
SXB_L0		GXB_TX_L1n					AC3				
XB_L0		GXB_TX_L1p			ļ		AC4		1	1	
XB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AB2				
XB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AB1				1
XB_L0		GXB_TX_L0n					AE3				
XB_L0		GXB_TX_L0p					AE4				
XB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AD2				
XB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AD1				
XB_L0		REFCLK0Lp					V6				
XB_L0		REFCLK0Ln					W6				
4		TDO		TDO			V7				
4		nCSO		DATA4			Y6				
A		TMS		TMS			R6				
A		AS_DATA3		DATA3			U6				
A		TCK		TCK			Y5				
A		AS_DATA2		DATA2			AB5				
A		TDI		TDI			T6				
A		AS_DATA1		DATA1			AD5				
A		DCLK		DCLK			N8				
A		AS_DATA0,ASDO		DATA0			AF5				
A	VREFB3AN0	10		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	T7	DQ1B			
A	VREFB3AN0	10		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7				
A	VREFB3AN0	10		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	T8	DQ1B			
A	VREFB3AN0	10		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	V8	DQ1B			
A	VREFB3AN0	10		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	W8	DQSn1B			
A	VREFB3AN0	10		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB6	DQ1B			
A	VREFB3AN0	10		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	Y9	DQS1B			
4	VREFB3AN0	10		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AA6				
A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R10	DQ1B			
A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AA7	DQ1B			
A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	R9	DQ1B			
A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	Y8	DQ1B			
A	VREFB3AN0	Ю		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	R8				
A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AD6	DQ1B			
4	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	P8				
A	VREFB3AN0	Ю			DIFFIO_TX_B8p	DIFFOUT_B8p	AD7	DQ1B			
3	VREFB3BN0	10			DIFFIO_TX_B9n	DIFFOUT_B9n	U9			GND	GND
3	VREFB3BN0	Ю			DIFFIO_RX_B10n	DIFFOUT_B10n	Y11	DQ2B		B_A_15	
3	VREFB3BN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	T9	DQ2B		B_WE#	
3	VREFB3BN0	Ю			DIFFIO_RX_B10p	DIFFOUT_B10p	W11	DQ2B		B_A_14	
3	VREFB3BN0	Ю			DIFFIO_RX_B11n	DIFFOUT_B11n	T11	DQSn2B		B_CS#_1	B_CS#_1
3	VREFB3BN0	10			DIFFIO_TX_B12n	DIFFOUT_B12n	AC10	DQ2B		B_A_13	
В	VREFB3BN0	10			DIFFIO_RX_B11p	DIFFOUT_B11p	R11	DQS2B		B_CS#_0	B_CS#_0
В	VREFB3BN0	10			DIFFIO_TX_B12p	DIFFOUT_B12p	AB10			B_A_12	1
В	VREFB3BN0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	AC8	DQ2B		B_A_11	
В	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT B14n	AB11	DQ2B	1	B_A_9	B_CA_9
В	VREFB3BN0	IO			DIFFIO TX B13p	DIFFOUT_B13p	AC9	DQ2B		B A 10	1
В	VREFB3BN0	10	1		DIFFIO_RX_B14p	DIFFOUT_B14p	AB12	DQ2B	İ	B_A_8	B_CA_8
В	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO RX B15n	DIFFOUT B15n	T12	1	1	1	1
В	VREFB3BN0	10			DIFFIO_TX_B16n	DIFFOUT_B16n	Y10	DQ2B		B_RAS#	
	VREFB3BN0	10	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	T13		1		
В								•			





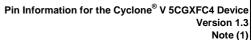
											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
3B	VREFB3BN0	10			DIFFIO_TX_B17n	DIFFOUT_B17n	V9			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AE8	DQ3B		B_BA_2	
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	V10	DQ3B		B_BA_0	
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	AD8	DQ3B		B_BA_1	
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	P10	DQSn3B		B_CK#	B_CK#
3B	VREFB3BN0	Ю			DIFFIO_TX_B20n	DIFFOUT_B20n	AF9	DQ3B		B_A_7	B_CA_7
3B	VREFB3BN0	10			DIFFIO_RX_B19p	DIFFOUT_B19p	N10	DQS3B		B_CK	B_CK
3B	VREFB3BN0	10			DIFFIO_TX_B20p	DIFFOUT_B20p	AE9			B_A_6	B_CA_6
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AF8	DQ3B		B_A_3	B_CA_3
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	U11	DQ3B		B_A_5	B_CA_5
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AF7	DQ3B		B_A_2	B_CA_2
3B	VREFB3BN0	10			DIFFIO_RX_B22p	DIFFOUT_B22p	U10	DQ3B		B_A_4	B_CA_4
3B	VREFB3BN0	10	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	P12			5 4 4	5.01.4
3B	VREFB3BN0	10	0.174		DIFFIO_TX_B24n	DIFFOUT_B24n	AF6	DQ3B		B_A_1	B_CA_1
3B	VREFB3BN0	10	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	P11	D00D		D 4 0	D 04 0
	VREFB3BN0	IO IO	D70 0		DIFFIO_TX_B24p	DIFFOUT_B24p	AE6	DQ3B		B_A_0	B_CA_0
4A	VREFB4AN0	IO IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AE11	DO4D		B DQ 0	B DO 0
	VREFB4AN0 VREFB4AN0	10			DIFFIO_RX_B26n DIFFIO_TX_B25p	DIFFOUT_B26n	AA14 AD11	DQ4B	+		B_DQ_0
						DIFFOUT_B25p		DQ4B		B_DQ_2	B_DQ_2
4A 4A	VREFB4AN0 VREFB4AN0	10	 		DIFFIO_RX_B26p DIFFIO_RX_B27n	DIFFOUT_B26p DIFFOUT_B27n	Y14 W13	DQ4B DQSn4B	+	B_DQ_1 B_DQS#_0	B_DQ_1 B DQS# 0
	VREFB4AN0	IO IO			DIFFIO_RX_B2/fi	DIFFOUT_B2/n	AD12	DQSN4B DQ4B		B_DQ3#_0 B DQ 3	B_DQS#_0 B DQ 3
4A 4A	VREFB4AN0 VREFB4AN0	IO IO			DIFFIO_IX_B28n DIFFIO_RX_B27p	DIFFOUT_B28n DIFFOUT_B27p	V13	DQ4B DQS4B	+	B DQS 0	B DQS 0
4A 4A	VREFB4AN0	IO IO			DIFFIO_RX_B27p	DIFFOUT B28p	AD13	DQ34B		B ODT 0	B ODT 0
4A 4A	VREFB4AN0	IO IO			DIFFIO_TX_B29n	DIFFOUT B29n	AE10	DQ4B	+	B ODT 1	B ODT 1
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT B30n	Y13	DQ4B	+	B DQ 4	B DQ 4
4A	VREFB4AN0	IO .			DIFFIO TX B29p	DIFFOUT B29p	AD10	DQ4B	+	B DQ 6	B DQ 6
4A	VREFB4AN0	IO .			DIFFIO RX B30p	DIFFOUT B30p	W12	DQ4B	+	B DQ 5	B DQ 5
4A	VREFB4AN0	IO .	CLK2n		DIFFIO RX B31n	DIFFOUT B31n	V112	DQ4D	+	D_DQ_0	<u>D_DQ_0</u>
4A	VREFB4AN0	IO .	OLIVEII		DIFFIO TX B32n	DIFFOUT B32n	AF12	DQ4B	-	B DQ 7	B_DQ_7
4A	VREFB4AN0	IO	CLK2p		DIFFIO RX B31p	DIFFOUT B31p	U12	54.5	-	5_5 4_,	5_5 4
4A	VREFB4AN0	IO .	OLIVED		DIFFIO TX B32p	DIFFOUT B32p	AF11	DQ4B	+	B DM 0	B DM 0
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT B33n	AC13	DQTD	-	GND	GND
4A	VREFB4AN0	IO.			DIFFIO RX B34n	DIFFOUT B34n	AC15	DQ5B	DQ1B	B DQ 8	B DQ 8
4A	VREFB4AN0	IO.			DIFFIO TX B33p	DIFFOUT B33p	AC14	DQ5B	DQ1B	B DQ 10	B DQ 10
4A	VREFB4AN0	IO			DIFFIO RX B34p	DIFFOUT_B34p	AB15	DQ5B	DQ1B	B_DQ_9	B_DQ_9
4A	VREFB4AN0	IO			DIFFIO RX B35n	DIFFOUT B35n	V14	DQSn5B	DQ1B	B DQS# 1	B_DQS#_1
4A	VREFB4AN0	10			DIFFIO TX B36n	DIFFOUT B36n	AF13	DQ5B	DQ1B	B DQ 11	B DQ 11
4A	VREFB4AN0	10			DIFFIO RX B35p	DIFFOUT_B35p	U14	DQS5B	DQ1B	B_DQS_1	B DQS 1
4A	VREFB4AN0	10			DIFFIO TX B36p	DIFFOUT B36p	AE13		1	B CKE 1	B CKE 1
4A	VREFB4AN0	10			DIFFIO TX B37n	DIFFOUT_B37n	AF14	DQ5B	DQ1B	B CKE 0	B_CKE_0
4A	VREFB4AN0	10			DIFFIO RX B38n	DIFFOUT B38n	AB16	DQ5B	DQ1B	B DQ 12	B DQ 12
4A	VREFB4AN0	10			DIFFIO_TX_B37p	DIFFOUT_B37p	AE14	DQ5B	DQ1B	B_DQ_14	B_DQ_14
4A	VREFB4AN0	10			DIFFIO RX B38p	DIFFOUT B38p	AA16	DQ5B	DQ1B	B DQ 13	B DQ 13
4A	VREFB4AN0	10	CLK3n		DIFFIO RX B39n	DIFFOUT B39n	Y16		1		
4A	VREFB4AN0	Ю			DIFFIO_TX_B40n	DIFFOUT_B40n	AF18	DQ5B	DQ1B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	Ю	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	Y15				
4A	VREFB4AN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AE18	DQ5B	DQ1B	B_DM_1	B_DM_1
4A	VREFB4AN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AD18			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AD16	DQ6B	DQ1B	B_DQ_16	B_DQ_16
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AC18	DQ6B	DQ1B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	Ю			DIFFIO_RX_B42p	DIFFOUT_B42p	AD17	DQ6B	DQ1B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	Ю			DIFFIO_RX_B43n	DIFFOUT_B43n	W15	DQSn6B	DQSn1B	B_DQS#_2	B_DQS#_2
4A	VREFB4AN0	Ю			DIFFIO_TX_B44n	DIFFOUT_B44n	AF19	DQ6B	DQ1B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	V15	DQS6B	DQS1B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	Ю			DIFFIO_TX_B44p	DIFFOUT_B44p	AE19			B_RESET#	B_RESET#
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AF22	DQ6B	DQ1B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AC17	DQ6B	DQ1B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AF21	DQ6B	DQ1B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AB17	DQ6B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	U17	1		GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AE21	DQ6B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	T17	1		GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AE20	DQ6B	DQ1B	B_DM_2	B_DM_2
4A	VREFB4AN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AD20	1		GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AE15	DQ7B	DQ2B	B_DQ_24	B_DQ_24
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AC20	DQ7B	DQ2B	B_DQ_26	B_DQ_26
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AE16	DQ7B	DQ2B	B_DQ_25	B_DQ_25
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	W17	DQSn7B	DQ2B	B_DQS#_3	B_DQS#_3
4A	VREFB4AN0	10		1	DIFFIO_TX_B52n	DIFFOUT_B52n	AD21	DQ7B	DQ2B	B_DQ_27	B_DQ_27



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
4A	VREFB4AN0	Ю			DIFFIO_RX_B51p	DIFFOUT_B51p	W16	DQS7B	DQ2B	B_DQS_3	B_DQS_3
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AD22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AE23	DQ7B	DQ2B	GND	GND
4A		IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AF16	DQ7B	DQ2B	B_DQ_28	B_DQ_28
4A		Ю			DIFFIO_TX_B53p	DIFFOUT_B53p	AD23	DQ7B	DQ2B	B_DQ_30	B_DQ_30
4A		Ю			DIFFIO_RX_B54p	DIFFOUT_B54p	AF17	DQ7B	DQ2B	B_DQ_29	B_DQ_29
4A		10			DIFFIO_RX_B55n	DIFFOUT_B55n	U16			GND	GND
4A		10			DIFFIO_TX_B56n	DIFFOUT_B56n	AF23	DQ7B	DQ2B	B_DQ_31	B_DQ_31
4A		IO			DIFFIO_RX_B55p	DIFFOUT_B55p	U15			GND	GND
4A		IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AE24	DQ7B	DQ2B	B_DM_3	B_DM_3
4A		10			DIFFIO_TX_B57n	DIFFOUT_B57n	AF24			GND	GND
4A		IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AA18	DQ8B	DQ2B	B_DQ_32	B_DQ_32
4A		IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AE25	DQ8B	DQ2B	B_DQ_34	B_DQ_34
4A	VREFB4AN0				DIFFIO_RX_B58p	DIFFOUT_B58p	Y18	DQ8B	DQ2B	B_DQ_33	B_DQ_33
4A		10			DIFFIO_RX_B59n	DIFFOUT_B59n	V17	DQSn8B	DQSn2B	B_DQS#_4	B_DQS#_4
4A	VREFB4AN0				DIFFIO_TX_B60n	DIFFOUT_B60n	AE26	DQ8B	DQ2B	B_DQ_35	B_DQ_35
4A		IO IO			DIFFIO_RX_B59p	DIFFOUT_B59p	V18	DQS8B	DQS2B	B_DQS_4	B_DQS_4
4A 4A		10			DIFFIO_TX_B60p	DIFFOUT_B60p	AD26	DOOD	DOOD	GND GND	GND
4A 4A		10			DIFFIO_TX_B61n DIFFIO_RX_B62n	DIFFOUT_B61n DIFFOUT_B62n	AC19 Y19	DQ8B DQ8B	DQ2B DQ2B		GND B DQ 36
4A 4A		10			DIFFIO_RX_B62fi	DIFFOUT_B62h	AB19	DQ8B	DQ2B DQ2B	B_DQ_36 B DQ 38	B_DQ_36 B DQ 38
4A 4A		IO			DIFFIO_TX_B6Tp	DIFFOUT B62p	Y20	DQ8B	DQ2B DQ2B	B_DQ_36 B DQ 37	B_DQ_36 B DQ 37
4A 4A		10			DIFFIO_RX_B62p	DIFFOUT B63n	W18	DQ8B	DQ2B	GND	GND
4A 4A		10			DIFFIO_RX_B63II	DIFFOUT B64n	AA21	DQ8B	DQ2B	B DQ 39	B DQ 39
4A 4A		10			DIFFIO_TX_B64II	DIFFOUT_B63p	V19	DQ0B	DQZB	GND	GND
4A		10			DIFFIO_TX_B64p	DIFFOUT B64p	AB22	DQ8B	DQ2B	B DM 4	B DM 4
5A		10	RZQ 1		DIFFIO_TX_B64p	DIFFOUT R1p	AC22	DQ6B DQ1R	DQ2B	B_DIVI_4	B_DIVI_4
5A		10	1221	INIT_DONE	DIFFIO RX R2p	DIFFOUT R2p	U19	DQTK			+
5A		10		PR REQUEST	DIFFIO TX R1n	DIFFOUT_R1n	AC23	DQ1R			-
5A		10		CRC ERROR	DIFFIO RX R2n	DIFFOUT R2n	V20	DQTK			†
5A		10		nCEO	DIFFIO TX R3p	DIFFOUT R3p	AA22	DQ1R			+
5A		IO IO		IIOEO	DIFFIO RX R4p	DIFFOUT R4p	W20	DQ1R			+
5A		10		CvP_CONFDONE	DIFFIO TX R3n	DIFFOUT_R3n	AA23	DQ1R			+
5A		IO			DIFFIO RX R4n	DIFFOUT R4n	W21	DQ1R			+
5A	VREFB5AN0	IO		DEV OE	DIFFIO TX R5p	DIFFOUT R5p	AC24				1
5A		10		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	V22	DQS1R			1
5A	VREFB5AN0	10		DEV_CLRn	DIFFIO TX R5n	DIFFOUT_R5n	AB24	DQ1R			1
5A		10		nPERSTL1	DIFFIO RX R6n	DIFFOUT_R6n	U22	DQSn1R			1
5A		10			DIFFIO_TX_R7p	DIFFOUT_R7p	Y23	DQ1R			1
5A	VREFB5AN0	10			DIFFIO RX R8p	DIFFOUT R8p	T19	DQ1R			
5A	VREFB5AN0	Ю			DIFFIO_TX_R7n	DIFFOUT_R7n	Y24				
5A	VREFB5AN0	Ю			DIFFIO_RX_R8n	DIFFOUT_R8n	U20	DQ1R			
5B	VREFB5BN0	IO	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R9p	DIFFOUT_R9p	T21				
5B	VREFB5BN0	IO			DIFFIO_TX_R10p	DIFFOUT_R10p	V23	DQ2R			
5B	VREFB5BN0	IO	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R9n	DIFFOUT_R9n	T22				
5B	VREFB5BN0	IO			DIFFIO_TX_R10n	DIFFOUT_R10n	V24	DQ2R			
5B		IO			DIFFIO_RX_R11p	DIFFOUT_R11p	T23	DQ2R			
5B		IO			DIFFIO_TX_R12p	DIFFOUT_R12p	AA24	DQ2R			1
5B		IO			DIFFIO_RX_R11n	DIFFOUT_R11n	T24	DQ2R			1
5B		IO			DIFFIO_TX_R12n	DIFFOUT_R12n	AB25	DQ2R			ļ
5B		IO			DIFFIO_RX_R13p	DIFFOUT_R13p	R23	DQS2R			
5B	VREFB5BN0	IO		-	DIFFIO_TX_R14p	DIFFOUT_R14p	AD25	L	-		_
5B		IO			DIFFIO_RX_R13n	DIFFOUT_R13n	P23	DQSn2R			
5B		IO			DIFFIO_TX_R14n	DIFFOUT_R14n	AC25	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	R24	DQ2R	-		4
5B	VREFB5BN0	IO .		-	DIFFIO_TX_R16p	DIFFOUT_R16p	U24	DQ2R	-		_
5B	VREFB5BN0	IO		-	DIFFIO_RX_R15n	DIFFOUT_R15n	R25	DQ2R	-	+	+
5B		10	louve.		DIFFIO_TX_R16n	DIFFOUT_R16n	V25	1	-		+
5B		10	CLK6p	-	DIFFIO_RX_R17p	DIFFOUT_R17p	R20	BOOD	-	+	+
5B		IO IO	OLIVO-	+	DIFFIO_TX_R18p	DIFFOUT_R18p	AB26	DQ3R	+	+	+
5B		IO IO	CLK6n	+	DIFFIO_RX_R17n	DIFFOUT_R17n	P20	DOOD	+	+	+
5B		IO .			DIFFIO_TX_R18n	DIFFOUT_R18n	AA26	DQ3R	+		
5B		10	EDIT DD OLKOUTS EDIT DD OLKOUT EDIT DE TE		DIFFIO_RX_R19p	DIFFOUT_R19p	T26	DQ3R	+		
5B		10	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB	+	DIFFIO_TX_R20p DIFFIO_RX_R19n	DIFFOUT_R20p DIFFOUT_R19n	Y25	DQ3R DQ3R	+	+	+
5B 5B		IO IO	EDIT BD CLKOUTT EDIT BD CLKOUT-	+	DIFFIO_RX_R19n DIFFIO_TX_R20n	DIFFOUT_R19n DIFFOUT_R20n	R26	DQ3R DQ3R	-		+
		10	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn	+		DIFFOUT_R20n DIFFOUT_R21p	Y26		-		+
5B				+	DIFFIO_RX_R21p		P21	DQS3R	-		+
5B 5B		10	 	+	DIFFIO_TX_R22p DIFFIO_RX_R21n	DIFFOUT_R22p DIFFOUT_R21n	W25 P22	DQSn3R	+		+
		•		+					+	+	
5B	VREFB5BN0	10		1	DIFFIO_TX_R22n	DIFFOUT_R22n	W26	DQ3R	1	1	1



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
5B	VREFB5BN0	IO			DIFFIO RX R23p	DIFFOUT R23p	N25	DQ3R	†	DDI(S/DDI(Z (Z)	LI DDIKE
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	U25	DQ3R	1	1	1
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	P26	DQ3R	1		
	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	U26		T		
	VREFB6AN0	IO	CLK5p		DIFFIO_RX_R25p	DIFFOUT_R25p	N20				
6A	VREFB6AN0	IO			DIFFIO_TX_R26p	DIFFOUT_R26p	J25	DQ4R		ļ	
6A	VREFB6AN0	10	CLK5n		DIFFIO_RX_R25n	DIFFOUT_R25n	M21			ļ	
6A	VREFB6AN0	IO			DIFFIO_TX_R26n	DIFFOUT_R26n	J26	DQ4R	<u> </u>		
6A	VREFB6AN0	10			DIFFIO_RX_R27p	DIFFOUT_R27p	N24	DQ4R			
6A	VREFB6AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB		DIFFIO_TX_R28p	DIFFOUT_R28p	F26	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	M24	DQ4R	 	 	
6A 6A	VREFB6AN0 VREFB6AN0	IO IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_R28n DIFFIO_RX_R29p	DIFFOUT_R28n DIFFOUT_R29p	G26 N23	DQ4R DQS4R	+	 	
6A	VREFB6AN0	IO IO			DIFFIO_RX_R29p DIFFIO_TX_R30p	DIFFOUT_R30p	G25	DQ54R	+	+	
6A	VREFB6AN0	10			DIFFIO_IX_R30p DIFFIO_RX_R29n	DIFFOUT_R30p DIFFOUT_R29n	M22	DQSn4R	+	+	-
6A	VREFB6AN0	10			DIFFIO_RX_R29II	DIFFOUT_R30n	H25	DQ314R DQ4R	+	+	-
6A	VREFB6AN0	10			DIFFIO_TX_R30II	DIFFOUT_R30II	M25	DQ4R DQ4R	+	+	+
6A	VREFB6AN0	10			DIFFIO_TX_R32p	DIFFOUT_R32p	D26	DQ4R	+	+	1
6A	VREFB6AN0	IO IO			DIFFIO RX R31n	DIFFOUT R31n	M26	DQ4R	+	+	1
6A	VREFB6AN0	10		1	DIFFIO_TX_R32n	DIFFOUT_R32n	E26		1	1	1
6A	VREFB6AN0	10	CLK4p,FPLL_TR_FBp	1	DIFFIO RX R33p	DIFFOUT R33p	K25		1	1	
	VREFB6AN0	10		1	DIFFIO_TX_R34p	DIFFOUT R34p	E24	DQ5R	1	1	
	VREFB6AN0	10	CLK4n,FPLL TR FBn	İ	DIFFIO RX R33n	DIFFOUT R33n	K26	1	1	1	
	VREFB6AN0	10	·	İ	DIFFIO TX R34n	DIFFOUT R34n	E25	DQ5R	1	1	
	VREFB6AN0	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	K24	DQ5R		1	
6A	VREFB6AN0	10			DIFFIO_TX_R36p	DIFFOUT_R36p	F24	DQ5R	1		
6A	VREFB6AN0	Ю			DIFFIO_RX_R35n	DIFFOUT_R35n	K23	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R36n	DIFFOUT_R36n	G24	DQ5R	T		
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R37p	L23	DQS5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R38p	H23				
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R37n	L24	DQSn5R			
6A	VREFB6AN0	Ю			DIFFIO_TX_R38n	DIFFOUT_R38n	H24	DQ5R			
6A	VREFB6AN0	10			DIFFIO_RX_R39p	DIFFOUT_R39p	H22	DQ5R		ļ	
6A	VREFB6AN0	10			DIFFIO_TX_R40p	DIFFOUT_R40p	F23	DQ5R	<u> </u>	<u> </u>	
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	J23	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R40n	G22			 	
6A	VREFB6AN0	IO IO			DIFFIO_RX_R41p	DIFFOUT_R41p	L22	DOOD	 		-
6A	VREFB6AN0	IO IO			DIFFIO_TX_R42p	DIFFOUT_R42p	B25	DQ6R	 	 	
6A	VREFB6AN0 VREFB6AN0	IO IO			DIFFIO_RX_R41n DIFFIO_TX_R42n	DIFFOUT_R41n	K21 B26	DOCD	+	4	+
6A 6A	VREFB6AN0	IO IO			DIFFIO_TX_R42n	DIFFOUT_R42n DIFFOUT_R43p	H19	DQ6R DQ6R	+	+	1
6A	VREFB6AN0	10			DIFFIO_RX_R43p	DIFFOUT_R44p	D25	DQ6R	+	+	1
	VREFB6AN0	10			DIFFIO RX R43n	DIFFOUT R43n	H20	DQ6R	+	+	1
6A	VREFB6AN0	IO IO			DIFFIO_TX_R44n	DIFFOUT_R44n	C25	DQ6R	+	+	1
6A	VREFB6AN0	IO			DIFFIO RX R45p	DIFFOUT R45p	J20	DQS6R	+	1	
6A	VREFB6AN0	10		İ	DIFFIO TX R46p	DIFFOUT R46p	D22		†	1	
6A	VREFB6AN0	10		İ	DIFFIO RX R45n	DIFFOUT R45n	J21	DQSn6R	1	1	
6A	VREFB6AN0	10			DIFFIO_TX_R46n	DIFFOUT_R46n	E23	DQ6R	1	1	
6A	VREFB6AN0	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	G20	DQ6R	1	1	
6A	VREFB6AN0	IO		İ	DIFFIO_TX_R48p	DIFFOUT_R48p	E21	DQ6R		1	
6A	VREFB6AN0	IO	_		DIFFIO_RX_R47n	DIFFOUT_R47n	F21	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R48n	DIFFOUT_R48n	F22				
7A		GND					D23				
7A	VREFB7AN0	Ю			DIFFIO_RX_T1p	DIFFOUT_T1p	H15			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	C23	DQ1T	DQ1T	T_DM_4	T_DM_4
7A	VREFB7AN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	J16			GND	GND
7A	VREFB7AN0	IO		ļ	DIFFIO_TX_T2n	DIFFOUT_T2n	C22	DQ1T	DQ1T	T_DQ_39	T_DQ_39
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	B24	DQ1T	DQ1T	T_DQ_37	T_DQ_37
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	A23	DQ1T	DQ1T	T_DQ_38	T_DQ_38
7A	VREFB7AN0	10			DIFFIO_RX_T3n	DIFFOUT_T3n	A24	DQ1T	DQ1T	T_DQ_36	T_DQ_36
7A	VREFB7AN0	10		1	DIFFIO_TX_T4n	DIFFOUT_T4n	A22	DQ1T	DQ1T	GND T DOO 4	GND T DOO 4
7A	VREFB7AN0	IO .		1	DIFFIO_RX_T5p	DIFFOUT_T5p	H18	DQS1T	DQS1T	T_DQS_4	T_DQS_4
7A	VREFB7ANO	IO IO		 	DIFFIO_TX_T6p	DIFFOUT_T6p	B22	DOC-4T	DOC-4T	GND	GND
7A	VREFB7ANO	10		 	DIFFIO_RX_T5n	DIFFOUT_T5n	H17	DQSn1T	DQSn1T	T_DQS#_4	T_DQS#_4
7A	VREFB7ANO	IO IO		1	DIFFIO_TX_T6n	DIFFOUT_T6n	A21	DQ1T	DQ1T	T_DQ_35	T_DQ_35
7A	VREFB7ANO	IO IO		1	DIFFIO_RX_T7p	DIFFOUT_T7p	D21	DQ1T	DQ1T	T_DQ_33	T_DQ_33
7A 7A	VREFB7AN0 VREFB7AN0	10		-	DIFFIO_TX_T8p DIFFIO_RX_T7n	DIFFOUT_T8p DIFFOUT_T7n	B21 D20	DQ1T DQ1T	DQ1T DQ1T	T_DQ_34 T_DQ_32	T_DQ_34 T_DQ_32
7A 7A	VREFB7AN0 VREFB7AN0	IO IO		1	DIFFIO_RX_17n DIFFIO_TX_T8n	DIFFOUT_T8n	D20 B20	וואַעו	ואַעוו	GND	GND
7A 7A	VREFB7AN0 VREFB7AN0	IO IO		1	DIFFIO_IX_I8N DIFFIO_RX_T9p	DIFFOUT_18h	G16	}	+	GND	GND
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											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	10			DIFFIO TX T10p	DIFFOUT_T10p	C20	DQ2T	DQ1T	T DM 3	T DM 3
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	G17			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	B19	DQ2T	DQ1T	T_DQ_31	T_DQ_31
7A	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	E20	DQ2T	DQ1T	T_DQ_29	T_DQ_29
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	C19	DQ2T	DQ1T	T_DQ_30	T_DQ_30
7A	VREFB7AN0	10			DIFFIO_RX_T11n	DIFFOUT_T11n	E19	DQ2T	DQ1T	T_DQ_28	T_DQ_28
7A 7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_TX_T12n DIFFIO_RX_T13p	DIFFOUT_T12n DIFFOUT_T13p	C18	DQ2T DQS2T	DQ1T DQ1T	GND T_DQS_3	GND T_DQS_3
7A 7A	VREFB7AN0	IO IO			DIFFIO_RX_113p DIFFIO_TX_T14p	DIFFOUT_T14p	J12 A19	DQ521	DQTI	GND	GND
7A	VREFB7AN0	10			DIFFIO_RX_T13n	DIFFOUT_T13n	J11	DQSn2T	DQ1T	T_DQS#_3	T_DQS#_3
7A	VREFB7AN0	10			DIFFIO_TX_T14n	DIFFOUT_T14n	A18	DQ2T	DQ1T	T_DQ_27	T_DQ_27
7A	VREFB7AN0	10			DIFFIO RX T15p	DIFFOUT_T15p	D18	DQ2T	DQ1T	T DQ 25	T DQ 25
7A	VREFB7AN0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	A17	DQ2T	DQ1T	T_DQ_26	T_DQ_26
7A	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	D17	DQ2T	DQ1T	T_DQ_24	T_DQ_24
7A	VREFB7AN0	10			DIFFIO_TX_T16n	DIFFOUT_T16n	A16			GND	GND
	VREFB7AN0	10			DIFFIO_RX_T17p	DIFFOUT_T17p	H14			GND	GND
7A	VREFB7AN0	10			DIFFIO_TX_T18p	DIFFOUT_T18p	C17	DQ3T	DQ2T	T_DM_2	T_DM_2
	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T17n DIFFIO_TX_T18n	DIFFOUT_T17n DIFFOUT_T18n	H13 B17	DQ3T	DQ2T	GND T DQ 23	GND T DQ 23
	VREFB7AN0	10			DIFFIO_TX_T18h	DIFFOUT_T18h	E18	DQ3T	DQ2T	T_DQ_23	T_DQ_23
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	A14	DQ3T	DQ2T	T DQ 22	T DQ 22
7A	VREFB7AN0	IO			DIFFIO RX T19n	DIFFOUT_T19n	F18	DQ3T	DQ2T	T DQ 20	T DQ 20
7A	VREFB7AN0	IO			DIFFIO TX T20n	DIFFOUT T20n	B14	DQ3T	DQ2T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	L12	DQS3T	DQS2T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	B15			T_RESET#	T_RESET#
7A	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	K11	DQSn3T	DQSn2T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	C15	DQ3T	DQ2T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	C14	DQ3T	DQ2T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	10			DIFFIO_TX_T24p	DIFFOUT_T24p	A8	DQ3T	DQ2T DQ2T	T_DQ_18	T_DQ_18
7A 7A	VREFB7AN0 VREFB7AN0	IO IO			DIFFIO_RX_T23n DIFFIO_TX_T24n	DIFFOUT_T23n DIFFOUT_T24n	D15 A9	DQ3T	DQ21	T_DQ_16 GND	T_DQ_16 GND
7A 7A	VREFB7AN0	IO IO	CLK11p		DIFFIO_TX_T24n	DIFFOUT_T25p	G15	+	+	GND	GND
7A	VREFB7AN0	IO IO	CERTIF		DIFFIO_TX_T26p	DIFFOUT_T26p	C9	DQ4T	DQ2T	T DM 1	T DM 1
7A	VREFB7AN0	IO	CLK11n		DIFFIO RX T25n	DIFFOUT_T25n	G14	DQTI	DQZI	1_0//_1	1_DIW_1
7A	VREFB7AN0	10			DIFFIO_TX_T26n	DIFFOUT_T26n	B9	DQ4T	DQ2T	T DQ 15	T DQ 15
7A	VREFB7AN0	10			DIFFIO_RX_T27p	DIFFOUT_T27p	E16	DQ4T	DQ2T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	D10	DQ4T	DQ2T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	D16	DQ4T	DQ2T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	C10	DQ4T	DQ2T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	N12	DQS4T	DQ2T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	B10			T_CKE_1	T_CKE_1
7A	VREFB7ANO	10			DIFFIO_RX_T29n	DIFFOUT_T29n	M12 A11	DQSn4T	DQ2T	T_DQS#_1 T_DQ_11	T_DQS#_1 T_DQ_11
7A 7A	VREFB7AN0 VREFB7AN0	IO IO			DIFFIO_TX_T30n DIFFIO_RX_T31p	DIFFOUT_T30n DIFFOUT_T31p	F16	DQ4T DQ4T	DQ2T DQ2T	T DQ 9	T_DQ_11
7A	VREFB7AN0	IO IO			DIFFIO_RX_131p	DIFFOUT_T31p	E10	DQ4T	DQ2T DQ2T	T DQ 10	T DQ_9
7A	VREFB7AN0	10			DIFFIO RX T31n	DIFFOUT T31n	E15	DQ4T	DQ2T	T DQ 8	T DQ 8
7A	VREFB7AN0	10			DIFFIO TX T32n	DIFFOUT T32n	E11	54.1	DQL.	GND	GND
7A	VREFB7AN0	10	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H12				
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	B12	DQ5T		T_DM_0	T_DM_0
7A	VREFB7AN0	Ю	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G11				
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	A13	DQ5T		T_DQ_7	T_DQ_7
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	G12	DQ5T		T_DQ_5	T_DQ_5
7A	VREFB7AN0	10			DIFFIO_TX_T36p	DIFFOUT_T36p	A12	DQ5T	+	T_DQ_6	T_DQ_6
7A	VREFB7ANO	IO IO		1	DIFFIO_RX_T35n	DIFFOUT_T35n	F12	DQ5T	+	T_DQ_4	T_DQ_4
7A 7A	VREFB7AN0 VREFB7AN0	IO IO		 	DIFFIO_TX_T36n DIFFIO_RX_T37p	DIFFOUT_T36n DIFFOUT_T37p	B11 M11	DQ5T DQS5T	+	T_ODT_1 T DQS 0	T_ODT_1 T DQS 0
7A 7A	VREFB7AN0	IO IO		 	DIFFIO_RX_137p	DIFFOUT_T38p	C13	ונפטטו	+	T ODT 0	T ODT 0
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT T37n	L11	DQSn5T	1	T_DQS#_0	T DQS# 0
7A	VREFB7AN0	IO		İ	DIFFIO_TX_T38n	DIFFOUT_T38n	C12	DQ5T5T	1	T DQ 3	T DQ 3
7A	VREFB7AN0	10			DIFFIO_RX_T39p	DIFFOUT_T39p	E13	DQ5T		T_DQ_1	T_DQ_1
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	D11	DQ5T		T_DQ_2	T_DQ_2
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	D13	DQ5T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	D12	1			
8A	VREFB8AN0	IO	CLK9p	ļ	DIFFIO_RX_T41p	DIFFOUT_T41p	N9	 		<u> </u>	
8A	VREFB8AN0	10	Louve .	1	DIFFIO_TX_T42p	DIFFOUT_T42p	A5	DQ6T	+	T_A_0	T_CA_0
8A	VREFB8AN0 VREFB8AN0	10	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n DIFFOUT_T42n	M10	DOST	+	T A 1	T CA 1
8A 8A	VREFB8AN0 VREFB8AN0	10		 	DIFFIO_TX_T42n DIFFIO_RX_T43p	DIFFOUT_T42n DIFFOUT_T43p	B6 H8	DQ6T DQ6T	+	T_A_1 T A 4	T_CA_1
8A	VREFB8AN0 VREFB8AN0	10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB	 	DIFFIO_RX_143p DIFFIO_TX_T44p	DIFFOUT_143p DIFFOUT_T44p	H8 A7	DQ6T	+	T A 2	T_CA_4 T_CA_2
8A	VREFB8AN0	10		 	DIFFIO_TX_T44p	DIFFOUT_T44p	H9	DQ6T	+	T_A_5	T_CA_5
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											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
8A	VREFB8AN0	10	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO TX T44n	DIFFOUT T44n	B7	DQ6T		T_A_3	T_CA_3
8A	VREFB8AN0	10			DIFFIO RX T45p	DIFFOUT T45p	M9	DQS6T		T CK	T_CK
8A	VREFB8AN0	10			DIFFIO_TX_T46p	DIFFOUT_T46p	D6			T_A_6	T_CA_6
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT T45n	L9	DQSn6T		T_CK#	T_CK#
8A	VREFB8AN0	10			DIFFIO_TX_T46n	DIFFOUT_T46n	E6	DQ6T		T_A_7	T_CA_7
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	H10	DQ6T		T_BA_1	
8A	VREFB8AN0	10			DIFFIO_TX_T48p	DIFFOUT_T48p	D7	DQ6T		T_BA_0	T
8A	VREFB8AN0	10			DIFFIO_RX_T47n	DIFFOUT_T47n	G10	DQ6T		T_BA_2	
8A	VREFB8AN0	10			DIFFIO_TX_T48n	DIFFOUT_T48n	C7			GND	GND
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	L8				
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	F6	DQ7T		T_CAS#	
8A	VREFB8AN0	10	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	K9				
8A	VREFB8AN0				DIFFIO_TX_T50n	DIFFOUT_T50n	G6	DQ7T		T_RAS#	
8A	VREFB8AN0				DIFFIO_RX_T51p	DIFFOUT_T51p	K8	DQ7T		T_A_8	T_CA_8
8A	VREFB8AN0				DIFFIO_TX_T52p	DIFFOUT_T52p	G7	DQ7T		T_A_10	
8A	VREFB8AN0				DIFFIO_RX_T51n	DIFFOUT_T51n	J8	DQ7T		T_A_9	T_CA_9
8A	VREFB8AN0				DIFFIO_TX_T52n	DIFFOUT_T52n	F7	DQ7T		T_A_11	
8A	VREFB8AN0				DIFFIO_RX_T53p	DIFFOUT_T53p	K10	DQS7T		T_CS#_0	T_CS#_0
8A	VREFB8AN0				DIFFIO_TX_T54p	DIFFOUT_T54p	H7	D00 TT	+	T_A_12	T 00" 4
8A	VREFB8AN0	10			DIFFIO_RX_T53n	DIFFOUT_T53n	J10	DQSn7T	+	T_CS#_1	T_CS#_1
8A	VREFB8AN0	10			DIFFIO_TX_T54n	DIFFOUT_T54n	J7	DQ7T	+	T_A_13	+
8A	VREFB8AN0	10			DIFFIO_RX_T55p	DIFFOUT_T55p	L7	DQ7T	+	T_A_14 T WE#	+
8A	VREFB8AN0	10			DIFFIO_TX_T56p	DIFFOUT_T56p	D8	DQ7T			
8A 8A	VREFB8AN0 VREFB8AN0	IO IO			DIFFIO_RX_T55n DIFFIO_TX_T56n	DIFFOUT_T55n DIFFOUT_T56n	K6 E9	DQ7T	+	T_A_15 GND	GND
	VREFB8ANU			MOELO	DIFFIO_IX_156n	DIFFOUT_1560		-	+	GND	GND
9A		MSEL0 CONF_DONE		MSEL0 CONF DONE			M7 A6	-	+	+	
9A		MSEL1		MSEL1			L6				+
9A 9A		InSTATUS		nSTATUS			B5				+
9A 9A		nCE		nCE		+	D5	+	+	+	+
9A		MSEL2		MSEL2		+	A2	+	+	+	+
9A		MSFL3		MSEL3		+	K5	+	+	+	+
9A		nCONFIG		nCONFIG			F5	+	+	+	+
9A		MSEL4		MSEL4			JS	+	+	+	+
9Α		GND		IVIOEL4			H5		-		+
9A		GND					V26	+	+	+	+
		GND					A25	+	+	+	+
		GND		†			D24				+
		GND		†			H26				+
		GND					L25				+
		GND					P24				+
		GND					AA25				+
		GND					AC26				+
		GND					AF25				+
		GND					G23				+
	İ	GND			1		K22	İ	İ	İ	1
	İ	GND			1		U23	İ	İ	İ	1
		GND					Y22				1
		GND				İ	AD24	1			1
	İ	GND					C21		İ	1	1
		GND					F20				
		GND					L20				
		GND					K19				
		GND					N21				
		GND					M19				
		GND					T20				
		GND					P19				
		GND					W19				
		GND					AC21				
		GND					AF20				
·		GND					B18	1	1	1	_
		GND					E17				
·		GND					L18	1	1	1	_
·		GND					K17	1	1	1	
		GND			ļ		J18	1			
		GND			ļ		N18	1	1	1	
		GND					M17	1	1	1	
		GND			ļ	ļ	R18	1			<u> </u>
		GND					P17	_			
	l	GND				1	AB18	1		1	



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					AE17				T
		GND					A15				Ī
		GND					D14				
		GND					H16				
		GND					L16				
		GND					L14				
		GND					K15				
		GND					J14				
		GND					N16				
		GND					N14				
		GND					M15				
		GND					T15				
		GND					R16				
		GND					R14				
		GND					P15				
		GND					V16				
		GND					AA15				
		GND					AD14				
		GND		1	ļ		G13	_	1	1	4
	-	GND					K13	_	1	ļ	4
	-	GND					K12	_	1	ļ	4
	1	GND		1	1		M13	+	1	1	+
	1	GND		1	1		R12	+	1	1	+
	-	GND GND					P13 U13	+	+	+	+
								+			+
		GND					Y12	+			+
		GND					C11				+
		GND GND					F10 L10				+
	1	GND		+			J9	+			+
	1	GND		+			N11	+			+
		GND					T10				+
	1	GND		+			P9	+			+
		GND					W9	+			+
		GND					AC11	+			+
		GND					AF10	+			+
		GND					B8	+			+
		GND					E7				-
		GND					H6				-
		GND					N6				1
		GND					M8				†
		GND					R7				1
		GND					P7				+
		GND					AB8				1
		GND					AE7				+
		GND					C5				1
		GND					B4				+
		GND					F4				1
		GND					E5			1	1
		GND					D4				1
		GND					H4			1	1
		GND					G5			1	1
		GND					L4				
		GND					J4			1	1
		GND					N4			1	1
		GND					M5				
		GND					T5				
		GND					R4				
		GND					P5				
		GND					V5				
		GND					V4				
		GND					U4				
		GND					AA5				
		GND					Y4				
		GND					W5				
		GND					AC5				
		GND					AB4				
		GND					AF4				
		GND					AE5				
		GND					AD4				



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					C2			1	*
		GND					C1		ĺ		
		GND					B3		ĺ		
		GND					B2				
		GND					F3				
		GND					E2				
		GND					E1				
		GND					D3				
		GND					H3				
		GND					G2				
		GND					G1				
		GND					L2		ļ		
		GND					L1		ļ		
		GND					K3				<u> </u>
		GND					J2				
		GND					J1				
		GND			-		N2		+		
		GND					N1				
	-	GND			 		M3	1	+	1	+
	-	GND			 		T3	1	+	1	+
	-	GND			 		R2	1	+	1	+
	-	GND GND			_		R1 P3	1	 	 	+
	 	GND			_			1	 	 	+
	 	GND			 	+	V3 U2	1	+	+	+
	 	GND			 	+	U1	1	+	+	+
	-	GND					AA2		+	+	4
		GND					AA2 AA1				+
	1	GND		-		-	Y3		+		+
		GND			<u> </u>		W2		+		+
		GND			<u> </u>		W1		+		+
		GND			<u> </u>		AC2		+		+
		GND		†			AC1				†
		GND		†			AB3				†
		GND					AF3				†
		GND					AF2				†
		GND					AE2				1
		GND					AE1				1
		GND					AD3				1
		VCC					K20		1		+
		VCC					L19		1		+
		VCC					J19		1		†
		VCC					N19				1
		VCC					M20				1
		VCC					R19				1
		VCC					L17	1			1
		VCC					K18				1
		VCC					J17				
		VCC					N17				
		VCC					M18				
		VCC					T18				
		VCC					R17				
		VCC					P18				
		VCC					L15				
		VCC					K16				
		VCC					K14				
		VCC					J15				
		VCC					N15		1		
		VCC					M16		1		
		VCC					M14	ļ	1		1
	1	VCC			ļ		T16	ļ	1	1	
		VCC					T14	ļ	1		1
		VCC					R15	ļ	1		1
		VCC					P16	ļ	1		1
		VCC				1	P14	ļ	_	 	
		VCC				1	L13			_	1
		VCC				1	J13			_	1
		VCC				-	N13	ļ		-	4
		VCC				-	R13	ļ		-	4
		DNU					A4				<u> </u>



			Ta								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		DNU					A3			1	1
		DNU					C24				
		DNU					F14				
		VCCPGM					AA9				
		VCCPGM					W22				1
		VCCPGM					F8				
		VCCBAT					E8				1
		VCCIO3A					Y7				1
		VCCIO3A					AC6				1
		VCCIO3B					U8				
		VCCIO3B					V11				
		VCCIO3B					AA10				
		VCCIO3B					AD9				
		VCCIO4A					U18				
		VCCIO4A					AE22				
		VCCIO4A					AA20				
		VCCIO4A					AD19				
		VCCIO4A					Y17				
		VCCIO4A					W14				
		VCCIO4A					AC16				
		VCCIO4A					AF15				
		VCCIO4A					AB13				
		VCCIO4A					AE12				
		VCCIO5A					V21				
		VCCIO5A				<u> </u>	AB23				
		VCCIO5B					N26				1
		VCCIO5B					T25				
		VCCIO5B					W24				
		VCCIO5B					R22				
		VCCIO6A					C26				
		VCCIO6A					F25				1
		VCCIO6A					J24				1
		VCCIO6A					E22				1
		VCCIO6A					M23				1
		VCCIO6A					H21				1
		VCCIO7A					A10				1
		VCCIO7A					B23				1
		VCCIO7A					A20				1
		VCCIO7A					D19				†
		VCCIO7A					G18				1
		VCCIO7A					C16				†
		VCCIO7A					F15				+
		VCCIO7A					B13				1
		VCCIO7A					E12				+
		VCCIO7A					H11				1
		VCCIO8A					C6				1
	1	VCCIO8A			1		D9	1	1	1	1
	1	VCCIOSA VCCIOSA			1		G8	1	1	1	1
	1	VCCIO8A			1		K7	1	1	1	1
	1	VCCPD3A			1		AB9	1	1	1	1
	i	VCCPD3B4A			Ì		AB21	İ	İ		1
	1	VCCPD3B4A			1		AA19	1	1	1	1
		VCCPD3B4A					AA17				1
		VCCPD3B4A			†		AA13	1	1	1	†
	1	VCCPD3B4A				†	AA11	1	1	+	+
	1	VCCPD5A			1		U21	1	1	1	1
	1	VCCPD5B				†	N22	1	1	+	+
		VCCPD5B			†		R21	1	1	1	†
	1	VCCPD6A				†	J22	1	1	+	+
	 	VCCPD6A			<u> </u>		L21	+	+	+	+
	 	VCCPD6A VCCPD7A8A			<u> </u>		F19	+	+	+	+
		VCCPD7A8A			†		F17	+	+	+	+
	1	VCCPD7A8A VCCPD7A8A	1		1		F17	+	+	+	+
		VCCPD7A8A VCCPD7A8A			+		F13	+	+	+	+
	-	VCCPD7A8A VCCPD7A8A			1		F11	+	+	+	+
21	VREFB3AN0	VOCED3ANO			1		AC7	+	+	+	+
3A								+	+	+	+
3B	VKELB3BN0	VREFB3BN0			1	 	AC12	-		+	+
4A 5A 5B	VKEFB4AN0	VREFB4AN0			 		AD15	+	+	+	+
AC	VREFB5AN0	VEEDEDNO			1	 	W23	-		+	+
2R	VREFB5BN0	AKELRORNO		I .	I		P25				



Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin	HMC Pin
Number				3	Channel					Assignment for DDR3/DDR2 (2)	Assignment for LPDDR2
6A	VREFB6AN0	VREEB6ANO					L26			DDRO/DDRE (2)	LIBBILE
7A	VREFB7AN0	VREFB7AN0		i	1		B16				+
8A	VREFB8AN0	VREEB8ANO					C8				†
071	VICEI BOXIIVO	NC		1			AA12				+
		NC					M6				+
		NC		1			AB7				+
		NC					C4				+
		NC		1			E4				-
		NC		 			G4				+
		NC		1			L5				-
		NC		 			C3				+
		NC		 			F2				+
		NC NC					F1				+
	+	NC		+	+		E3				+
	+	NC		+	+		D2				+
		NC		1	+		D1				+
		NC NC		1	+		H2				+
		NC		+			H2 H1				
		NC		.	+						+
		VCCH_GXBL		-		+	G3 R3				+
		VCCH_GXBL									_
		VCCH_GXBL					T4				_
		VCCH_GXBL					L3				
		VCCL_GXBL					J3				
		VCCL_GXBL					N3				
		VCCL_GXBL					U3				
		RREF_TL					B1				
		VCCA_FPLL			ļ		W7				
		VCCA_FPLL					J6				
		VCCA_FPLL					Y21				
		VCCA_FPLL					G21				
		VCC_AUX					G9				
		VCC_AUX					E14				
		VCC_AUX					G19				
		VCC_AUX					AB20				
		VCC_AUX					AB14				
		VCC_AUX					AA8				
		VCCE_GXBL					K4				
		VCCE_GXBL					N5				
		VCCE_GXBL					M4				
		VCCE GXBL					R5				
		VCCE_GXBL					P4				
		VCCE_GXBL					U5				

Notes:

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.

(2) RESET pin is only applicable for DDR3 device.



Version Number	Date	Changes Made
1.0	11/29/2012	Initial release.
1.1	4/26/2013	 - Added M301 package. - Updated the column from "HMC Pin Assignment for DDR3" to "HMC Pin Assignment for DDR3/DDR2". - Added note to the "HMC Pin Assignment for DDR3/DDR2" column.
1.2	7/4/2013	Added M383 package.
1.3	8/16/2013	Added nPERSTL0 to pin16 in F484 and U484 packages.