

								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M301	DQS for X8
GXB L1		REFCLK1Ln					E20	1
GXB_L1		REFCLK1Lp					E21	
GXB L1		GXB_TX_L5n					G21	1
GXB_L1		GXB_TX_L5p					H21	
GXB L1		GXB_RX_L5p,GXB_REFCLK_L5p					F18	1
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					G18	1
GXB_L0		GXB_TX_L2n					K21	+
GXB_L0		GXB_TX_L2p					L21	+
GXB L0		GXB_RX_L2p,GXB_REFCLK_L2p		i			J18	+
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					K18	+
GXB_L0		GXB_TX_L1n		i			N21	+
GXB_L0		GXB_TX_L1p					P21	+
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					M18	1
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					N18	+
GXB_L0		GXB_TX_L0n		†			T21	+
GXB_L0		GXB_TX_L0p					U21	+
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					R18	+
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n		-			T18	+
GXB_L0	1	REFCLK0Lp	1		1	+	U19	+
	+			+	1	-		+
GXB_L0 3A	+	REFCLK0Ln		TDO	1	-	V20	+
BA BA	1	TDO		TDO			Y21	+
<i>57</i> (nCSO		DATA4			W19	+
3A		TMS		TMS			Y20	4
3A		AS_DATA3		DATA3			W20	+
3A		TCK		TCK			V19	4
3A		AS_DATA2		DATA2			Y19	
3A		TDI		TDI			AA21	
3A		AS_DATA1		DATA1			W21	
3A		DCLK		DCLK			AA20	
3A		AS_DATA0,ASDO		DATA0			AA19	
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	AA18	DQ1B
3A	VREFB3AN0	Ю		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	V17	
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	AA17	DQ1B
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	V16	DQ1B
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	Y16	DQSn1B
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	V15	DQ1B
3A	VREFB3AN0	10		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AA16	DQS1B
3A	VREFB3AN0	10		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	W16	
3A	VREFB3AN0	10		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	Y15	DQ1B
3A	VREFB3AN0	IO		DATA13	DIFFIO TX B6n	DIFFOUT B6n	V9	DQ1B
3A	VREFB3AN0	10		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	AA15	DQ1B
3A	VREFB3AN0	IO		DATA15	DIFFIO TX B6p	DIFFOUT B6p	V10	DQ1B
BA .	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	W14	
3A	VREFB3AN0	IO		PR READY	DIFFIO TX B8n	DIFFOUT B8n	V11	DQ1B
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	Y14	1
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	V12	DQ1B
3B	VREFB3BN0	10			DIFFIO_RX_B10n	DIFFOUT_B10n	Y13	1
3B	VREFB3BN0	10			DIFFIO RX B11p	DIFFOUT B11p	W13	+
3B	VREFB3BN0	10			DIFFIO_RX_B14n	DIFFOUT_B14n	AA13	+
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	AA12	+
3B	VREFB3BN0	IO	OLIVORAT EL_DE_I DII		DIFFIO_RX_B18n	DIFFOUT B18n	AA11	DQ3B
3B	VREFB3BN0	IO			DIFFIO_KX_B16II	DIFFOUT B17p	W4	DQ3B
BB	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B18p	AA10	DQ3B
3B	VREFB3BN0	IO	1		DIFFIO_RX_B19n	DIFFOUT B19n	Y10	DQSn3B
3B 3B	VREFB3BN0 VREFB3BN0	IO IO			DIFFIO_RX_B19n DIFFIO TX B20n	DIFFOUT_B19h DIFFOUT B20n		DQSn3B DQ3B
				+			V5	
3B	VREFB3BN0	10	EDIT DI OLIVOUTA EDIT DI OLIVOUT		DIFFIO_RX_B19p	DIFFOUT_B19p	Y11	DQS3B
3B	VREFB3BN0	10	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	U5	DQ3B
3B	VREFB3BN0	10			DIFFIO_RX_B22n	DIFFOUT_B22n	W6	DQ3B
3B	VREFB3BN0	10	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	V4	DQ3B
BB .	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	V6	DQ3B
3B	VREFB3BN0	10	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	U4	1
3B	VREFB3BN0	10			DIFFIO_TX_B24n	DIFFOUT_B24n	V7	DQ3B
3B	VREFB3BN0	10	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	U3	



Bank	VREF	Din Name/Frantian	Ontional Function(s)	Cantinumetian Function	Dedicated Ty/Dy	Emulated LVDS Output Channel	M301	DQS for X8
	VKEF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	W301	DQS for X8
Number 3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	W7	DQ3B
łA	VREFB4AN0	10	RZQ 0		DIFFIO_TX_B25n	DIFFOUT_B25n	T2	מנטט
IA		10	NZQ_0		DIFFIO_TX_B26n	DIFFOUT_B26n	R3	
łA		10			DIFFIO_RX_B25p	DIFFOUT B25p	T3	
								
IA.	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	R4	+
IA.	VREFB4AN0	10			DIFFIO_RX_B27n	DIFFOUT_B27n	Y8	
IA.		IO			DIFFIO_RX_B27p	DIFFOUT_B27p	Y9	
4A	VREFB4AN0	10			DIFFIO_RX_B30n	DIFFOUT_B30n	AA8	
4A	VREFB4AN0	10			DIFFIO_RX_B30p	DIFFOUT_B30p	AA7	
4A		10	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	AA6	
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	Y6	
1A	VREFB4AN0	10			DIFFIO_RX_B34p	DIFFOUT_B34p	AA5	
1A	VREFB4AN0	10			DIFFIO_RX_B35n	DIFFOUT_B35n	Y5	
1A		10			DIFFIO_RX_B35p	DIFFOUT_B35p	Y4	
1A	VREFB4AN0	10			DIFFIO_RX_B38n	DIFFOUT_B38n	Y3	
1A	VREFB4AN0	10			DIFFIO_RX_B38p	DIFFOUT_B38p	AA3	
1A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	AA2	
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	AA1	
1A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	Y1	
1A	VREFB4AN0	10			DIFFIO_RX_B46n	DIFFOUT_B46n	W1	
4A	VREFB4AN0	10			DIFFIO_RX_B46p	DIFFOUT_B46p	W2	1
4A		10			DIFFIO_RX_B47n	DIFFOUT B47n	V1	
4A	VREFB4AN0	10			DIFFIO_RX_B47p	DIFFOUT B47p	V2	
5A	VREFB5AN0	IO	RZQ 1		DIFFIO TX R1p	DIFFOUT R1p	M4	
5A	VREFB5AN0	10	1129_1	INIT DONE	DIFFIO_RX_R2p	DIFFOUT R2p	R1	
5A	VREFB5AN0	10		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT R1n	M3	
5A		10		CRC ERROR	DIFFIO RX R2n	DIFFOUT R2n	P2	
5A	VREFB5AN0	10		nCEO	DIFFIO_RX_R3p	DIFFOUT_R3p	J4	+
5A	VREFB5AN0	10		IICEO	DIFFIO_TX_R3p	DIFFOUT R4p	M2	
5A 5A				O. P. CONFRONE				
		10		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	J3	_
5A		10			DIFFIO_RX_R4n	DIFFOUT_R4n	L2	_
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	G3	
5A	VREFB5AN0	10		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	N1	
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	H4	
5A		10		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	N2	
5A	VREFB5AN0	10			DIFFIO_TX_R7p	DIFFOUT_R7p	K4	
5A		10			DIFFIO_RX_R8p	DIFFOUT_R8p	P3	
5A		10			DIFFIO_TX_R7n	DIFFOUT_R7n	K3	
5A	VREFB5AN0	10			DIFFIO_RX_R8n	DIFFOUT_R8n	N4	
5B	VREFB5BN0	10	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	L1	
5B	VREFB5BN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	E4	
5B	VREFB5BN0	10	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	K1	
5B	VREFB5BN0	10			DIFFIO_TX_R18n	DIFFOUT_R18n	E3	
5B	VREFB5BN0	10			DIFFIO_RX_R19p	DIFFOUT_R19p	H1	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	F3	
5B	VREFB5BN0	10			DIFFIO_RX_R19n	DIFFOUT R19n	J2	+
5B	VREFB5BN0	10	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn	1	DIFFIO_TX_R20n	DIFFOUT_R20n	G4	1
5B	VREFB5BN0	10		+	DIFFIO_RX_R21p	DIFFOUT_R21p	H2	+
5B	VREFB5BN0	10		+	DIFFIO_RX_R21n	DIFFOUT_R21n	G2	+
5B	VREFB5BN0	10			DIFFIO_TX_R22n	DIFFOUT R22n	E5	+
5B	VREFB5BN0	10			DIFFIO_TX_R22fi DIFFIO_RX_R23p	DIFFOUT_R23p	F1	+
		10		+			E1	+
5B	VREFB5BN0				DIFFIO_TX_R24p	DIFFOUT_R24p		+
5B	VREFB5BN0	IO OND		-	DIFFIO_RX_R23n	DIFFOUT_R23n	F2	+
7.0	VDEEDTANK	GND		-	DIEERO DY TOT	DIFFOLIT TAZ-	D2	+
7A	VREFB7AN0	10			DIFFIO_RX_T17p	DIFFOUT_T17p	C1	
7A	VREFB7AN0	10			DIFFIO_RX_T17n	DIFFOUT_T17n	C2	
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	A1	
7A	VREFB7AN0	10			DIFFIO_RX_T19n	DIFFOUT_T19n	B2	
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	A2	
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	A3	
	VREFB7AN0	10			DIFFIO_RX_T27p	DIFFOUT_T27p	B3	
7A	VKEFD/AINU							
7A 7A		10			DIFFIO_RX_T27n	DIFFOUT_T27n	C4	



Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	M301	DQS for X8
lumber			,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	3	Channel			
Α	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	B4	
4	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	C5	
	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT T34n	D6	
·	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	B5	
· ·	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	C6	
\	VREFB7AN0	10			DIFFIO_TX_T35p	DIFFOUT T35n	A6	
١	VREFB7AN0				DIFFIO_TX_T36n	DIFFOUT_T36n	D7	
١	VREFB7AN0	10			DIFFIO_RX_T37p	DIFFOUT_T37p	A7	
١	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	B7	
١	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	D9	
ı	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	A8	
١	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	C7	
	VREFB7AN0	Ю			DIFFIO_RX_T39n	DIFFOUT_T39n	B8	
	VREFB7AN0	Ю	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	D8	
	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	C12	
	VREFB8AN0	10			DIFFIO TX T42p	DIFFOUT T42p	D14	DQ6T
	VREFB8AN0	10	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	D11	
	VREFB8AN0	IO			DIFFIO TX T42n	DIFFOUT T42n	D13	DQ6T
	VREFB8AN0	10	 	 	DIFFIO_RX_T43p	DIFFOUT_T43p	C10	DQ6T
	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB	+	DIFFIO_TX_T44p	DIFFOUT T44p	C17	DQ6T
		IO IO		+	DIFFIO_TX_T44p		B11	
	VREFB8AN0		EDIT TI OLIVOUTA EDIT TI OLIVOUTE			DIFFOUT_T43n		DQ6T
	VREFB8AN0	10	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	D17	DQ6T
	VREFB8AN0	10			DIFFIO_RX_T45p	DIFFOUT_T45p	A10	DQS6T
	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	B10	DQSn6T
	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	D16	DQ6T
	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	B12	DQ6T
	VREFB8AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	C16	DQ6T
	VREFB8AN0	10			DIFFIO_RX_T47n	DIFFOUT_T47n	A13	DQ6T
1	VREFB8AN0	10	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	A11	
1	VREFB8AN0	10	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	A12	
١	VREFB8AN0	IO			DIFFIO RX T51p	DIFFOUT T51p	B13	
1	VREFB8AN0	10			DIFFIO_RX_T53n	DIFFOUT_T53n	B14	
١	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	A15	
À .	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	B15	
À .	VICEI DO/1140	MSEL0		MSEL0	DII 110_10X_100II	Bii 1 001_100ii	A17	
A A		CONF_DONE		CONF_DONE			A16	
1								
	+	MSEL1		MSEL1			A19	
١		nSTATUS		nSTATUS			A18	
١		nCE		nCE			A20	
١		MSEL2		MSEL2			A21	
		MSEL3		MSEL3			B20	
		nCONFIG		nCONFIG			D19	
		MSEL4		MSEL4			B19	
		GND					C19	
		GND					M21	
		GND					M9	
		GND					A9	1
	1	GND			1		D10	İ
	1	GND	 	 	+	<u> </u>	J19	1
	 	GND	+	+	+		K13	+
	 	GND			+		J10	+
	+	GND	+	+	+	+	M11	-
	 							+
	 	GND	+		1	+	G20	+
	1	GND	+		+		F19	-
		GND					A4	
	1	GND			1		J12	
		GND					W5	
		GND					U18	
		GND					H20	
		GND					P18	
		GND					V13	
	1	GND					N12	Ì



							Note (1)		
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel		DQS for X8	
		GND					R19		
		GND					L4		
		GND					K11		
		GND					P20		
		GND					D15		
		GND					N10		
		GND					L18		
		GND					F4		
		GND		<u> </u>			M13		
	1	GND		+					
		GND					B16		
							W10		
		GND					E2		
		GND					U20		
		GND					L20		
		GND					H18		
		GND					B1		
		GND					K9		
		GND					E18		
		GND					D21		
		GND					НЗ		
	1	GND					R21		
	1	GND		1	İ		K19	1	
	İ	GND		1	İ		G19	1	
		GND					F21		
		GND					U1		
		GND		<u> </u>			J21		
	1	GND		+			T19		
	-								
		GND					M19		
		GND					D5		
		GND					V21		
		GND					T4		
		GND					V8		
		GND					C18		
		GND					AA14		
		GND					T20		
		GND					V3		
		GND					N20		
		GND					N19		
		GND					K20		
		GND					B21		
		vcc					L9		
		VCC					N11		
		VCC					L13		
	+	VCC	<u> </u>	†	†		J9		
	+	VCC		+	+	 	J9 J11	 	
	+	VCC			-			-	
	+		<u> </u>	 	 	 	M10	1	
	1	VCC			1		L12		
	_	VCC					M12		
	ļ	VCC		ļ			K10	ļ	
	ļ	VCC		ļ			N13	ļ	
		VCC					L10		
		VCC					K12		
		VCC			L		N9		
		VCC					L11		
		VCC					J13		
		DNU					C20		
	1	DNU					D20		
	1	DNU			İ		D4		
	1	DNU		1	1		D12	1	
	1	VCCPGM			 		Y18	-	
	+	VCCPGM	<u> </u>	†	†		T10	+	
	1	VCCPGM		<u> </u>	 		B17	1	
	1	VCCBAT		 	-		D18	 	
	1	VOCBAT					סוט	1	



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M301	DQS for X8
		VCCIO3A					W15	
		VCCIO3A					Y17	
		VCCIO3B					AA9	
		VCCIO3B					Y12	
		VCCIO4A					Y2	
		VCCIO4A					AA4	
		VCCIO4A					Y7	
		VCCIO5A					R2	
		VCCIO5A					N3	
		VCCIO5B					G1	
		VCCIO5B					K2	
		VCCIO7A					C8	
		VCCIO7A					B6	
		VCCIO7A					C3	
		VCCIO8A					A14	
	1	VCCIO8A					C13	1
	1	VCCPD3A					W17	1
		VCCPD3B4A					V14	
		VCCPD3B4A					W9	
		VCCPD5A					P1	
		VCCPD5B					J1	
		VCCPD7A8A		1			C14	
		VCCPD7A8A					B9	
Α	VREFB3AN0	VREFB3AN0					V18	
3 B	VREFB3BN0	VREFB3BN0					W12	
A	VREFB4AN0	VREFB4AN0		1			W8	
4 4	VREFB5AN0	VREFB5AN0					P4	
B	VREFB5BN0	VREFB5BN0		1			L3	
A	VREFB7AN0	VREFB7AN0					C9	+
4 4	VREFB/AN0	VREFB8AN0					C15	+
n .	VKEFBOAINU	VCCH_GXBL					M20	_
		VCCH_GXBL					E19	+
		VCCL_GXBL		ļ			J20	
		VCCL_GXBL VCCL_GXBL		ļ			R20	
				<u> </u>				
		RREF_TL					C21	
	-	VCCA_FPLL					U17 E17	+
	-	VCCA_FPLL						+
	-	VCCA_FPLL					U2	+
	-	VCCA_FPLL					D1	+
		VCC_AUX					B18	
	_	VCC_AUX					W18	
		VCC_AUX					C11	
		VCC_AUX					W11	
		VCC_AUX					D3	
		VCC_AUX					W3	1
		VCCE_GXBL					P19	1
		VCCE_GXBL					L19	
		VCCE_GXBL					F20	
		VCCE_GXBL					H19	

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.



Name Control											Note (1)
	Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin	HMC Pin
SECOND S	Number			. , ,			·				Assignment for
Marchest Marchest										DDR3/DDR2 (2)	LPDDR2
Marchest Marchest											
001 1								G23			
Col.											
Sign Ling Sign Sign											
09-11											
0811											
Column C											
SOLITION SOlition SOLITION SOLITION SOLITION SOLITION SOLITION SOLITION SOLITION SOLITION SOLITION SOLITION SOLITION	GXB_L1										
Description											
100.11											
Col.											
Section Sect										<u> </u>	
Cold											
Cold Cold			GXB_RX_L3p,GXB_REFCLK_L3p							<u> </u>	
Col. Col. Col. Type Col.										<u> </u>	
0.00	GXB_L0										
0.00 0.00											
1986 1986 174. 1987			GXB_RX_L2p,GXB_REFCLK_L2p								
Section Sect											
See 1											
Coll											
1989 1, 1989											
Color Colo		 		+		-	+			 	
GORD GORD RECOLUDE		 				-	-		-	 	
GORD GORD REPORT IN AC22		1		+	1	+	 		+	+	├
March Marc		 	CVB BY LOD CVB BEFOLK LOD			-	-		-	 	
SEFENAND SEFENAND		 		+		-	+			 	
TOO		1				-			-		
March Marc					TDO		-				
186 186	3A	1				-			-		
A	3A		TMC								
TOK	3A						-				
AS DATE DATE	3A	1				-			-		
Mail							-				
AS DATA COLK ACCURATE ACC	3A	1				-			-		
DCLK			1							+	
AS NEFESAND CO	3A										
MINEREDAMO C										+	
MEFERSAND O	34	V/DEER3ANO				DIEEIO BY Bin	DIEEOLIT B1n		DO1B	+	
MATERIANNO O									DQID		
Maria Mari						DIFFIO PX B1n			DO1B	+	
MATERIANNO D											
March Marc	3A		10								
VREPSAND											
Marie Mari	3A					DIFFIO RX B3p					
Nefesano C									Daoib		
ASA VREEBAND O	3A	VREFB3AN0				DIFFIO RX B5n			DQ1B		
VREFBAND O											
ASA VREFBAND O	3A										
VREFBANN O			10						DQ1B	1	
NREFSBAND C	3A					DIFFIO RX B7n					
NRERBANN O									DQ1B		
NEFB38NO O	3A					DIFFIO RX B7p	DIFFOUT B7p			1	
NEFB3BNO O DIFFIO R, 8100 DIFFOUR, 8110 DIFFOUR B110 AA16 DIFFOUR B110 AA16 DIFFOUR B110 AC16 A	3A								DQ1B		
DIFFIC RX B11p DIFFOUT B11p AC16	3B										
NEFESBIND O	3B										
NEFESSINO O	3B	VREFB3BN0				DIFFIO_RX_B14n					
NEFESSINO O	3B	VREFB3BN0				DIFFIO_RX_B15n	DIFFOUT_B15n	AD15			
NEFRSBNO O	3B										
NEFESBNO IO DIFFIC RX, B18n DIFFOUT, B18n AE13 DO28	3B	VREFB3BN0	10			DIFFIO_TX_B17n	DIFFOUT_B17n	AB14			
NEFESBNO IO DIFFIC RX, B18p DIFFOUT, B18p AE12 DO28	3B					DIFFIO_RX_B18n					
NEFESBNO IO DIFFIC RX, B18p DIFFOUT, B18p AE12 DO28	3B										
NEFESBNO O	3B	VREFB3BN0	10			DIFFIO_RX_B18p		AE12			
NEFESBNO O	3B										
NEFESBIND O DIFFIO TX B19p DIFFOUT B19p AE10 DOS2B	3B					DIFFIO_TX_B20n			DQ2B		
	3B					DIFFIO_RX_B19p			DQS2B		
NEFESBNO IO	3B	VREFB3BN0				DIFFIO_TX_B20p					
	3B			FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn							
		VREFB3BN0	10			DIFFIO_RX_B22n	DIFFOUT_B22n	AD11	DQ2B		
	3B			FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p					
	3B		10			DIFFIO_RX_B22p	DIFFOUT_B22p	AC12	DQ2B		
	3B	VREFB3BN0		CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	AD10			
38 VREFB38N0 O CLK/p DIFFOUT R. B23p DIFFOUT B23p AD9	3B					DIFFIO_TX_B24n			DQ2B		
38 VREFB38N0 O DIFFIO_TX_B24p DIFFOUT_B24p AA11 DQ28	3B			CLK1p							
4A VREFB4AND IO RZQ_0 DIFFIO_TX_B25n DIFFOUT_B25n AB10 AB10 4A VREFB4AND IO DIFFIO_TX_B25n DIFFOUT_B25n AE8 DQ3B 4A VREFB4AND IO DIFFIO_TX_B25p DIFFOUT_B25p AA9 DQ3B	3B								DQ2B		
4A VREFB4AN0 IO DIFFIO_TX_B25p DIFFOUT_B25p AA9 DQ3B	4A			RZQ_0			DIFFOUT_B25n	AB10			
	4A		IO								
4A VREFB4AND IO DIFFIO RX B26p DIFFOUT B26p AD8 DQ3B 4A VREFB4AND IO DIFFIO_RX_B27n DIFFOUT_B27n AC9 DQ5n3B										<u> </u>	
4A VREFB4AN0 IO DIFFIO_RX_B27n DIFFOUT_B27n AC9 DQSn3B	4A	VREFB4AN0				DIFFIO_RX_B26p	DIFFOUT_B26p	AD8			
	4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AC9	DQSn3B		



										Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
										<u> </u>
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_TX_B28n DIFFIO_RX_B27p	DIFFOUT_B28n DIFFOUT_B27p	AB9 AC8	DQ3B DQS3B		+
IA	VREFB4AN0	10			DIFFIO_TX_B28p	DIFFOUT_B28p	AA8	DQS3B	+	+
IA	VREFB4AN0	10			DIFFIO_TX_B29n	DIFFOUT_B29n	AC7	DQ3B	1	
1A	VREFB4AN0	10			DIFFIO_RX_B30n	DIFFOUT_B30n	AE6	DQ3B		
4A	VREFB4AN0	10			DIFFIO_TX_B29p	DIFFOUT_B29p	AC6	DQ3B		
4A	VREFB4AN0	10	OLIVO.		DIFFIO_RX_B30p	DIFFOUT_B30p	AD6	DQ3B		
4A 4A	VREFB4AN0 VREFB4AN0	10	CLK2n		DIFFIO_RX_B31n DIFFIO_TX_B32n	DIFFOUT_B31n DIFFOUT_B32n	AE5 AC4	DQ3B	+	+
4A	VREFB4AN0	10	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	AD5	DQSB	+	
4A	VREFB4AN0	10			DIFFIO_TX_B32p	DIFFOUT_B32p	AB5	DQ3B	1	
4A	VREFB4AN0	Ю			DIFFIO_TX_B33n	DIFFOUT_B33n	AC3			
4A	VREFB4AN0	10			DIFFIO_RX_B34n	DIFFOUT_B34n	AE3	DQ4B		
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_TX_B33p DIFFIO_RX_B34p	DIFFOUT_B33p DIFFOUT_B34p	AB4 AE2	DQ4B DQ4B		+
4A	VREFB4AN0	10			DIFFIO_RX_B35n	DIFFOUT_B34p DIFFOUT_B35n	AD4	DQSn4B	+	+
4A	VREFB4AN0	10			DIFFIO_TX_B36n	DIFFOUT_B36n	AA4	DQ4B	+	+
4A	VREFB4AN0	10			DIFFIO_RX_B35p	DIFFOUT_B35p	AD3	DQS4B		
4A	VREFB4AN0	Ю			DIFFIO_TX_B36p	DIFFOUT_B36p	AA3		1	
4A	VREFB4AN0	Ю			DIFFIO_TX_B37n	DIFFOUT_B37n	W3	DQ4B	<u> </u>	
4A	VREFB4AN0	10		1	DIFFIO_RX_B38n	DIFFOUT_B38n	AE1	DQ4B	+	+
4A 4A	VREFB4AN0 VREFB4AN0	10	-	-	DIFFIO_TX_B37p DIFFIO_RX_B38p	DIFFOUT B37p	V4 AD1	DQ4B	+	+
4A 4A		10	CLK3n	1	DIFFIO_RX_B38p DIFFIO_RX_B39n	DIFFOUT_B38p DIFFOUT_B39p	AD1 AC2	DQ4B	+	+
4A	VREFB4AN0	IO	CHOIL		DIFFIO_TX_B40n	DIFFOUT_B40n	Y3	DQ4B	+	
4A	VREFB4AN0	10	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	AC1		1	1
4A	VREFB4AN0	10			DIFFIO_TX_B40p	DIFFOUT_B40p	W4	DQ4B		
4A	VREFB4AN0	Ю			DIFFIO_RX_B43n	DIFFOUT_B43n	AB2			
4A	VREFB4AN0	10			DIFFIO_RX_B43p	DIFFOUT_B43p	AB1			
4A	VREFB4AN0	10			DIFFIO_RX_B46n	DIFFOUT_B46n	AA2	1		+
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_RX_B46p DIFFIO_RX_B47n	DIFFOUT_B46p DIFFOUT_B47n	Y2 Y1			+
4A	VREFB4AN0	10			DIFFIO_RX_B47p	DIFFOUT_B47II	W1		+	+
5A	VREFB5AN0	10	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	U2	DQ1R	+	1
5A		10		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V2		1	1
5A	VREFB5AN0	10		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	U1	DQ1R		
5A		10		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V1			
5A	VREFB5AN0	10		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T4	DQ1R		
5A	VREFB5AN0 VREFB5AN0	10		C.D. CONEDONE	DIFFIO_RX_R4p DIFFIO_TX_R3n	DIFFOUT_R4p DIFFOUT_R3n	R2 R3	DQ1R DQ1R		+
5A 5A	VREFB5AN0	10		CvP_CONFDONE	DIFFIO_IX_R3fi	DIFFOUT_R4n	T2	DQ1R DQ1R	+	+
5A	VREFB5AN0	10		DEV_OE	DIFFIO_RX_R4fi	DIFFOUT_R5p	P3	DQIK	+	+
5A	VREFB5AN0	10		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT R6p	P1	DQS1R	+	
5A	VREFB5AN0	10		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	N2	DQ1R	1	1
5A	VREFB5AN0	10		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	R1	DQSn1R		
5A	VREFB5AN0	10			DIFFIO_TX_R7p	DIFFOUT_R7p	N4	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	M1	DQ1R		
5A 5A	VREFB5AN0	10			DIFFIO_TX_R7n DIFFIO_RX_R8n	DIFFOUT_R7n	N3 N1	DQ1R		+
5B	VREFB5AN0 VREFB5BN0	10	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R8n DIFFOUT_R17p	L2	DQTR	+	+
5B	VREFB5BN0	10	CLK6n		DIFFIO_RX_R17p	DIFFOUT_R17n	M2		+	+
5B	VREFB5BN0	10	outon		DIFFIO RX R19p	DIFFOUT_R19p	K2	1	+	+
5B	VREFB5BN0	10	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	M4		1	
5B	VREFB5BN0	10			DIFFIO_RX_R19n	DIFFOUT_R19n	K1			1
5B	VREFB5BN0	10	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn	ļ	DIFFIO_TX_R20n	DIFFOUT_R20n	L3			4
5B	VREFB5BN0	10		1	DIFFIO_RX_R21p	DIFFOUT_R21p	H1	1	+	+
5B 5B	VREFB5BN0 VREFB5BN0	10		+	DIFFIO_TX_R22p DIFFIO_RX_R21n	DIFFOUT_R22p DIFFOUT_R21n	J4 .J1	 	+	+
5B	VREFB5BN0 VREFB5BN0	10	1	 	DIFFIO_RX_R21n DIFFIO_TX_R22n	DIFFOUT_R22n	J1 J3	†	+	+
5B	VREFB5BN0	10			DIFFIO_RX_R23p	DIFFOUT_R23p	H2	1		1
5B	VREFB5BN0	10			DIFFIO_TX_R24p	DIFFOUT_R24p	H4			
5B	VREFB5BN0	10			DIFFIO_RX_R23n	DIFFOUT_R23n	G1			
5B	VREFB5BN0	Ю			DIFFIO_TX_R24n	DIFFOUT_R24n	H3			
~.	Lunger	GND		ļ	DIEERO DI TIT	DISCOUT TAT	F3	.	CNID	CNID
7A 7A	VREFB7AN0 VREFB7AN0	10		-	DIFFIO_RX_T17p DIFFIO_RX_T17n	DIFFOUT_T17p DIFFOUT_T17n	E1 D1	 	GND GND	GND GND
7A 7A		10	†	1	DIFFIO_RX_117n DIFFIO_RX_T19p	DIFFOUT_T19p	D1 F2	1	GIND	GIND
7A	VREFB7AN0	10		<u> </u>	DIFFIO_RX_T19p	DIFFOUT_T19n	E2	†	+	
7A	VREFB7AN0	10			DIFFIO_TX_T22p	DIFFOUT_T22p	F4	1	T_RESET#	T_RESET#
7A	VREFB7AN0	10			DIFFIO_RX_T23p	DIFFOUT_T23p	E3			
7A	VREFB7AN0	10			DIFFIO_RX_T23n	DIFFOUT_T23n	D3			
7A	VREFB7AN0	10	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	C1			
7A		10			DIFFIO_TX_T26p	DIFFOUT_T26p	C7	DQ1T	T_DM_1	T_DM_1
7A	VREFB7ANO	10	CLK11n	1	DIFFIO_RX_T25n	DIFFOUT_T25n	B1	DOAT	T DO 45	T DO 45
7A 7A	VREFB7AN0 VREFB7AN0	10	-	-	DIFFIO_TX_T26n DIFFIO_RX_T27p	DIFFOUT_T26n DIFFOUT_T27p	C6 C3	DQ1T DQ1T	T_DQ_15 T_DQ_13	T_DQ_15 T_DQ_13
7A 7A	VREFB7AN0	10	 		DIFFIO_RX_127p	DIFFOUT_T28p	D4	DQ1T	T_DQ_13	T_DQ_13
7A 7A	VREFB7AN0	10	1	t	DIFFIO_TX_T26p	DIFFOUT_T27n	C2	DQ1T	T DQ 12	T_DQ_12
	VREFB7AN0	10			DIFFIO_TX_T28n	DIFFOUT_T28n	C4	DQ1T	T CKE 0	T CKE 0
7A 7A	VKEFB/AINU									



	wass	In the state of	le e us e to	In	In. r	Is a suppose	luc	Inco / ···	luna r	Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
	VREFB7AN0	10			DIFFIO_TX_T30p	DISSOLIT TOO	D8		T CKE 1	T CKE 1
A A	VREFB7AN0				DIFFIO_TX_T30p DIFFIO_RX_T29n	DIFFOUT_T30p DIFFOUT_T29n	A2	DQSn1T	T_DQS#_1	T_DQS#_1
4	VREFB7AN0	10			DIFFIO_TX_T30n	DIFFOUT_T30n	C8	DQ1T	T_DQ_11	T_DQ_11
4	VREFB7AN0	10			DIFFIO RX T31p	DIFFOUT T31p	A4	DQ1T	T DQ 11	T DQ 9
A	VREFB7AN0	10			DIFFIO_TX_T32p	DIFFOUT_T32p	B5	DQ1T	T_DQ_10	T_DQ_10
A	VREFB7AN0	10			DIFFIO_RX_T31n	DIFFOUT_T31n	A3	DQ1T	T_DQ_8	T_DQ_8
A	VREFB7AN0	10			DIFFIO_TX_T32n	DIFFOUT_T32n	B4		GND	GND
A	VREFB7AN0	10	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	B6			
Ά	VREFB7AN0	10			DIFFIO_TX_T34p	DIFFOUT_T34p	E8	DQ2T	T_DM_0	T_DM_0
Ά	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	A5		T DO 7	T DO =
'A	VREFB7AN0 VREFB7AN0	10			DIFFIO_TX_T34n DIFFIO_RX_T35p	DIFFOUT_T34n DIFFOUT_T35p	D9 B7	DQ2T DQ2T	T DQ 7 T DQ 5	T DQ 7 T DQ 5
A A	VREFB7AN0 VREFB7AN0				DIFFIO_RX_T35p	DIFFOUT_T36p	E10	DQ2T	T DQ 6	T DQ 6
'A	VREFB7AN0	10			DIFFIO_RX_T35n	DIFFOUT_T35n	A7	DQ2T	T DQ 4	T DQ 4
A		10			DIFFIO TX T36n	DIFFOUT_T36n	D10	DQ2T	T_DQ_4	T_ODT_1
Ά	VREFB7AN0	10			DIFFIO_RX_T37p	DIFFOUT_T37p	A9	DQS2T	T_DQS_0	T DQS 0
Ά	VREFB7AN0	10			DIFFIO_TX_T38p	DIFFOUT_T38p	E11		T_ODT_0	T_ODT_0
Ά	VREFB7AN0	10			DIFFIO_RX_T37n	DIFFOUT_T37n	A8	DQSn2T	T_DQS#_0	T_DQS#_0
A	VREFB7AN0				DIFFIO_TX_T38n	DIFFOUT_T38n	D11	DQ2T	T_DQ_3	T_DQ_3
Ά	VREFB7AN0	10			DIFFIO_RX_T39p	DIFFOUT_T39p	B9	DQ2T	T_DQ_1	T_DQ_1
Ά	VREFB7AN0	IO		+	DIFFIO_TX_T40p	DIFFOUT_T40p	C11	DQ2T	T_DQ_2	T_DQ_2
A	VREFB7AN0	IO .	270.0	+	DIFFIO_RX_T39n	DIFFOUT_T39n	A10	DQ2T	T DQ 0	T DQ 0
A	VREFB7AN0 VREFB8AN0	10	RZQ_2	+	DIFFIO_TX_T40n	DIFFOUT_T40n	B10	-	-	+
A A	VREFB8AN0 VREFB8AN0	10	CLK9p	+	DIFFIO_RX_T41p DIFFIO_TX_T42p	DIFFOUT_T41p DIFFOUT_T42p	B12 E13	DQ3T	T_A 0	T_CA_0
A	VREFB8AN0 VREFB8AN0	10	CLK9n	1	DIFFIO_TX_T42p DIFFIO_RX_T41n	DIFFOUT_T41n	E13	DUST	1_A_0	1_CA_U
SA.	VREFB8AN0	10	OLIVAN	+	DIFFIO_TX_T42n	DIFFOUT_T41n	D14	DQ3T	T A 1	T_CA_1
BA .	VREFB8AN0	10			DIFFIO_RX_T43p	DIFFOUT_T43p	A14	DQ3T	T_A_4	T_CA_4
SA.	VREFB8AN0	10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	E15	DQ3T	T_A_2	T_CA_2
3A	VREFB8AN0	Ю			DIFFIO_RX_T43n	DIFFOUT_T43n	A13	DQ3T	T A 5	T CA 5
SA.	VREFB8AN0	10	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	D15	DQ3T	T_A_3	T_CA_3
\$A	VREFB8AN0	10			DIFFIO_RX_T45p	DIFFOUT_T45p	C13	DQS3T	T_CK	T_CK
\$A	VREFB8AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	E17		T_A_6	T_CA_6
BA .		10			DIFFIO_RX_T45n	DIFFOUT_T45n	C12	DQSn3T	T_CK#	T_CK#
BA	VREFB8AN0	10			DIFFIO_TX_T46n	DIFFOUT_T46n	E16	DQ3T	T_A_7	T_CA_7
BA	VREFB8AN0	10			DIFFIO_RX_T47p	DIFFOUT_T47p	C14	DQ3T	T_BA_1	
3A	VREFB8AN0	IO		_	DIFFIO_TX_T48p	DIFFOUT_T48p	C16	DQ3T	T_BA_0	4
BA .	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	B14	DQ3T	T_BA_2	OND
BA BA	VREFB8AN0 VREFB8AN0	10	CLIVA- EDIL TI ED-		DIFFIO_TX_T48n DIFFIO_RX_T49p	DIFFOUT_T48n DIFFOUT_T49p	B15 B16		GND	GND
	VREFB8AN0	10	CLK8p,FPLL_TL_FBp	+				DQ4T	T_CAS#	+
BA BA	VREFB8AN0	10	CLK8n,FPLL_TL_FBn		DIFFIO_TX_T50p DIFFIO_RX_T49n	DIFFOUT_T50p DIFFOUT_T49n	E18 A15	DQ41	1 CA3#	+
BA .	VREFB8AN0	10	CEROII,FFEE_1E_FBII		DIFFIO_KX_149II	DIFFOUT_T50n	D19	DQ4T	T_RAS#	+
BA .	VREFB8AN0	10			DIFFIO_RX_T51p	DIFFOUT_T51p	B17	DQ4T	T A 8	T_CA_8
BA	VREFB8AN0	10			DIFFIO_TX_T52p	DIFFOUT_T52p	C19	DQ4T	T_A_10	1
BA.	VREFB8AN0	10			DIFFIO_RX_T51n	DIFFOUT_T51n	A17	DQ4T	T_A_9	T_CA_9
3A	VREFB8AN0	10			DIFFIO_TX_T52n	DIFFOUT_T52n	C18	DQ4T	T_A_11	
BA	VREFB8AN0	Ю			DIFFIO_RX_T53p	DIFFOUT_T53p	A19	DQS4T	T_CS#_0	T_CS#_0
3A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	C21		T_A_12	
BA .	VREFB8AN0	10			DIFFIO_RX_T53n	DIFFOUT_T53n	A18	DQSn4T	T_CS#_1	T_CS#_1
SA.	VREFB8AN0	IO		1	DIFFIO_TX_T54n	DIFFOUT_T54n	B20	DQ4T	T_A_13	+
BA BA	VREFB8AN0 VREFB8AN0	10	<u> </u>	+	DIFFIO RX T55p	DIFFOUT_T55p DIFFOUT_T56p	B19 D21	DQ4T DQ4T	T A 14 T WE#	+
				+						+
BA BA	VREFB8AN0	MSFI 0		MSEL0	DIFFIO_RX_T55n	DIFFOUT_T55n	A20 A23	DQ4T	T_A_15	+
A A	1	CONF_DONE		CONF_DONE	+	+	A23 A22	1	+	+
A A	1	MSEL1		MSEL1	+	+	A24	+		+
A A	1	nSTATUS		nSTATUS	1	+	B22	1		1
A A		nCE		nCE			A25			
9A		MSEL2		MSEL2	1		B25	1		1
BA .		MSEL3		MSEL3			B24			
Α		nCONFIG		nCONFIG			C23			
Α		MSEL4		MSEL4			C24			
		GND					C22			
		GND			-		A1			
		GND			-		A11			
	+	GND		1	1	+	AA1	+		+
	+	GND		+	+	-	AA10	+		+
	+	GND GND		+	+	-	AA15	+		+
	+			+	+	+	AA23 AB13	+	-	+
	+	GND GND		+	+	+	AB13 AB24	+	-	+
	+	GND		+	+	+	AB24 AC10	+	-	+
	1	GND		+	+	+	P25	1	+	+
	1	GND		+	+	+	AC25	1	+	+
	1	GND		+	+	+	AC5	1	+	+
	1	GND		1	1	+	AD17	1		1
	1	GND		1	1		AD22	1		
	1	GND		1			AE14		İ	1
		GND					AE19			
		•								





2 _										
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	Assignment for	Note (1 HMC Pin Assignment for LPDDR2
									. ,	
		GND					AE4			
		GND GND					B13			
		GND					B18 B23			
		GND					B8			
		GND					C25			
		GND					C5			
		GND GND					D12 D17			
		GND				+	D17 D2			
		GND					D22			
		GND					D22 D7			
		GND					E14			
		GND					E23			
		GND GND				+	E25 E4			
		GND					F24			1
		GND					G3			
		GND					H25			
		GND				1	R23			
		GND GND					K4 L1			
		GND				1	L12		 	
		GND					L14			
		GND					M11			
		GND					M13			
		GND			ļ		M15	ļ	 	
		GND GND		 	1	+	M23 P11	1	 	
		GND					P13			
		GND					P15			
		GND					R12			
		GND					R14			
		GND GND					R24 T22			<u> </u>
		GND					T24			
		GND					U23			
		GND					U25			
		GND					V23			
		GND GND					V24 Y23			
		GND					Y25			-
		GND					AB22			
		GND					F23			
		GND					AA24 G22			
		GND					G22			ļ
		GND GND					G24			
		GND					H23 J23			-
		GND					J24			
		GND					K22			
		GND					K24			
		GND GND				-	L23 L25			ļ
		GND				+	L25 M24	1	1	
		GND			1	1	N22	1	 	
		GND					N24			
		GND					P23			
		GND			1	1	T1	1	1	
		GND GND		 	1	+	U3 W22	1	 	
		GND			 	1	W24	 	 	
		GND			İ		Y4	İ	İ	
		VCC					L11			
		VCC					L13			
		VCC	<u> </u>		 	 	L15	 	 	
		vcc vcc				1	M12 M14	1	1	
		VCC					N11		1	
		VCC					N12			
		VCC					N13			
		VCC				ļ	N14			<u> </u>
		VCC	<u> </u>		 	 	N15	 	 	
		VCC VCC		 	1	+	P12 P14	1	 	
		VCC			1	1	R11	1	 	
		VCC					R13			
		VCC					R15			
		DNU				ļ	D24			
		DNU	1	1	1	i e	E24	1	1	1



Pin Information for the Cyclone® V 5CGXFC5 Device

		1	T			T		1		Note
ank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin	HMC Pin
mber					Channel				Assignment for	Assignment for
									DDR3/DDR2 (2)	LPDDR2
		DNU					G2			
		DNU					B11			
		VCCPGM					AC21			
		VCCPGM					T3			
		VCCPGM					D20			
		VCCBAT					B21			
		VCCIO3A					AB18			
		VCCIO3A					AC20			
	1	VCCIO3B					AC15			
	†	VCCIO3B VCCIO3B				+	AD12			
	†	VCCIO3B VCCIO3B				+	AE9			
	1	VCCIO3B VCCIO4A			1		AB3			
	1	VCCIO4A VCCIO4A					AB8	+		
	<u> </u>					_			_	
		VCCIO4A					AD2			
		VCCIO4A					AD7			
	ļ	VCCIO4A	_			-	W2	ļ		ļ
	l	VCCIO5A			1		P2	1		ļ
		VCCIO5A					R4			
		VCCIO5B					J2			
		VCCIO5B				1	M3			
		VCCIO7A					A6			
		VCCIO7A					B3			
		VCCIO7A					C10			
		VCCIO7A					E9			
	1	VCCIO7A			+		F1	+		1
	1	VCCIO7A VCCIO8A			1		A16			
	1				+		A21	+		
		VCCIO8A								
		VCCIO8A					C15			
		VCCIO8A					C20			
		VCCPD3A					AB16			
		VCCPD3B4A					AB7			
		VCCPD3B4A					AC13			
		VCCPD5A					P4			
		VCCPD5B					L4			
		VCCPD7A8A					D13			
		VCCPD7A8A					D16			
		VCCPD7A8A					D6			
	VREFB3AN0	VREFB3AN0					AD20			1
	VREFB3BN0	VREFB3BN0			+		AC11	+		1
	VREFB4AN0	VREFB4AN0			1		AE7			1
	VREFB5AN0	VREFB5AN0			+		V3	+		
	VREFB5BN0	VREFB5BN0					K3			
	VREFB7AN0	VREFB7AN0					C9			
	VREFB8AN0	VREFB8AN0			↓	1	C17	ļ		ļ
	l	VCCH_GXBL			1		L24	1		l
		VCCH_GXBL					U24			
		VCCL_GXBL					K23			
		VCCL_GXBL					T23			
		RREF_TL					D25			
		VCCA_FPLL					AB23			
		VCCA_FPLL				1	D23		İ	
	1	VCCA_FPLL			İ	İ	U4	1	İ	1
	1	VCCA_FPLL			1	1	G4	1	1	1
	 	VCC_AUX		+	+	+	AA13	1	+	1
	l	VCC_AUX		+	1	+	AA18	1	+	1
	 				 			-	_	
	!	VCC_AUX			+	+	AB6	!	_	l
	ļ	VCC_AUX	_			-	D18	ļ	_	ļ
	l	VCC_AUX			1		D5	1		ļ
	<u> </u>	VCC_AUX			1	1	E12			<u> </u>
		VCCE_GXBL					N23			
		VCCE_GXBL					P24			
	Ì	VCCE_GXBL		İ			W23	1		Ì

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.

(2) RESET pin is only applicable for DDR3 device.



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
GXB_L1		REFCLK1Ln					F5				
GXB_L1		REFCLK1Lp					G4				
GXB_L1 GXB_L1		GXB_TX_L5n GXB_TX_L5p					D3				
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					C2				
GXB_L1		GXB RX L5n,GXB REFCLK L5n					C1				
GXB_L1		GXB_TX_L4n					E1				
GXB_L1		GXB_TX_L4p					E2				
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2				
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					G1				
GXB_L1 GXB_L1		GXB_TX_L3n GXB_TX_L3p					J1 J2				
GXB_L1		GXB_TX_L3p GXB_RX_L3p,GXB_REFCLK_L3p					L2				
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					L1				
GXB_L0		GXB_TX_L2n					N1				
GXB_L0		GXB_TX_L2p					N2				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					R2				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R1				
GXB_L0 GXB L0	-	GXB_TX_L1n GXB_TX_L1p			-		U1				-
GXB_L0 GXB_L0	 	GXB_IX_L1p GXB_RX_L1p,GXB_REFCLK_L1p			1		W2	1	1	1	
GXB_L0	 	GXB_RX_L1p,GXB_REFCLK_L1p	<u> </u>		+		W1	+	+	<u> </u>	
GXB_L0	İ	GXB_TX_L0n					Y3				İ
GXB_L0		GXB_TX_L0p					Y4				İ
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AA2				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AA1				
GXB_L0		REFCLK0Lp					V4				
GXB_L0 3A		REFCLK0Ln		TDO			U4				
3A 3A		TDO nCSO		TDO DATA4			M5 R4				
3A		TMS		TMS			P5				
3A		AS DATA3		DATA3			T4				
3A		TCK		TCK			V5				
3A		AS_DATA2		DATA2			AA5				
3A		TDI		TDI			W5				
3A		AS_DATA1		DATA1			AB3				
3A 3A		DCLK AS_DATA0,ASDO		DCLK DATA0			V3 AB4				
3A	VREFB3AN0	AS_DATAU,ASDO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	R6	DQ1B			
3A	VREFB3AN0	10		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7	DQIB			
3A	VREFB3AN0			DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	R5	DQ1B			
3A	VREFB3AN0	10		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U8	DQ1B			
3A	VREFB3AN0	10		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	P6	DQSn1B			
3A		10		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	W8	DQ1B			
3A	VREFB3AN0			DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	N6	DQS1B			
3A 3A	VREFB3AN0 VREFB3AN0	10		DATA11 DATA14	DIFFIO_TX_B4p DIFFIO_RX_B5n	DIFFOUT_B4p DIFFOUT_B5n	W9 T7	DQ1B			
3A	VREFB3AN0	10		DATA14 DATA13	DIFFIO_RX_B5n DIFFIO_TX_B6n	DIFFOUT_B5n	17 U6	DQ1B			
3A	VREFB3AN0	10		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T8	DQ1B			
3A		10		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V6	DQ1B			İ
3A	VREFB3AN0			PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	M6				
3A	VREFB3AN0	10		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	R7	DQ1B			
3A	VREFB3AN0	10		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	M7				
3A	VREFB3AN0	10			DIFFIO_TX_B8p	DIFFOUT_B8p	P7	DQ1B		OND	OND
3B 3B	VREFB3BN0 VREFB3BN0		<u> </u>		DIFFIO_TX_B9n DIFFIO_RX_B10n	DIFFOUT_B9n DIFFOUT_B10n	AB6 V9	DOOR	1	GND B A 15	GND
3B 3B		10			DIFFIO_RX_B10n DIFFIO_TX_B9p	DIFFOUT_B10n	AB5	DQ2B DQ2B		B_A_15 B_WE#	
3B		10	<u> </u>		DIFFIO_TX_B9p	DIFFOUT_B10p	V10	DQ2B DQ2B	1	B_A_14	†
3B	VREFB3BN0	10			DIFFIO_RX_B11n	DIFFOUT_B11n	P8	DQSn2B		B_CS#_1	B_CS#_1
3B	VREFB3BN0	10			DIFFIO_TX_B12n	DIFFOUT_B12n	AA7	DQ2B		B_A_13	
3B	VREFB3BN0				DIFFIO_RX_B11p	DIFFOUT_B11p	N8	DQS2B		B_CS#_0	B_CS#_0
3B	VREFB3BN0	10			DIFFIO_TX_B12p	DIFFOUT_B12p	AB7			B_A_12	
3B	VREFB3BN0	10			DIFFIO_TX_B13n	DIFFOUT_B13n	AA8	DQ2B	ļ	B_A_11	D 04 0
3B	VREFB3BN0	10			DIFFIO_RX_B14n DIFFIO_TX_B13p	DIFFOUT_B14n	T9	DQ2B		B_A_9 B A 10	B_CA_9
3B 3B	VREFB3BN0 VREFB3BN0	10		1	DIFFIO_TX_B13p DIFFIO_RX_B14p	DIFFOUT_B13p DIFFOUT_B14p	AB8 U10	DQ2B DQ2B	1	B_A_10 B A 8	B CA 8
3B 3B	VREFB3BN0 VREFB3BN0		CLK0n,FPLL_BL_FBn		DIFFIO_RX_B14p	DIFFOUT_B14p	M8	DWZD		D_A_0	D_CA_0
3B		10	02.101q1 1 22_02_1 bil		DIFFIO_TX_B16n	DIFFOUT_B16n	AA10	DQ2B		B_RAS#	
3B	VREFB3BN0	10	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	M9	1	1		İ
3B	VREFB3BN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AA9	DQ2B		B_CAS#	
3B		10			DIFFIO_TX_B17n	DIFFOUT_B17n	Y10			GND	GND
3B	VREFB3BN0		1		DIFFIO_RX_B18n	DIFFOUT_B18n	T10	DQ3B		B_BA_2	



	luner.	Territoria	I= 0 1= 0 1)	Ia a	Ta	Te	le se :	Inaa /		luna n	Note (1)
ank umber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
B	VREFB3BN0	10			DIFFIO_TX_B17p	DIFFOUT_B17p	Y9	DQ3B		B_BA_0	
3	VREFB3BN0 VREFB3BN0	10			DIFFIO_RX_B18p	DIFFOUT_B18p	R9 U11	DQ3B	_	B_BA_1	B CK#
		lio			DIFFIO_RX_B19n	DIFFOUT_B19n	U11 R12	DQSn3B		B_CK#	B_CK# B_CA_7
3	VREFB3BN0 VREFB3BN0	lio		+	DIFFIO_TX_B20n DIFFIO_RX_B19p	DIFFOUT_B20n DIFFOUT_B19p	U12	DQ3B DQS3B	+	B_A_7 B_CK	B_CK_/
3	VREFB3BN0	in			DIFFIO_TX_B20p	DIFFOUT_B20p	P12	DQSSB		B A 6	B CA 6
3	VREFB3BN0	10	FPLL BL CLKOUT1,FPLL BL CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB10	DQ3B		B A 3	B CA 3
B	VREFB3BN0	10			DIFFIO RX B22n	DIFFOUT_B22n	R10	DQ3B		B A 5	B CA 5
В		10	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AB11	DQ3B		B_A_2	B_CA_2
В		10			DIFFIO_RX_B22p	DIFFOUT_B22p	R11	DQ3B		B_A_4	B_CA_4
В	VREFB3BN0	10	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	P9				1
В	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	Y11	DQ3B		B_A_1	B_CA_1
B	VREFB3BN0	10	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	N9				
B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AA12	DQ3B		B_A_0	B_CA_0
A A		10	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AB13	DQ4B		B DQ 0	B DQ 0
ıΔ	VREFB4AN0 VREFB4AN0	10			DIFFIO_RX_B26n DIFFIO_TX_B25p	DIFFOUT_B26n DIFFOUT_B25p	V13 AB12	DQ4B DQ4B		B_DQ_0 B DQ 2	B_DQ_0 B DQ 2
A A	VREFB4AN0	lio		+	DIFFIO_IX_B25p	DIFFOUT B26p	U13	DQ4B DQ4B	+	B_DQ_2 B DQ 1	B_DQ_2 B DQ 1
IA		lio		+	DIFFIO_RX_B26p DIFFIO_RX_B27n	DIFFOUT B27n	T12	DQSn4B	+	B_DQ_1 B_DQS#_0	B_DQ_1 B_DQS#_0
A	VREFB4AN0			+	DIFFIO_TX_B28n	DIFFOUT_B28n	AA14	DQ3H4B DQ4B	+	B DQ 3	B_DQ3#_0 B DQ 3
IA		10			DIFFIO RX B27p	DIFFOUT_B27p	T13	DQS4B		B_DQS_0	B_DQS_0
IA		10			DIFFIO_TX_B28p	DIFFOUT_B28p	AA13	540.5		B_ODT_0	B_ODT_0
IA.		10			DIFFIO_TX_B29n	DIFFOUT_B29n	AB15	DQ4B		B ODT 1	B ODT 1
IA.	VREFB4AN0	10			DIFFIO_RX_B30n	DIFFOUT_B30n	Y14	DQ4B		B_DQ_4	B_DQ_4
IA.	VREFB4AN0	10			DIFFIO_TX_B29p	DIFFOUT_B29p	AA15	DQ4B		B_DQ_6	B_DQ_6
IA.		IO			DIFFIO_RX_B30p	DIFFOUT_B30p	Y15	DQ4B		B_DQ_5	B_DQ_5
IA.	VREFB4AN0	10	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	V14				
A	VREFB4AN0	10			DIFFIO_TX_B32n	DIFFOUT_B32n	AB17	DQ4B		B_DQ_7	B_DQ_7
IA.	VREFB4AN0	10	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	V15				
A	VREFB4AN0	10			DIFFIO_TX_B32p	DIFFOUT_B32p	AB18	DQ4B		B_DM_0	B_DM_0
1A 1A	VREFB4AN0 VRFFB4AN0	lio			DIFFIO_TX_B33n	DIFFOUT_B33n	AB20	DOED	DO4D	GND	GND B DO 0
1A	VREFB4AN0 VREFB4AN0	lio		+	DIFFIO_RX_B34n DIFFIO_TX_B33p	DIFFOUT_B34n DIFFOUT_B33p	Y16 AB21	DQ5B DQ5B	DQ1B DQ1B	B_DQ_8 B_DQ_10	B_DQ_8 B_DQ_10
1A	VREFB4AN0	in			DIFFIO_TX_B33p	DIFFOUT B34p	Y17	DQ5B	DQ1B	B DQ 9	B_DQ_10
4A	VREFB4AN0	in			DIFFIO RX B35n	DIFFOUT_B35n	T14	DQSn5B	DQ1B	B DQS# 1	B DQS# 1
1A		10			DIFFIO_TX_B36n	DIFFOUT_B36n	AA17	DQ5B	DQ1B	B DQ 11	B DQ 11
4A		10			DIFFIO_RX_B35p	DIFFOUT_B35p	U15	DQS5B	DQ1B	B_DQS_1	B_DQS_1
4A	VREFB4AN0	10			DIFFIO_TX_B36p	DIFFOUT_B36p	AA18			B CKE 1	B CKE 1
1A	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA19	DQ5B	DQ1B	B_CKE_0	B_CKE_0
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	V20	DQ5B	DQ1B	B_DQ_12	B_DQ_12
1A		10			DIFFIO_TX_B37p	DIFFOUT_B37p	AA20	DQ5B	DQ1B	B_DQ_14	B_DQ_14
1A	VREFB4AN0				DIFFIO_RX_B38p	DIFFOUT_B38p	W19	DQ5B	DQ1B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	10	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	V16				2.20.12
4A		10	0116		DIFFIO_TX_B40n	DIFFOUT_B40n	AB22	DQ5B	DQ1B	B_DQ_15	B_DQ_15
1A	VREFB4AN0 VREFB4AN0	10	CLK3p		DIFFIO_RX_B39p DIFFIO_TX_B40p	DIFFOUT_B39p DIFFOUT_B40p	W16 AA22	DQ5B	DQ1B	B DM 1	B DM 1
1A		lio		+	DIFFIO_TX_B40p	DIFFOUT_B40p DIFFOUT_B41n	Y22	DQ5B	DQ1B	GND	GND
1Δ	VREFB4AN0	10		+	DIFFIO_TX_B4111 DIFFIO_RX_B42n	DIFFOUT_B41II	Y20	DQ6B	DQ1B	B_DQ_16	B_DQ_16
IA	VREFB4AN0	lio		+	DIFFIO_TX_B41p	DIFFOUT_B41p	W22	DQ6B	DQ1B	B_DQ_18	B_DQ_18
IA	VREFB4AN0	IO		1	DIFFIO_TX_B41p	DIFFOUT_B41p	Y19	DQ6B	DQ1B	B DQ 17	B_DQ_18
IA	VREFB4AN0	IO		1	DIFFIO_RX_B43n	DIFFOUT_B43n	P14	DQSn6B	DQSn1B	B_DQS#_2	B_DQS#_2
IA.		10			DIFFIO_TX_B44n	DIFFOUT_B44n	Y21	DQ6B	DQ1B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	R14	DQS6B	DQS1B	B_DQS_2	B_DQS_2
IA.	VREFB4AN0	Ю			DIFFIO_TX_B44p	DIFFOUT_B44p	W21			B_RESET#	B_RESET#
IA.	VREFB4AN0	Ю			DIFFIO_TX_B45n	DIFFOUT_B45n	U22	DQ6B	DQ1B	GND	GND
IA.	VREFB4AN0	10			DIFFIO_RX_B46n	DIFFOUT_B46n	V19	DQ6B	DQ1B	B_DQ_20	B_DQ_20
1A	VREFB4AN0	10			DIFFIO_TX_B45p	DIFFOUT_B45p	V21	DQ6B	DQ1B	B_DQ_22	B_DQ_22
IA.		10		+	DIFFIO_RX_B46p	DIFFOUT_B46p	V18	DQ6B	DQ1B	B_DQ_21	B_DQ_21
A A	VREFB4AN0	10		+	DIFFIO_RX_B47n DIFFIO_TX_B48n	DIFFOUT_B47n DIFFOUT_B48n	U16 U21	DQ6B	DQ1B	GND B DQ 23	GND B DQ 23
A A	VREFB4AN0 VREFB4AN0	lo		+	DIFFIO_TX_B48n DIFFIO_RX_B47p	DIFFOUT_B48n DIFFOUT_B47p	U21 U17	DQ6B	DQ1B	B_DQ_23 GND	B_DQ_23 GND
IA	VREFB4AN0 VREFB4AN0	lio		+	DIFFIO_RX_B47p	DIFFOUT_B48p	U20	DQ6B	DQ1B	B DM 2	B DM 2
SA SA	VREFB5AN0		RZQ_1	+	DIFFIO_TX_B46p	DIFFOUT_B48p DIFFOUT_R1p	T19	DQ1R	DOLID	D_DIVI_Z	ID_DIVI_Z
5A	VREFB5AN0		INEQ_1	INIT_DONE	DIFFIO_TX_R1p	DIFFOUT_R2p	T18	DAIN	+	+	+
SA .	VREFB5AN0	10		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT R1n	T20	DQ1R	+	1	+
5A	VREFB5AN0	10		CRC_ERROR	DIFFIO RX R2n	DIFFOUT_R2n	T17				1
5A	VREFB5AN0	10		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T22	DQ1R			
iA	VREFB5AN0	10			DIFFIO_RX_R4p	DIFFOUT_R4p	T15	DQ1R			1
iA	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	R22	DQ1R			
iΑ	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	R15	DQ1R			
iA	VREFB5AN0	10		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	R21				
A	VREFB5AN0	10			DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R			
5A 5A		10		DEV_OE		DIFFOUT_R5p DIFFOUT_R6p	11,2	DQS1R		_	



		In	Outland Emelor(s)								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	P22	DQ1R			
5A		IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R			
5A 5A		10			DIFFIO_TX_R7p DIFFIO_RX_R8p	DIFFOUT_R7p DIFFOUT_R8p	P19	DQ1R DQ1R			
5A 5A	VREFB5AN0 VREFB5AN0	io			DIFFIO_RX_R8p DIFFIO_TX_R7n	DIFFOUT_R7n	P16	DQ1R			
5A	VREFB5AN0	IO .			DIFFIO_TX_R/II	DIFFOUT_R8n	P17	DQ1R			+
5B		10	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	N16	Dani			
5B		IO	,		DIFFIO_TX_R18p	DIFFOUT_R18p	N20	DQ2R			
5B	VREFB5BN0	10	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	M16				
5B	VREFB5BN0	10			DIFFIO_TX_R18n	DIFFOUT_R18n	N21	DQ2R			
5B 5B	VREFB5BN0 VREFB5BN0	10	FPLL BR CLKOUT0,FPLL BR CLKOUTp,FPLL BR FB		DIFFIO_RX_R19p DIFFIO_TX_R20p	DIFFOUT_R19p DIFFOUT_R20p	N19 M22	DQ2R DQ2R			
5B		10	FPLL_BR_CLROUTU,FPLL_BR_CLROUTP,FPLL_BR_FB		DIFFIO_TX_R20p DIFFIO_RX_R19n	DIFFOUT R19n	M18	DQ2R DQ2R			
5B		10	FPLL BR CLKOUT1,FPLL BR CLKOUTn		DIFFIO_TX_R20n	DIFFOUT_R20n	L22	DQ2R			+
5B		10			DIFFIO_RX_R21p	DIFFOUT_R21p	K17	DQS2R			1
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	M20				
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	L17	DQSn2R			
5B	VREFB5BN0				DIFFIO_TX_R22n	DIFFOUT_R22n	M21	DQ2R			
5B	VREFB5BN0 VREFB5BN0	10		 	DIFFIO_RX_R23p DIFFIO_TX_R24p	DIFFOUT_R23p DIFFOUT_R24p	L19 K21	DQ2R DQ2R	1	+	
5B	VREFB5BN0 VREFB5BN0	10		+	DIFFIO_TX_R24p DIFFIO_RX_R23n	DIFFOUT_R24p DIFFOUT_R23n	K21 L18	DQ2R DQ2R	+	+	+
5B 5B		IO IO		1	DIFFIO_RX_R23n DIFFIO_TX_R24n	DIFFOUT_R23n DIFFOUT_R24n	K22	DWZK	+	+	+
7A	TALL BODING	GND		1	5 10_17_1\2 4 11	5 GGT_1(2-1)	F17	1		1	
7A	VREFB7AN0	10			DIFFIO_RX_T1p	DIFFOUT_T1p	H21			GND	GND
7A	VREFB7AN0	10			DIFFIO_TX_T2p	DIFFOUT_T2p	E21	DQ1T	DQ1T	T_DM_4	T_DM_4
7A		IO			DIFFIO_RX_T1n	DIFFOUT_T1n	G21			GND	GND
7A		IO			DIFFIO_TX_T2n	DIFFOUT_T2n	D21	DQ1T	DQ1T	T_DQ_39	T_DQ_39
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	E19	DQ1T	DQ1T	T_DQ_37	T_DQ_37
7A	VREFB7AN0				DIFFIO_TX_T4p	DIFFOUT_T4p	C20	DQ1T	DQ1T	T_DQ_38	T_DQ_38
7A 7A		10			DIFFIO_RX_T3n	DIFFOUT_T3n	D19 B20	DQ1T DQ1T	DQ1T DQ1T	T_DQ_36 GND	T_DQ_36 GND
7A 7A		IO IO			DIFFIO_TX_T4n	DIFFOUT T5p	J21	DQ11 DQS1T	DQ11	T DQS 4	T DQS 4
7A		10			DIFFIO TX T6p	DIFFOUT T6p	B18	DQ311	DQSTI	GND	GND
7A	VREFB7AN0				DIFFIO_RX_T5n	DIFFOUT_T5n	J22	DQSn1T	DQSn1T	T DQS# 4	T DQS# 4
7A	VREFB7AN0				DIFFIO_TX_T6n	DIFFOUT_T6n	B17	DQ1T	DQ1T	T DQ 35	T DQ 35
7A	VILLI DITTIO	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	C21	DQ1T	DQ1T	T_DQ_33	T_DQ_33
7A	VREFB7AN0	IO			DIFFIO_TX_T8p	DIFFOUT_T8p	G22	DQ1T	DQ1T	T_DQ_34	T_DQ_34
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	B21	DQ1T	DQ1T	T_DQ_32	T_DQ_32
7A		IO			DIFFIO_TX_T8n	DIFFOUT_T8n	F22			GND	GND
7A 7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T9p DIFFIO_TX_T10p	DIFFOUT_T9p DIFFOUT_T10p	G20 F22	DQ2T	DQ1T	GND T DM 3	GND T DM 3
7A	VREFB7AN0	IO .			DIFFIO_TX_T10p	DIFFOUT T9n	H20	DQZI	DQTI	GND	GND
7A	VREFB7AN0	IO .			DIFFIO TX T10n	DIFFOUT T10n	D22	DQ2T	DQ1T	T DQ 31	T DQ 31
7A		10			DIFFIO_RX_T11p	DIFFOUT_T11p	C19	DQ2T	DQ1T	T_DQ_29	T_DQ_29
7A	VREFB7AN0	10			DIFFIO_TX_T12p	DIFFOUT_T12p	B22	DQ2T	DQ1T	T_DQ_30	T_DQ_30
7A		IO			DIFFIO_RX_T11n	DIFFOUT_T11n	C18	DQ2T	DQ1T	T_DQ_28	T_DQ_28
7A		IO			DIFFIO_TX_T12n	DIFFOUT_T12n	A22	DQ2T	DQ1T	GND	GND
7A	VREFB7AN0	10		1	DIFFIO_RX_T13p	DIFFOUT_T13p	F19	DQS2T	DQ1T	T_DQS_3	T_DQS_3
7A	VILLI DITTIO	10		 	DIFFIO_TX_T14p	DIFFOUT_T14p	E20	DOC=2T	DO4T	GND T DOS# 3	GND T DOS# 3
7A		10		 	DIFFIO_RX_T13n DIFFIO_TX_T14n	DIFFOUT_T13n DIFFOUT_T14n	F18 F20	DQSn2T DQ2T	DQ1T DQ1T	T_DQS#_3 T_DQ_27	T_DQS#_3 T_DQ_27
7A		IO IO		†	DIFFIO_TX_T14n DIFFIO_RX_T15p	DIFFOUT_T15p	A18	DQ2T	DQ1T	T_DQ_25	T_DQ_27
7A		10		1	DIFFIO_TX_T16p	DIFFOUT_T16p	A20	DQ2T	DQ1T	T DQ 26	T DQ 26
7A	VREFB7AN0	10			DIFFIO_RX_T15n	DIFFOUT_T15n	A17	DQ2T	DQ1T	T_DQ_24	T_DQ_24
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A19			GND	GND
7A	VREFB7AN0				DIFFIO_RX_T17p	DIFFOUT_T17p	K20			GND	GND
7A		IO			DIFFIO_TX_T18p	DIFFOUT_T18p	B16	DQ3T	DQ2T	T_DM_2	T_DM_2
7A		IO .			DIFFIO_RX_T17n	DIFFOUT_T17n	K19	2007	2007	GND	GND
7A	VREFB7ANO	10		-	DIFFIO_TX_T18n	DIFFOUT_T18n	C16	DQ3T	DQ2T DQ2T	T_DQ_23 T_DQ_21	T_DQ_23 T_DQ_21
7A 7A	VREFB7AN0 VREFB7AN0	IO		+	DIFFIO_RX_T19p DIFFIO_TX_T20p	DIFFOUT_T19p DIFFOUT_T20p	D17 G17	DQ3T DQ3T	DQ2T DQ2T	T DQ 22	T_DQ_21 T_DQ_22
7A		10		+	DIFFIO_TX_T20p	DIFFOUT_T19n	E16	DQ3T	DQ2T DQ2T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	10		1	DIFFIO_TX_T20n	DIFFOUT_T20n	G16	DQ3T	DQ2T	GND	GND
7A	VREFB7AN0	10		İ	DIFFIO_RX_T21p	DIFFOUT_T21p	G18	DQS3T	DQS2T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	J19			T_RESET#	T_RESET#
7A		IO			DIFFIO_RX_T21n	DIFFOUT_T21n	H18	DQSn3T	DQSn2T	T_DQS#_2	T_DQS#_2
7A		10			DIFFIO_TX_T22n	DIFFOUT_T22n	J18	DQ3T	DQ2T	T_DQ_19	T_DQ_19
7A		10			DIFFIO_RX_T23p	DIFFOUT_T23p	E15	DQ3T	DQ2T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	10			DIFFIO_TX_T24p	DIFFOUT_T24p	A15	DQ3T	DQ2T	T_DQ_18	T_DQ_18
7A	VREFB7AN0 VREFB7AN0	10		-	DIFFIO_RX_T23n DIFFIO_TX_T24n	DIFFOUT_T23n DIFFOUT_T24n	F15 A14	DQ3T	DQ2T	T_DQ_16 GND	T_DQ_16 GND
7A 7A	VREFB7AN0 VREFB7AN0	10	CLK11p	+	DIFFIO_IX_124n DIFFIO_RX_T25p	DIFFOUT_T25p	H16	1	1	GIND	OIND
/A	VKEFB/ANU	JIO .	CENTIP	1	DIFFIO_KX_125P	DIFFOUI_125P	IU10	į.	l .	, i	1



	1		1	1	r	T			1	1	Note (1
ank umber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		T								T 514 4	
	VREFB7AN0 VREFB7AN0	10	CLK11n		DIFFIO_TX_T26p DIFFIO_RX_T25n	DIFFOUT_T26p DIFFOUT_T25n	J17 H15	DQ4T	DQ2T	T_DM_1	T_DM_1
	VREFB7AN0 VREFB7AN0	10	CERTIN		DIFFIO_RX_125n	DIFFOUT_T26n	K16	DQ4T	DQ2T	T DQ 15	T DQ 15
	VREFB7AN0	io			DIFFIO_RX_T27p	DIFFOUT_T27p	C15	DQ4T	DQ2T	T_DQ_13	T_DQ_13
	VREFB7AN0	10			DIFFIO_TX_T28p	DIFFOUT_T28p	G15	DQ4T	DQ2T	T_DQ_14	T_DQ_14
	VREFB7AN0	10			DIFFIO_RX_T27n	DIFFOUT_T27n	B15	DQ4T	DQ2T	T_DQ_12	T_DQ_12
	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	F14	DQ4T	DQ2T	T_CKE_0	T_CKE_0
١	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	H14	DQS4T	DQ2T	T_DQS_1	T_DQS_1
	VREFB7AN0				DIFFIO_TX_T30p	DIFFOUT_T30p	B13			T_CKE_1	T_CKE_1
١	VREFB7AN0	•			DIFFIO_RX_T29n	DIFFOUT_T29n	J13	DQSn4T	DQ2T	T_DQS#_1	T_DQS#_1
١	VREFB7AN0	10			DIFFIO_TX_T30n	DIFFOUT_T30n	A13	DQ4T	DQ2T	T_DQ_11	T_DQ_11
	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T31p DIFFIO_TX_T32p	DIFFOUT_T31p DIFFOUT_T32p	E14 J11	DQ4T DQ4T	DQ2T DQ2T	T_DQ_9 T_DQ_10	T_DQ_9 T_DQ_10
	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T31n	F13	DQ4T	DQ2T	T_DQ_10	T_DQ_10
`		IO IO			DIFFIO_RX_T3TII	DIFFOUT_T32n	H10	DQ41	DQZI	GND	GND
		10	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H13			OND	CIND
	VREFB7AN0	10			DIFFIO TX T34p	DIFFOUT T34p	G11	DQ5T		T DM 0	T DM 0
١	VREFB7AN0	10	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G13				
١		IO			DIFFIO_TX_T34n	DIFFOUT_T34n	F12	DQ5T		T_DQ_7	T_DQ_7
1	VREFB7AN0				DIFFIO_RX_T35p	DIFFOUT_T35p	D13	DQ5T		T_DQ_5	T_DQ_5
١	VREFB7AN0				DIFFIO_TX_T36p	DIFFOUT_T36p	B12	DQ5T		T_DQ_6	T_DQ_6
4		IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C13	DQ5T		T_DQ_4	T_DQ_4
\ \		10		1	DIFFIO_TX_T36n	DIFFOUT_T36n	A12	DQ5T		T_ODT_1	T_ODT_1
<u> </u>	VREFB7AN0	10			DIFFIO_RX_T37p	DIFFOUT_T37p	H11	DQS5T		T_DQS_0	T_DQS_0
١		10			DIFFIO_TX_T38p	DIFFOUT_T38p	L8	DOG-FT		T_ODT_0 T DQS# 0	T_ODT_0
\	VREFB7AN0 VREFB7AN0	io			DIFFIO_RX_T37n DIFFIO_TX_T38n	DIFFOUT_T37n DIFFOUT_T38n	G12 K9	DQSn5T DQ5T		T_DQ.3	T_DQS#_0 T_DQ_3
	VREFB7AN0	in			DIFFIO_TX_T38II	DIFFOUT T39p	D12	DQ5T		T DQ 1	T DQ 1
	VREFB7AN0	in .			DIFFIO TX T40p	DIFFOUT T40p	C11	DQ5T		T DQ 2	T DQ 2
	VREFB7AN0	10			DIFFIO RX T39n	DIFFOUT_T39n	E12	DQ5T		T_DQ_0	T DQ 0
		10	RZQ 2		DIFFIO_TX_T40n	DIFFOUT_T40n	B11				1
١	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	G10				
١	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	L7	DQ6T		T_A_0	T_CA_0
١	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	F10				
4	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	K7	DQ6T		T_A_1	T_CA_1
١.		IO			DIFFIO_RX_T43p	DIFFOUT_T43p	J7	DQ6T		T_A_4	T_CA_4
<u> </u>	VIILI DOVIIIO	10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	H8	DQ6T		T_A_2	T_CA_2
	VREFB8AN0 VREFB8AN0	10	FPLL TL CLKOUT1,FPLL TL CLKOUTn		DIFFIO_RX_T43n DIFFIO_TX_T44n	DIFFOUT_T43n DIFFOUT_T44n	J8 G8	DQ6T DQ6T		T_A_5 T A 3	T_CA_5 T_CA_3
<u>, </u>	VREFB8AN0	io	FPLL_IL_CLROUTI,FPLL_IL_CLROUTII		DIFFIO_TX_T44II	DIFFOUT_T45p	.19	DQS6T		T CK	T CK
\ \		10			DIFFIO_TX_T46p	DIFFOUT_T46p	A10	DQS01		T A 6	T CA 6
<u>, </u>	VREFB8AN0				DIFFIO RX T45n	DIFFOUT_T45n	H9	DQSn6T		T CK#	T CK#
4	VREFB8AN0	10			DIFFIO_TX_T46n	DIFFOUT_T46n	A9	DQ6T		T_A_7	T CA 7
4		10			DIFFIO_RX_T47p	DIFFOUT_T47p	B10	DQ6T		T_BA_1	
1	VREFB8AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	A5	DQ6T		T_BA_0	
١	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	C9	DQ6T		T_BA_2	
١.		Ю			DIFFIO_TX_T48n	DIFFOUT_T48n	B5			GND	GND
\	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	E10				
	VREFB8AN0	IO	OLIVA EDILL TIL ED	1	DIFFIO_TX_T50p	DIFFOUT_T50p	B6	DQ7T		T_CAS#	4
<u> </u>	VREFB8AN0	10	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	F9	DOTT	-	T DAC#	+
	VREFB8AN0 VREFB8AN0	10	+	+	DIFFIO_TX_T50n DIFFIO_RX_T51p	DIFFOUT_T50n DIFFOUT_T51p	B7 A8	DQ7T DQ7T	-	T_RAS# T A 8	T CA 8
		10									I_CA_8
	VREFB8AN0 VREFB8AN0	IO IO	1	+	DIFFIO_TX_T52p DIFFIO_RX_T51n	DIFFOUT_T52p DIFFOUT_T51n	C6 A7	DQ7T DQ7T	+	T_A_10 T_A_9	T CA 9
	VREFB8AN0	IO IO	 	1	DIFFIO_TX_T52n	DIFFOUT T52n	D6	DQ7T		T A 11	0/_3
	VREFB8AN0	10		1	DIFFIO_TX_T52ff	DIFFOUT_T53p	E9	DQS7T	Ì	T CS# 0	T CS# 0
	VREFB8AN0	10			DIFFIO_TX_T54p	DIFFOUT_T54p	D7			T A 12	1
		10			DIFFIO_RX_T53n	DIFFOUT_T53n	D9	DQSn7T		T_CS#_1	T_CS#_1
	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	C8	DQ7T		T_A_13	
	VREFB8AN0	10			DIFFIO_RX_T55p	DIFFOUT_T55p	G6	DQ7T		T_A_14	
	VREFB8AN0	10			DIFFIO_TX_T56p	DIFFOUT_T56p	F7	DQ7T		T_WE#	
١	VREFB8AN0	10			DIFFIO_RX_T55n	DIFFOUT_T55n	H6	DQ7T		T_A_15	1
١	VREFB8AN0	IO .		LIOSI A	DIFFIO_TX_T56n	DIFFOUT_T56n	E7	ļ		GND	GND
١	1	MSEL0		MSEL0			L6				4
١	+	CONF_DONE		CONF_DONE			K6	 	+	+	+
\ \	1	MSEL1 nSTATUS	+	MSEL1 nSTATUS	-		J6 H5	 		+	+
	1	nCF	+		-		G5	 		+	+
4	†	MSEL2		nCE MSEL2			A2	†	+	+	+
<u> </u>	†	MSEL3		MSFL3			F5	†		+	+
4	1	nCONFIG		nCONFIG			A4				1
Α	1	MSEL4		MSEL4	1		F3	1	1	1	1
							1. 0				



Bank Number	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for	HMC Pin Assignment for
Number									Assignment for	Assignment for
9A										
9A									DDR3/DDR2 (2)	LPDDR2
9A										
9A										
	GND					C5				
	GND					AB19				
	GND					AB14				
	GND					AB9				
	GND					AB2				
	GND					AB1				
	GND					AA11				
	GND					AA6				
	GND					AA4				
	GND					AA3				
	GND					Y18				
	GND					Y5				
	GND					Y2				
	GND					Y1				
	GND					W4				
	GND					W3				
	GND					V22				
	GND					V17				
	GND					V12				
	GND					V7				
	GND					V2				
	GND					V1				
	GND					U9				
	GND					U5				
	GND					U3				
	GND					T21				
	GND					T16				
	GND					T2				
	GND					T1				
	GND					R13				
	GND					R3				
	GND					P10				
	GND					P4				
	GND					P2				
	GND		İ			P1				
	GND		İ			N22				1
	GND					N17				
	GND		İ			N15				1
	GND					N13				
	GND		İ			N11				
	GND		İ			N7				1
	GND					N5				
	GND					N3				
	GND					M14				
	GND					M12				
	GND					M10				
1	GND					M4				1
	GND		1	†		M2	1	†	1	1
	GND		1	†		M1	1	†	1	1
1	GND					L21				1
t	GND		1	†		L15	1	t	†	†
t	GND		1	†		L13	1	t	†	†
+	GND		1	†		L11	1	t	†	†
1	GND					L5				1
-	GND			 	İ	L3		 		
+	GND		 	†	1	K14	 	† 	 	
	GND	<u> </u>		†	 	K12		 		
t	GND	<u> </u>		t	1	K12		t		
+	GND			t		K8		t		
t	GND	<u> </u>		t	1	K8		t		
+	GND	 	-	 		K4 K2	1	+	1	
-	GND	 		 		K2 K1	1	 	1	
t	GND	<u> </u>		t	1	J20		t		
+	GND	 	-	 		J20 J15	1	+	1	+
	GND			 		J15 J5		 		
+	GND			-		J5 J3			-	
-		 	-	 	1			 	-	
	GND			 		H22	-	 		
	GND			 		H12		 		
	GND			-		H7				
	GND			 		H4		 		
	GND			 		H3		 		
	GND	<u>l</u>	l	I	<u> </u>	H2	l	1	l	



Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tv/Dv	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin	HMC Pin
Number	VKEF	Fin Name/Function	Optional Function(s)	Configuration Function	Channel	Emulated LVDS Output Channel	F404	DQS IOI AO	DQS IOI X IO	Assignment for	Assignment for
Number					Channel					DDR3/DDR2 (2)	LPDDR2
										DDR3/DDR2 (2)	LPDDR2
	<u> </u>										+
		GND					H1				
		GND					G19				
		GND					G9				
		GND					G3				
		GND					F16				
		GND					F6				
		GND					F2				
		GND					F1				
		GND					E13				
	1	GND		t			E4				+
	1	GND		-							+
	ļ	GND					E3				+
		GND					D20				
		GND					D10				
		GND					D5				
		GND					D2				
		GND					D1				
		GND					C17				
		GND					C4				
	İ	GND		Ì	İ		C3		Ì	İ	1
	1	GND		1	1		B14	Ì	1	1	1
	 	GND	<u> </u>	 	 	1	B9	<u> </u>	†	†	+
	 			-	-			1	-	 	+
	1	GND			-		B2		 	 	+
	1	GND	1	+	1	 	B1	1	1	1	+
	ļ	GND				1	A21	ļ	<u> </u>	1	4
		GND					A11				
		VCC					P15				
		VCC					P13				
		VCC					P11				
		VCC					N14				
		VCC					N12				
	1	VCC					N10				+
	1	VCC		t			M15				+
	1	VCC		-			M13				+
	1			-							+
		VCC					M11				
		VCC					L16				
		VCC					L14				
		VCC					L12				
		VCC					L10				
		VCC					K15				
		VCC					K13				1
		VCC					K11				1
		vcc					J16				
	1	VCC					J14				+
	1	VCC		†		1	J12				+
	ļ										
		VCC					J10				
	ļ	DNU	ļ			ļ	B3	ļ			
	1	DNU		ļ	ļ		B4	ļ	1	1	1
	1	DNU		ļ			E17		1	1	1
		DNU					L9				
	1	VCCPGM	1				V8				
		VCCPGM					R19				
	Ì	VCCPGM					F8				1
	1	VCCBAT		1	1		A3	Ì	1	1	1
	1	VCCIO3A	1				T6	1	1	1	+
	1	VCCIO3A VCCIO3A	+	 	 		Y8	†	+	+	+
	1				-				 	 	+
	 	VCCIO3B	+	 	 	1	Y13	1	+	+	+
	ļ	VCCIO3B					W10				
	1	VCCIO3B		ļ	ļ		T11		1	1	1
	1	VCCIO3B		ļ			R8		1	1	1
		VCCIO4A					U19				
	1	VCCIO4A	1				AA21				
		VCCIO4A					AA16				
	T .	VCCIO4A		İ	İ		W20	İ	Ì	1	1
	l	VCCIO4A			<u> </u>		W15		1	1	—
	1	VCCIO4A VCCIO4A	†	 	 	1	U14	1	1	1	+
	1	VCCIO4A VCCIO5A		+	 		R18	1	+	+	+
	 	VOCIOSA		 	 		K18		 	+	+
	ļ	VCCIO5A				1	P20	ļ	<u> </u>	1	4
	ļ	VCCIO5B			ļ		M19		1	1	4
		VCCIO5B					K18				
		VCCIO7A					B19				
		VCCIO7A					H17				
		VCCIO7A					G14				1



Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin	HMC Pin
Number				•	Channel					Assignment for	Assignment for LPDDR2
										22NG/22N2 (2)	2. 55.12
		VCCIO7A					F21				
		VCCIO7A VCCIO7A		+		1	F11				
		VCCIO7A					E18				1
		VCCIO7A					D15				1
		VCCIO7A					C22				
		VCCIO7A		1			C12				
		VCCIO7A		1			A16				
		VCCIO8A		1			A6				
		VCCIO8A		Ť		İ	G7				
		VCCIO8A		Ť		İ	E8				
		VCCIO8A		Ť		İ	C7				
		VCCPD3A					W6				
		VCCPD3B4A					W17				
		VCCPD3B4A					W14				
		VCCPD3B4A					W12				
		VCCPD3B4A					W11				
		VCCPD5A					P21				
		VCCPD5B					N18				
		VCCPD5B					M17				
		VCCPD7A8A					E11				
		VCCPD7A8A					D16				
		VCCPD7A8A					D14				
		VCCPD7A8A					D8				
		VCCPD7A8A					C10				
3A	VREFB3AN0	VREFB3AN0					Y7				
3B	VREFB3BN0	VREFB3BN0					Y12				
4A	VREFB4AN0	VREFB4AN0					AB16				
5A	VREFB5AN0	VREFB5AN0		4			R20				
5B	VREFB5BN0	VREFB5BN0		4			L20				
7A	VREFB7AN0	VREFB7AN0		4			C14				
BA	VREFB8AN0	VREFB8AN0		.			B8				
		NC		.			Y6				
		NC		-			V11				
		VCCH_GXBL		-			M3				
	1	VCCH_GXBL		+	 		T3	 	-	-	
	 	VCCL_GXBL		 	 	+	P3	 		+	
	 	VCCL_GXBL RREF_TL		 	 	+	K3	 		+	
	 	VCCA_FPLL		 	 	+	A1 T5	 		+	
	1	VCCA_FPLL VCCA_FPLL	+		1		F4	1	+	-	1
	1	VCCA_FPLL VCCA_FPLL		1	1		U18	1	1		1
		VCCA_FPLL VCCA_FPLL			1		H19	1			1
	1	VCC_AUX	<u> </u>	 	1		E6	1	+	+	1
	1	VCC_AUX VCC_AUX	<u> </u>	 	1		D18	1	+	+	1
	-	VCC_AUX		1		+	W18		_	-	
	1	VCC_AUX		1	1		W13	1		<u> </u>	1
	1	VCC_AUX	<u> </u>	+	<u> </u>	†	W7	1		+	1
	1	VCC_AUX	<u> </u>	+	<u> </u>	†	D11	1		+	1
	1	VCCE_GXBL		†	1		L4	1		1	1
	1	VCCE GXBL		†	1		N4	1		1	1
	1	VCCE_GXBL		†	1		K5	1		1	1
	1	VCCE_GXBL		1	1		J4	1		1	1

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.

(2) RESET pin is only applicable for DDR3 device.



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
GXB_L1		REFCLK1Ln					G4				<u> </u>
GXB_L1		REFCLK1Lp					F5				
GXB_L1 GXB_L1		GXB_TX_L5n GXB_TX_L5p				+	D3				
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					C2				
GXB_L1		GXB RX L5n,GXB REFCLK L5n					C1				
GXB_L1		GXB_TX_L4n					E1				
GXB_L1		GXB_TX_L4p					E2				
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2				
GXB_L1 GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n GXB_TX_L3n					G1 J1				-
GXB_L1		GXB_TX_L3p					J2				-
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					L2				
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					L1				
GXB_L0		GXB_TX_L2n					N1				
GXB_L0		GXB_TX_L2p					N2				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					R2				
GXB_L0 GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n GXB_TX_L1n					R1 U1				
GXB_L0	l	GXB_TX_L1p			-	1	U2				
GXB_L0	l	GXB_RX_L1p,GXB_REFCLK_L1p		1	1		W2	1	1		
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					W1				
GXB_L0		GXB_TX_L0n					Y3				
GXB_L0		GXB_TX_L0p					Y4				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AA2				-
GXB_L0 GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n REFCLK0Lp					AA1 V4				
GXB_L0		REFCLK0Ln					U4 U4				
3A		TDO		TDO			V3				
3A		nCSO		DATA4			AB6				
3A		TMS		TMS			R4				
3A		AS_DATA3		DATA3			AA5				
3A 3A		TCK AS_DATA2		TCK DATA2			V5 T5				
3A		TDI		TDI			P5				
3A		AS_DATA1		DATA1			W5				
3A		DCLK		DCLK			M5				
3A		AS_DATA0,ASDO		DATA0			AB4				
3A	VREFB3AN0	10		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	P6	DQ1B			
3A	VREFB3AN0 VREFB3AN0			DATA5	DIFFIO_TX_B2n DIFFIO_RX_B1p	DIFFOUT_B2n	U7 N6	DQ1B			
3A		10		DATA8 DATA7	DIFFIO_RX_B1p	DIFFOUT_B1p DIFFOUT_B2p	U6	DQ1B DQ1B			
3A		IO		DATA10	DIFFIO_TX_B2p	DIFFOUT B3n	M6	DQSn1B			
3A		10		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	R5	DQ1B			
3A	VREFB3AN0	10		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	M7	DQS1B			
3A		10		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	R6				
3A		10		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R7	DQ1B			
3A 3A		IO IO		DATA13 CLKUSR	DIFFIO_TX_B6n DIFFIO_RX_B5p	DIFFOUT_B6n DIFFOUT_B5p	L7 T7	DQ1B DQ1B			
3A		10		DATA15	DIFFIO_RX_B5p	DIFFOUT_B6p	1.8	DQ1B			
3A	VREFB3AN0			PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	T8	DQID			1
3A	VREFB3AN0	10		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	P7	DQ1B			
3A	VREFB3AN0	10		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	T9				
3A	VILLI DOVING	10			DIFFIO_TX_B8p	DIFFOUT_B8p	P8	DQ1B		L	L
3B	VREFB3BN0			1	DIFFIO_TX_B9n	DIFFOUT_B9n	V8	DOOD	1	GND	GND
3B 3B	VREFB3BN0 VREFB3BN0	10 10		 	DIFFIO_RX_B10n DIFFIO_TX_B9p	DIFFOUT_B10n DIFFOUT_B9p	N8	DQ2B DQ2B	-	B_A_15 B_WE#	
3B 3B		10		 	DIFFIO_IX_B9p DIFFIO_RX_B10p	DIFFOUT_B10p	W8 M8	DQ2B DQ2B	1	B_WE# B_A_14	
<u>зв</u> 3В		10		<u> </u>	DIFFIO_RX_B10p	DIFFOUT_B11n	N9	DQSn2B	1	B_CS#_1	B CS# 1
3B	VREFB3BN0	10			DIFFIO_TX_B12n	DIFFOUT_B12n	AA7	DQ2B		B_A_13	
3B	VREFB3BN0				DIFFIO_RX_B11p	DIFFOUT_B11p	N10	DQS2B		B_CS#_0	B_CS#_0
3B	VREFB3BN0	10			DIFFIO_TX_B12p	DIFFOUT_B12p	AB7			B_A_12	
3B	VREFB3BN0	10		1	DIFFIO_TX_B13n	DIFFOUT_B13n	Y7	DQ2B	1	B_A_11	D CA C
3B	VREFB3BN0 VREFB3BN0	10			DIFFIO_RX_B14n DIFFIO_TX_B13p	DIFFOUT_B14n	U8 W7	DQ2B		B_A_9 B A 10	B_CA_9
3B 3B		10	1	1	DIFFIO_TX_B13p DIFFIO_RX_B14p	DIFFOUT_B13p DIFFOUT_B14p	W7 V9	DQ2B DQ2B	1	B_A_10 B A 8	B CA 8
3B 3B	VREFB3BN0 VREFB3BN0		CLK0n,FPLL_BL_FBn	-	DIFFIO_RX_B14p	DIFFOUT_B15n	R9	טעבט	+	D_A_0	D_UA_0
3B		10			DIFFIO_TX_B16n	DIFFOUT_B16n	AB8	DQ2B		B_RAS#	
3B	VREFB3BN0	10	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	P9				
3B	VREFB3BN0	10			DIFFIO_TX_B16p	DIFFOUT_B16p	AA8	DQ2B		B_CAS#	
3B		10		ļ	DIFFIO_TX_B17n	DIFFOUT_B17n	Y10	ļ	ļ	GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AA9	DQ3B		B_BA_2	



	lunes.	In	15 d 15 d 15	Ia a	Ta	Te	luia:	Inaa.:	Inco	luna n	Note (1)
ank umber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for	HMC Pin Assignment for
										DDR3/DDR2 (2)	LPDDR2
	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	AA10	DQ3B		B_BA_0	
	VREFB3BN0	10			DIFFIO_RX_B18p	DIFFOUT_B18p	Y9	DQ3B		B_BA_1	
	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	L9	DQSn3B		B_CK#	B_CK#
	VILLI DODITO	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	W11	DQ3B		B_A_7	B_CA_7
	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	M10	DQS3B		B_CK	B_CK
	VREFB3BN0 VREFB3BN0	10	FPLL BL CLKOUT1,FPLL BL CLKOUTn	+	DIFFIO_TX_B20p DIFFIO_TX_B21n	DIFFOUT_B20p DIFFOUT_B21n	Y11 AB10	DQ3B		B_A_6 B A 3	B_CA_6 B CA 3
	VREFB3BN0 VREFB3BN0	io	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUT1	_	DIFFIO_IX_B21n	DIFFOUT_B22n	U10	DQ3B		B_A_3 B A 5	B_CA_3 B CA 5
		10	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB	+	DIFFIO_TX_B21p	DIFFOUT_B21p	AB11	DQ3B		B_A_2	B_CA_2
		10	11 EE_BE_GEROOTO,11 EE_BE_GEROOTD,11 EE_BE_1 B		DIFFIO_RX_B22p	DIFFOUT_B22p	U11	DQ3B		B_A_4	B_CA_4
	VREFB3BN0	10	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	T10				1
	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	R11	DQ3B		B_A_1	B_CA_1
	VREFB3BN0	10	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	R10				
	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	P12	DQ3B		B_A_0	B_CA_0
		10	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AA13				
\	VILLI DIDUTE	10		+	DIFFIO_RX_B26n	DIFFOUT_B26n	W12	DQ4B		B_DQ_0	B_DQ_0
	VREFB4AN0 VREFB4AN0	io		_	DIFFIO_TX_B25p DIFFIO_RX_B26p	DIFFOUT_B25p DIFFOUT B26p	AB13 Y12	DQ4B DQ4B		B_DQ_2 B_DQ_1	B_DQ_2 B_DQ_1
		IO		+	DIFFIO_RX_B26p DIFFIO_RX_B27n	DIFFOUT B27n	U12	DQSn4B		B_DQ_1 B_DQS#_0	B_DQ_I B_DQS#_0
	VREFB4AN0 VREFB4AN0			+	DIFFIO_RX_B2/n DIFFIO_TX_B28n	DIFFOUT_B28n	R12	DQSn4B DQ4B	+	B_DQS#_0 B DQ 3	B_DQS#_0 B DQ 3
		IO		+	DIFFIO_TX_B280	DIFFOUT_B27p	T12	DQS4B	1	B_DQS_0	B_DQS_0
		10			DIFFIO_TX_B28p	DIFFOUT_B28p	T13	DQ04D		B_ODT_0	B_ODT_0
		10			DIFFIO_TX_B29n	DIFFOUT_B29n	AB15	DQ4B		B ODT 1	B ODT 1
1	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	W13	DQ4B		B_DQ_4	B_DQ_4
١	VREFB4AN0	10			DIFFIO_TX_B29p	DIFFOUT_B29p	AB16	DQ4B		B_DQ_6	B_DQ_6
١		IO			DIFFIO_RX_B30p	DIFFOUT_B30p	V13	DQ4B		B_DQ_5	B_DQ_5
١	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	T14				
	VREFB4AN0	10			DIFFIO_TX_B32n	DIFFOUT_B32n	AB18	DQ4B		B_DQ_7	B_DQ_7
	VREFB4AN0 VREFB4AN0	10	CLK2p	+	DIFFIO_RX_B31p DIFFIO_TX_B32p	DIFFOUT_B31p DIFFOUT_B32p	U13 AA18	DO 4D		B DM 0	B DM 0
		IO		_	DIFFIO_TX_B32p	DIFFOUT_B32p DIFFOUT_B33n	AA18 AA19	DQ4B		GND	GND
	VREFB4AN0	IO			DIFFIO_IX_B33II	DIFFOUT_B33fi DIFFOUT_B34n	Y14	DQ5B	DQ1B	B_DQ_8	B_DQ_8
	VREFB4AN0	10		+	DIFFIO_TX_B33p	DIFFOUT B33p	Y19	DQ5B DQ5B	DQ1B	B DQ 10	B_DQ_0 B DQ 10
	VREFB4AN0	10			DIFFIO RX B34p	DIFFOUT B34p	W14	DQ5B	DQ1B	B DQ 9	B DQ 9
\	VREFB4AN0	10			DIFFIO RX B35n	DIFFOUT B35n	P14	DQSn5B	DQ1B	B DQS# 1	B DQS# 1
1		IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AA20	DQ5B	DQ1B	B_DQ_11	B_DQ_11
١	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	R14	DQS5B	DQ1B	B_DQS_1	B_DQS_1
4	VREFB4AN0	10			DIFFIO_TX_B36p	DIFFOUT_B36p	Y20			B_CKE_1	B_CKE_1
4	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA15	DQ5B	DQ1B	B_CKE_0	B_CKE_0
١	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	U15	DQ5B	DQ1B	B_DQ_12	B_DQ_12
\ \		10			DIFFIO_TX_B37p	DIFFOUT_B37p	Y15	DQ5B	DQ1B	B_DQ_14	B_DQ_14
\ \	VREFB4AN0 VREFB4AN0	10	OLIVO-	_	DIFFIO_RX_B38p	DIFFOUT_B38p	V15	DQ5B	DQ1B	B_DQ_13	B_DQ_13
\ \		IO	CLK3n	+	DIFFIO_RX_B39n DIFFIO_TX_B40n	DIFFOUT_B39n DIFFOUT_B40n	R15 AB20	DQ5B	DQ1B	B_DQ_15	B_DQ_15
\ \	VREFB4AN0	io In	CLK3p		DIFFIO_TX_B40II	DIFFOUT_B39p	T15	DQSB	DQIB	D_DQ_13	D_DQ_13
\ \	VREFB4AN0	10	CERCOP		DIFFIO_TX_B40p	DIFFOUT B40p	AB21	DQ5B	DQ1B	B DM 1	B DM 1
`		10			DIFFIO_TX_B41n	DIFFOUT_B41n	AB22	5405	54.5	GND	GND
1	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	Y16	DQ6B	DQ1B	B_DQ_16	B_DQ_16
١	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AA22	DQ6B	DQ1B	B_DQ_18	B_DQ_18
	VREFB4AN0	10			DIFFIO_RX_B42p	DIFFOUT_B42p	Y17	DQ6B	DQ1B	B_DQ_17	B_DQ_17
١	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	U16	DQSn6B	DQSn1B	B_DQS#_2	B_DQS#_2
١		IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AA17	DQ6B	DQ1B	B_DQ_19	B_DQ_19
\		10		+	DIFFIO_RX_B43p	DIFFOUT_B43p	U17	DQS6B	DQS1B	B_DQS_2	B_DQS_2
	VREFB4AN0 VREFB4AN0	10		_	DIFFIO_TX_B44p	DIFFOUT_B44p DIFFOUT_B45n	AB17	DQ6B	DQ1B	B_RESET# GND	B_RESET#
	VREFB4AN0 VREFB4AN0	10			DIFFIO_TX_B45n DIFFIO_RX_B46n	DIFFOUT_B45n DIFFOUT_B46n	Y22 V18	DQ6B DQ6B	DQ1B DQ1B	B DQ 20	B DQ 20
`	VREFB4AN0	in		+	DIFFIO_TX_B45p	DIFFOUT_B45p	Y21	DQ6B	DQ1B	B DQ 22	B_DQ_20
		10		1	DIFFIO_RX_B46p	DIFFOUT_B45p	W18	DQ6B	DQ1B	B DQ 21	B DQ 21
		10			DIFFIO RX B47n	DIFFOUT_B47n	W16			GND	GND
	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	W21	DQ6B	DQ1B	B_DQ_23	B_DQ_23
	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	W17			GND	GND
\	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	W22	DQ6B	DQ1B	B_DM_2	B_DM_2
١	VREFB5AN0		RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	U22	DQ1R			
4	VREFB5AN0			INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V20	ļ			1
١	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	U21	DQ1R			
	VREFB5AN0	10		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V19	2012	-		
	VREFB5AN0	10		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T19	DQ1R	-	1	+
A	VREFB5ANO	10		CvP_CONFDONE	DIFFIO_RX_R4p	DIFFOUT_R4p	T17	DQ1R	+	+	+
4	VREFB5AN0 VREFB5AN0	io In		CVP_CONFIDURE	DIFFIO_TX_R3n DIFFIO_RX_R4n	DIFFOUT_R3n DIFFOUT_R4n	T20 T18	DQ1R DQ1R	1	+	+
<u>, </u>	VREFB5AN0	io		DEV OE	DIFFIO_RX_R4II	DIFFOUT_R5p	T22	DQ III	1		+
\ \	VREFB5AN0	10		52.02	DIFFIO_TX_R5p	DIFFOUT_R6p	R16	DQS1R	1	1	
	JUNIO	11.7	1								



		Din Name/Eurotian	Ontional Function(a)								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	R22	DQ1R			
5A 5A	VREFB5AN0 VREFB5AN0	10		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R		+	
5A	VREFB5AN0	IO			DIFFIO_TX_R7p DIFFIO_RX_R8p	DIFFOUT_R7p DIFFOUT_R8p	R20 R19	DQ1R DQ1R		+	+
5A	VREFB5AN0	IO .			DIFFIO_TX_R7n	DIFFOUT_R7n	R21	DQIK		+	+
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	P19	DQ1R		+	+
5B		10	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R9p	DIFFOUT R9p	M16	DQ		-	+
5B		10			DIFFIO_TX_R10p	DIFFOUT_R10p	E21	DQ2R		1	
5B	VREFB5BN0	IO	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R9n	DIFFOUT_R9n	M17				
5B	VREFB5BN0	10			DIFFIO_TX_R10n	DIFFOUT_R10n	D22	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	L19	DQ2R			
5B	VREFB5BN0				DIFFIO_TX_R12p	DIFFOUT_R12p	K21	DQ2R			
5B	VREFB5BN0				DIFFIO_RX_R11n	DIFFOUT_R11n	L20	DQ2R			
5B 5B		10			DIFFIO_TX_R12n	DIFFOUT_R12n DIFFOUT_R13p	J21	DQ2R		+	
5B 5B	VREFB5BN0 VREFB5BN0	10			DIFFIO_RX_R13p DIFFIO_TX_R14p	DIFFOUT_R13p	L15 G22	DQS2R	+	+	+
5B	VREFB5BN0	10			DIFFIO_TX_R14p	DIFFOUT_R13n	K15	DQSn2R		+	+
5B	VREFB5BN0	io			DIFFIO_TX_R14n	DIFFOUT_R14n	G21	DQ2R		+	+
5B		10			DIFFIO_RX_R15p	DIFFOUT_R15p	L18	DQ2R		-	†
5B	VREFB5BN0	10			DIFFIO_TX_R16p	DIFFOUT R16p	G20	DQ2R		1	1
5B	VREFB5BN0	10			DIFFIO_RX_R15n	DIFFOUT_R15n	K19	DQ2R		1	T .
5B	VREFB5BN0	IO			DIFFIO_TX_R16n	DIFFOUT_R16n	H21			<u> </u>	
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	L17			Т	
5B		10			DIFFIO_TX_R18p	DIFFOUT_R18p	E20	DQ3R			
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	K17				
5B	VREFB5BN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	F20	DQ3R			<u> </u>
5B	VREFB5BN0	IO .			DIFFIO_RX_R19p	DIFFOUT_R19p	H20	DQ3R			
5B 5B		10	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	G18	DQ3R		+	
5B 5B		10	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_RX_R19n DIFFIO_TX_R20n	DIFFOUT_R19n DIFFOUT_R20n	H19 G17	DQ3R DQ3R		+	
5B	VREFB5BN0	IO IO	FPLL_BR_CLROUTI,FPLL_BR_CLROUTII		DIFFIO_TX_R20II	DIFFOUT R21n	K16	DQS3R		+	+
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT R220	F19	DQSSK		+	+
5B	VREFB5BN0	10			DIFFIO RX R21n	DIFFOUT R21n	J16	DQSn3R		-	†
5B	VREFB5BN0	10			DIFFIO_TX_R22n	DIFFOUT R22n	F18	DQ3R		1	
5B	VREFB5BN0				DIFFIO RX R23p	DIFFOUT R23p	J17	DQ3R		1	
5B		10			DIFFIO_TX_R24p	DIFFOUT_R24p	J19	DQ3R		1	1
5B		10			DIFFIO_RX_R23n	DIFFOUT_R23n	J18	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	H18				
7A		GND					F17				4
7A		IO			DIFFIO_RX_T17p	DIFFOUT_T17p	H16			GND	GND
7A 7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_TX_T18p DIFFIO_RX_T17n	DIFFOUT_T18p DIFFOUT_T17n	C21 G16	DQ1T	DQ1T	T_DM_2 GND	T_DM_2 GND
7A 7A	VREFB7AN0 VREFB7AN0	io			DIFFIO_RX_I1/n DIFFIO_TX_T18n	DIFFOUT_117n DIFFOUT_T18n	C20	DQ1T	DQ1T	T DQ 23	T DQ 23
7A 7A		10			DIFFIO_TX_T18h	DIFFOUT_T19p	D18	DQ1T	DQ1T	T_DQ_21	T_DQ_23
7A	VREFB7AN0				DIFFIO_TX_T20p	DIFFOUT_T20p	B20	DQ1T	DQ1T	T DQ 22	T DQ 22
7A		10			DIFFIO_RX_T19n	DIFFOUT_T19n	E17	DQ1T	DQ1T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	10			DIFFIO_TX_T20n	DIFFOUT_T20n	B21	DQ1T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	G15	DQS1T	DQS1T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	B22			T_RESET#	T_RESET#
7A		10			DIFFIO_RX_T21n	DIFFOUT_T21n	G14	DQSn1T	DQSn1T	T_DQS#_2	T_DQS#_2
7A		10			DIFFIO_TX_T22n	DIFFOUT_T22n	A22	DQ1T	DQ1T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	E16	DQ1T	DQ1T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	IO		ļ	DIFFIO_TX_T24p	DIFFOUT_T24p	A20	DQ1T	DQ1T	T_DQ_18	T_DQ_18
7A	VREFB7AN0	10		 	DIFFIO_RX_T23n	DIFFOUT_T23n	D17	DQ1T	DQ1T	T_DQ_16	T_DQ_16
7A 7A		10	OLIVATA:	I	DIFFIO_TX_T24n	DIFFOUT_T24n	A19	 	+	GND	GND
7A 7A	VREFB7ANO	10	CLK11p	 	DIFFIO_RX_T25p	DIFFOUT_T25p	G13	DOST	DO1T	T_DM_1	T_DM_1
7A 7A		IO IO	CLK11n	 	DIFFIO_TX_T26p DIFFIO_RX_T25n	DIFFOUT_T26p DIFFOUT_T25n	C19 F14	DQ2T	DQ1T	I_DIVI_I	ו_ואוט_ו
7A 7A	VREFB7AN0	IO	OLIVI III	†	DIFFIO_RX_125n	DIFFOUT T26n	C18	DQ2T	DQ1T	T DQ 15	T DQ 15
7A	VREFB7AN0	10		1	DIFFIO_RX_T27p	DIFFOUT_T27p	C16	DQ2T	DQ1T	T DQ 13	T DQ 13
7A	VREFB7AN0	10			DIFFIO_TX_T28p	DIFFOUT_T28p	B16	DQ2T	DQ1T	T_DQ_14	T_DQ_14
7A		Ю			DIFFIO_RX_T27n	DIFFOUT_T27n	C15	DQ2T	DQ1T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	B15	DQ2T	DQ1T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	10			DIFFIO_RX_T29p	DIFFOUT_T29p	G12	DQS2T	DQ1T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	10			DIFFIO_TX_T30p	DIFFOUT_T30p	A18			T_CKE_1	T_CKE_1
7A		10			DIFFIO_RX_T29n	DIFFOUT_T29n	H12	DQSn2T	DQ1T	T_DQS#_1	T_DQS#_1
7A	***************************************	10			DIFFIO_TX_T30n	DIFFOUT_T30n	A17	DQ2T	DQ1T	T_DQ_11	T_DQ_11
7A	VREFB7AN0	10		1	DIFFIO_RX_T31p	DIFFOUT_T31p	F15	DQ2T	DQ1T	T_DQ_9	T_DQ_9
7A	VREFB7ANO	10	 	 	DIFFIO_TX_T32p	DIFFOUT_T32p	B18	DQ2T	DQ1T	T_DQ_10	T_DQ_10
7A	VREFB7AN0 VREFB7AN0	10		+	DIFFIO_RX_T31n DIFFIO_TX_T32n	DIFFOUT_T31n DIFFOUT_T32n	E14 B17	DQ2T	DQ1T	T_DQ_8 GND	T_DQ_8 GND
7A		10	CLK10n	 	DIFFIO_TX_T32n DIFFIO_RX_T33p		H10	1	+	GIND	GIND
7A	VREFB7AN0	JIO .	CLK10p	I .	DILLIOTKY 199b	DIFFOUT_T33p	וחוט	1		_1	

Page 20 of 35



	Lunes	In. 1. 15		10 0 0 0	To	I	111101	Inaa ()/a	Inaa () ()	Times no	Note (1
ank umber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	A15	DQ3T		T_DM_0	T_DM_0
	VREFB7AN0	10	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G11	Daoi		1_50	1_50
	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	A14	DQ3T		T_DQ_7	T_DQ_7
	VREFB7AN0				DIFFIO_RX_T35p	DIFFOUT_T35p	D13	DQ3T		T_DQ_5	T_DQ_5
		IO			DIFFIO_TX_T36p	DIFFOUT_T36p	C14	DQ3T		T_DQ_6	T_DQ_6
	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T35n DIFFIO_TX_T36n	DIFFOUT_T35n DIFFOUT_T36n	C13 D14	DQ3T DQ3T		T_DQ_4 T_ODT_1	T_DQ_4 T_ODT_1
	VREFB7AN0	IO			DIFFIO_TX_T30II	DIFFOUT_T37p	H9	DQS3T		T DQS 0	T DQS 0
	VREFB7AN0				DIFFIO_TX_T38p	DIFFOUT_T38p	A13	DQOST		T_ODT_0	T_ODT_0
	VREFB7AN0				DIFFIO_RX_T37n	DIFFOUT_T37n	G8	DQSn3T		T_DQS#_0	T_DQS#_0
		10			DIFFIO_TX_T38n	DIFFOUT_T38n	B13	DQ3T		T_DQ_3	T_DQ_3
		IO			DIFFIO_RX_T39p	DIFFOUT_T39p	E12	DQ3T		T_DQ_1	T_DQ_1
		10			DIFFIO_TX_T40p	DIFFOUT_T40p	B12	DQ3T		T_DQ_2	T_DQ_2
	VREFB7AN0 VREFB7AN0	10	RZQ 2		DIFFIO_RX_T39n DIFFIO_TX_T40n	DIFFOUT_T39n DIFFOUT_T40n	F12 A12	DQ3T		T_DQ_0	T_DQ_0
		IO IO	CLK9p		DIFFIO_TX_T40II	DIFFOUT_T41p	G10				+
	VREFB8AN0	10			DIFFIO TX T42p	DIFFOUT_T42p	C11	DQ4T		T A 0	T CA 0
	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	F10				
		10			DIFFIO_TX_T42n	DIFFOUT_T42n	B11	DQ4T		T_A_1	T_CA_1
	VREFB8AN0		<u> </u>		DIFFIO_RX_T43p	DIFFOUT_T43p	D11	DQ4T		T_A_4	T_CA_4
	VREFB8AN0 VREFB8AN0		FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p DIFFIO_RX_T43n	DIFFOUT_T44p DIFFOUT_T43n	A8	DQ4T DQ4T	 	T_A_2 T_A_5	T_CA_2
		10	FPLL TL CLKOUT1,FPLL TL CLKOUTn		DIFFIO_RX_143n DIFFIO_TX_T44n	DIFFOUT_143n DIFFOUT_T44n	E11	DQ41 DQ4T	†	T A 3	T_CA_5 T_CA_3
	VREFB8AN0	10	TILL IL GENOUTI, FFEE IL GENOUTII		DIFFIO_TX_T44II	DIFFOUT_T45p	J9	DQS4T	†	T CK	T CK
·		10			DIFFIO_TX_T46p	DIFFOUT_T46p	F8			T_A_6	T_CA_6
V.	VREFB8AN0				DIFFIO_RX_T45n	DIFFOUT_T45n	J8	DQSn4T		T_CK#	T_CK#
	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	E7	DQ4T		T_A_7	T_CA_7
	VREFB8AN0	10			DIFFIO_RX_T47p	DIFFOUT_T47p	C10	DQ4T		T_BA_1	-
	VREFB8AN0 VREFB8AN0	10			DIFFIO_TX_T48p DIFFIO_RX_T47n	DIFFOUT_T48p DIFFOUT_T47n	C6 C9	DQ4T DQ4T		T_BA_0 T_BA_2	
		IO			DIFFIO_RX_14/II	DIFFOUT_T48n	D7	DQ41		GND	GND
		10	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	K7			0.15	10.15
1	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	A10	DQ5T		T_CAS#	1
4	VREFB8AN0	10	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	J7				
	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	A9	DQ5T		T_RAS#	
	VREFB8AN0 VREFB8AN0	IO IO			DIFFIO_RX_T51p	DIFFOUT_T51p	D9 B6	DQ5T		T_A_8 T_A_10	T_CA_8
	VREFB8AN0 VREFB8AN0	io			DIFFIO_TX_T52p DIFFIO_RX_T51n	DIFFOUT_T52p DIFFOUT_T51n	D8	DQ5T DQ5T		T_A_10	T CA 9
	VREFB8AN0	10			DIFFIO_RX_151II	DIFFOUT T52n	B5	DQ5T		T A 11	I_CA_9
	VREFB8AN0	10			DIFFIO RX T53p	DIFFOUT_T53p	H8	DQS5T		T CS# 0	T CS# 0
	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	C8			T_A_12	
	VREFB8AN0				DIFFIO_RX_T53n	DIFFOUT_T53n	G7	DQSn5T		T_CS#_1	T_CS#_1
		10			DIFFIO_TX_T54n	DIFFOUT_T54n	B8	DQ5T		T_A_13	
	VREFB8AN0 VREFB8AN0	10			DIFFIO_RX_T55p DIFFIO_TX_T56p	DIFFOUT_T55p DIFFOUT_T56p	H6 E6	DQ5T DQ5T		T_A_14 T WE#	
	VREFB8AN0	io			DIFFIO_TX_T55n	DIFFOUT_T55n	G6	DQ5T		T A 15	+
	VREFB8AN0	10			DIFFIO_TX_T56n	DIFFOUT_T56n	F7	DQST		GND	GND
		MSEL0		MSEL0			L6				
		CONF_DONE		CONF_DONE			J6				
	1	MSEL1		MSEL1	ļ		K6		_	1	
	+	nSTATUS nCE		nSTATUS nCE			G5 H5	 	+		+
	+	MSEL2		MSEL2			A2		+		+
	+	MSEL3		MSEL3			F5				+
	1	nCONFIG		nCONFIG	1		A4	Ì	1		1
		MSEL4		MSEL4			C5				1
		GND					F3				
	1	GND			ļ		F21		_	1	
	 	GND GND			1		AB19 AB2	-	 	1	+
	+	GND GND	+		1		AB2 AB1	1	+	+	+
	1	GND			-		AA16	†	 	+	+
		GND					AA11	İ			1
		GND					AA4				
		GND					AA3				
		GND					Y13		1		1
	1	GND			ļ		Y8		_	1	
	+	GND	+		1	+	Y5	ļ	+	1	+
	 	GND GND		+	-		Y2 Y1	 	 	+	+
	†	GND	-				W20	†	†	+	+
	1	GND					W4	1	1		
			•			t and the second					

Page 21 of 35



								· Inner va Inner Ivan				
Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin	HMC Pin	
Number				_	Channel	-				Assignment for DDR3/DDR2 (2)	Assignment for	
										DDR3/DDR2 (2)	LPDDR2	
		GND					W3					
		GND					V22					
		GND					V17					
		GND					V2					
		GND					V1					
		GND					U19					
		GND					U14					
		GND					U9					
		GND					U5					
		GND					U3					
		GND					T11					
		GND					T2					
		GND					T1					
		GND					R13					
		GND					R3					
		GND					P10					
		GND					P4					
		GND					P2					
		GND					P1					
		GND					N22					
		GND					N15					
		GND					N13					
		GND					N11					
		GND					N7					
		GND					N5					
		GND					N3					
		GND					M19					
		GND					M14					
		GND					M12					
		GND					M9					
		GND					M4					
		GND					M2				1	
		GND					M1					
		GND					L16				1	
		GND					L13					
		GND					L11				1	
		GND					L5				1	
		GND					L3				1	
		GND					K14				+	
		GND					K12				1	
		GND					K10				1	
		GND					K8				+	
		GND					K4				+	
		GND		+			K2				+	
		GND		+			K1				+	
	1	GND	<u> </u>	-		†	J20	t		1	† 	
	1	GND	<u> </u>	-		†	J15	t		1	† 	
		GND			-	1	J13		<u> </u>	1	 	
	1	GND	<u> </u>	-		†	J13	t		1	† 	
		GND			-	1	J5		<u> </u>	1	 	
	1	GND	<u> </u>	1	1	1	J3	t	1	 	+	
	1	GND		 	1	 	H14	† 	1	 	+	
		GND	 	 	 	 	H14 H4	 	1	1	+	
	1	GND	<u> </u>	1	1	1	H4 H3	t	1	 	+	
		GND		-	-	+	H3 H2	—	-	1	+	
	 		-	 	-			 	 	 	+	
		GND		-	-	+	H1	—	-	1	+	
	-	GND			-		G9	-	-	 	+	
	-	GND					G3	-		 	+	
	-	GND			-		F16	-	-	 	+	
	-	GND					F11	-		 	+	
	1	GND		1	1	 	F6	1	1	1	+	
	1	GND		1	1	 	F2	 	1	 	+	
		GND	ļ	.	ļ	 	F1	-	ļ	 	+	
		GND	1				E13	Ļ		ļ		
		GND	1				E4	Ļ		ļ	4	
		GND					E3				4	
		GND					D20				1	
		GND					D10				1	
		GND					D5					
		GND		1			D2			ļ	1	
		GND					D1				1	
		GND					C22			<u> </u>		



David.	Lyper	Dia Namatra	Continued Franciscosts	0	D	Ferritary 41 MDC Co	11101	DOD ()**	DO0 (****	LIMO DI	Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					C17				
		GND					C7				
		GND					C4				
		GND					C3				
		GND					B14				
		GND					B2				
		GND					B1				
		GND					A21				
		GND					A11				
		GND					A5				
		VCC					J14				
		VCC					P15				
		VCC					P13				
		VCC					P11				
		VCC					N14				
		VCC					N12				
		VCC					M15				
		VCC					M13				
	 	VCC			-		M11 L14		 	 	
	 	VCC		 				-	 	1	
	-	VCC					L12	ļ	 	1	
	 	VCC		 			L10	-	 	1	
	-	VCC					K13	ļ	 	1	
		VCC					K11				
		VCC					K9				
		VCC					J12				
		VCC					J10				
		VCC					H15				
		VCC					H13				
		VCC					H11				
		DNU					B3				
		DNU					B4				
		DNU					D21				
		DNU					E10				
		VCCPGM					Y6				
		VCCPGM					U20				
		VCCPGM					B7				
		VCCBAT					A3				
		VCCIO3A					T6				
		VCCIO3A					AA6				
		VCCIO3B					V7				
		VCCIO3B					AB9				
		VCCIO3B					W10				
		VCCIO3B					R8				
		VCCIO4A					T16				
		VCCIO4A		 			AB14	-	 	1	
	-	VCCIO4A					AA21	ļ	 	1	
	 	VCCIO4A VCCIO4A		 	-		Y18 W15		 	 	
	 	VCCIO4A VCCIO4A		-	-		W15 V12		1	-	
	 				-		V12 T21		 	 	
	-	VCCIO5A VCCIO5A		-	-		R18		†	1	+
	 	VCCIO5B		-	-		H22		1	-	
	1	VCCIO5B VCCIO5B		 	 		P20	1	1	}	
	-	VCCIO5B VCCIO5B		-	-		N17		†	1	+
	 	VCCIO5B VCCIO5B		 	-		N17 L21		 	 	
	-	VCCIO5B VCCIO5B		-	-		K18		†	1	+
	 	VCCIO5B VCCIO5B		 	-		K18 G19		 	 	
					-				 	 	
	 	VCCIO7A		-	-		B19		1	-	
	 	VCCIO7A VCCIO7A		-	-		H17 E18		1	-	
	 			 	-				 	 	
	-	VCCIO7A VCCIO7A		-	-		D15		†	1	
		VCCIO7A VCCIO7A		 	-		C12 A16		 	 	
	 				-				 	 	
	 	VCCIO8A VCCIO8A		 	-		E8 H7		 	 	
	 	VCCIOSA		-	-		H/ B9		1	-	
	 		<u> </u>	 	1		B9 A6	 	 	1	
	 	VCCIO8A			-				 	 	
	 	VCCPD3A		 			V6	-	 	1	
	-	VCCPD3B4A		-	-		V16		†	1	+
		VCCPD3B4A		 			W9		1	-	
		VCCPD3B4A	j	1	1	1	V14	1	1	1	1



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		VCCPD3B4A					V10				1
		VCCPD5A					P17				+
		VCCPD5B					N19				1
		VCCPD5B					M18				1
		VCCPD7A8A					F13				1
		VCCPD7A8A					F9				1
		VCCPD7A8A					E15				1
		VCCPD7A8A					E9				1
3A	VREFB3AN0	VREFB3AN0					W6				
3B	VREFB3BN0	VREFB3BN0					AB12				1
4A	VREFB4AN0	VREFB4AN0					AA14				1
5A	VREFB5AN0	VREFB5AN0					V21				
5B	VREFB5BN0	VREFB5BN0					K20				1
7A	VREFB7AN0	VREFB7AN0					D16				1
8A	VREFB8AN0	VREFB8AN0					B10				1
		NC					AB3				1
	İ	NC					V11				1
	İ	NC					P22				1
		NC					P21				1
		NC					P18				1
		NC					P16				1
		NC					N21				1
		NC					N20				1
		NC				İ	N18				1
		NC					N16				+
		NC					M22				1
		NC				İ	M21				1
		NC					M20				+
		NC				İ	L22				1
		NC					K22				+
		NC					J22				+
		NC					F22				+
		NC					E22				+
		VCCH_GXBL					T3				+
		VCCH GXBL					M3				+
		VCCL GXBL			1		P3				1
		VCCL GXBL			İ		K3		1		1
		RREF_TL			İ		A1		1		1
		VCCA_FPLL			1		T4		1		1
		VCCA_FPLL			İ		F4		İ		1
		VCCA_FPLL			1		U18		1		1
		VCCA FPLL			1		E19		1		1
		VCC_AUX			1		D6		1		1
		VCC AUX			1		D12		1		1
	l	VCC_AUX		<u> </u>	<u> </u>		D19		+	1	+
		VCC_AUX			1		W19		1		1
		VCC_AUX			1		AA12		1		1
		VCC AUX					AB5				1
		VCCE_GXBL			İ		L4		1		1
		VCCE_GXBL			1		N4		1		1
		VCCE_GXBL			1		K5		1		1
		VCCE_GXBL			1		J4		1		1

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.

(2) RESET pin is only applicable for DDR3 device.



											Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
GXB_L1		REFCLK1Ln					P6				
GXB_L1		REFCLK1Lp					N7				
GXB_L1 GXB_L1		GXB_TX_L5n GXB_TX_L5p				+	K1 K2				
GXB_L1		GXB_TX_L5p GXB_RX_L5p,GXB_REFCLK_L5p					M2		†		
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					M1				
GXB_L1		GXB_TX_L4n					P1				
GXB_L1		GXB_TX_L4p					P2				
SXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					T2				
SXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					T1				
GXB_L1 GXB_L1		GXB_TX_L3n GXB_TX_L3p					W3 W4				
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					VV4 V2				
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					V1				
SXB_L0		GXB_TX_L2n					AA3				
GXB_L0		GXB_TX_L2p					AA4				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					Y2				
SXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					Y1				
SXB_L0		GXB_TX_L1n					AC3		+		
SXB_L0 SXB_L0		GXB_TX_L1p GXB_RX_L1p,GXB_REFCLK_L1p	+		1	 	AC4 AB2	1	+	1	l .
SXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AB1		+	+	†
SXB_L0		GXB_TX_L0n			1		AE3	1	1		1
SXB_L0		GXB_TX_L0p					AE4				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AD2				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AD1				
SXB_L0		REFCLK0Lp					V6				
SXB_L0		REFCLK0Ln TDO		TDO			W6 V7				
A A		nCSO		DATA4			V7 Y6	1	+		
BA		TMS		TMS			R6				
3A		AS DATA3		DATA3			U6				
3A		TCK		TCK			Y5				
3A		AS_DATA2		DATA2			AB5				
3A		TDI		TDI			T6				
3A		AS_DATA1		DATA1			AD5				
BA		DCLK AS DATA0.ASDO		DCLK DATA0			N8 AF5				
BA	VREFB3AN0	IO		DATA6	DIFFIO RX B1n	DIFFOUT_B1n	T7	DQ1B			
3A	VREFB3AN0	10		DATA5	DIFFIO TX B2n	DIFFOUT B2n	U7	54.5			
3A	VREFB3AN0	IO		DATA8	DIFFIO RX B1p	DIFFOUT B1p	T8	DQ1B			
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	V8	DQ1B			
3A	VREFB3AN0	10		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	W8	DQSn1B			
BA	VREFB3AN0	10		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB6	DQ1B			
BA	VREFB3AN0	10		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	Y9	DQS1B			
BA BA	VREFB3AN0 VREFB3AN0	IO IO	+	DATA11 DATA14	DIFFIO_TX_B4p DIFFIO_RX_B5n	DIFFOUT_B4p DIFFOUT_B5n	AA6 R10	DQ1B	+	1	1
A .	VREFB3AN0	10		DATA13	DIFFIO_RX_BSII	DIFFOUT_B6n	AA7	DQ1B			
A	VREFB3AN0	10		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	R9	DQ1B	1		†
A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	Y8	DQ1B			
A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	R8				
A	VREFB3AN0	10		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AD6	DQ1B	1		
A	VREFB3AN0	10		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	P8	2012	+	1	1
A B	VREFB3AN0 VREFB3BN0	10			DIFFIO_TX_B8p DIFFIO_TX_B9n	DIFFOUT_B8p DIFFOUT_B9n	AD7 U9	DQ1B	+	GND	GND
B B		10			DIFFIO_IX_B9N	DIFFOUT_B90	Y11	DQ2B	+	B_A_15	GIND
В		10			DIFFIO_TX_B10II	DIFFOUT_B9p	T9	DQ2B	†	B_WE#	l .
В		10			DIFFIO_RX_B10p	DIFFOUT_B10p	W11	DQ2B		B_A_14	
В		IO			DIFFIO_RX_B11n	DIFFOUT_B11n	T11	DQSn2B		B_CS#_1	B_CS#_1
В		10			DIFFIO_TX_B12n	DIFFOUT_B12n	AC10	DQ2B		B_A_13	
B		10			DIFFIO_RX_B11p	DIFFOUT_B11p	R11	DQS2B	_	B_CS#_0	B_CS#_0
B		10	<u> </u>		DIFFIO_TX_B12p	DIFFOUT_B12p	AB10	DOOD	+	B_A_12	
BB BB	VREFB3BN0 VREFB3BN0	10			DIFFIO_TX_B13n DIFFIO_RX_B14n	DIFFOUT_B13n DIFFOUT_B14n	AC8 AB11	DQ2B DQ2B	+	B_A_11 B_A_9	B_CA_9
В	VREFB3BN0	IO			DIFFIO_RX_B14II	DIFFOUT_B13p	AC9	DQ2B DQ2B	+	B_A_9 B A 10	D_0A_8
B	VREFB3BN0	10			DIFFIO_RX_B14p	DIFFOUT_B14p	AB12	DQ2B	1	B_A_10	B_CA_8
В	VREFB3BN0	10	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	T12	1	1		
В		IO			DIFFIO_TX_B16n	DIFFOUT_B16n	Y10	DQ2B		B_RAS#	
В	VREFB3BN0		CLK0p,FPLL_BL_FBp	1	DIFFIO_RX_B15p	DIFFOUT_B15p	T13			1	



		T	T								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
an.	VDEEDODNO	IO.			DIFFIG TV DAG-	DIFFOLIT DAG-	1440	DOOD		D CAC#	
3B	VREFB3BN0 VREFB3BN0	10			DIFFIO_TX_B16p DIFFIO_TX_B17n	DIFFOUT_B16p DIFFOUT_B17n	W10 V9	DQ2B		B_CAS# GND	GND
3B	VREFB3BN0	io			DIFFIO_IX_B17II	DIFFOUT_B17/1	AE8	DQ3B		B_BA_2	GIND
3B	VREFB3BN0	10			DIFFIO TX B17p	DIFFOUT B17p	V10	DQ3B		B_BA_0	
3B	VREFB3BN0	10			DIFFIO_RX_B18p	DIFFOUT_B18p	AD8	DQ3B		B_BA_1	
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	P10	DQSn3B		B_CK#	B_CK#
3B		IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AF9	DQ3B		B_A_7	B_CA_7
3B	VREFB3BN0				DIFFIO_RX_B19p	DIFFOUT_B19p	N10	DQS3B		B_CK	B_CK
3B	VREFB3BN0				DIFFIO_TX_B20p	DIFFOUT_B20p	AE9			B_A_6	B_CA_6
3B		10	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AF8	DQ3B	_	B_A_3 B_A_5	B_CA_3 B_CA_5
3B 3B	VREFB3BN0 VREFB3BN0		FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_RX_B22n DIFFIO_TX_B21p	DIFFOUT_B22n DIFFOUT_B21p	U11 AF7	DQ3B DQ3B		B_A_2	B_CA_5
3B		in .	FFLL_BL_CLROUTU,FFLL_BL_CLROUTP,FFLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B22p	U10	DQ3B		B A 4	B CA 4
3B	VREFB3BN0	10	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	P12	DQ3B		D_A_4	D_CA_4
3B	VREFB3BN0		OLANI.		DIFFIO_TX_B24n	DIFFOUT_B24n	AF6	DQ3B		B A 1	B_CA_1
3B		IO	CLK1p		DIFFIO RX B23p	DIFFOUT B23p	P11				
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AE6	DQ3B		B_A_0	B_CA_0
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AE11				
4A	VILLI DIVINO	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	AA14	DQ4B		B_DQ_0	B_DQ_0
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AD11	DQ4B		B_DQ_2	B_DQ_2
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	Y14	DQ4B		B_DQ_1	B_DQ_1
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	W13	DQSn4B		B_DQS#_0	B_DQS#_0
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_TX_B28n	DIFFOUT_B28n	AD12 V13	DQ4B DQS4B		B_DQ_3 B DQS 0	B_DQ_3 B_DQS_0
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_RX_B27p DIFFIO_TX_B28p	DIFFOUT_B27p DIFFOUT_B28p	V13 AD13	DQS4B		B_DQS_0 B_ODT_0	B_ODT_0
4A 4A	VREFB4AN0	In			DIFFIO_TX_B29n	DIFFOUT B29n	AE10	DQ4B		B ODT 1	B ODT 1
4A	VREFB4AN0	in .			DIFFIO RX B30n	DIFFOUT B30n	Y13	DQ4B DQ4B		B DQ 4	B DQ 4
4A	VREFB4AN0	in .			DIFFIO_TX_B29p	DIFFOUT_B29p	AD10	DQ4B		B DQ 6	B DQ 6
4A	VREFB4AN0	10			DIFFIO RX B30p	DIFFOUT B30p	W12	DQ4B		B DQ 5	B DQ 5
4A	VREFB4AN0	10	CLK2n		DIFFIO RX B31n	DIFFOUT_B31n	V12				
4A	VREFB4AN0	10			DIFFIO TX B32n	DIFFOUT B32n	AF12	DQ4B		B DQ 7	B DQ 7
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	U12				
4A	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AF11	DQ4B		B_DM_0	B_DM_0
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AC13			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AC15	DQ5B	DQ1B	B_DQ_8	B_DQ_8
4A	VREFB4AN0	10			DIFFIO_TX_B33p	DIFFOUT_B33p	AC14	DQ5B	DQ1B	B_DQ_10	B_DQ_10
4A	VREFB4AN0	10			DIFFIO_RX_B34p	DIFFOUT_B34p	AB15	DQ5B	DQ1B	B_DQ_9 B_DQS#_1	B_DQ_9 B_DQS#_1
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_RX_B35n DIFFIO_TX_B36n	DIFFOUT_B35n DIFFOUT_B36n	V14 AF13	DQSn5B DQ5B	DQ1B DQ1B	B_DQS#_1 B DQ 11	B_DQS#_1 B DQ 11
4A 4A	VREFB4AN0	10			DIFFIO_TX_B350	DIFFOUT B35p	U14	DQS5B	DQ1B DQ1B	B_DQ_11	B DQS 1
4A 4A	VREFB4AN0	in .			DIFFIO_KX_B35p	DIFFOUT_B35p DIFFOUT_B36p	AE13	DQSSB	DQIB	B CKE 1	B CKE 1
4A	VREFB4AN0	in .			DIFFIO TX B37n	DIFFOUT B37n	AF14	DQ5B	DQ1B	B CKE 0	B CKE 0
4A	VREFB4AN0	IO			DIFFIO RX B38n	DIFFOUT_B38n	AB16	DQ5B	DQ1B	B DQ 12	B DQ 12
4A	VREFB4AN0	10			DIFFIO_TX_B37p	DIFFOUT_B37p	AE14	DQ5B	DQ1B	B_DQ_14	B_DQ_14
4A	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AA16	DQ5B	DQ1B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	Y16				
4A	VREFB4AN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AF18	DQ5B	DQ1B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	Y15	<u> </u>			
4A	VREFB4AN0	10			DIFFIO_TX_B40p	DIFFOUT_B40p	AE18	DQ5B	DQ1B	B_DM_1	B_DM_1
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_TX_B41n	DIFFOUT_B41n	AD18 AD16	DOER	DO4B	GND B DO 16	GND B DQ 16
4A 4A	VREFB4AN0 VREFB4AN0	IO IO			DIFFIO_RX_B42n DIFFIO_TX_B41p	DIFFOUT_B42n DIFFOUT_B41p	AD16 AC18	DQ6B DQ6B	DQ1B DQ1B	B_DQ_16 B_DQ_18	B_DQ_16 B_DQ_18
4A 4A	VREFB4AN0	IO			DIFFIO_TX_B4Tp	DIFFOUT_B41p DIFFOUT_B42p	AD17	DQ6B DQ6B	DQ1B DQ1B	B_DQ_17	B_DQ_18 B DQ 17
4A 4A	VREFB4AN0	IO IO		+	DIFFIO_RX_B42p	DIFFOUT B43n	W15	DQSn6B	DQSn1B	B DQS# 2	B DQS# 2
4A	VREFB4AN0	10			DIFFIO_TX_B44n	DIFFOUT B44n	AF19	DQ6B	DQ1B	B_DQ3#_2 B DQ 19	B DQ 19
4A		10			DIFFIO RX B43p	DIFFOUT B43p	V15	DQS6B	DQS1B	B DQS 2	B DQS 2
4A		10			DIFFIO_TX_B44p	DIFFOUT_B44p	AE19			B_RESET#	B_RESET#
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AF22	DQ6B	DQ1B	GND	GND
4A		IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AC17	DQ6B	DQ1B	B_DQ_20	B_DQ_20
4A		IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AF21	DQ6B	DQ1B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AB17	DQ6B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	U17	<u> </u>		GND	GND
4A	VREFB4AN0	10			DIFFIO_TX_B48n	DIFFOUT_B48n	AE21	DQ6B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	10			DIFFIO_RX_B47p	DIFFOUT_B47p	T17	DOCD	DOAR	GND	GND B. DM 3
4A	VREFB4ANO	10			DIFFIO_TX_B48p	DIFFOUT_B48p	AE20	DQ6B	DQ1B	B_DM_2	B_DM_2
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_TX_B49n DIFFIO_RX_B50n	DIFFOUT_B49n DIFFOUT_B50n	AD20 AE15	DQ7B	DQ2B	GND B DQ 24	GND B DQ 24
4A 4A		IO IO			DIFFIO_TX_B49p	DIFFOUT_B30II DIFFOUT_B49p	AC20	DQ7B DQ7B	DQ2B DQ2B	B_DQ_26	B_DQ_24 B_DQ_26
4A 4A	VREFB4AN0			1	DIFFIO_TX_B49p	DIFFOUT_B50p	AE16	DQ7B DQ7B	DQ2B DQ2B	B_DQ_25	B_DQ_25
4A	vKEFB4AN0	JIO .		1	DIFFIO_KX_B50b	Inition i Ronb	AE16	Ind\R	DUZB	D_UU_25	ש_טע_



		Ta: .:	In the section (a)			Tru/Du Trundets d 1 1/20 0 1 1 1 2		DOS for VS			Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
4A	VREFB4AN0	10			DIFFIO_RX_B51n	DIFFOUT B51n	W17	DQSn7B	DQ2B	B_DQS#_3	B_DQS#_3
4A 4A	VREFB4AN0	io		+	DIFFIO_RX_B51II	DIFFOUT_B51II	AD21	DQ3II7B DQ7B	DQ2B DQ2B	B_DQ3#_3 B DQ 27	B_DQ3#_3 B DQ 27
4A	VREFB4AN0	10			DIFFIO_RX_B51p	DIFFOUT_B51p	W16	DQS7B	DQ2B	B_DQS_3	B_DQS_3
4A	VREFB4AN0	10			DIFFIO_TX_B52p	DIFFOUT_B52p	AD22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AE23	DQ7B	DQ2B	GND	GND
4A	VREFB4AN0				DIFFIO_RX_B54n	DIFFOUT_B54n	AF16	DQ7B	DQ2B	B_DQ_28	B_DQ_28
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AD23	DQ7B	DQ2B	B_DQ_30	B_DQ_30
4A	VREFB4AN0				DIFFIO_RX_B54p	DIFFOUT_B54p	AF17	DQ7B	DQ2B	B_DQ_29	B_DQ_29
4A 4A		10			DIFFIO_RX_B55n DIFFIO_TX_B56n	DIFFOUT_B55n DIFFOUT_B56n	U16 AF23	DO3D	DQ2B	GND B DQ 31	GND B DQ 31
4A 4A		io		+	DIFFIO_IX_B55p	DIFFOUT_B55p	U15	DQ7B	DQ2B	GND	GND
4A		10			DIFFIO_TX_B56p	DIFFOUT_B56p	AE24	DQ7B	DQ2B	B_DM_3	B_DM_3
4A	VREFB4AN0	10			DIFFIO TX B57n	DIFFOUT_B57n	AF24			GND	GND
4A		10			DIFFIO_RX_B58n	DIFFOUT_B58n	AA18	DQ8B	DQ2B	B_DQ_32	B_DQ_32
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AE25	DQ8B	DQ2B	B_DQ_34	B_DQ_34
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	Y18	DQ8B	DQ2B	B_DQ_33	B_DQ_33
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	V17	DQSn8B	DQSn2B	B_DQS#_4	B_DQS#_4
4A 4A	VREFB4AN0	10		+	DIFFIO_TX_B60n	DIFFOUT_B60n	AE26	DQ8B	DQ2B	B_DQ_35	B_DQ_35
4A 4A	VREFB4AN0 VREFB4AN0	10		+	DIFFIO_RX_B59p	DIFFOUT_B59p	V18	DQS8B	DQS2B	B_DQS_4 GND	B_DQS_4 GND
4A 4A	VREFB4AN0 VREFB4AN0	IO IO		+	DIFFIO_TX_B60p DIFFIO_TX_B61n	DIFFOUT_B60p DIFFOUT_B61n	AD26 AC19	DQ8B	DQ2B	GND	GND
4A 4A	VREFB4AN0	IO		†	DIFFIO_IX_B61n DIFFIO_RX_B62n	DIFFOUT_B62n	Y19	DQ8B DQ8B	DQ2B	B_DQ_36	B_DQ_36
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AB19	DQ8B	DQ2B	B_DQ_38	B_DQ_38
4A	VREFB4AN0	IO			DIFFIO RX B62p	DIFFOUT_B62p	Y20	DQ8B	DQ2B	B DQ 37	B DQ 37
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B63n	W18			GND	GND
4A	VREFB4AN0	10			DIFFIO_TX_B64n	DIFFOUT_B64n	AA21	DQ8B	DQ2B	B_DQ_39	B_DQ_39
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B63p	V19			GND	GND
4A	VREFB4AN0	10			DIFFIO_TX_B64p	DIFFOUT_B64p	AB22	DQ8B	DQ2B	B_DM_4	B_DM_4
5A	VREFB5AN0	10	RZQ_1	WIT BOUE	DIFFIO_TX_R1p	DIFFOUT_R1p	AC22	DQ1R			-
5A	VREFB5AN0 VREFB5AN0	10		INIT_DONE PR REQUEST	DIFFIO_RX_R2p DIFFIO_TX_R1n	DIFFOUT_R2p DIFFOUT_R1n	U19 AC23	DQ1R			
5A	VREFB5AN0	io		CRC ERROR	DIFFIO_TX_R1II	DIFFOUT_R2n	V20	DQIK			+
5A	VREFB5AN0	10		nCEO	DIFFIO_TX_R3p	DIFFOUT R3p	AA22	DQ1R			+
5A	VREFB5AN0	IO			DIFFIO RX R4p	DIFFOUT R4p	W20	DQ1R			<u> </u>
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AA23	DQ1R			
5A	VREFB5AN0	10			DIFFIO_RX_R4n	DIFFOUT_R4n	W21	DQ1R			
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AC24				
5A	VREFB5AN0	10		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	V22	DQS1R			
5A	VREFB5AN0	10		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AB24	DQ1R			
5A	VREFB5AN0 VREFB5AN0	10		nPERSTL1	DIFFIO_RX_R6n DIFFIO_TX_R7p	DIFFOUT_R6n DIFFOUT_R7p	U22 Y23	DQSn1R DQ1R	_		
5A	VREFB5AN0	IO			DIFFIO_TX_R/p	DIFFOUT_R8p	T19	DQ1R DQ1R			+
5A	VREFB5AN0	10			DIFFIO_TX_R7n	DIFFOUT_R7n	Y24	DQIII			+
5A	VREFB5AN0	10			DIFFIO RX R8n	DIFFOUT_R8n	U20	DQ1R			†
5B	VREFB5BN0	10	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R9p	DIFFOUT_R9p	T21				
5B	VREFB5BN0	IO			DIFFIO_TX_R10p	DIFFOUT_R10p	V23	DQ2R			
5B	VREFB5BN0	10	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R9n	DIFFOUT_R9n	T22				
5B	VREFB5BN0	IO		ļ	DIFFIO_TX_R10n	DIFFOUT_R10n	V24	DQ2R			
5B	VREFB5BN0	10		+	DIFFIO_RX_R11p	DIFFOUT_R11p	T23	DQ2R	+		
5B	VREFB5BN0	10		+	DIFFIO_TX_R12p DIFFIO_RX_R11n	DIFFOUT_R12p DIFFOUT_R11n	AA24	DQ2R			
5B 5B	VREFB5BN0 VREFB5BN0	IO IO		+	DIFFIO_RX_R11n DIFFIO_TX_R12n	DIFFOUT_R11n DIFFOUT_R12n	T24 AB25	DQ2R DQ2R	+		+
5B	VREFB5BN0	10		+	DIFFIO_IX_R12h	DIFFOUT_R12h	R23	DQ2R DQS2R	+		+
5B	VREFB5BN0	IO		†	DIFFIO TX R14p	DIFFOUT R14p	AD25	2 40211	+		+
5B		10		1	DIFFIO_RX_R13n	DIFFOUT_R13n	P23	DQSn2R	1		†
5B		IO			DIFFIO_TX_R14n	DIFFOUT_R14n	AC25	DQ2R			
5B		IO			DIFFIO_RX_R15p	DIFFOUT_R15p	R24	DQ2R			
5B		Ю			DIFFIO_TX_R16p	DIFFOUT_R16p	U24	DQ2R			
5B		IO		 	DIFFIO_RX_R15n	DIFFOUT_R15n	R25	DQ2R			
5B		10	laura.	+	DIFFIO_TX_R16n	DIFFOUT_R16n	V25		+		+
5B	VREFB5BN0	10	CLK6p	+	DIFFIO_RX_R17p	DIFFOUT_R17p	R20	DOSB			+
5B 5B	VREFB5BN0		CIKEN	+	DIFFIO_TX_R18p	DIFFOUT_R18p	AB26	DQ3R	+		+
5B	VREFB5BN0 VREFB5BN0	10	CLK6n	+	DIFFIO_RX_R17n DIFFIO_TX_R18n	DIFFOUT_R17n DIFFOUT_R18n	P20 AA26	DQ3R	+		+
5B	VREFB5BN0 VREFB5BN0	IO IO		+	DIFFIO_IX_R18h	DIFFOUT_R18h DIFFOUT_R19p	T26	DQ3R DQ3R	+		+
5B	VREFB5BN0	10	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB	1	DIFFIO_TX_R20p	DIFFOUT_R20p	Y25	DQ3R	1		<u> </u>
5B	VREFB5BN0	10		1	DIFFIO_RX_R19n	DIFFOUT_R19n	R26	DQ3R	1		
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R20n	DIFFOUT_R20n	Y26	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	P21	DQS3R			



				1 T		Ty/Dy Emulated LVDS Output Charact		D00 (V0 D00 (V40			Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
iB	VREFB5BN0	10			DIFFIO_TX_R22p	DIFFOUT_R22p	W25				
B B	VREFB5BN0 VREFB5BN0	10			DIFFIO_RX_R21n DIFFIO_TX_R22n	DIFFOUT_R21n DIFFOUT_R22n	P22 W26	DQSn3R DQ3R			
B B		lio			DIFFIO_IX_R22h DIFFIO_RX_R23p	DIFFOUT_R22n DIFFOUT_R23p	N25	DQ3R DQ3R			+
iB		10			DIFFIO_TX_R24p	DIFFOUT_R24p	U25	DQ3R			+
iB	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	P26	DQ3R			
iВ	VREFB5BN0	10			DIFFIO_TX_R24n	DIFFOUT_R24n	U26				
iA iA	VREFB6AN0 VREFB6AN0	10	CLK5p		DIFFIO_RX_R25p	DIFFOUT_R25p DIFFOUT_R26p	N20	2012			
iA iA	VREFB6AN0 VREFB6AN0	IIO	CLK5n		DIFFIO_TX_R26p DIFFIO_RX_R25n	DIFFOUT_R25p DIFFOUT_R25n	J25 M21	DQ4R			+
SA SA	VREFB6AN0	10	CEROII		DIFFIO TX R26n	DIFFOUT R26n	J26	DQ4R			1
SA.	VREFB6AN0	Ю			DIFFIO_RX_R27p	DIFFOUT_R27p	N24	DQ4R			
SA.	VREFB6AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB		DIFFIO_TX_R28p	DIFFOUT_R28p	F26	DQ4R]
SA.	VREFB6AN0	IO	EDIL TO OLYGUT EDIL TO OLYGUT		DIFFIO_RX_R27n	DIFFOUT_R27n	M24	DQ4R			
iA iA	VREFB6AN0 VREFB6AN0	10	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_R28n DIFFIO_RX_R29p	DIFFOUT_R28n DIFFOUT_R29p	G26 N23	DQ4R DQS4R			
SA SA		lio			DIFFIO_RX_R29p DIFFIO_TX_R30p	DIFFOUT_R30p	G25	DQ54R			+
6A	VREFB6AN0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	M22	DQSn4R			1
6A	VREFB6AN0	10			DIFFIO_TX_R30n	DIFFOUT_R30n	H25	DQ4R			
SA .	VREFB6AN0				DIFFIO_RX_R31p	DIFFOUT_R31p	M25	DQ4R			
SA.	VREFB6AN0	10			DIFFIO_TX_R32p	DIFFOUT_R32p	D26	DQ4R			
6A		10			DIFFIO_RX_R31n DIFFIO_TX_R32n	DIFFOUT_R31n DIFFOUT_R32n	M26 E26	DQ4R			+
6A	VREFB6AN0	10	CLK4p,FPLL_TR_FBp		DIFFIO_TX_R32II	DIFFOUT_R33p	K25				+
6A	VREFB6AN0	IO	OEX ID, I TEE_ING I DP		DIFFIO_TX_R34p	DIFFOUT_R34p	E24	DQ5R			1
6A	VREFB6AN0	10	CLK4n,FPLL_TR_FBn		DIFFIO_RX_R33n	DIFFOUT_R33n	K26				
6A	VREFB6AN0	IO			DIFFIO_TX_R34n	DIFFOUT_R34n	E25	DQ5R			
6A	VREFB6AN0	10			DIFFIO_RX_R35p	DIFFOUT_R35p	K24	DQ5R			
6A	VREFB6AN0 VREFB6AN0	10			DIFFIO_TX_R36p DIFFIO_RX_R35n	DIFFOUT_R36p DIFFOUT_R35n	F24 K23	DQ5R DQ5R			
6A	VREFB6AN0 VREFB6AN0	10			DIFFIO_RX_R35n DIFFIO_TX_R36n	DIFFOUT_R35n DIFFOUT_R36n	G24	DQ5R DQ5R			+
6A	VREFB6AN0	10			DIFFIO_RX_R37p	DIFFOUT_R37p	L23	DQS5R			+
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R38p	H23				1
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R37n	L24	DQSn5R			
6A	VREFB6AN0	10			DIFFIO_TX_R38n	DIFFOUT_R38n	H24	DQ5R			
6A	VREFB6AN0 VREFB6AN0	10			DIFFIO_RX_R39p DIFFIO_TX_R40p	DIFFOUT_R39p DIFFOUT_R40p	H22 F23	DQ5R DQ5R			-
6A	VREFB6AN0 VREFB6AN0	lio			DIFFIO_IX_R40p DIFFIO_RX_R39n	DIFFOUT_R40p DIFFOUT_R39n	J23	DQ5R DQ5R			+
6A	VREFB6AN0	10			DIFFIO_TX_R40n	DIFFOUT R40n	G22	DQSK			+
6A	VREFB6AN0	IO			DIFFIO RX R41p	DIFFOUT_R41p	L22				1
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R42p	B25	DQ6R			
6A	VREFB6AN0	10			DIFFIO_RX_R41n	DIFFOUT_R41n	K21				
6A	VREFB6AN0	10			DIFFIO_TX_R42n	DIFFOUT_R42n	B26	DQ6R			
6A 6A	VREFB6AN0 VREFB6AN0	10			DIFFIO_RX_R43p DIFFIO_TX_R44p	DIFFOUT_R43p DIFFOUT_R44p	H19 D25	DQ6R DQ6R			+
6A		IO			DIFFIO RX R43n	DIFFOUT R43n	H20	DQ6R			1
6A		10			DIFFIO_TX_R44n	DIFFOUT_R44n	C25	DQ6R			1
6A		IO			DIFFIO_RX_R45p	DIFFOUT_R45p	J20	DQS6R			
6A	VREFB6AN0	10			DIFFIO_TX_R46p	DIFFOUT_R46p	D22	D00-02	_		4
6A	VREFB6AN0 VREFB6AN0	10			DIFFIO_RX_R45n	DIFFOUT_R45n	J21	DQSn6R			
6A	VREFB6AN0	10			DIFFIO_TX_R46n DIFFIO_RX_R47p	DIFFOUT_R46n DIFFOUT_R47p	E23 G20	DQ6R DQ6R			+
6A	VREFB6AN0	10			DIFFIO_TX_R48p	DIFFOUT_R48p	E21	DQ6R			+
6A	VREFB6AN0	10			DIFFIO_RX_R47n	DIFFOUT_R47n	F21	DQ6R			1
6A	VREFB6AN0	IO			DIFFIO_TX_R48n	DIFFOUT_R48n	F22				
7A	l	GND			L	<u> </u>	D23	ļ		OND	OND
7A 7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T1p DIFFIO_TX_T2p	DIFFOUT_T1p DIFFOUT_T2p	H15	DQ1T	DQ1T	GND T DM 4	GND T DM 4
7A 7A	VREFB7AN0 VREFB7AN0	lio		+	DIFFIO_IX_I2p	DIFFOUT_12p DIFFOUT_T1n	J16	ואַעוו	DQTI	GND	GND
7A	VREFB7AN0	10		+	DIFFIO_TX_T2n	DIFFOUT_T2n	C22	DQ1T	DQ1T	T DQ 39	T DQ 39
7A	VREFB7AN0	10			DIFFIO_RX_T3p	DIFFOUT_T3p	B24	DQ1T	DQ1T	T_DQ_37	T_DQ_37
7A	VREFB7AN0	Ю			DIFFIO_TX_T4p	DIFFOUT_T4p	A23	DQ1T	DQ1T	T_DQ_38	T_DQ_38
7A	VREFB7AN0	10			DIFFIO_RX_T3n	DIFFOUT_T3n	A24	DQ1T	DQ1T	T_DQ_36	T_DQ_36
7A	VREFB7ANO	10			DIFFIO_TX_T4n	DIFFOUT_T4n	A22	DQ1T	DQ1T	GND T DOC 4	GND T DOC 4
7A 7A	VREFB7AN0 VREFB7AN0	lio			DIFFIO_RX_T5p DIFFIO_TX_T6p	DIFFOUT_T5p DIFFOUT_T6p	H18 B22	DQS1T	DQS1T	T_DQS_4 GND	T_DQS_4 GND
7A	VREFB7AN0 VREFB7AN0	lio		+	DIFFIO_TX_T6p DIFFIO_RX_T5n	DIFFOUT_T5n	H17	DQSn1T	DQSn1T	T_DQS#_4	T_DQS#_4
7A	VREFB7AN0	Ю		1	DIFFIO_TX_T6n	DIFFOUT_T6n	A21	DQ1T	DQ1T	T_DQ_35	T_DQ_35
7A	VREFB7AN0	10			DIFFIO_RX_T7p	DIFFOUT_T7p	D21	DQ1T	DQ1T	T_DQ_33	T DQ 33



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
										7.00.01	T 20 01
7A 7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_TX_T8p DIFFIO_RX_T7n	DIFFOUT_T8p DIFFOUT_T7n	B21 D20	DQ1T DQ1T	DQ1T DQ1T	T_DQ_34 T DQ 32	T_DQ_34 T_DQ_32
7A 7A	VREFB7AN0	io			DIFFIO_RX_17h	DIFFOUT_17h DIFFOUT_T8n	B20	DQTI	DQTI	GND	GND
7A	VREFB7AN0	10			DIFFIO_RX_T9p	DIFFOUT_T9p	G16			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	C20	DQ2T	DQ1T	T_DM_3	T_DM_3
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	G17			GND	GND
7A	VREFB7AN0	10			DIFFIO_TX_T10n	DIFFOUT_T10n DIFFOUT_T11p	B19	DQ2T DQ2T	DQ1T DQ1T	T_DQ_31 T_DQ_29	T_DQ_31 T_DQ_29
7A 7A	VREFB7AN0 VREFB7AN0	10 10			DIFFIO_RX_T11p DIFFIO_TX_T12p	DIFFOUT_T12p	E20 C19	DQ2T DQ2T	DQ1T DQ1T	T_DQ_29	T DQ_29
7A	VREFB7AN0	10			DIFFIO RX T11n	DIFFOUT_T11n	E19	DQ2T	DQ1T	T DQ 28	T DQ 28
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	C18	DQ2T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	J12	DQS2T	DQ1T	T_DQS_3	T_DQS_3
7A	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	A19			GND	GND
7A 7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T13n DIFFIO_TX_T14n	DIFFOUT_T13n DIFFOUT_T14n	J11 A18	DQSn2T DQ2T	DQ1T DQ1T	T_DQS#_3 T_DQ_27	T_DQS#_3 T_DQ_27
7A	VREFB7AN0	io			DIFFIO_TX_T14II	DIFFOUT_T15p	D18	DQ2T	DQ1T	T DQ 25	T DQ 25
7A	VREFB7AN0	10			DIFFIO_TX_T16p	DIFFOUT_T16p	A17	DQ2T	DQ1T	T_DQ_26	T_DQ_26
7A	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	D17	DQ2T	DQ1T	T_DQ_24	T_DQ_24
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A16			GND	GND
7A	VREFB7AN0	10		ļ	DIFFIO_RX_T17p	DIFFOUT_T17p	H14	B007	2007	GND	GND
7A 7A	VREFB7AN0	10			DIFFIO_TX_T18p	DIFFOUT_T18p	C17 H13	DQ3T	DQ2T	T_DM_2 GND	T_DM_2 GND
7A 7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T17n DIFFIO_TX_T18n	DIFFOUT_T17n DIFFOUT_T18n	B17	DQ3T	DQ2T	T_DQ_23	T DQ 23
7A	VREFB7AN0	10			DIFFIO RX T19p	DIFFOUT T19p	F18	DQ3T	DQ2T	T DQ 21	T DQ 21
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	A14	DQ3T	DQ2T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	F18	DQ3T	DQ2T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	B14	DQ3T	DQ2T	GND	GND
7A 7A	VREFB7AN0	10			DIFFIO_RX_T21p	DIFFOUT_T21p	L12 B15	DQS3T	DQS2T	T_DQS_2 T_RESET#	T_DQS_2 T_RESET#
7A 7A	VREFB7AN0 VREFB7AN0	IO IO			DIFFIO_TX_T22p DIFFIO_RX_T21n	DIFFOUT_T22p DIFFOUT_T21n	K11	DQSn3T	DQSn2T	T DQS# 2	T DQS# 2
7A	VREFB7AN0	io			DIFFIO_RX_121II	DIFFOUT_T22n	C15	DQ3T3T	DQ3H21	T DQ 19	T_DQ3#_2 T_DQ_19
7A	VREFB7AN0	10			DIFFIO_RX_T23p	DIFFOUT_T23p	C14	DQ3T	DQ2T	T DQ 17	T DQ 17
7A	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A8	DQ3T	DQ2T	T_DQ_18	T_DQ_18
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D15	DQ3T	DQ2T	T_DQ_16	T_DQ_16
7A 7A	VREFB7AN0	10	0.1744		DIFFIO_TX_T24n	DIFFOUT_T24n	A9			GND	GND
7A 7A	VREFB7AN0 VREFB7AN0	10	CLK11p		DIFFIO_RX_T25p DIFFIO_TX_T26p	DIFFOUT_T25p DIFFOUT_T26p	G15 C9	DQ4T	DQ2T	T DM 1	T DM 1
7A	VREFB7AN0	IO .	CLK11n		DIFFIO_TX_T26p	DIFFOUT T25n	G14	DQ41	DQZI	I_DIVI_I	I_DIVI_I
7A	VREFB7AN0	10	OLA THE		DIFFIO_TX_T26n	DIFFOUT_T26n	B9	DQ4T	DQ2T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	E16	DQ4T	DQ2T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	D10	DQ4T	DQ2T	T_DQ_14	T_DQ_14
7A 7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T27n	DIFFOUT_T27n DIFFOUT_T28n	D16	DQ4T DQ4T	DQ2T DQ2T	T_DQ_12 T CKE 0	T_DQ_12 T CKE 0
7A 7A	VREFB7AN0	10			DIFFIO_TX_T28n DIFFIO_RX_T29p	DIFFOUT_T29p	C10 N12	DQ41 DQS4T	DQ2T DQ2T	T DQS 1	T DQS 1
7A	VREFB7AN0	10			DIFFIO_TX_T30p	DIFFOUT T30p	B10	DQ341	DQZI	T CKE 1	T CKE 1
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	M12	DQSn4T	DQ2T	T_DQS#_1	T_DQS#_1
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A11	DQ4T	DQ2T	T_DQ_11	T_DQ_11
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	F16	DQ4T	DQ2T	T_DQ_9	T_DQ_9
7A 7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_TX_T32p DIFFIO_RX_T31n	DIFFOUT_T32p DIFFOUT_T31n	E10 E15	DQ4T DQ4T	DQ2T DQ2T	T_DQ_10 T DQ 8	T_DQ_10 T_DQ_8
7A 7Δ	VREFB7AN0	IO IO			DIFFIO_TX_T32n	DIFFOUT_T32n	F11	DQ41	DQZ1	GND	GND
7A	VREFB7AN0	10	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H12			OND	CIND
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	B12	DQ5T		T_DM_0	T_DM_0
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G11				
7A	VREFB7AN0	10		ļ	DIFFIO_TX_T34n	DIFFOUT_T34n	A13	DQ5T		T_DQ_7	T_DQ_7
7A 7A	VREFB7AN0 VREFB7AN0	10		 	DIFFIO_RX_T35p DIFFIO_TX_T36p	DIFFOUT_T35p DIFFOUT_T36p	G12 A12	DQ5T DQ5T		T_DQ_5 T DQ 6	T_DQ_5 T DQ 6
7A 7A	VREFB7AN0	10			DIFFIO_TX_T36p	DIFFOUT_136p DIFFOUT_T35n	F12	DQ5T DQ5T	+	T DQ_6	T DQ 4
7A	VREFB7AN0	10		1	DIFFIO_TX_T36n	DIFFOUT_T36n	B11	DQ5T	Ì	T_ODT_1	T_ODT_1
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	M11	DQS5T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	C13			T_ODT_0	T_ODT_0
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	L11	DQSn5T		T_DQS#_0	T_DQS#_0
7A 7A	VREFB7AN0	10		 	DIFFIO_TX_T38n	DIFFOUT_T38n	C12	DQ5T		T_DQ_3 T_DQ_1	T_DQ_3 T_DQ_1
7A 7A	VREFB7AN0 VREFB7AN0	IO IO		 	DIFFIO_RX_T39p DIFFIO_TX_T40p	DIFFOUT_T39p DIFFOUT_T40p	E13	DQ5T DQ5T	1	T DQ_1	T DQ 2
7A	VREFB7AN0	10		<u> </u>	DIFFIO_TX_140p	DIFFOUT_T39n	D13	DQ5T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	D12				1
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	N9				
8A	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	A5	DQ6T		T_A_0	T_CA_0





			T	To a							Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
8A	VREFB8AN0	10	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	M10				+
8A		10	CERSII		DIFFIO_RX_141II	DIFFOUT_T41II	B6	DQ6T		T A 1	T CA 1
8A		IO			DIFFIO_RX_T43p	DIFFOUT_T43p	H8	DQ6T		T_A_4	T_CA_4
8A		10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	A7	DQ6T		T_A_2	T_CA_2
8A		IO			DIFFIO_RX_T43n	DIFFOUT_T43n	H9	DQ6T		T_A_5	T_CA_5
8A		10	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	B7	DQ6T		T_A_3	T_CA_3
8A		10			DIFFIO_RX_T45p	DIFFOUT_T45p	M9	DQS6T		T_CK	T_CK
8A		10			DIFFIO_TX_T46p	DIFFOUT_T46p	D6	BOO 07		T_A_6	T_CA_6
8A 8A	VREFB8AN0 VREFB8AN0	10		+	DIFFIO_RX_T45n DIFFIO_TX_T46n	DIFFOUT_T45n DIFFOUT_T46n	L9 E6	DQSn6T DQ6T		T_CK# T A 7	T_CK# T_CA_7
8A	VREFB8AN0	10			DIFFIO_TX_T46II	DIFFOUT_T47p	H10	DQ6T		T_BA_1	I_CA_/
8A		IO			DIFFIO_TX_T48p	DIFFOUT_T48p	D7	DQ6T		T_BA_0	+
8A	VREFB8AN0	IO			DIFFIO RX T47n	DIFFOUT_T47n	G10	DQ6T		T_BA_2	
8A	VREFB8AN0	10			DIFFIO_TX_T48n	DIFFOUT_T48n	C7			GND	GND
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	L8				
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	F6	DQ7T		T_CAS#	
8A	VREFB8AN0	10	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	К9				
8A	VREFB8AN0	10		1	DIFFIO_TX_T50n	DIFFOUT_T50n	G6	DQ7T		T_RAS#	T CA 2
8A 8A	VREFB8ANO	10			DIFFIO_RX_T51p	DIFFOUT_T51p	K8 G7	DQ7T		T_A_8	T_CA_8
8A 8A	VREFB8AN0 VREFB8AN0	lio	+	1	DIFFIO_TX_T52p DIFFIO_RX_T51n	DIFFOUT_T52p DIFFOUT_T51n	J8	DQ7T DQ7T	+	T_A_10 T_A_9	T CA 9
8A	VREFB8AN0	lio			DIFFIO_RX_151h DIFFIO_TX_T52h	DIFFOUT_T52n	J8 F7	DQ7T	+	T_A_9	1_0/_0
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	K10	DQS7T		T_CS#_0	T CS# 0
8A	VREFB8AN0	IO			DIFFIO TX T54p	DIFFOUT_T54p	H7			T A 12	1
8A	VREFB8AN0	10			DIFFIO_RX_T53n	DIFFOUT_T53n	J10	DQSn7T		T_CS#_1	T_CS#_1
8A	VREFB8AN0	10			DIFFIO_TX_T54n	DIFFOUT_T54n	J7	DQ7T		T_A_13	
8A	VREFB8AN0	10			DIFFIO_RX_T55p	DIFFOUT_T55p	L7	DQ7T		T_A_14	
8A	VREFB8AN0	10			DIFFIO_TX_T56p	DIFFOUT_T56p	D8	DQ7T		T_WE#	
8A	VREFB8AN0	10			DIFFIO_RX_T55n	DIFFOUT_T55n	K6	DQ7T		T_A_15	ON ID
9A	VREFB8AN0	IO MSEL0		MSEL0	DIFFIO_TX_T56n	DIFFOUT_T56n	E9 M7			GND	GND
9A		CONF DONE		CONF DONE			A6				+
9A		MSEL1		MSEL1			L6				+
9A		nSTATUS		nSTATUS			B5				
9A		nCE		nCE			D5				
9A		MSEL2		MSEL2			A2				
9A		MSEL3		MSEL3			K5				
9A		nCONFIG		nCONFIG			F5				
9A 9A		MSEL4		MSEL4			J5 H5				
9A	-	GND GND		+			V26	-		_	
		GND					A25				+
		GND					D24				
		GND					H26				1
		GND					L25				
		GND					P24				
		GND		-		<u> </u>	AA25				4
	1	GND	+	1	+	+	AC26	+	+	-	+
	-	GND GND			+		AF25 G23	 	+		+
	1	GND			1	<u> </u>	K22	+			+
	<u> </u>	GND			<u> </u>	<u> </u>	U23	<u>† </u>	+		+
	t	GND		1	†	†	Y22	†	+		†
		GND					AD24				1
		GND					C21				
		GND					F20				
		GND					L20	<u> </u>			1
	-	GND		1	+		K19	+			+
	1	GND	+	1	+	+	N21	+	+	-	+
	 	GND GND		+	+	+	M19	+	+		+
	 	GND	+	1	+	<u> </u>	T20 P19	+	+		+
	1	GND			+	†	W19	†	+		+
		GND		1	+	<u> </u>	AC21	 			+
		GND					AF20	1		İ	1
		GND					B18				
		GND					E17				
		GND					L18	1			1
		GND		1			K17				<u> </u>





											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					J18				†
		GND					N18			ļ	
		GND GND					M17 R18			+	+
		GND					P17			†	+
		GND					AB18			1	†
		GND					AE17				
		GND					A15				
		GND GND				+	D14 H16			1	+
		GND					L16			1	+
		GND					L14				
		GND					K15				
		GND GND					J14 N16			+	+
		GND					N14			+	+
		GND					M15				1
		GND					T15				
		GND		ļ	ļ		R16	ļ	<u> </u>		
		GND GND		+	+	-	R14 P15	1	1	+	+
		GND					V16	1		+	+
		GND					AA15		İ	†	<u>† </u>
		GND					AD14				1
		GND					G13				
		GND GND					K13 K12			-	+
		GND					M13				+
		GND					R12				1
		GND					P13				
		GND					U13				
		GND GND				-	Y12 C11			+	+
		GND					F10				+
		GND					L10				1
		GND					J9				
		GND GND					N11 T10			+	+
		GND					P9			+	+
		GND					W9			1	†
		GND					AC11				
		GND					AF10				
		GND GND					B8 E7			-	+
		GND					H6				+
		GND					N6				1
		GND					M8				
		GND				 	R7	1		+	+
		GND GND				+	P7 AB8	1	1	+	+
		GND					AE7			1	
		GND					C5				1
		GND					B4			1	1
		GND GND					F4	<u> </u>	1	+	+
	 	GND				1	E5 D4	1	1	+	+
		GND					H4			1	1
		GND					G5				
		GND					L4			<u> </u>	<u> </u>
		GND GND					J4 N4	1	1	1	+
	 	GND				1	M5	1	1	+	+
		GND					T5			1	1
		GND					R4				
		GND					P5	ļ			<u> </u>
	1	GND				 	V5	 	1	+	+
	 	GND GND				1	V4 U4	1	1	+	+
		GND					AA5	<u> </u>	<u> </u>		





											NOIE (1
Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin	HMC Pin
Number					Channel					Assignment for	Assignment for
										DDR3/DDR2 (2)	LPDDR2
	1	GND			+		Y4			+	+
	<u> </u>	GND			+		W5	+		+	+
		GND					AC5				+
		GND					AB4			+	+
	-	GND		+			AF4				+
	-	GND		+			AE5				+
	-	GND		+			AD4				+
	1	GND					C2				+
	1	GND					C1				+
	<u> </u>	GND			+		B3	+		+	+
	1	GND					B2				+
	1	GND					F3				+
	1	GND			+		E2			+	+
	1	GND			+		E1			+	+
		GND			+		D3		+	+	+
		GND			+		H3		+	+	+
					+				+	+	+
	1	GND GND			+	 	G2 G1	 	+	+	+
	 	GND		+	 	 	L2	 		+	+
	}		+	+	+	+		 	+	+	+
	}	GND	+	+	+	+	L1	 	+	+	+
	 	GND		+	+	+	K3 J2	 	+	+	+
	ļ	GND		+				-			+
	 	GND GND		+	 	 	J1	 		+	+
	1	GND		+	+	 	N2	 	+	+	+
							N1			_	
		GND					M3 T3			_	+
		GND					13			_	+
		GND					R2 R1				4
		GND					R1				4
		GND					P3				
		GND					V3				
		GND					U2				
		GND			<u> </u>		U1				
		GND					AA2				
		GND					AA1				
		GND					Y3				
		GND					W2				
		GND			<u> </u>		W1				
		GND					AC2				
		GND					AC1				
		GND					AB3				
		GND					AF3				
		GND					AF2				
		GND					AE2				
		GND					AE1				
	1	GND			1		AD3	ļ		1	_
	1	VCC			<u> </u>		K20	1	1	1	
	1	VCC			<u> </u>		L19	1	1	1	
		VCC				1	J19				
		VCC					N19				
		VCC					M20				1
		VCC					R19				
		VCC					L17				
		VCC					K18				
		VCC					J17				
		VCC					N17				
		VCC					M18				
		VCC					T18				
		VCC					R17				
		VCC					P18				
		VCC					L15				
		VCC					K16				
		VCC					K14				
		VCC					J15	1		1	1
	Ì	VCC					N15				1
	1	VCC					M16	İ	İ	İ	1
	İ	VCC					M14				1
	Ì	VCC					T16				1
		VCC		•	1	†	T14	1	1	1	+





											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		VCC					R15				1
		VCC					P16				_
	-	VCC VCC					P14 L13	-	_		+
		VCC					J13				+
		VCC					N13				†
		VCC					R13				T
		DNU					A4				<u> </u>
		DNU DNU			_		A3 C24				+
		DNU					F14				+
		VCCPGM					AA9				†
		VCCPGM					W22				
		VCCPGM					F8				
		VCCBAT					E8				4
	-	VCCIO3A VCCIO3A			+	+	Y7 AC6				+
	<u> </u>	VCCIO3A VCCIO3B			1	+	U8	+	+	+	+
		VCCIO3B			1		V11	1	1		1
		VCCIO3B					AA10				
		VCCIO3B					AD9	1			
	-	VCCIO4A VCCIO4A			+	+	U18 AE22	+	+	1	+
		VCCIO4A VCCIO4A				+	AE22 AA20				+
		VCCIO4A VCCIO4A					AD19				+
		VCCIO4A					Y17				1
		VCCIO4A					W14				
		VCCIO4A					AC16				
		VCCIO4A VCCIO4A					AF15 AB13			_	
		VCCIO4A VCCIO4A					AE12				+
		VCCIO5A					V21				†
		VCCIO5A					AB23				
		VCCIO5B					N26				
		VCCIO5B					T25				4
		VCCIO5B VCCIO5B				+	W24 R22				+
		VCCIOSB VCCIO6A					C26				+
		VCCIO6A					F25				1
		VCCIO6A					J24				
		VCCIO6A					E22				4
	-	VCCIO6A VCCIO6A					M23 H21	-	_		+
	+	VCCIO7A					A10				+
		VCCIO7A					B23				1
		VCCIO7A					A20				
		VCCIO7A					D19				
	1	VCCIO7A VCCIO7A		+	+	+	G18 C16	+	+	-	+
		VCCIO7A VCCIO7A			+	+	F15	1	+		+
		VCCIO7A VCCIO7A			1		B13	1	1		1
		VCCIO7A					E12				
		VCCIO7A		_			H11				1
		VCCIO8A			+	+	C6	1	+		4
	+	VCCIO8A VCCIO8A			+	+	D9 G8	+	+		+
	+	VCCIOSA VCCIOSA			+	+	K7	+	+		+
		VCCPD3A			<u> </u>		AB9				<u>† </u>
		VCCPD3B4A					AB21				
		VCCPD3B4A					AA19				
	-	VCCPD3B4A			+	+	AA17	+	+	1	+
		VCCPD3B4A VCCPD3B4A			+	+	AA13 AA11	1	+		+
		VCCPD5A			1		U21		1		1
		VCCPD5B					N22	1			1
		VCCPD5B					R21				
		VCCPD6A			-		J22	1			+
	-	VCCPD6A VCCPD7A8A		+	+	+	L21 F19	+	+	+	+
		VOCEDIAGA	1		1	1	1719			1	



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
	-	VCCPD7A8A					F17				
		VCCPD7A8A					F13		+		
		VCCPD7A8A					F11		+		
		VCCPD7A8A					F9				
3A	VREER3ANO	VREFB3AN0					AC7		+		
3B	VREFB3BN0			†			AC12				
4A	VREFB4AN0	VPEERANIO		†			AD15				
5A	VREFB5AN0	VREERSANO					W23		+		
5B	VREFB5BN0			†			P25				
6A	VREFB6AN0	VPEERGANO		†			L26				
7A	VREFB7AN0	VPEER7ANO		†			B16				
BA	VREFB8AN0	VREERSANO					C8		+		
U/ (VICEI DOMINO	NC		†			AA12				
	-	NC NC	1		-	†	M6	1	+	+	1
		NC NC				 	AB7	+	+	+	
	 	NC NC				 	C4	+	+	+	
	-	NC NC	1		-	†	E4	1	+	+	1
		NC					G4				
		NC		†			L5				
		NC		†			C3				
		NC		†			F2				
		NC					F1				
		NC					E3				
		NC NC		1			D2				
		NC NC		1			D1				
		NC		1			H2				
		NC NC		1			H1				
		NC NC					G3		+		
		VCCH_GXBL		1			R3				
		VCCH GXBL		1			T4				
		VCCH_GXBL		1			L3				
		VCCL GXBL					J3		+		
		VCCL GXBL		1			N3				
		VCCL_GXBL		1			U3				
		RREF_TL		†			B1				
		VCCA_FPLL		1			W7				
	1	VCCA_FFLL VCCA FPLL				†	J6	+	+	+	1
	 	VCCA_FPLL VCCA_FPLL				 	Y21	+	+	+	
	-	VCCA_FPLL VCCA_FPLL	1		-	†	G21	1	+	+	1
		VCC AUX				†	G9	+	+	+	1
		VCC_AUX	1		-	†	E14	1	+	+	1
		VCC_AUX			-	†	G19	1	+	+	1
	1	VCC_AUX				†	AB20	+	+	+	1
	-	VCC_AUX			-	†	AB14	1	+	+	1
	-	VCC_AUX			-	†	AA8	1	+	+	1
	t	VCCE GXBL				†	K4	†	+	+	1
		VCCE_GXBL				1	N5	+	+	+	
		VCCE_GXBL				†	M4	+	+	+	1
		VCCE_GXBL VCCE_GXBL				†	R5	+	+	+	1
		VCCE_GXBL				†	P4	+	+	+	1
		VCCE_GXBL		 		+	U5	+	+	-	

Notes:

(1) For more information about pin definition and pin connection guidelines, refer to the

Cyclone V Device Family Pin Connection Guidelines.

(2) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone[®] V 5CGXFC5 Device Version 1.2

Version Number	Date	Changes Made
1.0	11/29/2012	Initial release.
1.1	4/26/2013	 - Added M301 package. - Updated the column from "HMC Pin Assignment for DDR3" to "HMC Pin Assignment for DDR3/DDR2". - Added note to the "HMC Pin Assignment for DDR3/DDR2" column.
1.2	7/4/2013	Added M383 package.