

# TXS0108E面向开漏和推挽应用的 8 位双向电压电平转换 应用

## 1 特性

- 无需方向控制信号
- 最大数据速率
  - 110Mbps (推挽)
  - 1.2Mbps (开漏)
- A 端口 1.2V 至 3.6V; B 端口 1.65V 至 5.5V ( $V_{CCA} \leq V_{CCB}$ )
- 无需电源定序 -  $V_{CCA}$  或  $V_{CCB}$  均可优先斜升
- 锁断性能超过 100mA, 符合 JESD 78 II 类规范的要求
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求 (A 端口)
  - 2000V 人体放电模型 (A114-B)
  - 150V 机器模型 (A115-A)
  - 1000V 充电器件模型 (C101)
- IEC 61000-4-2 ESD (B 端口)
  - $\pm 8\text{kV}$  接触放电
  - $\pm 6\text{kV}$  气隙放电

## 2 应用

- 手持终端
- 智能电话
- 平板电脑
- 台式计算机

## 3 说明

这款 8 位非反向转换器使用两个独立的可配置电源轨。A 端口跟踪  $V_{CCA}$  引脚的电源电压。 $V_{CCA}$  引脚可接受 1.2V 到 3.6V 范围内的任意电源电压。B 端口跟踪  $V_{CCB}$  引脚的电源电压。 $V_{CCB}$  引脚可接受 1.65V 到 5.5V 范围内的任意电源电压。这两个输入电源引脚可实现 1.2V、1.8V、2.5V、3.3V 和 5V 电压节点之间的任意低压双向转换。

输出使能 (OE) 输入为低电平时, 所有输出均将置于高阻抗 (Hi-Z) 状态。

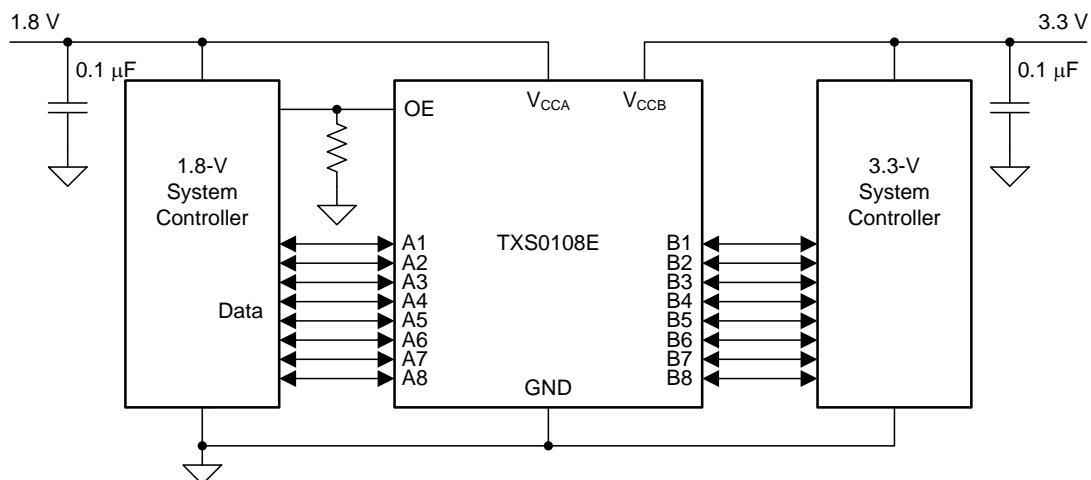
为确保输出在上电或断电期间处于 Hi-Z 状态, 需通过一个下拉电阻将 OE 接至 GND。该电阻的最小值取决于驱动器的拉电流能力。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TXS0108EPW	TSSOP (20)	6.50mm x 6.40mm
TXS0108ERGY	VQFN (20)	4.50mm x 3.50mm
TXS0108EZXY	UFBGA (20)	3.00mm x 2.50mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

简化应用



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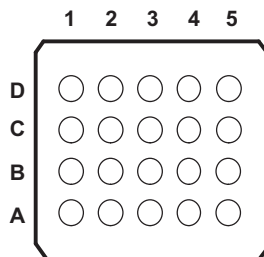
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## 4 修订历史记录

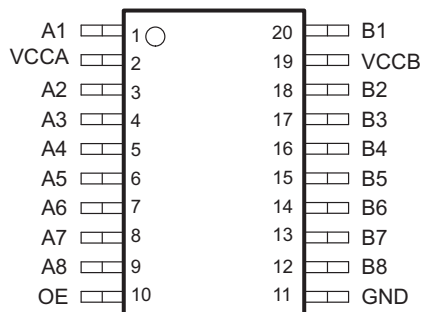
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## 5 Pin Configuration and Functions

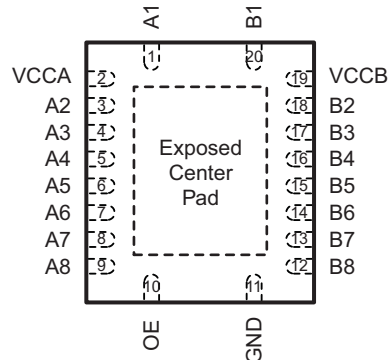
**ZXY PACKAGE  
20 BUMP  
(BOTTOM VIEW)**



**PW PACKAGE  
20-PIN TSSOP  
(TOP VIEW)**



**RGY PACKAGE  
20 PINS  
(TOP VIEW)**



The exposed center pad, if used, must be connected as a secondary ground or left electrically open.

**Table 1. Pin Assignments**

	1	2	3	4	5
<b>D</b>	VCCB	B2	B4	B6	B8
<b>C</b>	B1	B3	B5	B7	GND
<b>B</b>	A1	A3	A5	A7	OE
<b>A</b>	VCCA	A2	A4	A6	A8

### Pin Functions

PIN NO.			TYPE <sup>(1)</sup>	DESCRIPTION
NAME	PW, RGY	ZXY		
A1	1	B1	I/O	Input/output 1. Referenced to $V_{CCA}$
A2	3	A2	I/O	Input/output 2. Referenced to $V_{CCA}$
A3	4	B2	I/O	Input/output 3. Referenced to $V_{CCA}$
A4	5	A3	I/O	Input/output 4. Referenced to $V_{CCA}$
A5	6	B3	I/O	Input/output 5. Referenced to $V_{CCA}$
A6	7	A4	I/O	Input/output 6. Referenced to $V_{CCA}$
A7	8	B4	I/O	Input/output 7. Referenced to $V_{CCA}$
A8	9	A5	I/O	Input/output 8. Referenced to $V_{CCA}$
B1	20	C 1	I/O	Input/output 1. Referenced to $V_{CCB}$
B2	18	D2	I/O	Input/output 2. Referenced to $V_{CCB}$
B3	17	C2	I/O	Input/output 3. Referenced to $V_{CCB}$
B4	16	D3	I/O	Input/output 4. Referenced to $V_{CCB}$
B5	15	C3	I/O	Input/output 5. Referenced to $V_{CCB}$
B6	14	D4	I/O	Input/output 6. Referenced to $V_{CCB}$
B7	13	C4	I/O	Input/output 7. Referenced to $V_{CCB}$
B8	12	D5	I/O	Input/output 8. Referenced to $V_{CCB}$
GND	11	C5	—	Ground
OE	10	B5	I	Tri-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to $V_{CCA}$ .
VCCA	2	A1	P	A-port supply voltage. $1.2\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$ , $V_{CCA} \leq V_{CCB}$ .
VCCB	19	D1	P	B-port supply voltage. $1.65\text{ V} \leq V_{CCB} \leq 5.5\text{ V}$ .
Thermal Pad			—	For the RGY package, the exposed center thermal pad must be either be connected to Ground or left electrically opened.

(1) I = input, O = output, I/O = input and output, P = power

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, $V_{CCA}$		–0.5	4.6	V
Supply voltage, $V_{CCB}$		–0.5	5.5	V
Input voltage, $V_I$ <sup>(2)</sup>	A port	–0.5	4.6	V
	B port	–0.5	6.5	
Voltage applied to any output in the high-impedance or power-off state, $V_O$ <sup>(2)</sup>	A port	–0.5	4.6	V
	B port	–0.5	6.5	
Voltage applied to any output in the high or low state, $V_O$ <sup>(2) (3)</sup>	A port	–0.5	$V_{CCA} + 0.5$	V
	B port	–0.5	$V_{CCB} + 0.5$	V
Input clamp current, $I_{IK}$	$V_I < 0$		–50	mA
Output clamp current, $I_{OK}$	$V_O < 0$		–50	mA
Continuous output current, $I_O$		–50	50	mA
Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND		–100	100	mA
Junction temperature, $T_J$			150	°C
Storage temperature, $T_{stg}$		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative Voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CCA}$  and  $V_{CCB}$  are provided in the recommended operating conditions table.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	
	Machine model (MM)	±150	
	IEC 61000-4-2 ESD (B Port) Contact Discharge	±8000	
	IEC 61000-4-2 ESD (B Port) Air-Gap Discharge	±6000	

- (1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

				MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage <sup>(3)</sup>			1.2	3.6	V
V <sub>CCB</sub>	Supply voltage <sup>(3)</sup>			1.65	5.5	V
V <sub>IH</sub>	High-level input voltage	A-Port I/Os	V <sub>CCA</sub> (V) = 1.2 to 1.95	V <sub>CCB</sub> (V) = 1.65 to 5.5	V <sub>CCI</sub> – 0.2	V <sub>CCI</sub>
			V <sub>CCA</sub> (V) = 1.95 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5	V <sub>CCI</sub> – 0.4	V <sub>CCI</sub>
		B-Port I/Os	V <sub>CCA</sub> (V) = 1.2 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5	V <sub>CCI</sub> – 0.4	V <sub>CCI</sub>
			OE	V <sub>CCA</sub> (V) = 1.2 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5	V <sub>CCA</sub> × 0.65
V <sub>IL</sub>	Low-level input voltage	A-Port I/Os	V <sub>CCA</sub> (V) = 1.2 to 1.95	V <sub>CCB</sub> (V) = 1.65 to 5.5	0	0.15
			V <sub>CCA</sub> (V) = 1.95 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5	0	0.15
		B-Port I/Os	V <sub>CCA</sub> (V) = 1.2 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5	0	0.15
			OE	V <sub>CCA</sub> (V) = 1.2 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5	0 V <sub>CCA</sub> × 0.35
Δt/Δv	Input transition rise or fall rate	A-Port I/Os Push-pull	V <sub>CCA</sub> (V) = 1.2 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5		10 ns/V
		B-Port I/Os Push-pull	V <sub>CCA</sub> (V) = 1.2 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5		10 ns/V
		Control input	V <sub>CCA</sub> (V) = 1.2 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5		10 ns/V
T <sub>A</sub>	Operating free-air temperature			–40	85	°C

 (1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the data input port.

 (2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

 (3) V<sub>CCA</sub> must be less than or equal to V<sub>CCB</sub>, and V<sub>CCA</sub> must not exceed 3.6 V.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TXS0108E			UNIT
		PW (TSSOP)	RGY	ZXY	
		20 PINS	20 PINS	20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	101.5	34.7	101.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	35.9	39.5	35.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	52.4	12.7	52.4	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.3	0.9	2.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	51.9	12.7	51.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	7.5	—	°C/W

 (1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics application report](#).

## 6.5 Electrical Characteristics: $T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ <sup>(1)(2)(3)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CCA}$ (V)	$V_{CCB}$ (V)	$T_A = 25^{\circ}\text{C}$			$T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$V_{OHA}$ Port A output high voltage	$I_{OH} = -20\ \mu\text{A}$ $V_{IB} \geq V_{CCB} - 0.4\ \text{V}$	1.2	1.65 to 5.5	$V_{CCA} \times 0.67$					V
$V_{OLA}$ Port A output low voltage	$I_{OL} = 135\ \mu\text{A}$ , $V_{IB} \leq 0.15\ \text{V}$	1.2	1.65 to 5.5	0.25					V
	$I_{OL} = 180\ \mu\text{A}$ , $V_{IB} \leq 0.15\ \text{V}$	1.4	1.65 to 5.5					0.4	
	$I_{OL} = 220\ \mu\text{A}$ , $V_{IB} \leq 0.15\ \text{V}$	1.65	1.65 to 5.5					0.4	
	$I_{OL} = 300\ \mu\text{A}$ , $V_{IB} \leq 0.15\ \text{V}$	2.3	1.65 to 5.5					0.4	
	$I_{OL} = 400\ \mu\text{A}$ , $V_{IB} \leq 0.15\ \text{V}$	3	1.65 to 5.5					0.55	
$V_{OHB}$ Port B output high voltage	$I_{OH} = -20\ \mu\text{A}$ , $V_{IA} \geq V_{CCA} - 0.2\ \text{V}$	1.2	1.65 to 5.5	$V_{CCB} \times 0.67$					V
$V_{OLB}$ Port B output low voltage	$I_{OL} = 220\ \mu\text{A}$ , $V_{IA} \leq 0.15\ \text{V}$	1.2 to 3.6	1.65					0.4	V
	$I_{OL} = 300\ \mu\text{A}$ , $V_{IA} \leq 0.15\ \text{V}$	1.2 to 3.6	2.3					0.4	
	$I_{OL} = 400\ \mu\text{A}$ , $V_{IA} \leq 0.15\ \text{V}$	1.2 to 3.6	3					0.55	
	$I_{OL} = 620\ \mu\text{A}$ , $V_{IA} \leq 0.15\ \text{V}$	1.2 to 3.6	4.5					0.55	
$I_I$ Input leakage current	OE: $V_I = V_{CCI}$ or GND	1.2	1.65 to 5.5	-1		1		2	$\mu\text{A}$
$I_{OZ}$ High-impedance state output current	A or B port	1.2	1.65 to 5.5	-1		1	-2	2	$\mu\text{A}$
$I_{CCA}$ $V_{CCA}$ supply current	$V_I = V_O = \text{Open}$ , $I_O = 0$	1.2	1.65 to 5.5	1.5			-2	2	$\mu\text{A}$
		1.5 to 3.6	2.3 to 5.5					2	
		3.6	0					2	
		0	5.5					-1	
$I_{CCB}$ $V_{CCB}$ supply current	$V_I = V_O = \text{Open}$ , $I_O = 0$	1.2	1.65 to 5.5	1.5					$\mu\text{A}$
		1.5 to 3.6	2.3 to 5.5					6	
		3.6	0					-1	
		0	5.5					1.2	
$I_{CCA} + I_{CCB}$ Combined supply current	$V_I = V_{CCI}$ or GND, $I_O = 0$	1.2	2.3 to 5.5	3					$\mu\text{A}$
		1.5 to 3.6	2.3 to 5.5					8	
$I_{CCZA}$ High-impedance state $V_{CCA}$ supply current	$V_I = V_O = \text{Open}$ , $I_O = 0$ , OE = GND	1.2	1.65 to 5.5	0.05					$\mu\text{A}$
$I_{CCZB}$ High-impedance state $V_{CCB}$ supply current	$V_I = V_O = \text{Open}$ , $I_O = 0$ , OE = GND	1.2	1.65 to 5.5	4					$\mu\text{A}$
$C_i$ Input capacitance	OE	3.3	3.3	4.5				5.5	pF
$C_{io}$ Input-to-output internal capacitance	A port	3.3	3.3	6				7	pF
	B port	3.3	3.3	5.5				6	

- (1)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.
- (2)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- (3)  $V_{CCA}$  must be less than or equal to  $V_{CCB}$ , and  $V_{CCA}$  must not exceed 3.6 V.

## 6.6 Timing Requirements: $V_{CCA} = 1.2 \text{ V}$

 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 1.2 \text{ V}$ 

			$V_{CCB} \text{ (V)}$				UNIT
			1.8 (TYP)	2.5 (TYP)	3.3 (TYP)	5 (TYP)	
Data rate	Push-pull		20	20	20	20	Mbps
	Open-drain		2	2	2	2	
$t_w$ Pulse duration	Data inputs	Push-pull	50	50	50	50	ns
		Open-drain	500	500	500	500	

## 6.7 Timing Requirements: $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$

 over recommended operating free-air temperature range,  $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$  (unless otherwise noted)

			$V_{CC\ B} = 1.8\ V$ $\pm 0.15\ V$		$V_{CC\ B} = 2.5\ V$ $\pm 0.2\ V$		$V_{CC\ B} = 3.3\ V$ $\pm 0.3\ V$		$V_{CC\ B} = 5\ V$ $\pm 0.5\ V$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Push-pull		40		60		60		50		Mbps
	Open-drain		2		2		2		2		
$t_w$ Pulse duration	Data inputs	Push-pull	25		16.7		16.7		20		ns
		Open-drain	500		500		500		500		

## 6.8 Timing Requirements: $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$

 over recommended operating free-air temperature range,  $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (unless otherwise noted)

			V <sub>CC B</sub> = 1.8 V ± 0.15 V		V <sub>CC B</sub> = 2.5 V ± 0.2 V		V <sub>CC B</sub> = 3.3 V ± 0.3 V		V <sub>CC B</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Push-pull		40		60		60		60		Mbps
	Open-drain		2		2		2		2		
t <sub>w</sub> Pulse duration	Data inputs	Push-pull	25		16.7		16.7		16.7		ns
		Open-drain	500		500		500		500		

## 6.9 Timing Requirements: $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$

 over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted)

				$V_{CCB} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V}$ $\pm 0.5 \text{ V}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Push-pull			60		60		60	Mbps	
	Open-drain			2		2		2		
$t_w$ Pulse duration	Data inputs	Push-pull		16.7		16.7		16.7	ns	
		Open-drain		500		500		500		

## 6.10 Timing Requirements: $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$

 over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
Data rate	Push-pull		60		60		Mbps
	Open-drain		2		2		
$t_w$	Pulse duration	Data inputs	Push-pull	16.7	16.7		ns
			Open-drain	500	500		



## 6.11 Switching Characteristics: $V_{CCA} = 1.2\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$V_{CCB} = 1.8\text{ V}$ $\pm 0.15\text{ V}$			$V_{CCB} = 2.5\text{ V}$ $\pm 0.2\text{ V}$			$V_{CCB} = 3.3\text{ V}$ $\pm 0.3\text{ V}$			$V_{CCB} = 5\text{ V}$ $\pm 0.5\text{ V}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PHL}$ Propagation delay time (high-to-low output)	A-to-B	Push-pull driving		6.5			5.9			5.7			5.5		ns
		Open-drain driving		11.9			11.1			11			11.1		
$t_{PLH}$ Propagation delay time (low-to-high output)	A-to-B	Push-pull driving		7.1			6.3			6.2			6.6		
		Open-drain driving		293			236			197			152		
$t_{PHL}$ Propagation delay time (high-to-low output)	B-to-A	Push-pull driving		6.4			6			5.8			5.6		ns
		Open-drain driving		8.5			6.8			6.2			5.9		
$t_{PLH}$ Propagation delay time (low-to-high output)	B-to-A	Push-pull driving		5.6			4.1			3.6			3.2		
		Open-drain driving		312			248			192			132		
$t_{en}$ Enable time	OE-to-A or B	Push-pull driving		200			200			200			200		ns
$t_{dis}$ Disable time	OE-to-A or B	Push-pull driving		16.8			13.9			13.2			13.5		ns
$t_{rA}$ Input rise time	A-port rise time	Push-pull driving		7.9			6.7			6.5			6.4		ns
		Open-drain driving		296			238			185			127		
$t_{rB}$ Input rise time	B-port rise time	Push-pull driving		6.3			3.3			1.8			1.5		ns
		Open-drain driving		236			164			115			60		
$t_{fA}$ Input fall time	A-port fall time	Push-pull driving		5.8			4.8			4.3			3.8		ns
		Open-drain driving		5.9			4.7			4.1			3.5		
$t_{fB}$ Input fall time	B-port fall time	Push-pull driving		4.6			2.8			2.2			1.9		
		Open-drain driving		4.5			2.7			2.2			1.9		
$t_{SK(O)}$ Skew (time), output	Channel -to- channel skew	Push-pull driving		1			1			1			1		ns
Maximum data rate	A or B	Push-pull driving		20			20			20			20		Mbps
		Open-drain driving		2			2			2			2		

## 6.12 Switching Characteristics: $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		V <sub>CCB</sub> = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PHL</sub>	Propagation delay time (high-to-low output)	A-to-B	Push-pull driving	11		9.2		8.6		8.6		ns
			Open-drain driving	4	14.4	3.6	12.8	3.5	12.2	3.5	12	
t <sub>PLH</sub>	Propagation delay time (low-to-high output)	A-to-B	Push-pull driving	12		10		9.8		9.7		
			Open-drain driving	182	720	143	554	114	473	81	384	
t <sub>PHL</sub>	Propagation delay time (high-to-low output)	B-to-A	Push-pull driving	12.7		11.1		11		12		ns
			Open-drain driving	3.4	13.2	3.1	9.6	2.8	8.5	2.5	7.5	
t <sub>PLH</sub>	Propagation delay time (low-to-high output)	B-to-A	Push-pull driving	9.5		6.2		5.1		1.6		
			Open-drain driving	186	745	147	603	118	519	84	407	
t <sub>en</sub>	Enable time	OE-to-A or B	Push-pull driving	200		200		200		200		ns
t <sub>dis</sub>	Disable time	OE-to-A or B	Push-pull driving	28.1		22		20.1		19.6		ns
t <sub>rA</sub>	Input rise time	A-port rise time	Push-pull driving	3.5	13.1	3	9.8	3.1	9	3.2	8.3	ns
			Open-drain driving	147	982	115	716	92	592	66	481	
t <sub>rB</sub>	Input rise time	B-port rise time	Push-pull driving	2.9	11.4	1.9	7.4	0.9	4.7	0.7	2.6	ns
			Open-drain driving	135	1020	91	756	58	653	20	370	
t <sub>fA</sub>	Input fall time	A-port fall time	Push-pull driving	2.3	9.9	1.7	7.7	1.6	6.8	1.7	6	ns
			Open-drain driving	2.4	10	2.1	7.9	1.7	7	1.5	6.2	
t <sub>fB</sub>	Input fall time	B-port fall time	Push-pull driving	2	8.7	1.3	5.5	0.9	3.8	0.8	3.1	
			Open-drain driving	1.2	11.5	1.3	8.6	1	9.6	0.5	7.7	
t <sub>SK(O)</sub>	Skew (time), output	Channel-to-channel skew	Push-pull driving	1		1	1	1.1		1		ns
	Maximum data rate	A or B	Push-pull driving	40		60		60		50		Mbps
			Open-drain driving	2		2		2		2		

### 6.13 Switching Characteristics: $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PHL}$ Propagation delay time (high-to-low output)	A-to-B	Push-pull driving		8.2		6.4		5.7		5.6	ns
		Open-drain driving	3.6	11.4	3.2	9.9	3.1	9.3	3.1	8.9	
$t_{PLH}$ Propagation delay time (low-to-high output)	A-to-B	Push-pull driving		9		2.1		6.5		6.3	
		Open-drain driving	194	729	155	584	126	466	90	346	
$t_{PHL}$ Propagation delay time (high-to-low output)	B-to-A	Push-pull driving		9.8		8		7.4		7	ns
		Open-drain driving	3.4	12.1	2.8	8.5	2.5	7.3	2.1	6.2	
$t_{PLH}$ Propagation delay time (low-to-high output)	B-to-A	Push-pull driving		10.2		7		5.8		5	
		Open-drain driving	197	733	159	578	129	459	93	323	
$t_{en}$ Enable time	OE-to-A or B	Push-pull driving		200		200		200		200	ns
$t_{dis}$ Disable time	OE-to-A or B	Push-pull driving		25.1		18.8		16.5		15.3	ns
$t_{rA}$ Input rise time	A-port rise time	Push-pull driving	3.1	11.9	2.6	8.6	2.7	7.8	2.8	7.2	ns
		Open-drain driving	155	996	124	691	100	508	72	350	
$t_{rB}$ Input rise time	B-port rise time	Push-pull driving	2.8	10.5	1.8	7.2	1.2	5.2	0.7	2.7	ns
		Open-drain driving	132	1001	106	677	73	546	32	323	
$t_{fA}$ Input fall time	A-port fall time	Push-pull driving	2.1	8.8	1.6	6.6	1.4	5.7	1.4	4.9	ns
		Open-drain driving	2.2	9	1.7	6.7	1.4	5.8	1.2	5.2	
$t_{fB}$ Input fall time	B-port fall time	Push-pull driving	2	8.3	1.3	5.4	0.9	3.9	0.7	3	
		Open-drain driving	0.8	10.5	0.7	10.7	1	9.6	0.6	7.8	
$t_{SK(O)}$ Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1		1		1	ns
Maximum data rate	A or B	Push-pull driving	40		60		60		60		Mbps
		Open-drain driving	2		2		2		2		

## 6.14 Switching Characteristics: $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$

 over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PHL}$ Propagation delay time (high-to-low output)	A -to-B	Push-pull driving		5		4		3.7	ns
		Open-drain driving	2.4	6.9	2.3	6.3	2.2	5.8	
$t_{PLH}$ Propagation delay time (low-to-high output)	A -to-B	Push-pull driving		5.2		4.3		3.9	ns
		Open-drain driving	149	592	125	488	93	368	
$t_{PHL}$ Propagation delay time (high-to-low output)	B-to-A	Push-pull driving		5.4		4.7		4.2	ns
		Open-drain driving	2.5	7.3	2.2	6	1.8	4.9	
$t_{PLH}$ Propagation delay time (low-to-high output)	B-to-A	Push-pull driving		5.9		4.4		3.5	ns
		Open-drain driving	150	595	126	481	94	345	
$t_{en}$ Enable time	OE-to-A or B	Push-pull driving		200		200		200	ns
$t_{dis}$ Disable time	OE-to-A or B	Push-pull driving		15.7		12.9		11.2	ns
$t_{rA}$ Input rise time	A-port rise time	Push-pull driving	2	7.3	2.1	6.4	2.2	5.8	ns
		Open-drain driving	110	692	93	529	68	369	
$t_{rB}$ Input rise time	B-port rise time	Push-pull driving	1.8	6.5	1.3	5.1	0.7	3.4	ns
		Open-drain driving	107	693	79	483	41	304	
$t_{fA}$ Input fall time	A-port fall time	Push-pull driving	1.5	5.7	1.2	4.7	1.3	3.8	ns
		Open-drain driving	1.5	5.6	1.2	4.7	1.1	4	
$t_{fB}$ Input fall time	B-port fall time	Push-pull driving	1.4	5.4	0.9	4.1	0.7	3	ns
		Open-drain driving	0.4	14.2	0.5	19.4	0.4	3	
$t_{SK(O)}$ Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1.2		1	ns
Maximum data rate	A or B	Push-pull driving	60		60		60		Mbps
		Open-drain driving	2		2		2		

## 6.15 Switching Characteristics: $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
				MIN	MAX	MIN	MAX	
$t_{PHL}$	Propagation delay time (high-to-low output)	A-to-B	Push-pull driving		3.8		3.1	ns
			Open-drain driving	2	5.3	1.9	4.8	
$t_{PLH}$	Propagation delay time (low-to-high output)	A-to-B	Push-pull driving		3.9		3.5	
			Open-drain driving	111	439	87	352	
$t_{PHL}$	Propagation delay time (high-to-low output)	B-to-A	Push-pull driving		4.2		3.8	ns
			Open-drain driving	2.1	5.5	1.7	4.5	
$t_{PLH}$	Propagation delay time (low-to-high output)	A-to-B	Push-pull driving		3.8		4.3	
			Open-drain driving	112	449	86	339	
$t_{en}$	Enable time	OE-to-A or B	Push-pull driving		200		200	ns
$t_{dis}$	Disable time	OE-to-A or B	Push-pull driving		11.9		9.8	ns
$t_{rA}$	Input rise time	A-port rise time	Push-pull driving	1.8	5.7	1.9	5	ns
			Open-drain driving	75	446	57	337	
$t_{rB}$	Input rise time	B-port rise time	Push-pull driving	1.5	5	1	3.6	ns
			Open-drain driving	72	427	40	290	
$t_{fA}$	Input fall time	A-port fall time	Push-pull driving	1.2	4.5	1.1	3.5	ns
			Open-drain driving	1.1	4.4	1	3.7	
$t_{fB}$	Input fall time	B-port fall time	Push-pull driving	1.1	4.2	0.8	3.1	
			Open-drain driving	1	4.2	0.8	3.1	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1	ns
	Maximum data rate	A or B	Push-pull driving	60		60		Mbps
			Open-drain driving	2		2		

## 6.16 Operating Characteristics: $V_{CCA} = 1.2\text{ V}$ to $1.5\text{ V}$ , $V_{CCB} = 1.2\text{ V}$ to $1.5\text{ V}$

 $T_A = 25^\circ\text{C}$ 

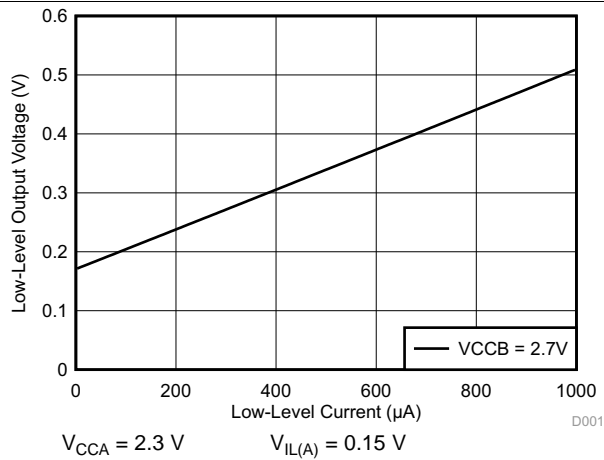
PARAMETER		TEST CONDITIONS		V <sub>CCA</sub> = 1.2 V, V <sub>CCB</sub> = 1.2 V			V <sub>CCA</sub> = 1.2 V, V <sub>CCB</sub> = 1.2 V			V <sub>CCA</sub> = 1.5 V, V <sub>CCB</sub> = 1.5 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
C <sub>pdA</sub> Power dissipation capacitance	CL = 0 f = 10 MHz tr= tf= 1 ns OE = V <sub>CCA</sub> (outputs enabled)	A-port input, B-port output	5.9			5.7			5.9			pF	
		B-port input, A-port output	10.2			10.3			9.9				
C <sub>pdB</sub> Power dissipation capacitance		A-port input, B-port output	29.9			22.2			21.5				
		B-port input, A-port output	22.9			16.7			16.7				
C <sub>pdA</sub> Power dissipation capacitance	CL = 0 f = 10 MHz tr= tf= 1 ns OE = V <sub>CCA</sub> (outputs enabled)	A-port input, B-port output	0.01			0.01			0.01			pF	
		B-port input, A-port output	0.06			0.01			0.01				
C <sub>pdB</sub> Power dissipation capacitance		A-port input, B-port output	0.06			0.01			0.01				
		B-port input, A-port output	0.06			0.01			0.01				

## 6.17 Operating Characteristics: $V_{CCA} = 1.8\text{ V}$ to $3.3\text{ V}$ , $V_{CCB} = 1.8\text{ V}$ to $3.3\text{ V}$

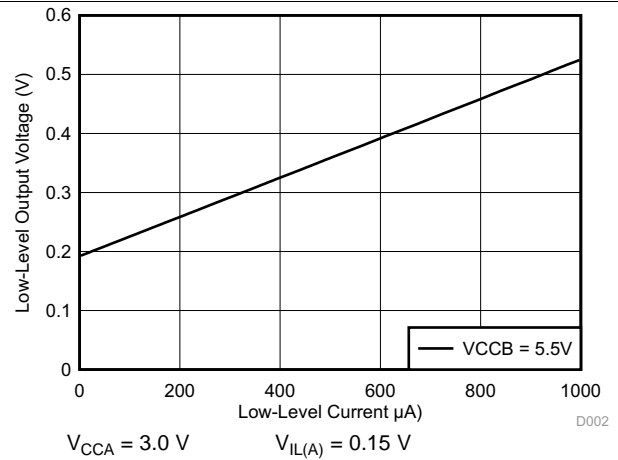
 $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS		V <sub>CCA</sub> = 1.8 V, V <sub>CCB</sub> = 1.8 V			V <sub>CCA</sub> = 2.5 V, V <sub>CCB</sub> = 2.5 V			V <sub>CCA</sub> = 2.5 V, V <sub>CCB</sub> = 2.5 V			V <sub>CCA</sub> = 3.3 V, V <sub>CCB</sub> = 3.3 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
C <sub>pdA</sub>	Power dissipation capacitance	CL = 0 f = 10 MHz tr= tf= 1 ns OE = V <sub>CCA</sub> (outputs enabled)	A-port input, B-port output	5.9			6.7			6.9			8			pF
			B-port input, A-port output	9.7			9.7			9.4			9.8			
C <sub>pdB</sub>	Power dissipation capacitance		A-port input, B-port output	20.8			21			23.4			23			
			B-port input, A-port output	16.8			17.8			20.8			20.9			
C <sub>pdA</sub>	Power dissipation capacitance	CL = 0 f = 10 MHz tr= tf= 1 ns OE = V <sub>CCA</sub> (outputs enabled)	A-port input, B-port output	0.01			0.01			0.01			0.01			pF
			B-port input, A-port output	0.01			0.01			0.01			0.01			
C <sub>pdB</sub>	Power dissipation capacitance		A-port input, B-port output	0.01			0.01			0.03			0.02			
			B-port input, A-port output	0.01			0.01			0.03			0.02			

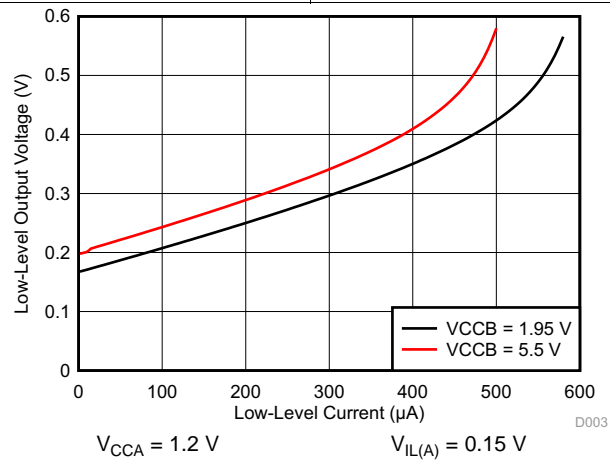
## 7 Typical Characteristics



**图 1. Low-Level Output Voltage ( $V_{OL(Bx)}$ ) vs Low-Level Current ( $I_{OL(Bx)}$ )**



**图 2. Low-Level Output Voltage ( $V_{OL(Bx)}$ ) vs Low-Level Current ( $I_{OL(Bx)}$ )**

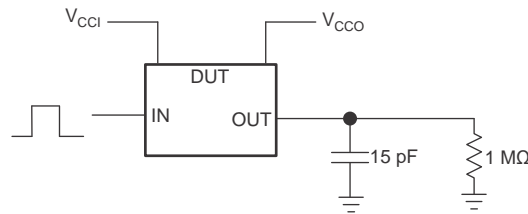


**图 3. Low-Level Output Voltage ( $V_{OL(Bx)}$ ) vs Low-Level Current ( $I_{OL(Bx)}$ )**

## 8 Parameter Measurement Information

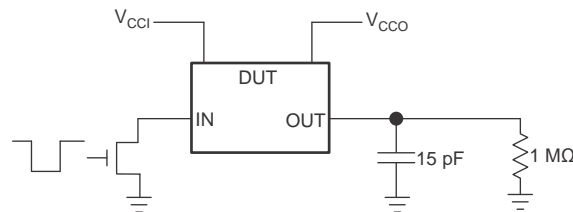
### 8.1 Load Circuits

图 4 shows the push-pull driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time. 图 5 shows the open-drain driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time.



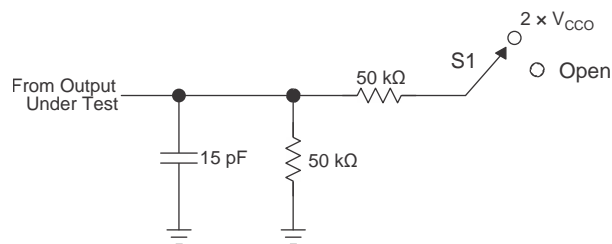
- (1)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- (2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

**图 4. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time And Fall-Time Measurement Using a Push-Pull Driver**



- (1)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- (2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

**图 5. Data Rate (10 pF), Pulse Duration (10 pF), Propagation Delay, Output Rise-Time And Fall-Time Measurement Using an Open-Drain Driver**



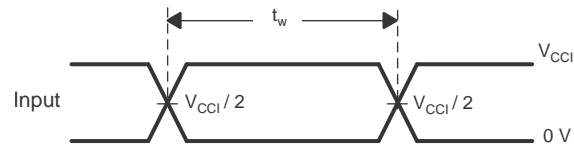
TEST	S1
$t_{PZL}$ , $t_{PLZ}$ ( $t_{dis}$ )	$2 \times V_{CCO}$
$t_{PHZ}$ , $t_{PZH}$ ( $t_{en}$ )	Open

- (1)  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- (2)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

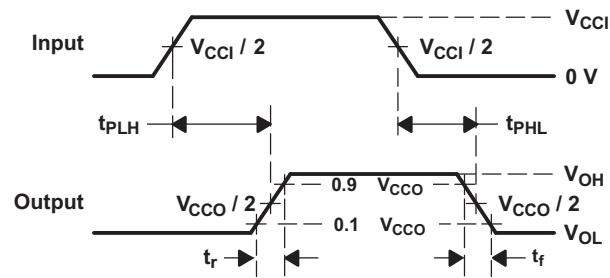
**图 6. Load Circuit for Enable-Time and Disable-Time Measurement**



## 8.2 Voltage Waveforms



**图 7. Pulse Duration (Push-Pull)**



**图 8. Propagation Delay Times**

## 9 Detailed Description

### 9.1 Overview

The TXS0108E device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A-port accepts I/O voltages ranging from 1.2 V to 3.6 V. The B-port accepts I/O voltages from 1.65 V to 5.5 V. The device uses pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. The pull-up resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

### 9.2 Functional Block Diagram

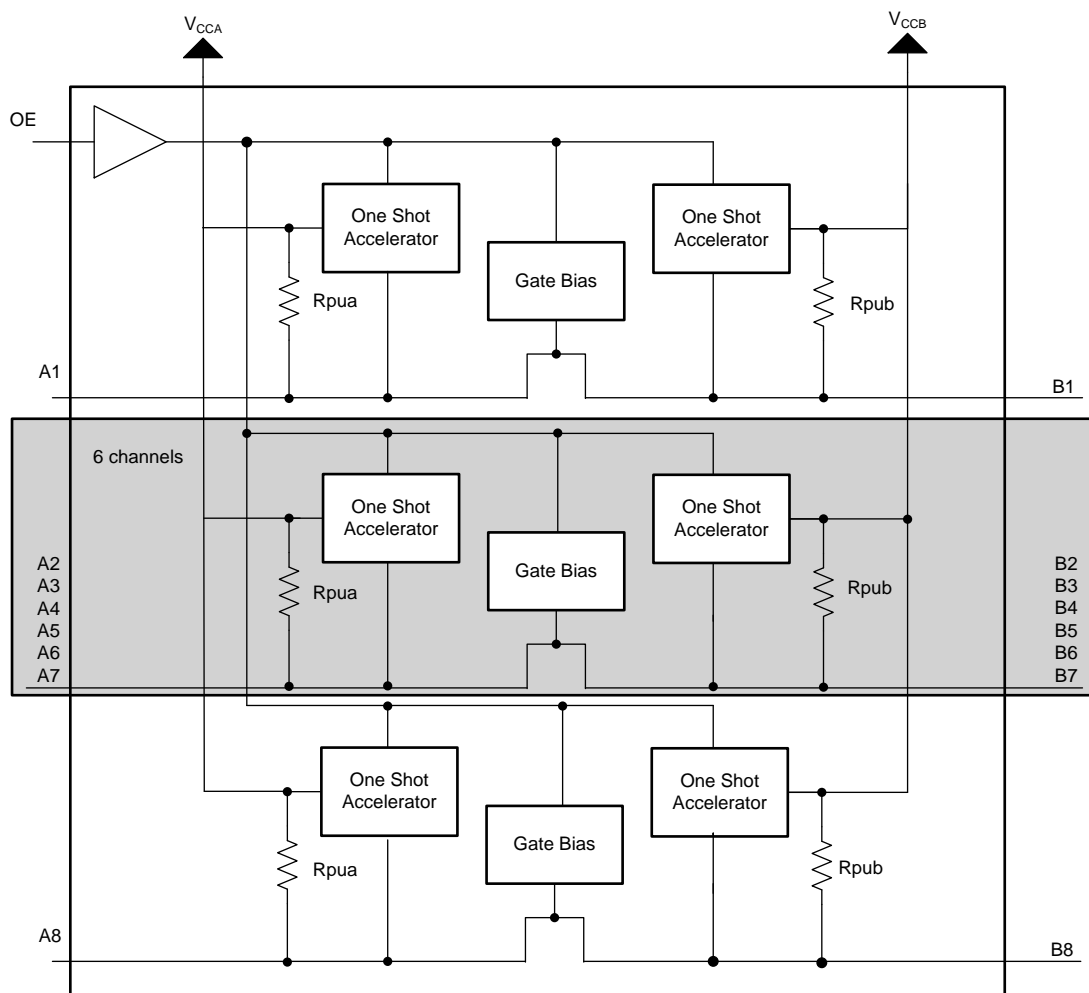


图 9. Functional Block Diagram

Each A-port I/O has a pull-up resistor ( $R_{PUA}$ ) to  $V_{CCA}$  and each B-port I/O has a pull-up resistor ( $R_{PUB}$ ) to  $V_{CCB}$ .  $R_{PUA}$  and  $R_{PUB}$  have a value of 40 k $\Omega$  when the output is driving low.  $R_{PUA}$  and  $R_{PUB}$  have a value of 4 k $\Omega$  when the output is driving high.  $R_{PUA}$  and  $R_{PUB}$  are disabled when OE = Low.

## 9.3 Feature Description

### 9.3.1 Architecture

图 10 describes semi-buffered architecture design this application requires for both push-pull and open-drain mode. This application uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high edges), a high-on-resistance N-channel pass-gate transistor (on the order of  $300\ \Omega$  to  $500\ \Omega$ ) and pull-up resistors (to provide DC-bias and drive capabilities) to meet these requirements. This design needs no direction-control signal (to control the direction of data flow from A to B or from B to A). The resulting implementation supports both low-speed open-drain operation as well as high-speed push-pull operation.

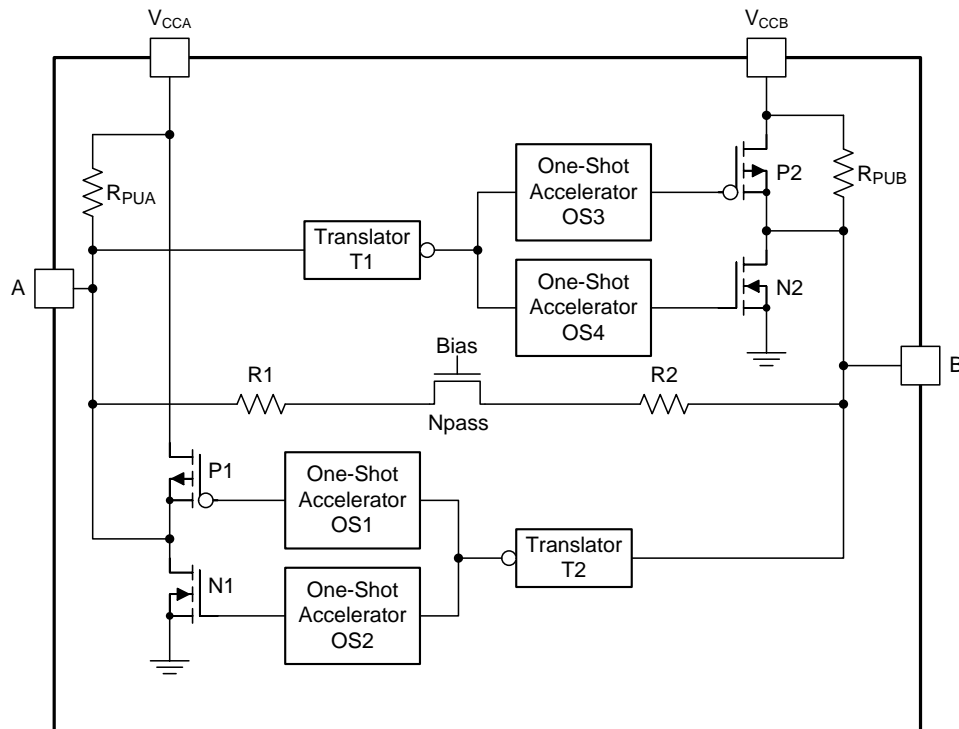


图 10. Architecture of a TXS0108E Cell

When transmitting data from A-ports to B-ports, during a rising edge the one-shot circuit (OS3) turns on the PMOS transistor (P2) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from A to B, the one-shot circuit (OS4) turns on the N-channel MOSFET transistor (N2) for a short-duration which speeds up the high-to-low transition. The B-port edge-rate accelerator consists of one-shot circuits OS3 and OS4. Transistors P2 and N2 and serves to rapidly force the B port high or low when a corresponding transition is detected on the A port.

When transmitting data from B- to A-ports, during a rising edge the one-shot circuit (OS1) turns on the PMOS transistor (P1) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from B to A, the one-shot circuit (OS2) turns on NMOS transistor (N1) for a short-duration and this speeds up the high-to-low transition. The A-port edge-rate accelerator consists of one-shots OS1 and OS2, transistors P1 and N1 components and form the edge-rate accelerator and serves to rapidly force the A port high or low when a corresponding transition is detected on the B port.

## Feature Description (接下页)

### 9.3.2 Input Driver Requirements

The continuous DC-current *sinking* capability is determined by the external system-level open-drain (or push-pull) drivers that are interfaced to the TXS0108E I/O pins. Because the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest DC-current *sourcing* capability of hundreds of micro-amperes, as determined by the internal pull-up resistors.

The fall time ( $t_{fA}$ ,  $t_{fB}$ ) of a signal depends on the edge-rate and output impedance of the external device driving TXS0108E data I/Os, as well as the capacitive loading on the data lines.

Similarly, the  $t_{PHL}$  and maximum data rates also depend on the output impedance of the external driver. The values for  $t_{fA}$ ,  $t_{fB}$ ,  $t_{PHL}$ , and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50  $\Omega$ .

### 9.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper one-shot triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The one-shot circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The one-shot duration has been set to best optimize trade-offs between dynamic  $I_{CC}$ , load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance of the TXS0108E output. Therefore, TI recommends that this lumped-load capacitance is considered in order to avoid one-shot retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

### 9.3.4 Enable and Disable

The TXS0108E has an OE pin input that is used to disable the device by setting the OE pin low, which places all I/Os in the Hi-Z state. The disable time ( $t_{dis}$ ) indicates the delay between the time when the OE pin goes low and when the outputs actually get disabled (Hi-Z). The enable time ( $t_{en}$ ) indicates the amount of time the design must allow for the one-shot circuitry to become operational after the OE pin goes high.

### 9.3.5 Pull-up or Pull-down Resistors on I/O Lines

The TXS0108E has the smart pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line. Each A-port I/O has a pull-up resistor ( $R_{PUA}$ ) to  $V_{CCA}$  and each B-port I/O has a pull-up resistor ( $R_{PUB}$ ) to  $V_{CCB}$ .  $R_{PUA}$  and  $R_{PUB}$  have a value of 40 k $\Omega$  when the output is driving low.  $R_{PUA}$  and  $R_{PUB}$  have a value of 4 k $\Omega$  when the output is driving high.  $R_{PUA}$  and  $R_{PUB}$  are disabled when OE = Low. This feature provides lower static power consumption (when the I/Os are passing a low), and supports lower  $V_{OL}$  values for the same size pass-gate transistor, and helps improve simultaneous switching performance.

## 9.4 Device Functional Modes

The TXS0108E device has two functional modes, enabled and disabled. To disable the device set the OE pin input low, which places all I/Os in a high impedance state. Setting the OE pin input high enables the device.

## 10 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The TXS0108E can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The device is ideal for use in applications where an open-drain driver is connected to the data I/Os. The device is appropriate for applications where a push-pull driver is connected to the data I/Os, but the TXB0104 device, (SCES650) *4-Bit Bidirectional Voltage-Level Translator* might be a better option for such push-pull applications. The device is a semi-buffered auto-direction-sensing voltage translator design is optimized for translation applications (for example, MMC Card Interfaces) that require the system to start out in a low-speed open-drain mode and then switch to a higher speed push-pull mode.

### 10.2 Typical Application

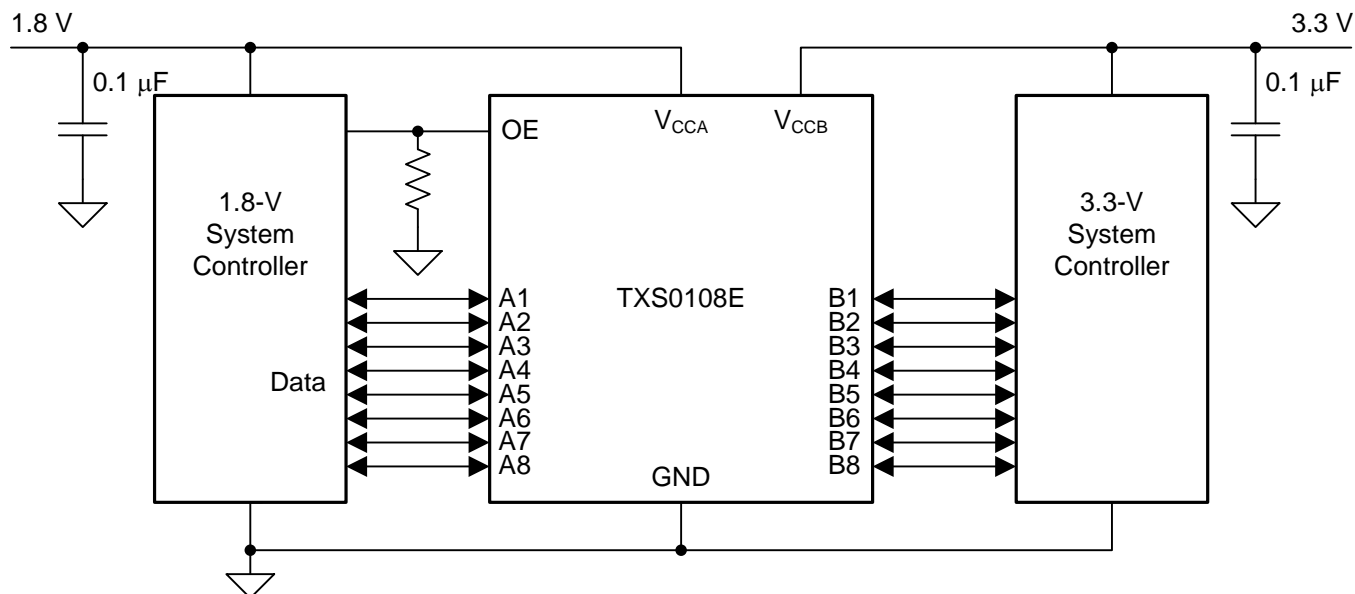


图 11. Typical Application Circuit

#### 10.2.1 Design Requirements

For this design example, use the parameters listed in 表 2. Ensure that  $V_{CCA} \leq V_{CCB}$ .

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.4 V to 3.6 V
Output voltage range	1.65 V to 5.5 V

#### 10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

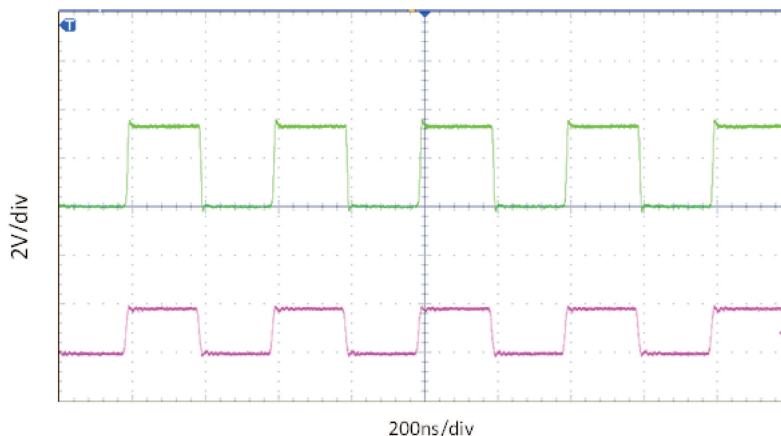
- Input voltage range
  - Use the supply voltage of the device that is driving the TXS0108E device to determine the input voltage range. For a valid logic high the value must exceed the  $V_{IH}$  of the input port. For a valid logic low the value

must be less than the  $V_{IL}$  of the input port.

- Output voltage range
  - Use the supply voltage of the device that the TXS0108E device is driving to determine the output voltage range.
  - The TXS0108E device has smart internal pull-up resistors. External pull-up resistors can be added to reduce the total RC of a signal trace if necessary.
- An external pull-down resistor decreases the output  $V_{OH}$  and  $V_{OL}$ . Use 公式 1 to calculate the  $V_{OH}$  as a result of an external pull-down resistor.

$$V_{OH} = V_{CCX} \times R_{PD} / (R_{PD} + 4 \text{ k}\Omega) \quad (1)$$

### 10.2.3 Application Curves



$$V_{CCA} = 1.8 \text{ V}$$

$$V_{CCB} = 3.3 \text{ V}$$

**图 12. Level-Translation of a 2.5-MHz Signal**

## 11 Power Supply Recommendations

During operation, ensure that  $V_{CCA} \leq V_{CCB}$  at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by  $V_{CCA}$  and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pull-down resistor and must not be enabled until  $V_{CCA}$  and  $V_{CCB}$  are fully ramped and stable. The minimum value of the pull-down resistor to ground is determined by the current-sourcing capability of the driver.

## 12 Layout

### 12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. Place the capacitors as close as possible to the  $V_{CCA}$ ,  $V_{CCB}$  pin and GND pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30 ns, ensuring that any reflection encounters low impedance at the source driver.

### 12.2 Layout Example

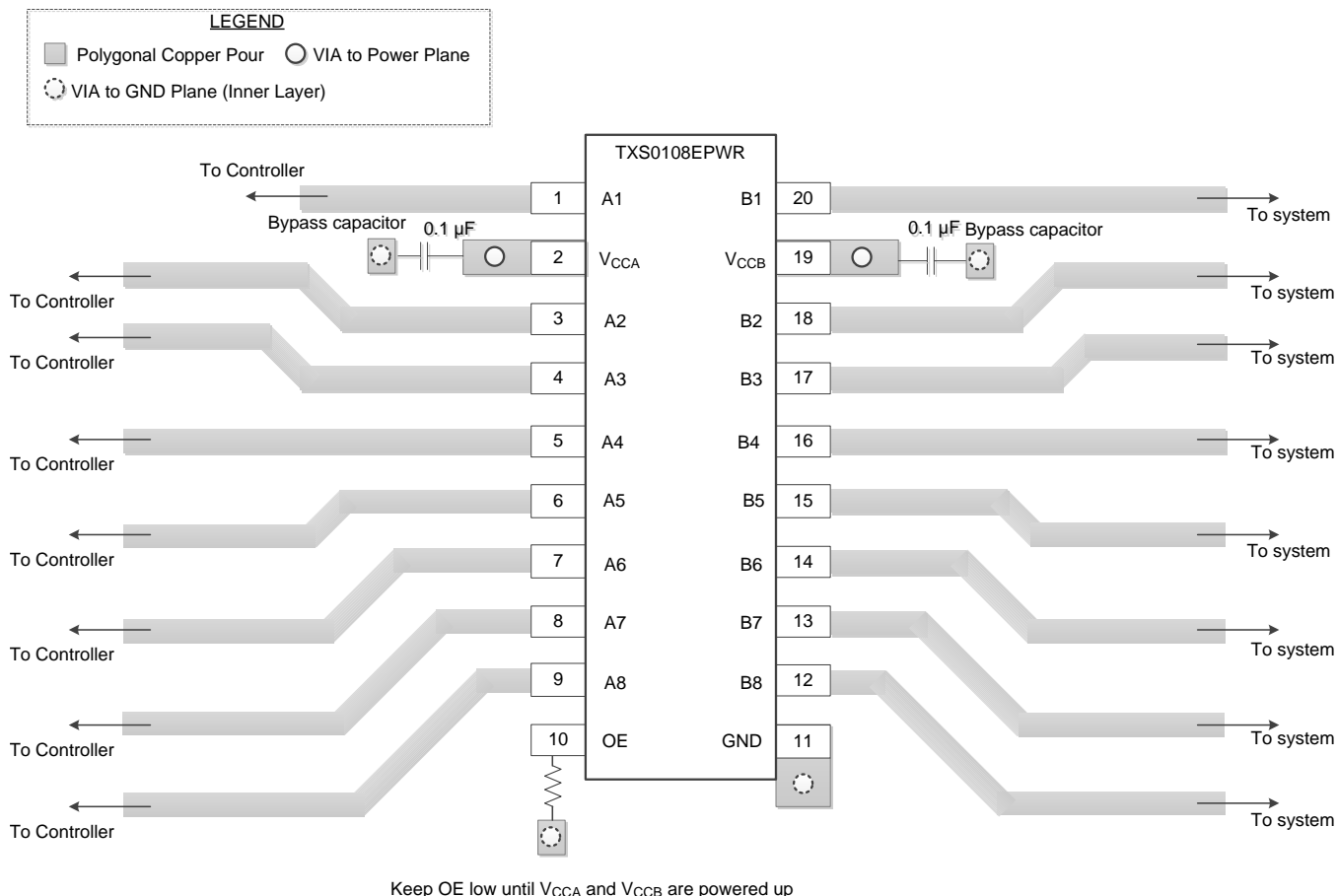


图 13. Layout Example

## 13 器件和文档支持

### 13.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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### 13.2 商标

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### 13.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 13.4 术语表

**SLYZ022** — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

## 14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。



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## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS0108ENMER	ACTIVE	NFBGA	NME	20	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	2APW	<a href="#">Samples</a>
TXS0108EPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF08E	<a href="#">Samples</a>
TXS0108EPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF08E	<a href="#">Samples</a>
TXS0108ERGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YF08E	<a href="#">Samples</a>
TXS0108EZXYR	ACTIVE	BGA MICROSTAR JUNIOR	ZXY	20	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	YF08E	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0108EPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TXS0108ERGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
TXS0108EZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	330.0	12.4	2.75	3.45	1.05	4.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS

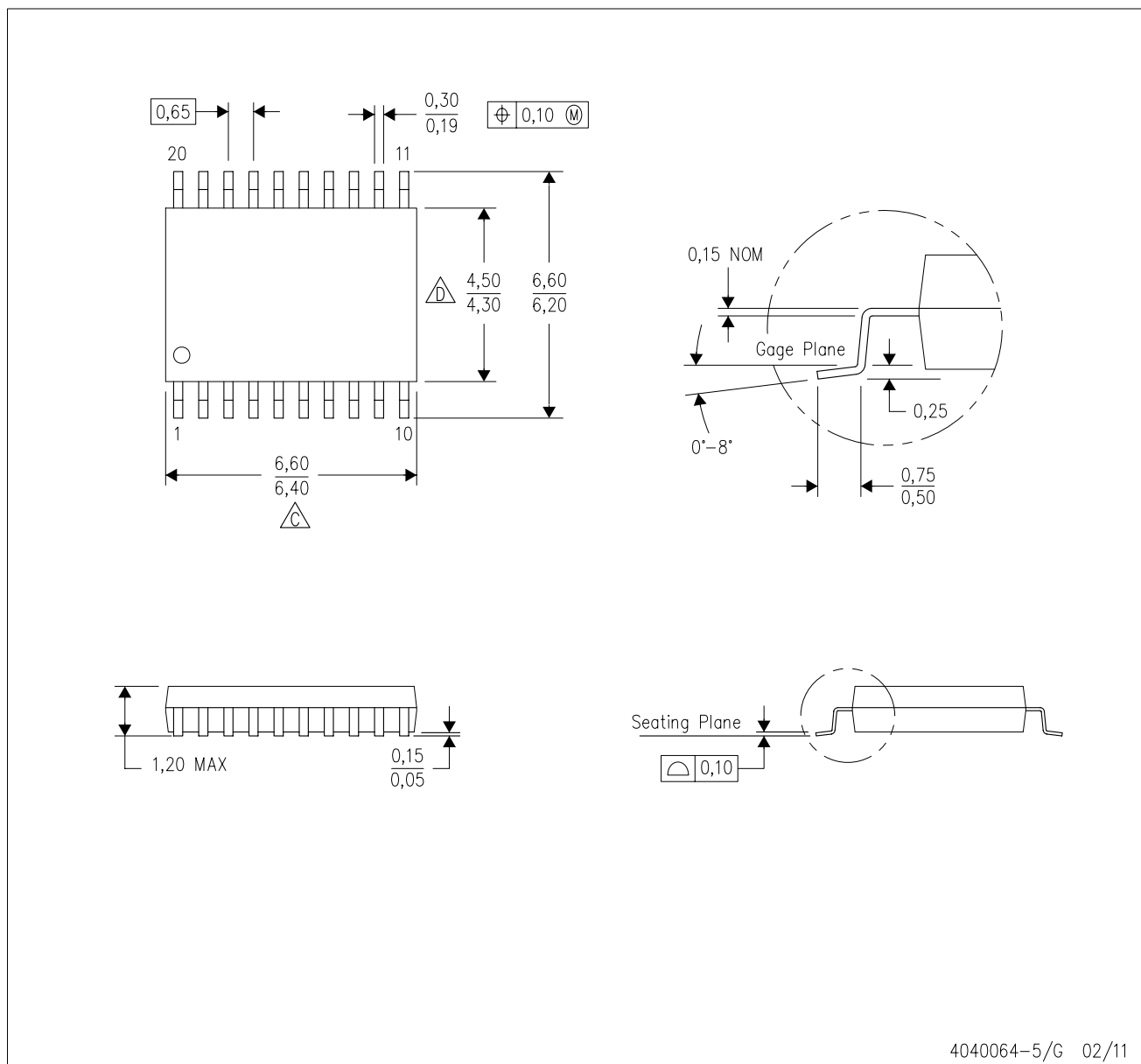


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0108EPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TXS0108ERGYR	VQFN	RGY	20	3000	853.0	449.0	35.0
TXS0108EZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	350.0	350.0	43.0

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

## GENERIC PACKAGE VIEW

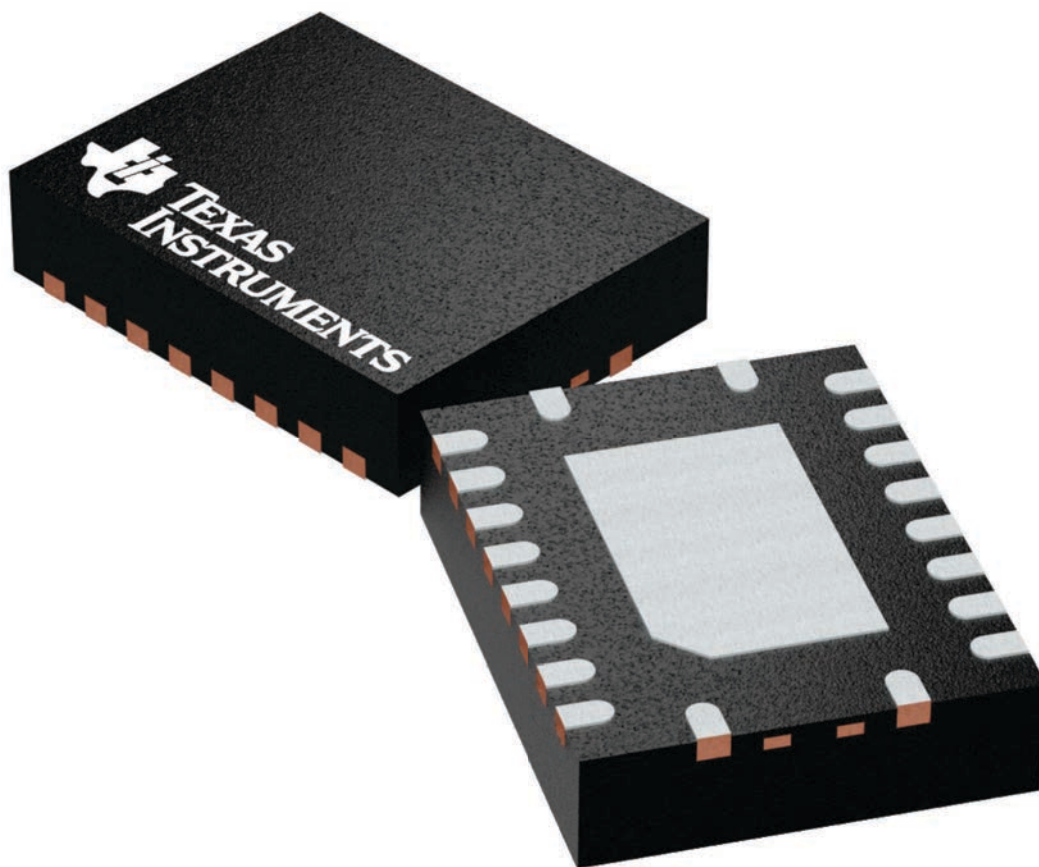
**RGY 20**

**VQFN - 1 mm max height**

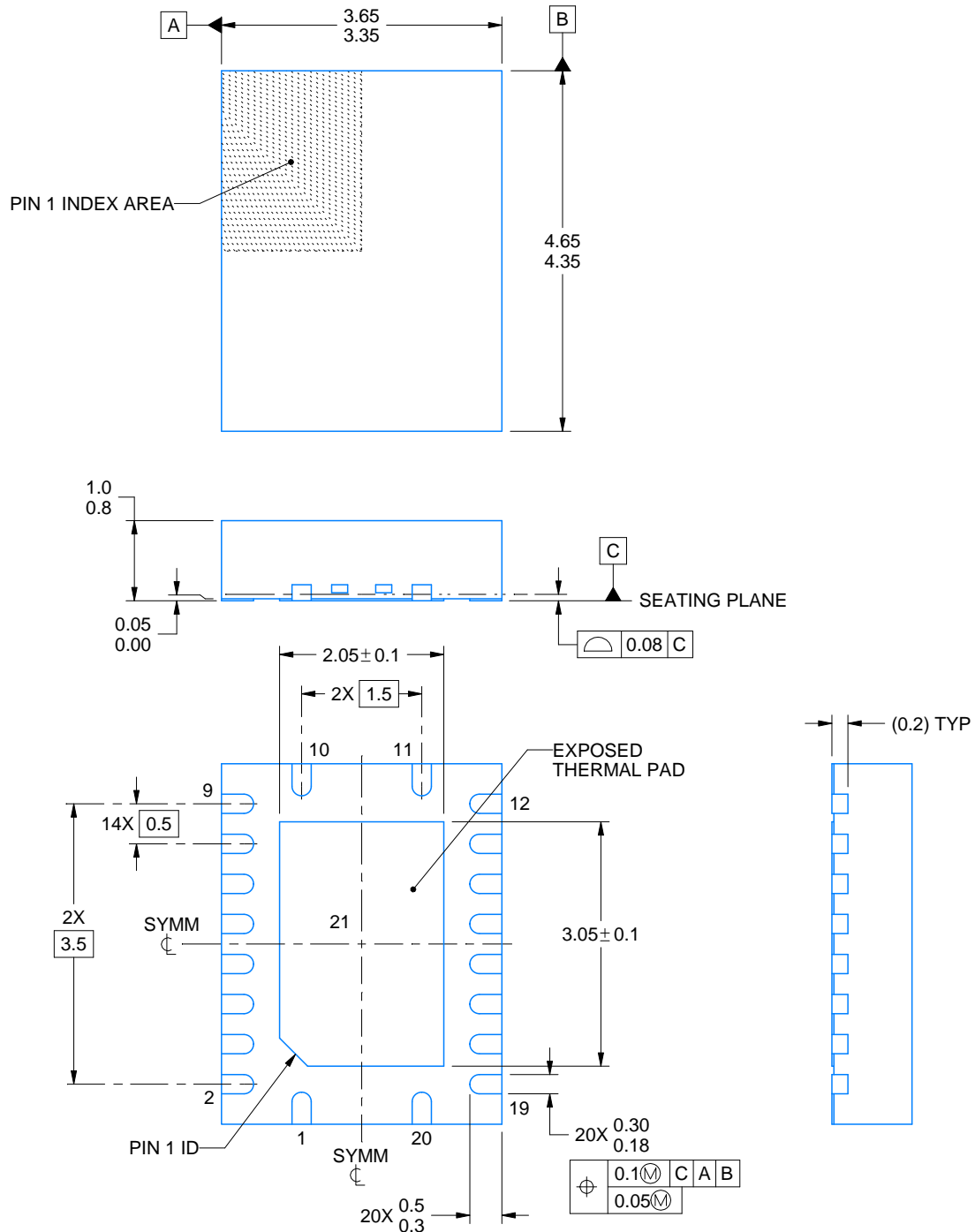
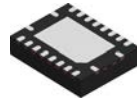
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

#### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

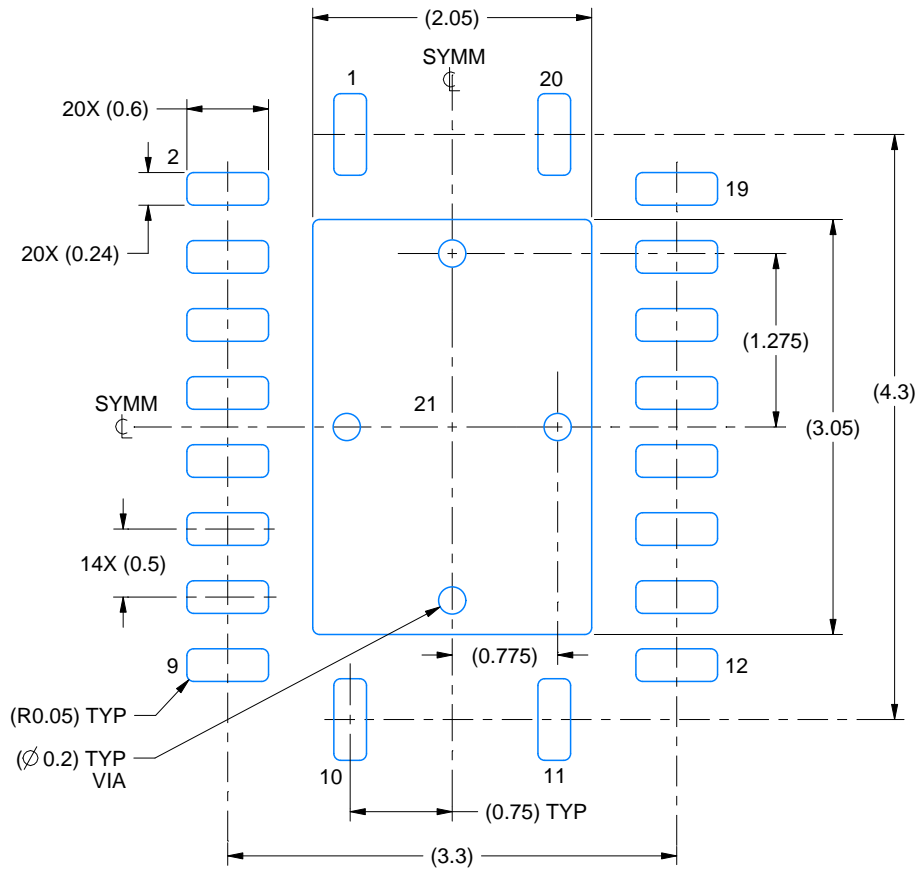


# EXAMPLE BOARD LAYOUT

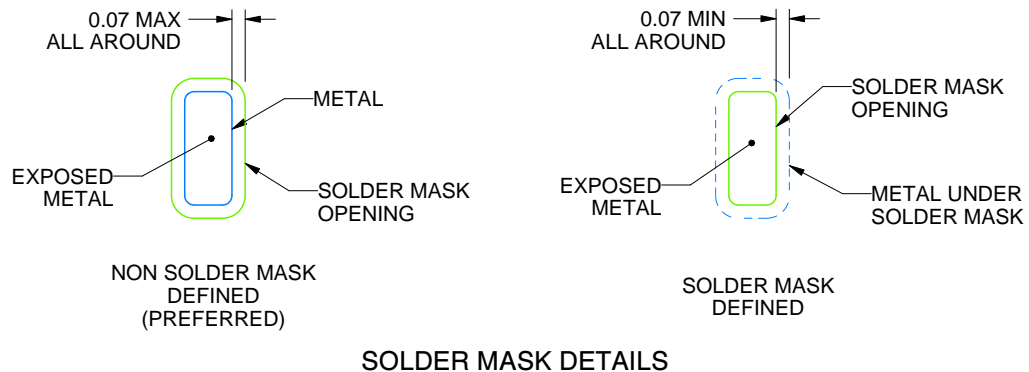
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



4225320/A 09/2019

NOTES: (continued)

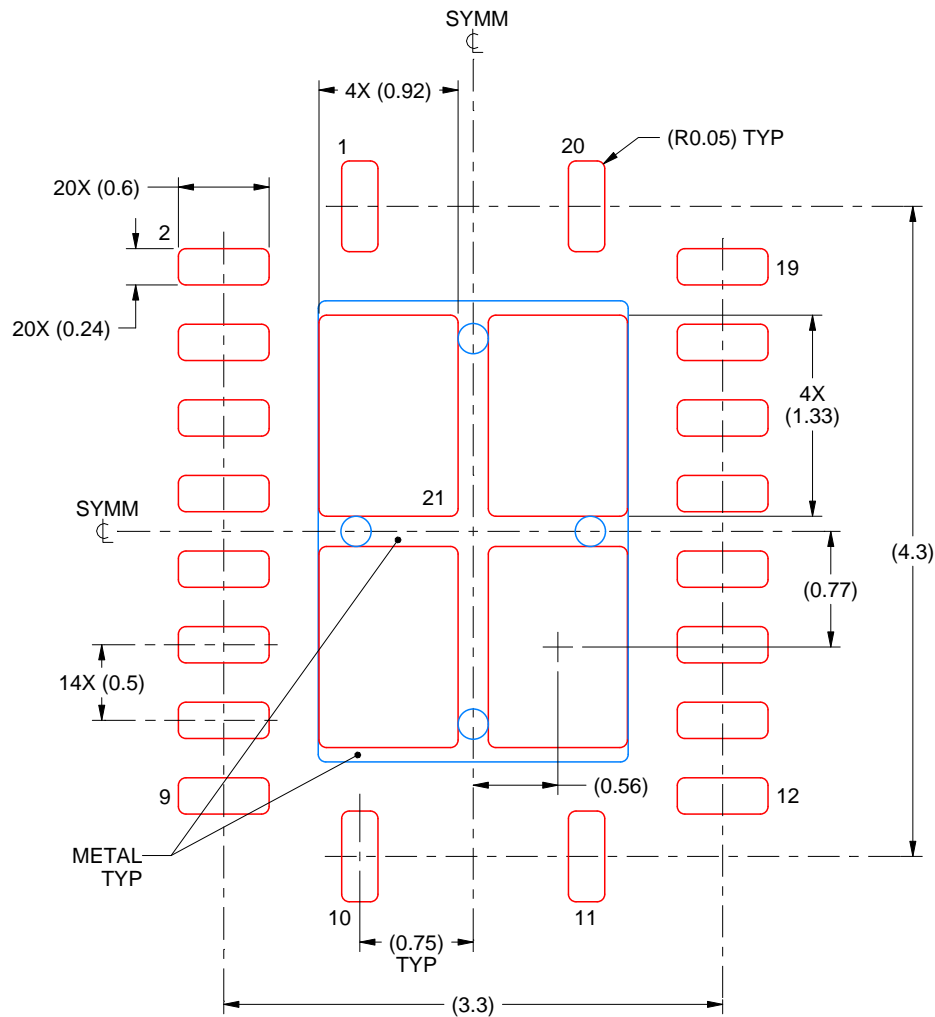
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



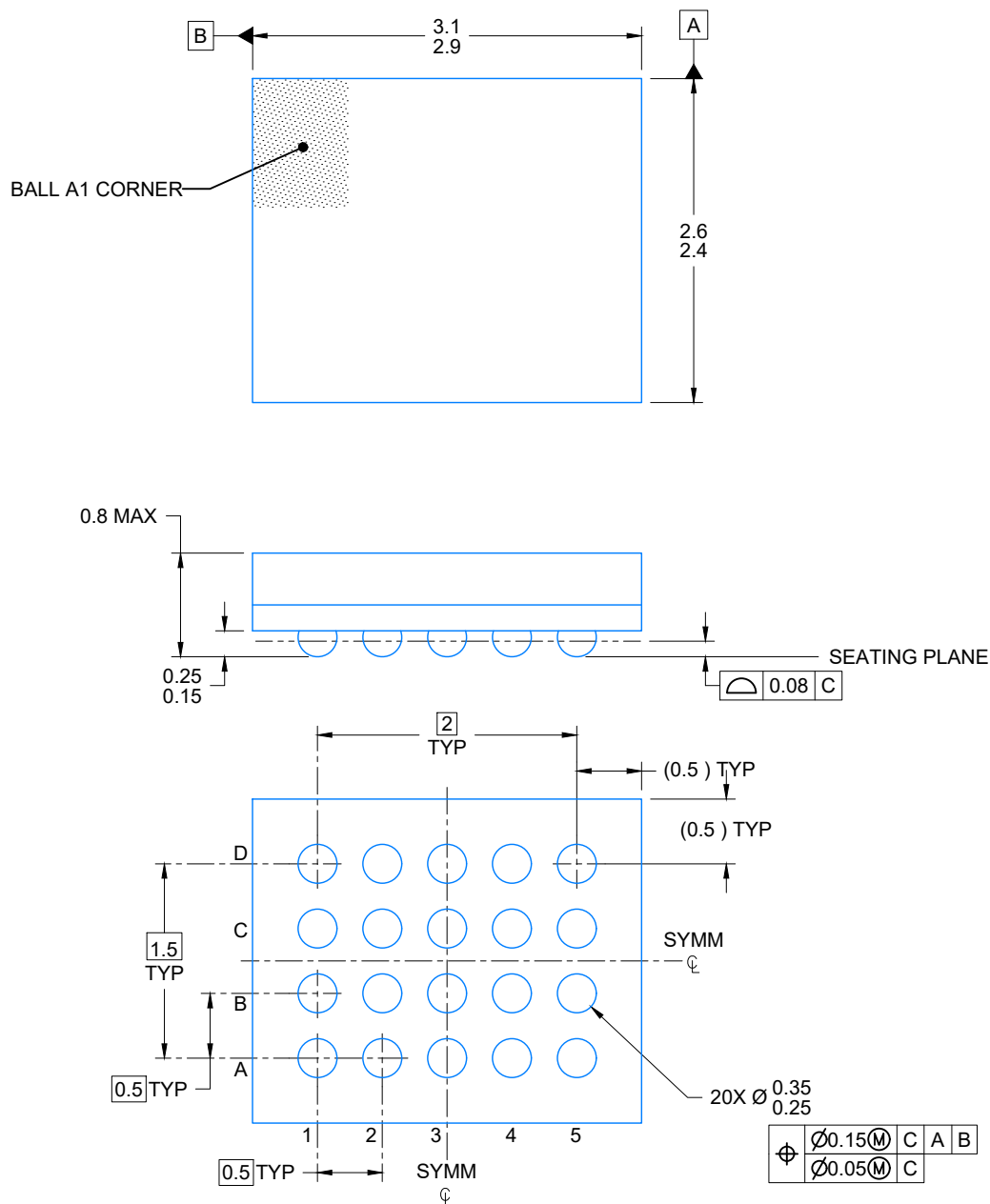
**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

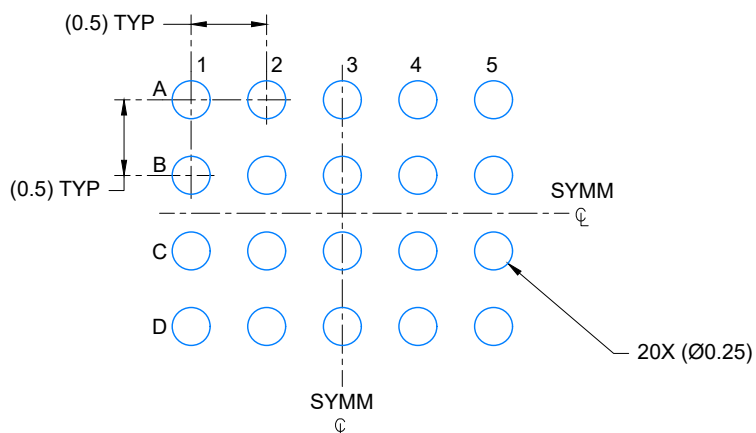


4224888/B 08/2019

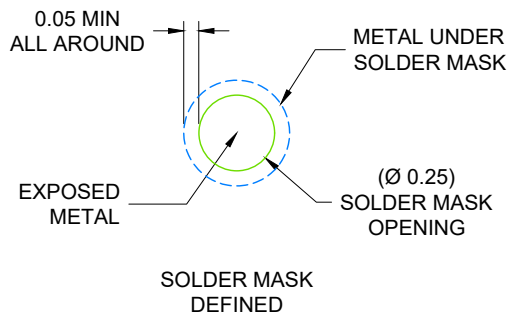
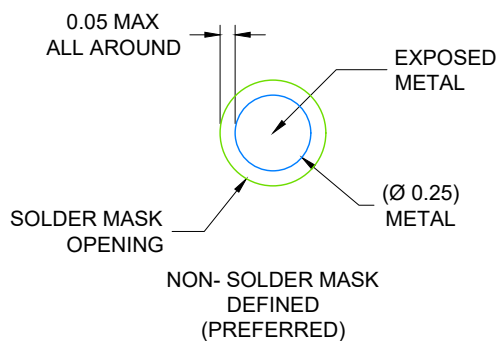
NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE  
SCALE: 20X



SOLDER MASK DETAILS  
NOT TO SCALE

4224888/B 08/2019

NOTES: (continued)

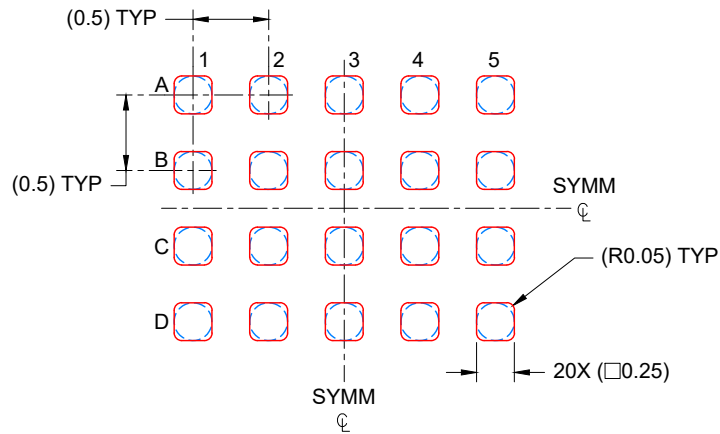
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

NME0020A

NFBGA - 0.8 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.100 mm THICK STENCIL  
SCALE: 20X

4224888/B 08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



## VFBGA - 0.61 mm max height

## PLASTIC BALL GRID ARRAY



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

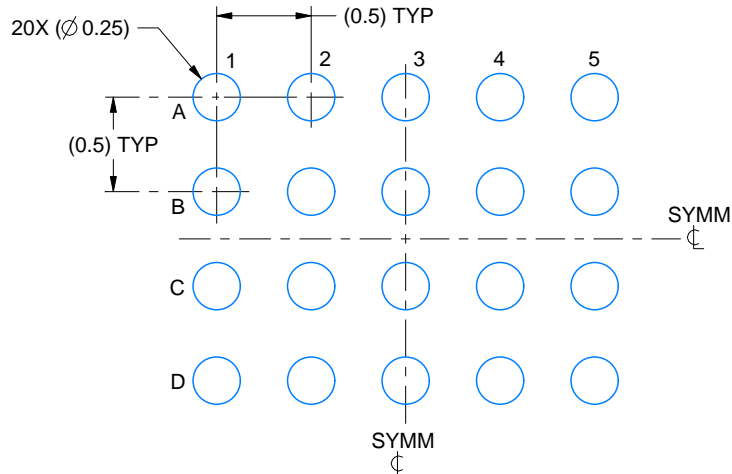
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

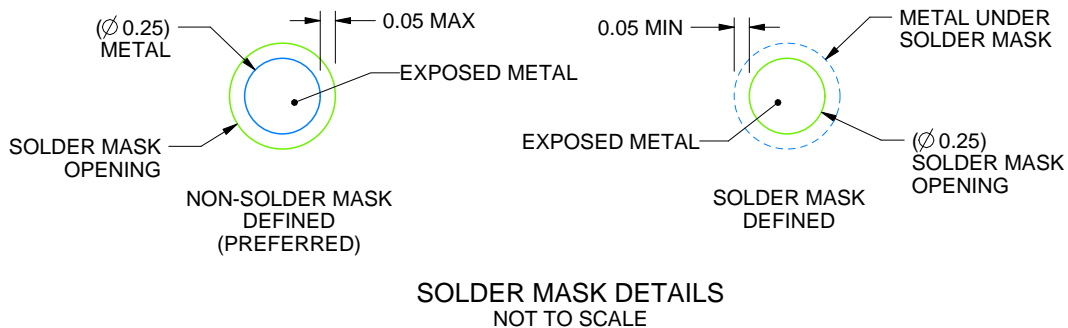
ZXY0020A

VFBGA - 0.61 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:25X



4222996/A 12/2016

NOTES: (continued)

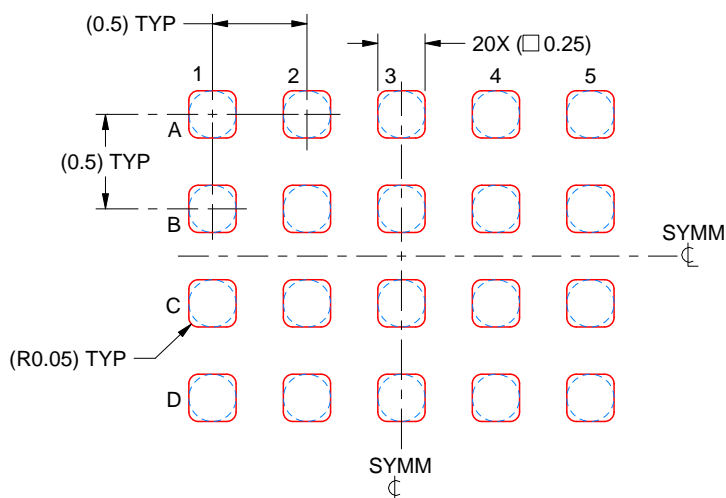
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

## EXAMPLE STENCIL DESIGN

ZXY0020A

VFBGA - 0.61 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 25X

4222996/A 12/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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