Twin Lakes M/B

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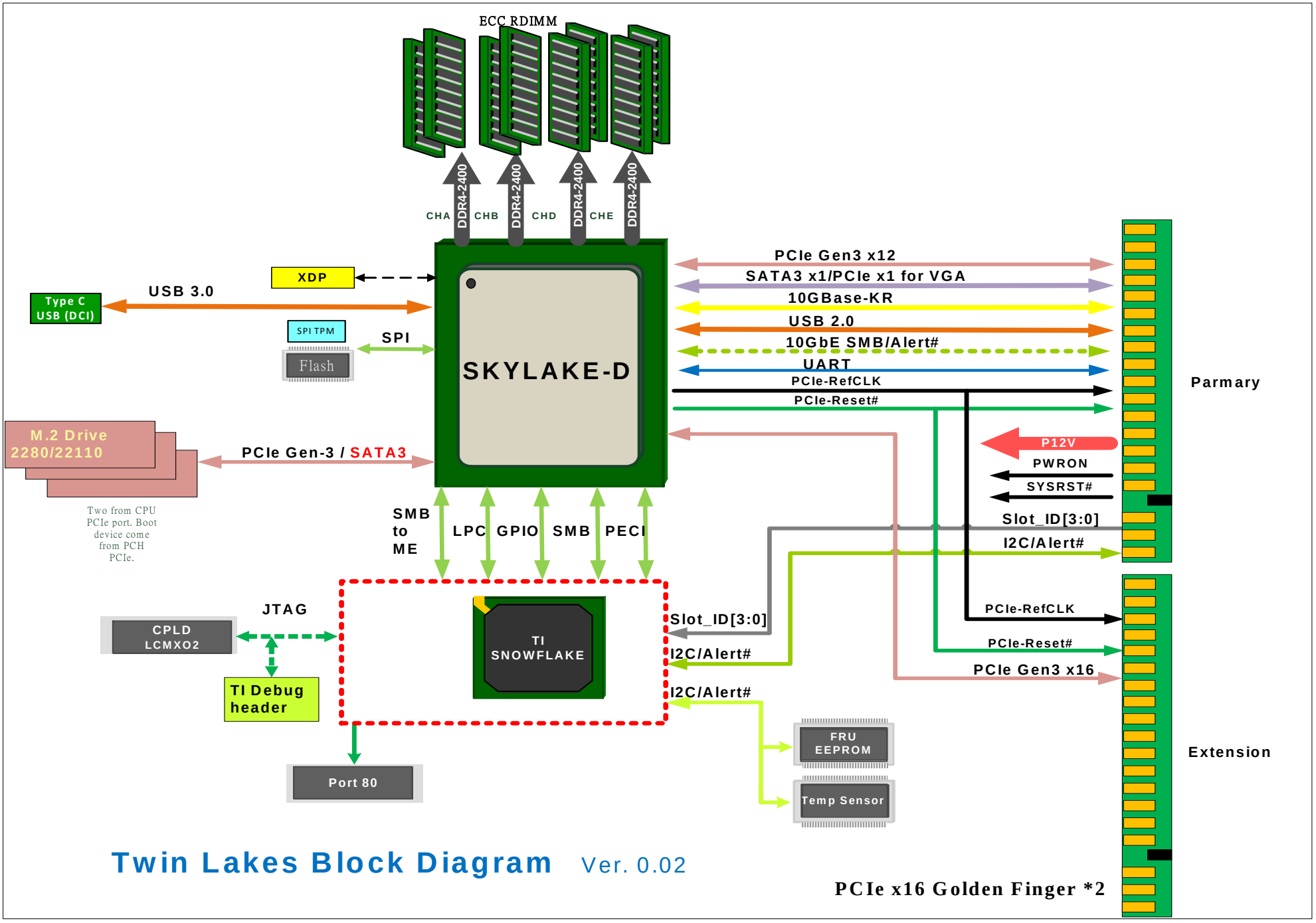
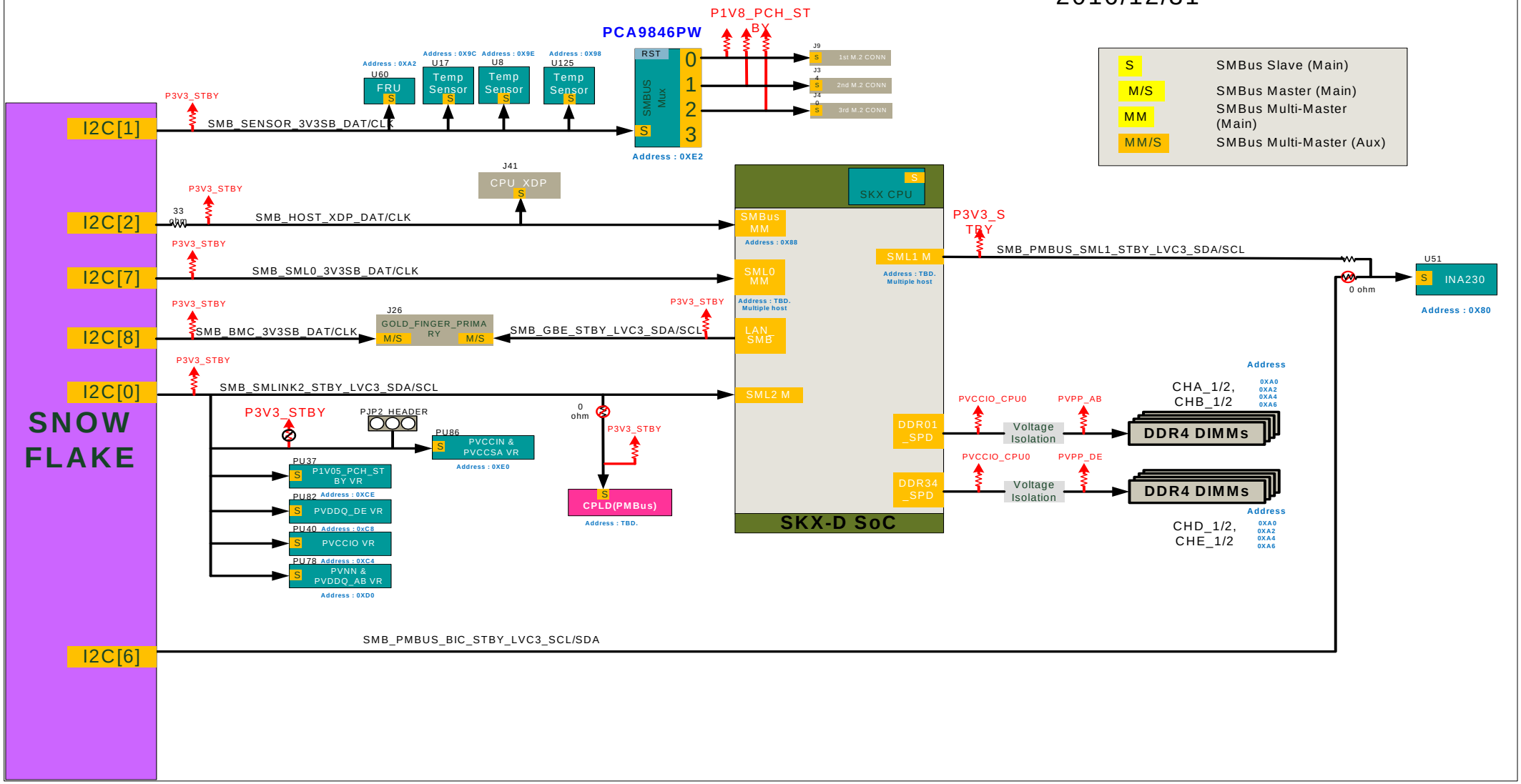


Twin Lakes Block Diagram Ver. 0.02

Twin Lakes BLOCK DIAGRAM

Twin Lakes SMBus TOPOLOGY

2016/12/31



SMBUS BLOCK DIAGRAM

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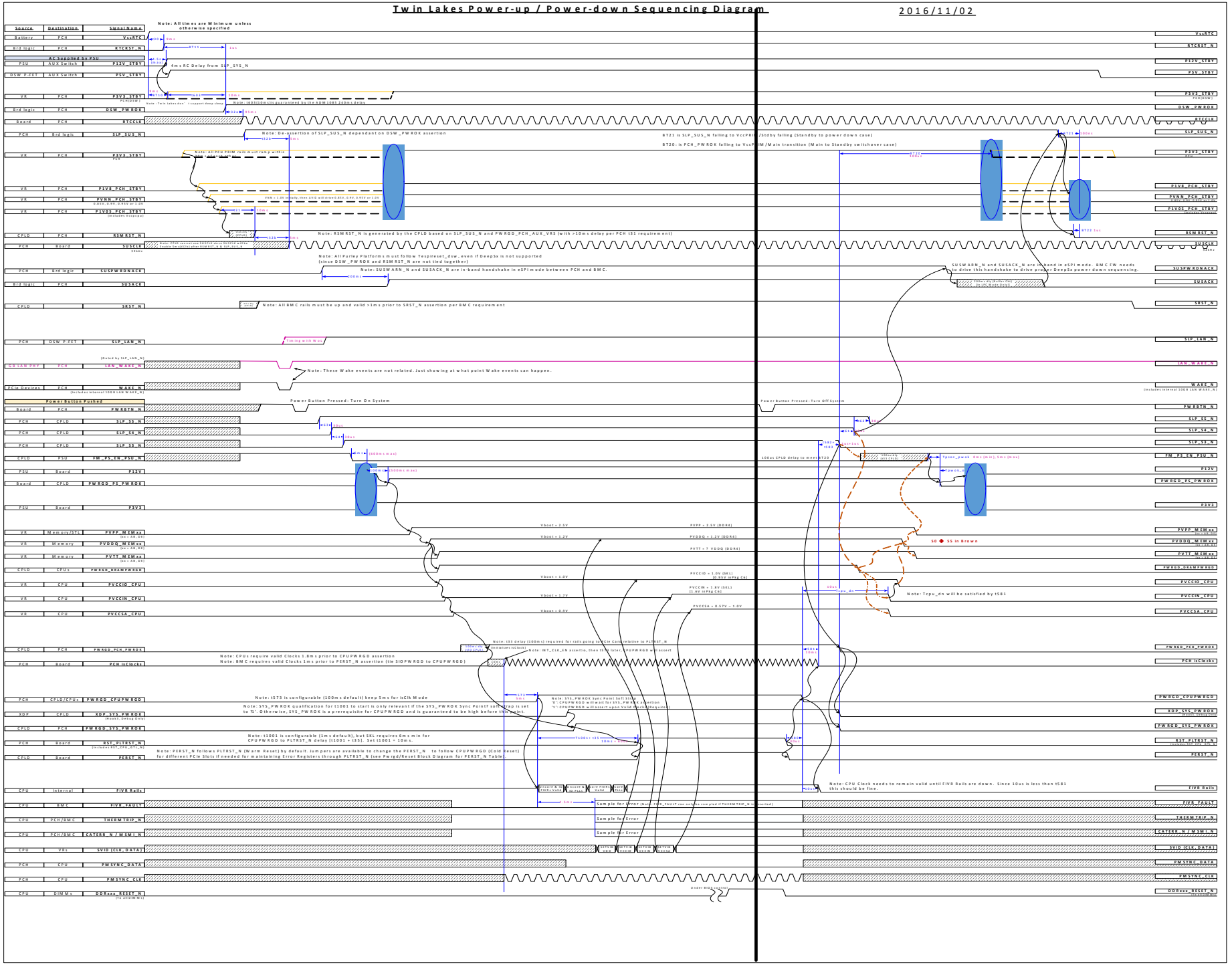

POWER SEQUENCE DIAGRAM

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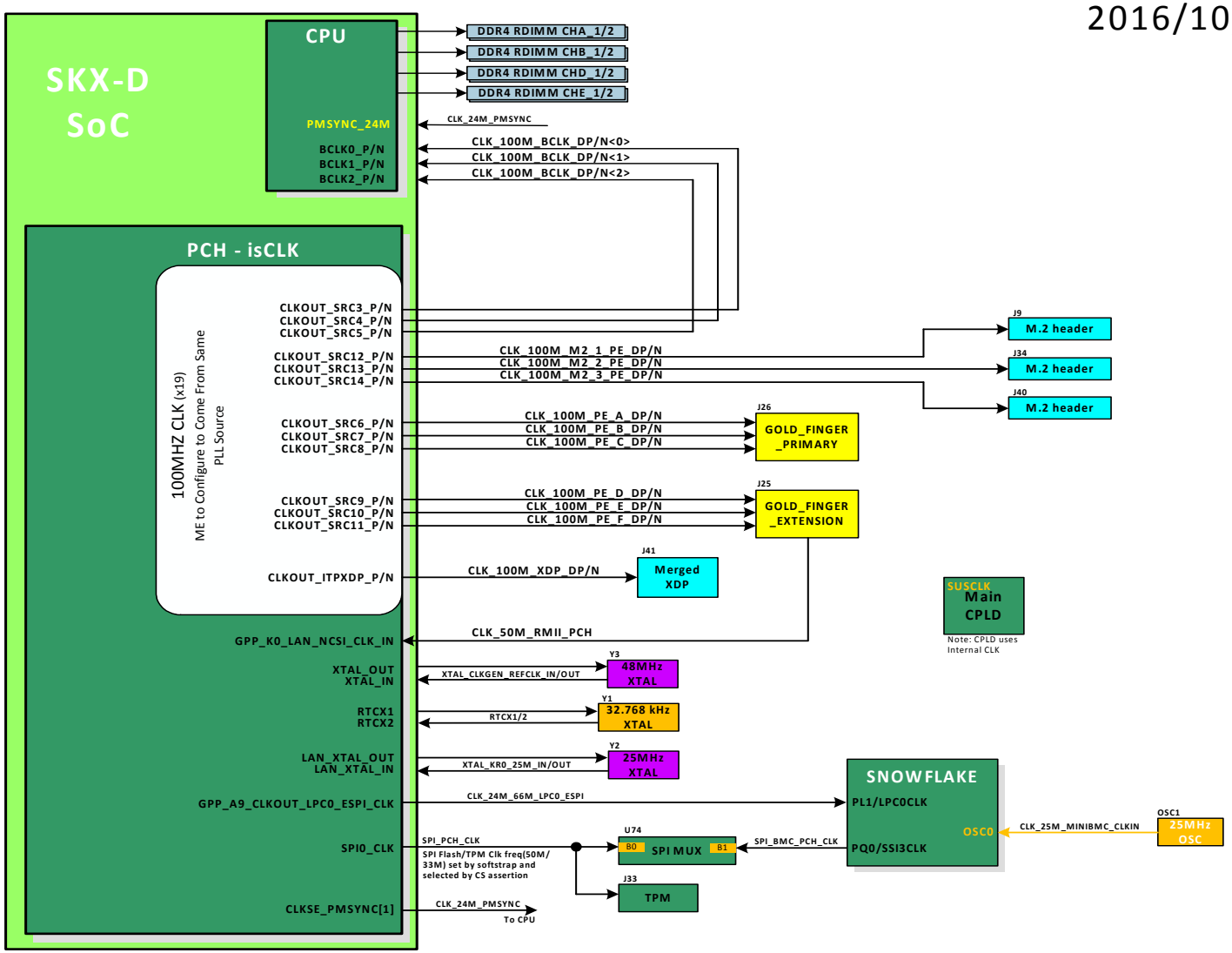
Twin Lakes Clock Block Diagram

2016/10/14



CLOCK DIAGRAM

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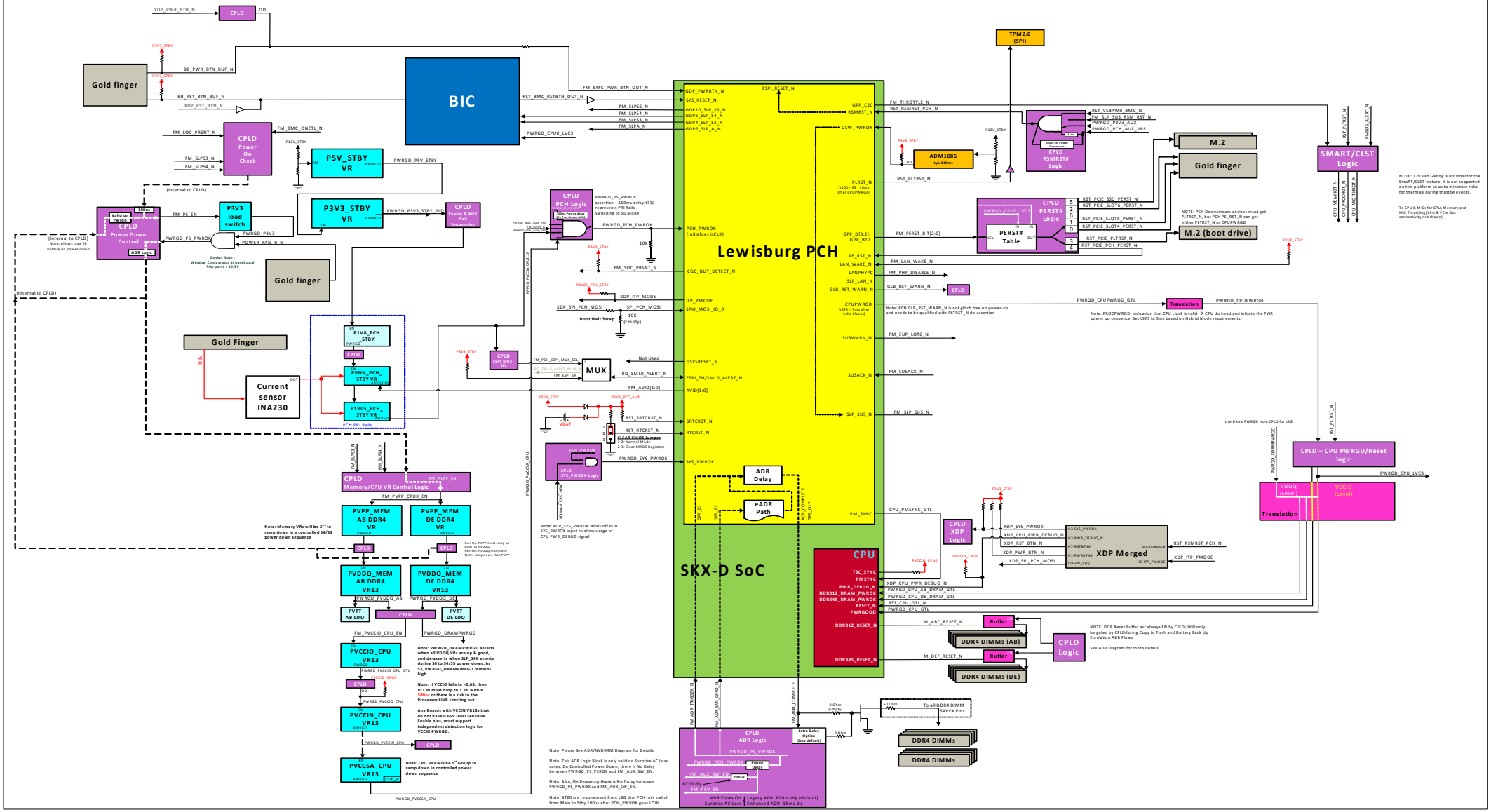
Power Good/ Reset Block Diagram

Note : It was referred to Yuba City Diagram

2016/11/3

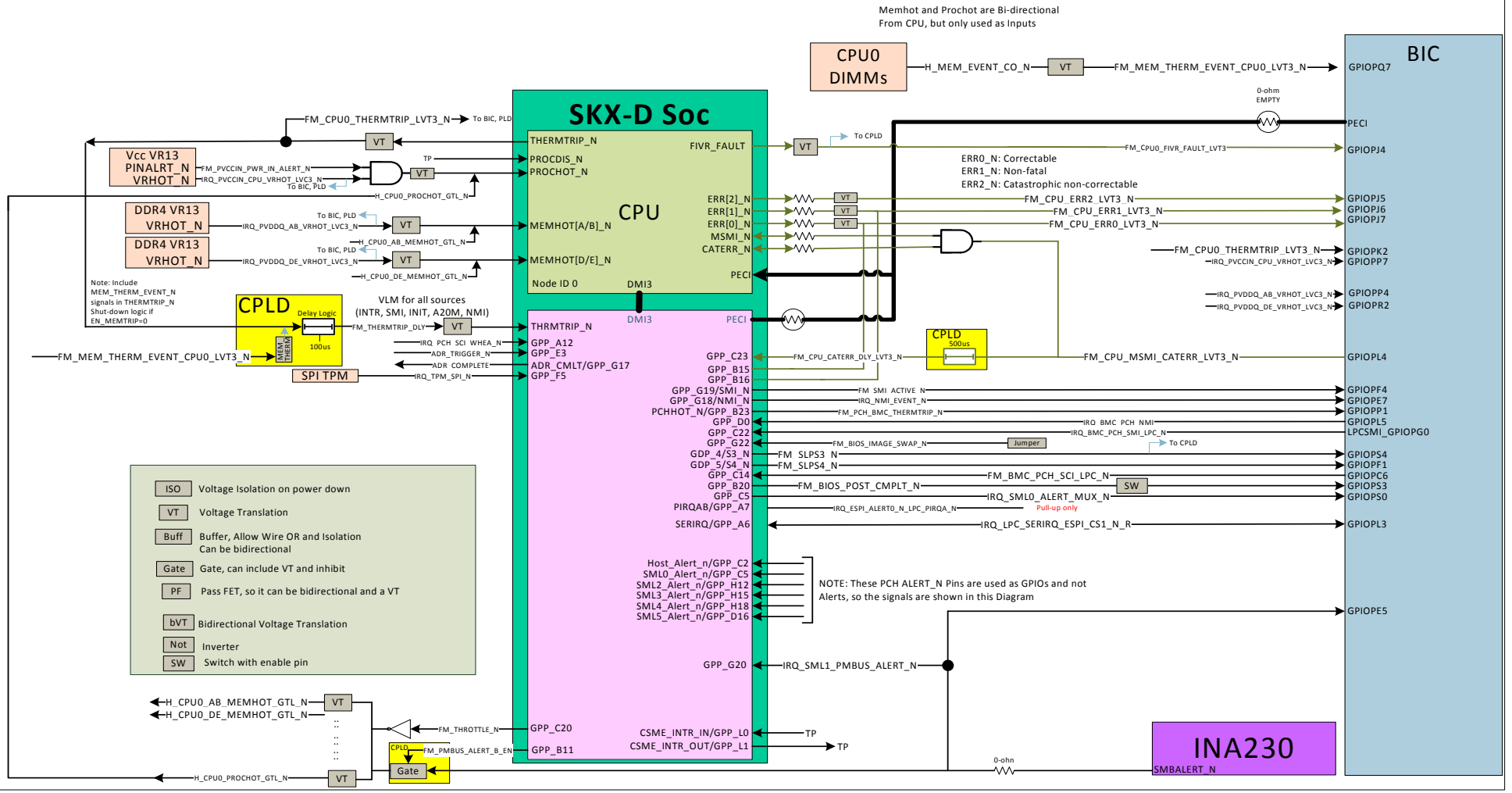


PWRGD/RST DIAGRAM

Twin Lakes Interrupt/ Error Block Diagram

Note : This diagram is refer to Yuba City block diagram.

2016/10/26



INTERRUPT/ERROR ESCALATION

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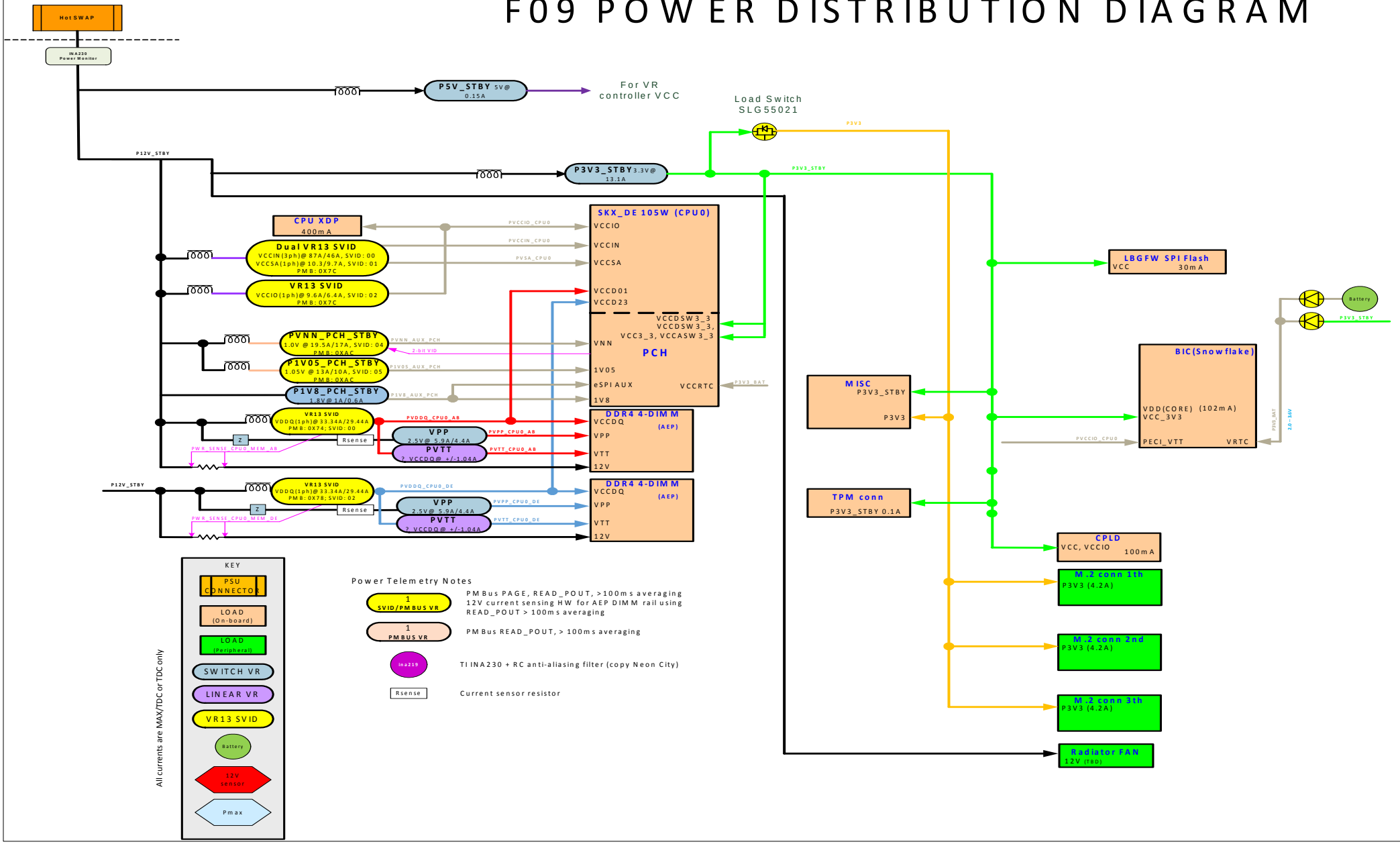
F09 POWER DISTRIBUTION DIAGRAM



POWER TOPOLOGY

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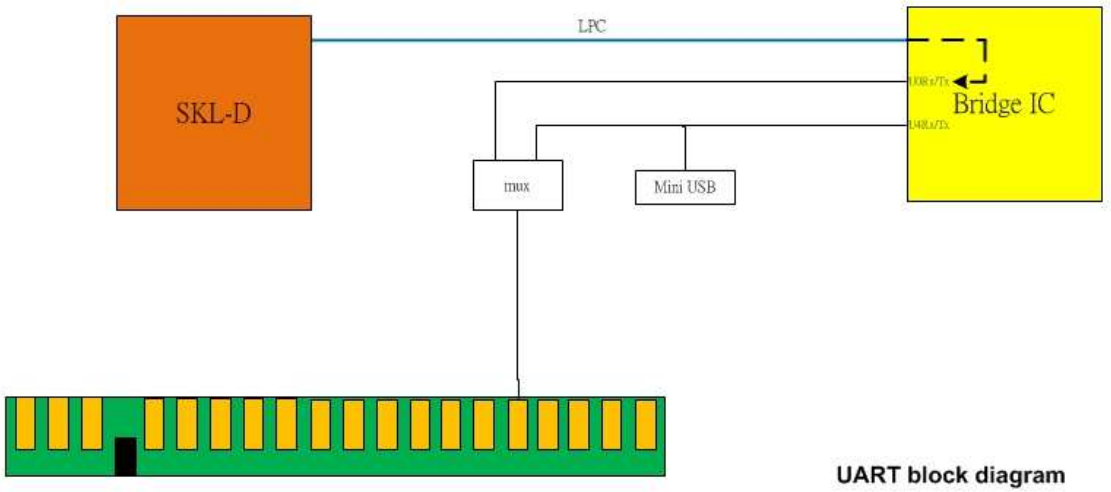

UART block diagram

BRIDGR IC BLOCK DIAGRAM

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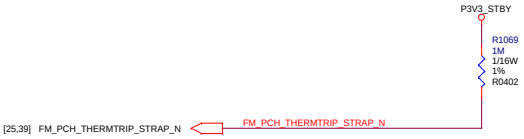
ESPI OR LPC

0 : LPC

EXI BOOT STALLBYPASS (DFX)



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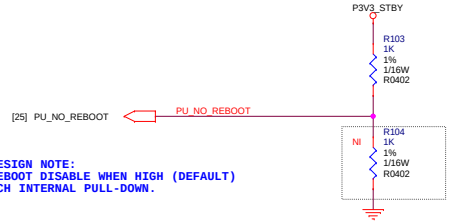
DESIGN NOTE:
EXI BOOT STALL BYPASS DISABLE WHEN LOW (DEFAULT)
PCH INTERNAL PULL-DOWN. DISABLED AFTER STRAP SAMPLING
FOR ENABLE EXI BOOT REPLACE PU TO 1K

NO REBOOT STRAP



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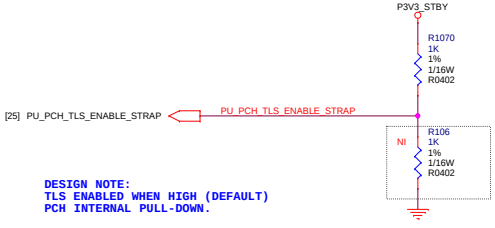
DESIGN NOTE:
REBOOT DISABLE WHEN HIGH (DEFAULT)
PCH INTERNAL PULL-DOWN.

TLS CONFIDENTIALITY



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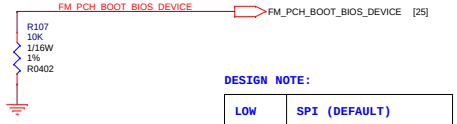
DESIGN NOTE:
TLS ENABLED WHEN HIGH (DEFAULT)
PCH INTERNAL PULL-DOWN.

BOOT BIOS DEVICE



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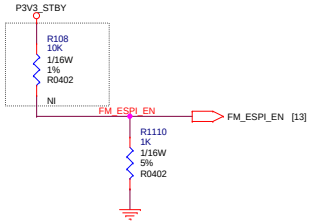
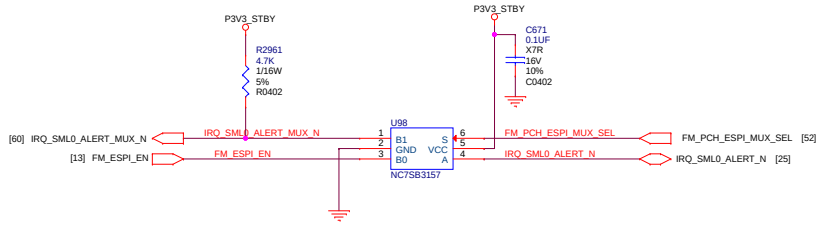
DESIGN NOTE:

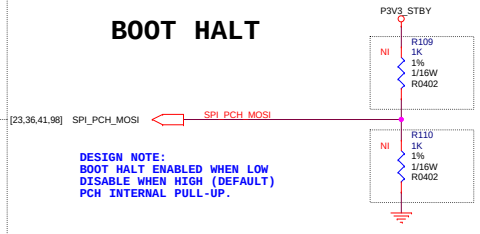
LOW	SPI (DEFAULT)
HIGH	LPC / ESPI

PCH HAS INTERNAL PULL-DOWN





BOOT HALT



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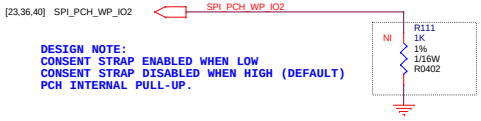
DESIGN NOTE:
BOOT HALT ENABLED WHEN LOW
DISABLE WHEN HIGH (DEFAULT)
PCH INTERNAL PULL-UP.

CONSENT STRAP



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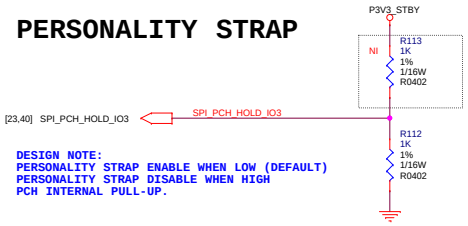
DESIGN NOTE:
CONSENT STRAP ENABLED WHEN LOW
CONSENT STRAP DISABLED WHEN HIGH (DEFAULT)
PCH INTERNAL PULL-UP.

PERSONALITY STRAP



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DESIGN NOTE:
PERSONALITY STRAP ENABLE WHEN LOW (DEFAULT)
PERSONALITY STRAP DISABLE WHEN HIGH
PCH INTERNAL PULL-UP.

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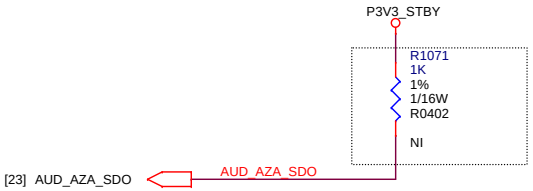
FLASH SECURITY OVERRIDE



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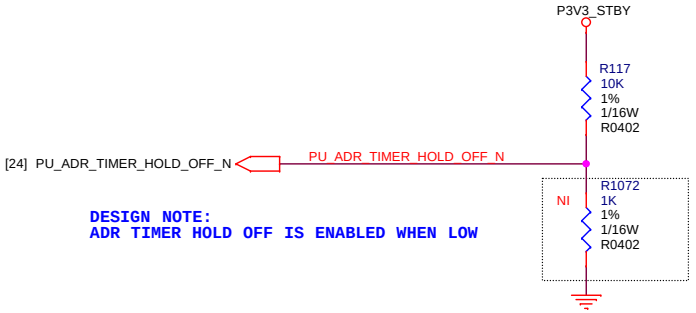
DESIGN NOTE:

LOW	FLASH SECURITY OVERRYDE DISABLE (DEFAULT)
HIGH	FLASH SECURITY OVERRIDE ENABLE

PCH HAS INTERNAL PULL-DOWN

ADR TIMER OFF



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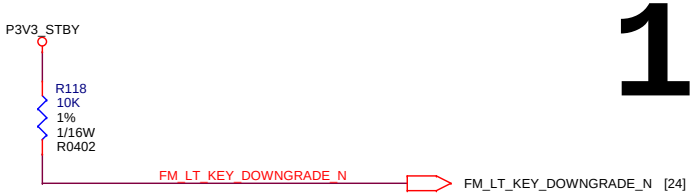
DESIGN NOTE:
ADR TIMER HOLD OFF IS ENABLED WHEN LOW

LT KEY DOWNGRADE



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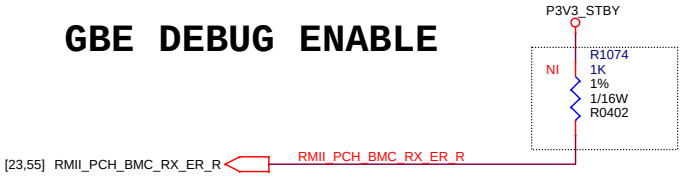
GBE DEBUG ENABLE



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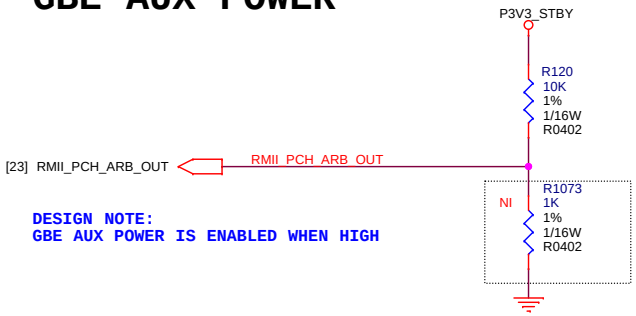
DESIGN NOTE:
GBE DEBUG MODE IS ENABLED WHEN HIGH
PCH HAS INTERNAL PULL-DOWN.

GBE AUX POWER



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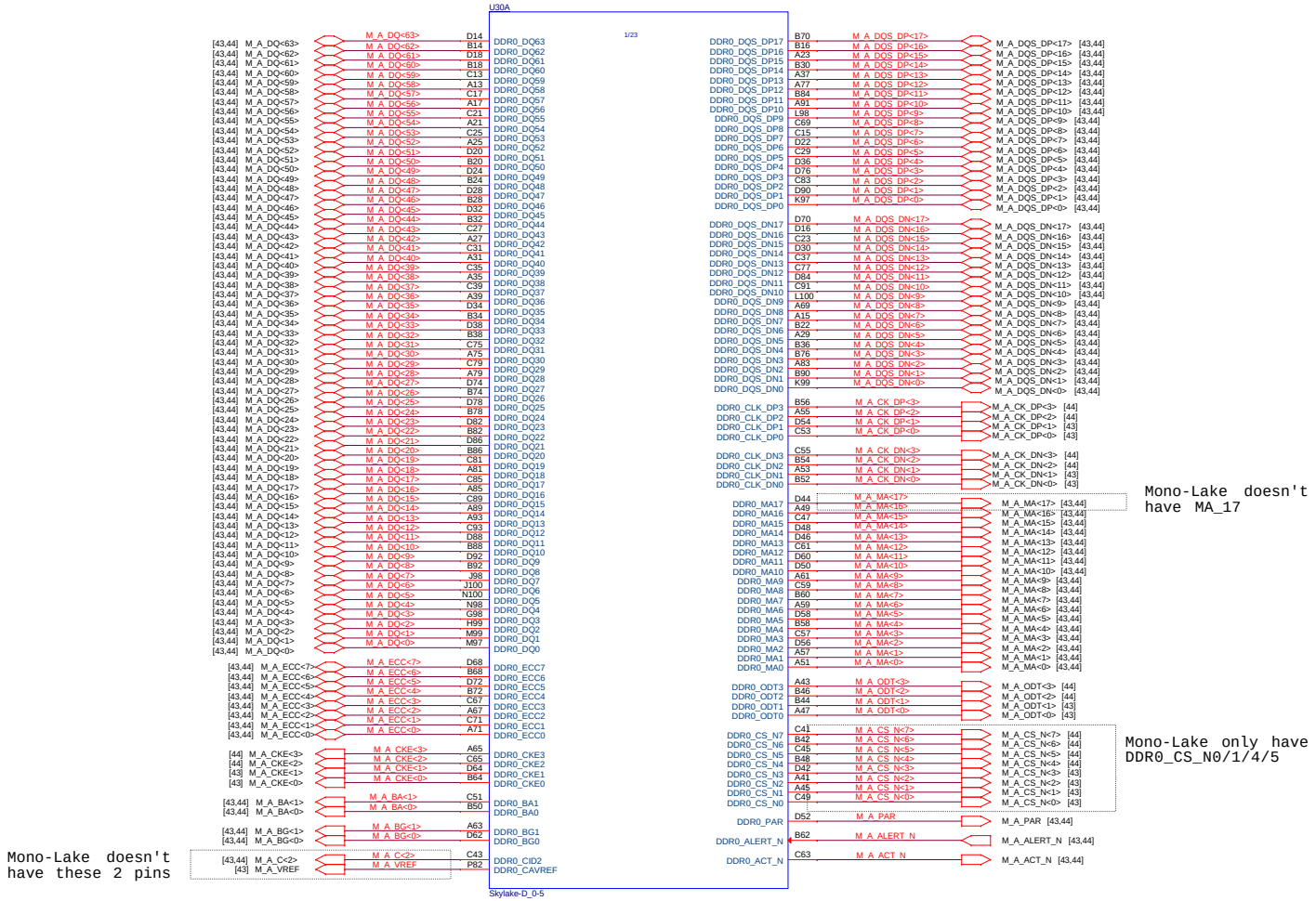
DESIGN NOTE:
GBE AUX POWER IS ENABLED WHEN HIGH



SKL-D DDR4 CHANNEL A

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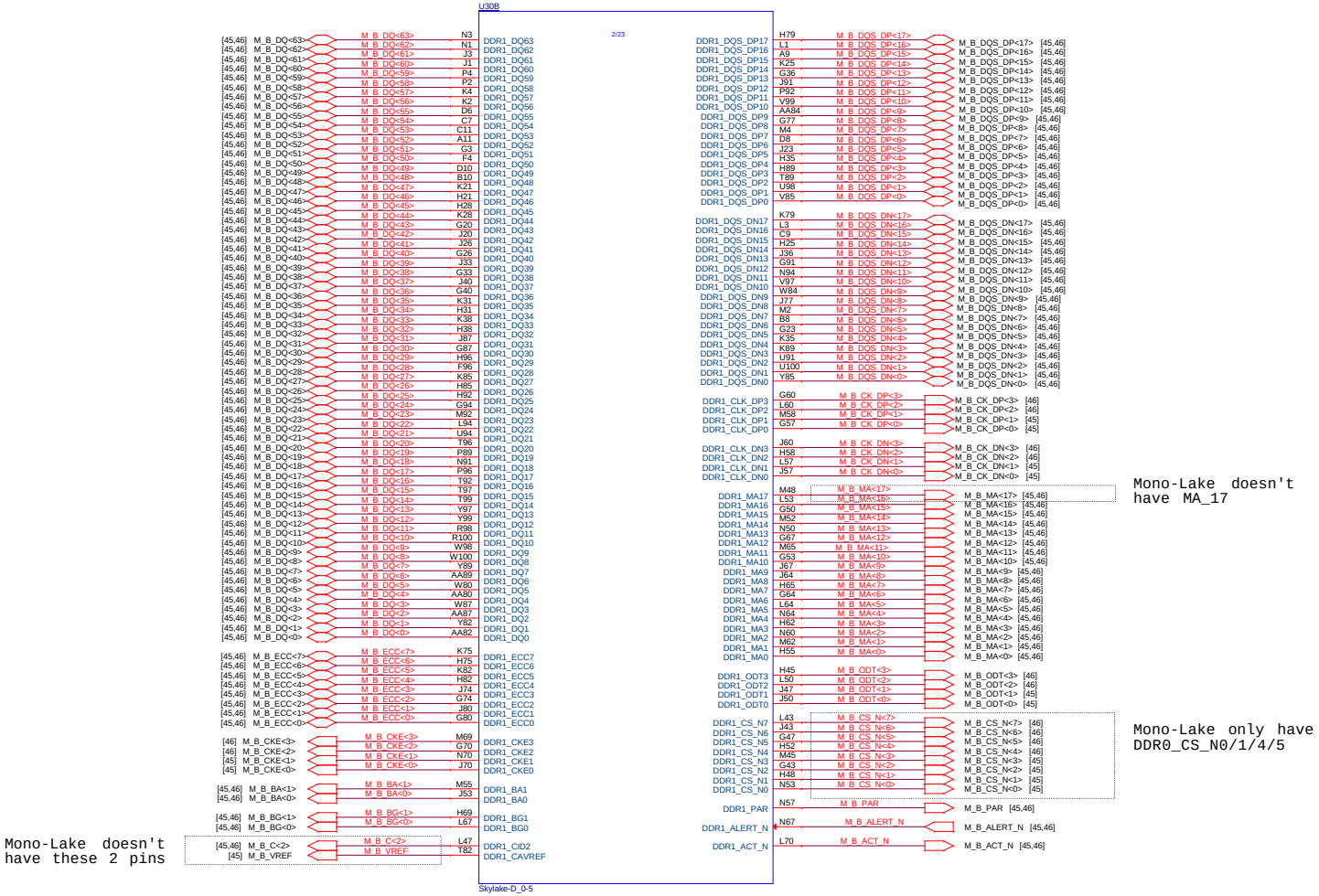

SKL-D DDR4 CHANNEL B

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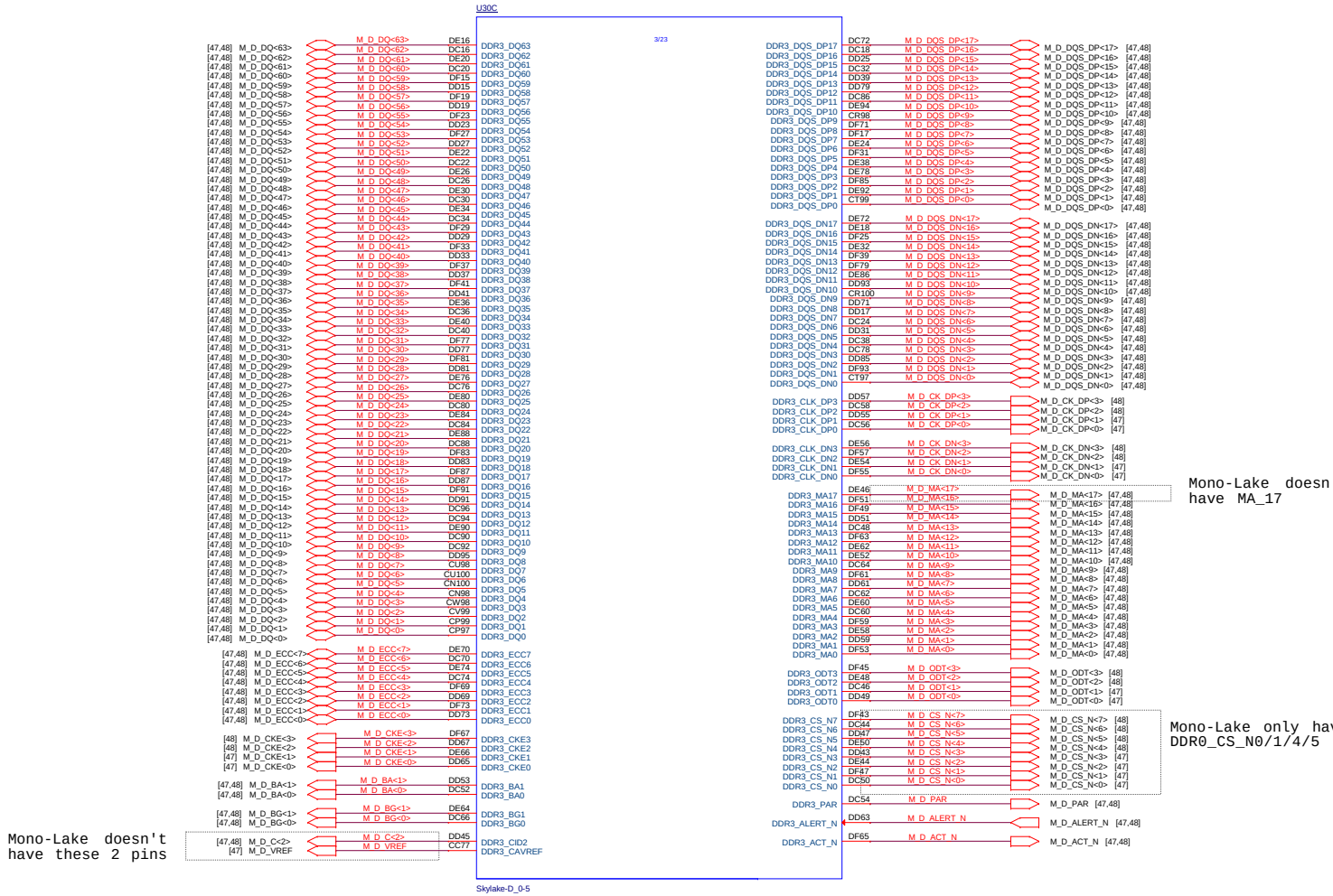

SKL-D DDR4 CHANNEL D

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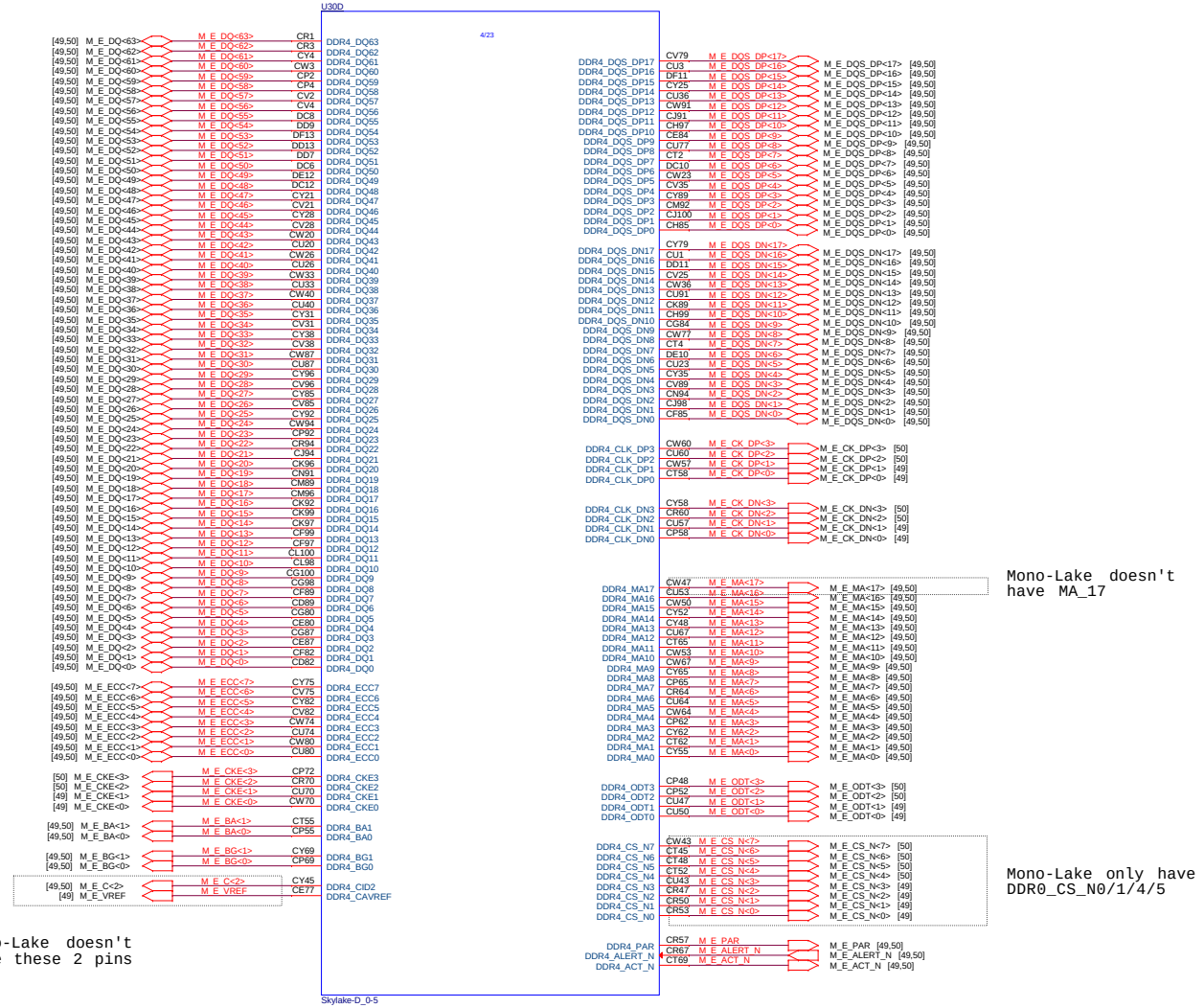

SKL-D DDR4 CHANNEL E

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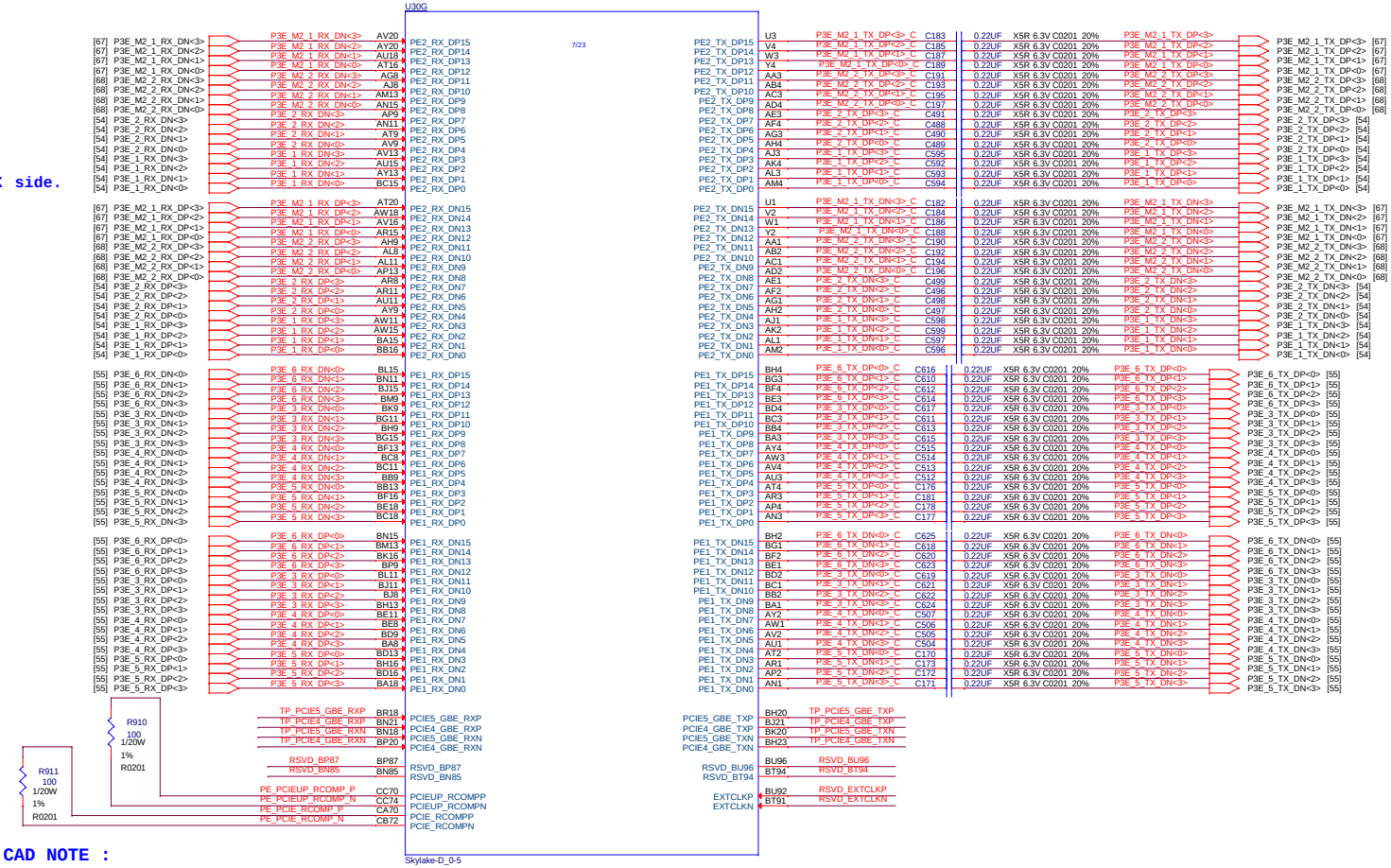
DESIGN NOTE :
Co-layout C211, C212 with C188, C189.
(1) Stuff C211 and C212. Unstuff C188 , C189 for SATA
(2) Stuff C188 , C189. Unstuff C211 and C212 for PCIe.(default)

DESIGN NOTE :
Polarity inversion at RX side.



CAD NOTE :

R910 nad R911 PLACE UNDER SOC CAVITY AREA

SKL-D PCIE CPU/PCH

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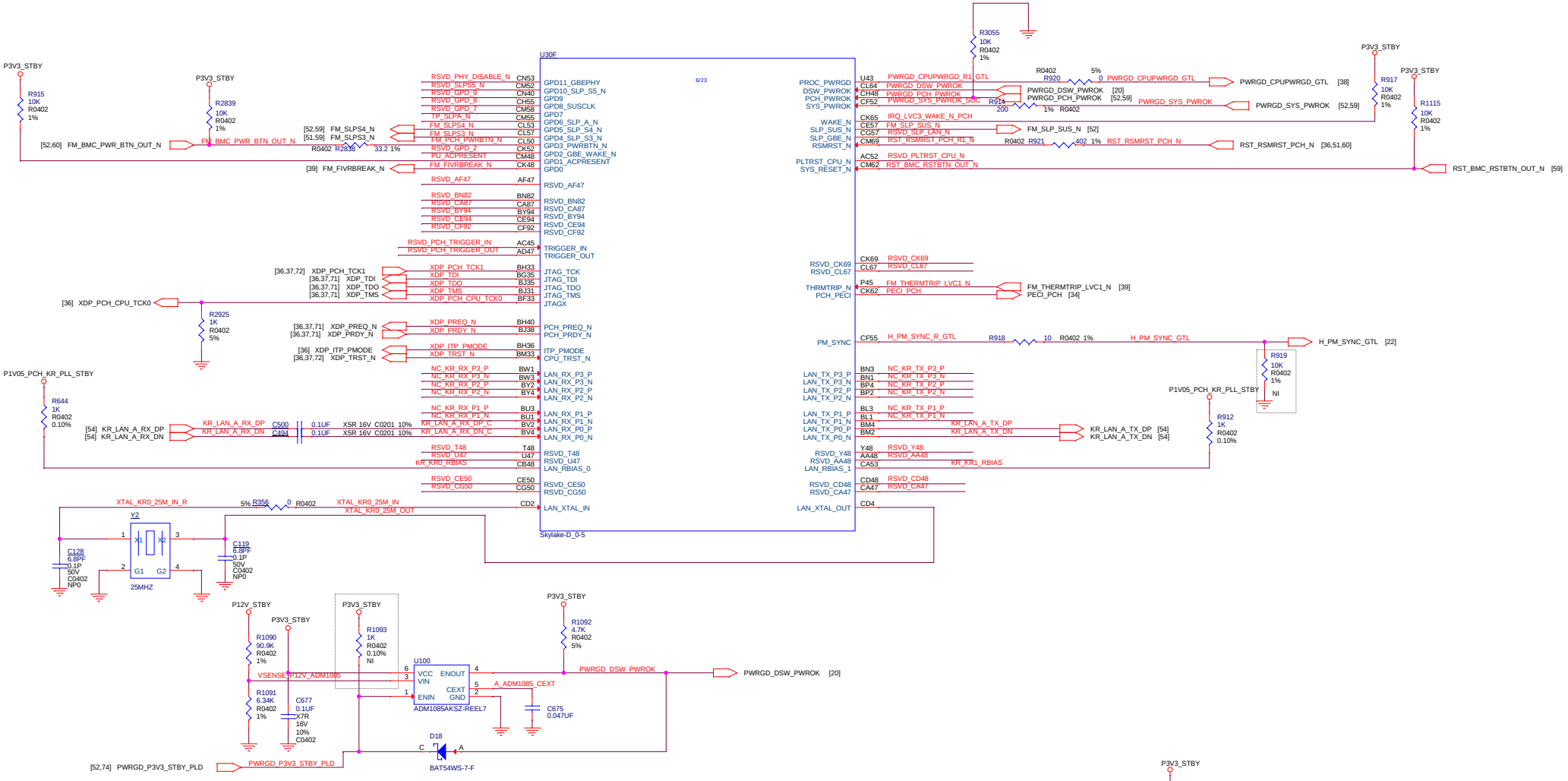

Design note :
(1) VIN Rising Threshold, VTH_RISING Min : 0.56 Typ : 0.6 Max : 0.64 V (VCC = 3.3 V)
(2) VIN Falling Threshold, VTH_FALLING Min : 0.545 Typ : 0.585 Max : 0.625 V (VCC = 3.3 V)

Triggger point :
0.585----->8.97V falling
0.6------>9.2V rising.

Design note :
Baseboard will have a window comparator to monitor P12V_STBY.

SKL-D 10G KR LAN

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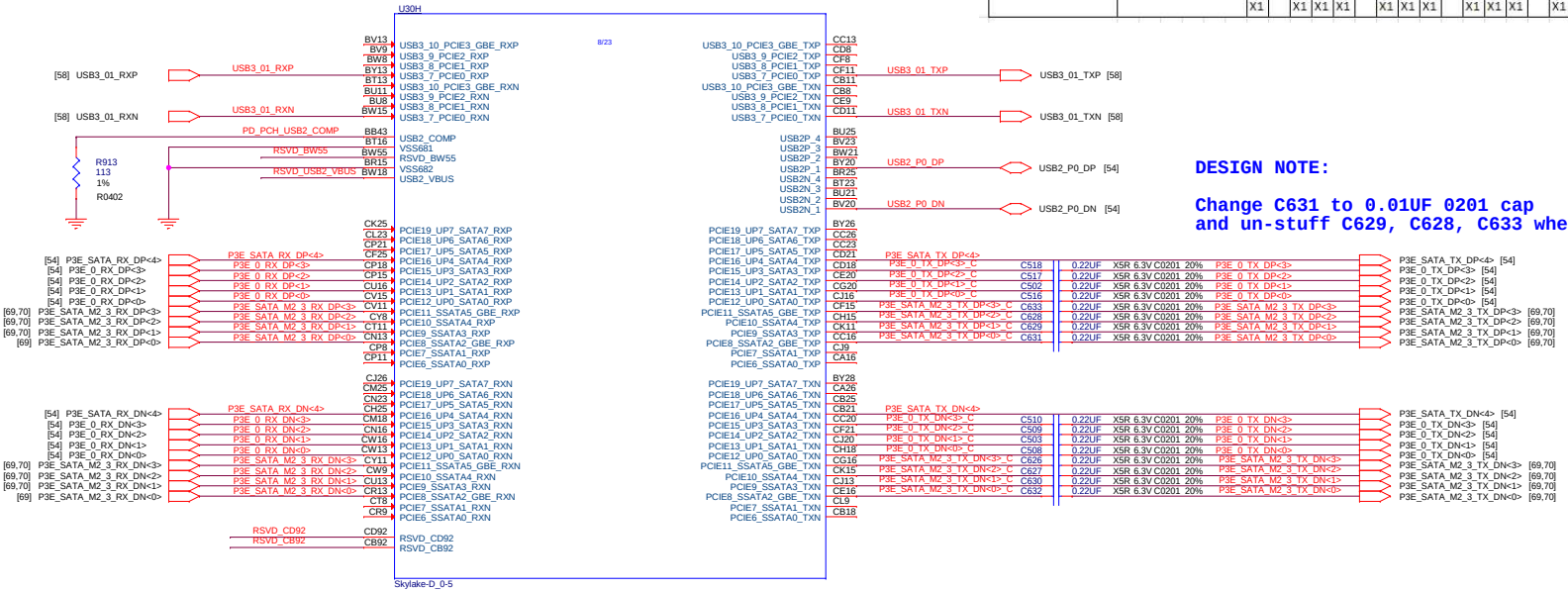
Flex I/O Port #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
USB3							1	2	3	4																
PCIe Root Port							0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
GbE										X	X	X			X			X								
SATA																			0	1	2	3	4	5	6	7
sSATA													0	1	2	3	4	5								
PCIe Uplink																			0	1	2	3	4	5	6	7
PCIe Configurations							X4				X4				X4				X4				X4			
							X2		X1		X2		X1		X2		X1		X2		X1		X2		X1	
							X2		X1	X1	X2		X1	X1	X2		X1	X1	X2		X1	X1	X2		X1	X1
							X1		X1	X1	X1		X1	X1	X1		X1	X1	X1		X1	X1	X1		X1	X1



DESIGN NOTE:

Change C631 to 0.01UF 0201 cap and un-stuff C629, C628, C633 when config to SATA.

SKL-D SATA, USB2, USB3

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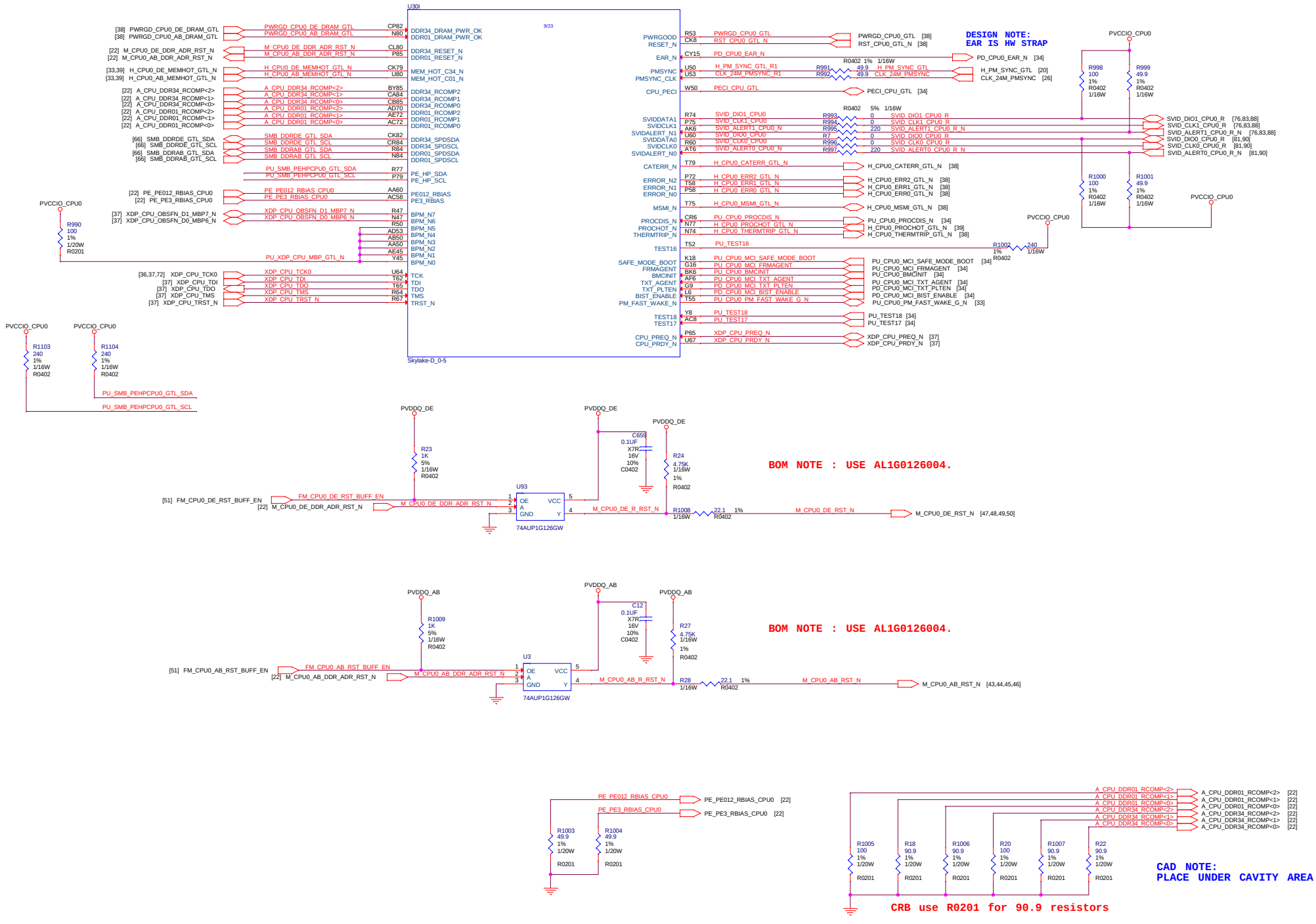

SKL-D LPC,SPI,GPIO,INT,PWR SEQ

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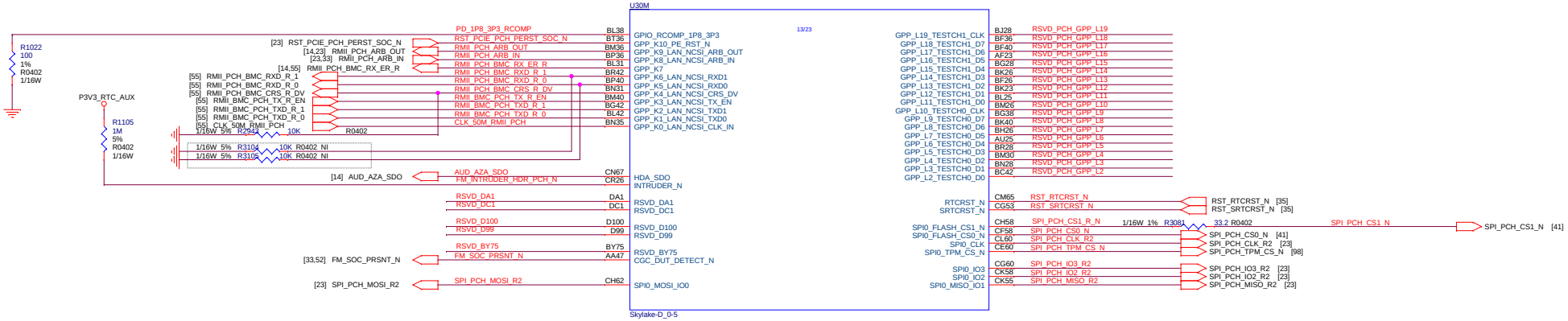
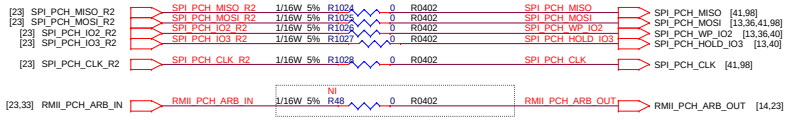


CAD NOTE:
PLACE NEAR SOC BTW 2'' TO 3''



SKL-D UART,JTAG,SVID

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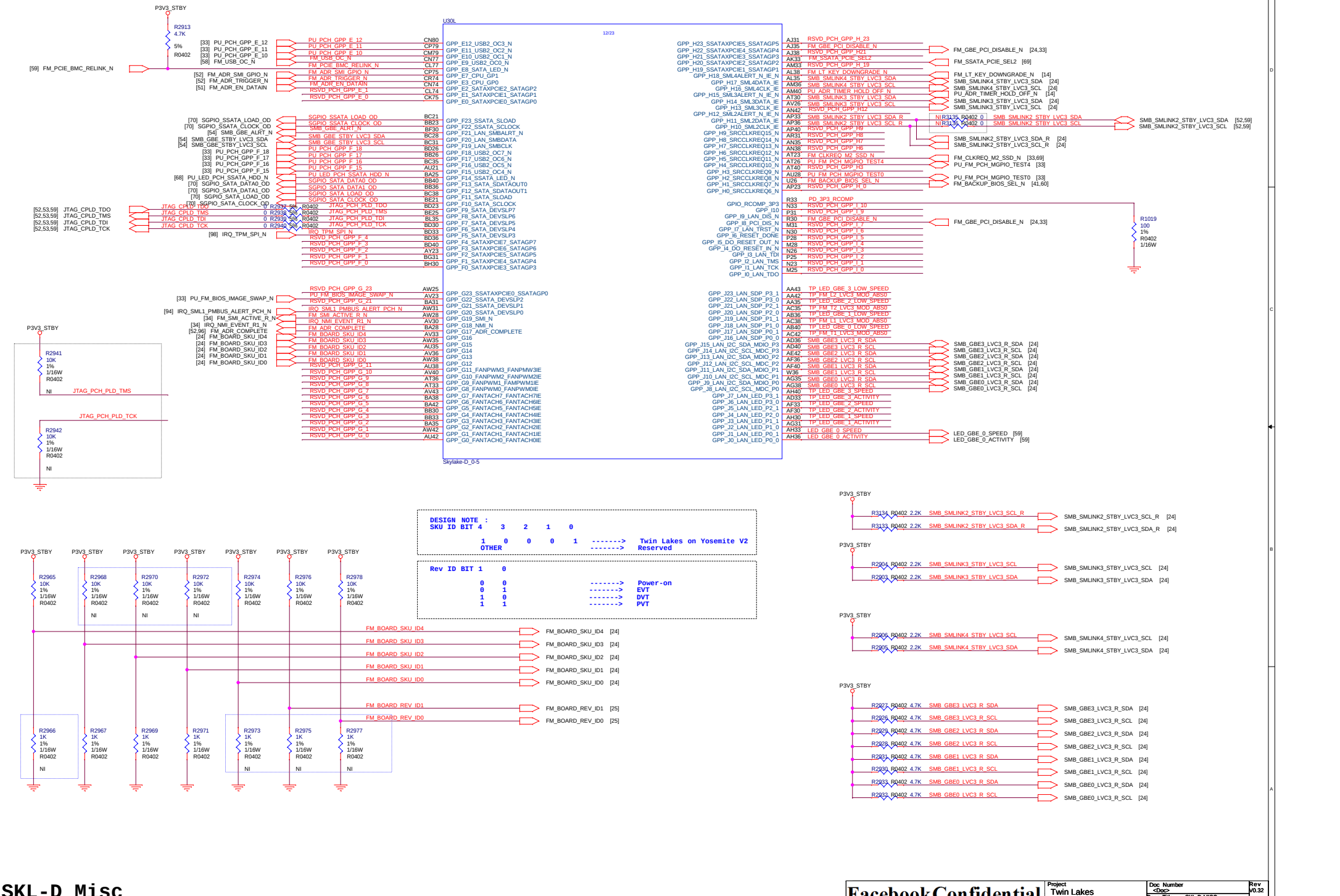

SKL-D Misc

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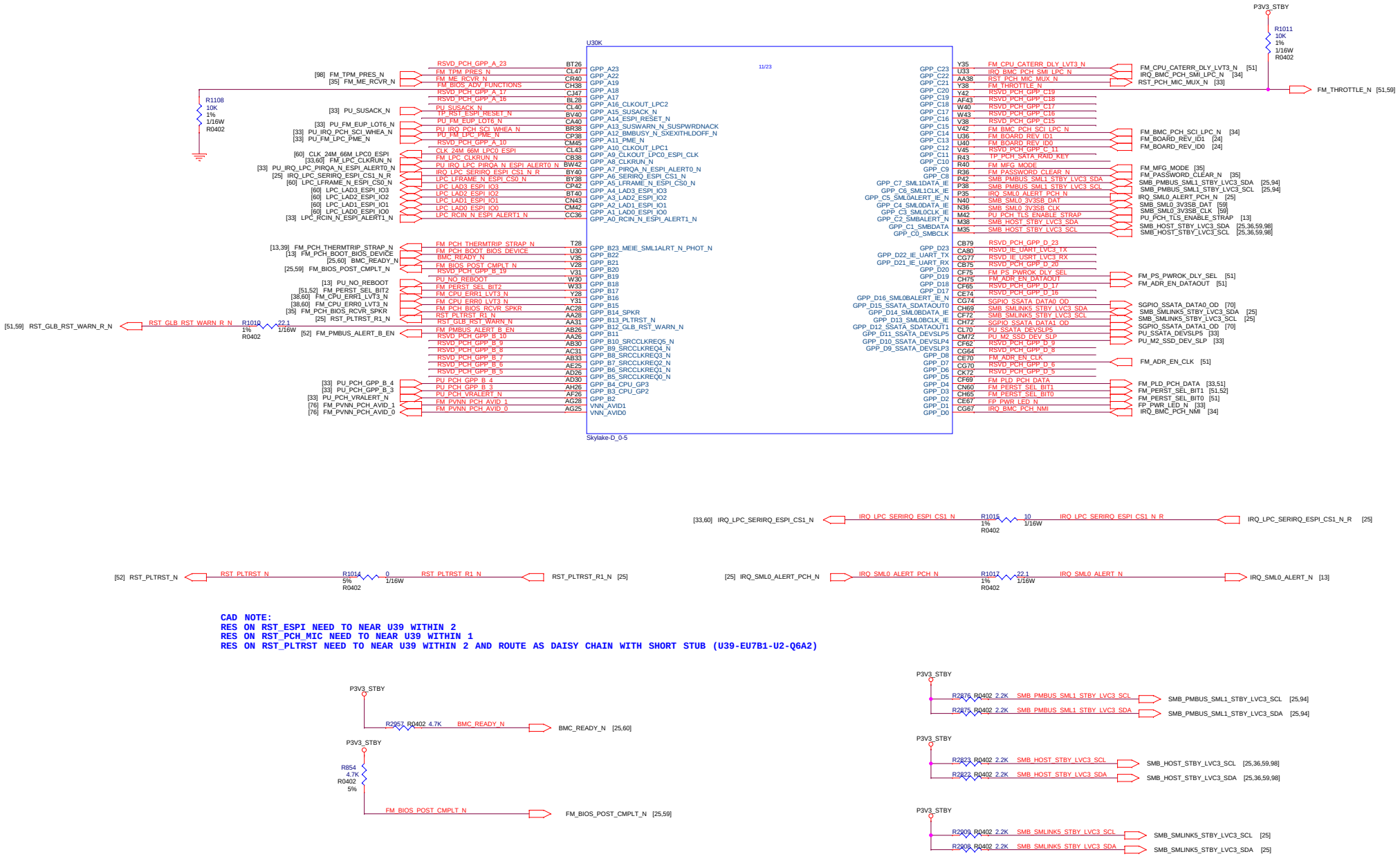

SKL-D GPP

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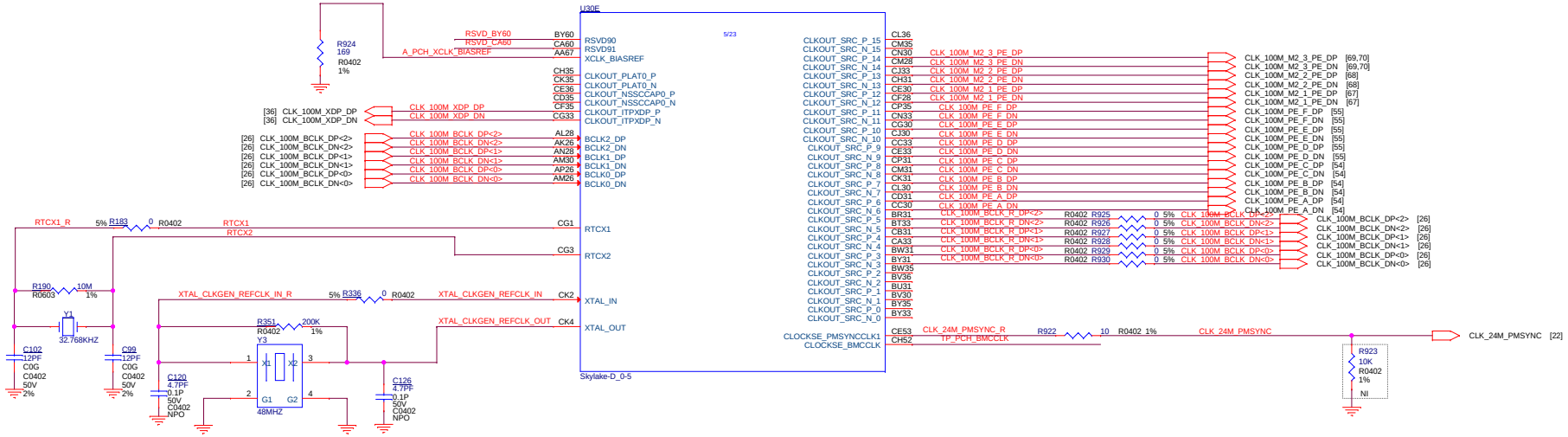

SKL-D CLK

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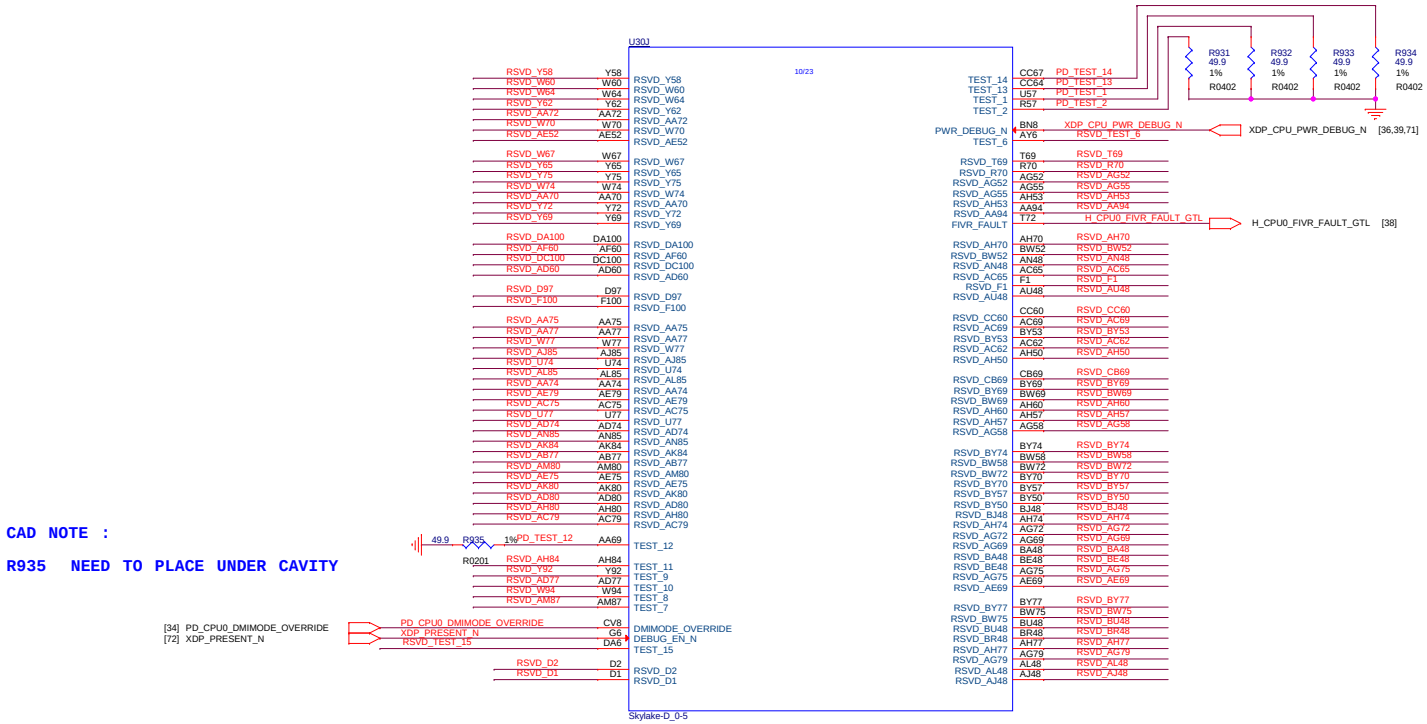

CAD NOTE :

R935 NEED TO PLACE UNDER CAVITY

SKL-D TEST,DDR MISC,SMBus

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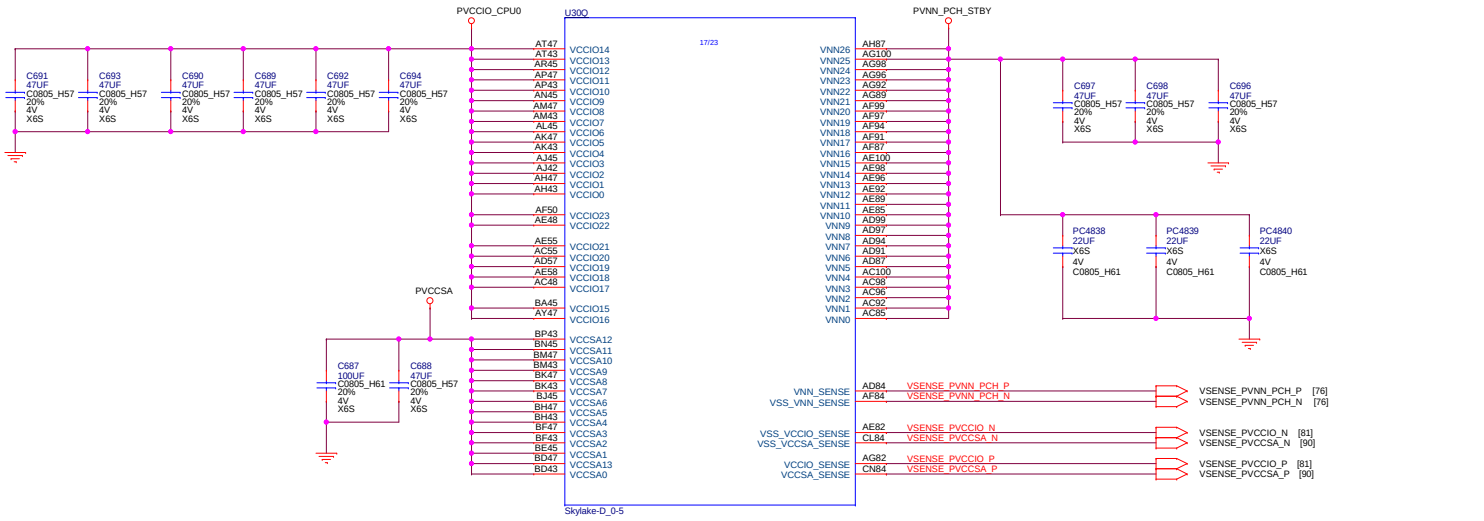

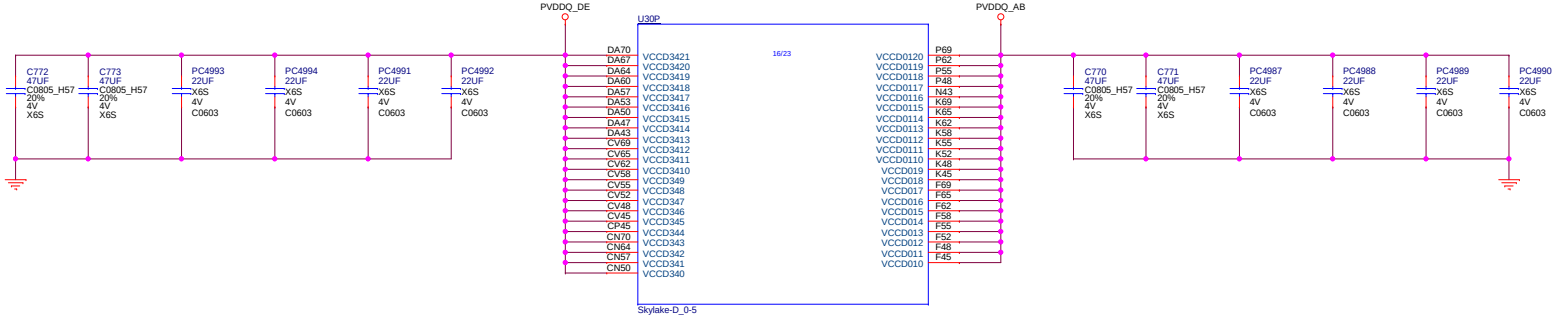

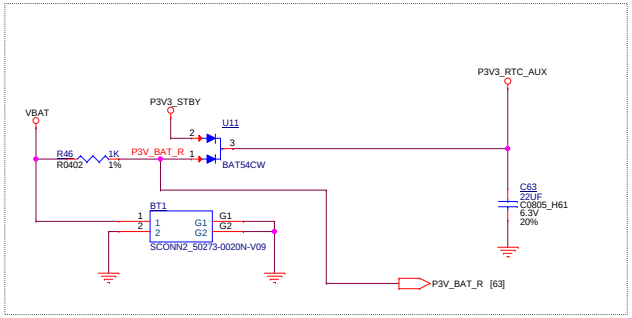

SKL-D POWER<1>

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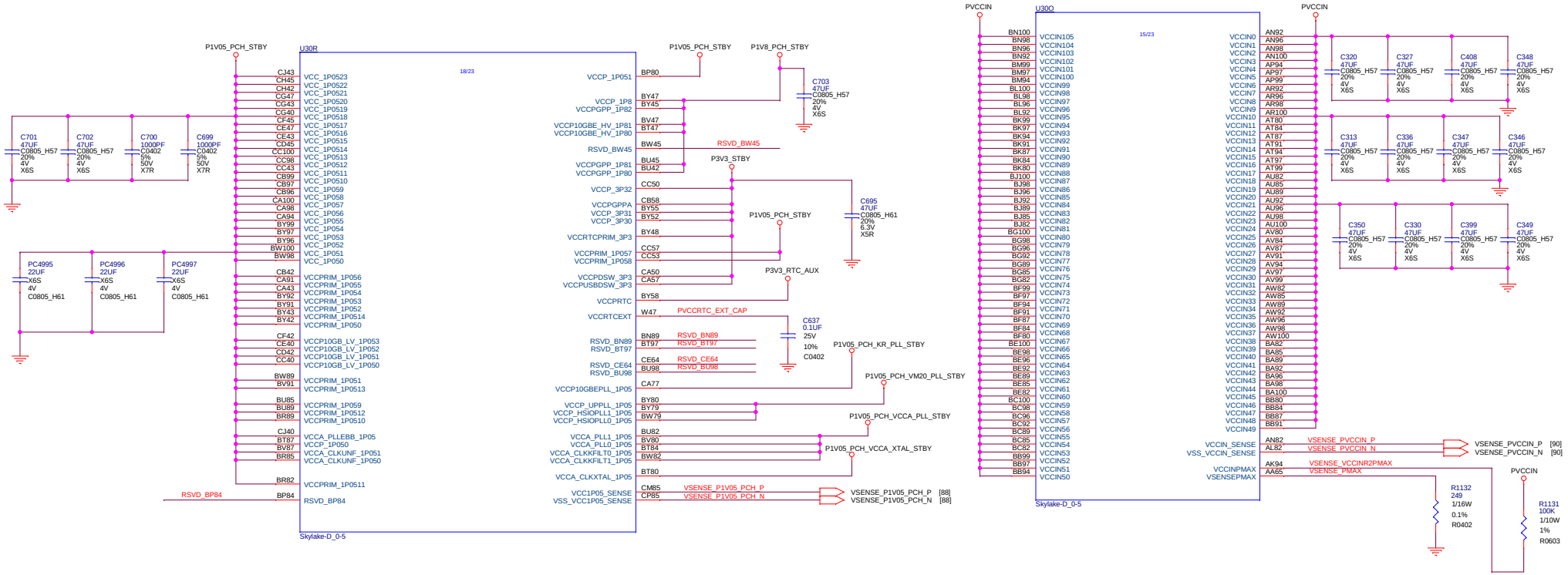
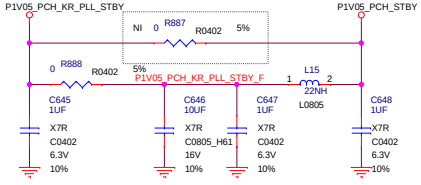
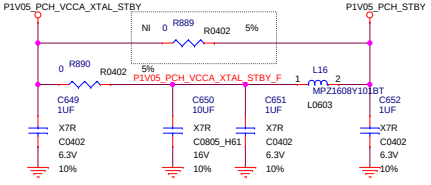
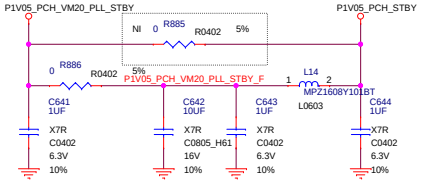
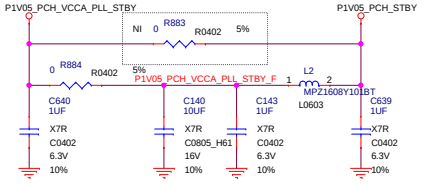
	Page Title: SKL-D POWER<1>		
Size: C	Date: Thursday, June 14, 2018	Sheet 28 of 99	





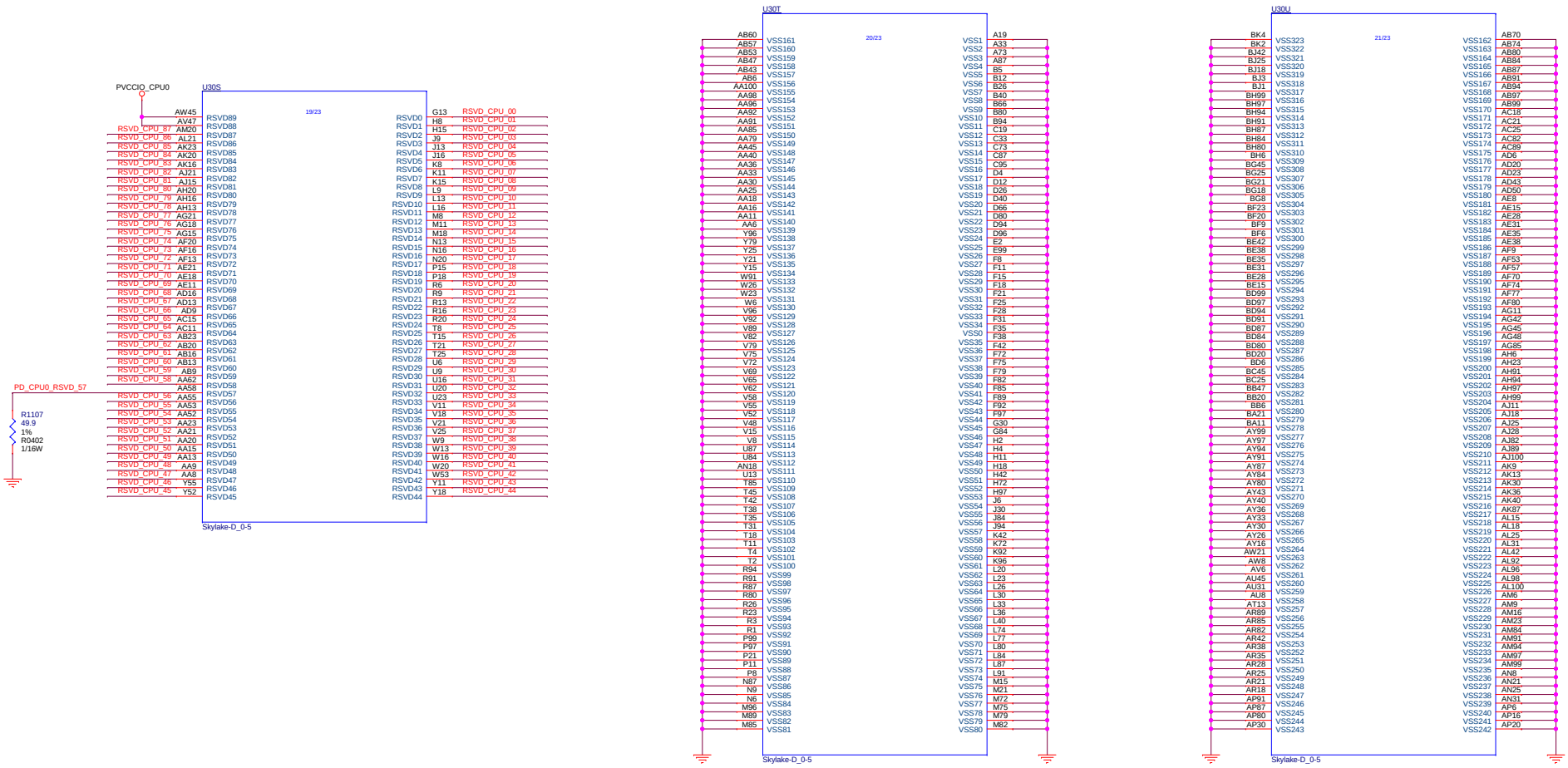






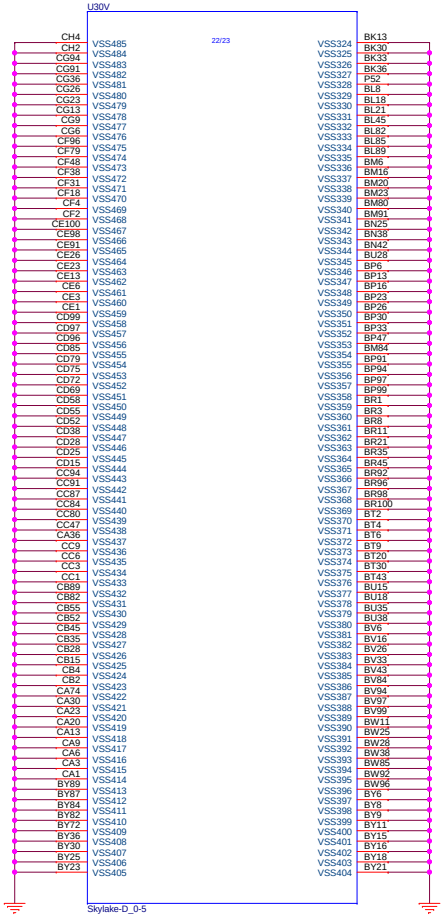
SKL-D POWER<2>

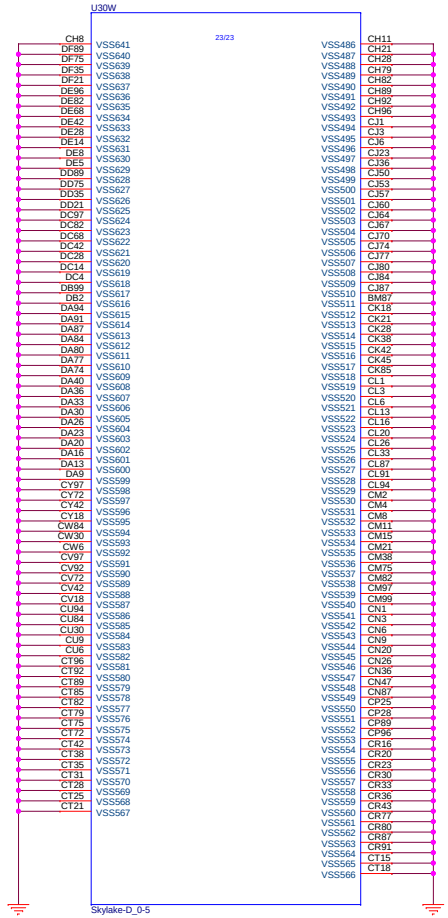
Project: Twin Lakes	Doc Number: <Doc>		Rev: V0.32
	Page Title: SKL-D POWER<2>		
Size: C	Date: Thursday, June 14, 2018	Sheet 29 of 99	

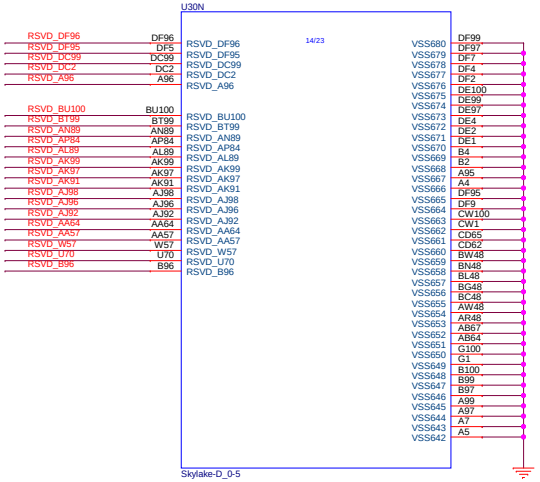


SKL-D GND<1>

Project: Twin Lakes		Doc Number: <Doc>	Rev: V0.32
		Page Title: SKL-D GND<1>	
Size: C	Date: Thursday, June 14, 2018	Sheet 30 of 99	







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Project: Twin Lakes	Doc Number: <Doc>		Rev: V0.32
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PVCCIO_CPU0

1% R2840 R0402 75 H_CPU0_AB_MEMHOT_GTL_N → H_CPU0_AB_MEMHOT_GTL_N [22,39]

1% R2841 R0402 75 H_CPU0_DE_MEMHOT_GTL_N → H_CPU0_DE_MEMHOT_GTL_N [22,39]

1% R2842 R0402 150 PU_CPU0_PM_FAST_WAKE_G_N → PU_CPU0_PM_FAST_WAKE_G_N [22]

DESIGN NOTE :

R2840, R2841, R2842 are placed close to SoC.

P3V3_STBY

R2843 R0402 10K PU_PCH_GPP_B_3 → PU_PCH_GPP_B_3 [25]

R2844 R0402 10K PU_PCH_GPP_B_4 → PU_PCH_GPP_B_4 [25]

R2845 R0402 10K PU_PCH_GPP_E_10 → PU_PCH_GPP_E_10 [24]

R2846 R0402 10K PU_PCH_GPP_E_11 → PU_PCH_GPP_E_11 [24]

R2848 R0402 10K PU_PCH_GPP_E_12 → PU_PCH_GPP_E_12 [24]

R2847 R0402 10K PU_PCH_GPP_F_15 → PU_PCH_GPP_F_15 [24]

R2849 R0402 10K PU_PCH_GPP_F_16 → PU_PCH_GPP_F_16 [24]

R2851 R0402 10K PU_PCH_GPP_F_17 → PU_PCH_GPP_F_17 [24]

R2850 R0402 10K PU_PCH_GPP_F_18 → PU_PCH_GPP_F_18 [24]

R2852 R0402 10K PU_FM_PCH_MGPIO_TEST0 → PU_FM_PCH_MGPIO_TEST0 [24]

R2854 R0402 10K PU_FM_PCH_MGPIO_TEST4 → PU_FM_PCH_MGPIO_TEST4 [24]

R2853 R0402 10K FM_CLKREQ_M2_SSD_N → FM_CLKREQ_M2_SSD_N [24,69]

R2855 R0402 10K FM_GBE_PCI_DISABLE_N → FM_GBE_PCI_DISABLE_N [24]

P3V3_STBY

R2867 R0402 10K IRQ_LPC_SERIRQ_ESPI_CS1_N → IRQ_LPC_SERIRQ_ESPI_CS1_N [25,60]

R2868 R0402 10K LPC_RCIN_N_ESPI_ALERT1_N → LPC_RCIN_N_ESPI_ALERT1_N [25]

R2869 R0402 10K PU_IRQ_LPC_PIRQA_N_ESPI_ALERT0_N → PU_IRQ_LPC_PIRQA_N_ESPI_ALERT0_N [25]

R2871 R0402 10K FM_LPC_CLKRUN_N → FM_LPC_CLKRUN_N [25,60]

R2872 R0402 10K PU_IRQ_PCH_SCI_WHEA_N → PU_IRQ_PCH_SCI_WHEA_N [25]

R2870 R0402 10K PU_FM_LPC_PME_N → PU_FM_LPC_PME_N [25]

R2911 R0402 10K PU_SUSACK_N → PU_SUSACK_N [25]

R2960 R0402 10K PU_FM_EUP_LOT6_N → PU_FM_EUP_LOT6_N [25]

R2873 R0402 10K RMII_PCH_ARB_IN → RMII_PCH_ARB_IN [23]

P3V3_STBY

R2858 R0402 10K RST_PCH_MIC_MUX_N → RST_PCH_MIC_MUX_N [25]

R2859 R0402 10K FM_PLD_PCH_DATA → FM_PLD_PCH_DATA [25,51]

R2861 R0402 10K FP_PWR_LED_N → FP_PWR_LED_N [25]

R2860 R0402 10K PU_PCH_VRALERT_N → PU_PCH_VRALERT_N [25]

R2863 R0402 10K FM_SOC_PRSNT_N → FM_SOC_PRSNT_N [23,52]

R2864 R0402 10K PU_SSATA_DEVSLP5 → PU_SSATA_DEVSLP5 [25]

R2866 R0402 10K PU_FM_BIOS_IMAGE_SWAP_N → PU_FM_BIOS_IMAGE_SWAP_N [24]

R2910 R0402 10K PU_M2_SSD_DEV_SLP → PU_M2_SSD_DEV_SLP [25]

NI

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CPU SIDE BAND: HW STRAPS

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		Page Title: CPU SIDE BAND: HW STRAPS	
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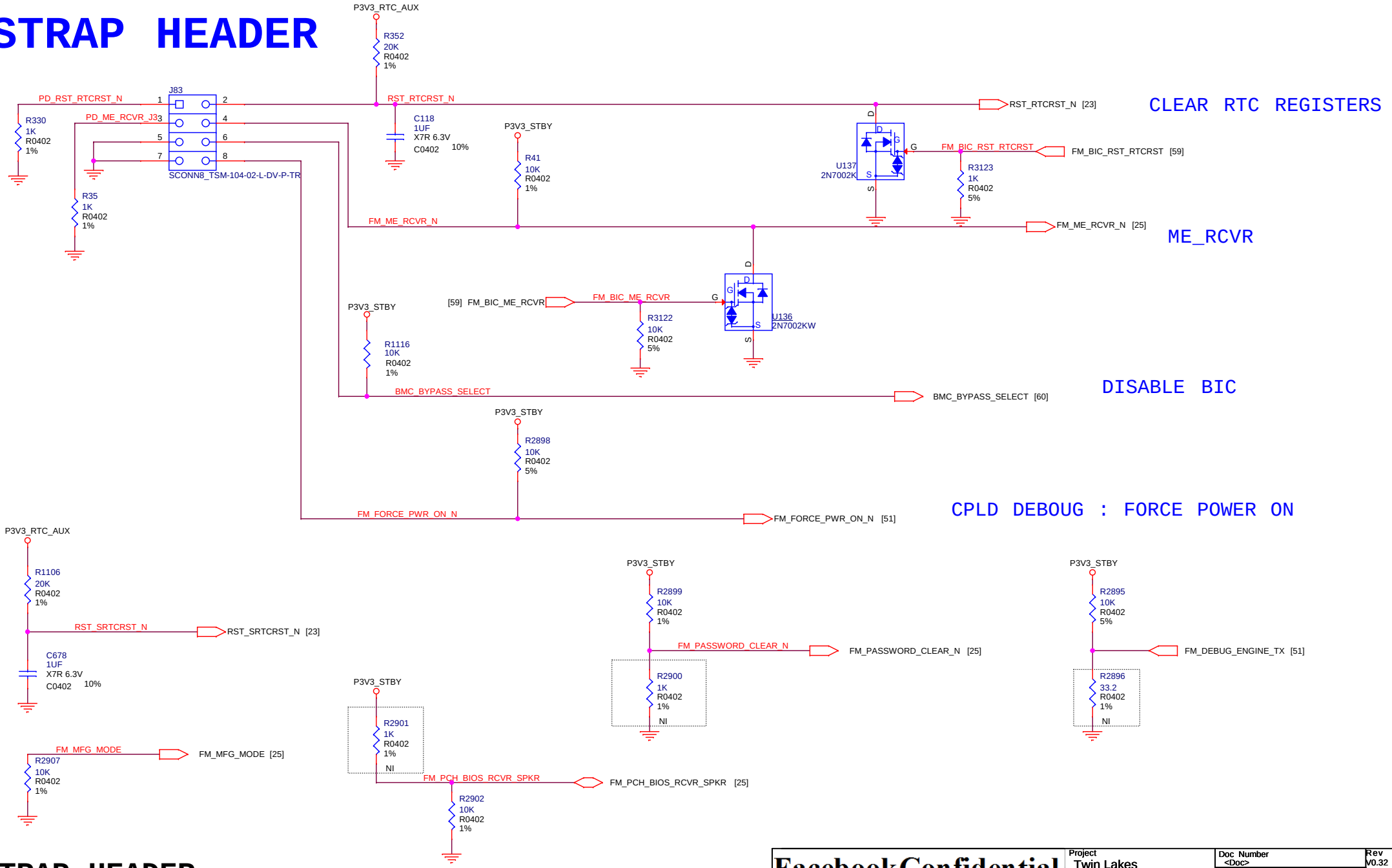
STRAP HEADER



STRAP HEADER

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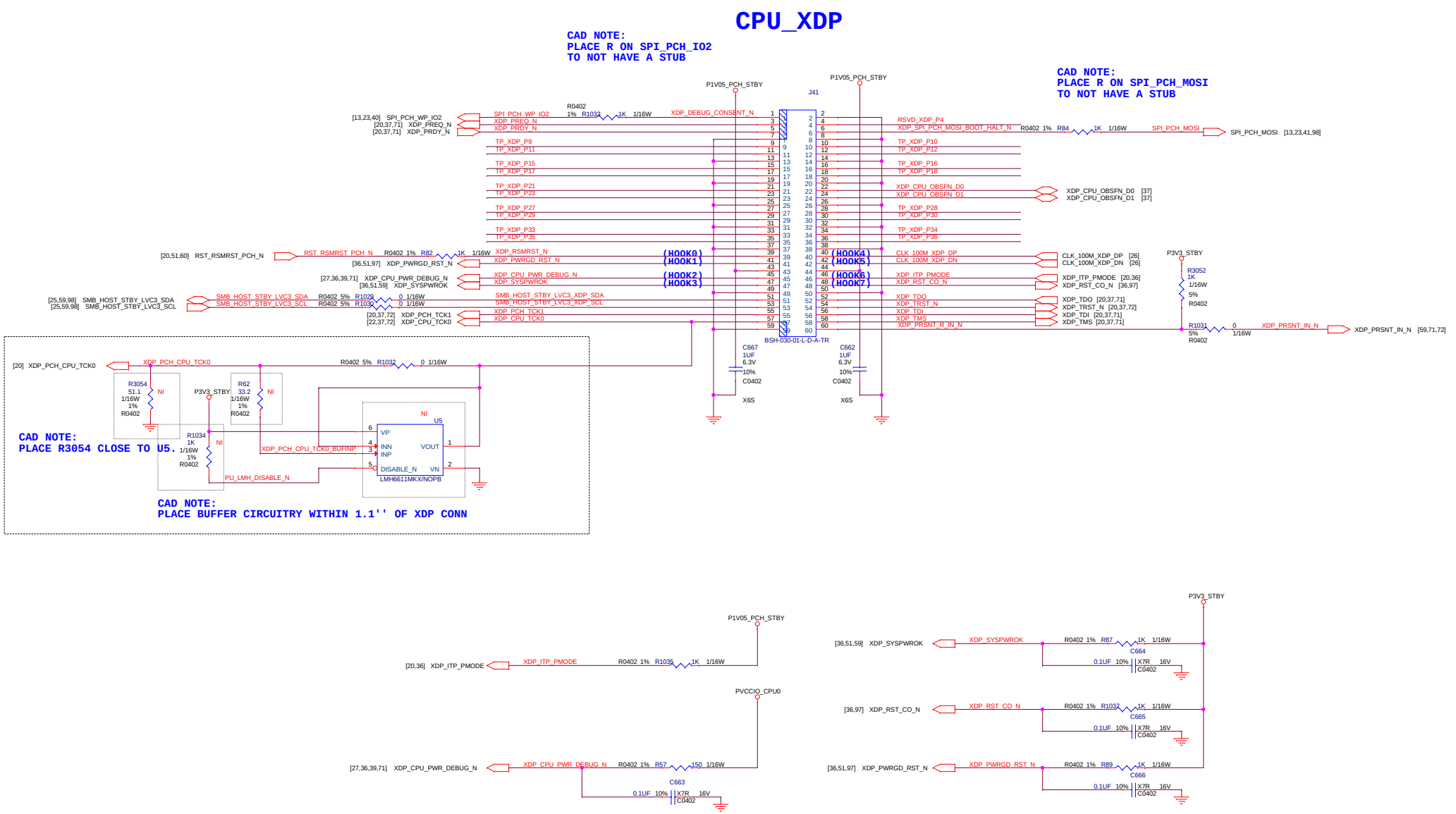
CPU_XDP



MERGED XDP 1 OF 2

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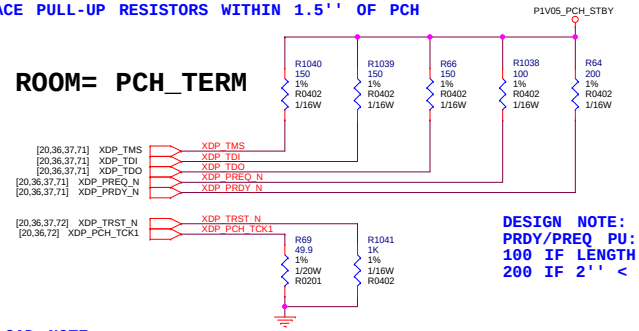
PCH XDP TERMINATIONS

CAD NOTE:
PLACE PULL-UP RESISTORS WITHIN 1.5'' OF PCH

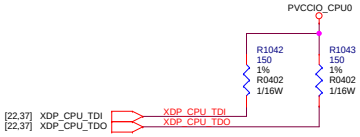


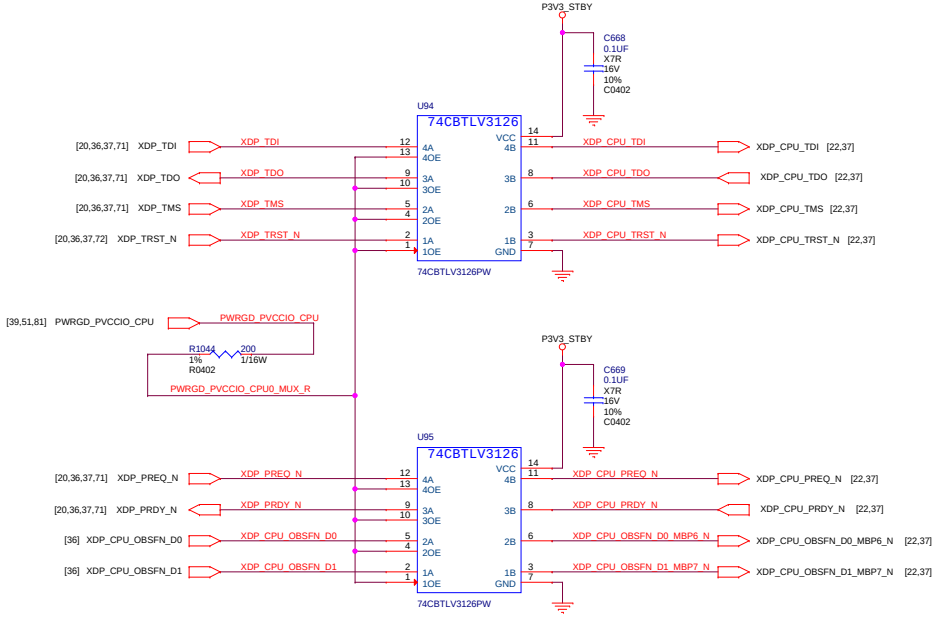
DESIGN NOTE:
PRDY/PREQ PU:
100 IF LENGTH < 24''
200 IF 2'' < LENGTH < 48''

CAD NOTE:
PLACE PULL-DOWN RESISTORS WITHIN 1.1'' OF PCH

CPU0 XDP TERMINATIONS

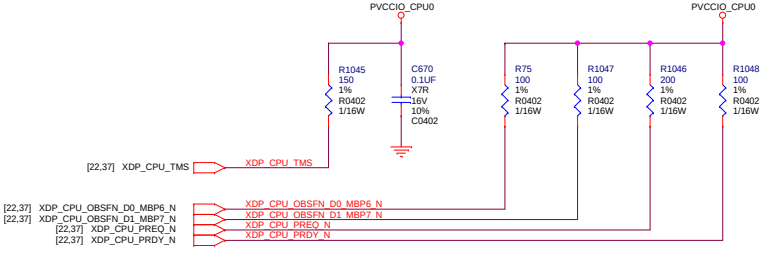
CAD NOTE:
PLACE PULL-UP RESISTORS WITHIN 1.5'' OF CPU0

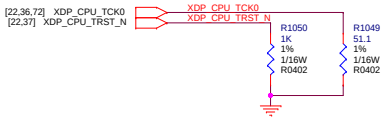




CAD NOTE:
PLACE BUFFER CIRCUITRY WITHIN 1.1'' OF XDP CONN

CAD NOTE:
PLACE PULL-UP RESISTORS WITHIN 1.5'' OF CPU(Receiver side)





DESIGN NOTE:
PRDY/PREQ PU:
100 IF LENGTH < 24''
200 IF 2'' < LENGTH < 48''

CAD NOTE:
PLACE PULL-DOWN RESISTORS WITHIN 1.1'' OF CPU (Receiver side)

MERGED XDP 2 OF 2

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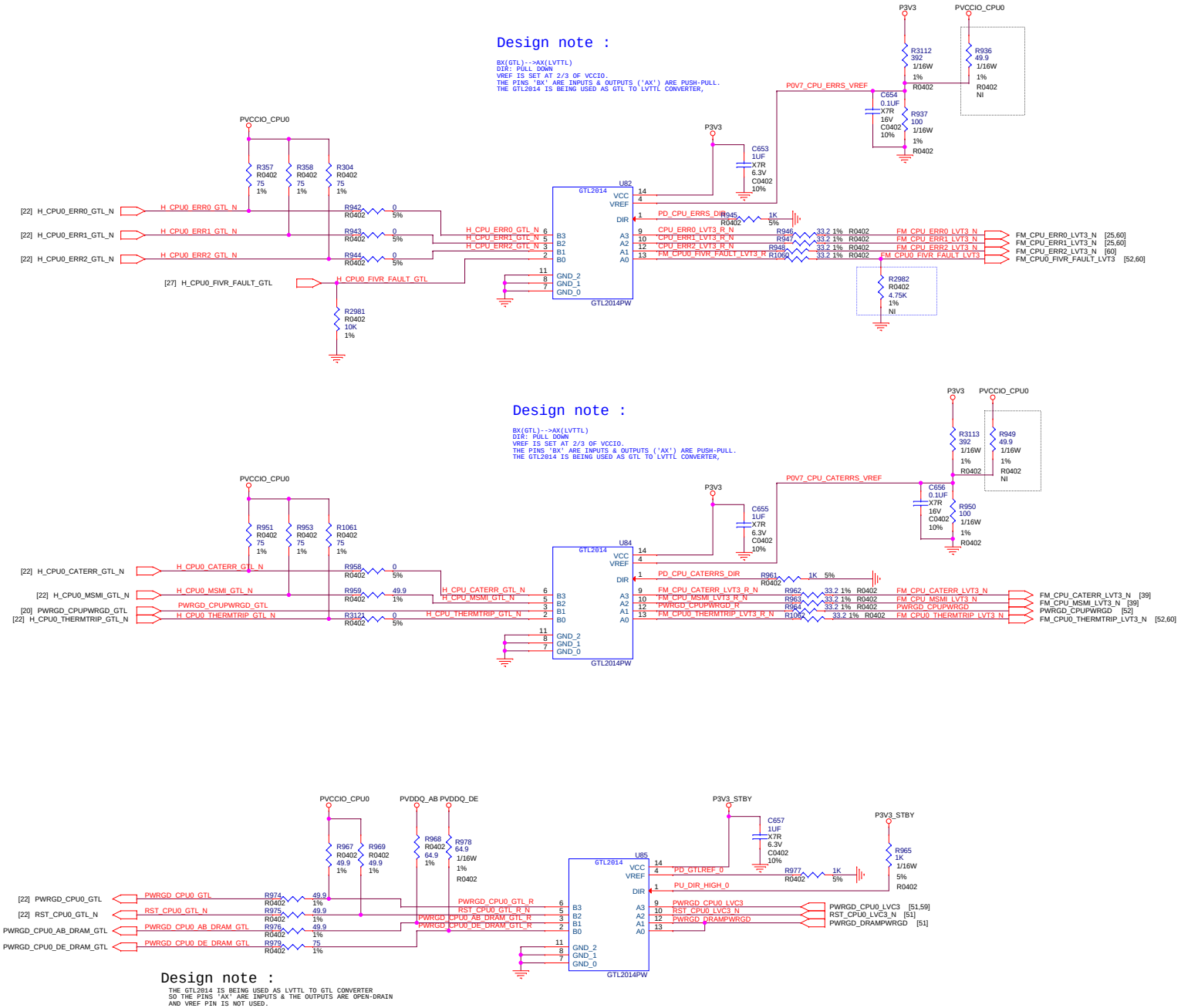
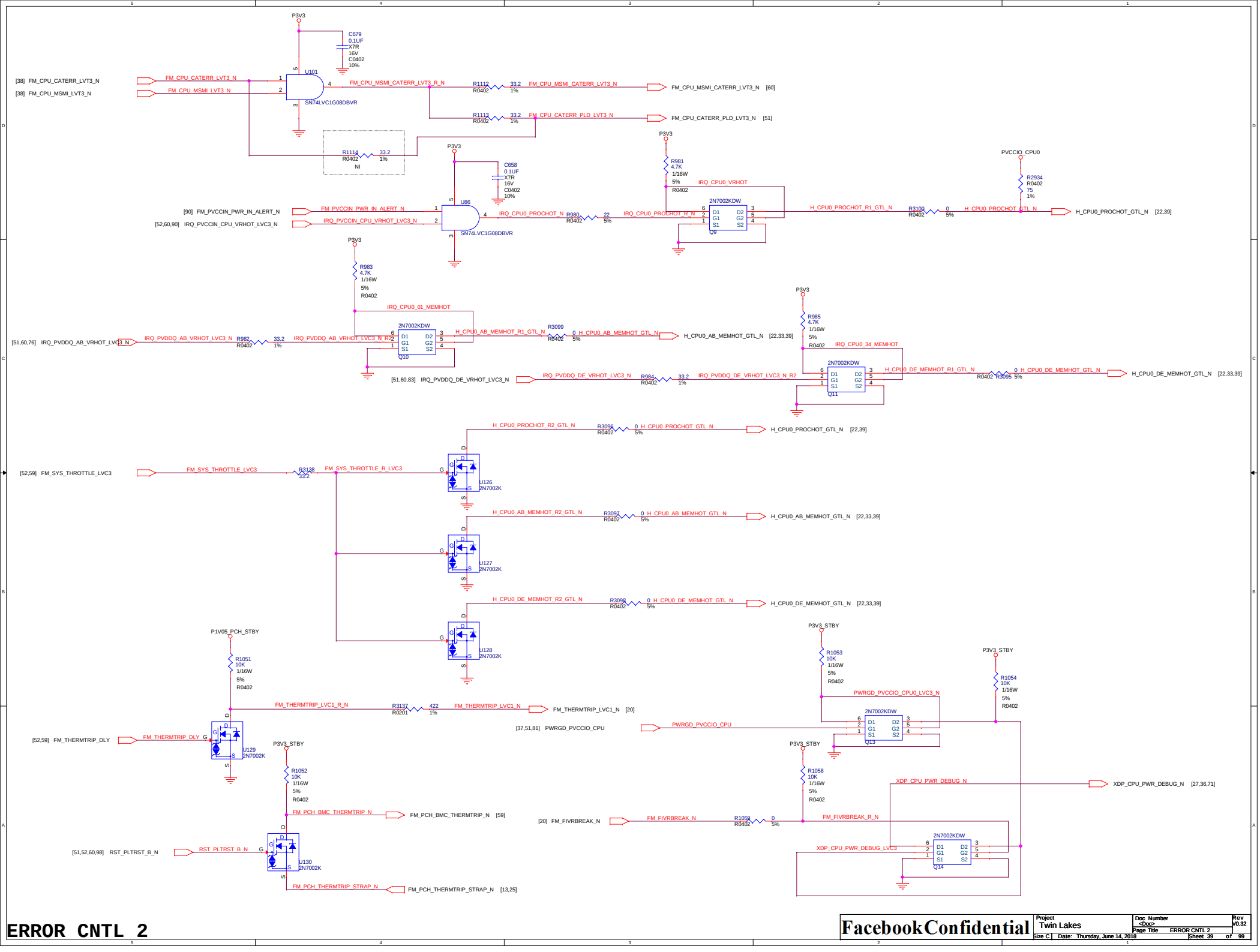

Design note :
BX(GTL)-->AX(LVTTL)
DIR: PULL DOWN
VREF IS SET AT 2/3 OF VCCIO.
THE PINS 'BX' ARE INPUTS & OUTPUTS ('AX') ARE PUSH-PULL.
THE GTL2014 IS BEING USED AS GTL TO LVTTL CONVERTER,
P3V3
PVCCIO_CPU0
P0V7_CPU_ERRS_VREF
U82
GTL2014
GTL2014PW
PD_CPU_ERRS_DIR
H_CPU0_ERR0_GTL_N
H_CPU0_ERR1_GTL_N
H_CPU0_ERR2_GTL_N
H_CPU0_FIVR_FAULT_GTL
FM_CPU_ERR0_LVT3_N
FM_CPU_ERR1_LVT3_N
FM_CPU_ERR2_LVT3_N
FM_CPU0_FIVR_FAULT_LVT3
Design note :
BX(GTL)-->AX(LVTTL)
DIR: PULL DOWN
VREF IS SET AT 2/3 OF VCCIO.
THE PINS 'BX' ARE INPUTS & OUTPUTS ('AX') ARE PUSH-PULL.
THE GTL2014 IS BEING USED AS GTL TO LVTTL CONVERTER,
P0V7_CPU_CATERRS_VREF
U84
PD_CPU_CATERRS_DIR
H_CPU0_CATERR_GTL_N
H_CPU0_MSMI_GTL_N
PWRGD_CPUPWRGD_GTL
H_CPU0_THERMTRIP_GTL_N
FM_CPU_CATERR_LVT3_N
FM_CPU_MSMI_LVT3_N
PWRGD_CPUPWRGD
FM_CPU0_THERMTRIP_LVT3_N
PVDDQ_AB
PVDDQ_DE
P3V3_STBY
U85
PD_GTLREF_0
PU_DIR_HIGH_0
PWRGD_CPU0_GTL
RST_CPU0_GTL_N
PWRGD_CPU0_AB_DRAM_GTL
PWRGD_CPU0_DE_DRAM_GTL
PWRGD_CPU0_LVC3
RST_CPU0_LVC3_N
PWRGD_DRAMPWRGD
Design note :
THE GTL2014 IS BEING USED AS LVTTL TO GTL CONVERTER
SO THE PINS 'AX' ARE INPUTS & THE OUTPUTS ARE OPEN-DRAIN
AND VREF PIN IS NOT USED.

ERROR CNTL 1



ERROR CNTL 2

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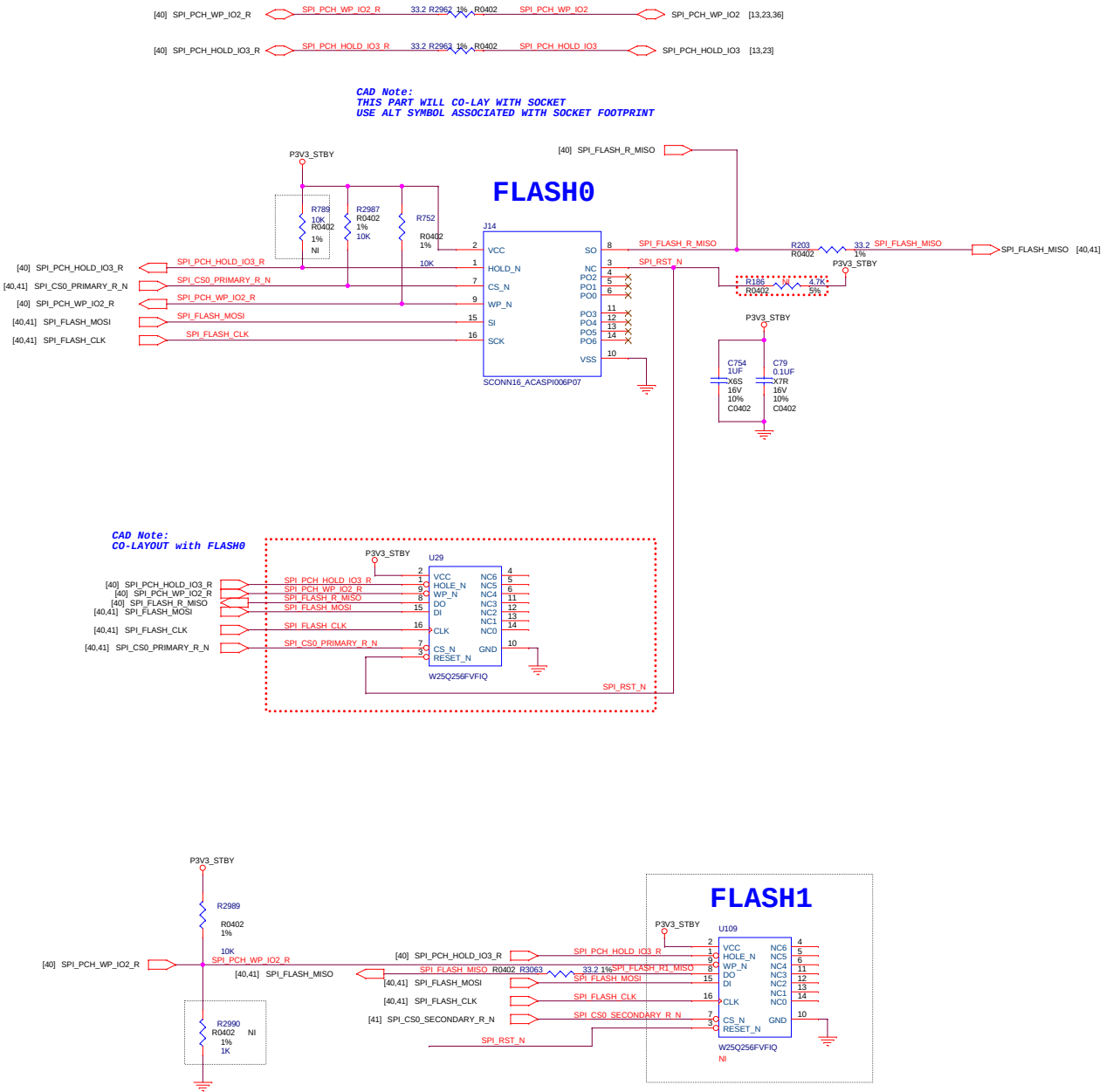

CPU SPI

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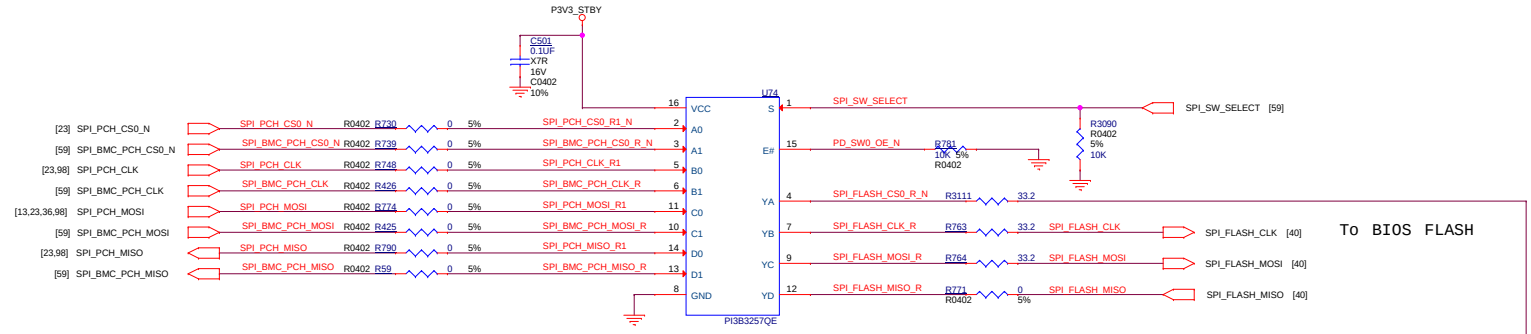
Truth Table

E	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

Channel 0 from SOC

Channel 1 from Bridge IC

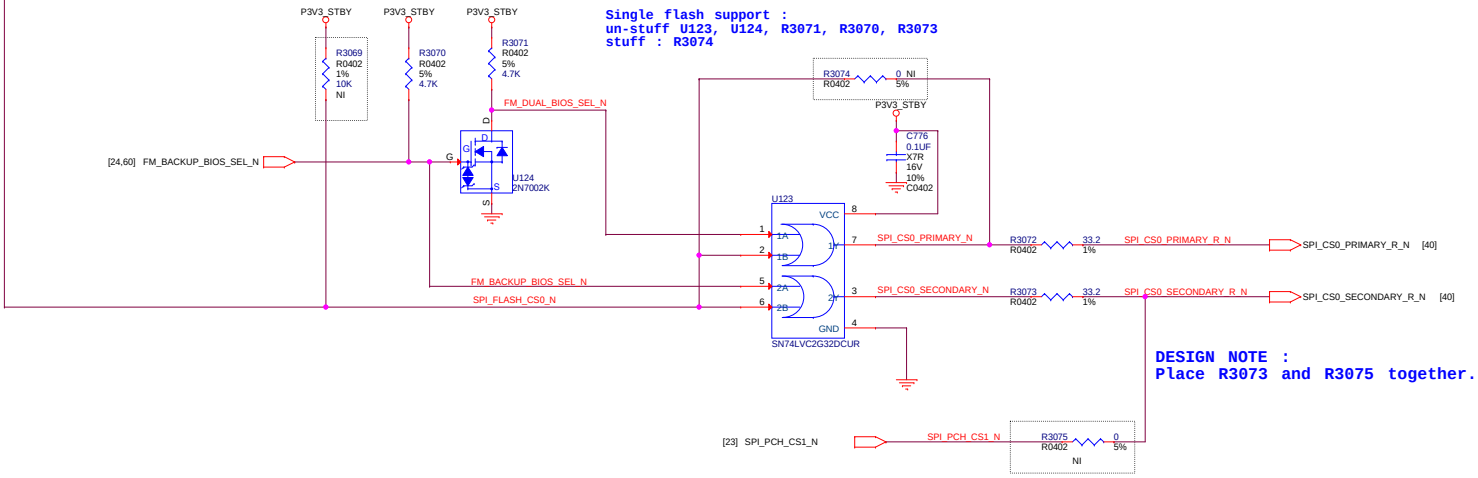


To BIOS FLASH

DESIGN NOTE :

Dual flash support :
Stuff : U123, U124, R3071, R3070, R3073
un-stuff : R3074

Single flash support :
un-stuff U123, U124, R3071, R3070, R3073
stuff : R3074



DESIGN NOTE :
Place R3073 and R3075 together.

SPI MUX

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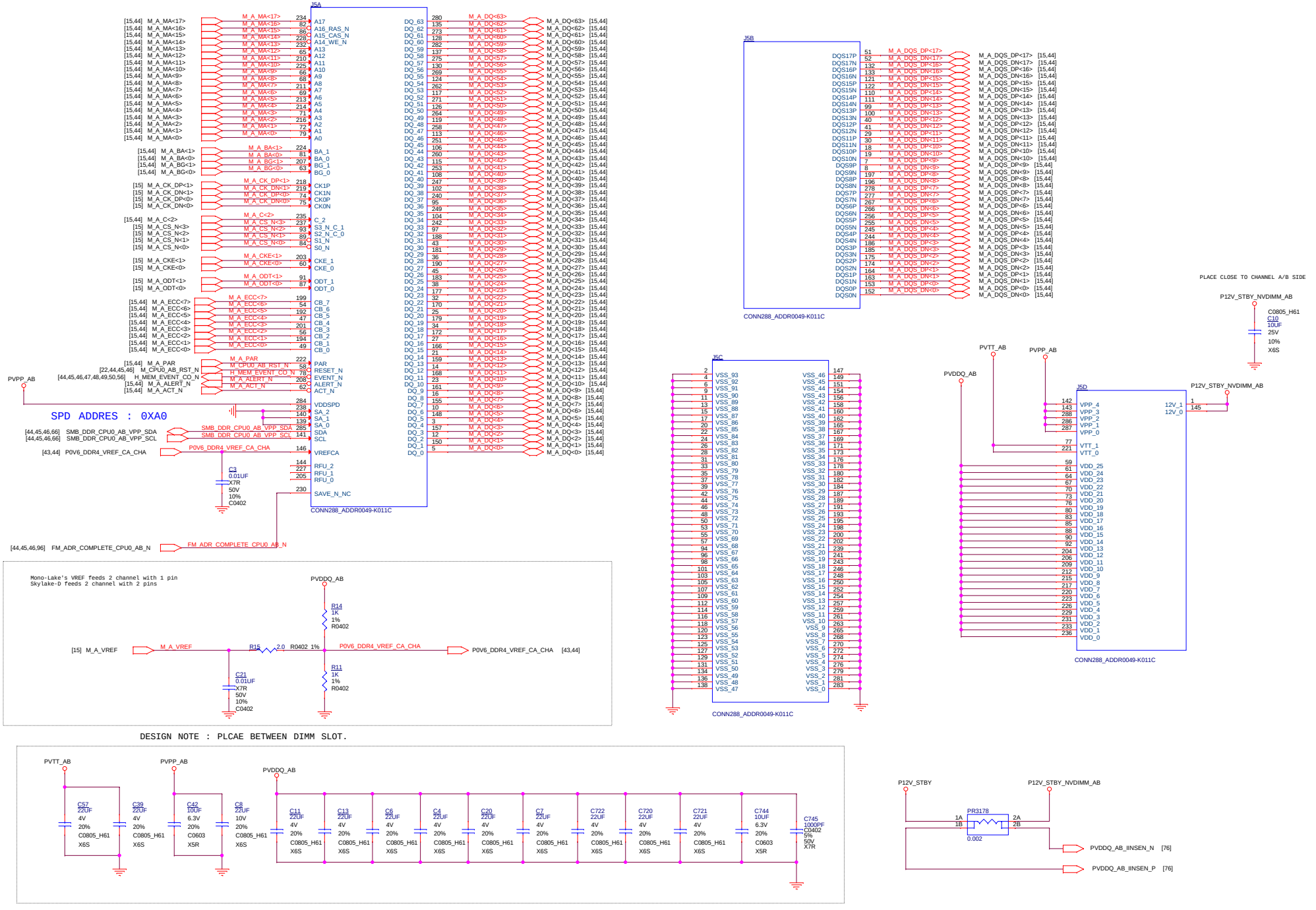
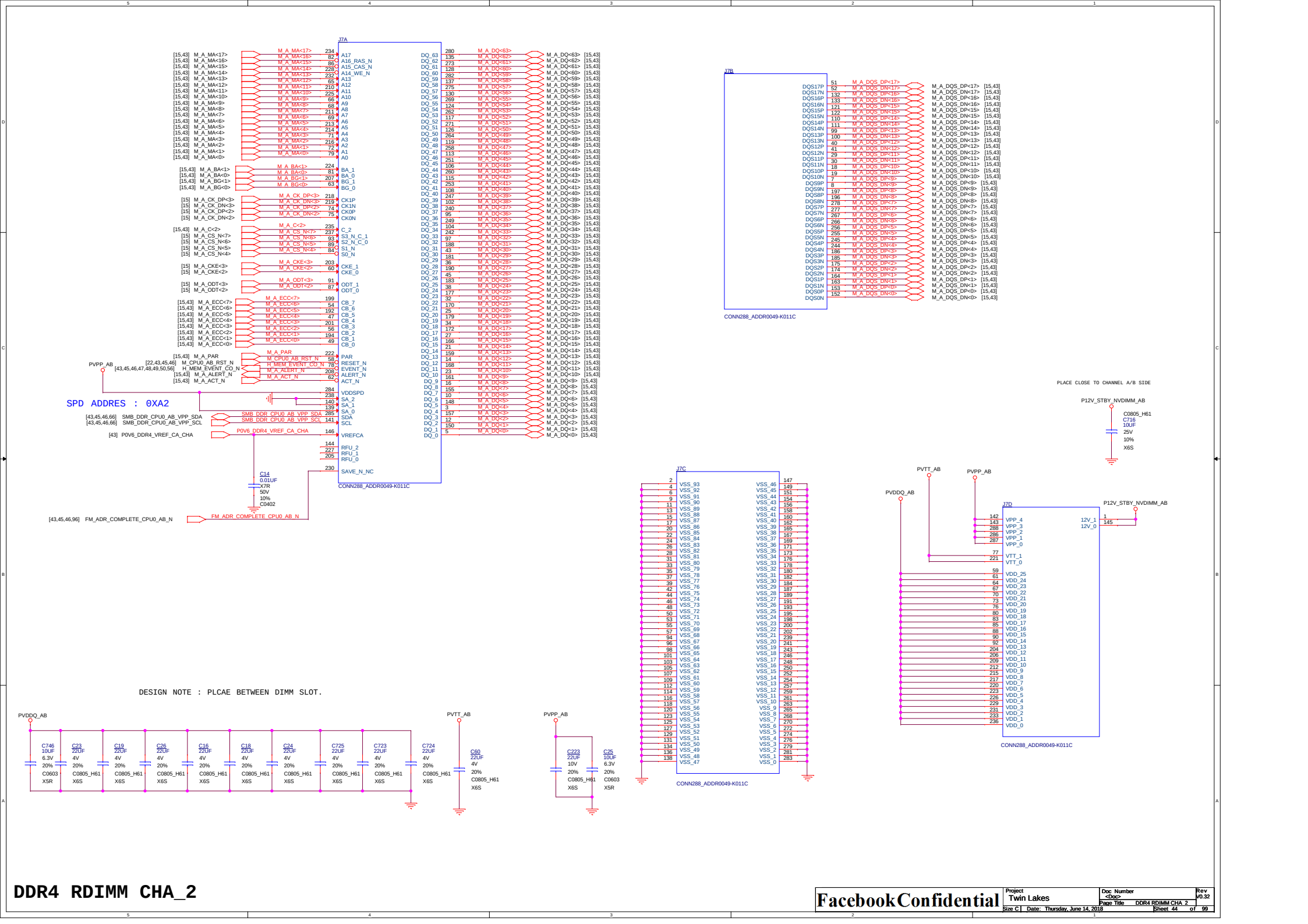


DDR4 RDIMM CHA_1



DDR4 RDIMM CHA_2

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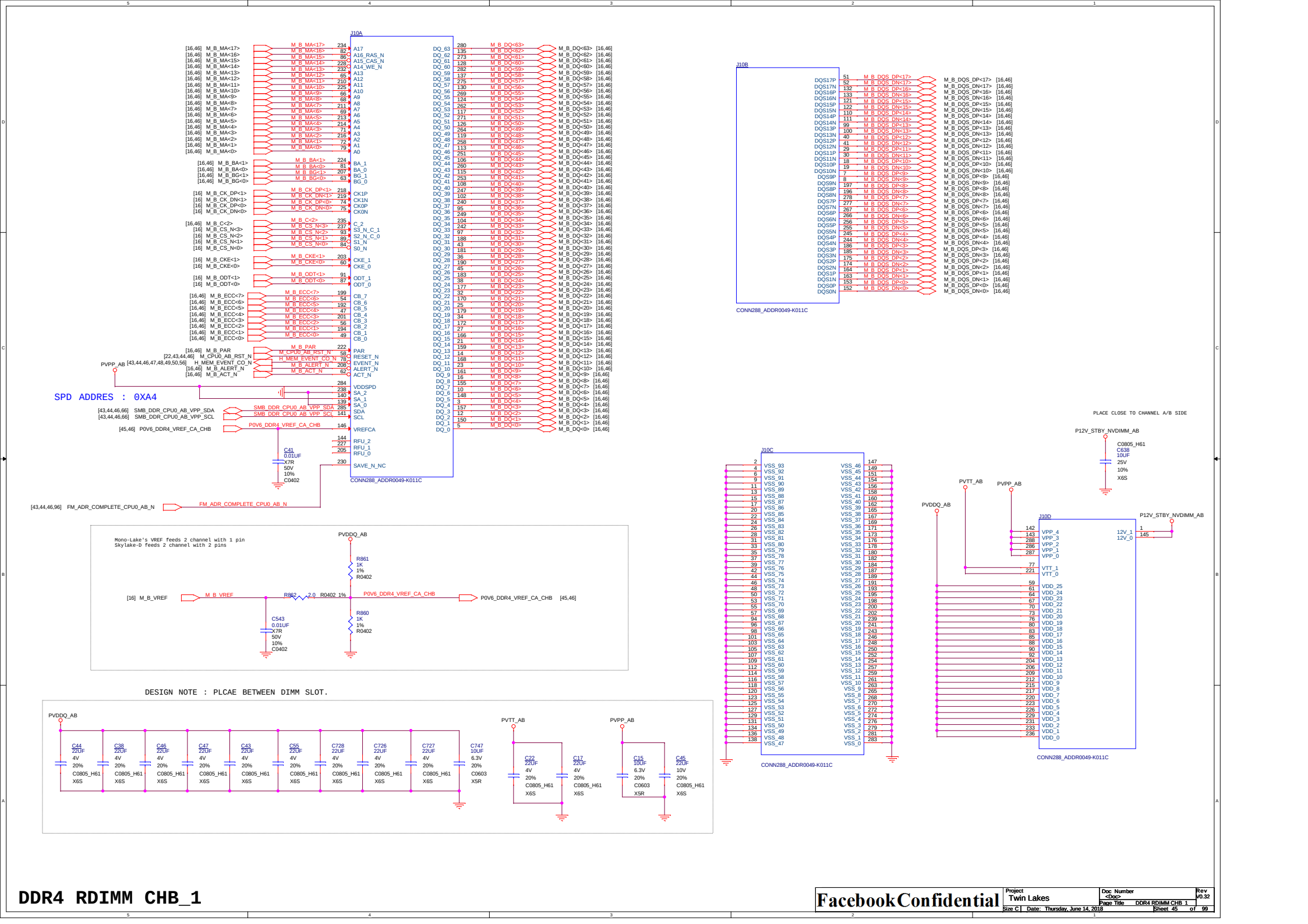

DDR4 RDIMM CHB_1

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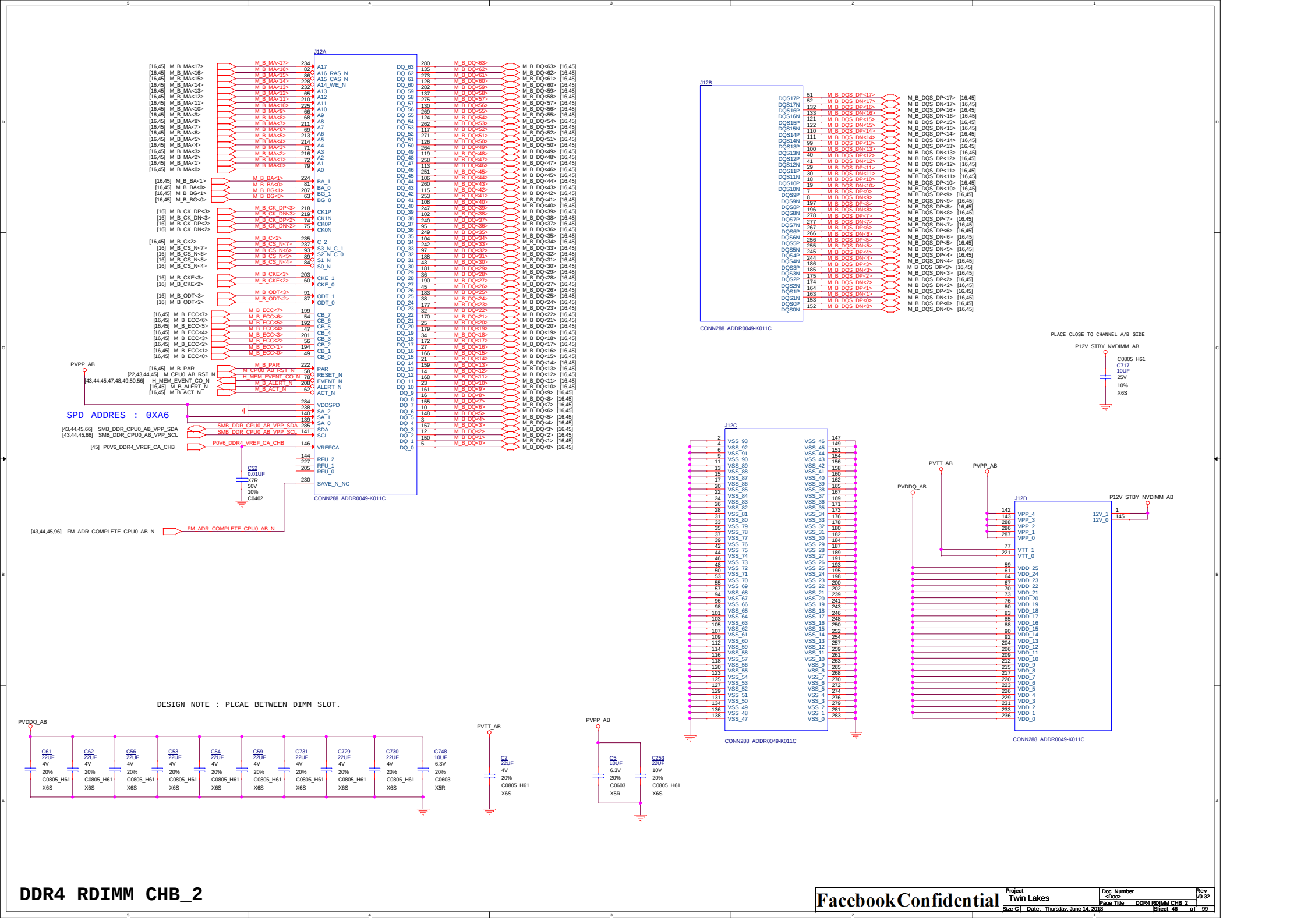

DDR4 RDIMM CHB_2

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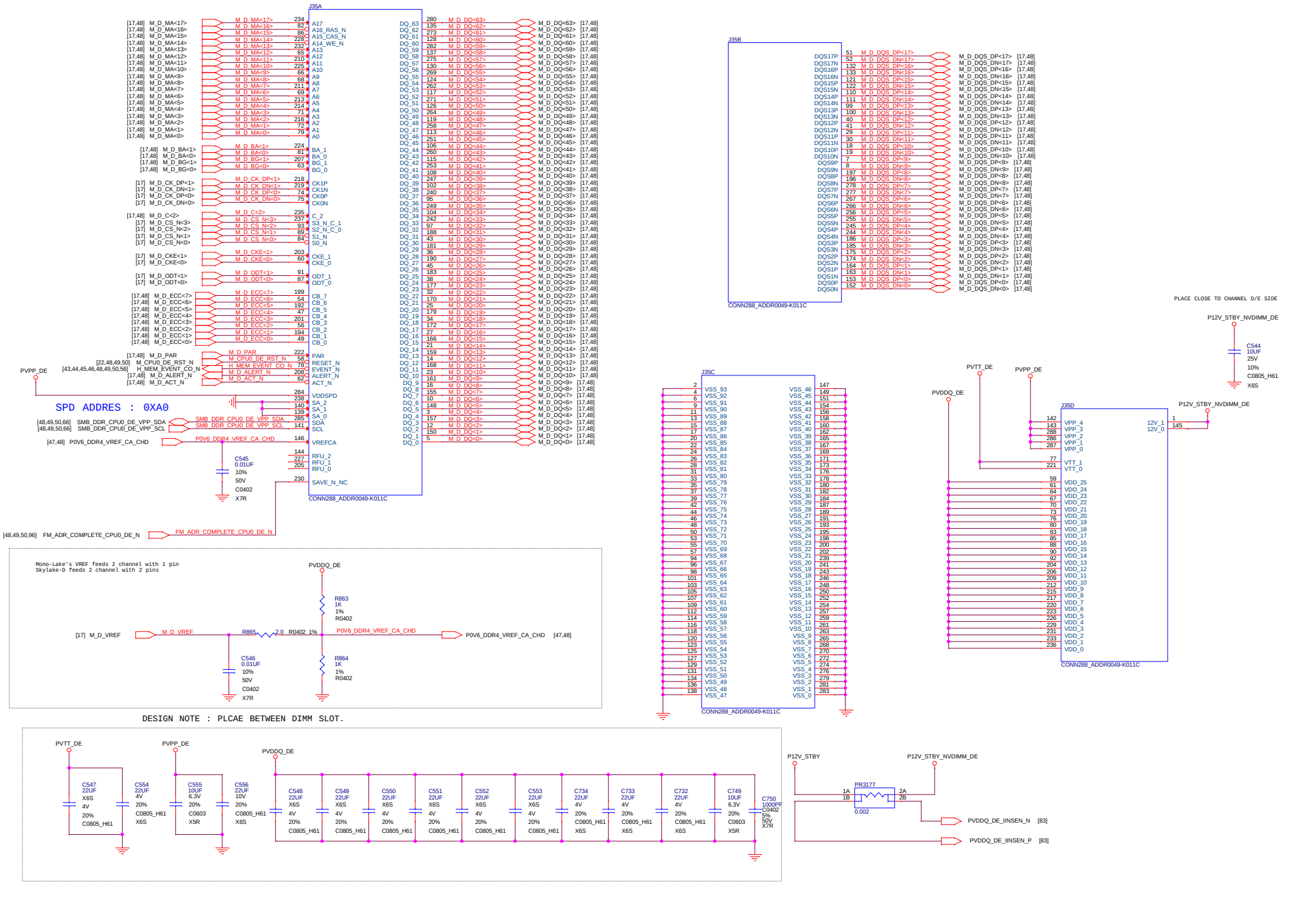

DDR4 RDIMM CHD_1

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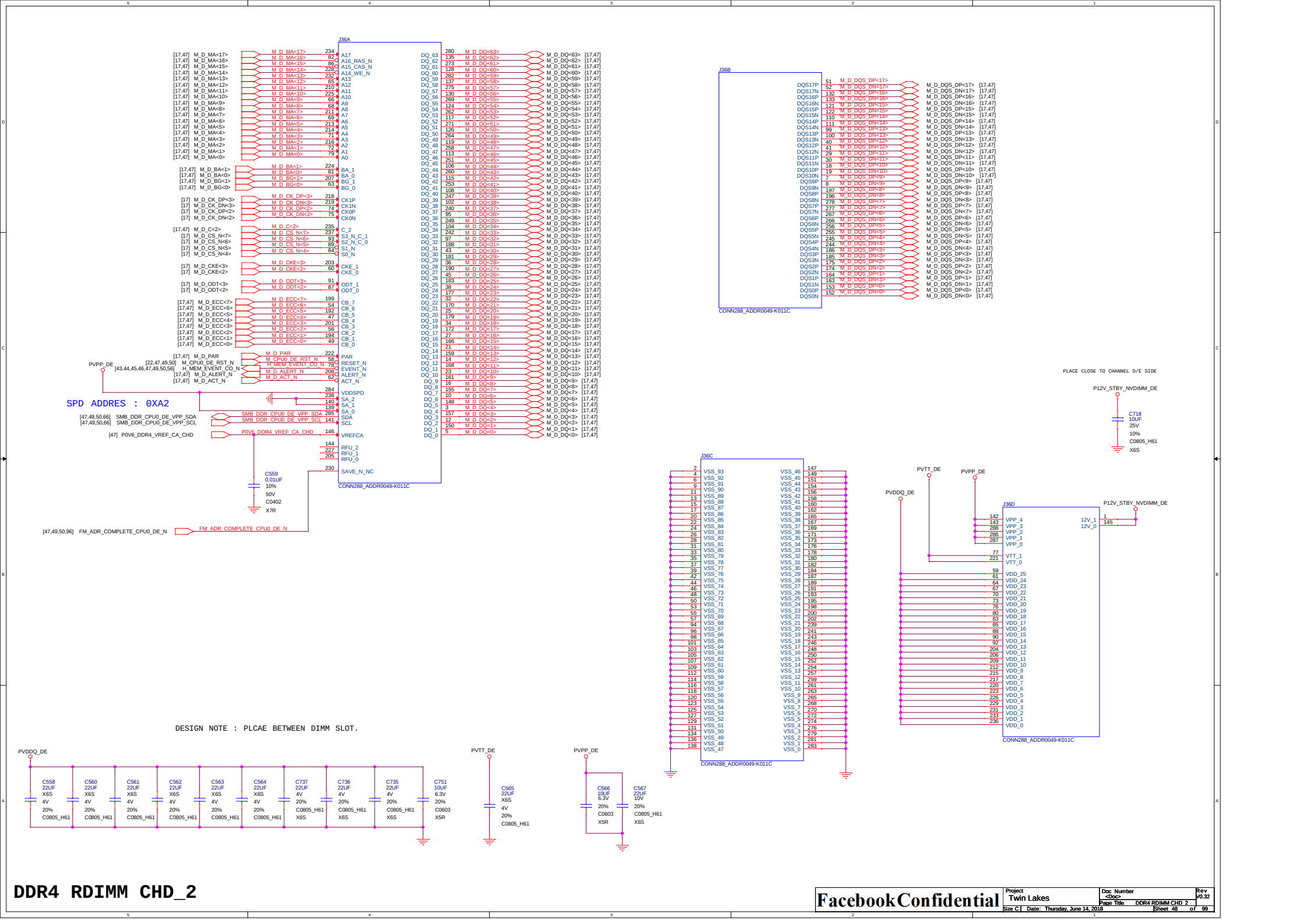

DDR4 RDIMM CHD_2

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		Page Title: DDR4 RDIMM CHD_2	
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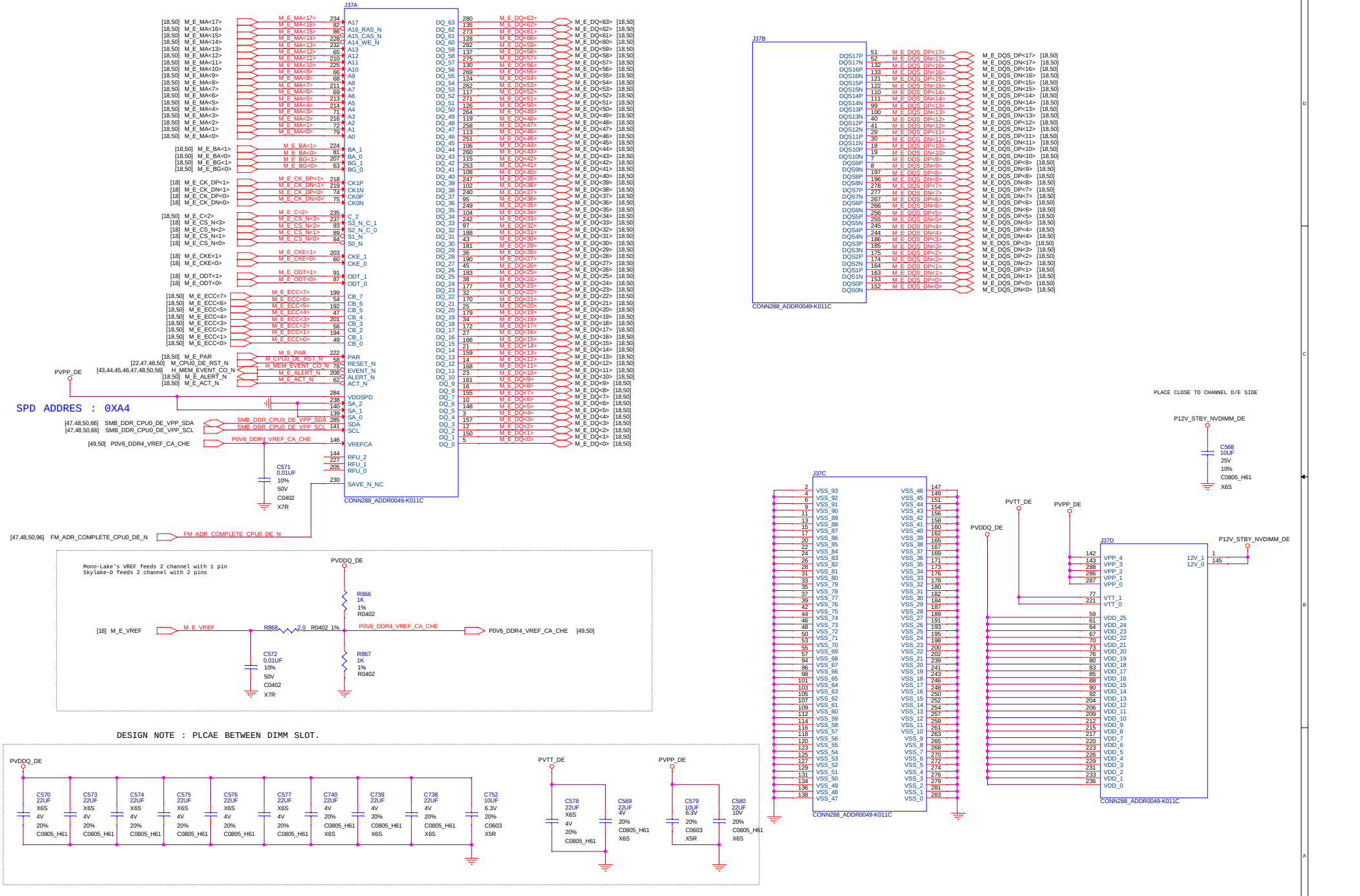

DDR4 RDIMM CHE_1

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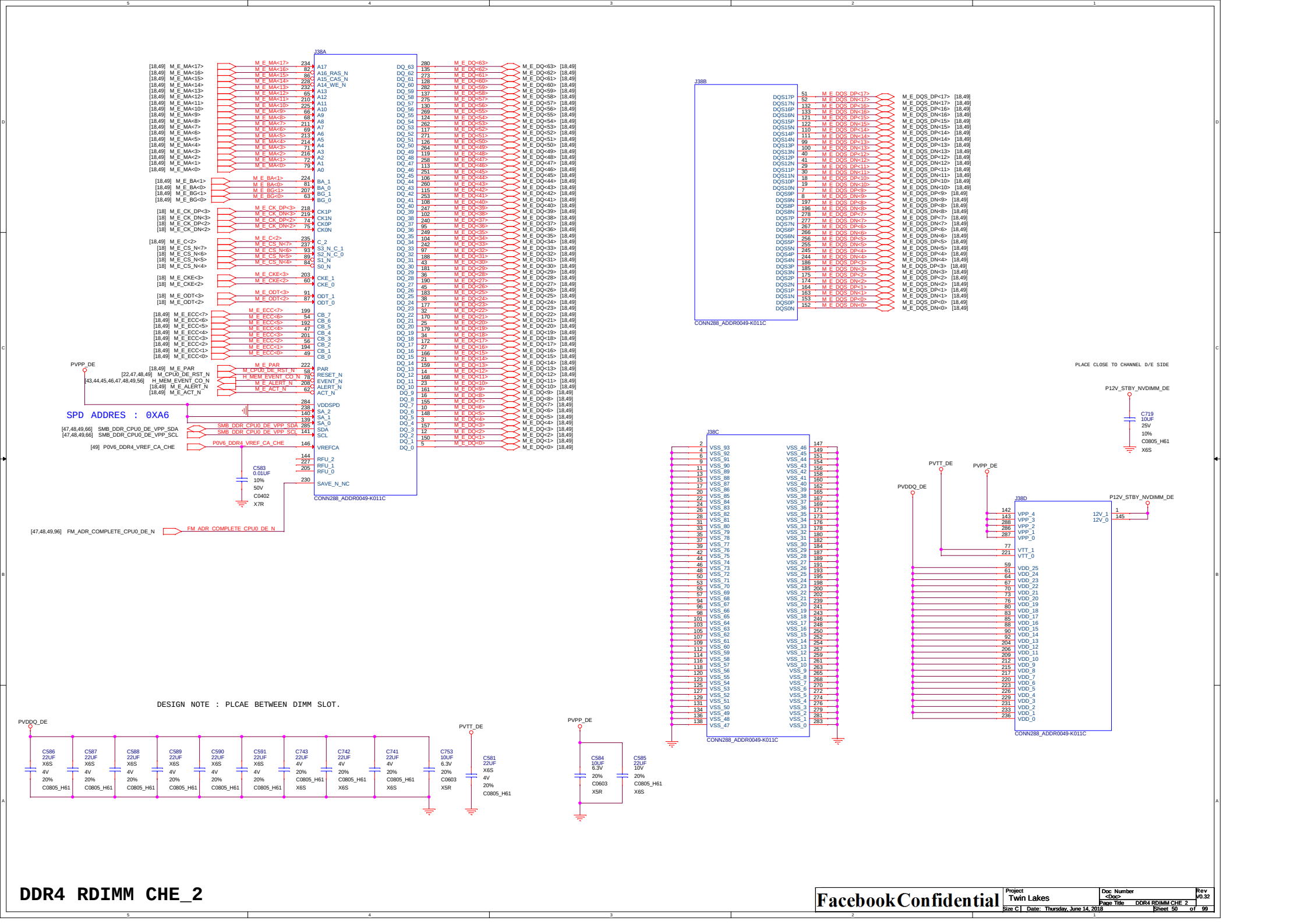

DDR4 RDIMM CHE_2

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	Page Title: DDR4 RDIMM CHE_2		
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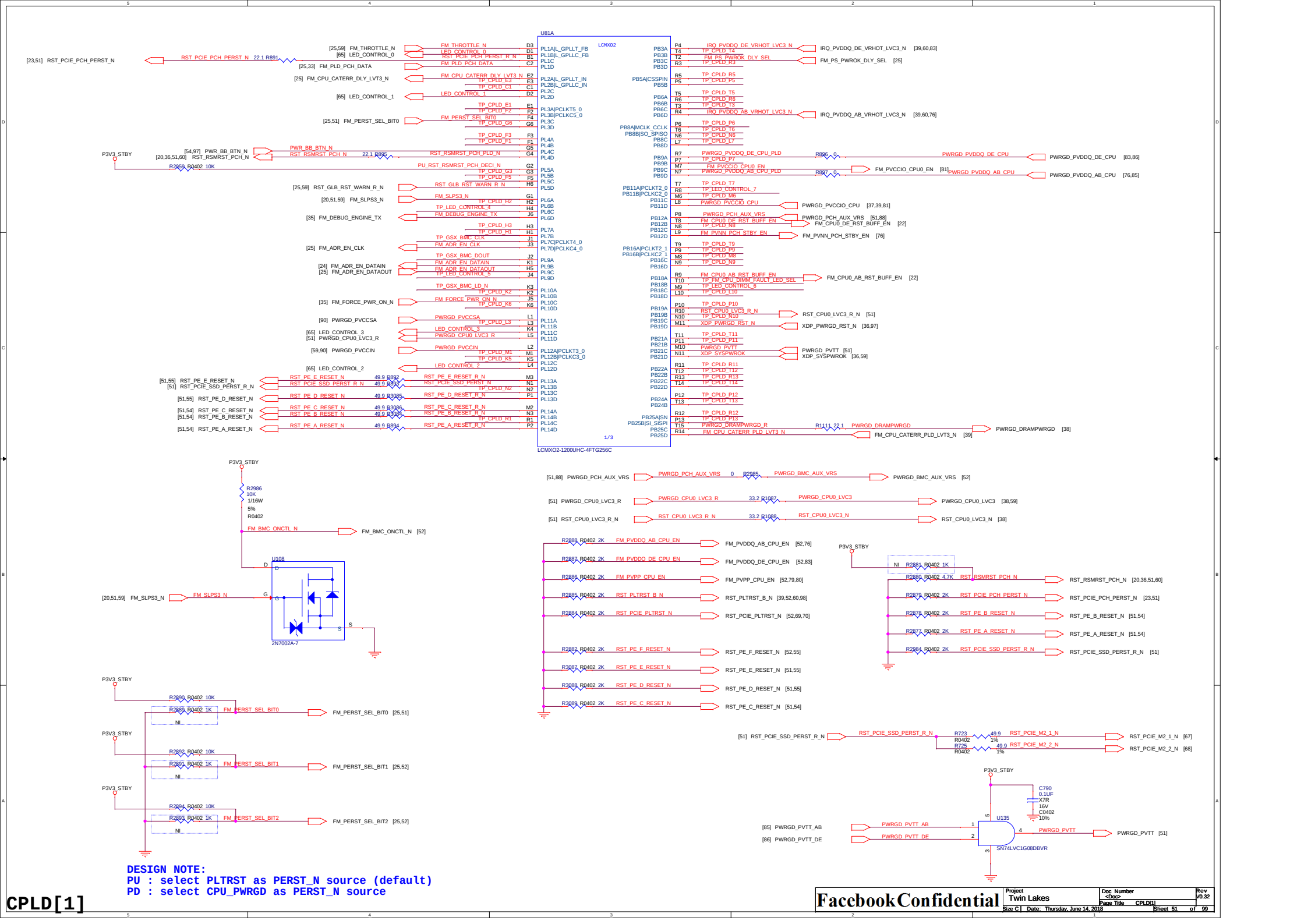
U81A
LCMX02
LCMXO2-1200UHC-4FTG256C
1/3
[23,51] RST_PCIE_PCH_PERST_N
RST_PCIE_PCH_PERST_N 22.1 R891
[25,59] FM_THROTTLE_N
[65] LED_CONTROL_0
[25,33] FM_PLD_PCH_DATA
[25] FM_CPU_CATERR_DLY_LVT3_N
[65] LED_CONTROL_1
[25,51] FM_PERST_SEL_BIT0
P3V3_STBY
[54,97] PWR_BB_BTN_N
[20,36,51,60] RST_RSMRST_PCH_N
R2959 R0402 10K
[25,59] RST_GLB_RST_WARN_R_N
[20,51,59] FM_SLPS3_N
[35] FM_DEBUG_ENGINE_TX
[25] FM_ADR_EN_CLK
[24] FM_ADR_EN_DATAIN
[25] FM_ADR_EN_DATAOUT
[35] FM_FORCE_PWR_ON_N
[90] PWRGD_PVCCSA
[65] LED_CONTROL_3
[51] PWRGD_CPU0_LVC3_R
[59,90] PWRGD_PVCCIN
[65] LED_CONTROL_2
[51,55] RST_PE_E_RESET_N
[51] RST_PCIE_SSD_PERST_R_N
[51,55] RST_PE_D_RESET_N
[51,54] RST_PE_C_RESET_N
[51,54] RST_PE_B_RESET_N
[51,54] RST_PE_A_RESET_N
[39,60,83]
[39,60,76]
[81]
[76,85]
[37,39,81]
[51,88]
[22]
[76]
[51]
[36,97]
[36,59]
[38]
[52,76]
[52,83]
[52,79,80]
[39,52,60,98]
[52,69,70]
[52,55]
[51,55]
[51,54]
[39]
[38,59]
[52]
[20,51,59] FM_SLPS3_N
2N7002A-7
[25,51] FM_PERST_SEL_BIT0
[25,52]
[25,51] FM_PERST_SEL_BIT1
[25,52]
[25,51] FM_PERST_SEL_BIT2
[25,52]
[51] RST_PCIE_SSD_PERST_R_N
[67]
[68]
[85] PWRGD_PVTT_AB
[86] PWRGD_PVTT_DE
[51]
SN74LVC1G08DBVR
DESIGN NOTE:
PU : select PLTRST as PERST_N source (default)
PD : select CPU_PWRGD as PERST_N source
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CPLD[2]

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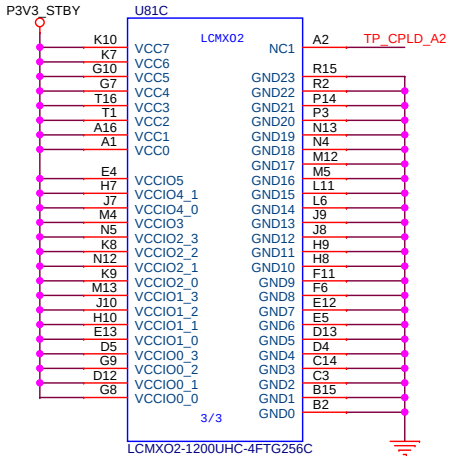

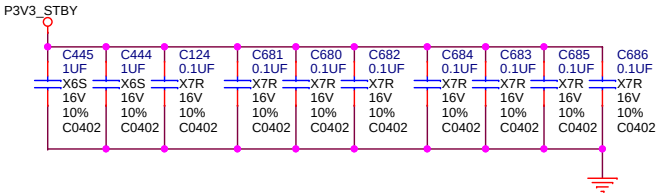

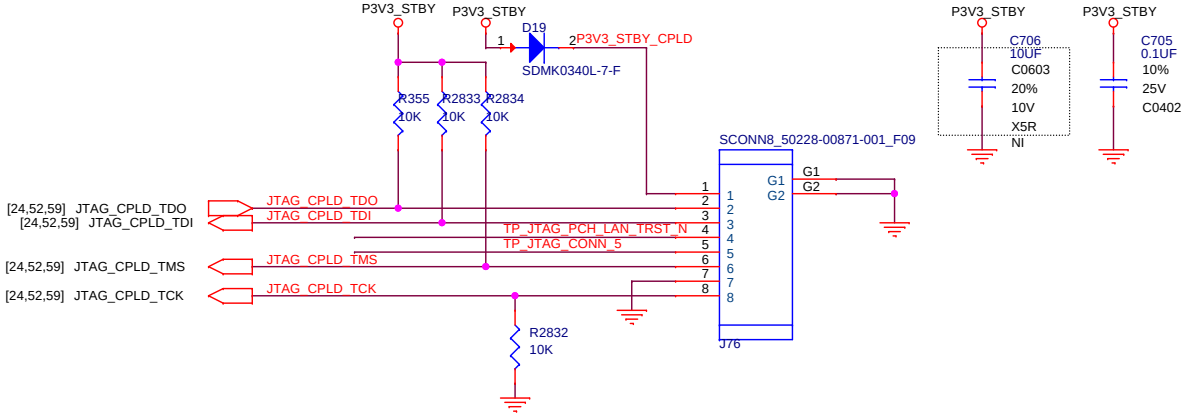

CPLD[3]

Project: Twin Lakes	Doc Number: <Doc>		Rev: V0.32
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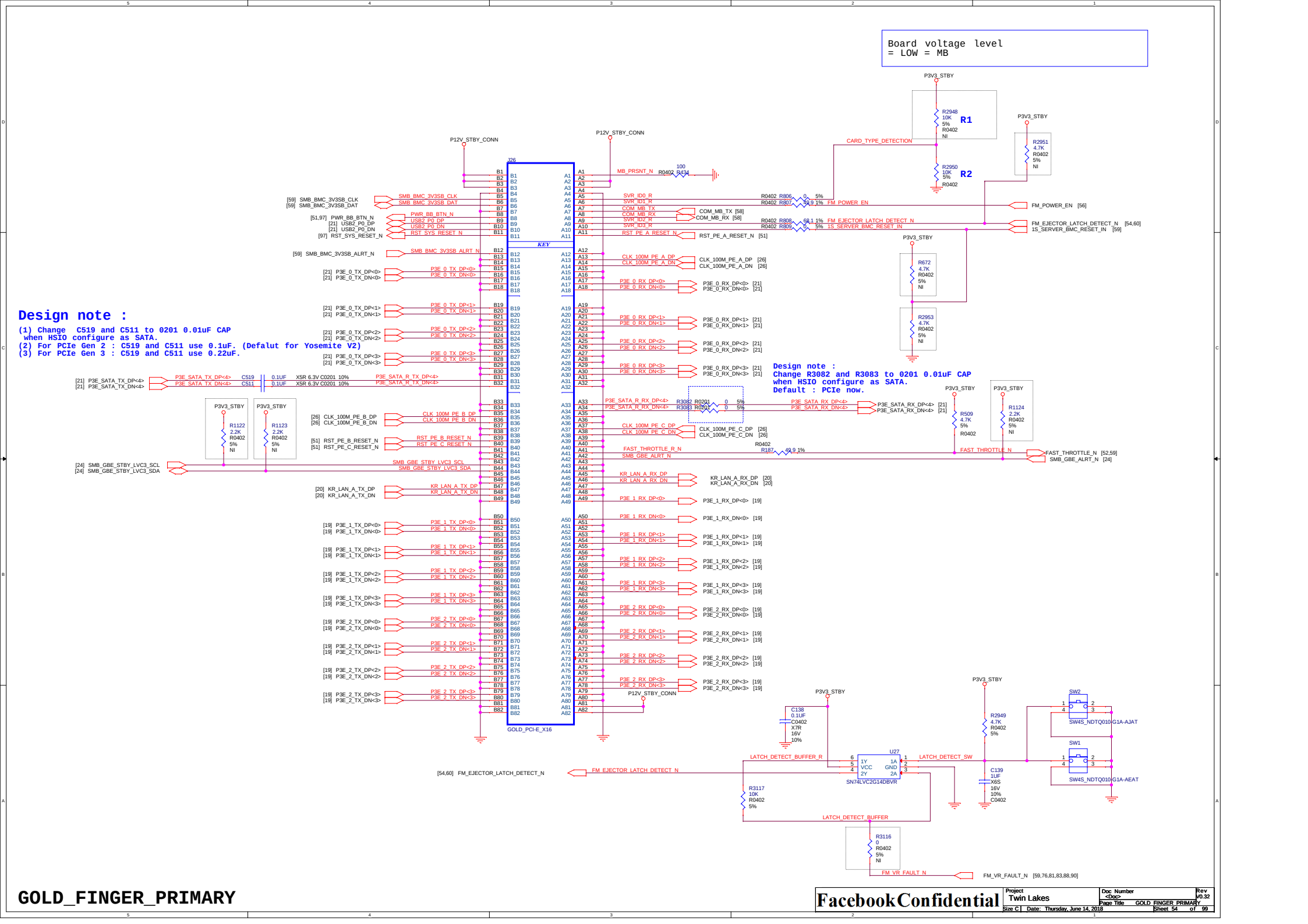
Board voltage level
= LOW = MB
Design note :
(1) Change C519 and C511 to 0201 0.01uF CAP
when HSIO configure as SATA.
(2) For PCIe Gen 2 : C519 and C511 use 0.1uF. (Defalut for Yosemite V2)
(3) For PCIe Gen 3 : C519 and C511 use 0.22uF.
Design note :
Change R3082 and R3083 to 0201 0.01uF CAP
when HSIO configure as SATA.
Default : PCIe now.
P12V_STBY_CONN
P3V3_STBY
J26
KEY
GOLD_PCI-E_X16
R1
R2
CARD_TYPE_DETECTION
FM_POWER_EN
FM_EJECTOR_LATCH_DETECT_N
1S_SERVER_BMC_RESET_IN
SMB_BMC_3V3SB_CLK
SMB_BMC_3V3SB_DAT
SMB_BMC_3V3SB_ALRT_N
PWR_BB_BTN_N
USB2_P0_DP
USB2_P0_DN
RST_SYS_RESET_N
MB_PRSNT_N
SVR_ID0_R
SVR_ID1_R
SVR_ID2_R
SVR_ID3_R
COM_MB_TX
COM_MB_RX
RST_PE_A_RESET_N
CLK_100M_PE_A_DP
CLK_100M_PE_A_DN
P3E_0_TX_DP<0>
P3E_0_TX_DN<0>
P3E_0_RX_DP<0>
P3E_0_RX_DN<0>
P3E_SATA_TX_DP<4>
P3E_SATA_TX_DN<4>
P3E_SATA_R_TX_DP<4>
P3E_SATA_R_TX_DN<4>
P3E_SATA_R_RX_DP<4>
P3E_SATA_R_RX_DN<4>
P3E_SATA_RX_DP<4>
P3E_SATA_RX_DN<4>
CLK_100M_PE_B_DP
CLK_100M_PE_B_DN
RST_PE_B_RESET_N
RST_PE_C_RESET_N
CLK_100M_PE_C_DP
CLK_100M_PE_C_DN
FAST_THROTTLE_R_N
SMB_GBE_ALRT_N
FAST_THROTTLE_N
SMB_GBE_STBY_LVC3_SCL
SMB_GBE_STBY_LVC3_SDA
KR_LAN_A_TX_DP
KR_LAN_A_TX_DN
KR_LAN_A_RX_DP
KR_LAN_A_RX_DN
P3E_1_TX_DP<0>
P3E_1_TX_DN<0>
P3E_1_RX_DP<0>
P3E_1_RX_DN<0>
P3E_2_TX_DP<0>
P3E_2_TX_DN<0>
P3E_2_RX_DP<0>
P3E_2_RX_DN<0>
FM_EJECTOR_LATCH_DETECT_N
LATCH_DETECT_BUFFER_R
LATCH_DETECT_SW
LATCH_DETECT_BUFFER
SN74LVC2G14DBVR
SW4S_NDTQ010-G1A-AJAT
SW4S_NDTQ010-G1A-AEAT
FM_VR_FAULT_N
Design note :
(1) Change C519 and C511 to 0201 0.01uF CAP
when HSIO configure as SATA.
(2) For PCIe Gen 2 : C519 and C511 use 0.1uF. (Defalut for Yosemite V2)
(3) For PCIe Gen 3 : C519 and C511 use 0.22uF.
GOLD_FINGER_PRIMARY
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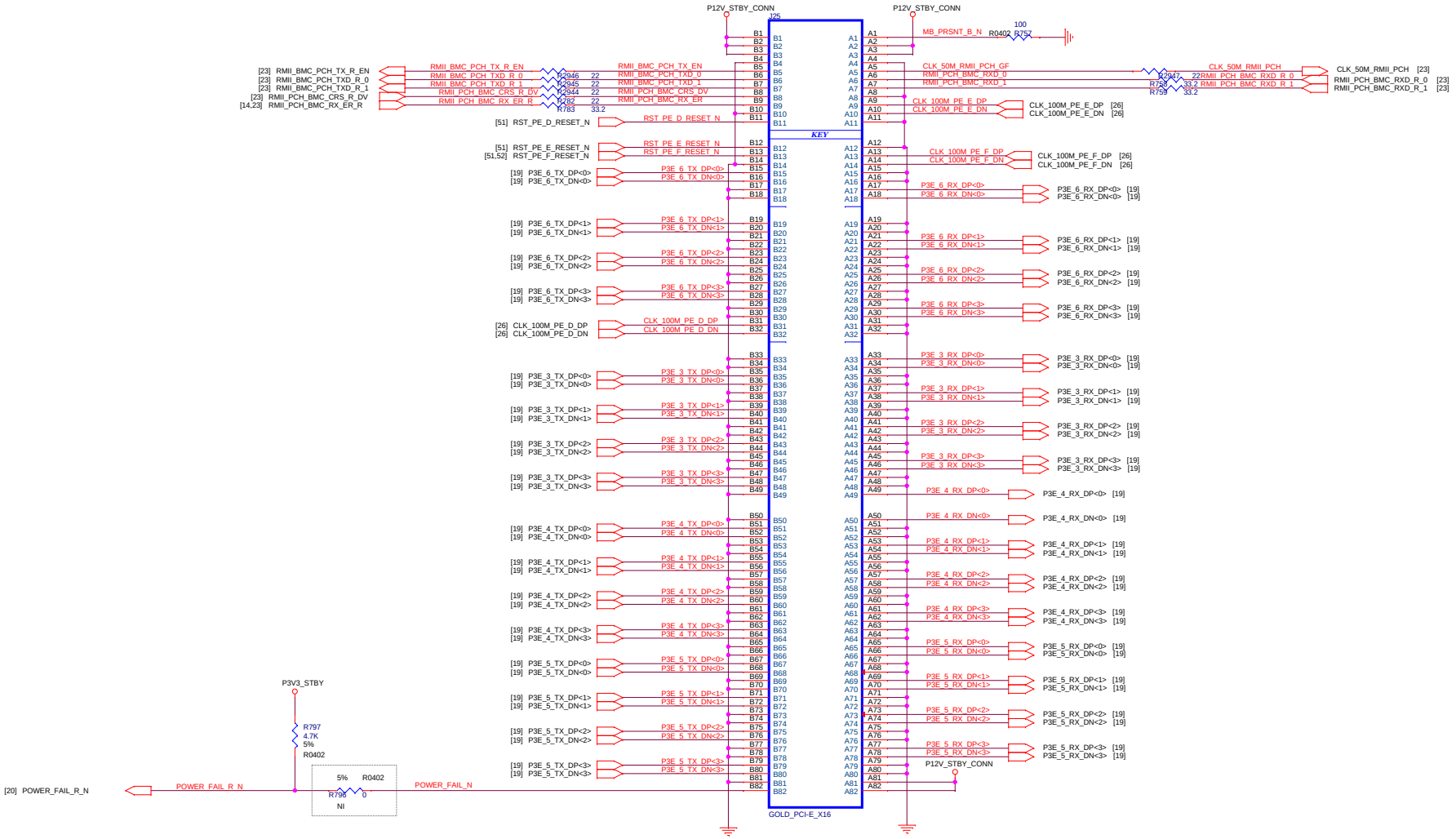

Design note :
POWER_FAIL_N is a open drain output from baseboard.

GOLD_FINGER_EXTENSION

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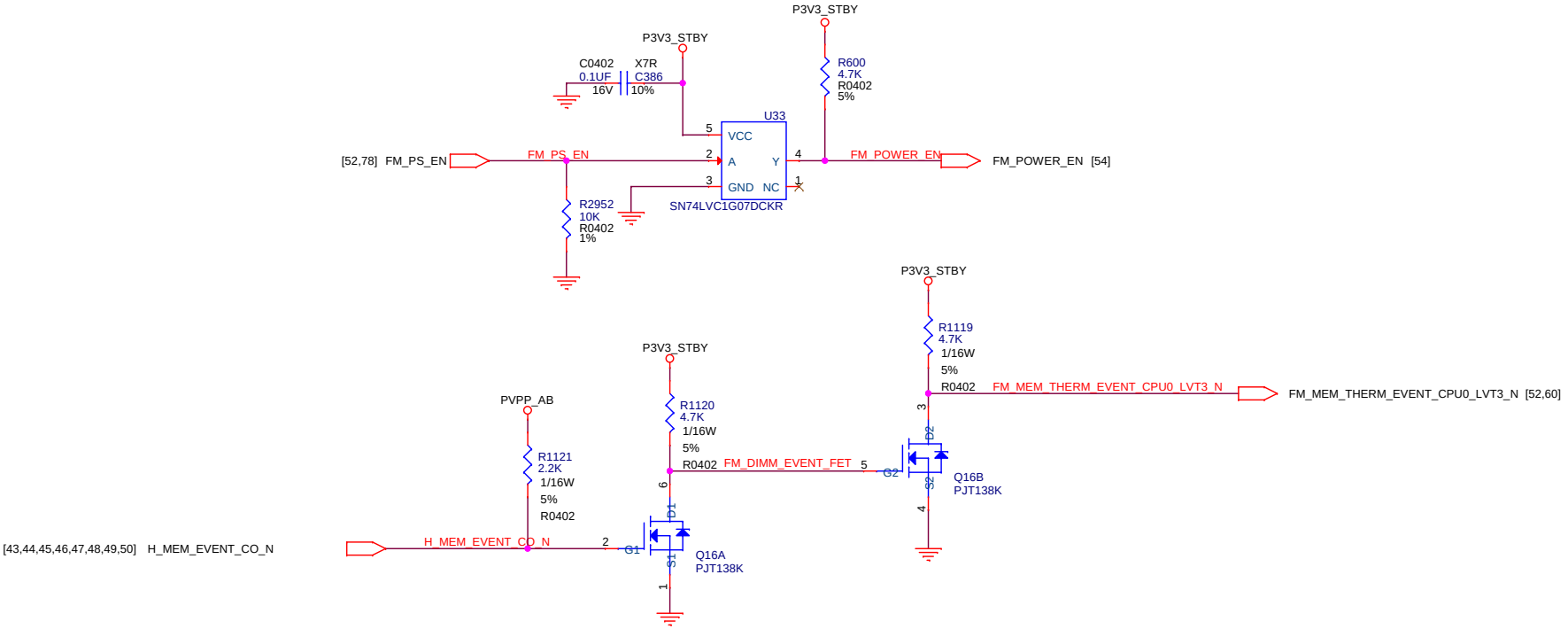

LEVEL_SHIFT<1>

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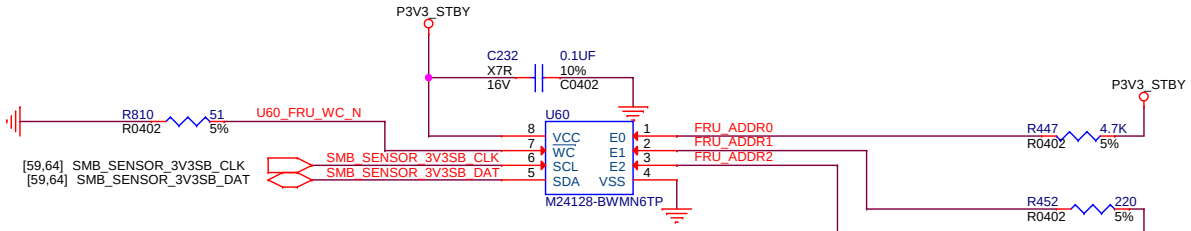
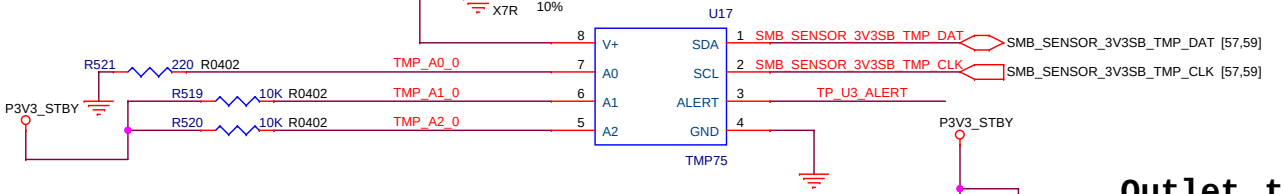
SMBus (8-bit) Address:0xA2

FRU



Outlet temp. sensor (TOP)

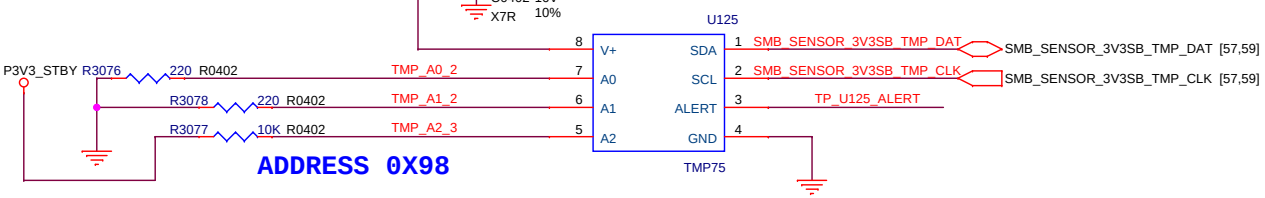
Place at TOP side close to J40 (M.2 conn)



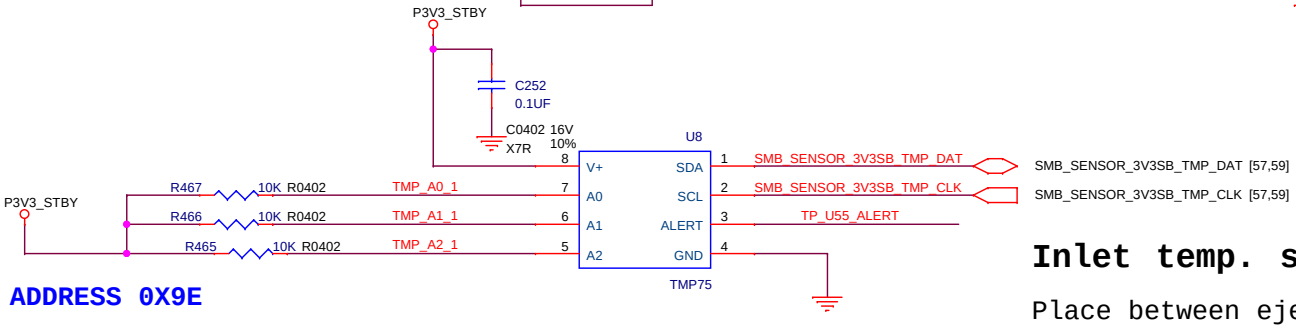
ADDRESS 0X9C

Outlet temp. sensor (BOT)

Place at BOT side close to J40 (M.2 conn)



ADDRESS 0X98



ADDRESS 0X9E

Inlet temp. sensor.

Place between ejector and radiator.

FRU & Temperature Sensor

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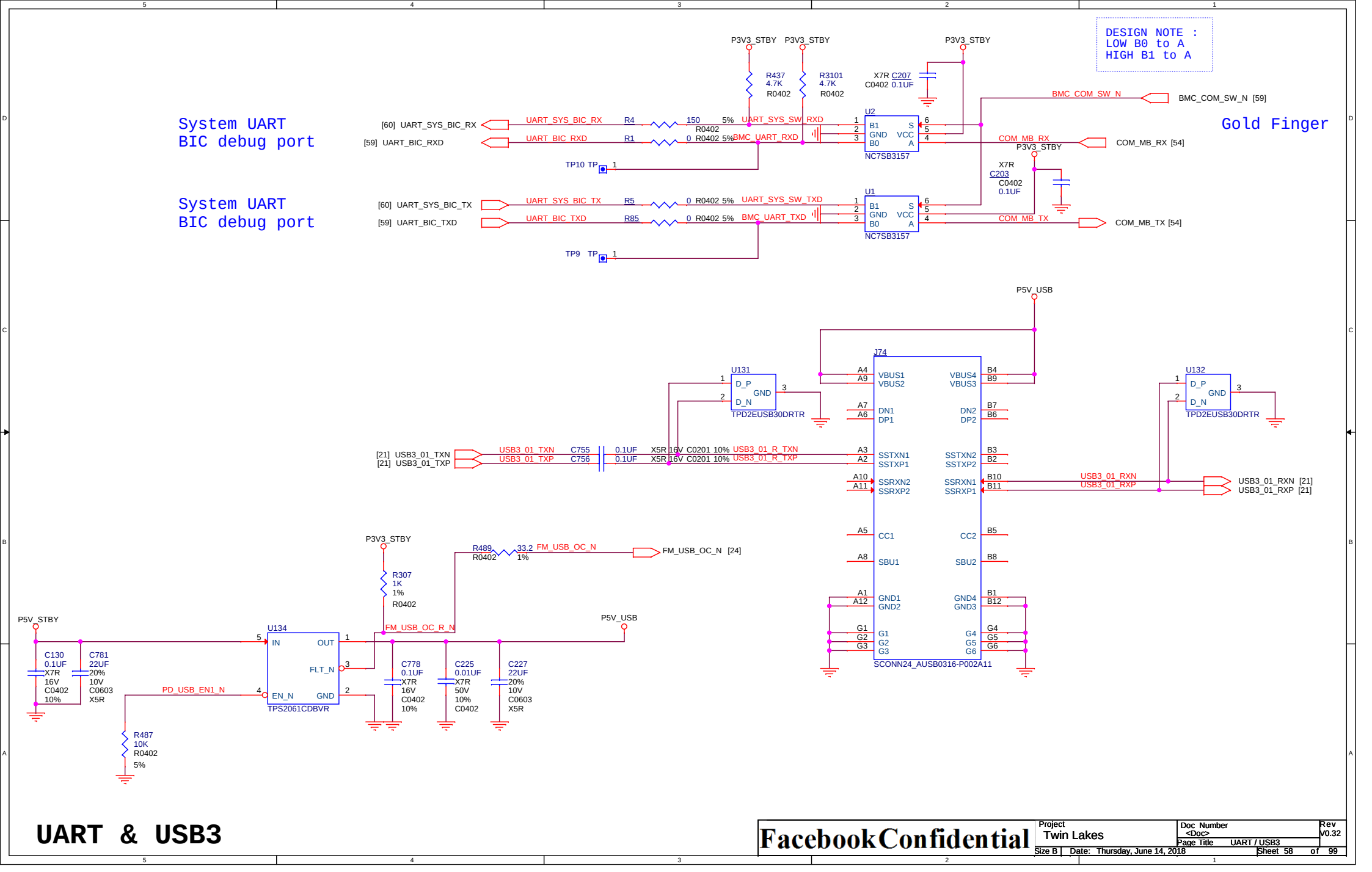

UART & USB3

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	Page Title: UART / USB3		
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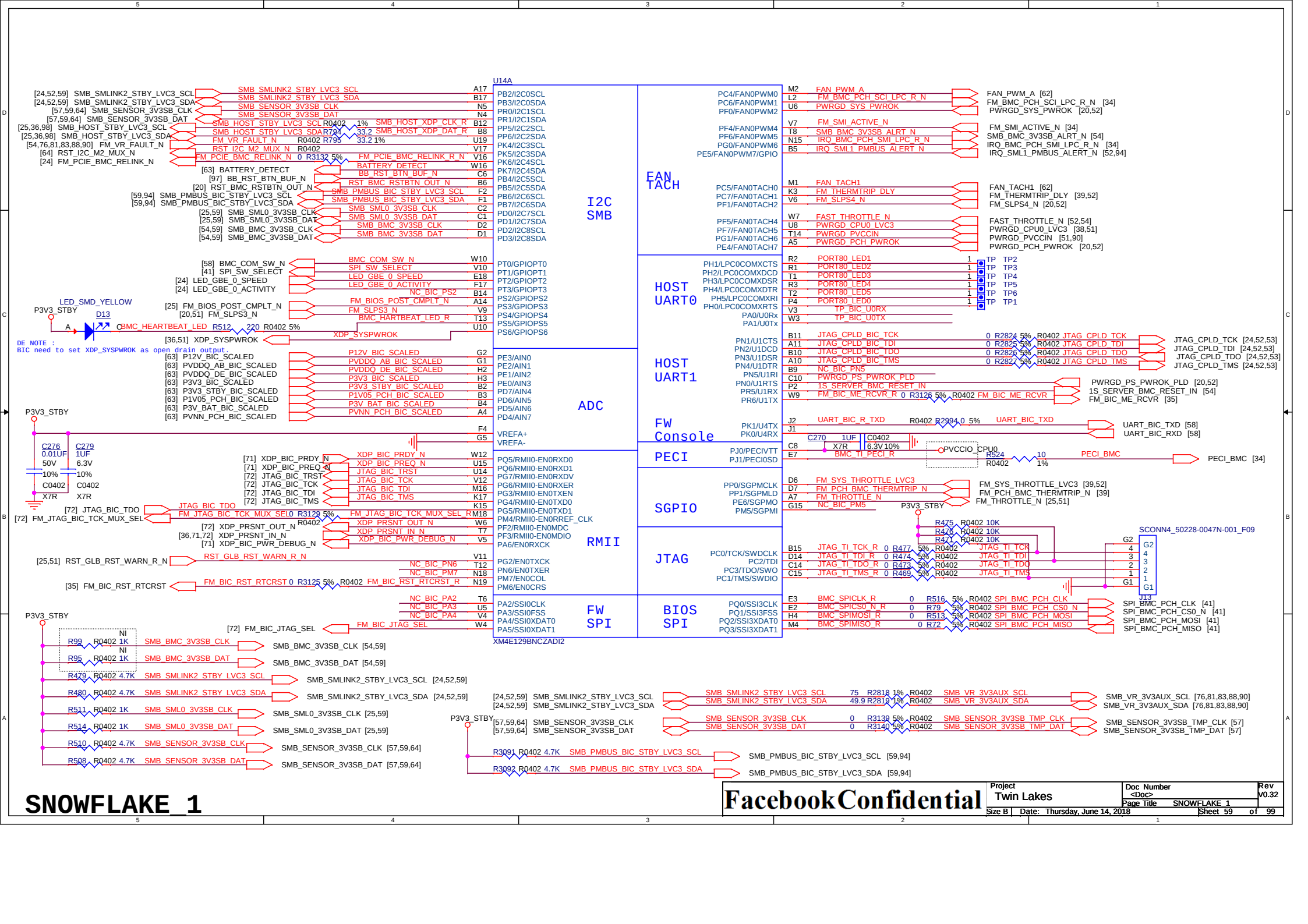
U14A
I2C SMB
FAN TACH
HOST UART0
HOST UART1
ADC
FW Console
PECI
SGPIO
RMII
JTAG
FW SPI
BIOS SPI
XM4E129BNCZADI2
SNOWFLAKE_1
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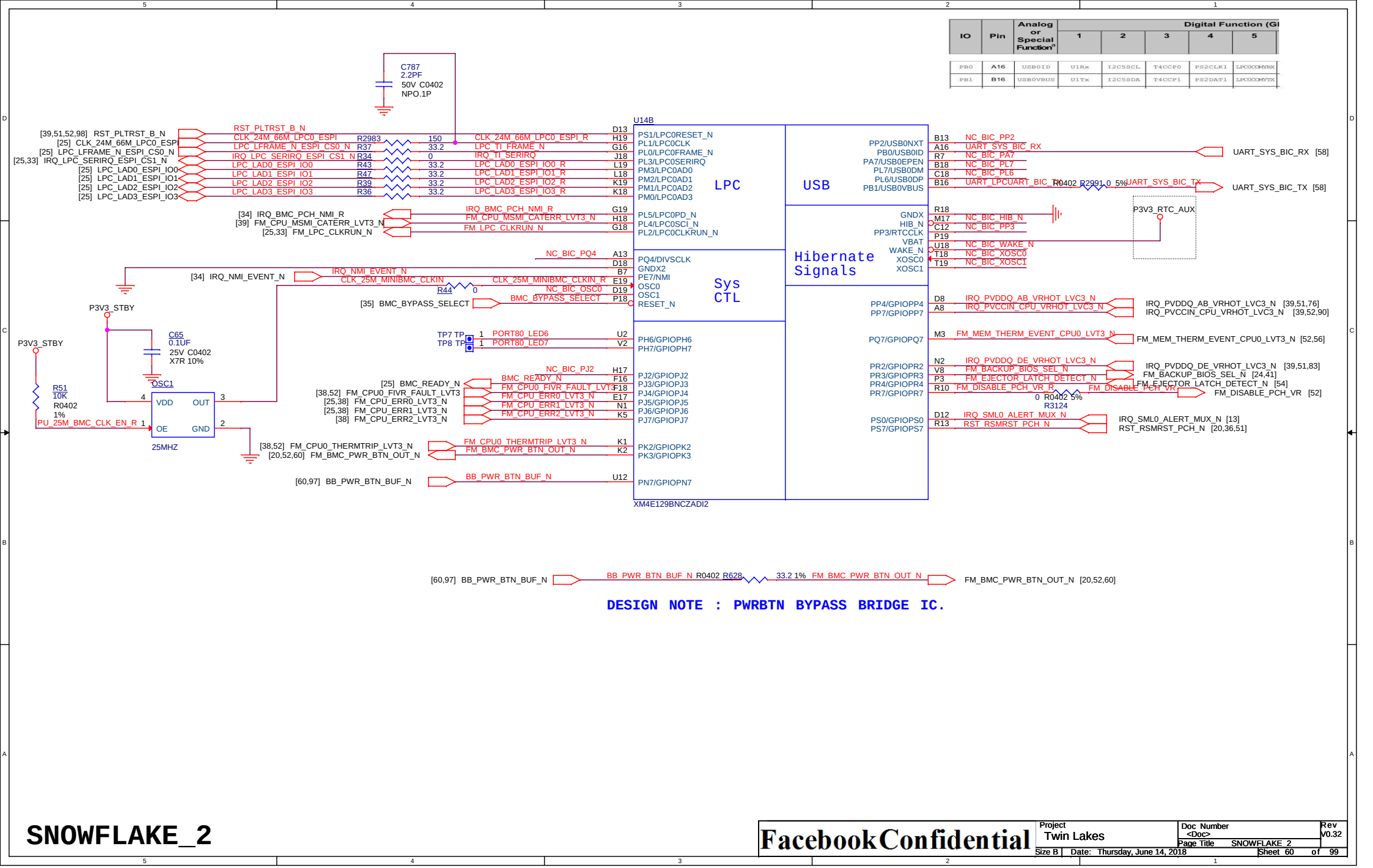

IO	Pin	Analog or Special Function[3]	Digital Function (GI 1	2	3	4	5
PB0	A16	USB0ID	U1Rx	I2C5SCL	T4CCP0	PS2CLK1	LPC0COMRX
PB1	B16	USB0VBUS	U1Tx	I2C5SDA	T4CCP1	PS2DAT1	LPC0COMTX

SNOWFLAKE_2

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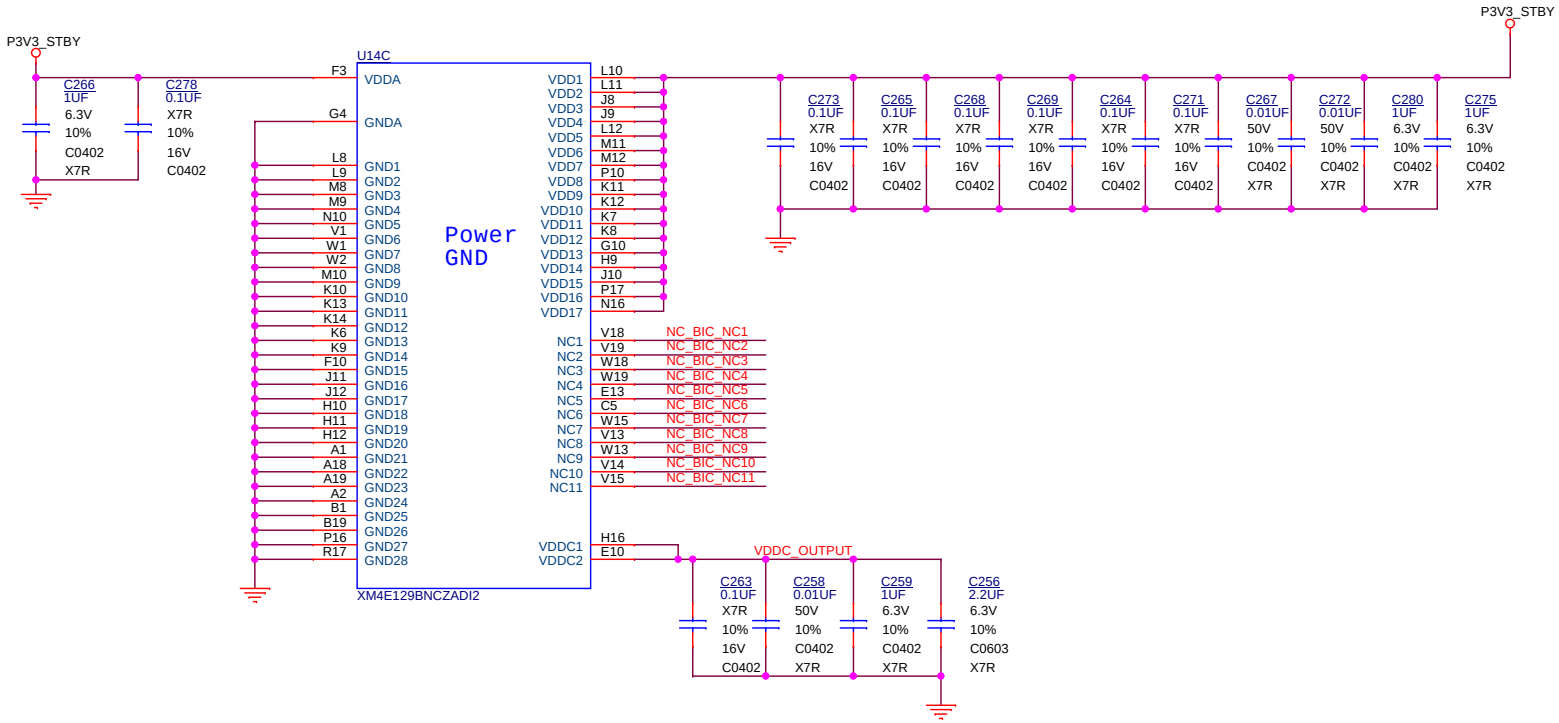

SNOWFLAKE_3

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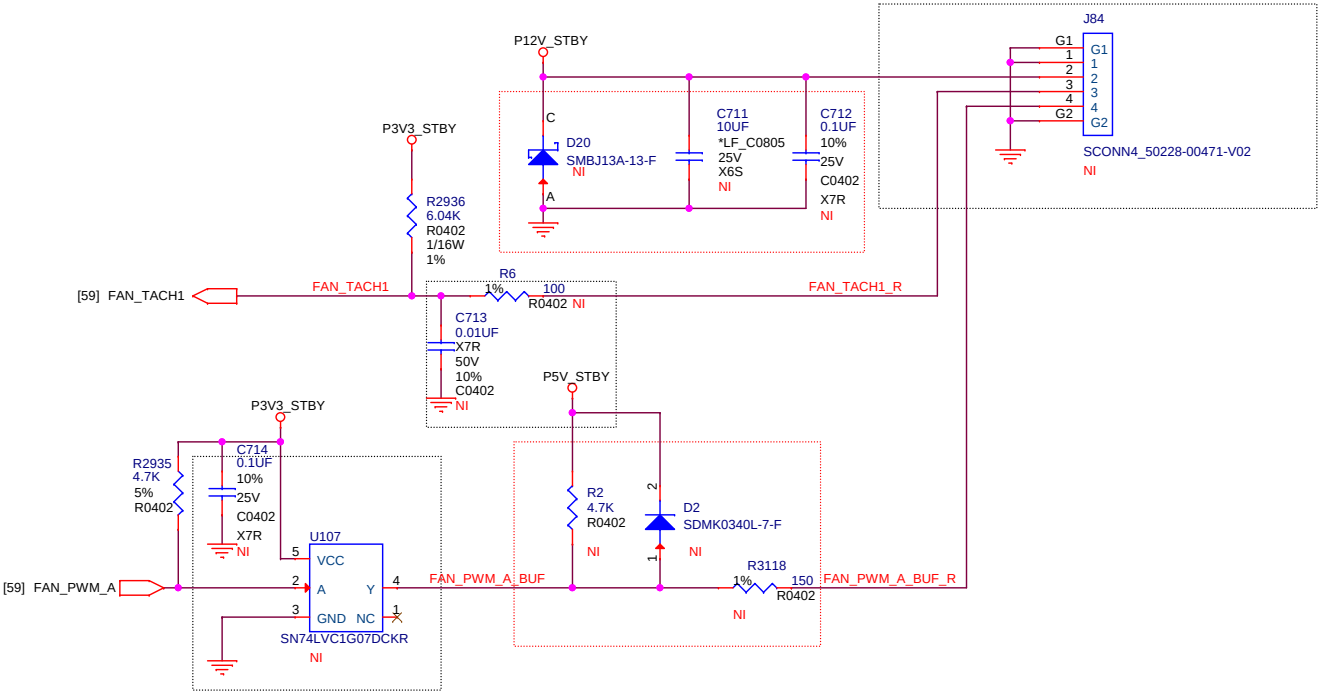
DESIGN NOTE

PMUP CONN FOR LIQUID COOLER RADIATOR



LIQUID PUMP CONNECTOR

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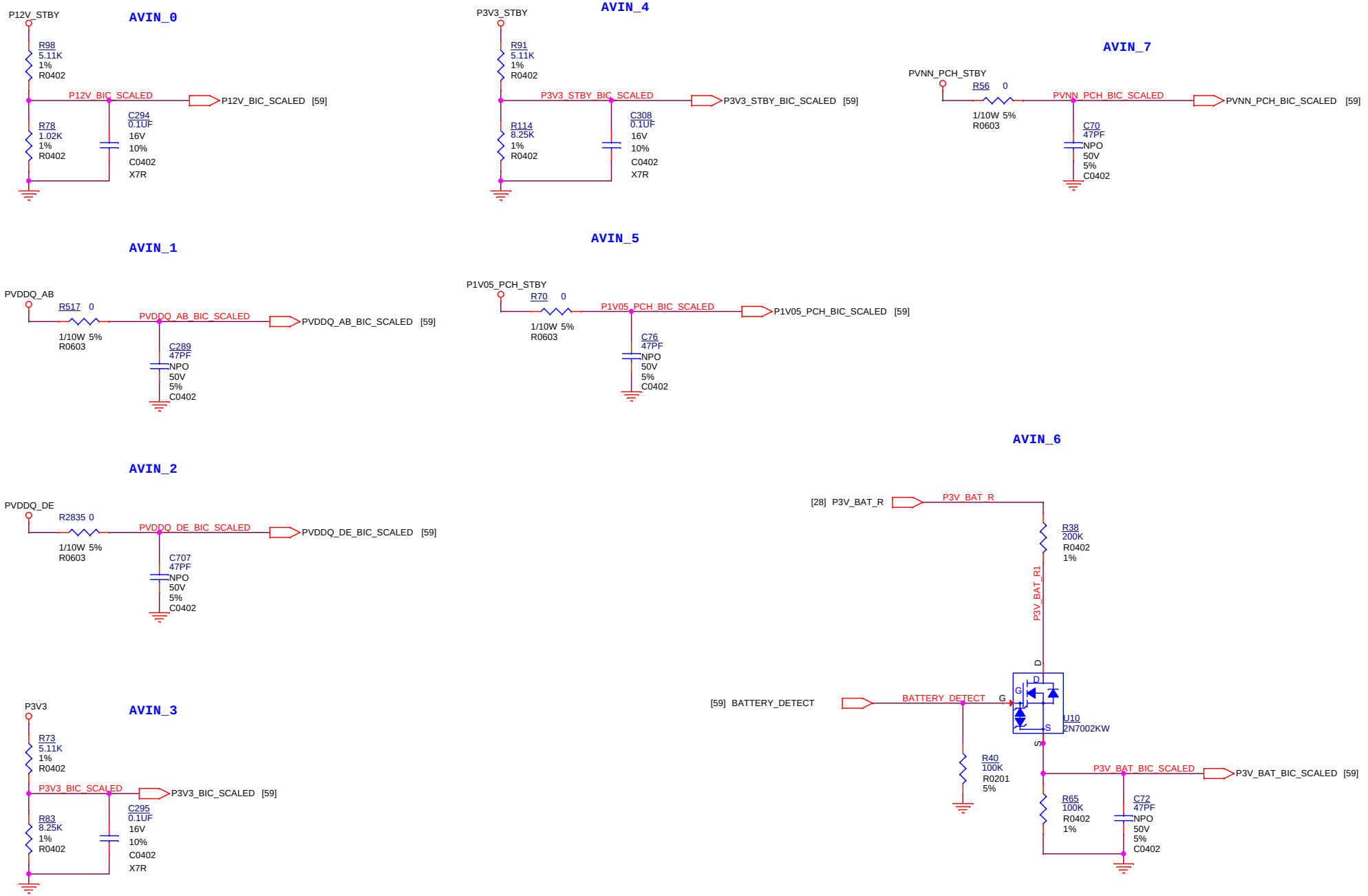

VOLTAGE MONITOR

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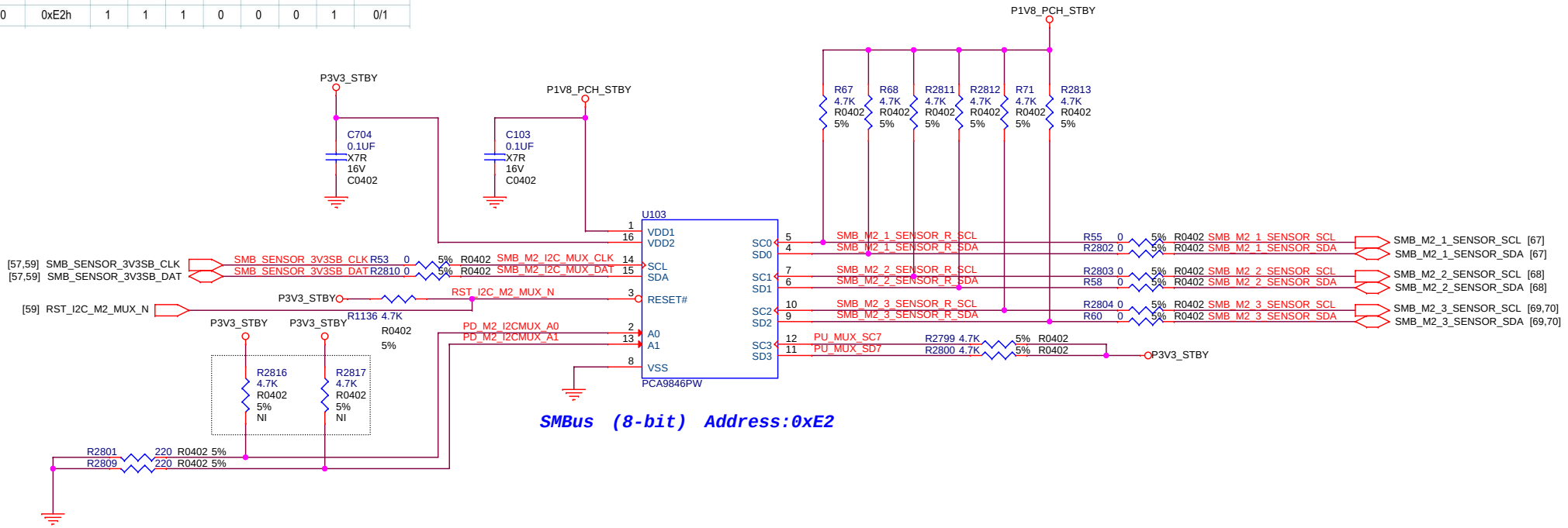
PCA9848 address pins		8-bit I²C-bus address	Slave address/bit pattern master must send							
A1	A0		A7	A6	A5	A4	A3	A2	A1	A0 - R/$\overline{W}$
0	SCL	0xE0h	1	1	1	0	0	0	0	0/1
0	0	0xE2h	1	1	1	0	0	0	1	0/1



M.2 SMBUS MUX

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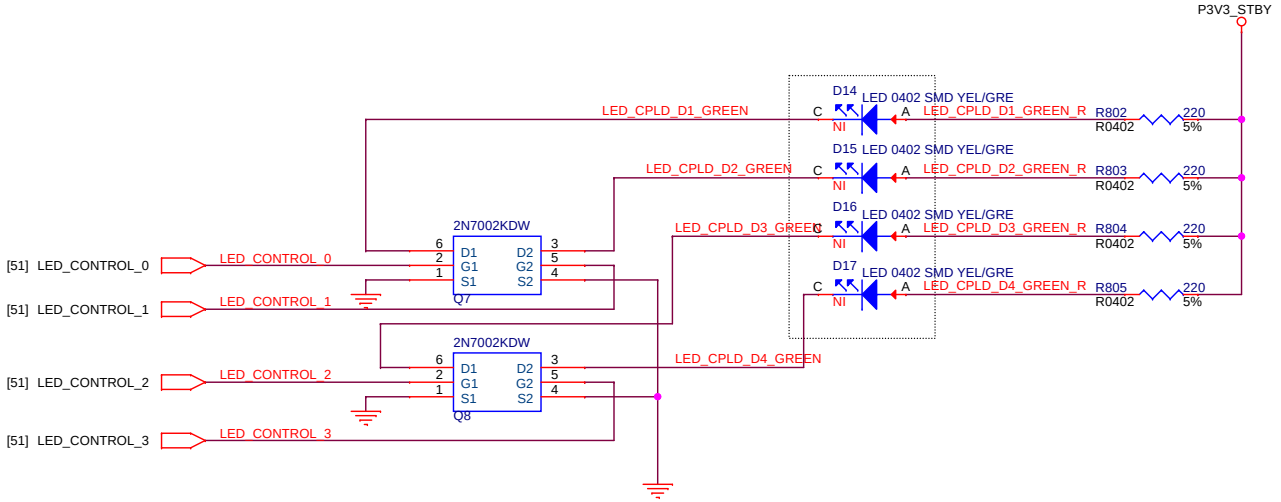
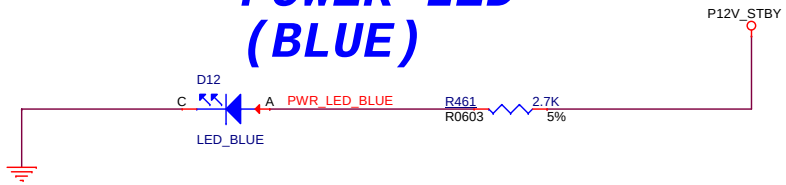
CPLD DEBUG LED



POWER LED (BLUE)



PWR / DEBUG LED

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		Page Title: PWR/ DEBUG LED	
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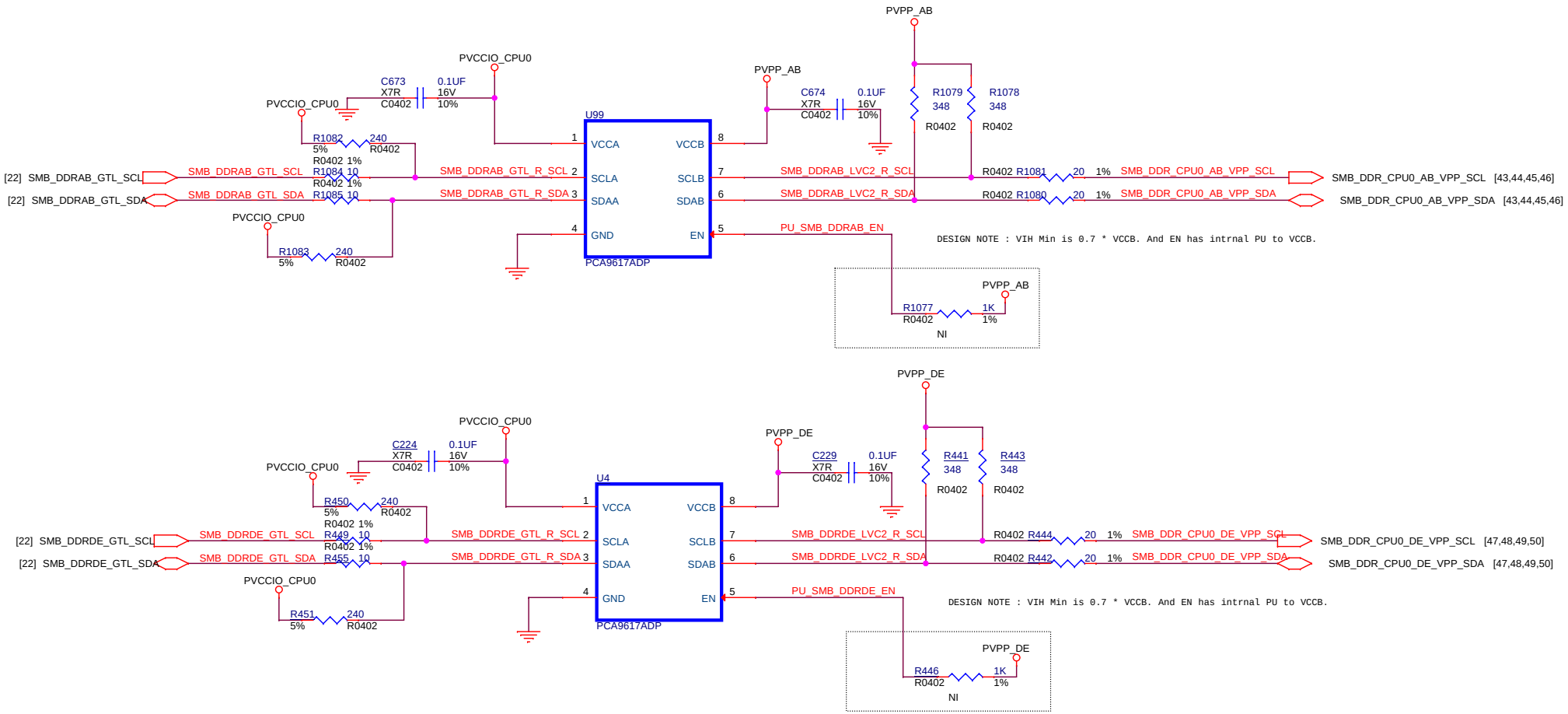

SMBUS ISOLATOR

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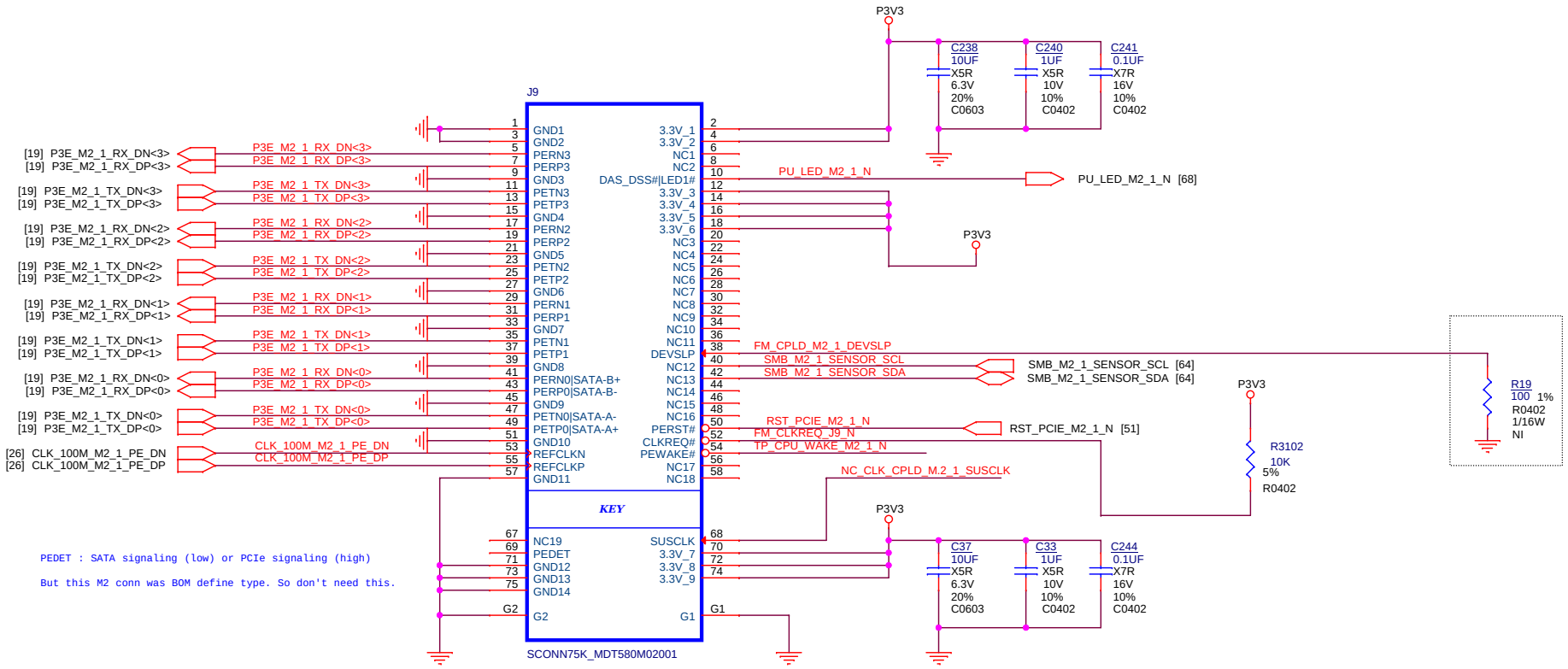

The 1st M.2 CONN

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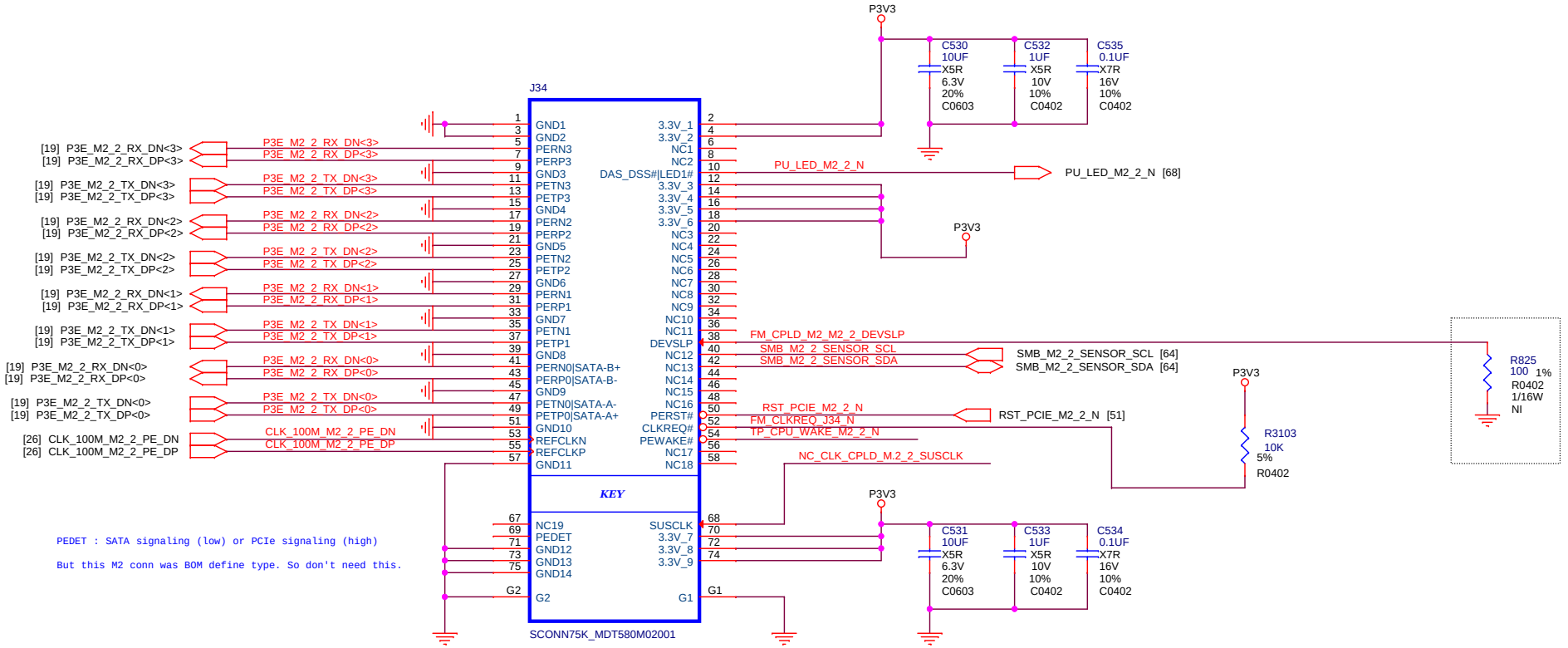

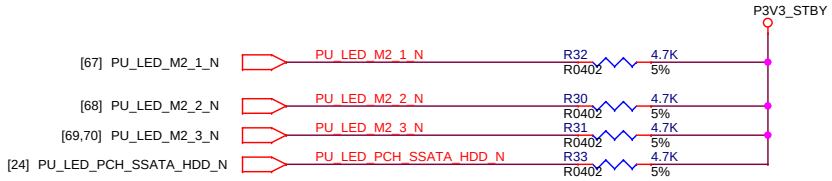

The 2nd M.2 CONN

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Project: Twin Lakes	Doc Number: <Doc>		Rev: V0.32
	Page Title: The 2nd M.2 CONN		
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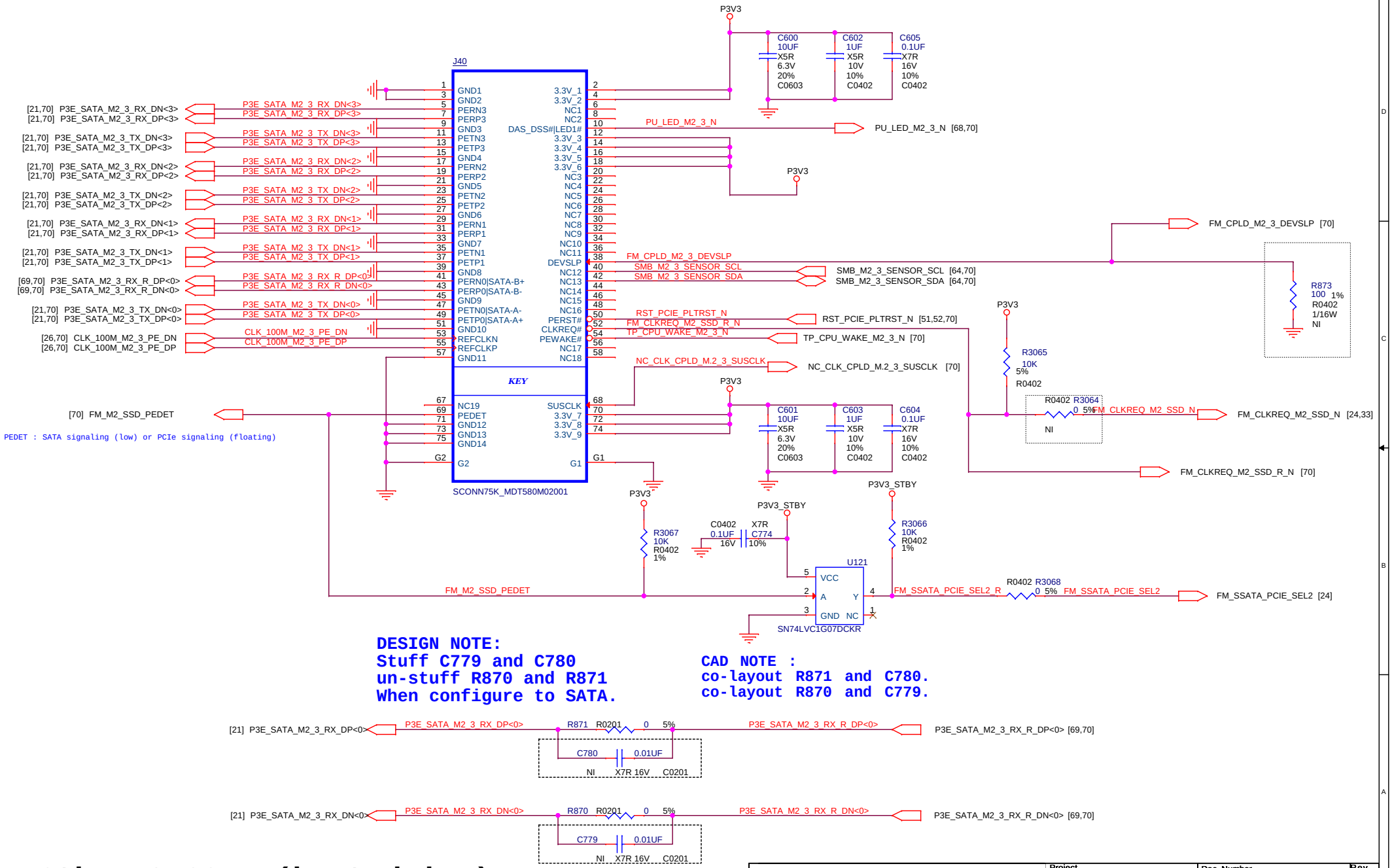

The 0th M.2 CONN (boot drive)

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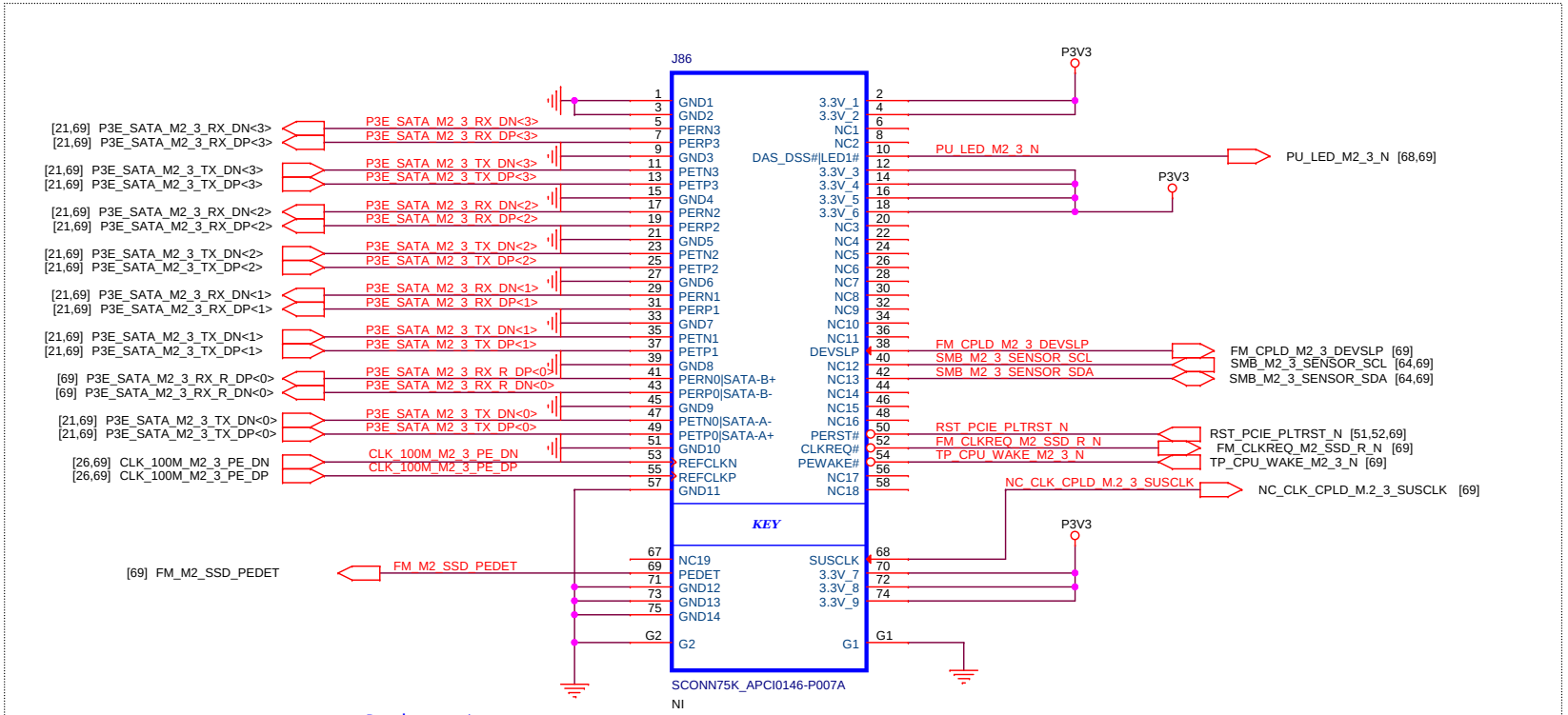
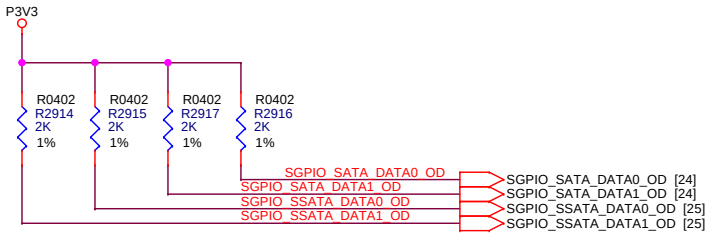
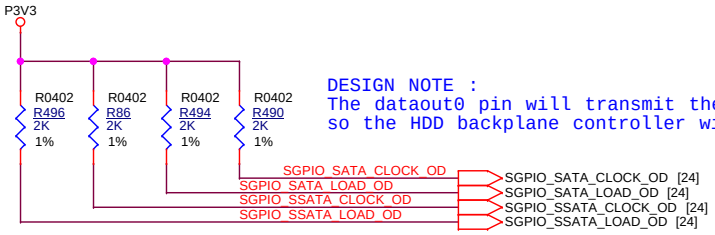


Design note :
Will only use 5.8mm M.2 connector and latch for boot drive on Yosemite V2.
But co-layout with low profile M.2 connector and latch for OCP.





DESIGN NOTE :
The dataout0 pin will transmit the LED information for all 6 drives.
so the HDD backplane controller will need to ignore the first two drives of the SGPIO packet.

SGPIO

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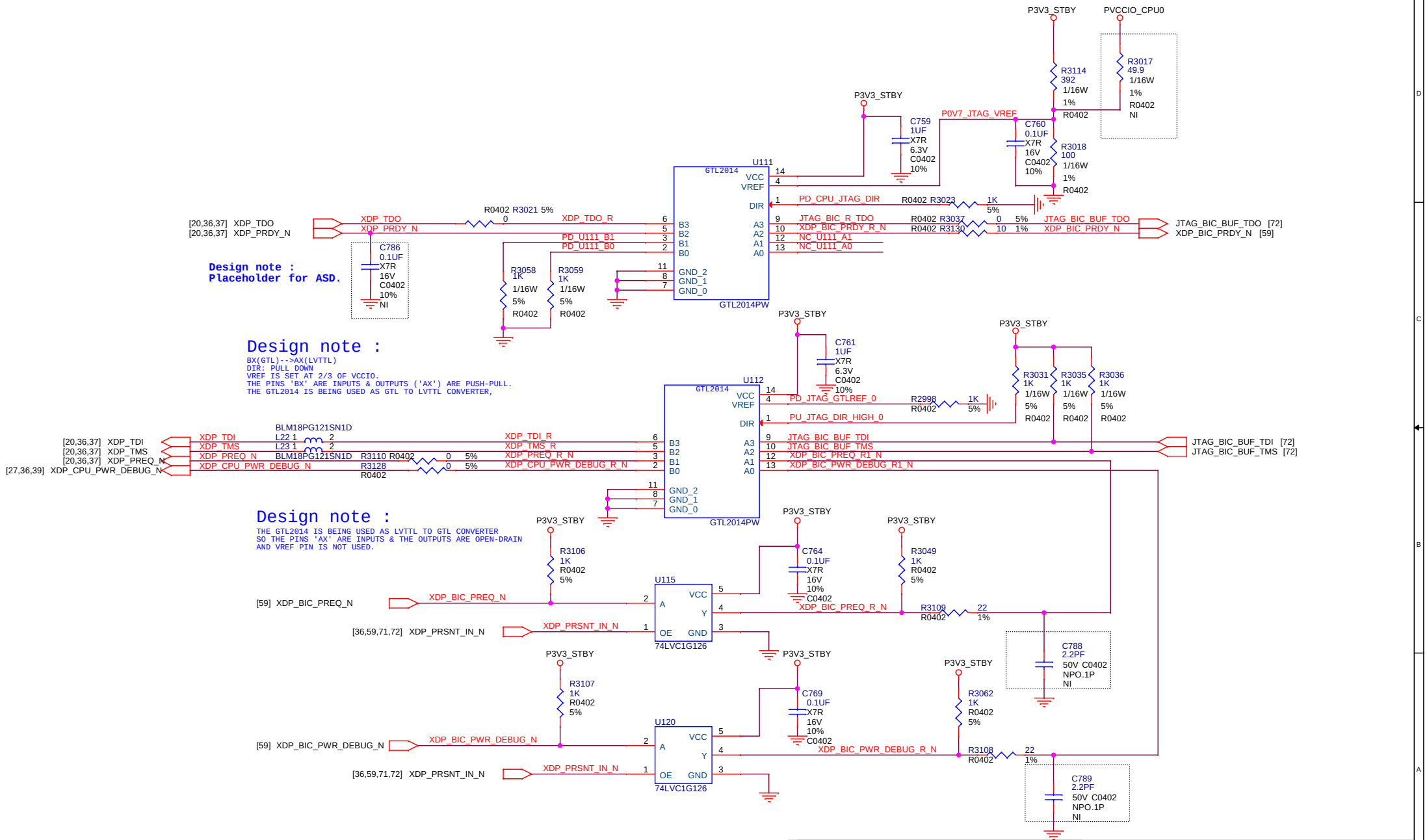

BMC REMOTE DEBUG[1]

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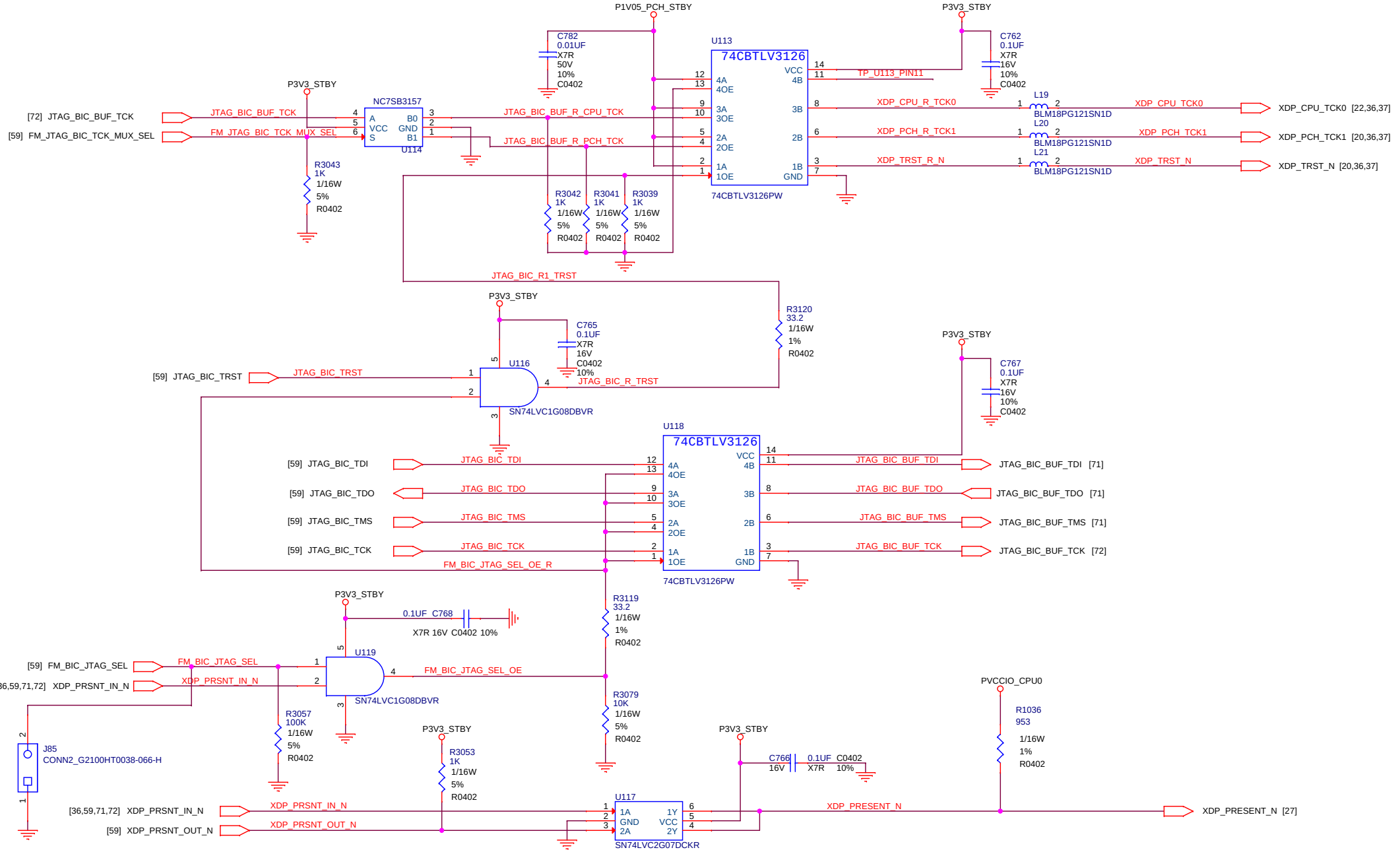

BMC REMOTE DEBUG[2]

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		Page Title: BMC REMOTE DEBUG[2]	
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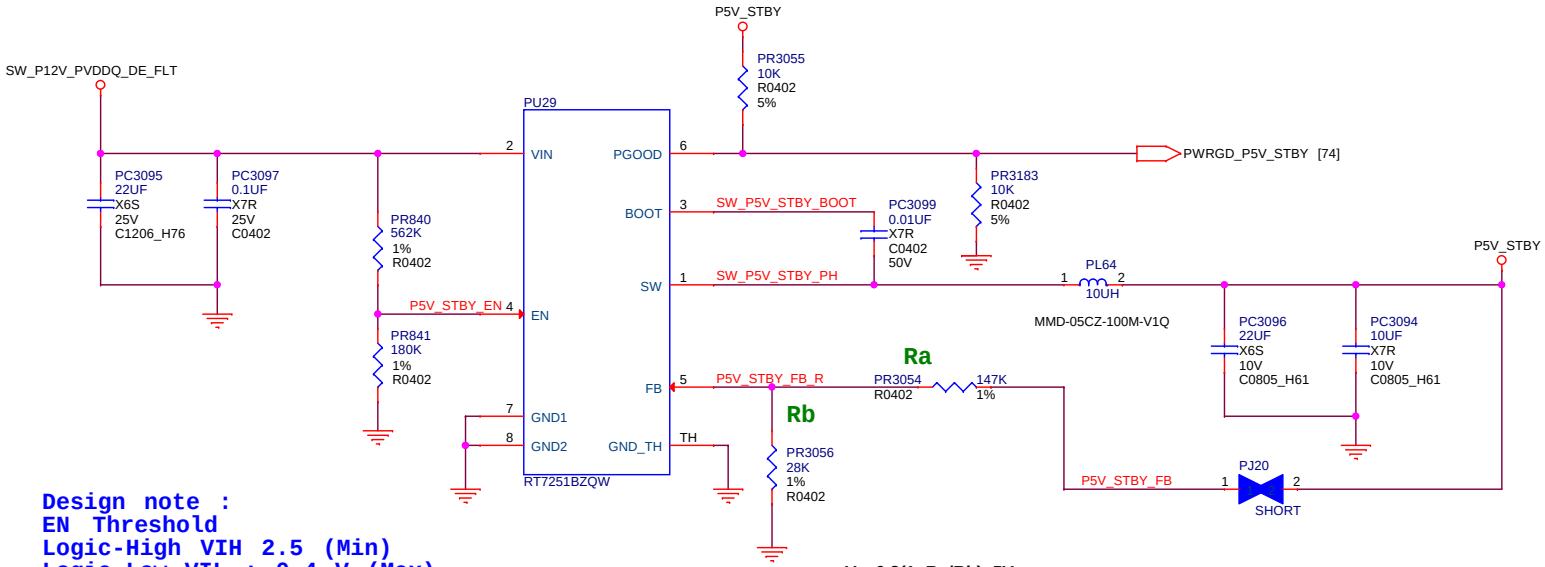
P5V_STBY Design specification

Output Voltage = 5V± 5 %
Output Ripple & Noise : ± 0 5 %
Transient Tolerance = 500mV
TDC = 0.2A
Max current =0.2A
Current step=0.1A
Over-Current Protection(IC rating) = 2.6A
Slew Rate = 0.1 A/us
Work Frequency = 800kHZ
Efficiency > 80% @TDC



P5V_STBY

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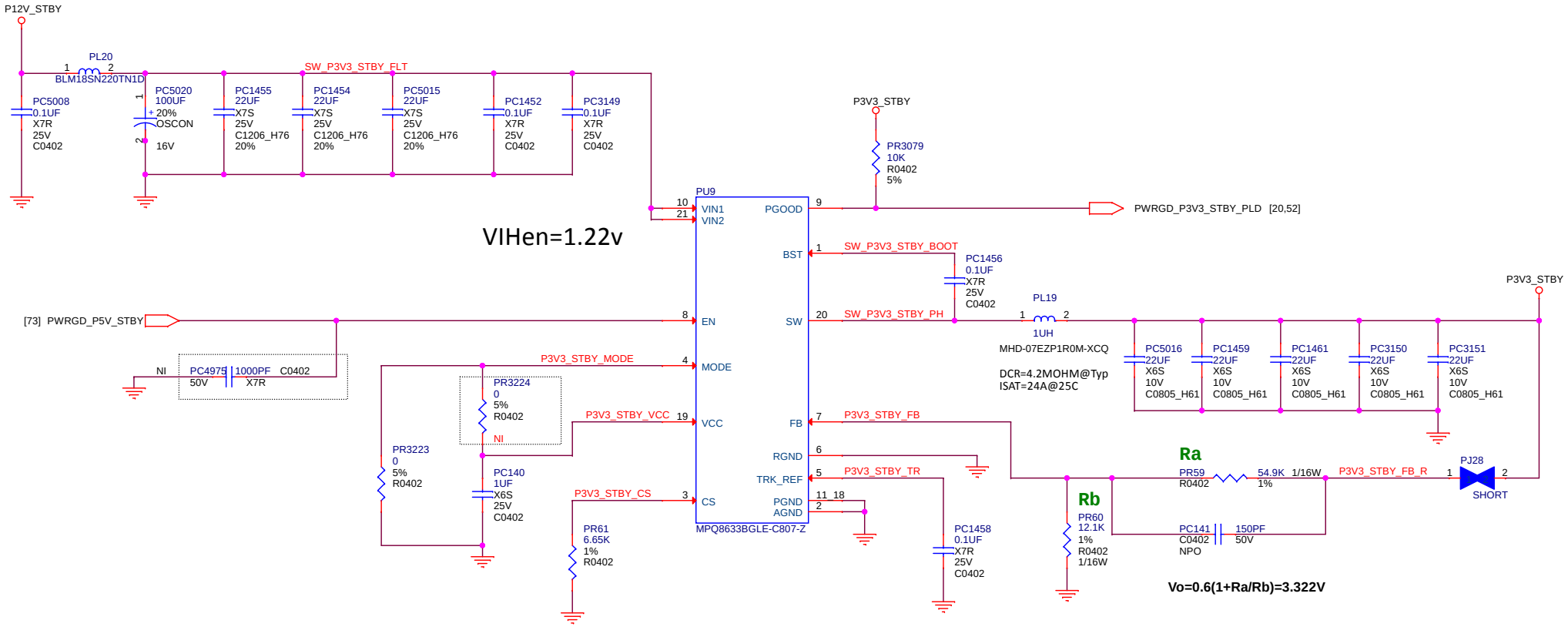
Design specification

Output Voltage = 3.3V± 5 %
Output Ripple & Noise ± 0 5 %
Transient Tolerance = 330mV
TDC = 12.68A
Max current = 14A
OCP(IMAX*130%)=18.2A
Current Step = 6 A
Slew Rate = 1 A/us
Work frequency = 600KHZ
Efficiency > 90% @TDC



P3V3_STBY

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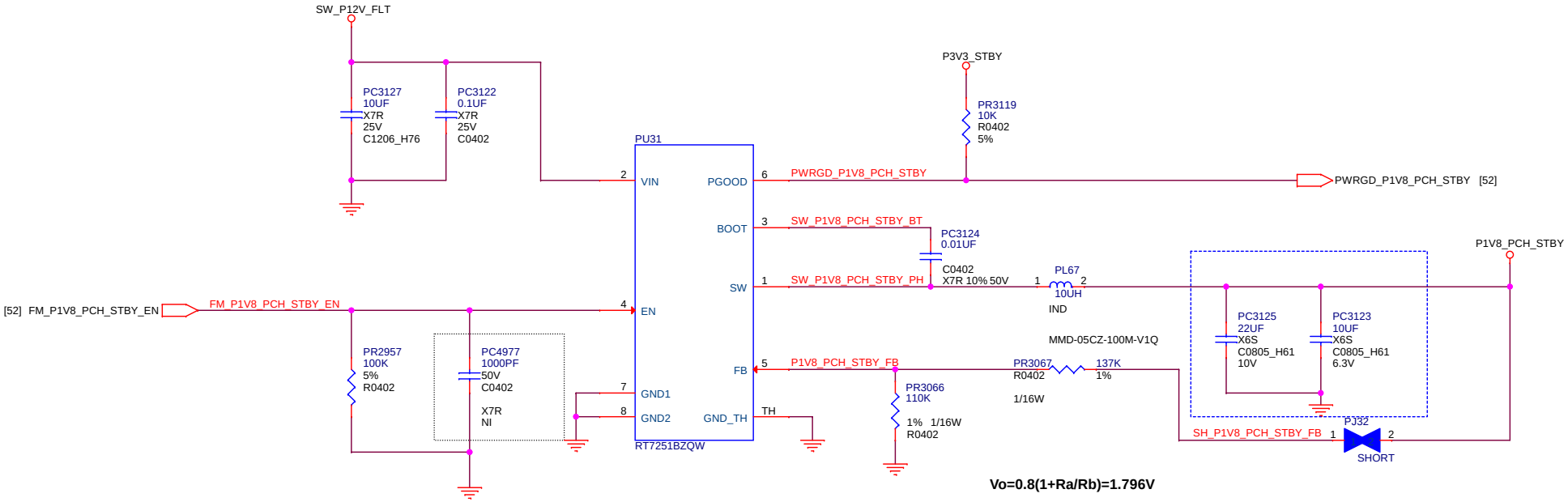
P1V8_PCH_STBY Design SPECIFICATION

OUTPUT VOLTAGE=1.8V
OUTPUT RIPPLE=+/-18MV
TRANSIENT TOLERANCE=+/-90MV
TDC=0.65A
MAX CURRENT=1A
OVER CURRENT PROTECTION(IC RATING)=2.6A
CURRENT STEP=0.35A
SLEW RATE=8A/US
WORK FREQUENCY=800KHZ
Efficiency > 80% @TDC



Vo=0.8(1+Ra/Rb)=1.796V

DESIGN NOTE:

To workaround a voltage leakage issue on P1V8_PCH_STBY power rail then cause over voltage protection.

Workaround :
1. Change PC3123 to a bleeding 100ohm 0805 resistor.
2. Change PC3125 to 47uF 0805 4V X6S capacitor.

P1V8_PCH_STBY

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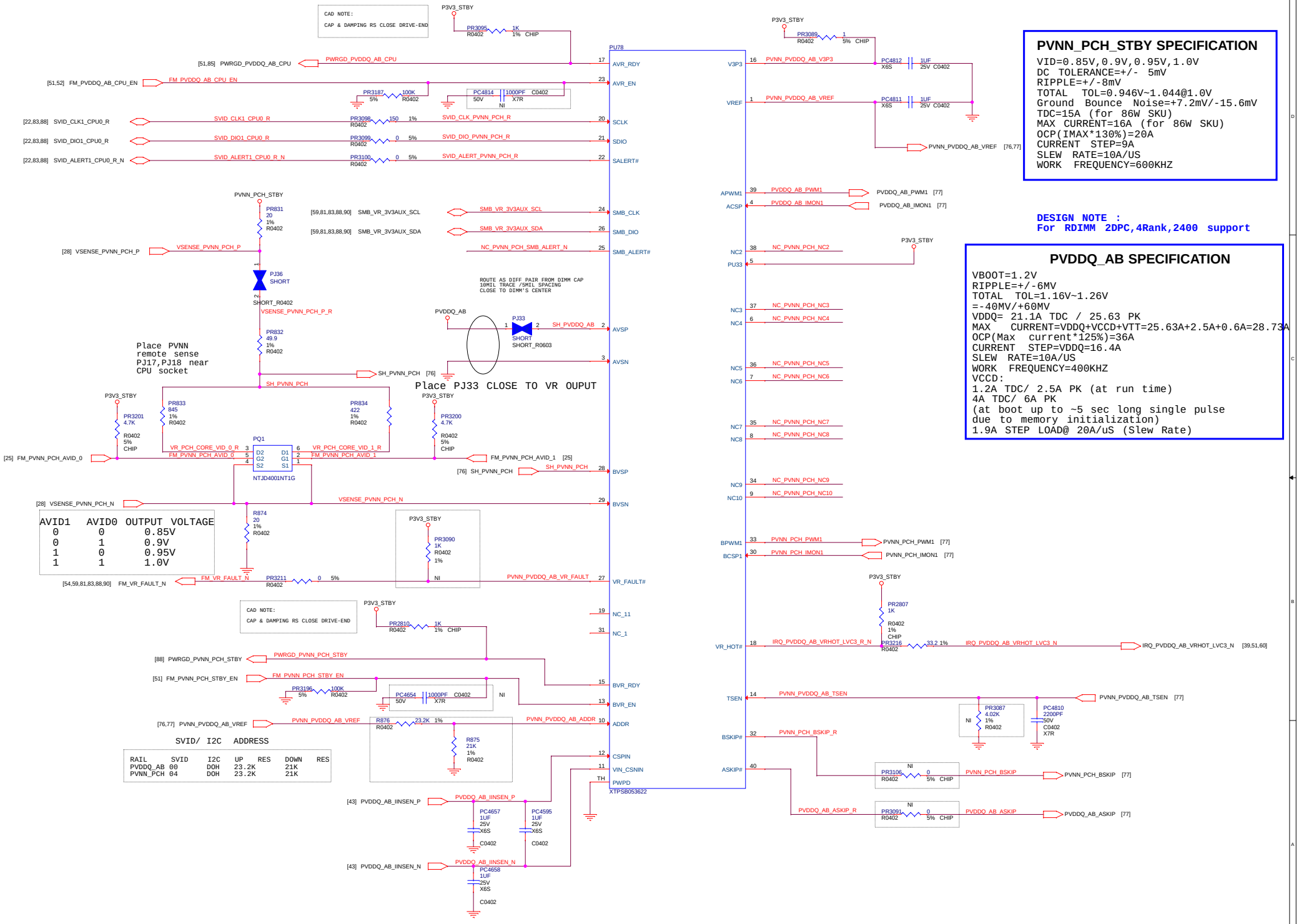

PVNN_PCH_STBY SPECIFICATION

VID=0.85V,0.9V,0.95V,1.0V
DC TOLERANCE=+/- 5mV
RIPPLE=+/-8mV
TOTAL TOL=0.946V~1.044@1.0V
Ground Bounce Noise=+7.2mV/-15.6mV
TDC=15A (for 86W SKU)
MAX CURRENT=16A (for 86W SKU)
OCP(IMAX*130%)=20A
CURRENT STEP=9A
SLEW RATE=10A/US
WORK FREQUENCY=600KHZ

DESIGN NOTE :
For RDIMM 2DPC,4Rank,2400 support

PVDDQ_AB SPECIFICATION

VBOOT=1.2V
RIPPLE=+/-6MV
TOTAL TOL=1.16V~1.26V
=-40MV/+60MV
VDDQ= 21.1A TDC / 25.63 PK
MAX CURRENT=VDDQ+VCCD+VTT=25.63A+2.5A+0.6A=28.73A
OCP(Max current*125%)=36A
CURRENT STEP=VDDQ=16.4A
SLEW RATE=10A/US
WORK FREQUENCY=400KHZ
VCCD:
1.2A TDC/ 2.5A PK (at run time)
4A TDC/ 6A PK
(at boot up to ~5 sec long single pulse
due to memory initialization)
1.9A STEP LOAD@ 20A/uS (Slew Rate)

PVNN & PVDDQ_AB [1]

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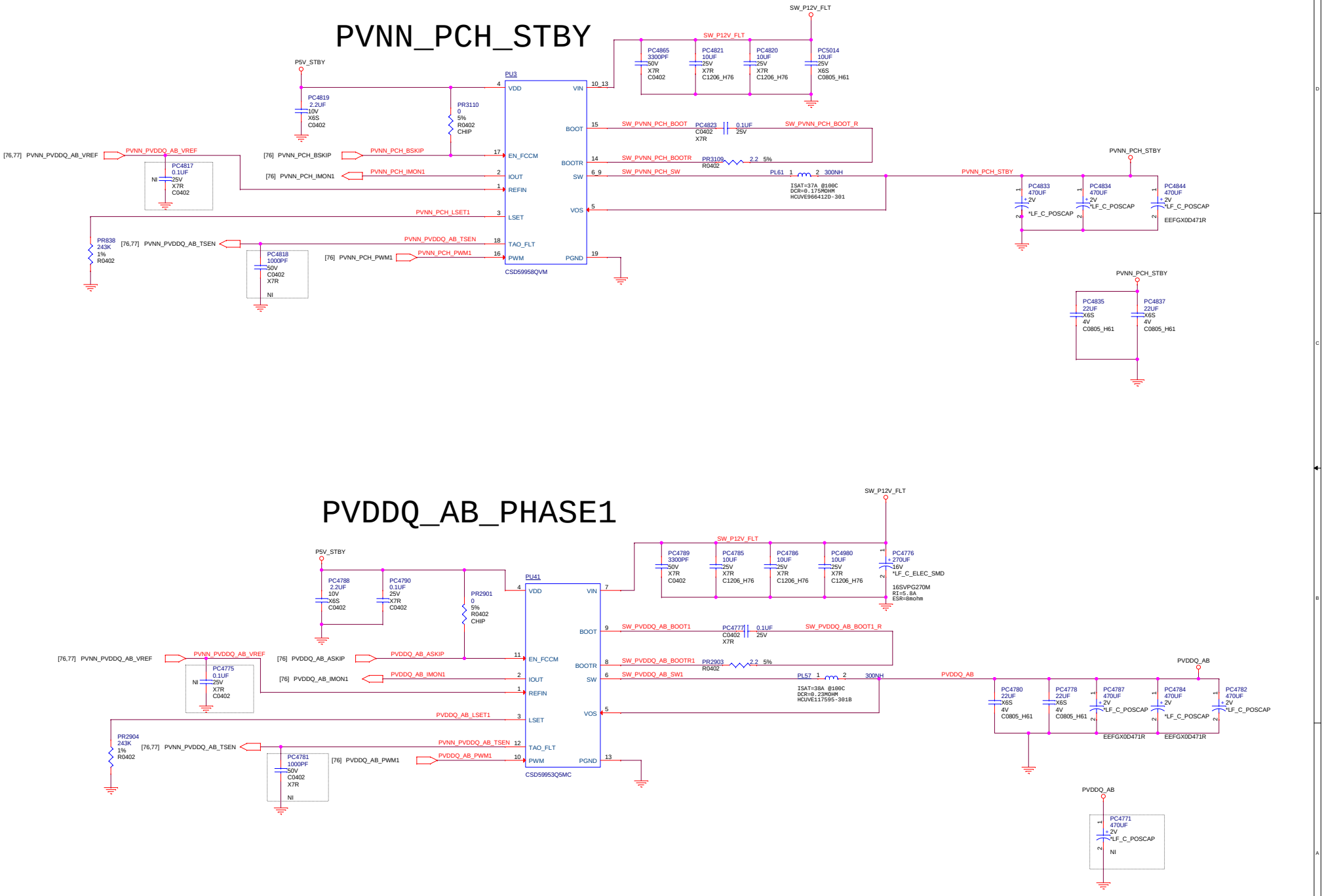

PVNN & PVDDQ_AB [2]

Project: Twin Lakes	Doc Number: <Doc>	Rev: V0.32
	Page Title: PVNN & PVDDQ_AB[2]	
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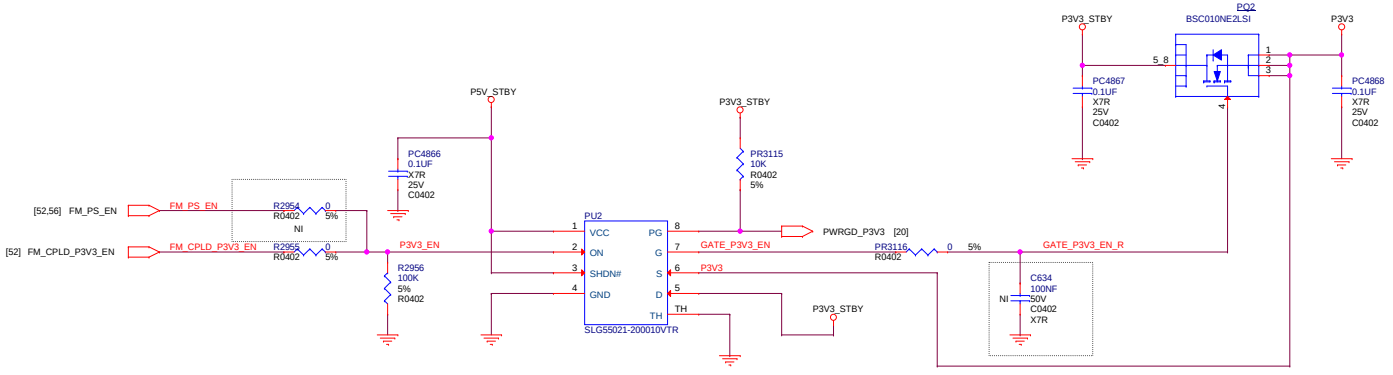
Design Note
Max Loading: 15.5A

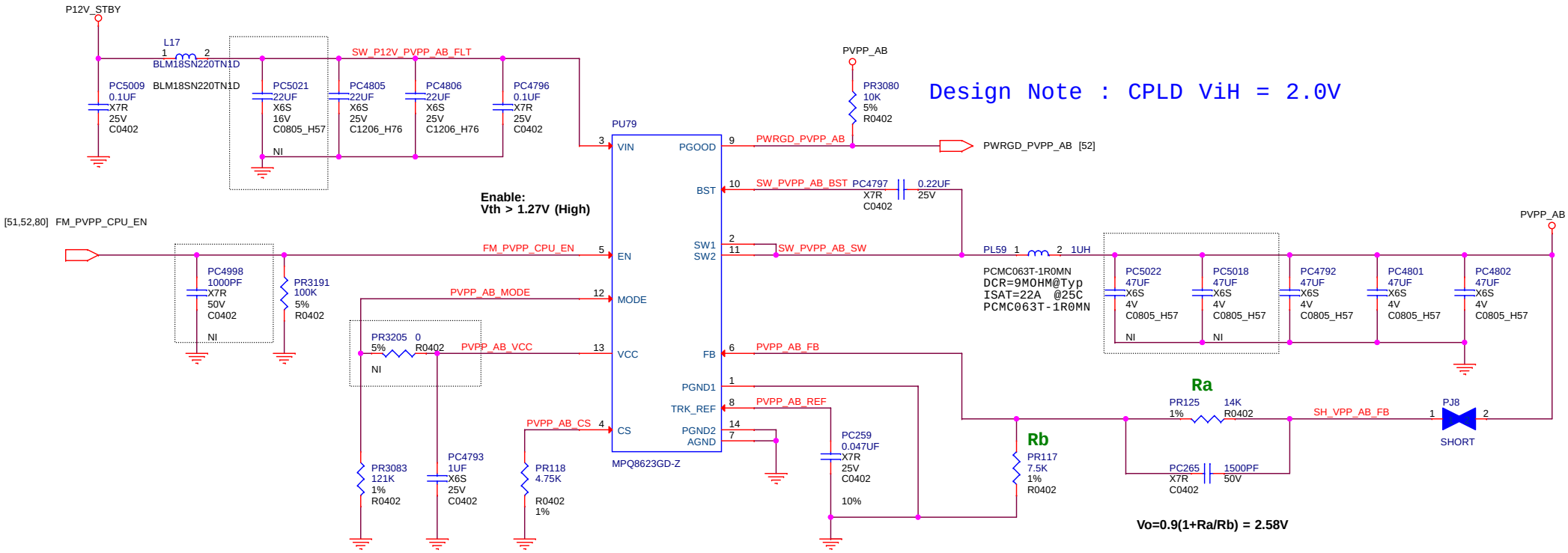


Create one pin from CPLD should be a delay version on FM_PS_EN

P3V3 POWER SWITCH

PVPP_AB Design specification

OUTPUT VOLTAGE=2.58V
OUTPUT RIPPLE<+/-25MV
DC TOLERANCE = +/- 37.5MV
Total Allowable Tolerance=+175MV/-165MV(2.75V/2.41V)
@ DIMM GOLDEN FINGER
TDC=4.4A
MAX CURRENT=5.94A
OCP(IMAX*130%)=7.8A
CURRENT STEP=3.54A
SLEW RATE=14.34A/US
Work frequency = 660KHZ
Efficiency > 90% @TDC



PVPP_AB VR

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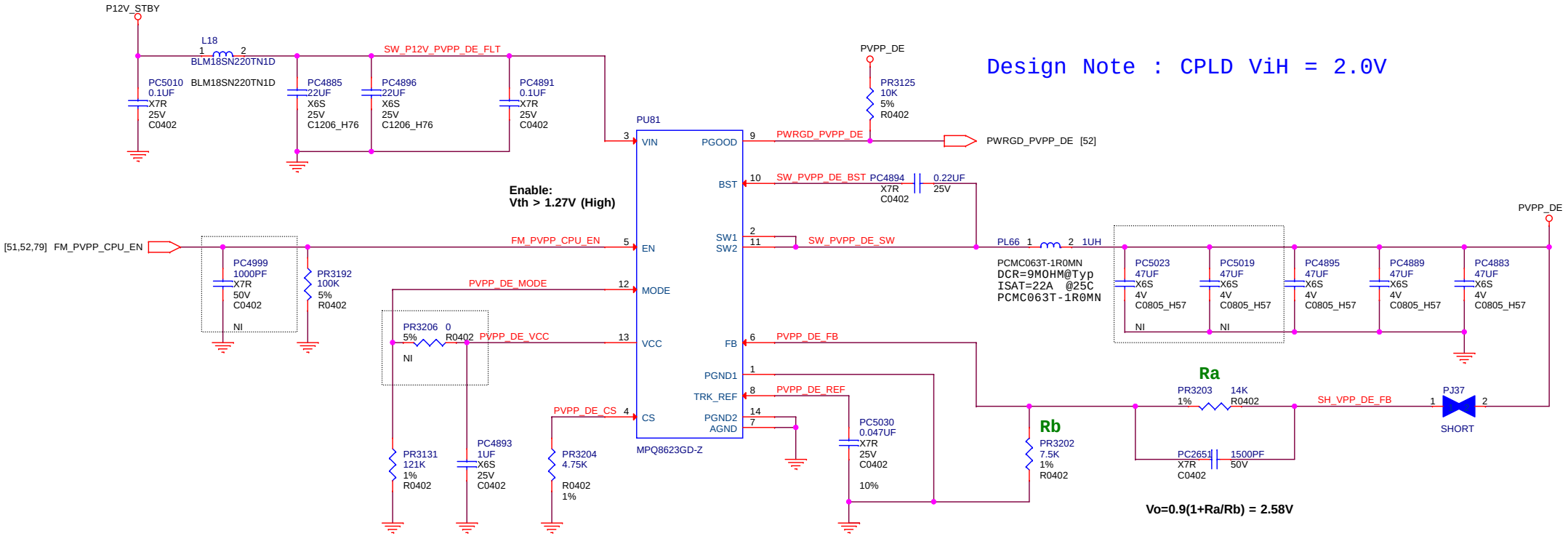
PVPP_DE Design specification

OUTPUT VOLTAGE=2.58V
OUTPUT RIPPLE<+/-25MV
DC TOLERANCE = +/- 37.5MV
Total Allowable Tolerance=+175MV/-165MV(2.75V/2.41V)
@ DIMM GOLDEN FINGER
TDC=4.4A
MAX CURRENT=5.94A
OCP(IMAX*130%)=7.8A
CURRENT STEP=3.54A
SLEW RATE=14.34A/US
Work frequency = 660KHZ
Efficiency > 90% @TDC



PVPP_DE VR

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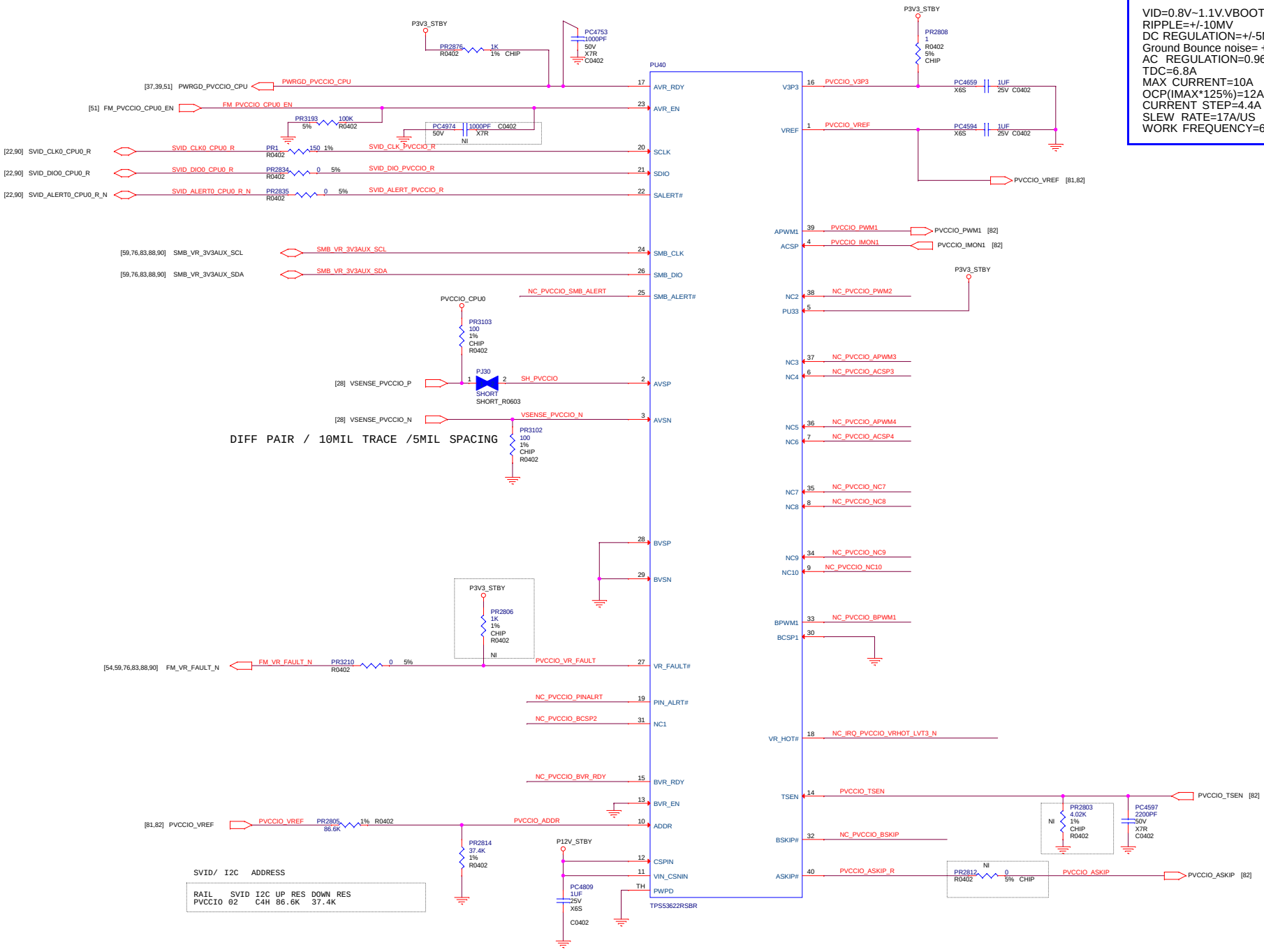

Project: Twin Lakes	Doc Number: <Doc>	Rev: V0.32
	Page Title: PVCCIO[1]	
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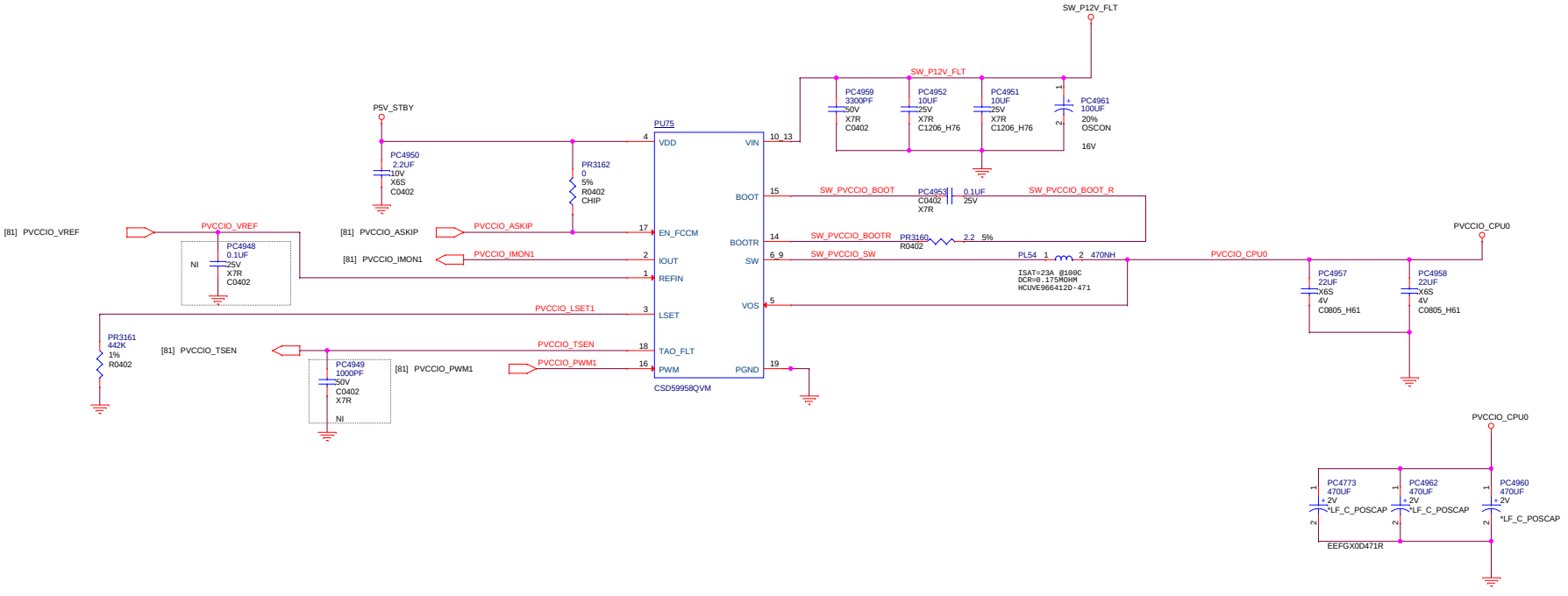
PVCCIO PHASE



PVCCIO_PHASE

Project: Twin Lakes	Doc Number: <Doc>		Rev: V0.32
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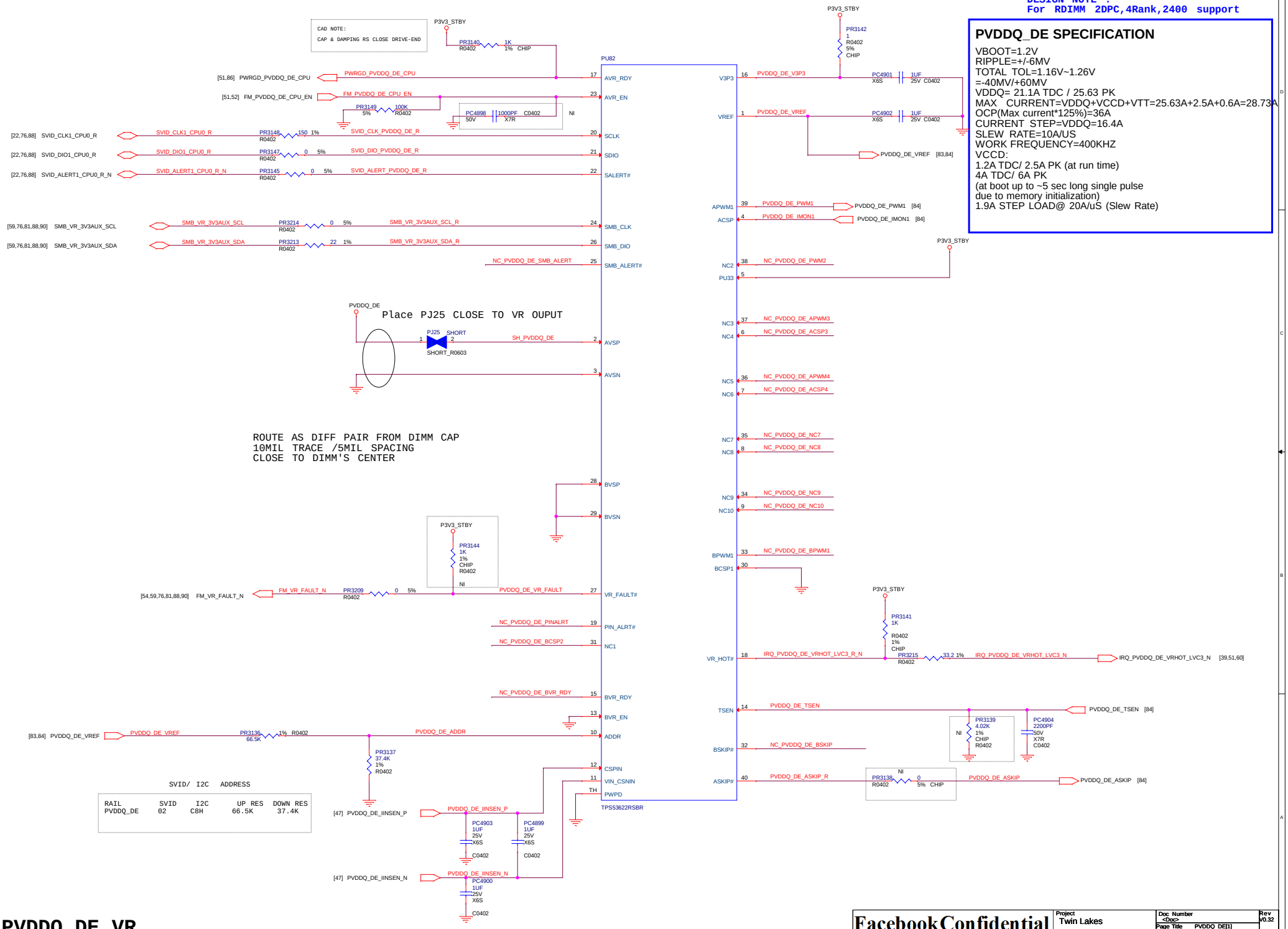
DESIGN NOTE :
For RDIMM 2DPC,4Rank,2400 support
PVDDQ_DE SPECIFICATION
VBOOT=1.2V
RIPPLE=+/-6MV
TOTAL TOL=1.16V~1.26V
=-40MV/+60MV
VDDQ= 21.1A TDC / 25.63 PK
MAX CURRENT=VDDQ+VCCD+VTT=25.63A+2.5A+0.6A=28.73A
OCP(Max current*125%)=36A
CURRENT STEP=VDDQ=16.4A
SLEW RATE=10A/US
WORK FREQUENCY=400KHZ
VCCD:
1.2A TDC/ 2.5A PK (at run time)
4A TDC/ 6A PK
(at boot up to ~5 sec long single pulse
due to memory initialization)
1.9A STEP LOAD@ 20A/uS (Slew Rate)
CAD NOTE:
CAP & DAMPING RS CLOSE DRIVE-END
Place PJ25 CLOSE TO VR OUPUT
ROUTE AS DIFF PAIR FROM DIMM CAP
10MIL TRACE /5MIL SPACING
CLOSE TO DIMM'S CENTER
SVID/ I2C ADDRESS
RAIL SVID I2C UP RES DOWN RES
PVDDQ_DE 02 C8H 66.5K 37.4K
PU82
TPS53622RSBR
PVDDQ_DE
PJ25 SHORT
SHORT_R0603
P3V3_STBY
PVDDQ_DE_VREF
PVDDQ_DE_ADDR
PVDDQ_DE_IINSEN_P
PVDDQ_DE_IINSEN_N
PVDDQ_DE_VR_FAULT
PVDDQ_DE_TSEN
PVDDQ_DE_ASKIP
PVDDQ_DE_PWM1
PVDDQ_DE_IMON1
IRQ_PVDDQ_DE_VRHOT_LVC3_N
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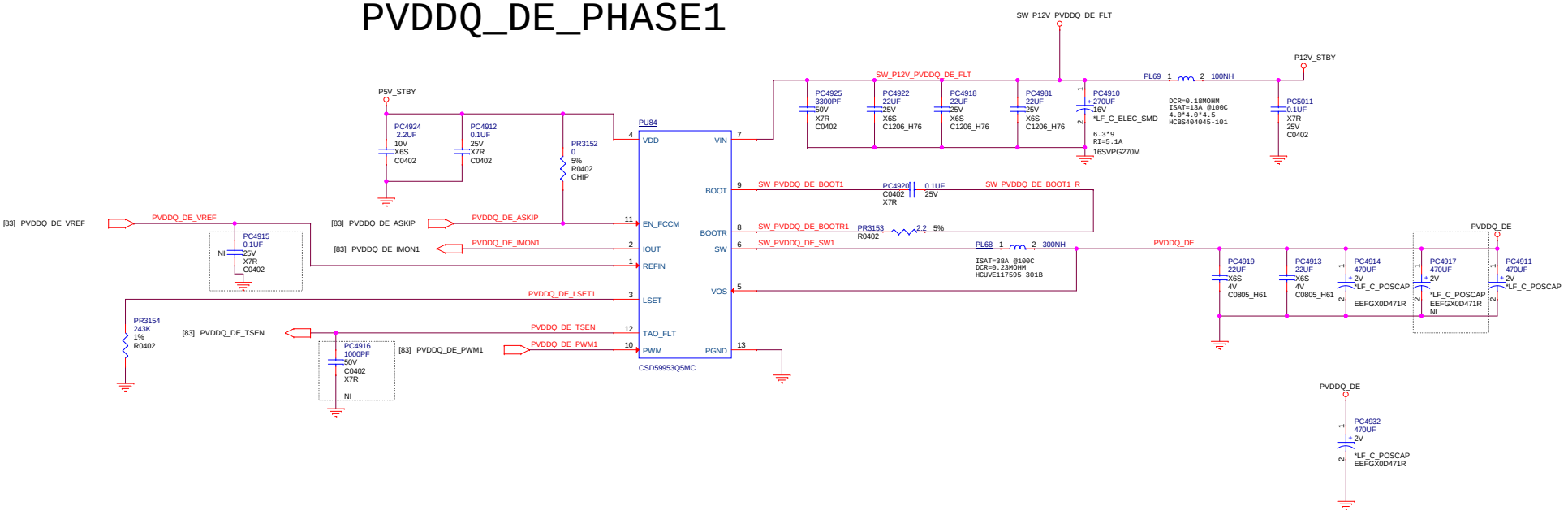
PVDDQ_DE VR

PVDDQ_DE_PHASE1



PVDDQ_DE_PHASE1

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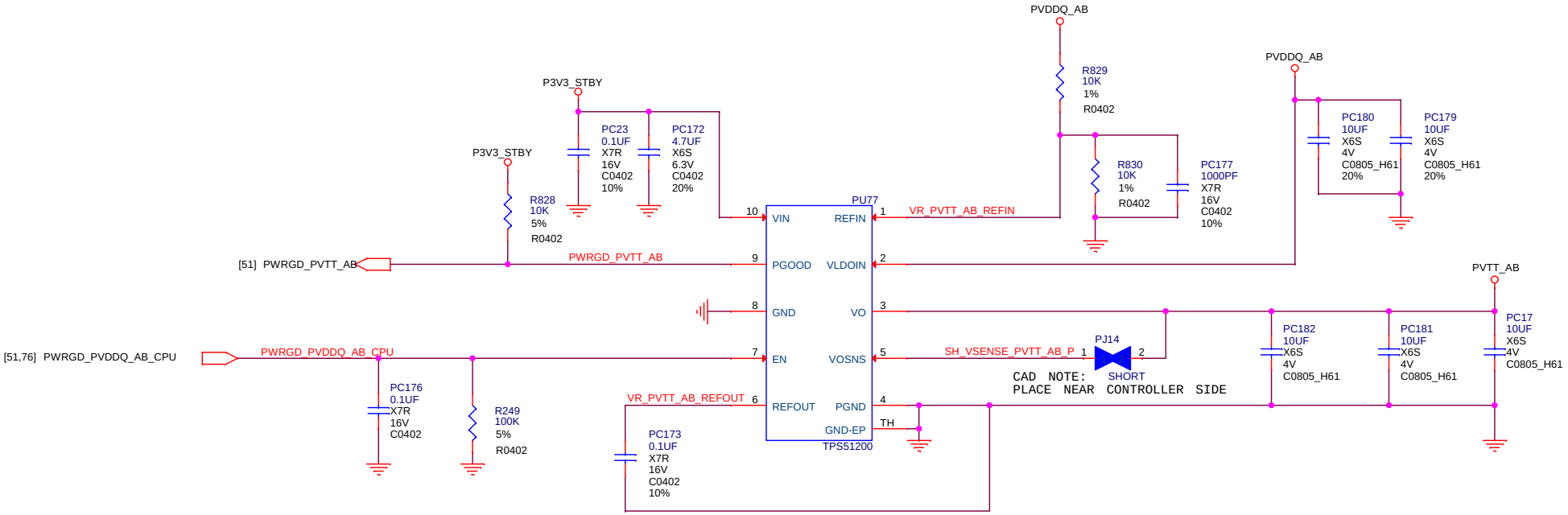
PVTT_AB Design specification

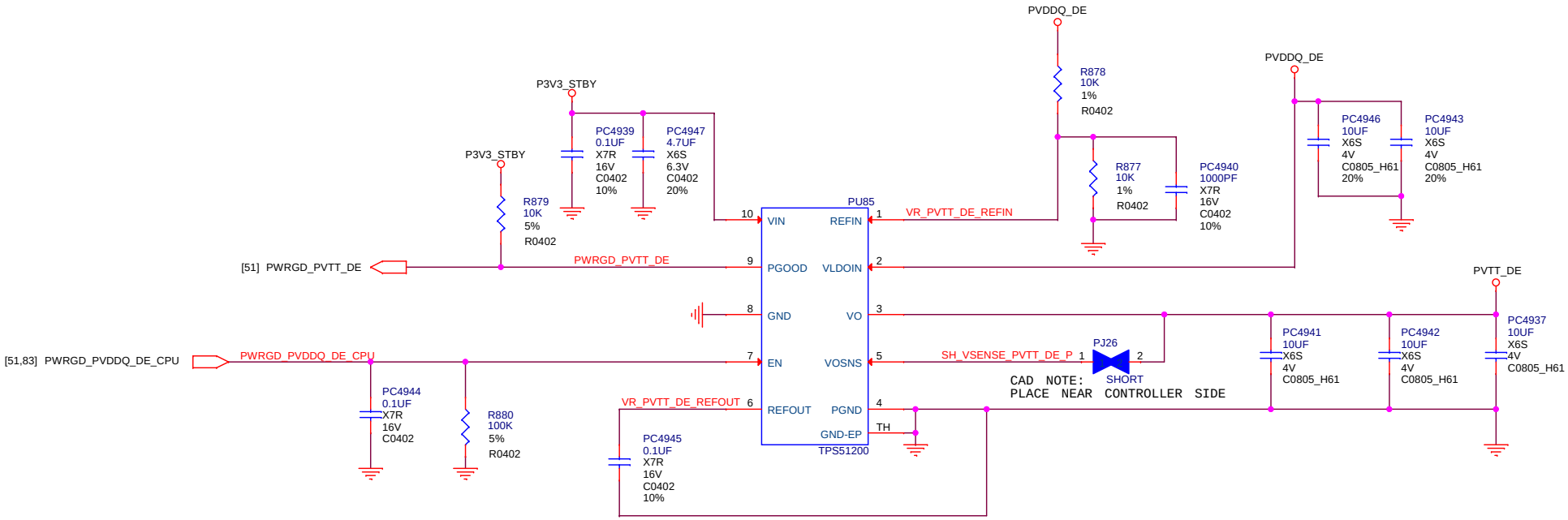
Output Voltage = 0.607V
DC <+/- 6mV
Ripple < +/- 9mV
Total TOL= 0.555V~0.651V
= -52mV/+44mV
TDC = 1.04A
Max current =1.04A
Slew Rate = 4 A/us
Load step (mA to mA) =1.48 A pk
PD = (1.215V -0.6075 V) * 1.04A = 0.63 W



PVTT_AB

PVTT_DE Design specification

Output Voltage = 0.607V
DC <+/- 6mV
Ripple < +/- 9mV
Total TOL= 0.555V~0.651V
= -52mV/+44mV
TDC = 1.04A
Max current =1.04A
Slew Rate = 4 A/us
Load step (mA to mA) =1.48 A pk
PD = (1.215V -0.6075 V) * 1.04A = 0.63 W



PVTT_DE

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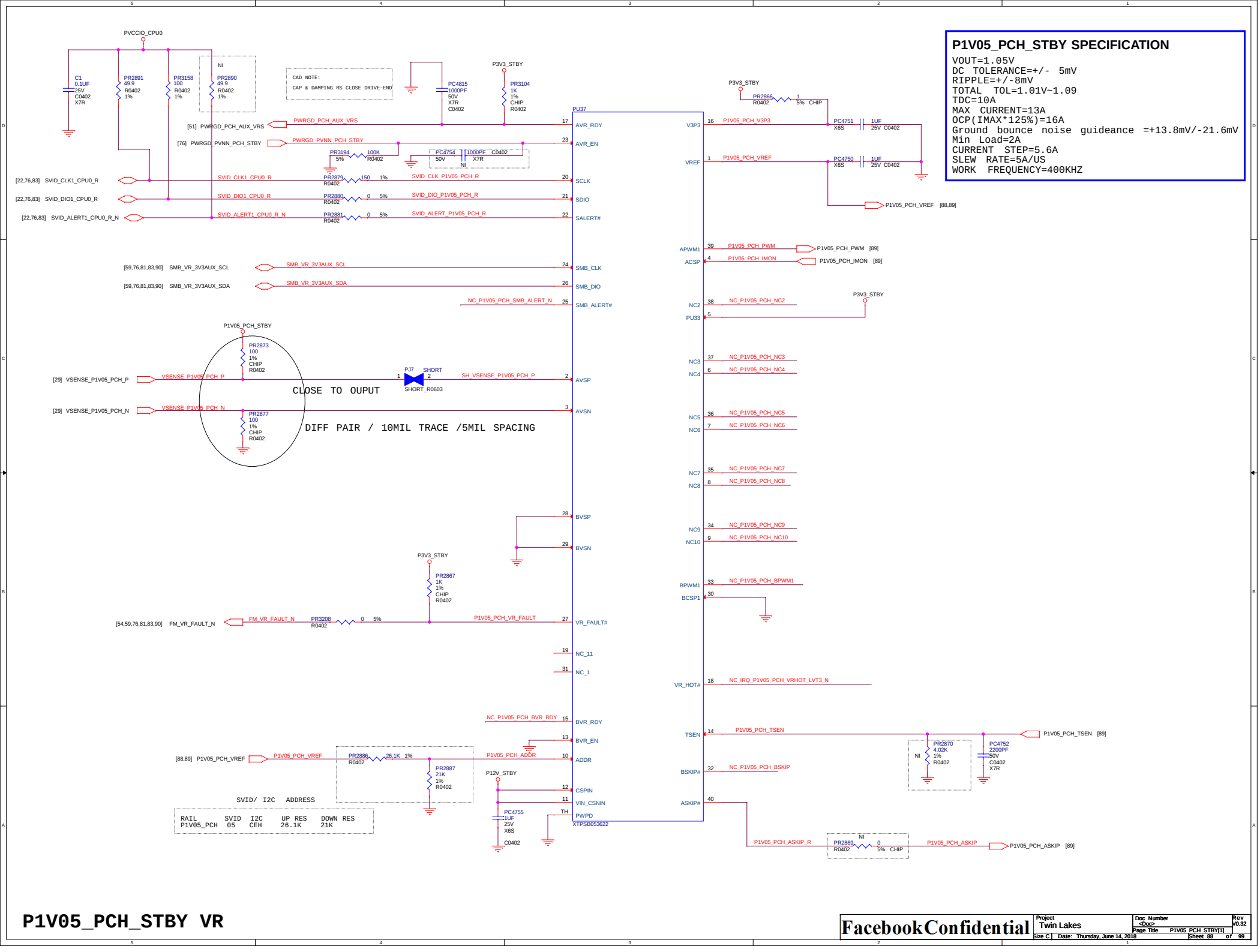
P1V05_PCH_STBY SPECIFICATION
VOUT=1.05V
DC TOLERANCE=+/- 5mV
RIPPLE=+/-8mV
TOTAL TOL=1.01V~1.09
TDC=10A
MAX CURRENT=13A
OCP(IMAX*125%)=16A
Ground bounce noise guideance =+13.8mV/-21.6mV
Min Load=2A
CURRENT STEP=5.6A
SLEW RATE=5A/US
WORK FREQUENCY=400KHZ
PVCCIO_CPU0
P3V3_STBY
PU37
CAD NOTE:
CAP & DAMPING RS CLOSE DRIVE-END
CLOSE TO OUPUT
DIFF PAIR / 10MIL TRACE /5MIL SPACING
SVID/ I2C ADDRESS
RAIL SVID I2C UP RES DOWN RES
P1V05_PCH 05 CEH 26.1K 21K
XTPSB053622
P1V05_PCH_STBY VR
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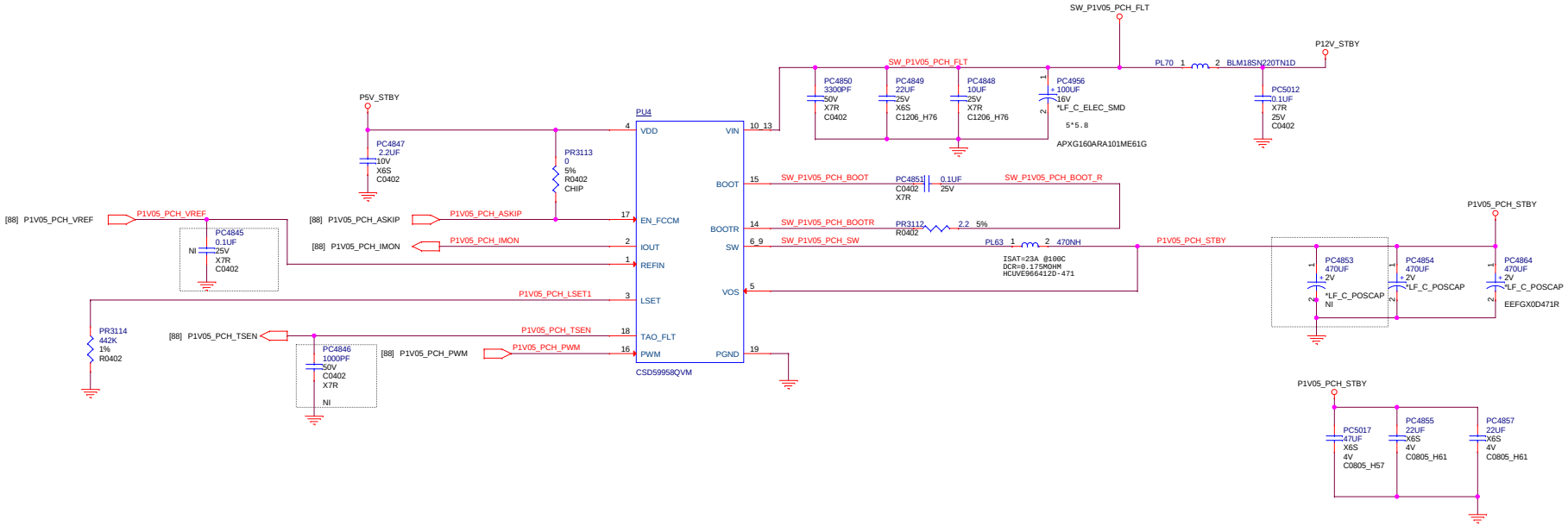
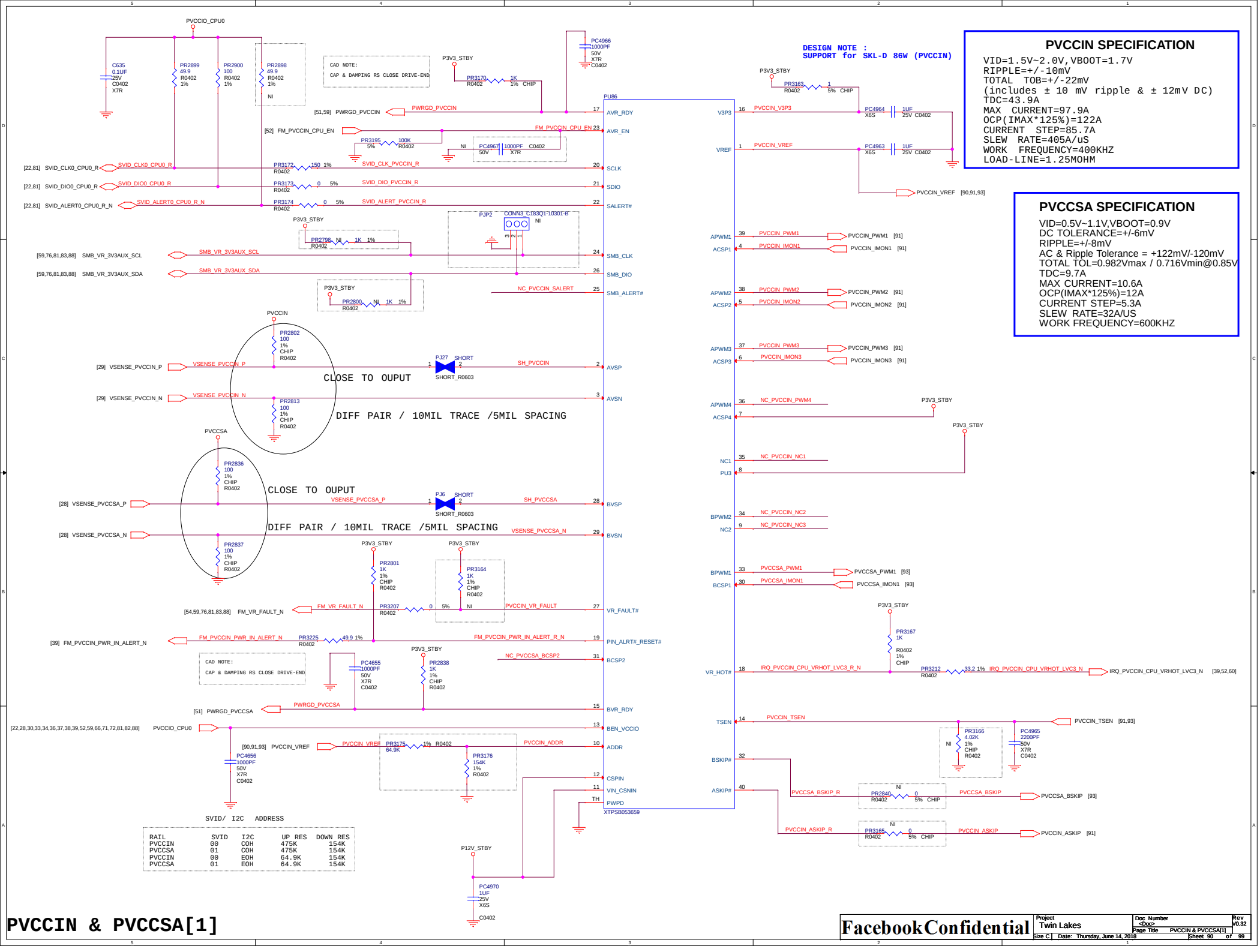
P1V05_PCH_STBY PHASE



Design Note :

If you want to achieve +/- 3mV ripple voltage to meet Intel PDG when use KR interface.
1.PC4853 pop 470uF
2.PC5017,PC4855, PC4857, C702, PC4995, PC4996,C701. PC4997 pop 100uF/0805/X6S''


DESIGN NOTE :
SUPPORT for SKL-D 86W (PVCCIN)
PVCCIN SPECIFICATION
VID=1.5V~2.0V,VBOOT=1.7V
RIPPLE=+/-10mV
TOTAL TOB=+/-22mV
(includes ± 10 mV ripple & ± 12mV DC)
TDC=43.9A
MAX CURRENT=97.9A
OCP(IMAX*125%)=122A
CURRENT STEP=85.7A
SLEW RATE=405A/uS
WORK FREQUENCY=400KHZ
LOAD-LINE=1.25MOHM
PVCCSA SPECIFICATION
VID=0.5V~1.1V,VBOOT=0.9V
DC TOLERANCE=+/-6mV
RIPPLE=+/-8mV
AC & Ripple Tolerance = +122mV/-120mV
TOTAL TOL=0.982Vmax / 0.716Vmin@0.85V
TDC=9.7A
MAX CURRENT=10.6A
OCP(IMAX*125%)=12A
CURRENT STEP=5.3A
SLEW RATE=32A/US
WORK FREQUENCY=600KHZ
CLOSE TO OUPUT
DIFF PAIR / 10MIL TRACE /5MIL SPACING
CLOSE TO OUPUT
DIFF PAIR / 10MIL TRACE /5MIL SPACING
SVID/ I2C ADDRESS
RAIL SVID I2C UP RES DOWN RES
PVCCIN 00 COH 475K 154K
PVCCSA 01 COH 475K 154K
PVCCIN 00 EOH 64.9K 154K
PVCCSA 01 EOH 64.9K 154K
PU86
XTPSB053659
PVCCIO_CPU0
PVCCIN
PVCCSA
P3V3_STBY
P12V_STBY
CAD NOTE:
CAP & DAMPING RS CLOSE DRIVE-END
SHORT_R0603
CONN3_C183Q1-10301-B
PWRGD_PVCCIN
FM_PVCCIN_CPU_EN
SVID_CLK_PVCCIN_R
SVID_DIO_PVCCIN_R
SVID_ALERT_PVCCIN_R
SMB_VR_3V3AUX_SCL
SMB_VR_3V3AUX_SDA
NC_PVCCIN_SALERT
VSENSE_PVCCIN_P
VSENSE_PVCCIN_N
SH_PVCCIN
VSENSE_PVCCSA_P
VSENSE_PVCCSA_N
SH_PVCCSA
FM_VR_FAULT_N
PVCCIN_VR_FAULT
FM_PVCCIN_PWR_IN_ALERT_N
FM_PVCCIN_PWR_IN_ALERT_R_N
NC_PVCCSA_BCSP2
PWRGD_PVCCSA
PVCCIN_ADDR
PVCCIN_V3P3
PVCCIN_VREF
PVCCIN_PWM1
PVCCIN_IMON1
PVCCIN_PWM2
PVCCIN_IMON2
PVCCIN_PWM3
PVCCIN_IMON3
NC_PVCCIN_PWM4
NC_PVCCIN_NC1
NC_PVCCIN_NC2
NC_PVCCIN_NC3
PVCCSA_PWM1
PVCCSA_IMON1
IRQ_PVCCIN_CPU_VRHOT_LVC3_R_N
IRQ_PVCCIN_CPU_VRHOT_LVC3_N
PVCCIN_TSEN
PVCCSA_BSKIP_R
PVCCSA_BSKIP
PVCCIN_ASKIP_R
PVCCIN_ASKIP
C635 0.1UF 25V C0402 X7R
PR2899 49.9 R0402 1%
PR2900 100 R0402 1%
PR2898 49.9 R0402 1% NI
PC4966 1000PF 50V X7R C0402
PR3170 1K R0402 1% CHIP
PR3195 100K 5% R0402
PC4967 1000PF 50V X7R C0402 NI
PR3172 150 1% R0402
PR3173 0 5% R0402
PR3174 0 5% R0402
PR2798 NI 1K 1% R0402
PR2800 NI 1K 1% R0402
PR2802 100 1% CHIP R0402
PR2813 100 1% CHIP R0402
PR2836 100 1% CHIP R0402
PR2837 100 1% CHIP R0402
PR2801 1K 1% CHIP R0402
PR3164 1K 1% CHIP R0402
PR3207 0 5% R0402 NI
PR3225 49.9 1% R0402
PC4655 1000PF 50V X7R C0402
PR2838 1K 1% CHIP R0402
PC4656 1000PF 50V X7R C0402
PR3175 64.9K 1% R0402
PR3176 154K 1% R0402
PC4970 1UF 25V X6S C0402
PR3163 1 5% CHIP R0402
PC4964 1UF 25V X6S C0402
PC4963 1UF 25V X6S C0402
PR3167 1K R0402 1% CHIP
PR3212 33.2 1% R0402
PR3166 4.02K 1% CHIP R0402 NI
PC4965 2200PF 50V X7R C0402
PR2840 0 5% R0402 NI CHIP
PR3165 0 5% R0402 NI CHIP
PJP2
PJ27 SHORT
PJ6 SHORT
[22,81] SVID_CLK0_CPU0_R
[22,81] SVID_DIO0_CPU0_R
[22,81] SVID_ALERT0_CPU0_R_N
[59,76,81,83,88] SMB_VR_3V3AUX_SCL
[59,76,81,83,88] SMB_VR_3V3AUX_SDA
[29] VSENSE_PVCCIN_P
[29] VSENSE_PVCCIN_N
[28] VSENSE_PVCCSA_P
[28] VSENSE_PVCCSA_N
[54,59,76,81,83,88] FM_VR_FAULT_N
[39] FM_PVCCIN_PWR_IN_ALERT_N
[51] PWRGD_PVCCSA
[22,28,30,33,34,36,37,38,39,52,59,66,71,72,81,82,88] PVCCIO_CPU0
[90,91,93] PVCCIN_VREF
[52] FM_PVCCIN_CPU_EN
[51,59] PWRGD_PVCCIN
[91,93] PVCCIN_TSEN
[93] PVCCSA_BSKIP
[91] PVCCIN_ASKIP
[39,52,60] IRQ_PVCCIN_CPU_VRHOT_LVC3_N
[90,91,93] PVCCIN_VREF
[91] PVCCIN_PWM1
[91] PVCCIN_IMON1
[91] PVCCIN_PWM2
[91] PVCCIN_IMON2
[91] PVCCIN_PWM3
[91] PVCCIN_IMON3
[93] PVCCSA_PWM1
[93] PVCCSA_IMON1
SCLK
SDIO
SALERT#
SMB_CLK
SMB_DIO
SMB_ALERT#
AVSP
AVSN
BVSP
BVSN
VR_FAULT#
PIN_ALRT#_RESET#
BCSP2
BVR_RDY
BEN_VCCIO
ADDR
CSPIN
VIN_CSNIN
PWPD
AVR_RDY
AVR_EN
V3P3
VREF
APWM1
ACSP1
APWM2
ACSP2
APWM3
ACSP3
APWM4
ACSP4
NC1
PU3
BPWM2
NC2
BPWM1
BCSP1
VR_HOT#
TSEN
BSKIP#
ASKIP#
TH
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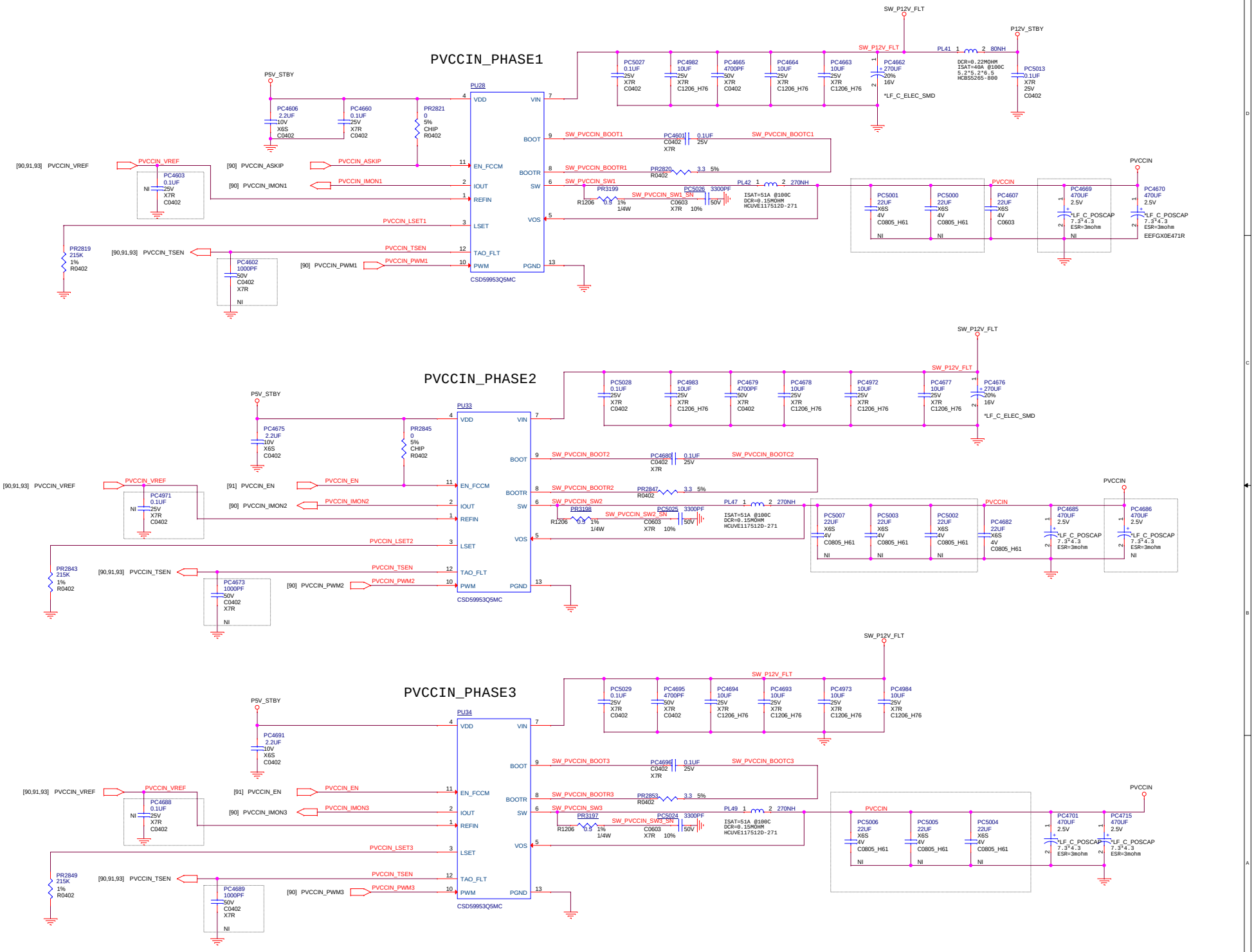
PVCCIN & PVCCSA[1]



PVCCIN & PVCCSA[2]

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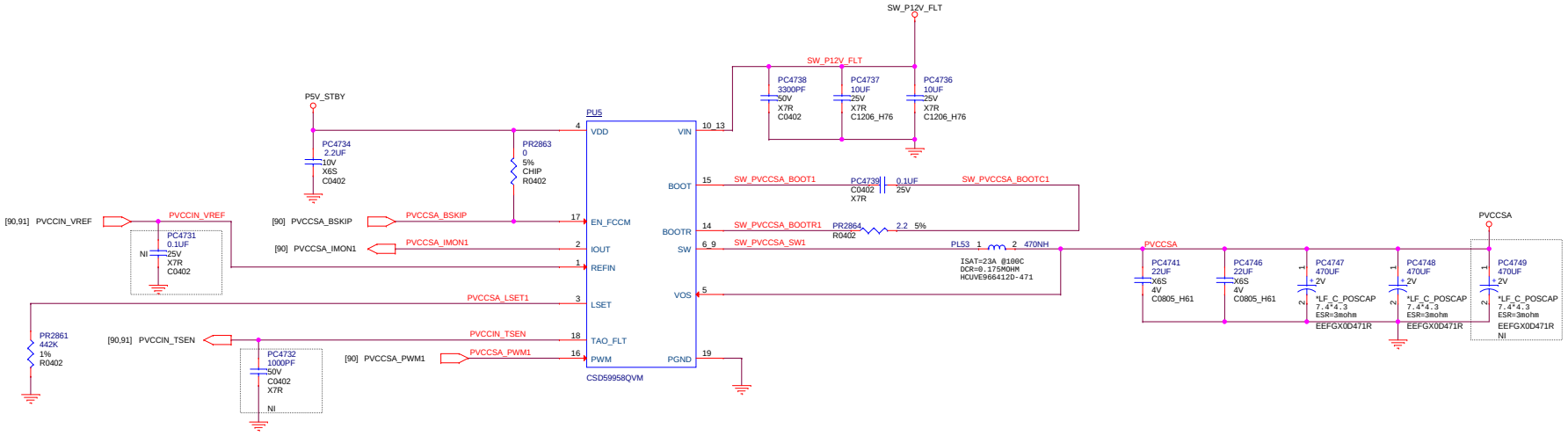
PVCCSA PHASE



PVCCIN & PVCCSA[4]

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		Page Title: PVCCIN & PVCCSA[4]	
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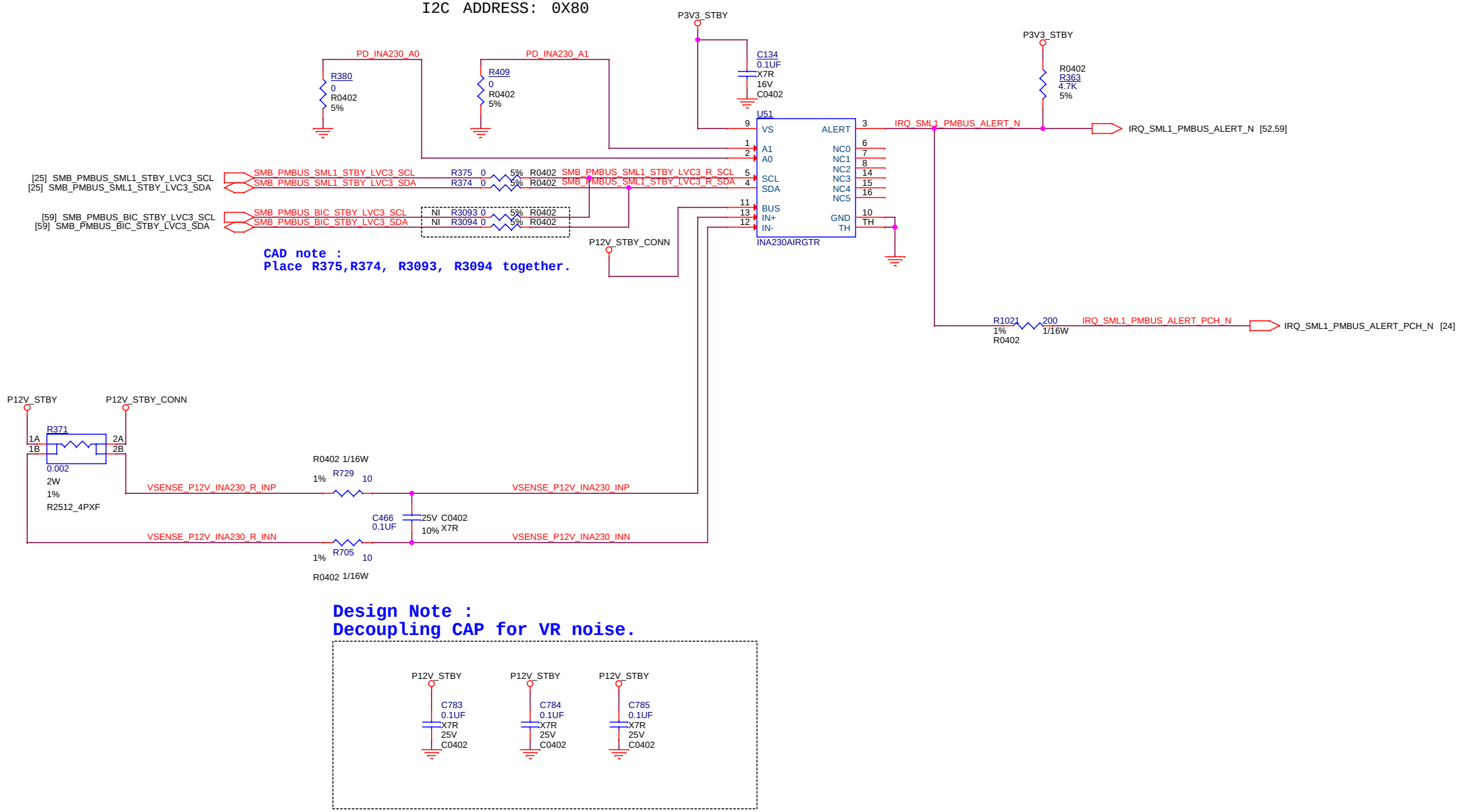

Power sensing INA230

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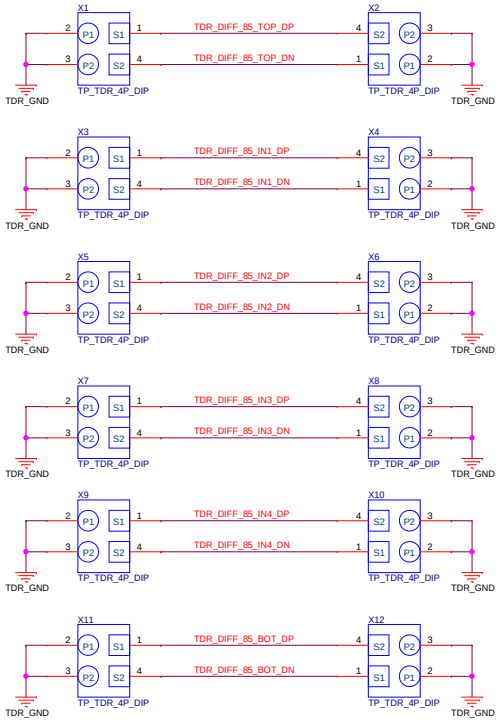
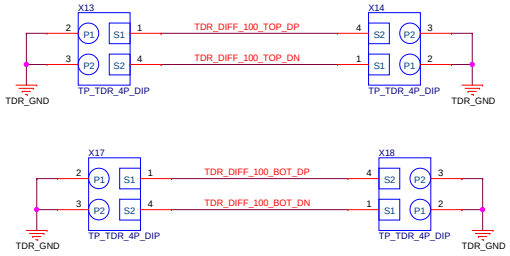
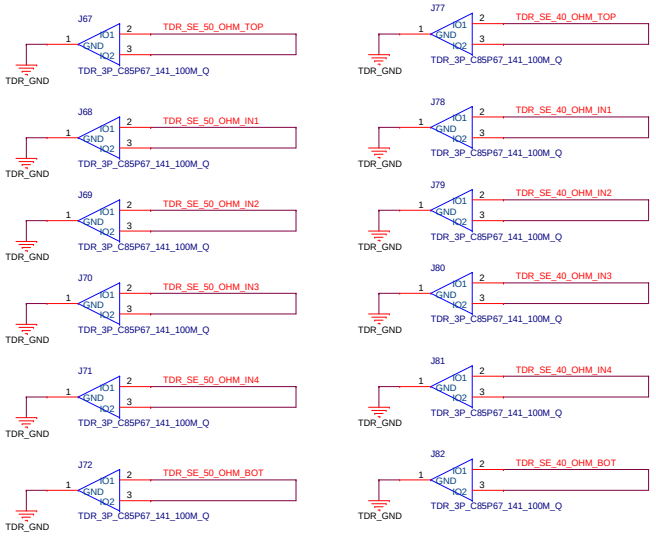
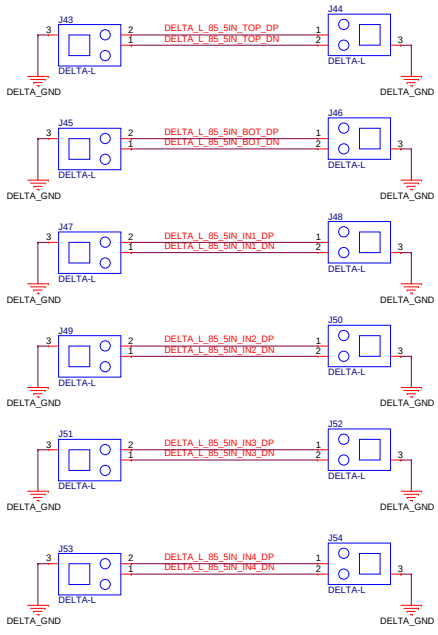






5 INCH



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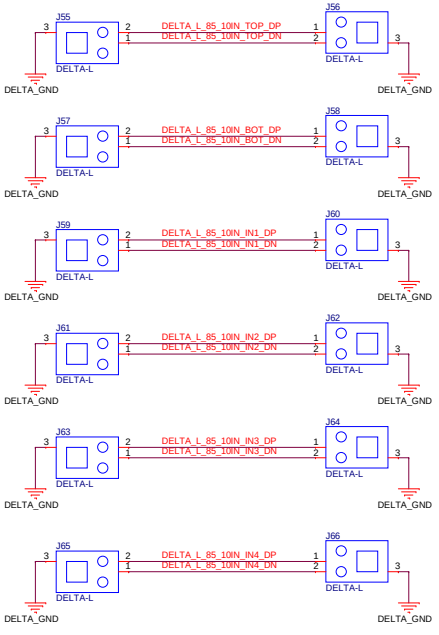

DELTA-L/TDR

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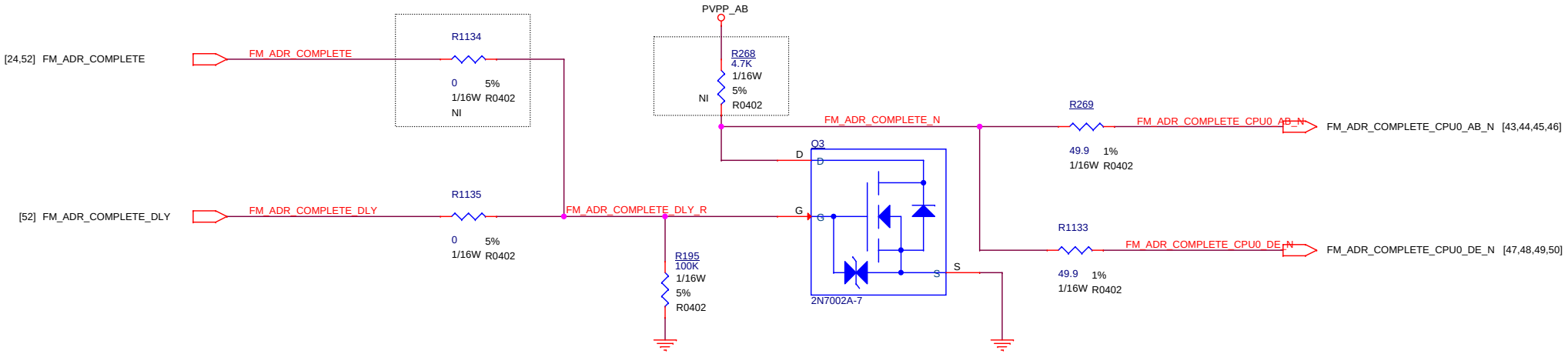

ADR FUNCTION

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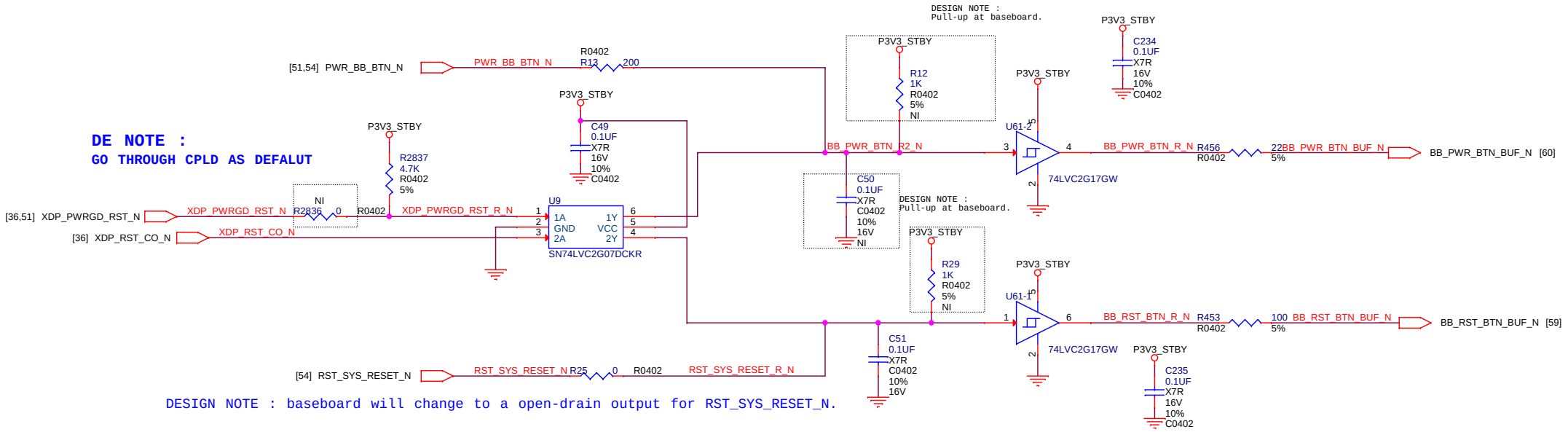
DESIGN NOTE : baseboard will change to a open-drain output for PWR_BB_BTN_N.



DESIGN NOTE : baseboard will change to a open-drain output for RST_SYS_RESET_N.

PWR/RST BTN LOGIC

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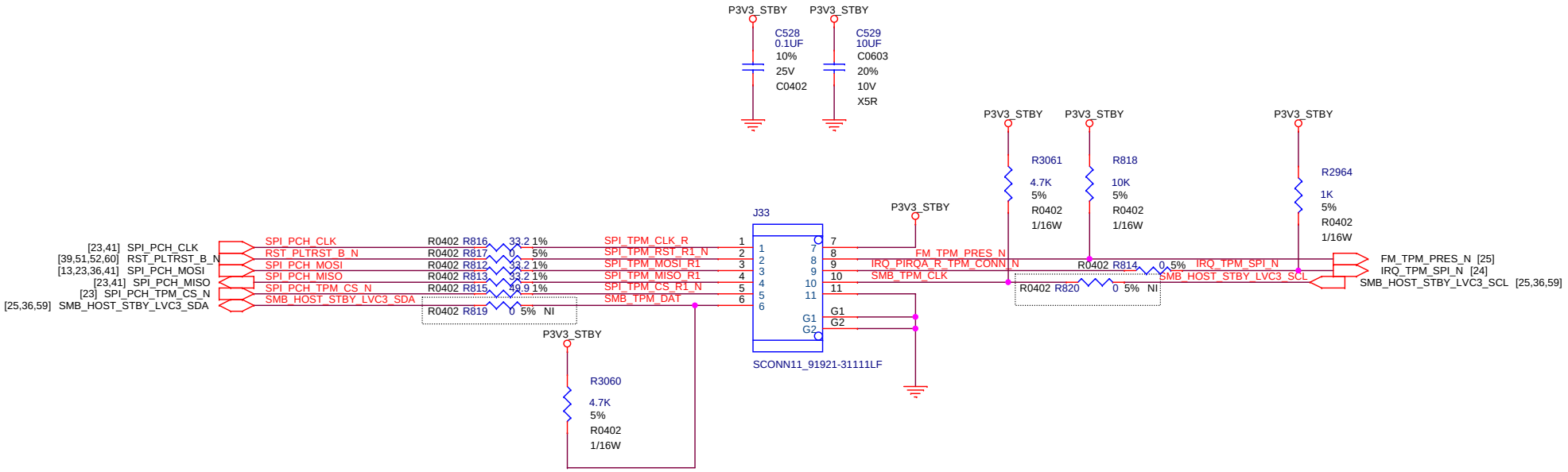

TPM

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DM1 DUMMY_SYMBOL QUANTA_LOGO_7X26

DM2 DUMMY_SYMBOL WEEE

DM3 DUMMY_SYMBOL PB-E1_SMALL

DM4 DUMMY_SYMBOL BARCODE

DM5 DUMMY_SYMBOL PCBA_LABEL_15X5

TP TP_M2_LATCH

TP TP_HEAT_SINK1

TP TP_CPU_BACKPLANE

TP TP_TPM_SCREW

TP TP_TPM_NUT

TP TP_BATTERY_CABLE

TP TP_BIOS_LABEL

TP TP_EJECTOR_1

TP TP_EJECTOR_2

TP TP_M2_LATCH1

TP TP_M2_LATCH2

TP TP_JUMPER_1

TP TP_JUMPER_2

TP TP_JUMPER_5

TP TP_JUMPER_4

Mech Hole

RADIATOR HOLE

H15

HOLE_C11D5-5B9I7_NPM_RB

For TPM module

H7

HOLE_C6D3-4B6_NPB

Boot drive M2 LATCH HOLE

H16

HOLE_D2-6N_RB

H17

HOLE_OBD3-2X4-8N

ICT Positioning HOLE

H19

D2-54N

Ejector Hole

H8

HOLE3_C13D3-7B13N_P4-5_NPM

H10

HOLE3_C13D3-7B13N_P4-5_NPM

PC5031 1000PF

TP_PC177_L — TP_PC177_R

C0402 X7R 16V 10%

TP_PR2903_L — PR3217 2.2 5% — TP_PR2903_R

R0402

TP_PR2886_L — PR3218 26.1K 1% — TP_PR2886_R

R0402

TP_PR59_L — PR3219 54.9K 1% — TP_PR59_R

R0402

TP_PR2805_L — PR3220 86.6K 1% — TP_PR2805_R

R0402

TP_PR3083_L — PR3221 121K 1% — TP_PR3083_R

R0402

TP_R351_L — R3131 200K 1% — TP_R351_R

R0402

TP_PR3114_L — PR3222 442K 1% — TP_PR3114_R

R0402

H20

HOLE_D2-15N_RB

H21

HOLE_D2-15N_RB

H22

HOLE_D2-15N_RB

CPU HS GRIP

DESIGN NOTE :
Will change to diameter 6.7 mm hole.

H6

HOLE_D6-7N

H5

HOLE_D6-7N

H4

HOLE_D6-7N

H3

HOLE_D6-7N

TP

M2 LATCH HOLE

H11

HOLE_OBD3-2X4-8N

H12

HOLE_OBD3-2X4-8N

H13

HOLE_OBD3-2X4-8N

H14

HOLE_OBD3-2X4-8N

SCREW/TP

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