Yosemite V2
BASEBOARD

<Variant Name>

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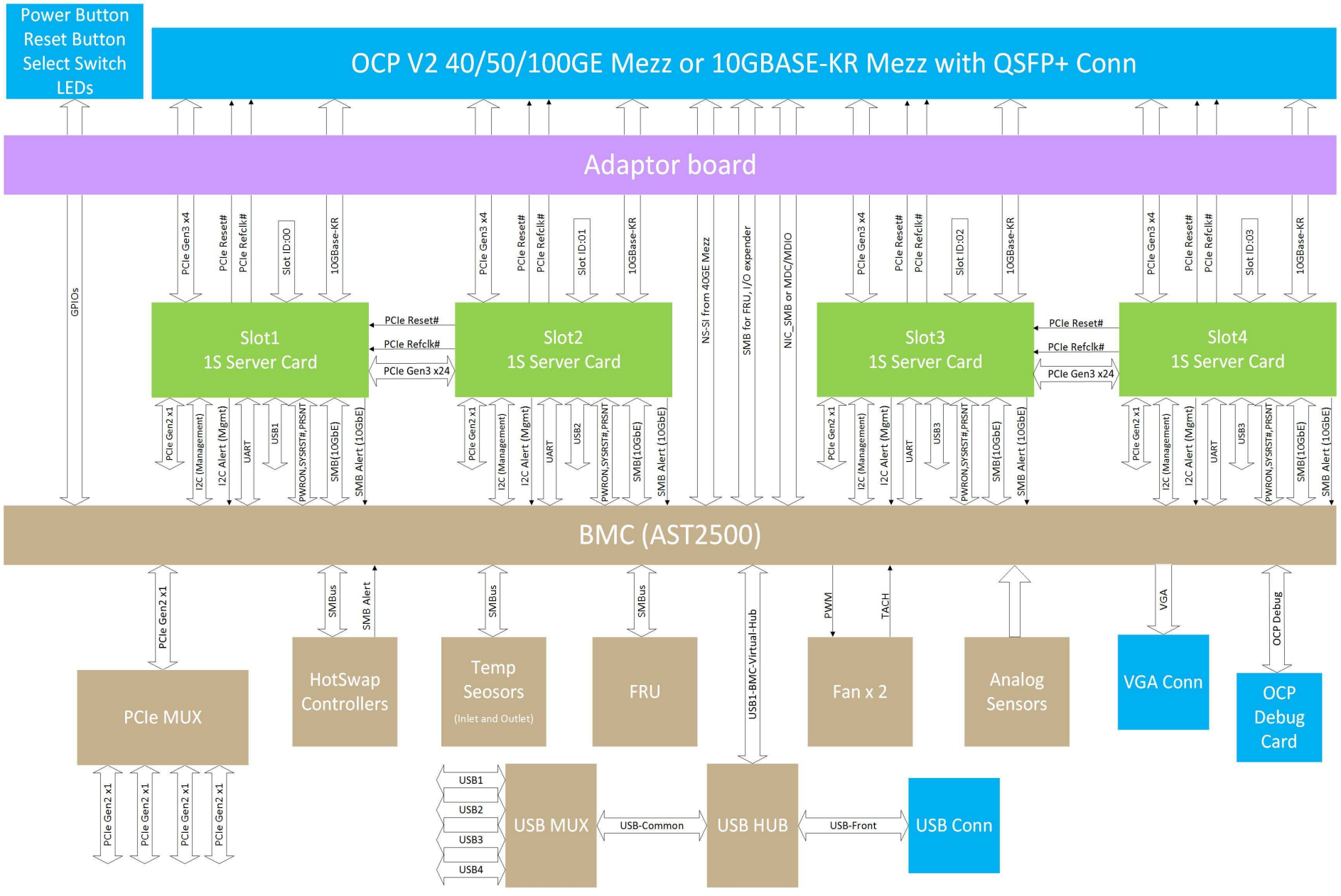
Yosemite V2 Block Diagram V0.03



Board Block Diagram

<Variant Name>

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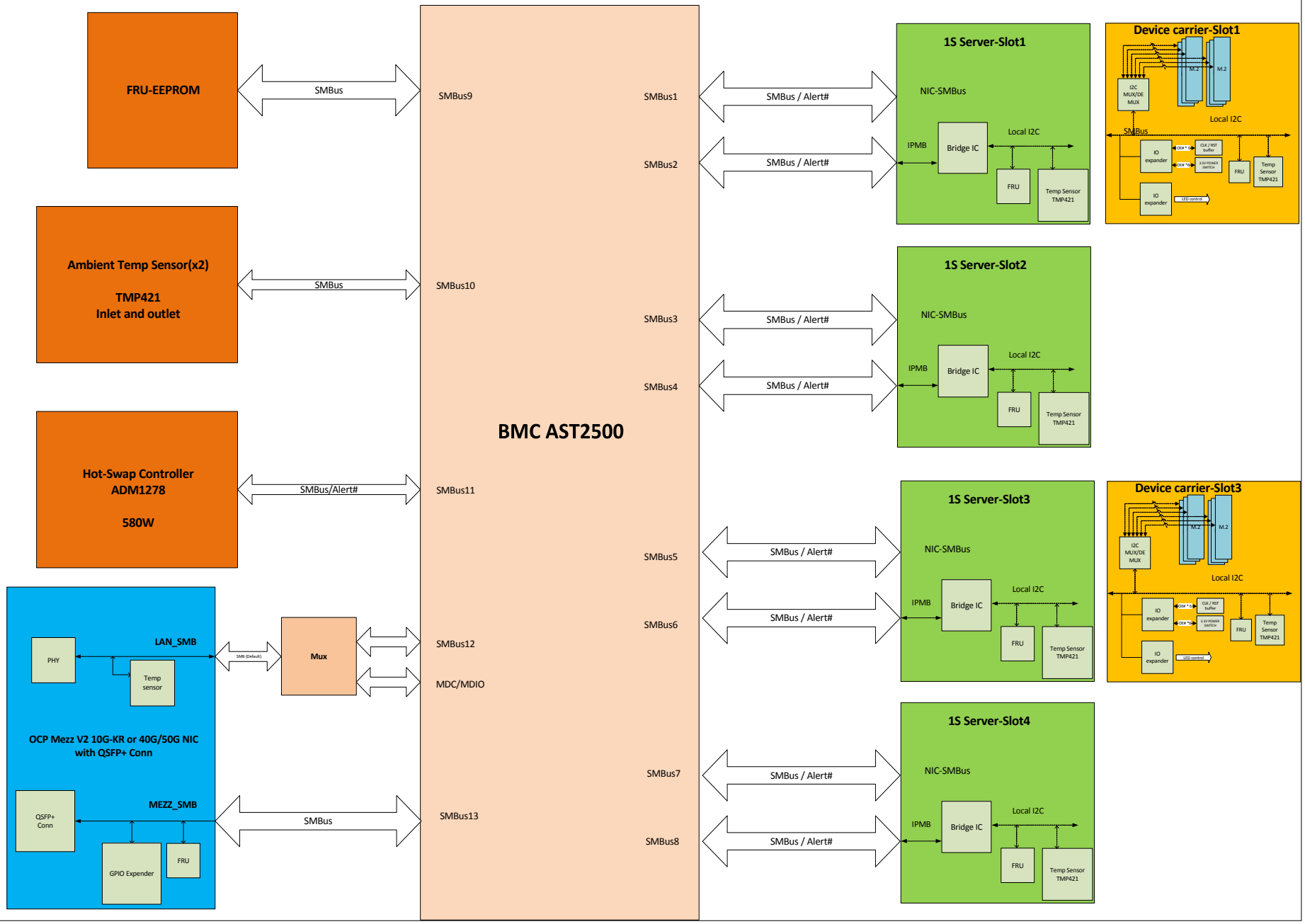
Yosemite V2 SMB Diagram V0.02



SMBus Block Diagram

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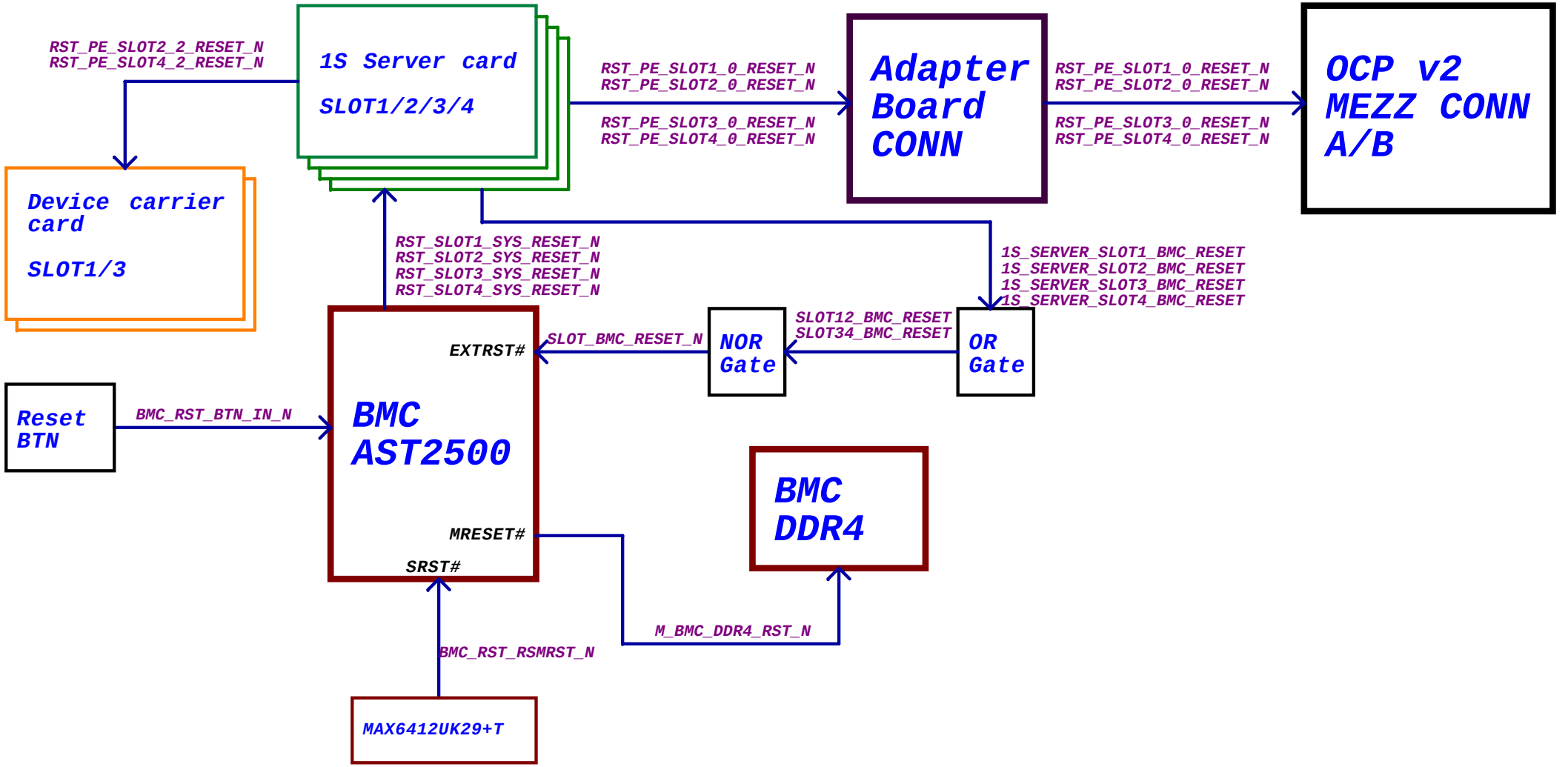
Reset Block Diagram V.03



Reset Block Diagram

<Variant Name>

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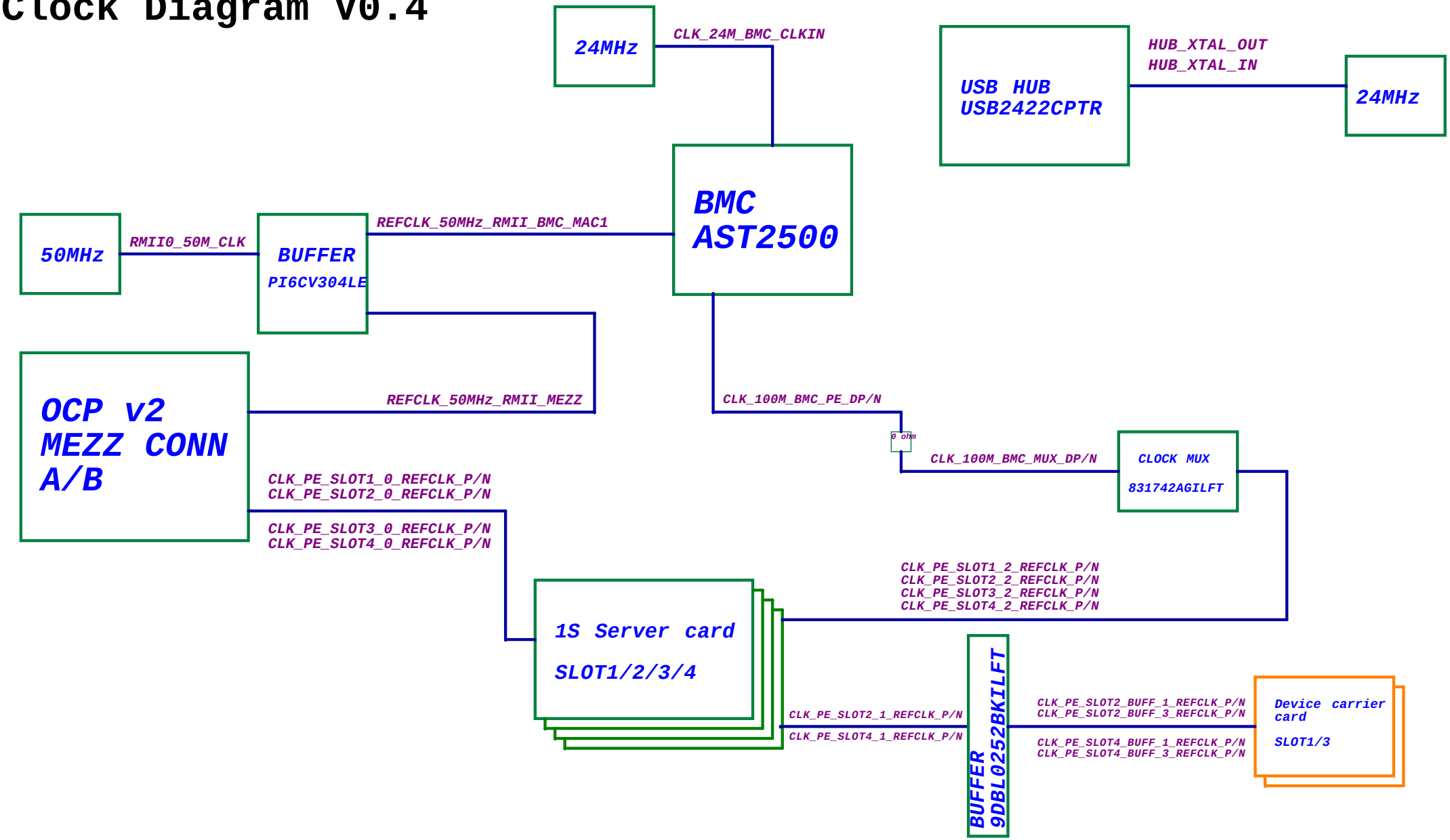
Clock Diagram V0.4



Clock Block Diagram

<Variant Name>

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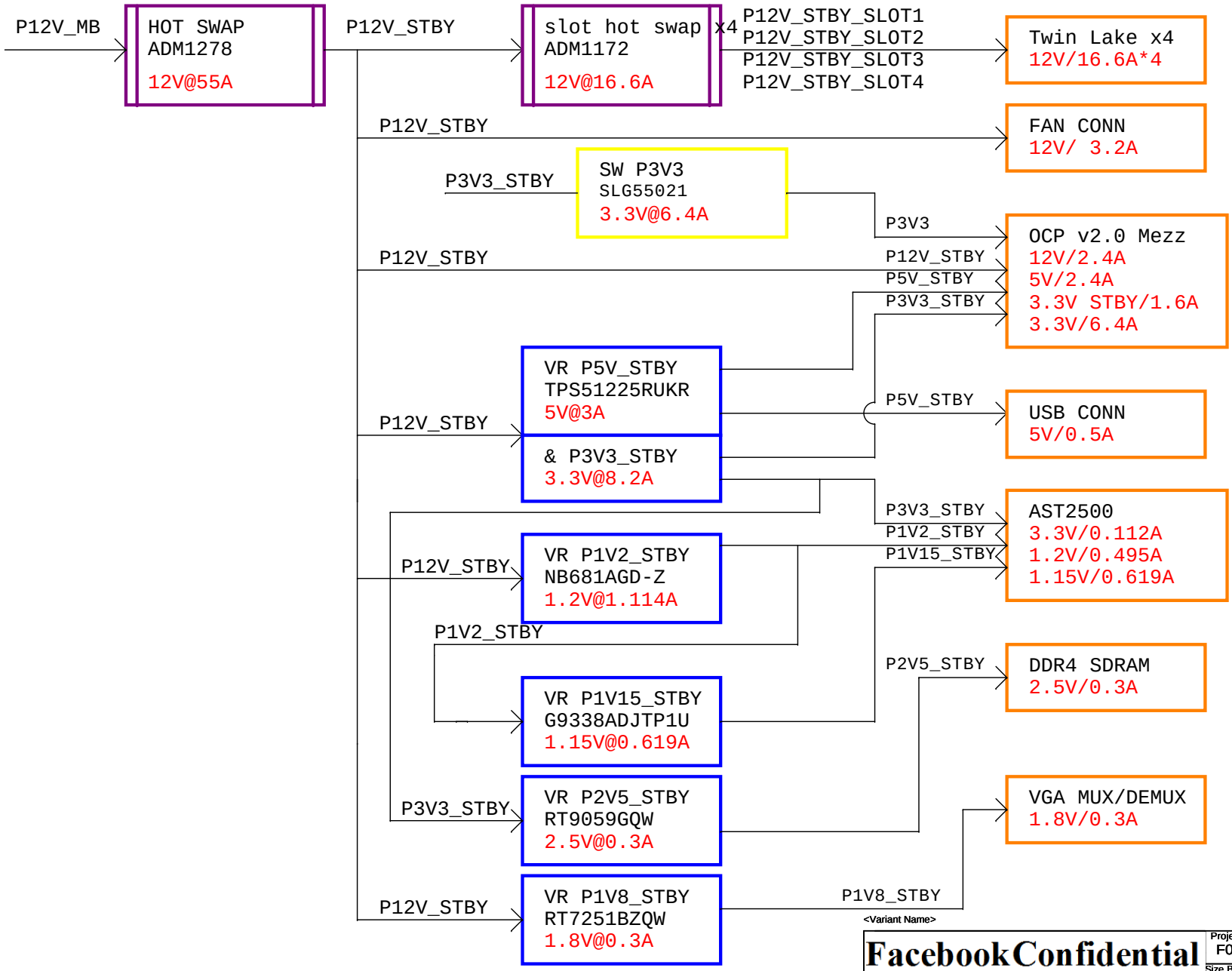
Power Block Diagram V0.2



Power rail	COND1	
(units: mA)	mean	max
Core 1.15V power	495	619
DDR3 1.35V power *(Include DRAM)*	394	501
DDR4 1.20V power *(Include DRAM)*	395	495
3.3V power *PV33D/LPVDD*	20	21
3.3V power *R1VDD/R2VDD*	16	17
3.3V power *PLLAV33/MPLLAV33*	6	7
3.3V power *VPLLAV33*	2	3
3.3V power *ADCAV33*	2	3
3.3V power *DACAV33/DACDV33*	60	61
Chip total power *(DDR3, Watt)*	1.46	1.76
Chip total power *(DDR4, Watt)*	1.40	1.68

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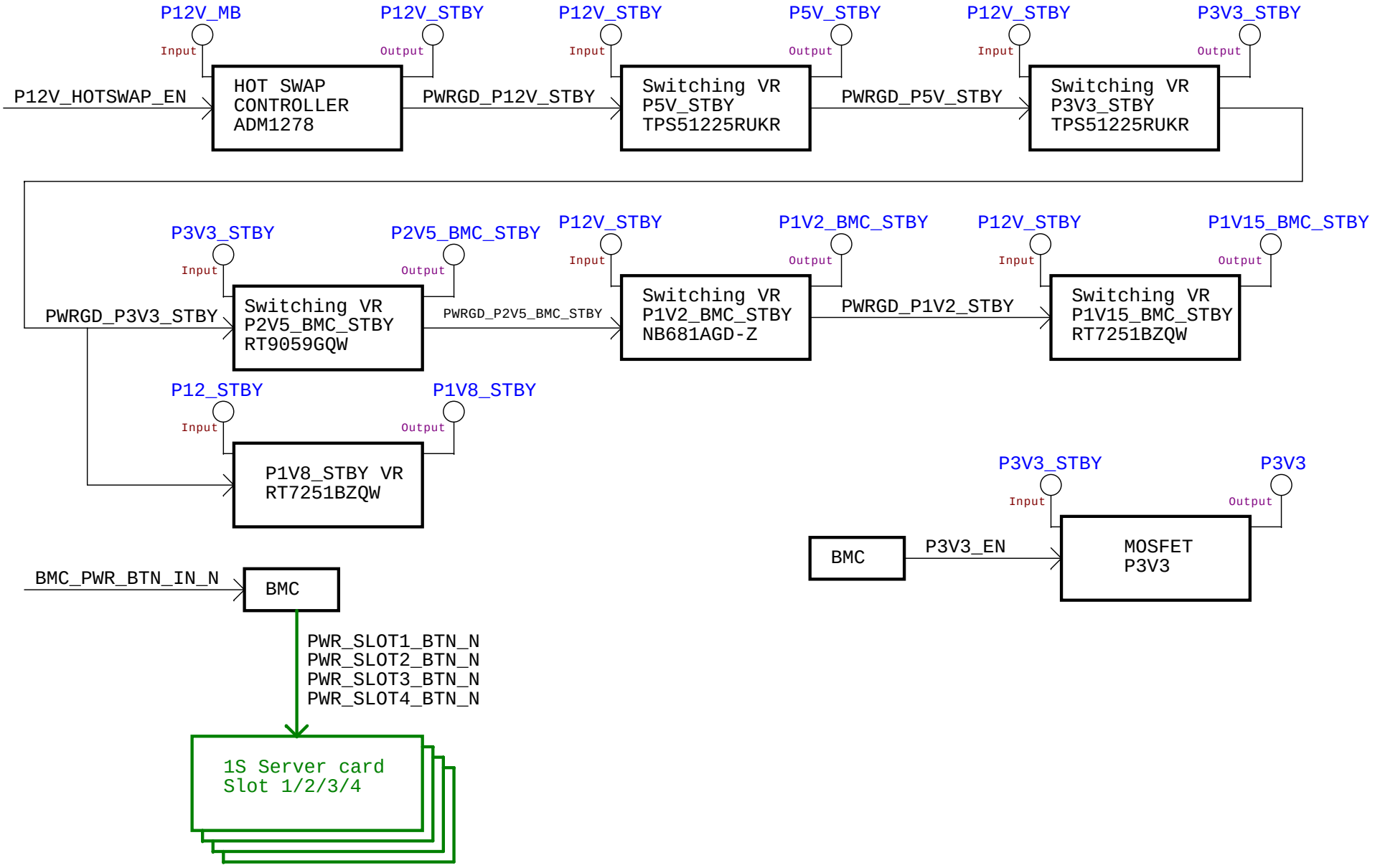
Power Sequence SYSTEM V0.5



Power Sequence SYSTEM

<Variant Name>

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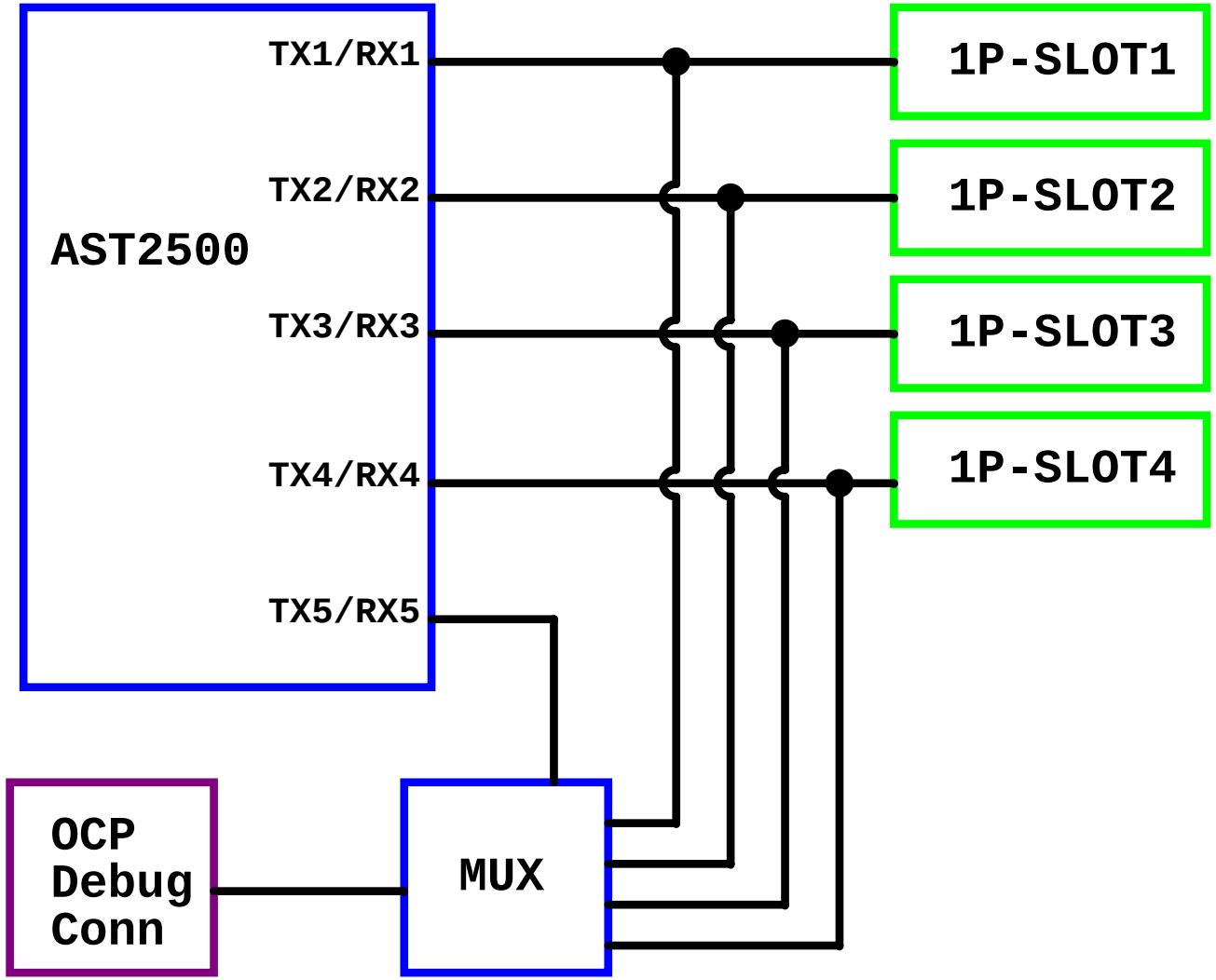
UART Topology v0.2



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J35 Rev13

	10	9	8	7	6	5	4	3	2	1	
M	No Pin		No Pin		No Pin		No Pin		No Pin		M
L	PE_SLOT1_0_RX3_N	GND	PE_SLOT1_0_RX1_N	GND	KR_SLOT1_RX0_N	GND	PE_SLOT3_0_TX2_N	GND	PE_SLOT3_0_TX0_N	GND	L
K	PE_SLOT1_0_RX3_P	PE_SLOT1_0_TX2_N	PE_SLOT1_0_RX1_P	PE_SLOT1_0_TX0_N	KR_SLOT1_RX0_P	PE_SLOT3_0_TX3_N	PE_SLOT3_0_TX2_P	PE_SLOT3_0_TX1_N	PE_SLOT3_0_TX0_P	KR_SLOT3_TX0_N	K
J	GND	PE_SLOT1_0_TX2_P	GND	PE_SLOT1_0_TX0_P	GND	PE_SLOT3_0_TX3_P	GND	PE_SLOT3_0_TX1_P	GND	KR_SLOT3_TX0_P	J
I	PE_SLOT1_0_TX3_N	GND	PE_SLOT1_0_TX1_N	GND	KR_SLOT1_TX0_P	GND	PE_SLOT3_0_RX2_N	GND	PE_SLOT3_0_RX0_N	GND	I
H	PE_SLOT1_0_TX3_P	PE_SLOT1_0_RX2_N	PE_SLOT1_0_TX1_P	PE_SLOT1_0_RX0_N	KR_SLOT1_TX0_N	PE_SLOT3_0_RX3_N	PE_SLOT3_0_RX2_P	PE_SLOT3_0_RX1_N	PE_SLOT3_0_RX0_P	KR_SLOT3_RX0_N	H
G	GND	PE_SLOT1_0_RX2_P	GND	PE_SLOT1_0_RX0_P	GND	PE_SLOT3_0_RX3_P	GND	PE_SLOT3_0_RX1_P	GND	KR_SLOT3_RX0_P	G
F	P12V_STBY	GND	MEZZ_PRSNTID_A_SEL_N	GND	SMB_MEZZ_NIC_DAT_MDIO	GND	CLK_PE_SLOT1_0_REFCLK_P	GND	BMC_NCSI_RMII_TXD_1	GND	F
E	P12V_STBY	P12V_STBY	MEZZ_PRSNTID_B_SEL_N	MEZZ_PRSNTA2_N	SMB_MEZZ_NIC_CLK_MDC	SMB_MEZZ_SMDATA	CLK_PE_SLOT1_0_REFCLK_N	CLK_PE_SLOT3_0_REFCLK_P	BMC_NCSI_RMII_TXD_0	BMC_NCSI_RMII_RXD_1_R	E
D	GND	P12V_STBY	GND	MEZZ_PRSNTB2_N	GND	SMB_MEZZ_SMCLK	GND	CLK_PE_SLOT3_0_REFCLK_N	GND	BMC_NCSI_RMII_RXD_0_R	D
C	P12V_STBY	GND	P3V3_STBY	GND	LAN_3V3STB_ALERT_N	GND	DEBUG_RST_BTN_N	GND	BMC_NCSI_RMII_TX_EN	GND	C
B	P12V_STBY	P12V_STBY	P3V3_STBY	P3V3_STBY	PCIE_WAKE_N	RST_N3_N	FM_UART_SWITCH_N	DEBUG_PORT_V1_UART_TX	REFCLK_50MHz_RMII_MEZZ	BMC_NCSI_RMII_CSR_DV_R	B
A	GND	P12V_STBY	GND	P3V3_STBY	GND	RST_N1_N	GND	DEBUG_PORT_V1_UART_5V_RX	GND	BMC_NCSI_RMII_RX_ER_R	A
	10	9	8	7	6	5	4	3	2	1	

J38 Rev13

	10	9	8	7	6	5	4	3	2	1	
M	No Pin		No Pin		No Pin		No Pin		No Pin		M
L	PE_SLOT2_0_TX3_P	GND	PE_SLOT2_0_TX1_P	GND	KR_SLOT2_TX0_N	GND	PE_SLOT4_0_TX2_P	GND	PE_SLOT4_0_RX0_P	GND	L
K	PE_SLOT2_0_TX3_N	PE_SLOT2_0_TX2_P	PE_SLOT2_0_TX1_N	PE_SLOT2_0_TX0_P	KR_SLOT2_TX0_P	PE_SLOT4_0_TX3_P	PE_SLOT4_0_TX2_N	PE_SLOT4_0_RX1_P	PE_SLOT4_0_RX0_N	KR_SLOT4_RX0_P	K
J	GND	PE_SLOT2_0_TX2_N	GND	PE_SLOT2_0_TX0_N	GND	PE_SLOT4_0_TX3_N	GND	PE_SLOT4_0_RX1_N	GND	KR_SLOT4_RX0_N	J
I	PE_SLOT2_0_RX3_P	GND	PE_SLOT2_0_RX1_P	GND	KR_SLOT2_RX0_N	GND	PE_SLOT4_0_RX2_P	GND	PE_SLOT4_0_TX0_P	GND	I
H	PE_SLOT2_0_RX3_N	PE_SLOT2_0_RX2_P	PE_SLOT2_0_RX1_N	PE_SLOT2_0_RX0_P	KR_SLOT2_RX0_P	PE_SLOT4_0_RX3_P	PE_SLOT4_0_RX2_N	PE_SLOT4_0_TX1_P	PE_SLOT4_0_TX0_N	KR_SLOT4_TX0_P	H
G	GND	PE_SLOT2_0_RX2_N	GND	PE_SLOT2_0_RX0_N	GND	PE_SLOT4_0_RX3_N	GND	PE_SLOT4_0_TX1_N	GND	KR_SLOT4_TX0_N	G
F	P5V_STBY	GND	LED_POSTCODE_0	GND	PWR_BTN_N_R1	GND	P3V3	GND	RST_N4_N	GND	F
E	P5V_STBY	P5V_STBY	LED_POSTCODE_1	LED_POSTCODE_2	RST_BTN_N_R1	P3V3	P3V3	P3V3	RST_N2_N	CLK_PE_SLOT2_0_REFCLK_P	E
D	GND	P5V_STBY	GND	LED_POSTCODE_3	GND	P3V3	GND	P3V3	SLED_SEATED_N	CLK_PE_SLOT2_0_REFCLK_N	D
C	HAND_SW_ID1	GND	P5V_STBY	GND	LED_POSTCODE_6	GND	P3V3	GND	P3V3	GND	C
B	HAND_SW_ID2	HAND_SW_ID4	P5V_STBY	LED_POSTCODE_4	LED_POSTCODE_7	P3V3	P3V3	P3V3	P3V3	CLK_PE_SLOT4_0_REFCLK_P	B
A	GND	HAND_SW_ID8	GND	LED_POSTCODE_5	GND	P3V3	GND	P3V3	GND	CLK_PE_SLO4_0_REFCLK_N	A
	10	9	8	7	6	5	4	3	2	1	

Adapter Board CONN Pin mapping

<Variant Name>

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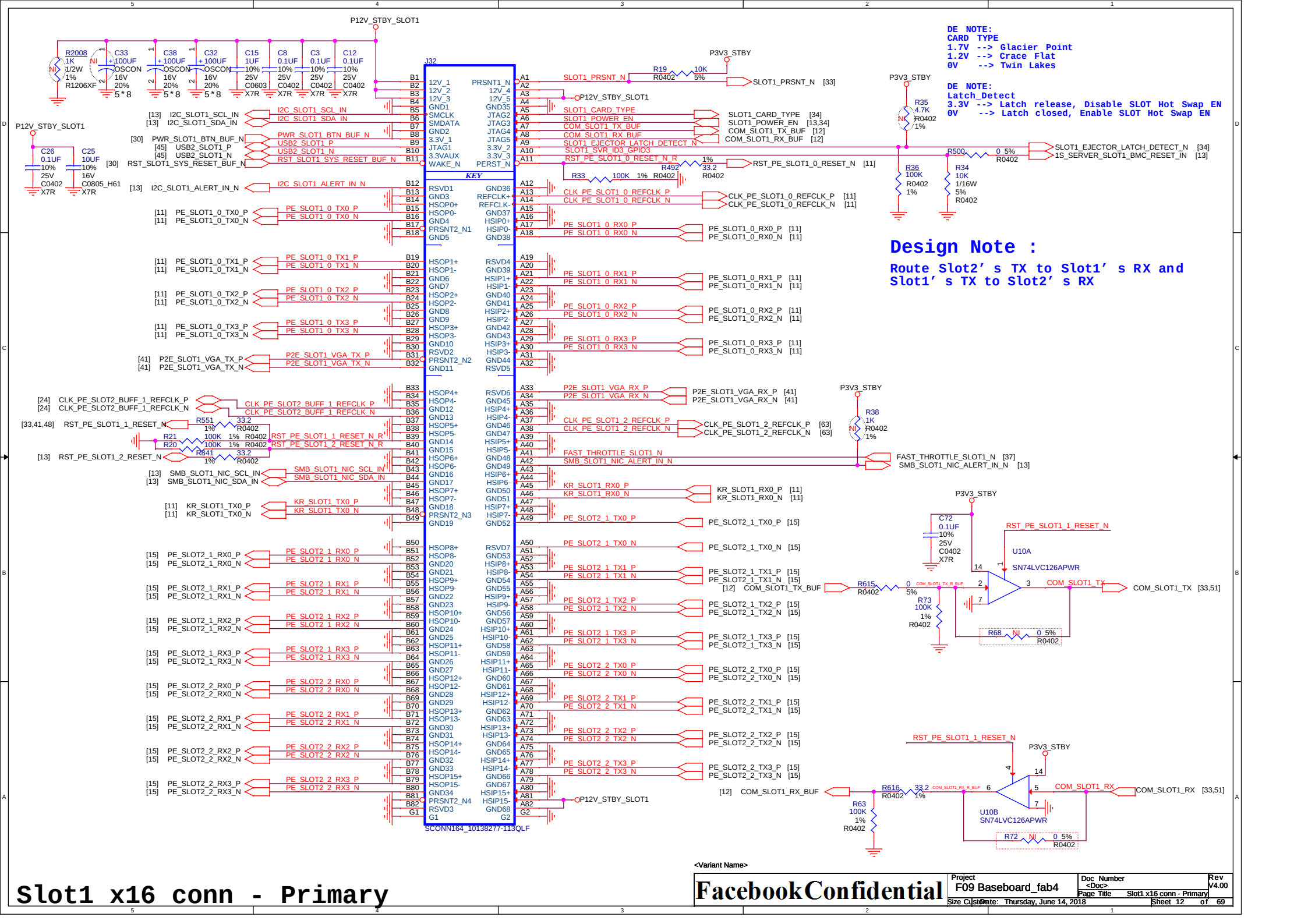
Adapter Board CONN


P12V_STBY_SLOT1
J32
SCONN164_10138277-113QLF
P3V3_STBY
DE NOTE:
CARD TYPE
1.7V --> Glacier Point
1.2V --> Crace Flat
0V --> Twin Lakes
DE NOTE:
Latch_Detect
3.3V --> Latch release, Disable SLOT Hot Swap EN
0V --> Latch closed, Enable SLOT Hot Swap EN
Design Note :
Route Slot2' s TX to Slot1' s RX and
Slot1' s TX to Slot2' s RX
U10A
SN74LVC126APWR
U10B
SN74LVC126APWR
<Variant Name>
FacebookConfidential
Slot1 x16 conn - Primary
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<Doc>
Page Title
Slot1 x16 conn - Primary
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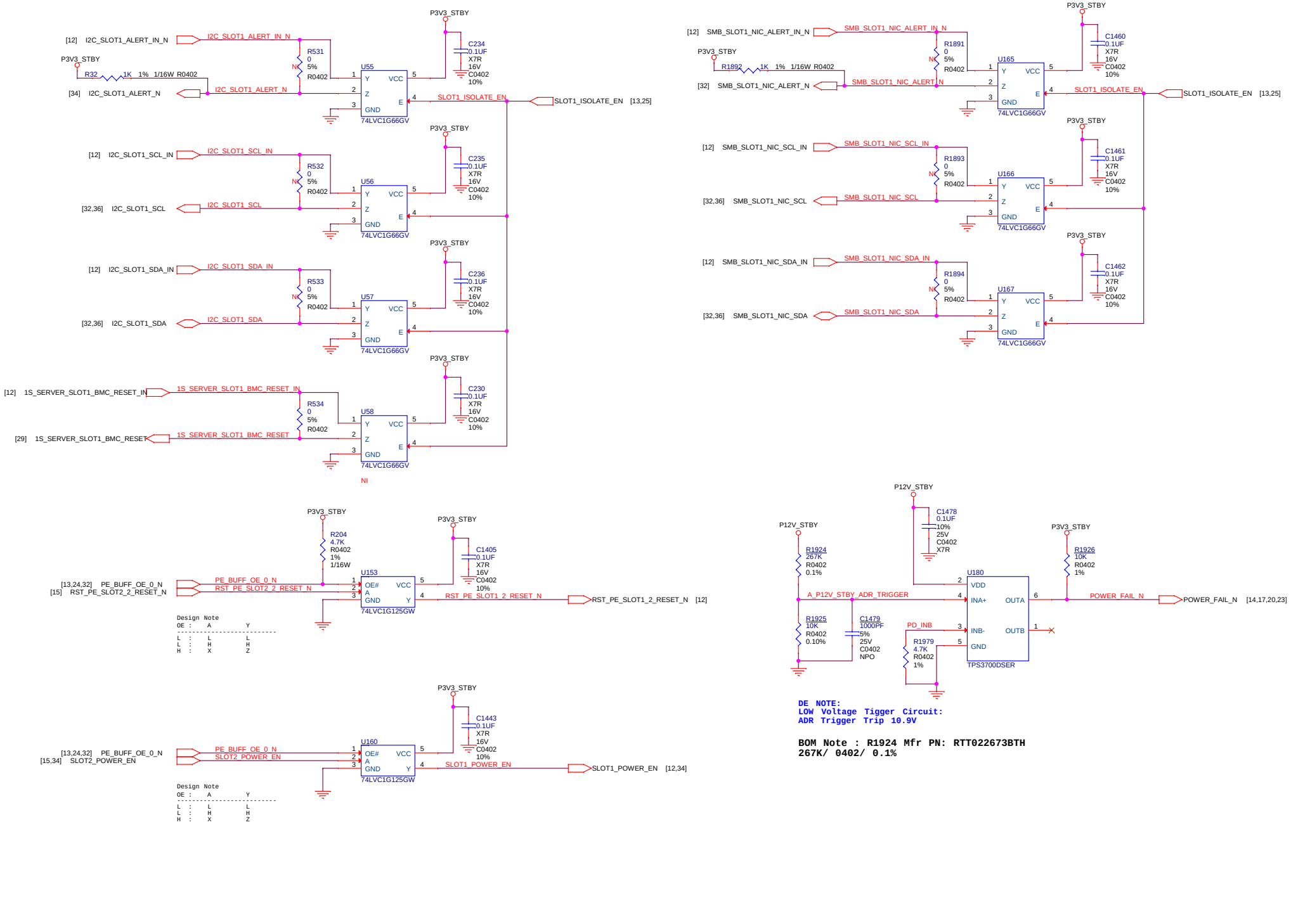

Slot1 Bilateral switch

<Variant Name>

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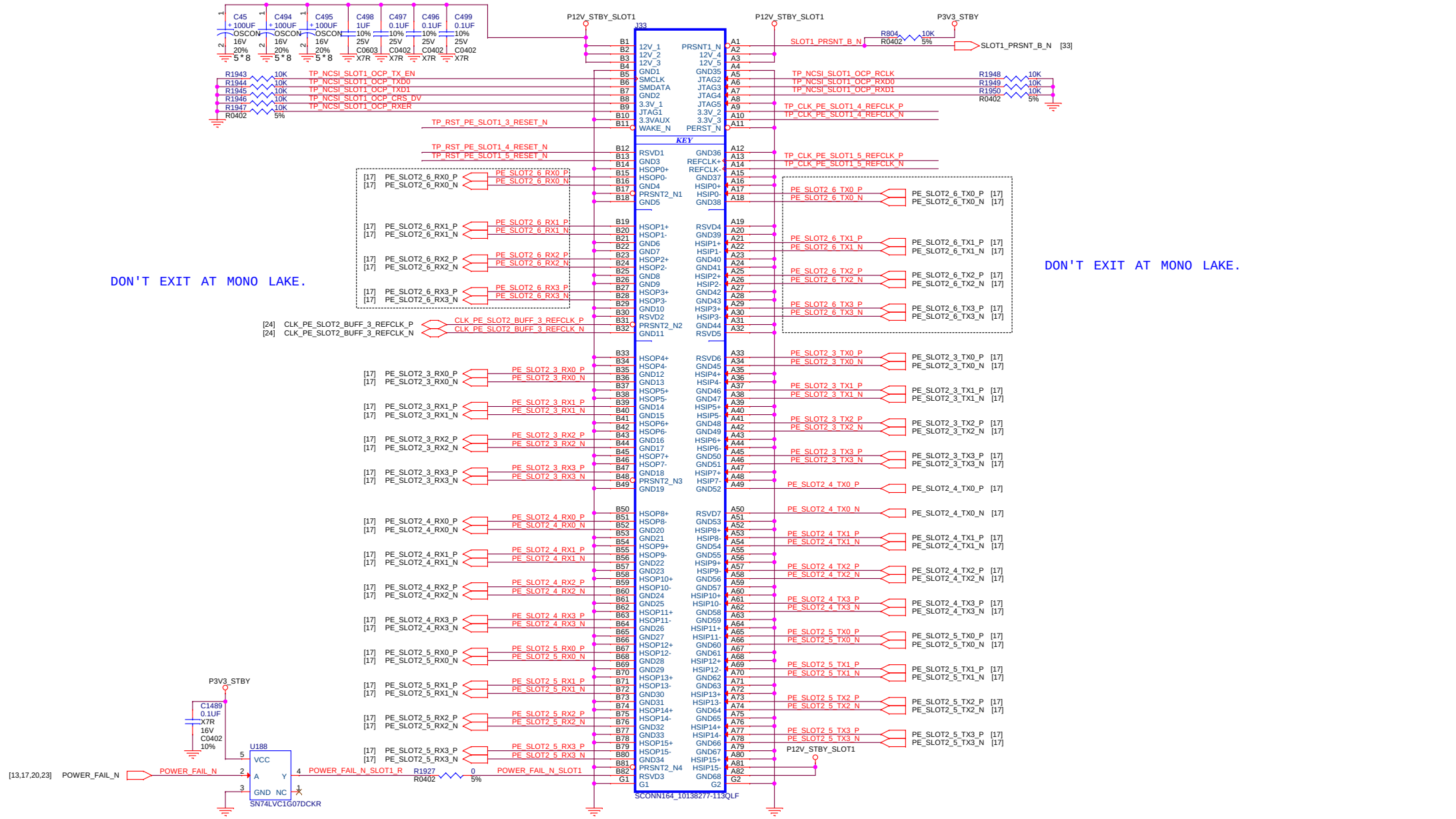

Slot1 X16 conn - Extension

<Variant Name>

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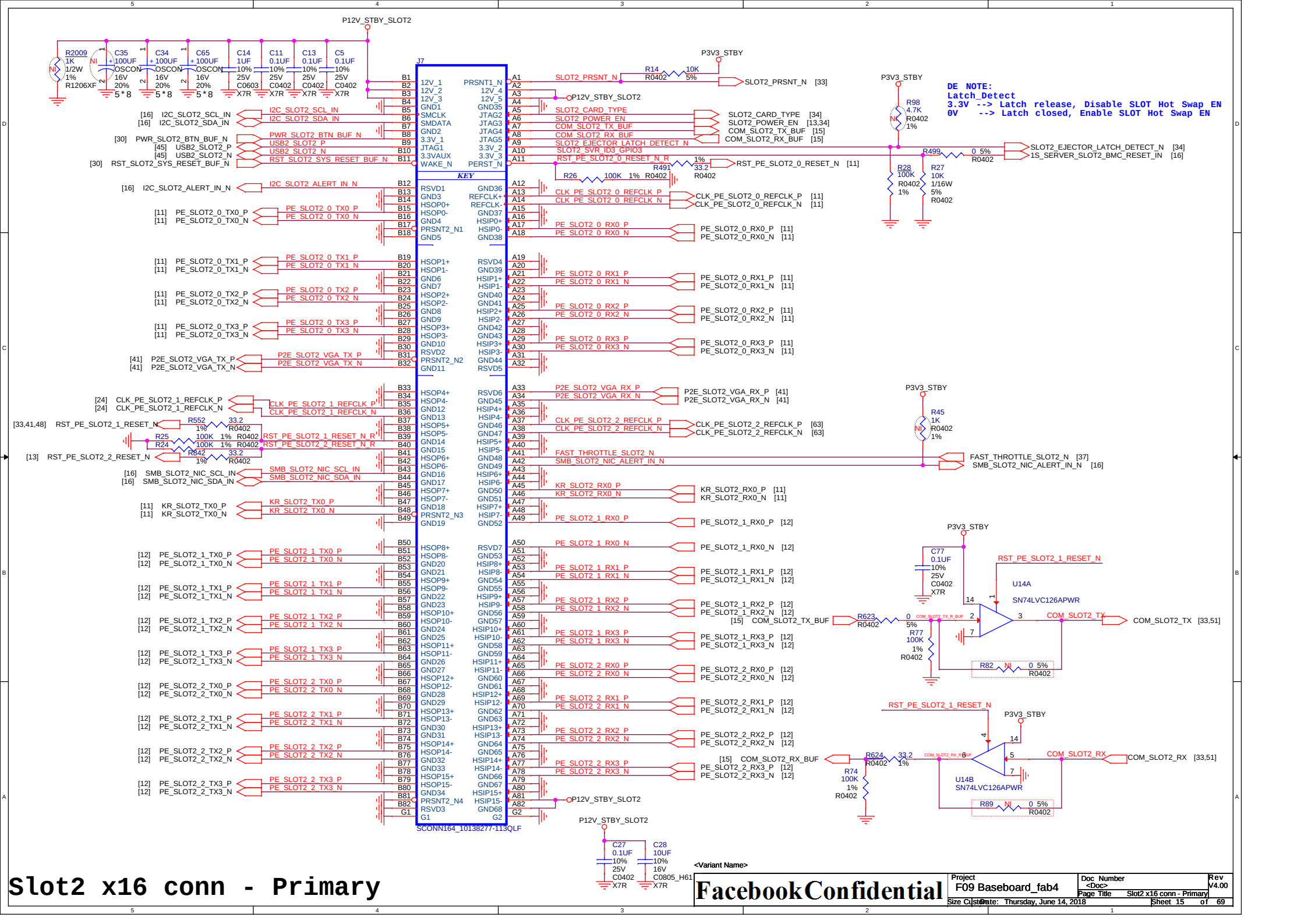

Slot2 x16 conn - Primary

<variant_name>

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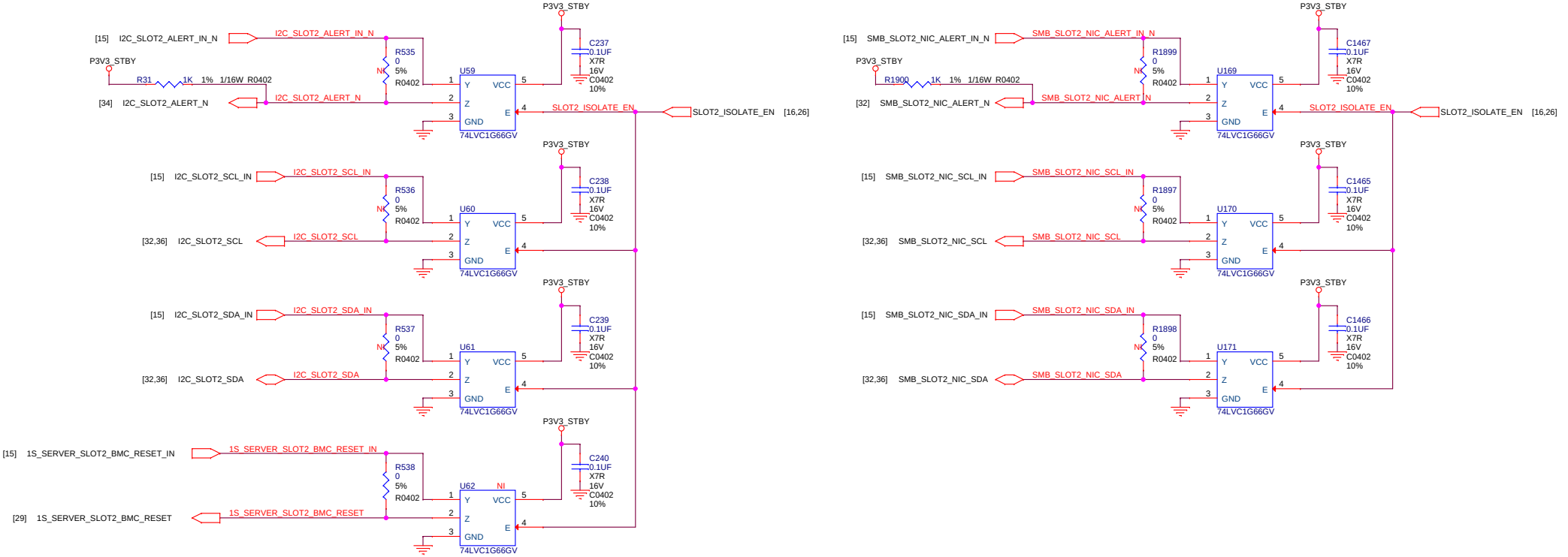

Slot2 Bilateral switch

<Variant Name>

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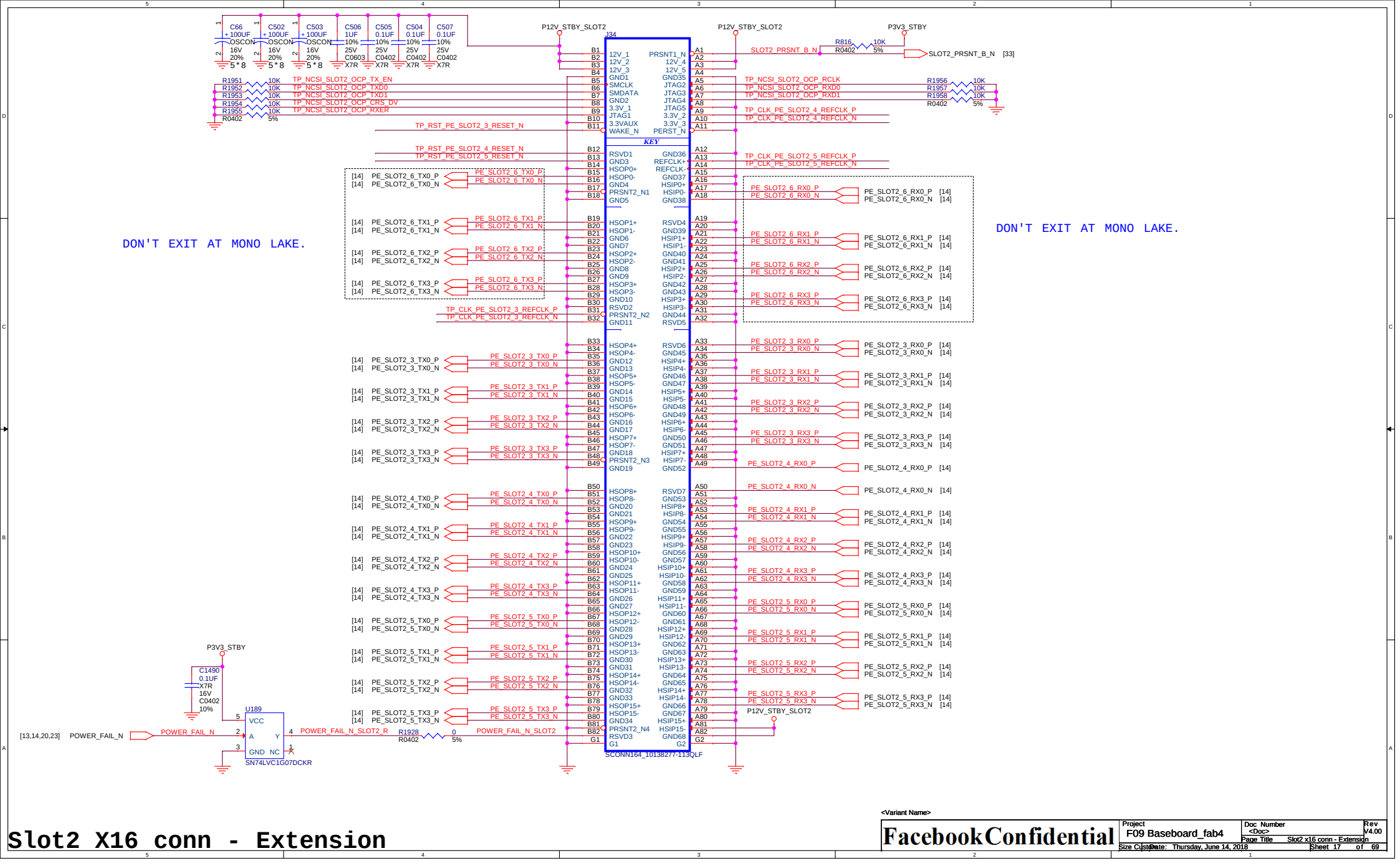

Slot2 X16 conn - Extension

<Variant Name>

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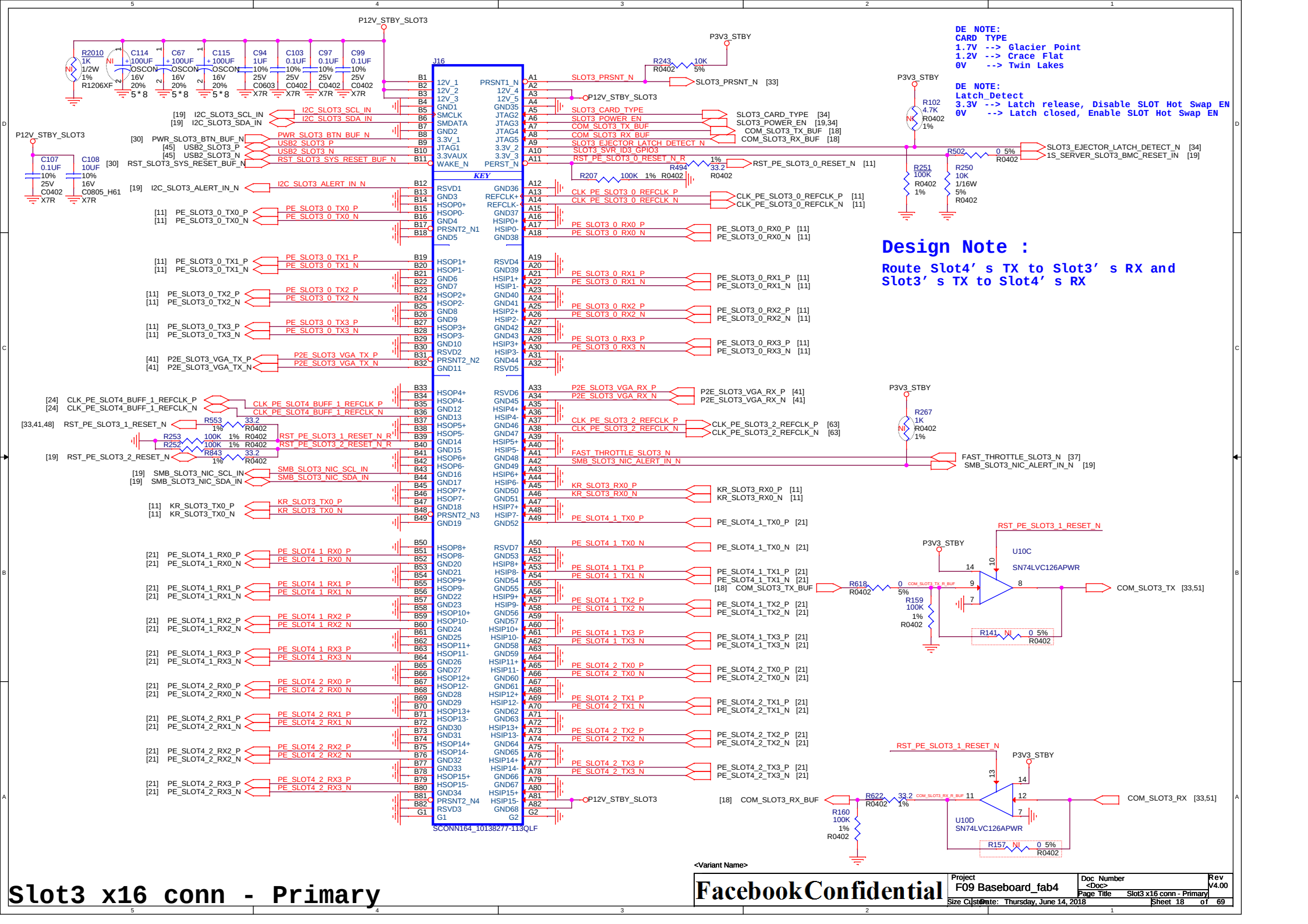
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P3V3_STBY
J16
SCONN164_10138277-113QLF
KEY
DE NOTE:
CARD TYPE
1.7V --> Glacier Point
1.2V --> Crace Flat
0V --> Twin Lakes
DE NOTE:
Latch_Detect
3.3V --> Latch release, Disable SLOT Hot Swap EN
0V --> Latch closed, Enable SLOT Hot Swap EN
Design Note :
Route Slot4' s TX to Slot3' s RX and
Slot3' s TX to Slot4' s RX
U10C
SN74LVC126APWR
U10D
SN74LVC126APWR
COM_SLOT3_TX
COM_SLOT3_RX
FAST_THROTTLE_SLOT3_N
SMB_SLOT3_NIC_ALERT_IN_N
SLOT3_EJECTOR_LATCH_DETECT_N
1S_SERVER_SLOT3_BMC_RESET_IN
RST_PE_SLOT3_0_RESET_N
RST_PE_SLOT3_1_RESET_N
SLOT3_PRSNT_N
SLOT3_CARD_TYPE
SLOT3_POWER_EN
COM_SLOT3_TX_BUF
COM_SLOT3_RX_BUF
CLK_PE_SLOT3_0_REFCLK_P
CLK_PE_SLOT3_0_REFCLK_N
PE_SLOT3_0_RX0_P
PE_SLOT3_0_RX0_N
PE_SLOT3_0_RX1_P
PE_SLOT3_0_RX1_N
PE_SLOT3_0_RX2_P
PE_SLOT3_0_RX2_N
PE_SLOT3_0_RX3_P
PE_SLOT3_0_RX3_N
P2E_SLOT3_VGA_RX_P
P2E_SLOT3_VGA_RX_N
CLK_PE_SLOT3_2_REFCLK_P
CLK_PE_SLOT3_2_REFCLK_N
KR_SLOT3_RX0_P
KR_SLOT3_RX0_N
PE_SLOT4_1_TX0_P
PE_SLOT4_1_TX0_N
PE_SLOT4_1_TX1_P
PE_SLOT4_1_TX1_N
PE_SLOT4_1_TX2_P
PE_SLOT4_1_TX2_N
PE_SLOT4_1_TX3_P
PE_SLOT4_1_TX3_N
PE_SLOT4_2_TX0_P
PE_SLOT4_2_TX0_N
PE_SLOT4_2_TX1_P
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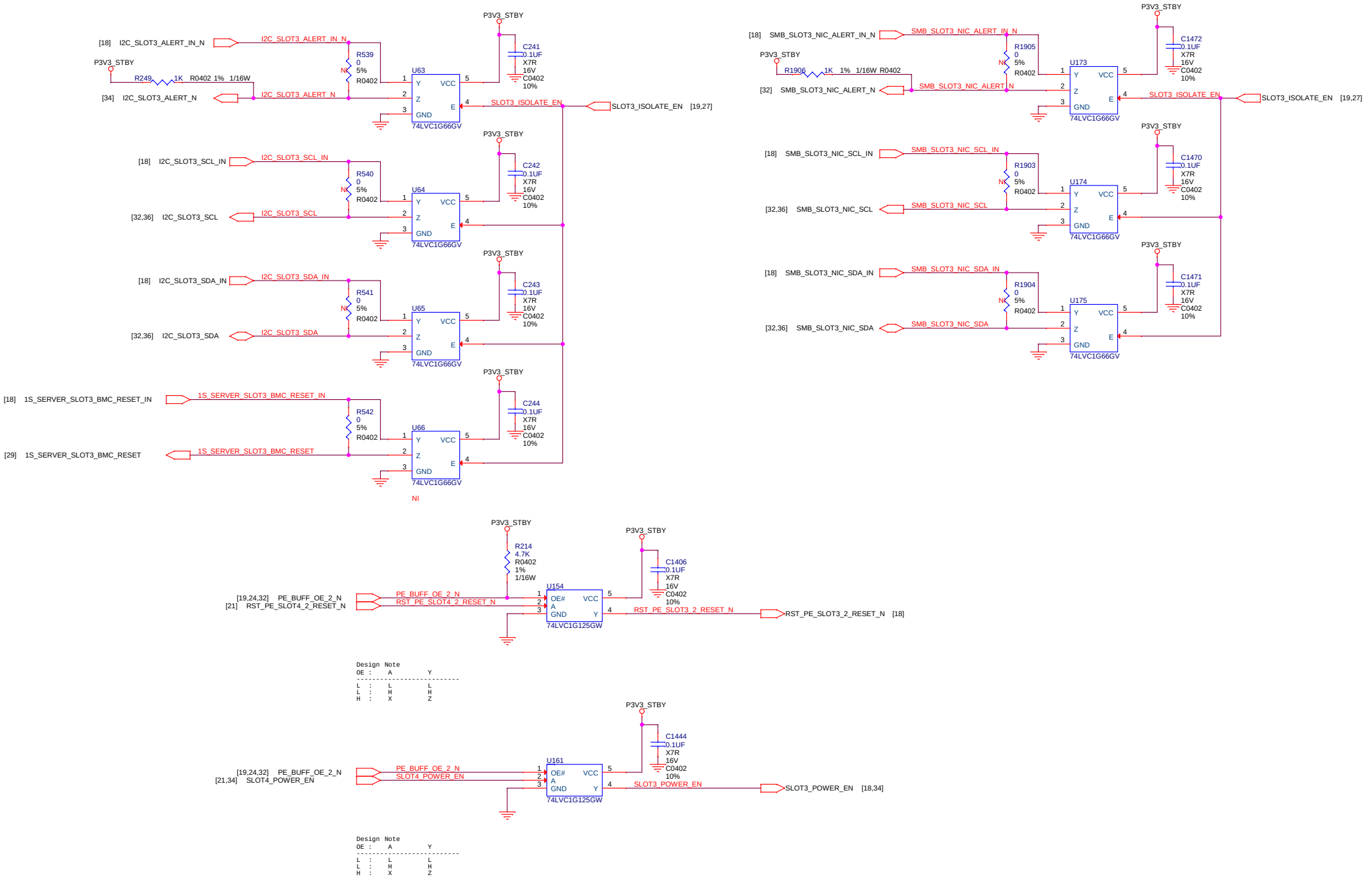
PE_SLOT4_2_TX2_P
PE_SLOT4_2_TX2_N
PE_SLOT4_2_TX3_P
PE_SLOT4_2_TX3_N
I2C_SLOT3_SCL_IN
I2C_SLOT3_SDA_IN
I2C_SLOT3_ALERT_IN_N
PWR_SLOT3_BTN_BUF_N
USB2_SLOT3_P
USB2_SLOT3_N
RST_SLOT3_SYS_RESET_BUF_N
P2E_SLOT3_VGA_TX_P
P2E_SLOT3_VGA_TX_N
KR_SLOT3_TX0_P
KR_SLOT3_TX0_N
SMB_SLOT3_NIC_SCL_IN
SMB_SLOT3_NIC_SDA_IN
RST_PE_SLOT3_2_RESET_N
SLOT3_SVR_ID3_GPIO3
CLK_PE_SLOT4_BUFF_1_REFCLK_P
CLK_PE_SLOT4_BUFF_1_REFCLK_N



Slot3 Bilateral switch

<Variant Name>

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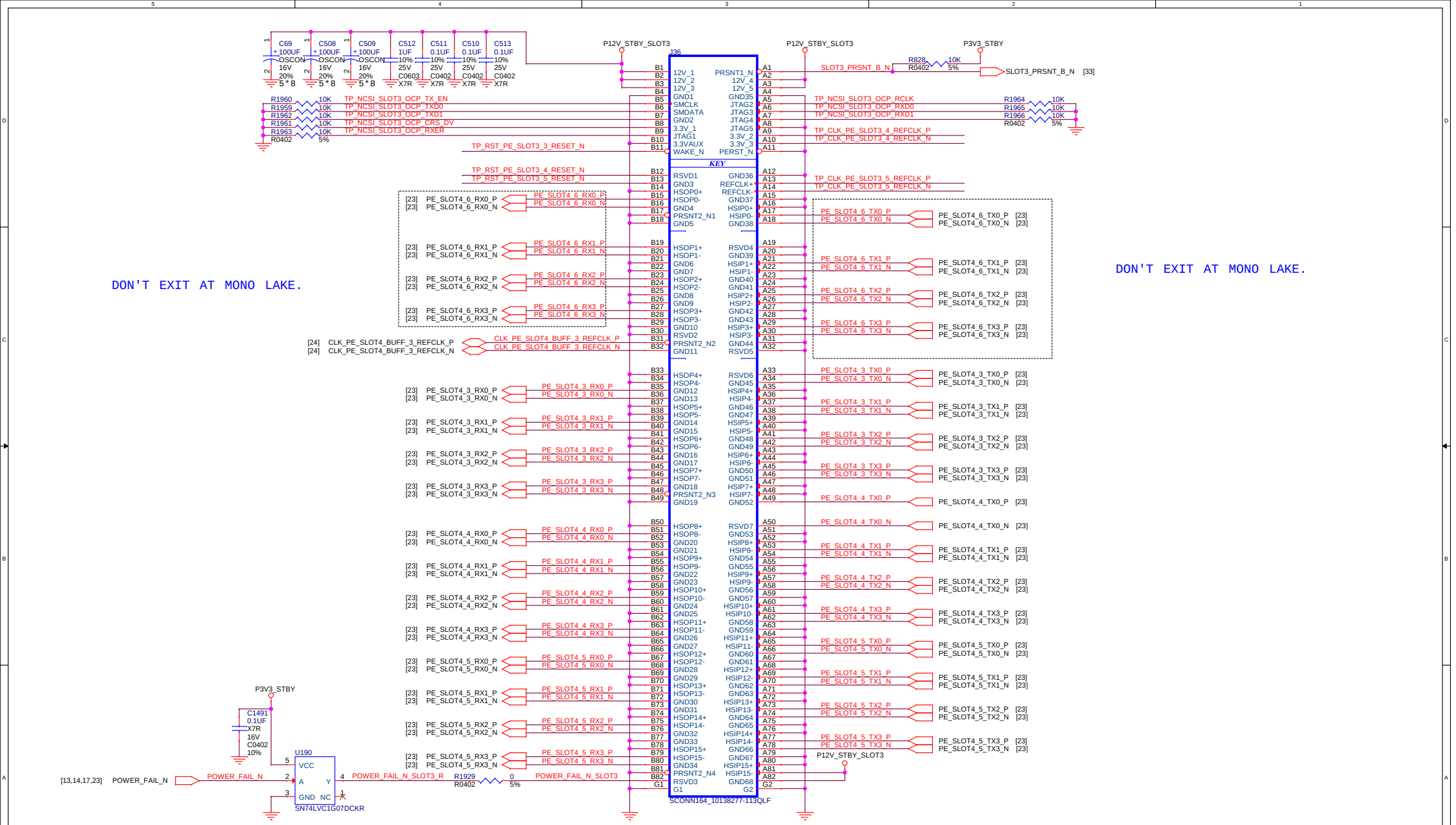

<variant_name>

Slot3 X16 conn - Extension

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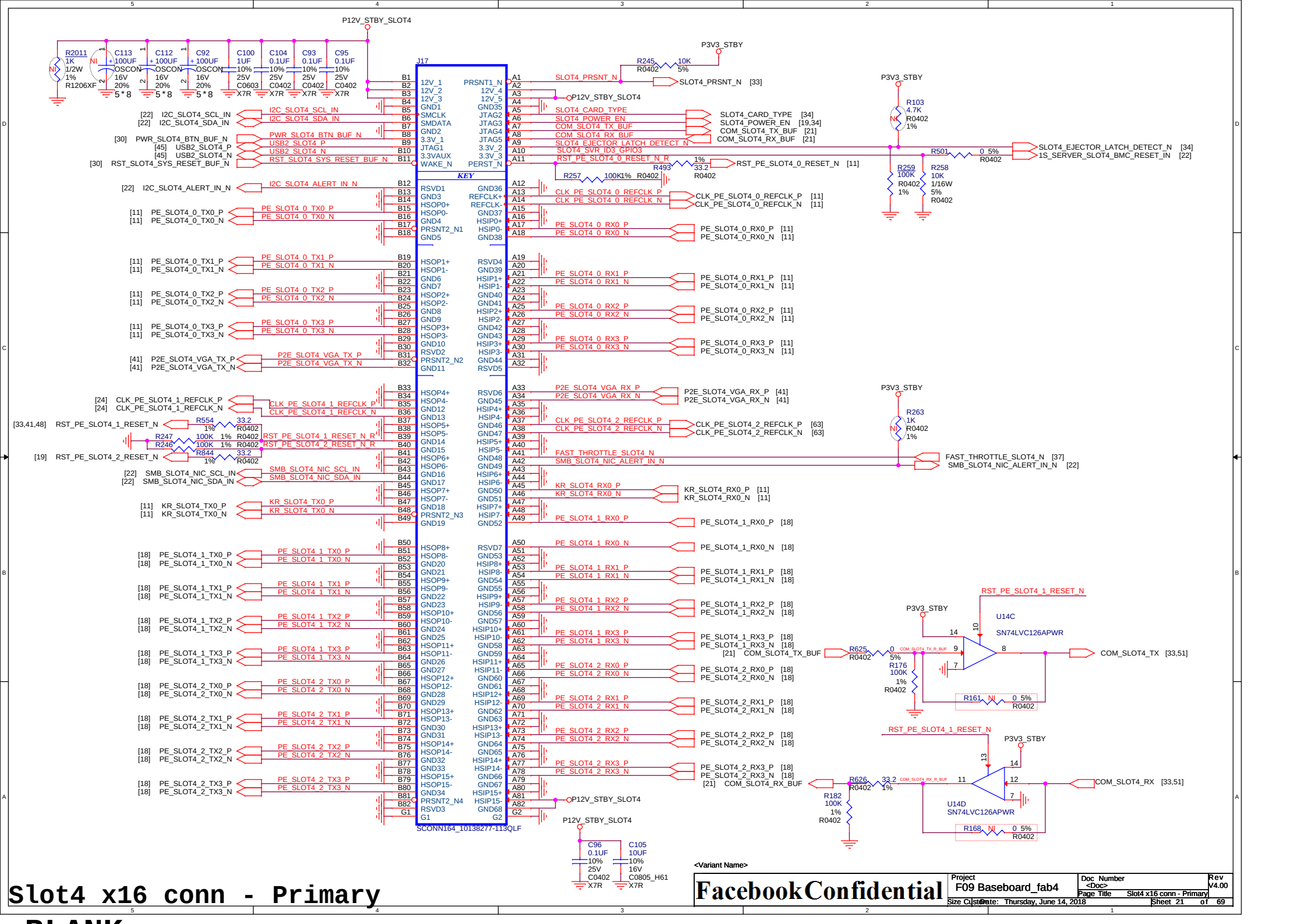

Slot4 x16 conn - Primary

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<Variant Name>

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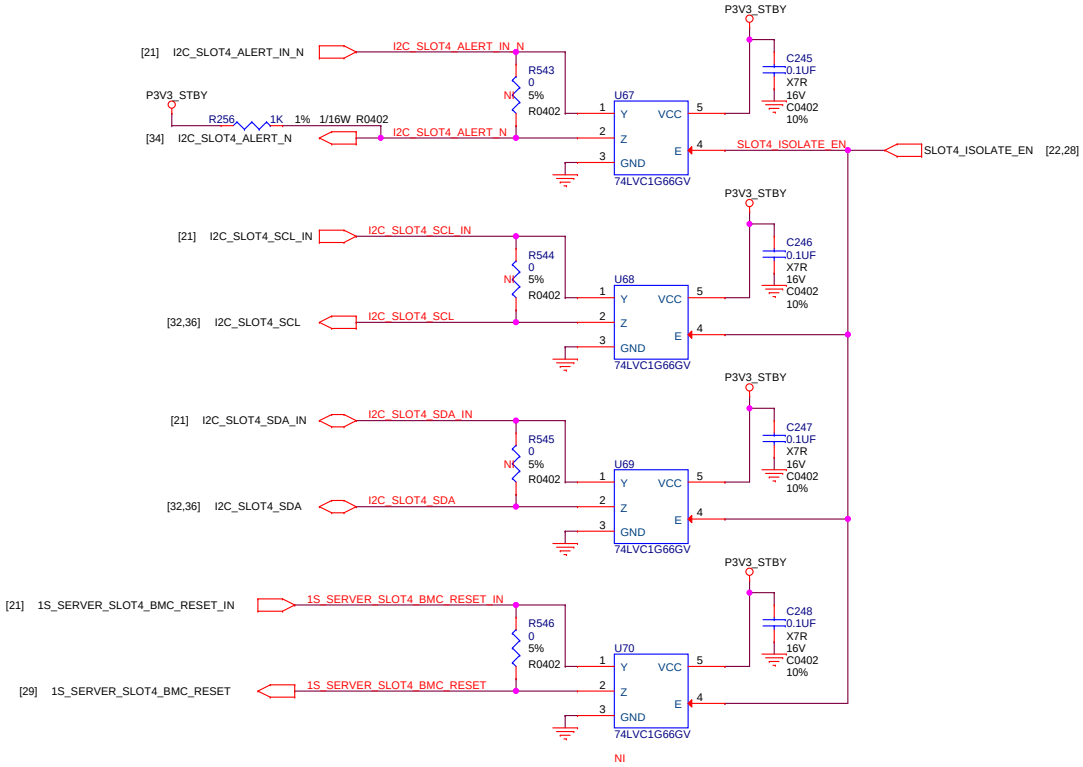

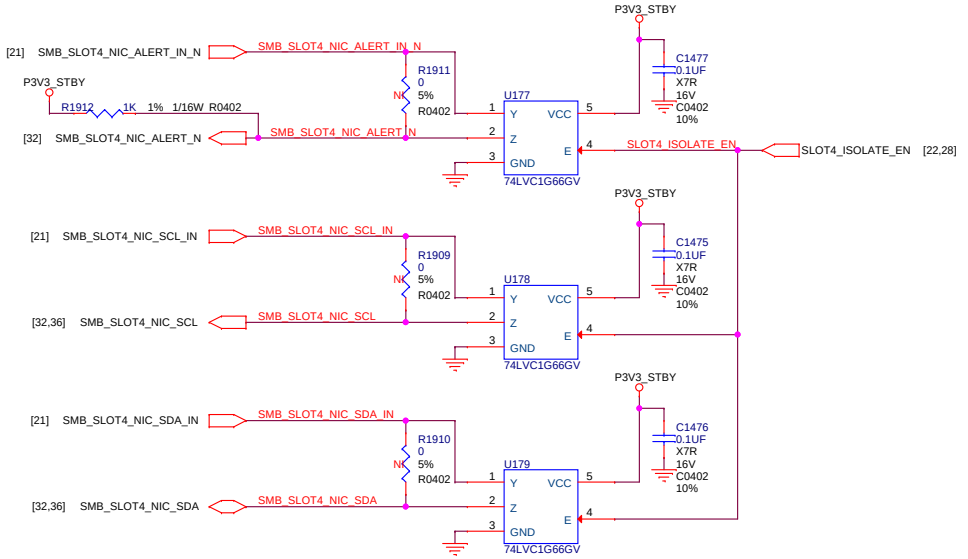

Slot4 Bilateral switch

<Variant Name>

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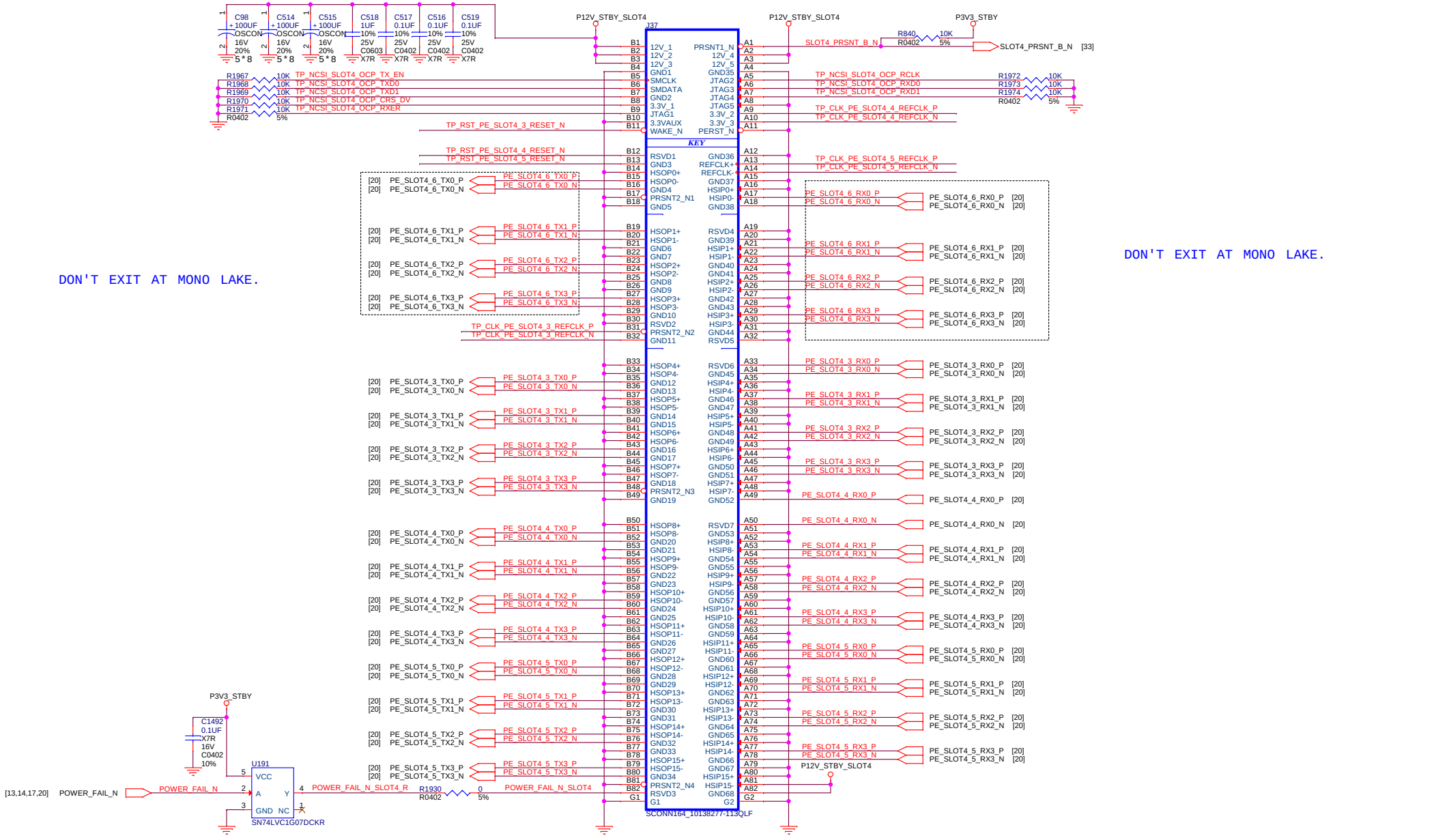
Project: F09 Baseboard_fab4	Doc Number: <Doc>	Rev: V4.00
	Page Title: Slot4Bilateral switch	
Size: Custom	Date: Thursday, June 14, 2018	Sheet 22 of 69

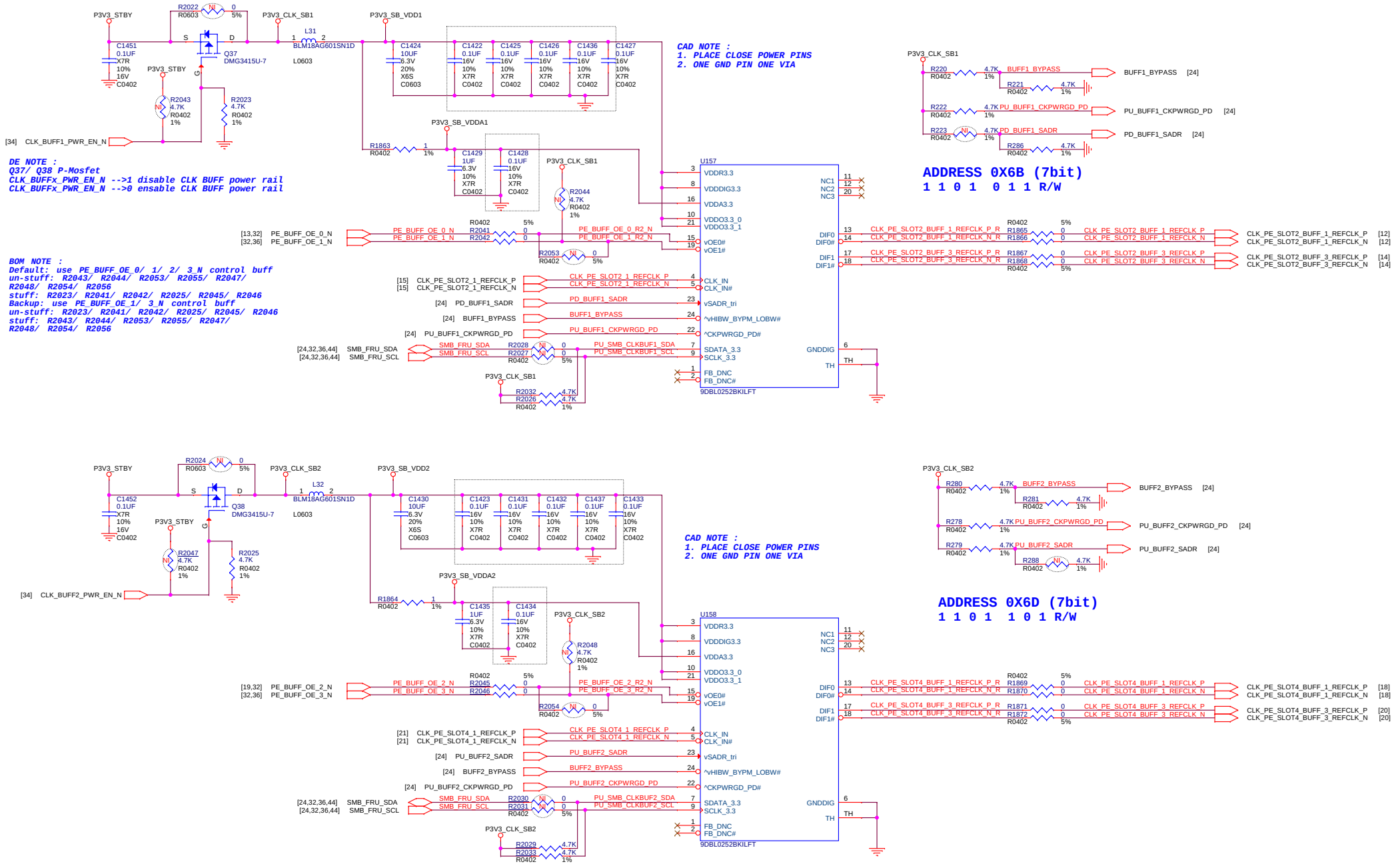


Slot4 X16 conn - Extension

<Variant Name>

FacebookConfidential

Project: F09 Baseboard_fab4	Doc Number: <Doc>	Rev: V4.00	
Size: Custom	Date: Thursday, June 14, 2018	Page Title: Slot4 x16 conn - Extension	Sheet 23 of 69

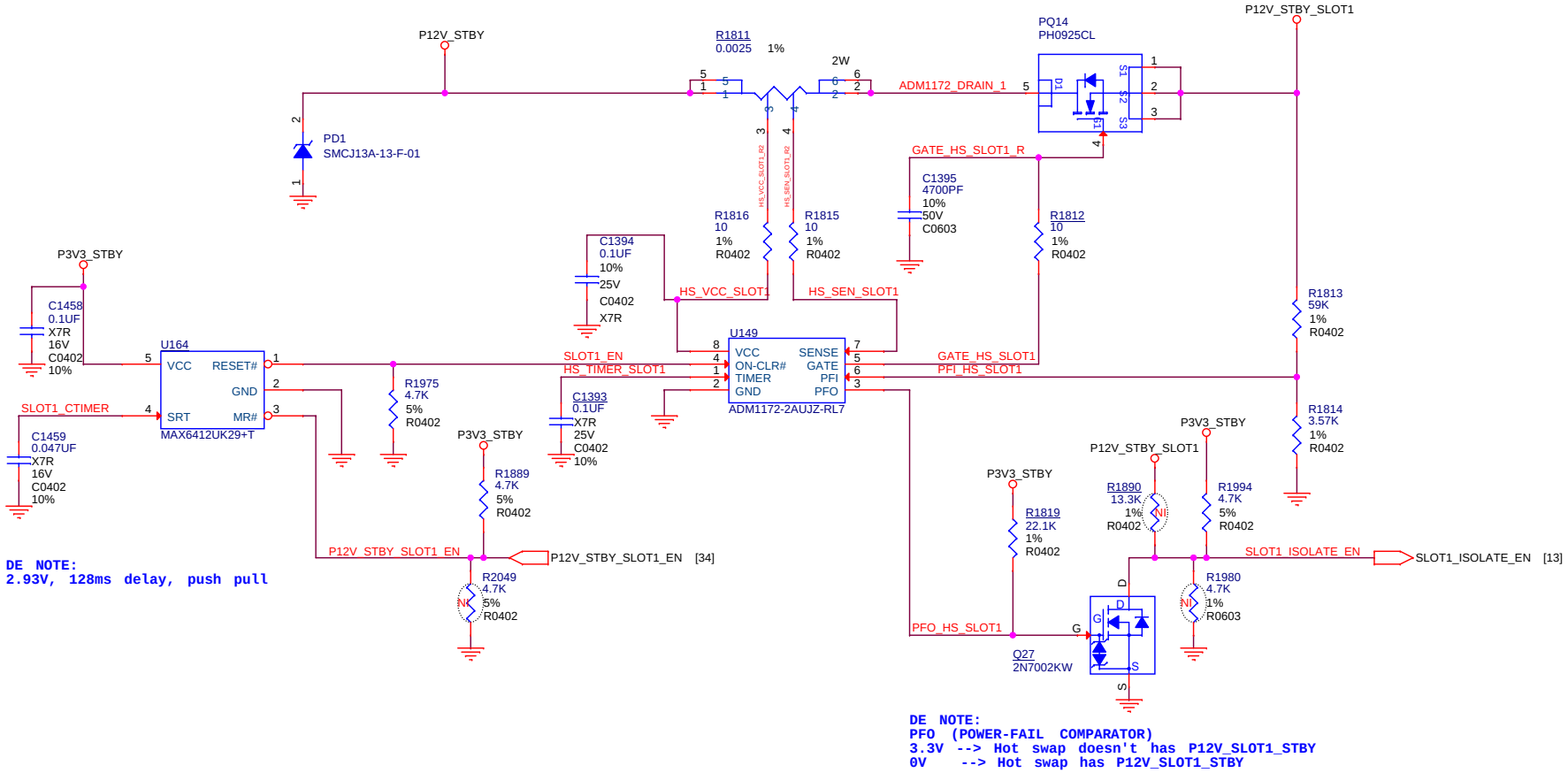


CLOCK BUFF

<Variant Name>

FacebookConfidential

Project: F09 Baseboard_fab4		Doc Number: <Doc>	Rev: V4.00
Size: Custom	Date: Thursday, June 14, 2018	Page Title: CLK BUFF	Sheet 24 of 69

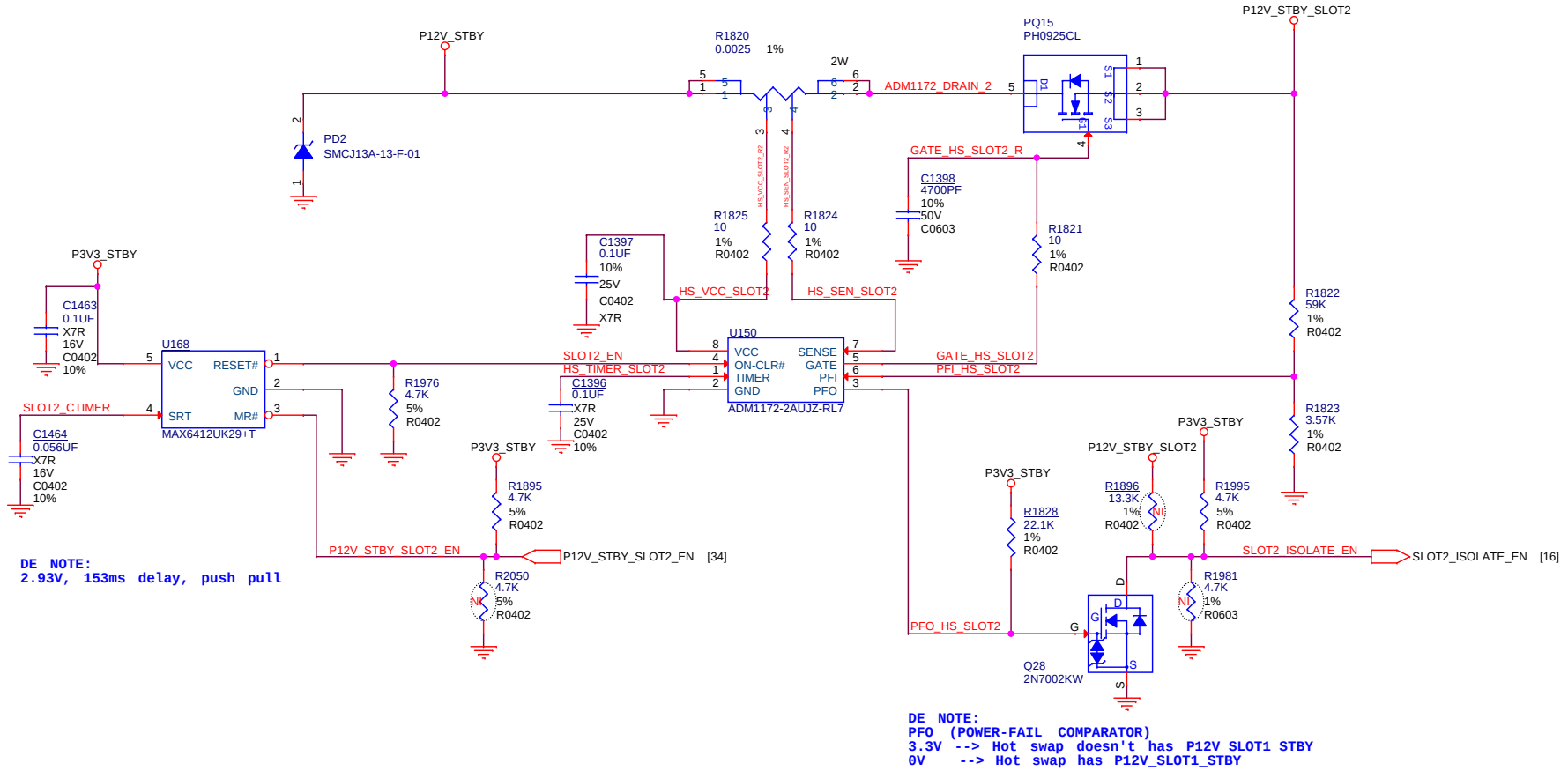


Slot1 Power Switch

<Variant Name>

FacebookConfidential

Project: F09 Baseboard_fab4	Doc Number: <Doc>		Rev: V4.00
	Page Title: Slot1 Power Switch		
Size: B	Date: Thursday, June 14, 2018	Sheet 25 of 69	



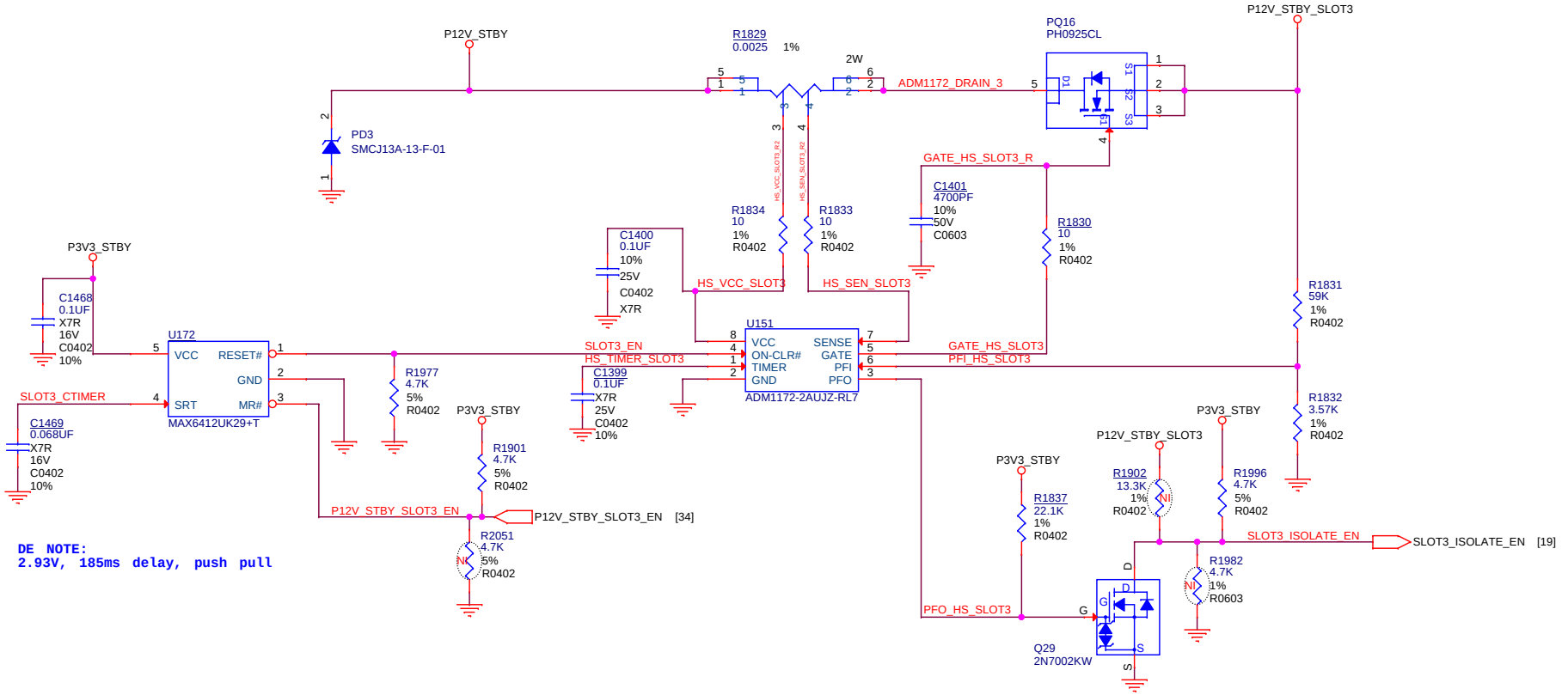
Slot2 Power Switch

<Variant Name>

FacebookConfidential

Project: F09 Baseboard_fab4	Doc Number: <Doc>		Rev: V4.00
	Page Title: Slot2 Power Switch		
Size B	Date: Thursday, June 14, 2018	Sheet 26	of 69

OCP: 20A
I= 50 mV/ 2.5 m ohm
=20A



DE NOTE:
2.93V, 185ms delay, push pull

DE NOTE:
PFO (POWER-FAIL COMPARATOR)
3.3V --> Hot swap doesn't has P12V_SLOT1_STBY
0V --> Hot swap has P12V_SLOT1_STBY

Slot3 Power Switch

<Variant Name>

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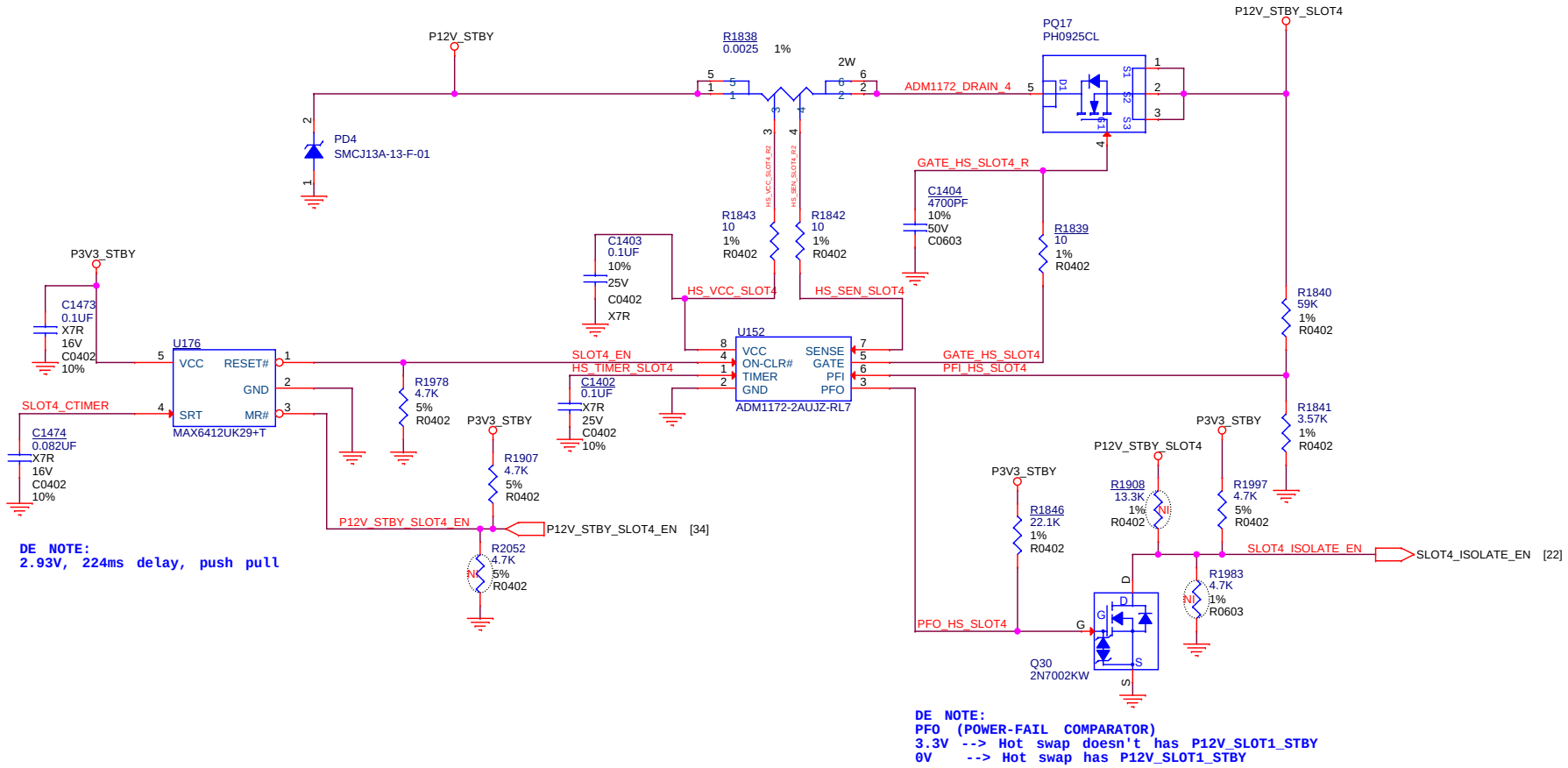
Project: F09 Baseboard_fab4	Doc Number: <Doc>		Rev: V4.00
	Page Title: Slot3 Power Switch		
Size: B	Date: Thursday, June 14, 2018	Sheet 27	of 69

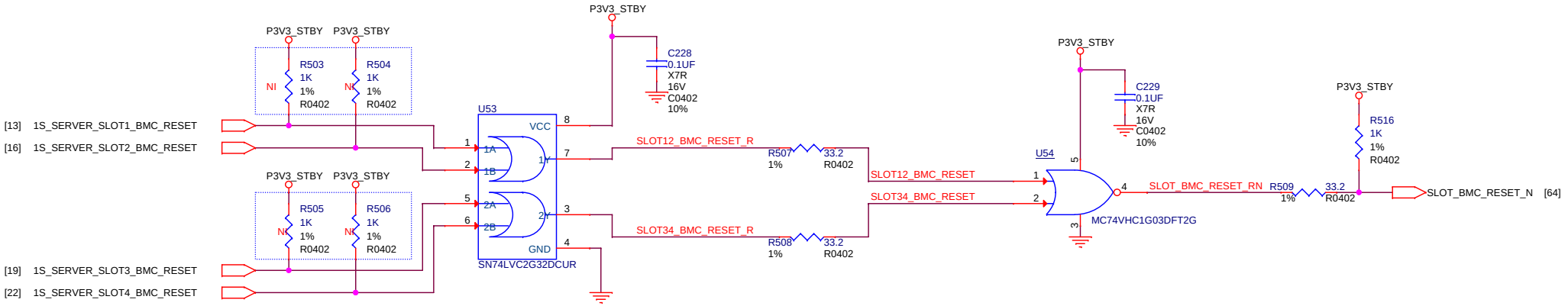


Slot4 Power Switch

<Variant Name>

FacebookConfidential

Project: F09 Baseboard_fab4	Doc Number: <Doc>		Rev: V4.00
	Page Title: Slot4 Power Switch		
Size B	Date: Thursday, June 14, 2018	Sheet 28	of 69

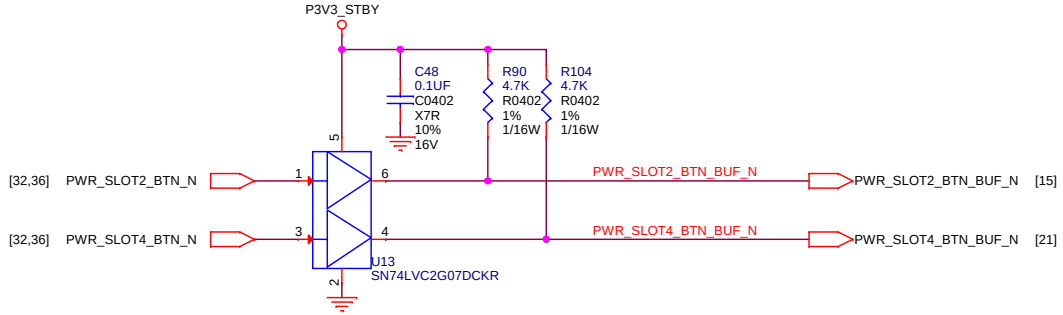


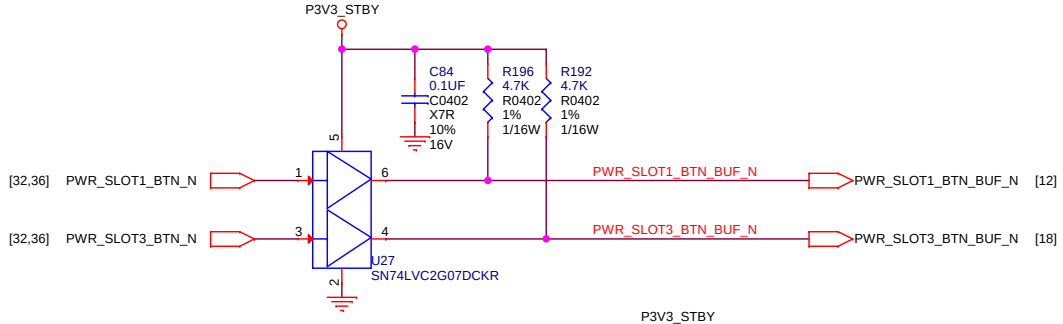
BMC RESET

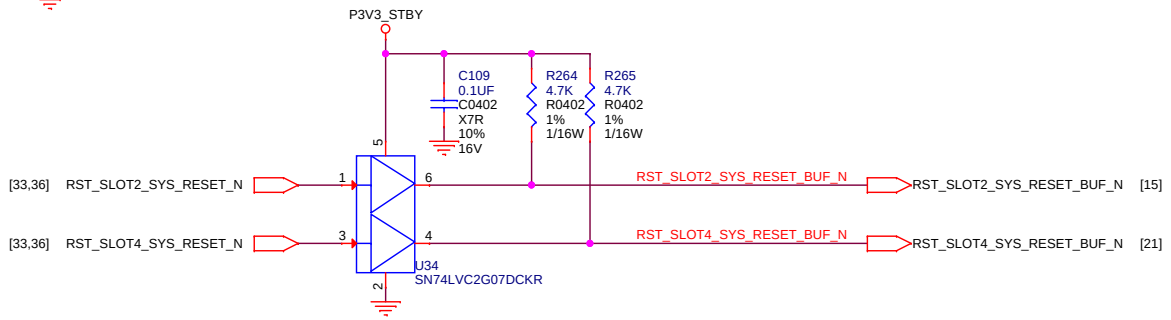
<Variant Name>

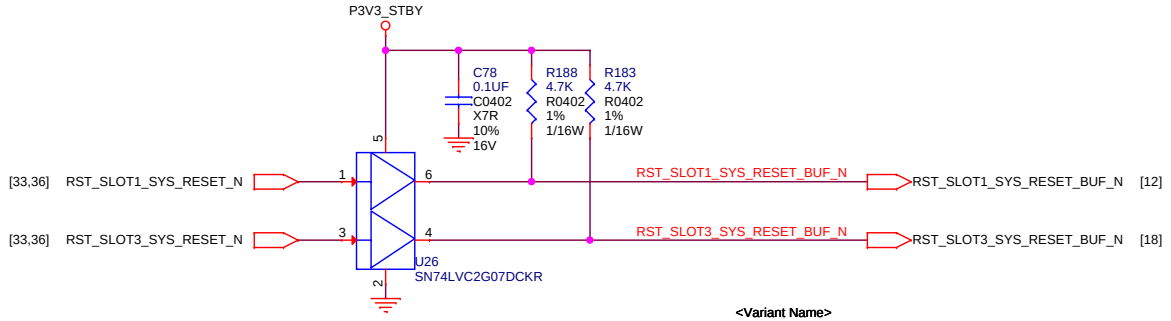
FacebookConfidential

Project: F09 Baseboard_fab4	Doc Number: <Doc>		Rev: V4.00
	Page Title: BMC RESET		
Size: B	Date: Thursday, June 14, 2018	Sheet 29 of 69	









PWR/RST BTN BUFFER

<Variant Name>

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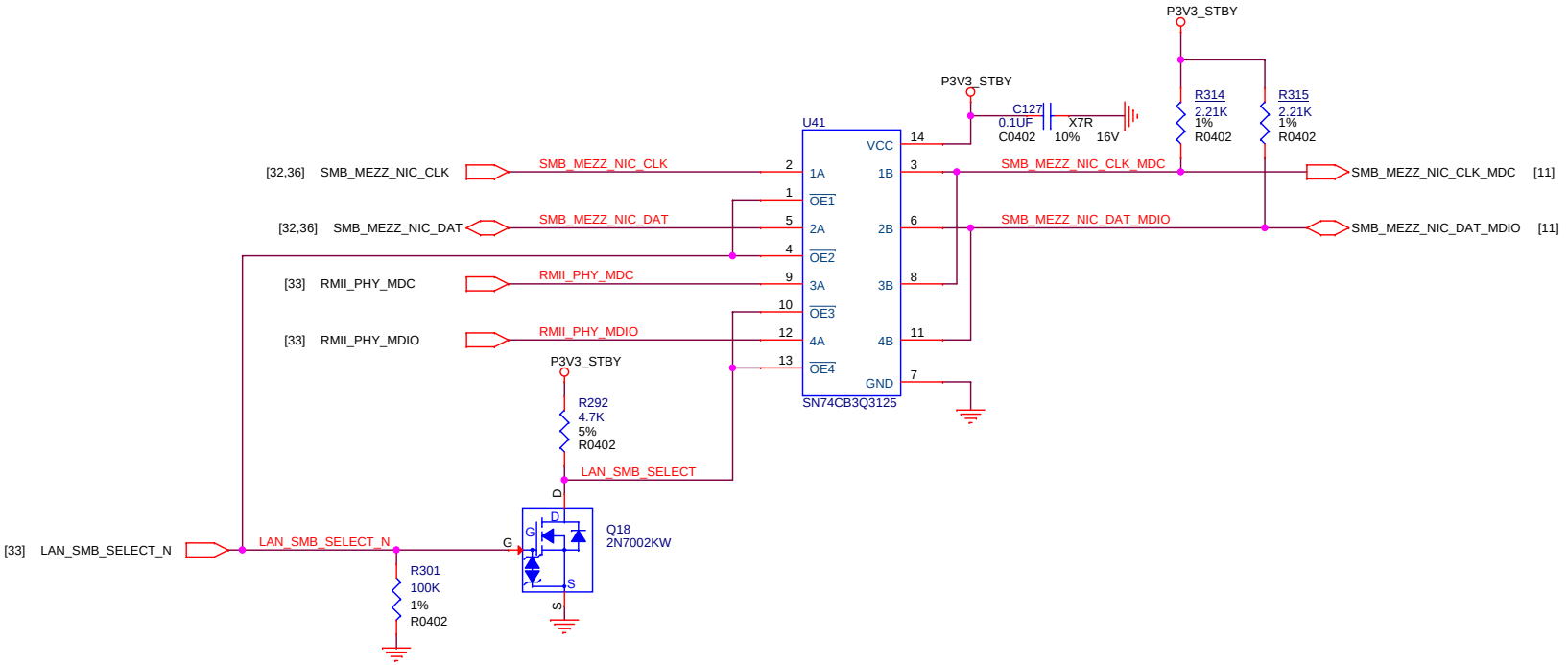
Project: F09 Baseboard_fab4		Doc Number: <Doc>	Rev: V4.00
		Page Title: PWR/RST BTN BUFFER	
Size: B	Date: Thursday, June 14, 2018	Sheet 30 of 69	



LAN_SMB_SELECT_N
Low: select SMB_MEZZ_NIC_CLK/DAT(default)
High: select RMII_PHY_MDC/MDIO

OCP MEZZ Card NIC SMB/MDC MUX

<Variant Name>

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Project: F09 Baseboard_fab4	Doc Number: <Doc>	Rev: V4.00
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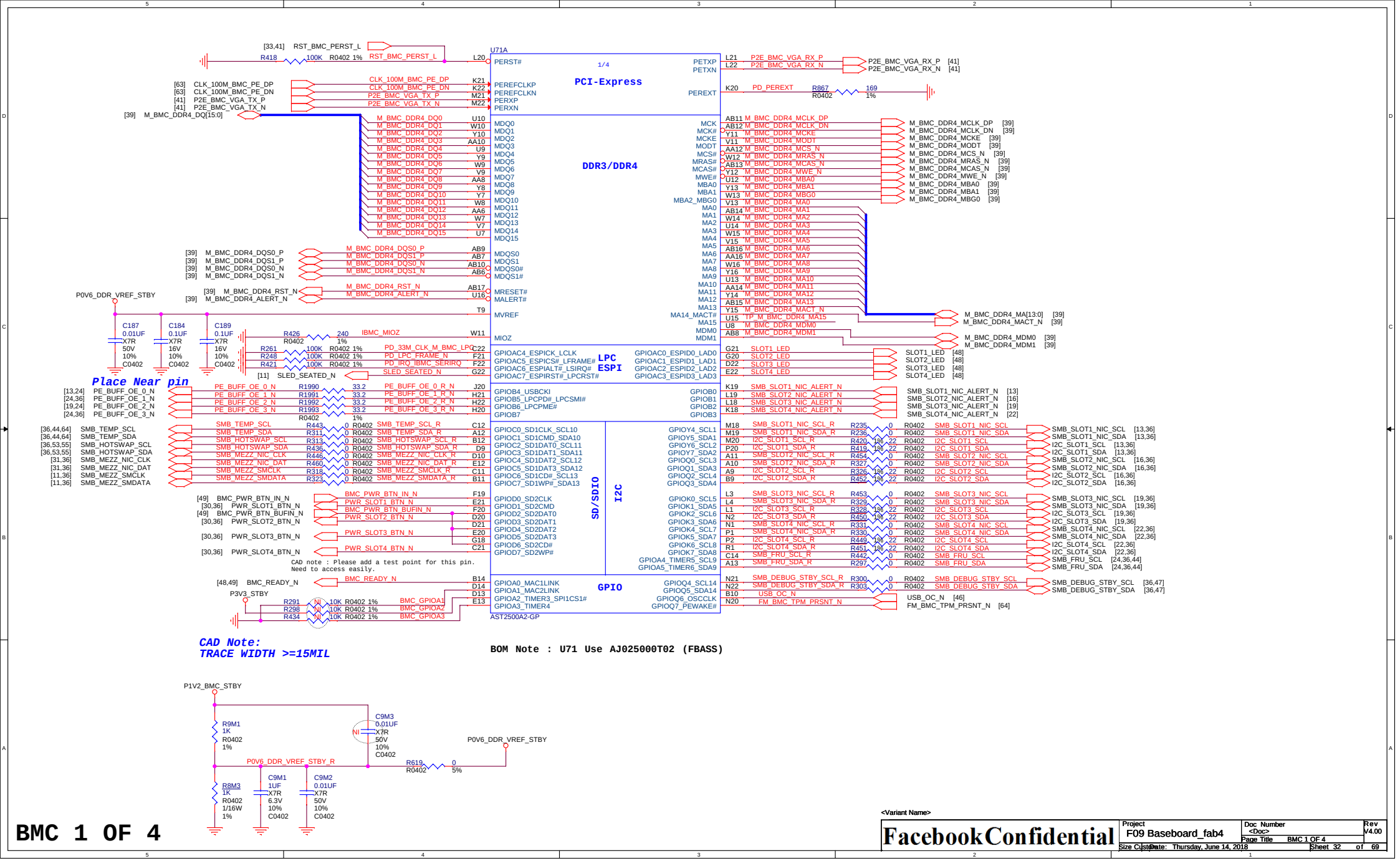
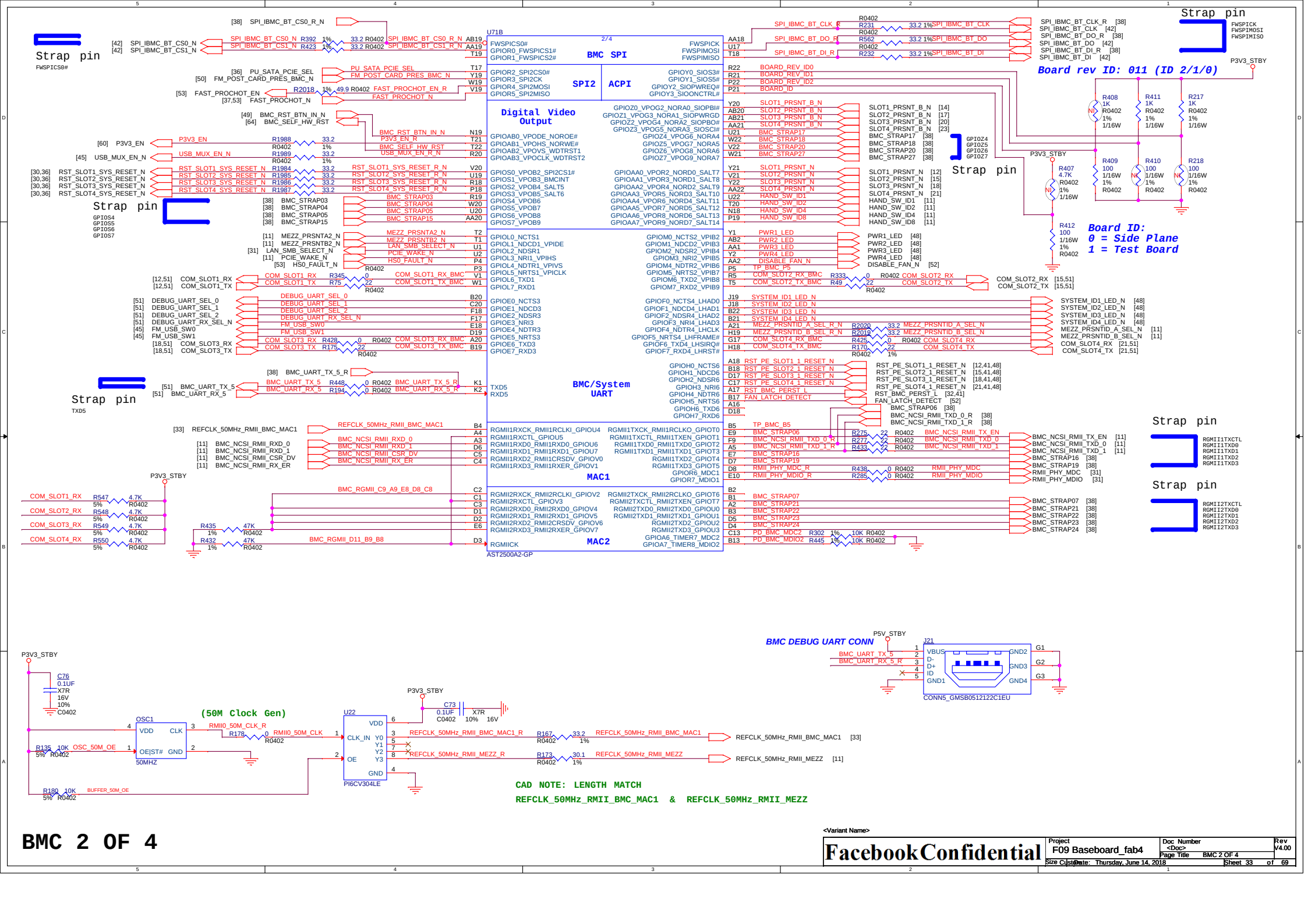
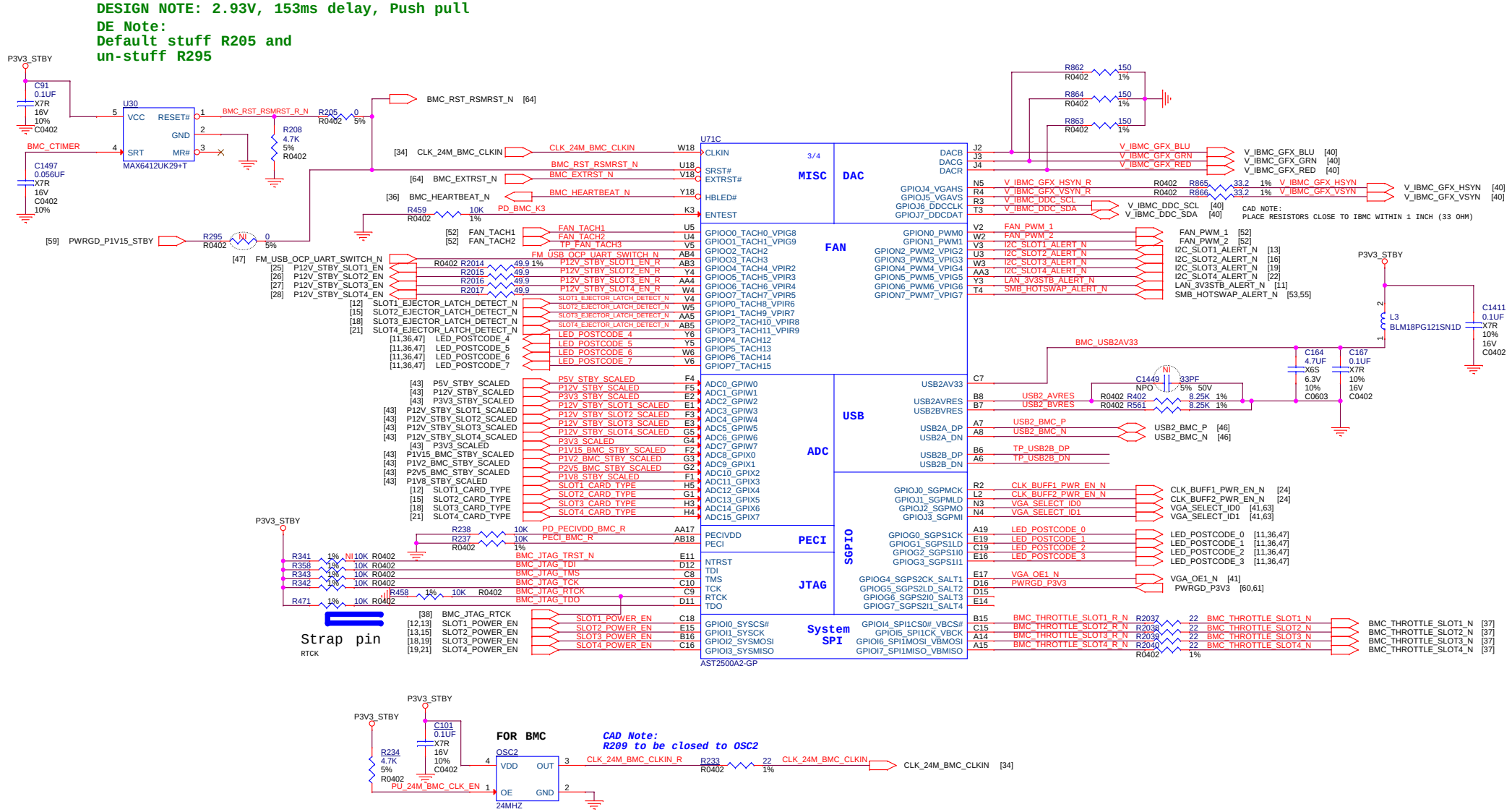
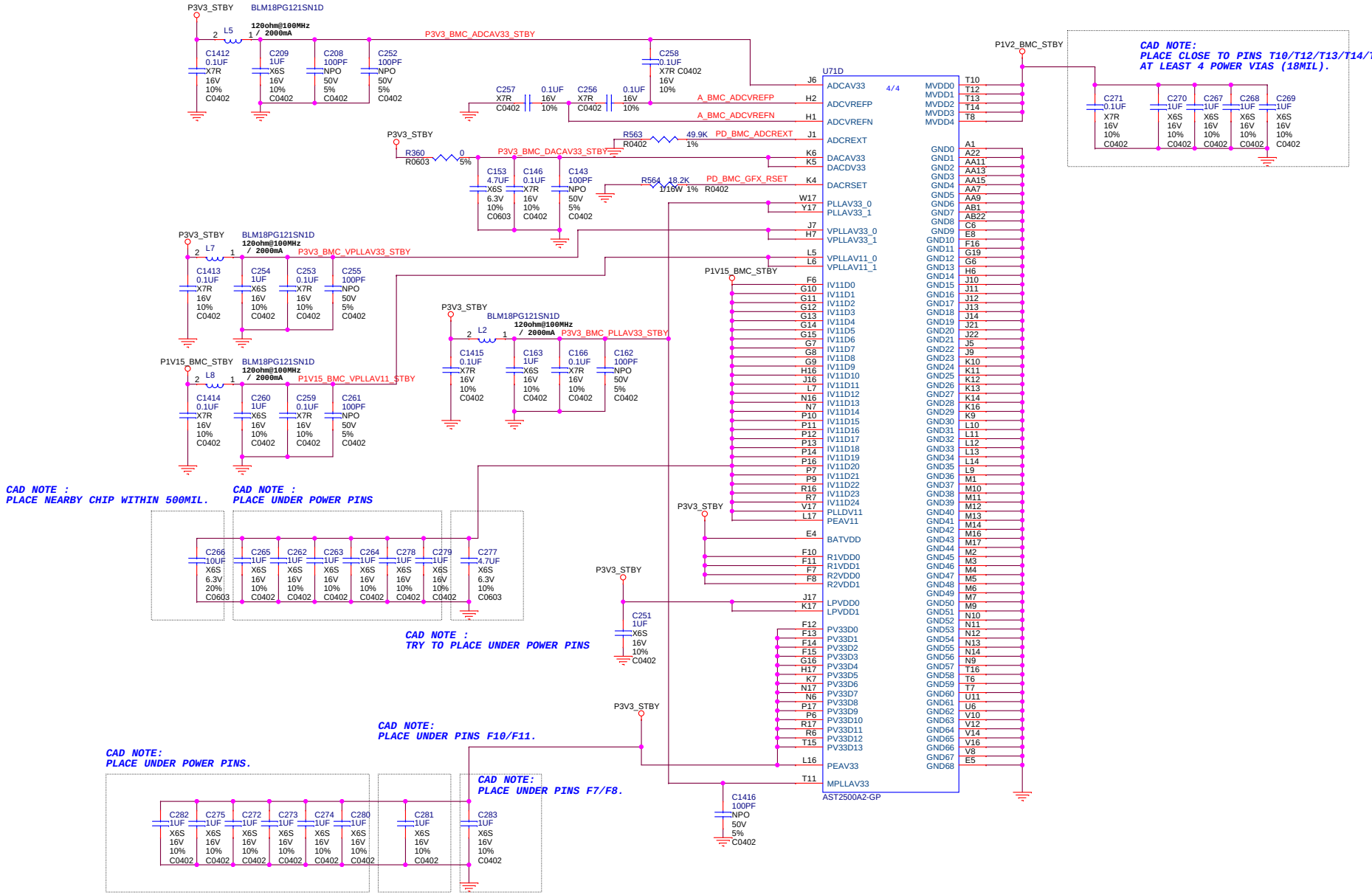
Page Title: OCP MEZZ Card NIC SMB/MDC MUX		



BMC 1 OF 4


U71B
BMC SPI
SPI2
ACPI
Digital Video Output
BMC/System UART
MAC1
MAC2
AST2500A2-GP
Strap pin
FWSPICS0#
GPIOS4 GPIOS5 GPIOS6 GPIOS7
TXD5
Board rev ID: 011 (ID 2/1/0)
Board ID:
0 = Side Plane
1 = Test Board
BMC DEBUG UART CONN
CONN5_GMSB0512122C1EU
(50M Clock Gen)
OSC1
50MHZ
PI6CV304LE
CAD NOTE: LENGTH MATCH
REFCLK_50MHz_RMII_BMC_MAC1 & REFCLK_50MHz_RMII_MEZZ
BMC 2 OF 4
FacebookConfidential
F09 Baseboard_fab4
Thursday, June 14, 2018


DESIGN NOTE: 2.93V, 153ms delay, Push pull
DE Note:
Default stuff R205 and
un-stuff R295
P3V3_STBY
C91 0.1UF X7R 16V 10% C0402
U30
MAX6412UK29+T
VCC
RESET#
GND
SRT
MR#
BMC_CTIMER
C1497 0.056UF X7R 16V C0402 10%
BMC_RST_RSMRST_R_N
R205 0 R0402 5%
R208 4.7K 5% R0402
BMC_RST_RSMRST_N [64]
PWRGD_P1V15_STBY [59]
R295 NI 0 R0402 5%
FM_USB_OCP_UART_SWITCH_N [47]
P12V_STBY_SLOT1_EN [25]
P12V_STBY_SLOT2_EN [26]
P12V_STBY_SLOT3_EN [27]
P12V_STBY_SLOT4_EN [28]
R2014 R2015 R2016 R2017 49.9 1%
SLOT1_EJECTOR_LATCH_DETECT_N [12]
SLOT2_EJECTOR_LATCH_DETECT_N [15]
SLOT3_EJECTOR_LATCH_DETECT_N [18]
SLOT4_EJECTOR_LATCH_DETECT_N [21]
LED_POSTCODE_4 [11,36,47]
LED_POSTCODE_5 [11,36,47]
LED_POSTCODE_6 [11,36,47]
LED_POSTCODE_7 [11,36,47]
P5V_STBY_SCALED [43]
P12V_STBY_SCALED [43]
P3V3_STBY_SCALED [43]
P12V_STBY_SLOT1_SCALED [43]
P12V_STBY_SLOT2_SCALED [43]
P12V_STBY_SLOT3_SCALED [43]
P12V_STBY_SLOT4_SCALED [43]
P1V15_BMC_STBY_SCALED [43]
P1V2_BMC_STBY_SCALED [43]
P2V5_BMC_STBY_SCALED [43]
P1V8_STBY_SCALED [43]
SLOT1_CARD_TYPE [12]
SLOT2_CARD_TYPE [15]
SLOT3_CARD_TYPE [18]
SLOT4_CARD_TYPE [21]
U71C
CLKIN
SRST#
EXTRST#
HBLED#
ENTEST
MISC
3/4
CLK_24M_BMC_CLKIN [34]
BMC_EXTRST_N [64]
BMC_HEARTBEAT_N [36]
R459 10K 1%
PD_BMC_K3
FAN_TACH1 [52]
FAN_TACH2 [52]
TP_FAN_TACH3
FAN
ADC
USB
PECI
JTAG
SGPIO
System SPI
DAC
AST2500A2-GP
R862 R864 R863 150 1%
V_IBMC_GFX_BLU [40]
V_IBMC_GFX_GRN [40]
V_IBMC_GFX_RED [40]
V_IBMC_GFX_HSYN [40]
V_IBMC_GFX_VSYN [40]
R865 R866 33.2 1%
V_IBMC_DDC_SCL [40]
V_IBMC_DDC_SDA [40]
CAD NOTE:
PLACE RESISTORS CLOSE TO IBMC WITHIN 1 INCH (33 OHM)
FAN_PWM_1 [52]
FAN_PWM_2 [52]
I2C_SLOT1_ALERT_N [13]
I2C_SLOT2_ALERT_N [16]
I2C_SLOT3_ALERT_N [19]
I2C_SLOT4_ALERT_N [22]
LAN_3V3STB_ALERT_N [11]
SMB_HOTSWAP_ALERT_N [53,55]
L3 BLM18PG121SN1D
C1411 0.1UF X7R 10% 16V C0402
BMC_USB2AV33
C164 4.7UF X6S 6.3V 10% C0603
C167 0.1UF X7R 10% 16V C0402
C1449 NI 33PF NPO 5% 50V
R402 R561 8.25K 1%
USB2_AVRES
USB2_BMC_P [46]
USB2_BMC_N [46]
TP_USB2B_DP
TP_USB2B_DN
CLK_BUFF1_PWR_EN_N [24]
CLK_BUFF2_PWR_EN_N [24]
VGA_SELECT_ID0 [41,63]
VGA_SELECT_ID1 [41,63]
LED_POSTCODE_0 [11,36,47]
LED_POSTCODE_1 [11,36,47]
LED_POSTCODE_2 [11,36,47]
LED_POSTCODE_3 [11,36,47]
VGA_OE1_N [41]
PWRGD_P3V3 [60,61]
R238 R237 10K 1%
PD_PECIVDD_BMC_R
PECI_BMC_R
R341 R358 R343 R342 10K R0402 1%
BMC_JTAG_TRST_N
BMC_JTAG_TDI
BMC_JTAG_TMS
BMC_JTAG_TCK
R458 10K R0402 1%
BMC_JTAG_RTCK
R471 10K R0402 1%
BMC_JTAG_TDO
Strap pin
RTCK
SLOT1_POWER_EN [12,13]
SLOT2_POWER_EN [13,15]
SLOT3_POWER_EN [18,19]
SLOT4_POWER_EN [19,21]
R2037 R2038 R2039 R2040 22 1%
BMC_THROTTLE_SLOT1_R_N
BMC_THROTTLE_SLOT2_R_N
BMC_THROTTLE_SLOT3_R_N
BMC_THROTTLE_SLOT4_R_N
BMC_THROTTLE_SLOT1_N [37]
BMC_THROTTLE_SLOT2_N [37]
BMC_THROTTLE_SLOT3_N [37]
BMC_THROTTLE_SLOT4_N [37]
C101 0.1UF X7R 16V 10% C0402
R234 4.7K 5% R0402
PU_24M_BMC_CLK_EN
OSC2
VDD
OUT
OE
GND
24MHZ
FOR BMC
CAD Note:
R209 to be closed to OSC2
CLK_24M_BMC_CLKIN_R
R233 22 1%
CLK_24M_BMC_CLKIN [34]



BMC 4 OF 4

<Variant Name>

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Project: F09 Baseboard_fab4		Doc Number: <Doc>	Rev: V4.00
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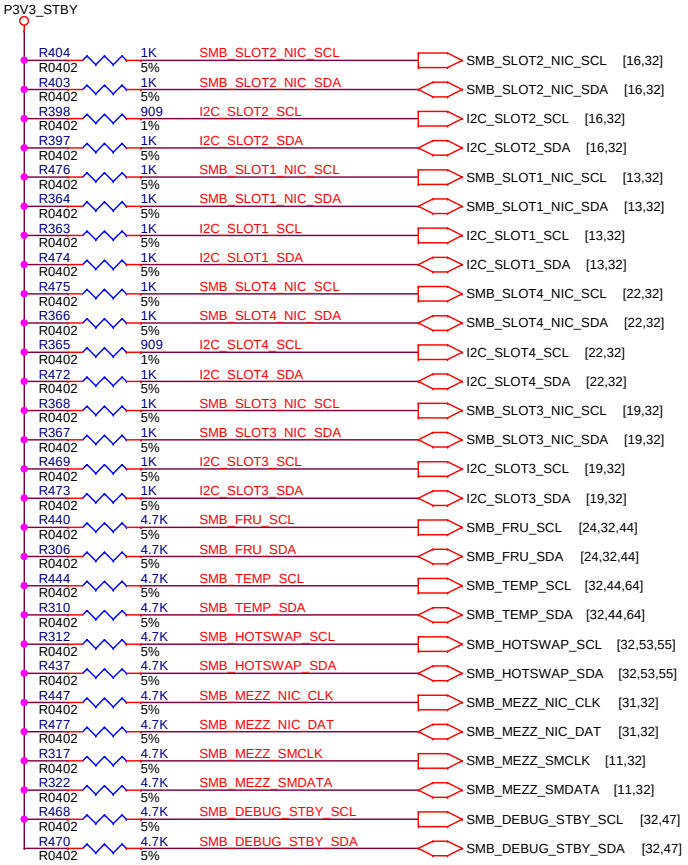
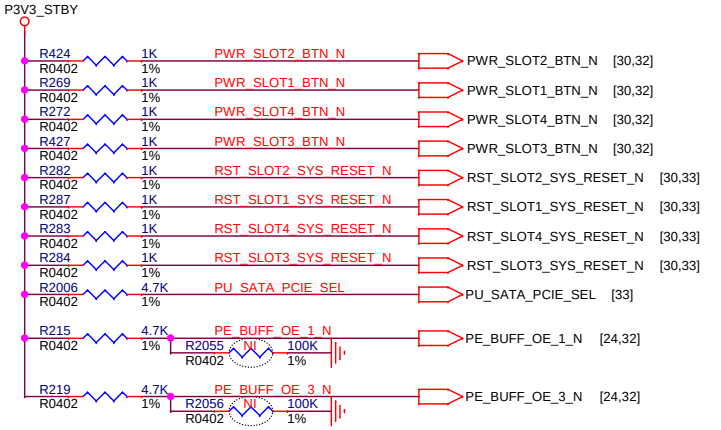
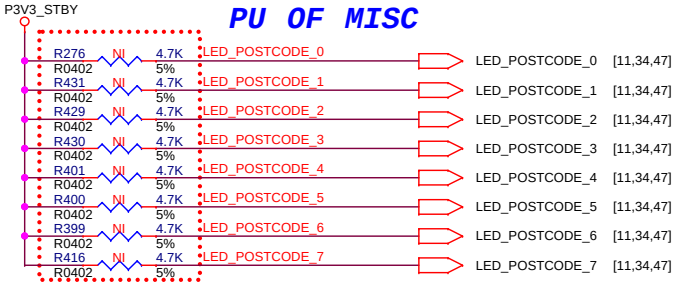
PU OF BMC SMBUS

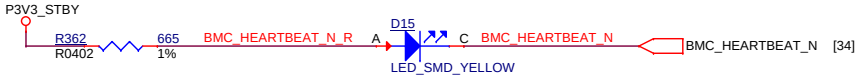




PU OF MISC



HEART BEATING LED



BMC PULL UP

<Variant Name>

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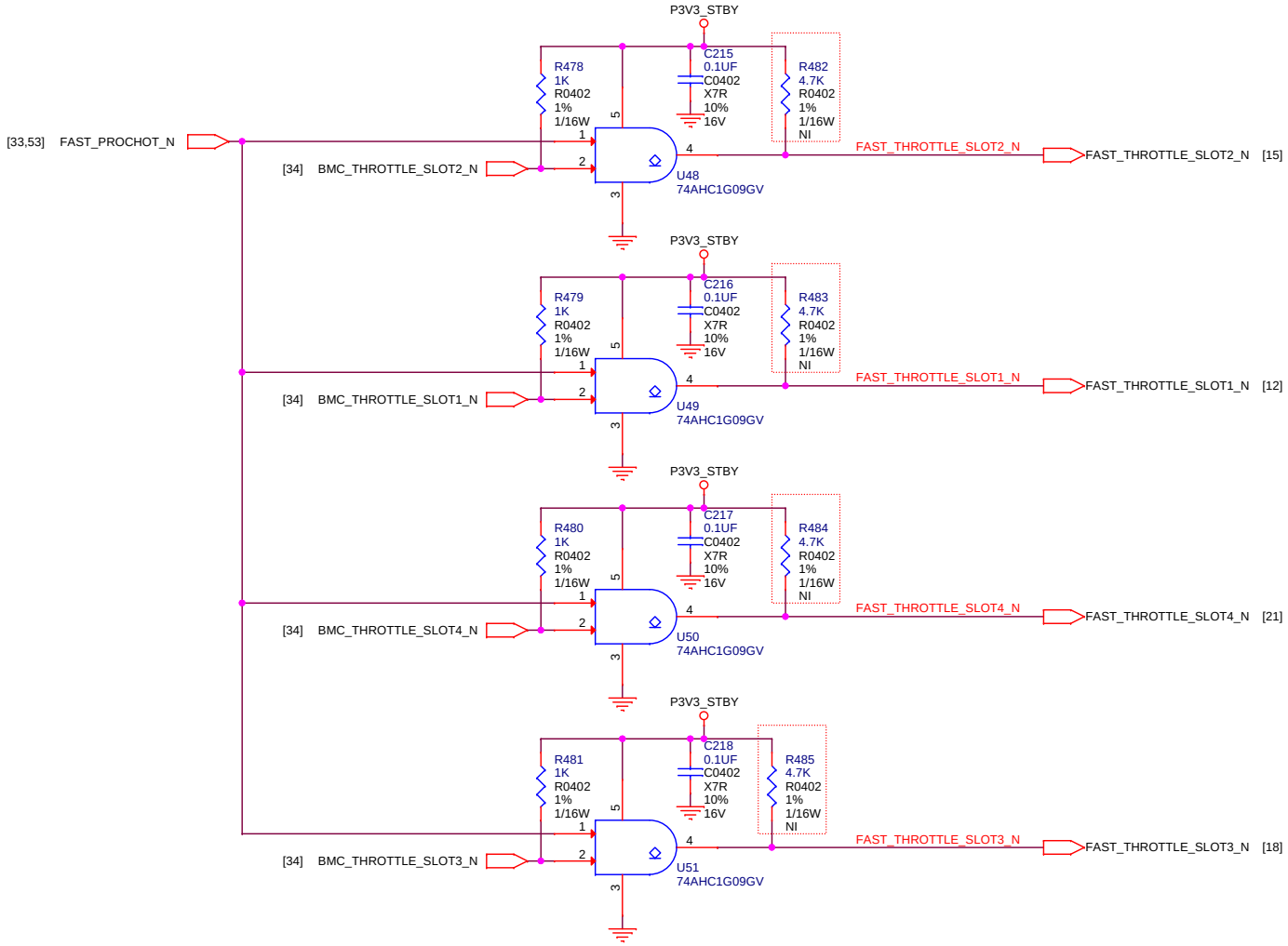
Project: F09 Baseboard_fab4	Doc Number: <Doc>		Rev: V4.00
	Page Title: BMC PULL UP		
Size: B	Date: Thursday, June 14, 2018	Sheet 36	of 69



FAST_THROTTLE_N

<Variant Name>

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Project: F09 Baseboard_fab4	Doc Number: <Doc>		Rev: V4.00
	Page Title: FAST_THROTTLE_N		
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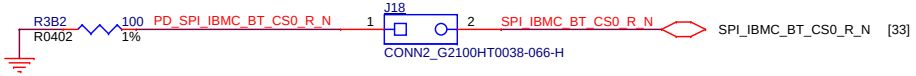
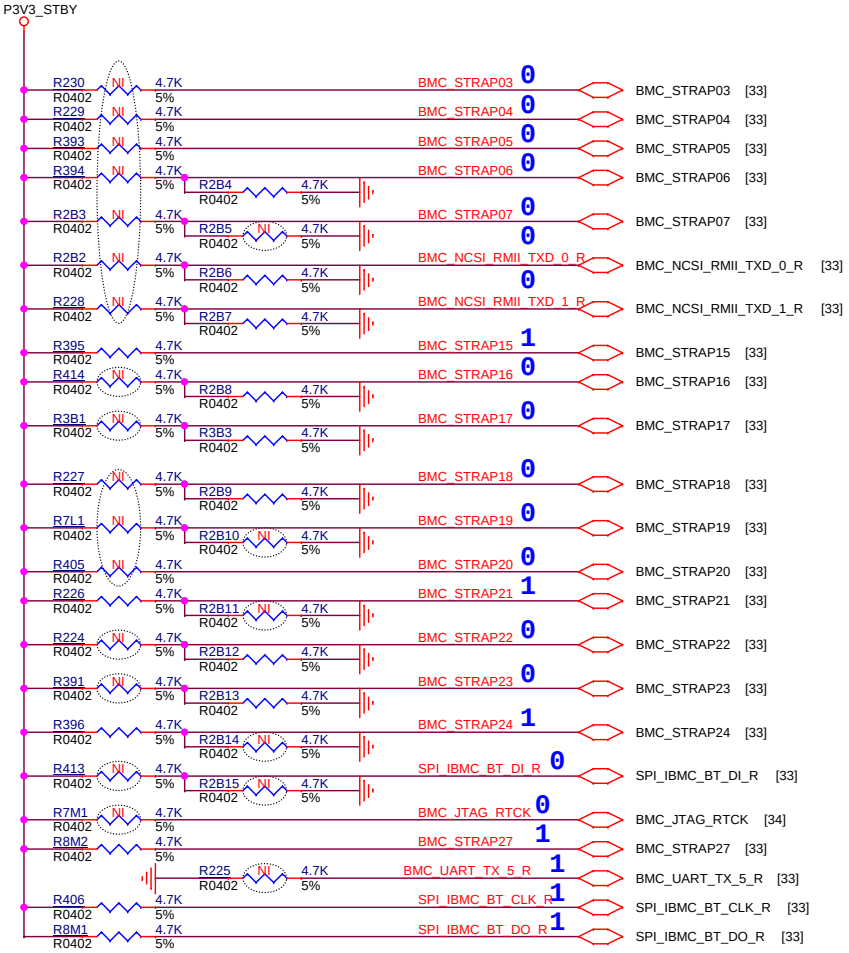
FWSPICS0#: embedded internal pull high, strap value = inverse of input
- Strap value = 0, pull high the pin to 3.3V standby power by a resistor of value 2.2K .
- Strap value = 1, pull-down the pin to ground by a resistor of value 1K ~ 4.7K .





STRAP 00
AB19
FWSPICS0#
DISABLE CPU BOOT **0**
0: ENABLE BOOT (DFLT)
1: DISABLE CPU OPERATION, WHEN NO FIRMWARE EXIST

STRAP 03
R19
GPIOS4 **0**
VGA MEMORY SIZE [3:2] (ALONG WITH SOFT STRAP 2)
00: SELECT 8MB VGA MEMORY
01: SELECT 16MB VGA MEMORY (DFLT)
11: SELECT 64MB VGA MEMORY
10: SELECT 32MB VGA MEMORY

STRAP 04
W20
GPIOS5 **0**
RESERVED (0)

STRAP 05
U20
GPIOS6 **0**
ENABLE DEICATED VGA BIOS ROM
0: NO VGA BIOS ROM, VGA BIOS IS MERGED IN THE SYSTEM BIOS (DFLT)
1: ENABLE DEDICATED VGA BIOS ROM

STRAP 06
E9
RGMII1TXCTL
DFINE MAC1 INTERFACE **0**
0: RMII/NCSI (DFLT)
1: RGMII

STRAP 07
B1
RGMII2TXCTL
DFINE MAC2 INTERFACE **0**
0: RMII/NCSI (DFLT)
1: RGMII

STRAP 12/13
F9/A5
RGMII1TXD0/RGMII1TXD1
SPI MODE SELECTION [13:12] **00**
00: DISABLE SPI INTERFACE (DFLT)
01: ENABLE SPI MASTER
10: ENABLE SPI MASTER AND SPI SLAVE TO AHB BRIDGE
11: ENABLE SPI PASS-THROUGH

STRAP 15
AA20
GPIOS7 **1**
VGA CLASS CODE SELECTION
0: SELECT THE CLASS CODE FOR VIDEO DEVICE
1: SELECT THE CLASS CODE FOR VGA DEVICE (DFLT)

STRAP 16
E7
RGMII1TXD2 **0**
SUPER-IO CONFIGURATION ADDRESS SELECTION
0: DECODE 0X2E (DFLT)
1: DECODE 0X4E

STRAP 17
U21
GPIOZ4 **0**
ENABLE BMC 2ND BOOT WATCHDOG TIMER
0: DISABLE (DFLT)
1: ENABLE TIMER START COUNTING AT POWER UP

STRAP 18
W22
GPIOZ5 **0**
SELECT USBCKI INPUT FREQUENCY
0: 24MHZ (DFLT)
1: 48MHZ

STRAP 19
D7
RGMII1TXD3
ENABLE ACPI FUNCTION **0**
0: DISABLE ACPI (DFLT)
1: ENABLE ACPI

STRAP 20
V22
GPIOZ6 **0**
DISABLE LPC TO DECODE SUPER-IO 0X2E/0X4E ADDRESS
0: ENABLE ADDRESS DECODING (DFLT)
1: DISABLE ADDRESS DECODING

STRAP 21
A2
RGMII2TXD0 **1**
ENABLE GPIOD PASS-THROUGH MODE
0: DISABLE
1: ENABLE PASS-THRU AT POWER ON (DFLT)

STRAP 22
B3
RGMII2TXD1 **0**
ENABLE GPIOE PASS-THROUGH MODE
0: DISABLE (DFLT)
1: ENABLE PASS-THRU AT POWER ON

STRAP 23
D5
RGMII2TXD2 **0**
SELECT 25MHZ REFERENCE CLOCK INPUT MODE
0: CLKIN IS 24MHZ AND USBCKI NOT USED (DFLT)
1: CLKIN IS 25MHZ AND USBCKI = 24/48MHZ

STRAP 24
D4
RGMII2TXD3 **1**
SELECT DDR4 SDRAM
0: DDR3 SDRAM
1: DDR4 SDRAM (DFLT)

STRAP 25
T18
FWSPIMISO **0**
ENABLE ESPI MODE
0: LPC MODE (DFLT)
1: ESPI MODE

STRAP 26
C9 **0**
RTCK
ENABLE ESPI FLASH MODE (BIT VALID ONLY WHEN ESPI MODE IS ENABLE)
0: ESPI RESPOND WITH NO FLASH ATTACHED (DFLT)
1: ESPI RESPOND WITH FLASH ATTACHED

STRAP 27
W21 **1**
GPIOZ7
ENABLE FAST RESET MODE FOR ARM ICE DEBUGGER
0: LONG RESET MODE, NORMAL OPERATION
1: FAST RESET MODE, FOR ICE DEBUGGER CONNECTION (DFLT)

STRAP 29
K1
TXD5 **1**
SELECT UART DEBUG PORT (IT CAN SUPPORT FIRMWARE UPDATE CAPABILITY)
0: SELECT UART1 AS BMC CONSOLE PORT
1: SELECT UART5 AS BMC CONSOLE PORT (DFLT)

STRAP 30
AA18
FWSPICK **1**
ENABLE GPIO STRAP MODE
0: DISABLE
1: ENABLE(DFLT)

STRAP 31
U17
FWSPIMOSI **1**
ENABLE SPI FLASH STRAP AUTO FETCH MODE
0: DISABLE
1: ENABLE(DFLT)

BMC HW STRAPPING

<Variant Name>

FacebookConfidential

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	Page Title: BMC HW STRAPPING		
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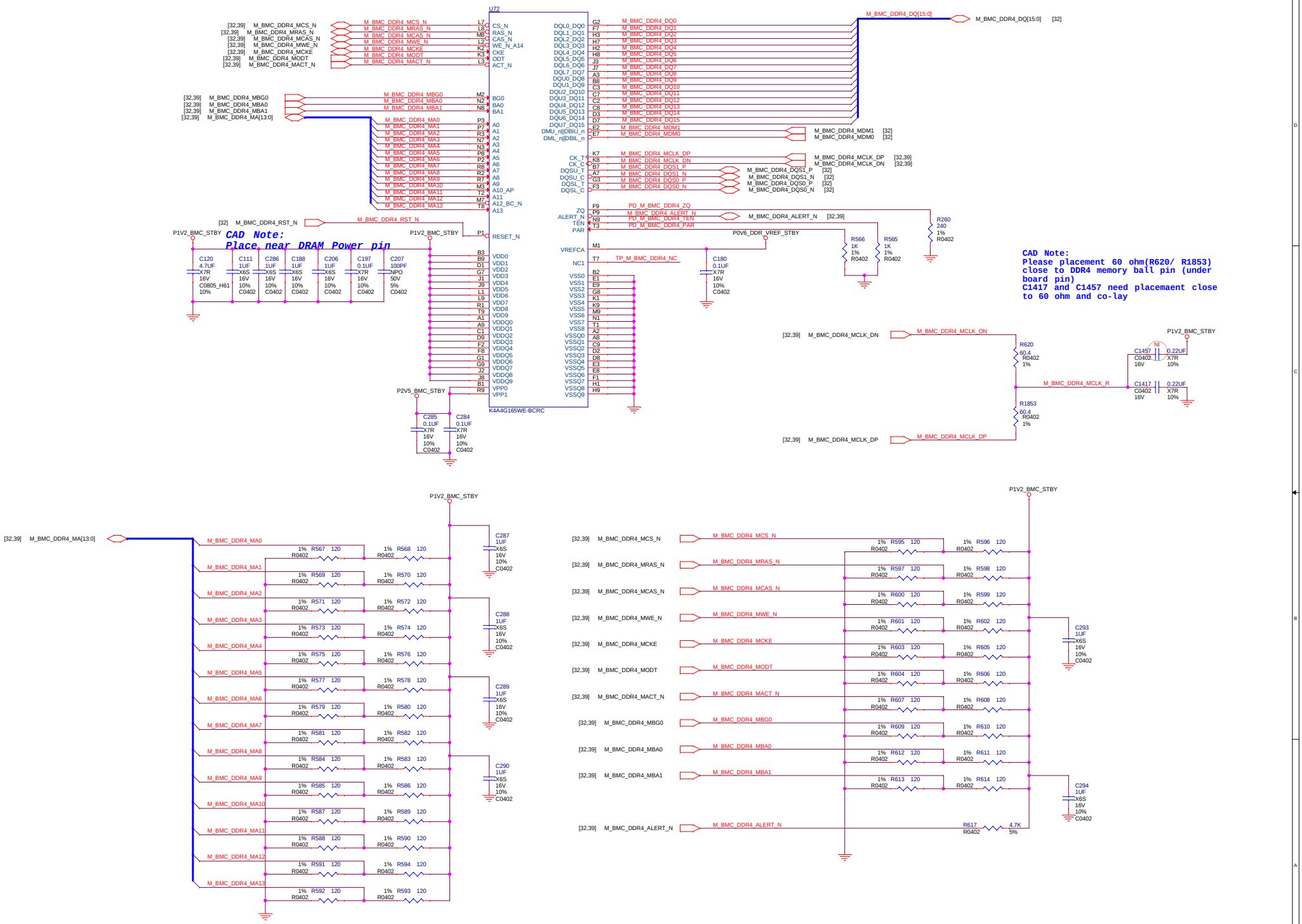

BMC DDR4 SDRAM

<Variant Name>

FacebookConfidential

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	Page Title: BMC DDR4 SDRAM		
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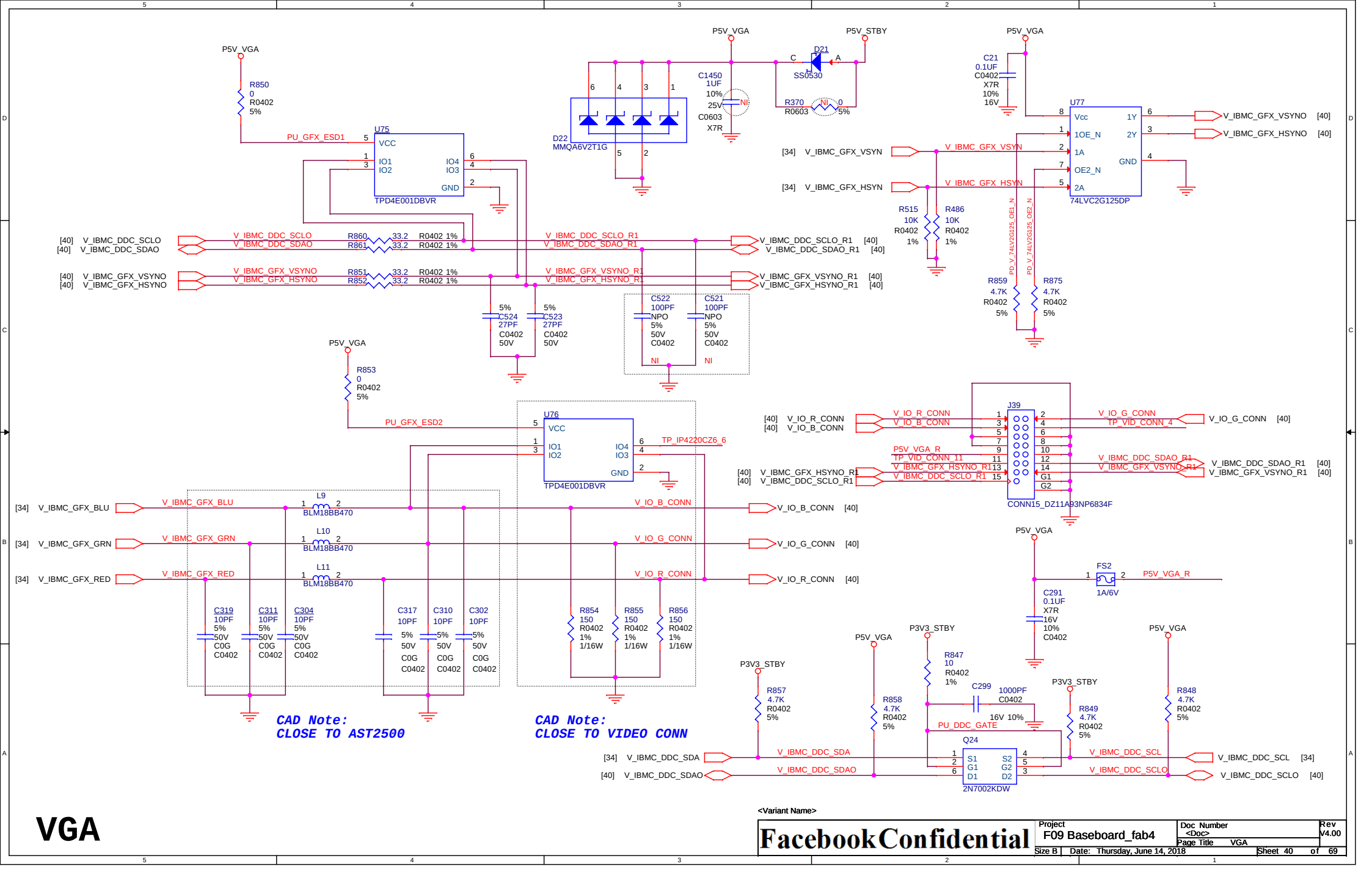

VGA

<Variant Name>

FacebookConfidential

Project	Doc Number	Rev
F09 Baseboard_fab4	<Doc>	V4.00
	Page Title VGA	
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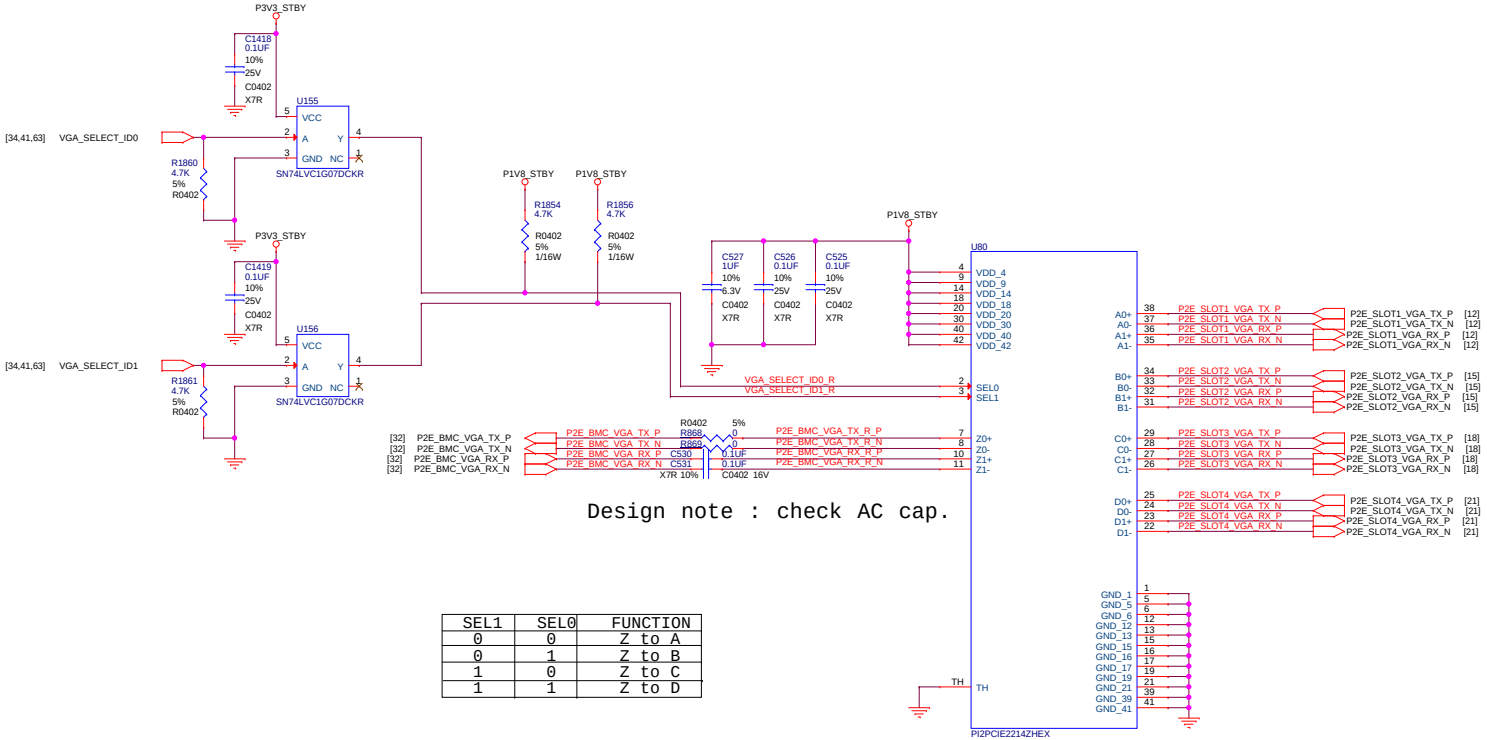
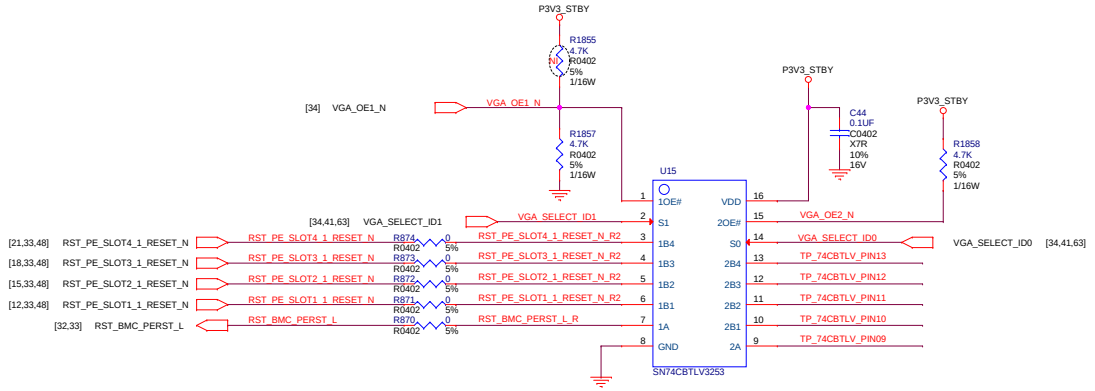
VGA PCIe mux

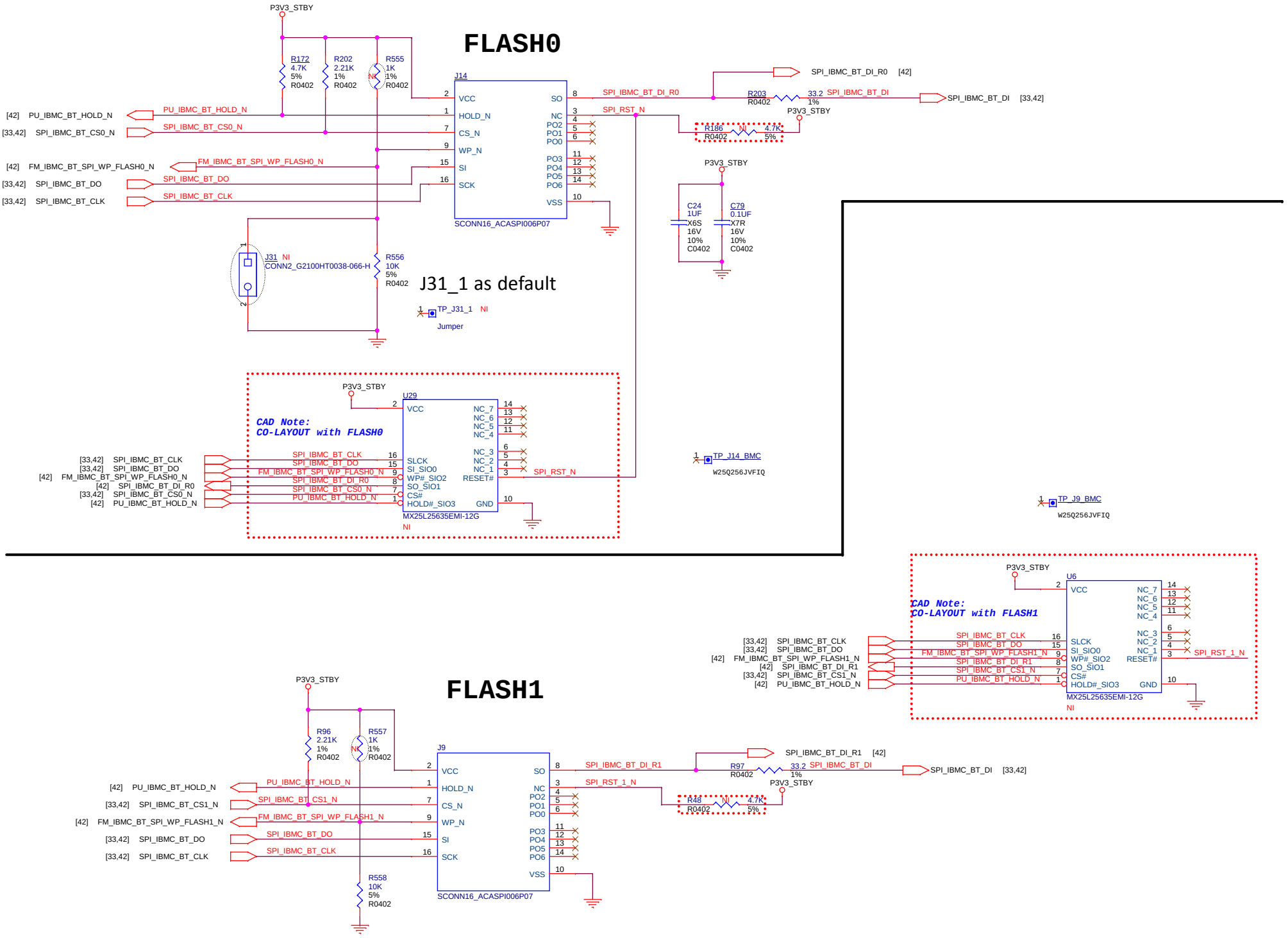


Design note : check AC cap.

SEL1	SEL0	FUNCTION
0	0	Z to A
0	1	Z to B
1	0	Z to C
1	1	Z to D



OE#	S1	S0	FUNCTION
0	0	0	A = B1
0	0	1	A = B2
0	1	0	A = B3
0	1	1	A = B4



BMC SPI FLASH

<Variant Name>

FacebookConfidential

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Size: Custom	Page Title: BMC SPI FLASH	
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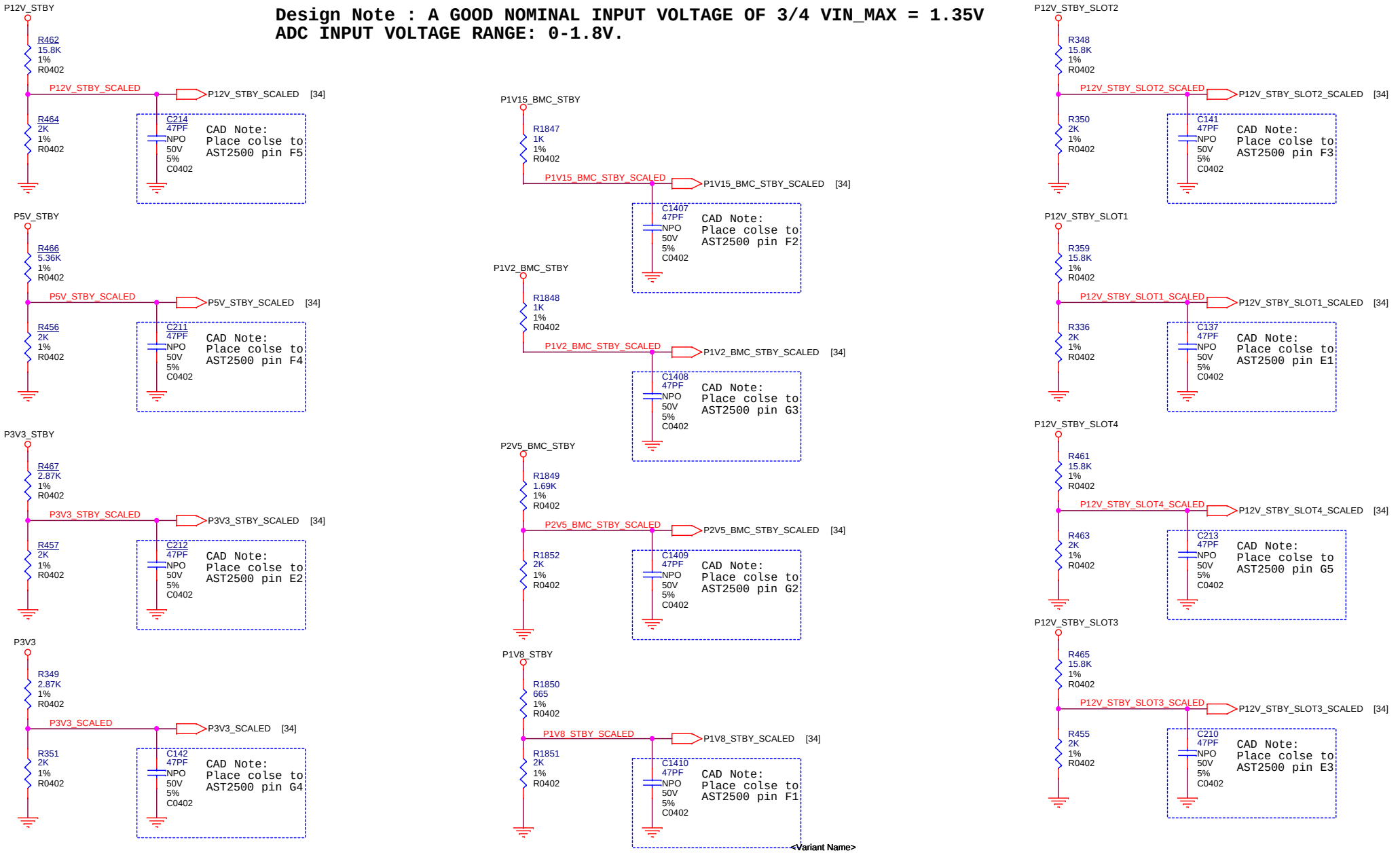
ROUTE ALL ADC NETS AT 6 MILLS WIDE

Design Note : A GOOD NOMINAL INPUT VOLTAGE OF 3/4 VIN_MAX = 1.35V
ADC INPUT VOLTAGE RANGE: 0-1.8V.



BMC VOLTAGE SENSOR

<Variant Name>

FacebookConfidential

Project: F09 Baseboard_fab4	Doc Number: <Doc>	Rev: V4.00	
	Page Title: BMC VOLTAGE SENSOR		
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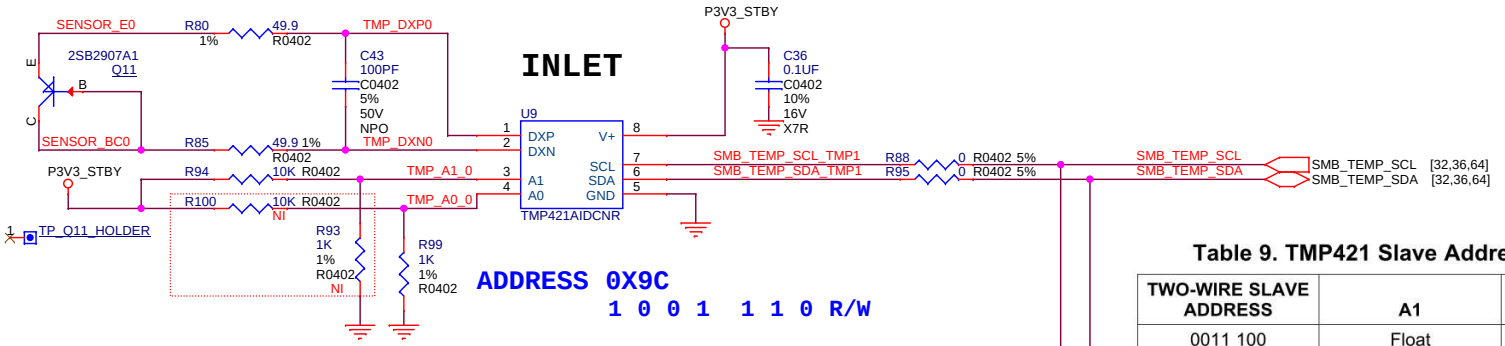

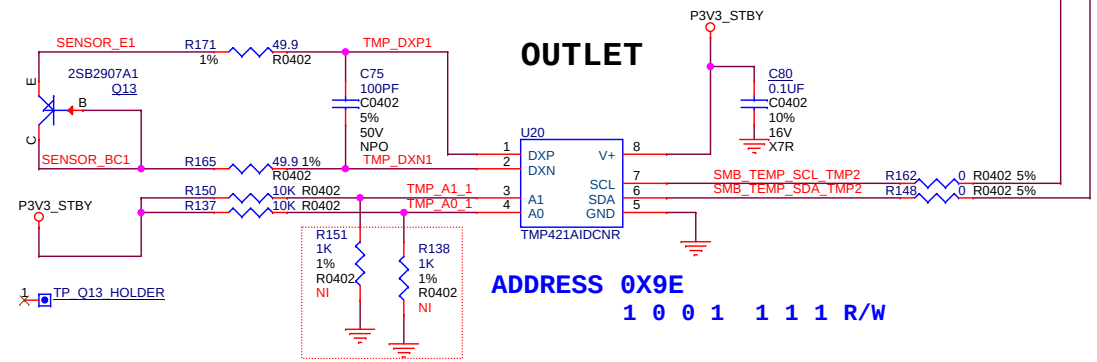

Table 9. TMP421 Slave Address Options

TWO-WIRE SLAVE ADDRESS	A1	A0
0011 100	Float	0
0011 101	Float	1
0011 110	0	Float
0011 111	1	Float
0101 010	Float	Float
1001 100	0	0
1001 101	0	1
1001 110	1	0
1001 111	1	1

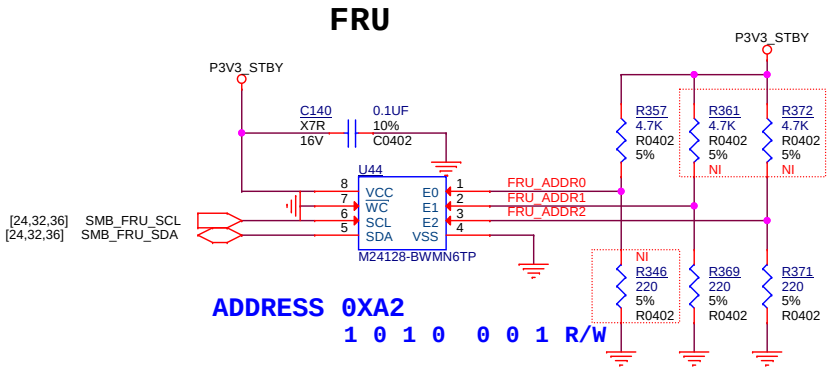

Table 2. Device Select Code

	Device Type Identifier[1]				Chip Enable Address[2]			$\overline{RW}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	E2	E1	E0	$\overline{RW}$

Note: 1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

FRU address

TEMP SENSOR / FRU

<Variant Name>

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	Page Title: TEMP SENSOR & FRU		
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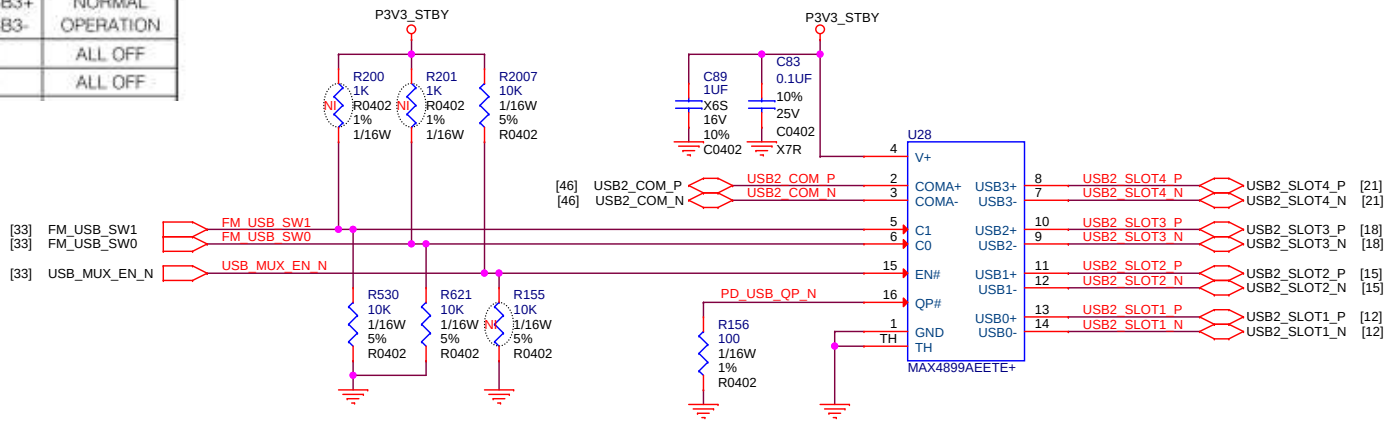
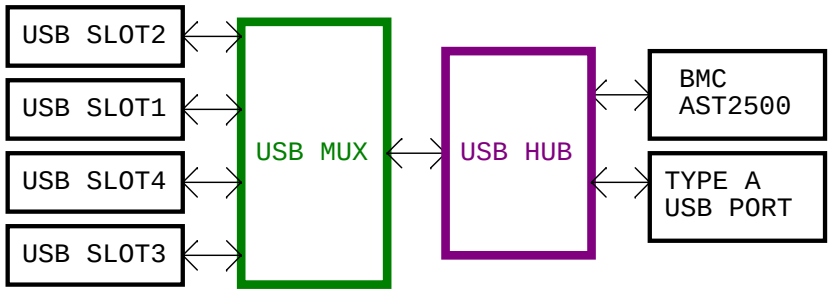
MAX4899AE					
QP	EN	C_1	C_0	FUNCTION	COMMENT
0	0	0	0	COMA+ →USB0+ COMA- →USB0-	NORMAL OPERATION
0	0	0	1	COMA+ →USB1+ COMA- →USB1-	NORMAL OPERATION
0	0	1	0	COMA+ →USB2+ COMA- →USB2-	NORMAL OPERATION
0	0	1	1	COMA+ →USB3+ COMA- →USB3-	NORMAL OPERATION
0	1	X	X	HIGH-Z	ALL OFF
1	1	X	X	HIGH-Z	ALL OFF



DESIGN NOTE:



USB MUX

<Variant Name>

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F09 Baseboard_fab4	<Doc>	V4.00
	Page Title: USB MUX	
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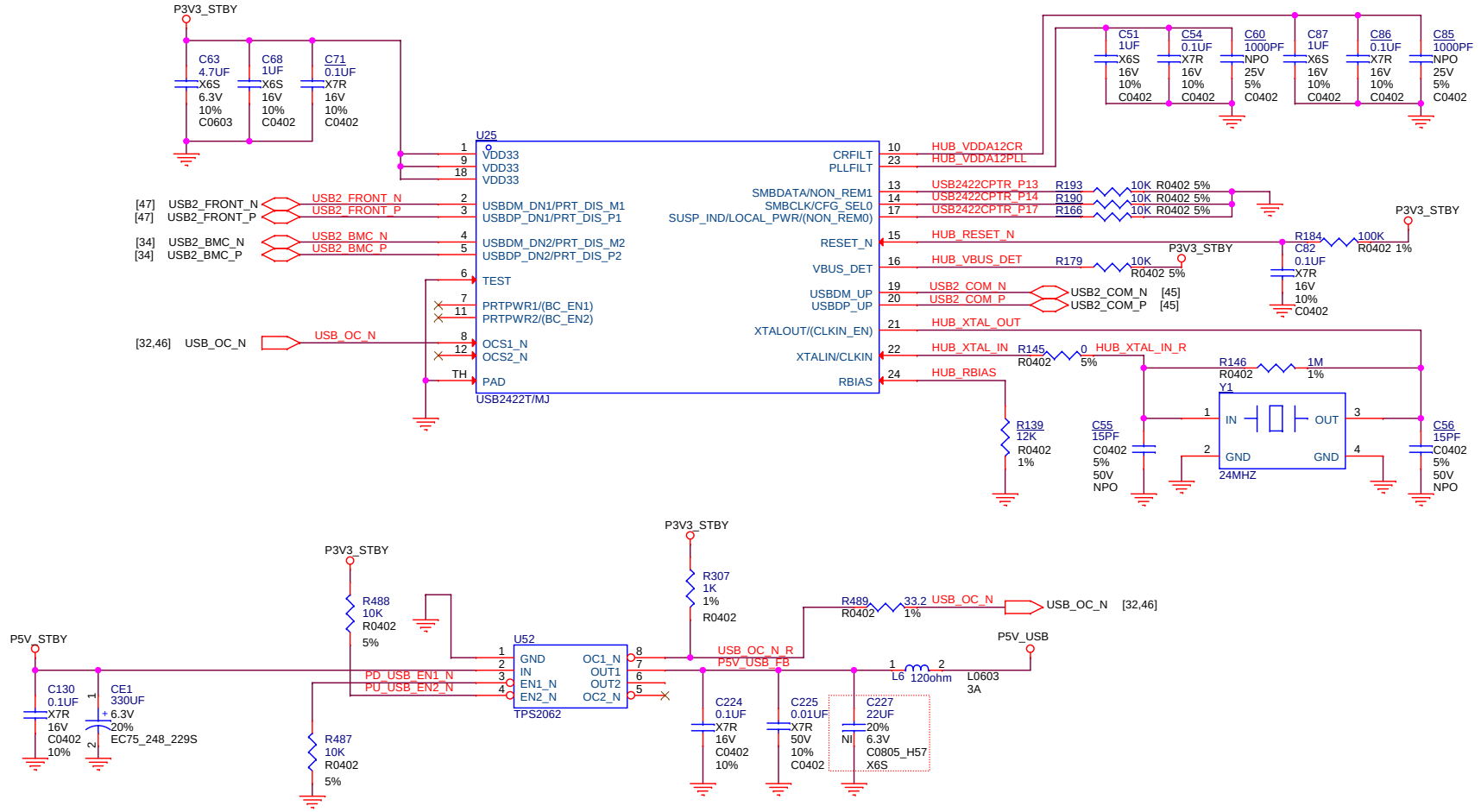

USB HUB

<Variant Name>

FacebookConfidential

Project F09 Baseboard_fab4	Doc Number <Doc>		Rev V4.00
	Page Title USB HUB		
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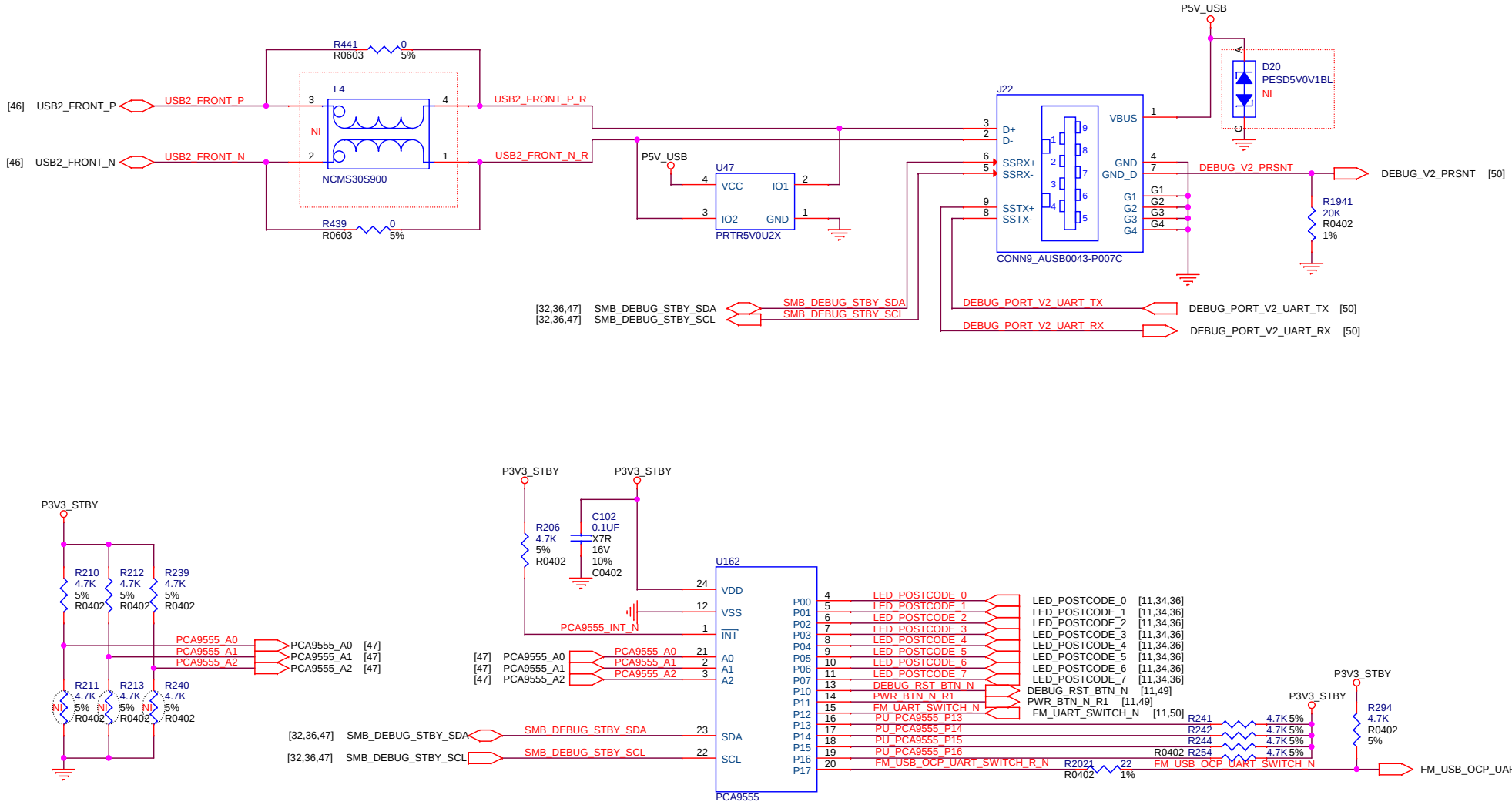

PCA9555 ADDRESS: 0X4E [0 1 0 0 A2 A1 A0 0]

USB3.0 CONN

<Variant Name>

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	Page Title: SELECT SWITCH		
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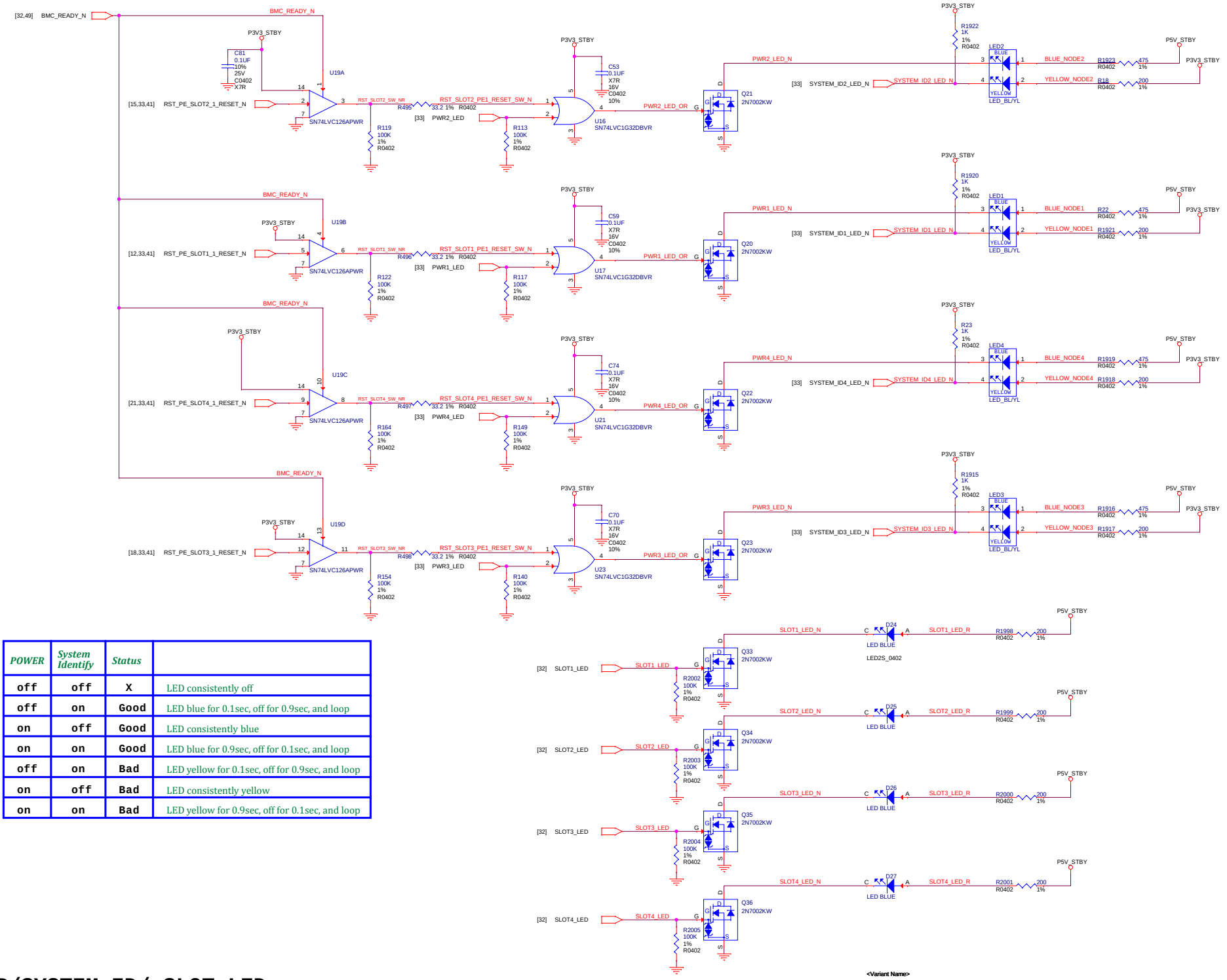

POWER	System Identify	Status	
off	off	X	LED consistently off
off	on	Good	LED blue for 0.1sec, off for 0.9sec, and loop
on	off	Good	LED consistently blue
on	on	Good	LED blue for 0.9sec, off for 0.1sec, and loop
off	on	Bad	LED yellow for 0.1sec, off for 0.9sec, and loop
on	off	Bad	LED consistently yellow
on	on	Bad	LED yellow for 0.9sec, off for 0.1sec, and loop

PWR/SYSTEM_ID/ SLOT LED

<Variant Name>

Project	F09 Baseboard_fab4
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Page Title	PWR/SYSTEM_ID LED
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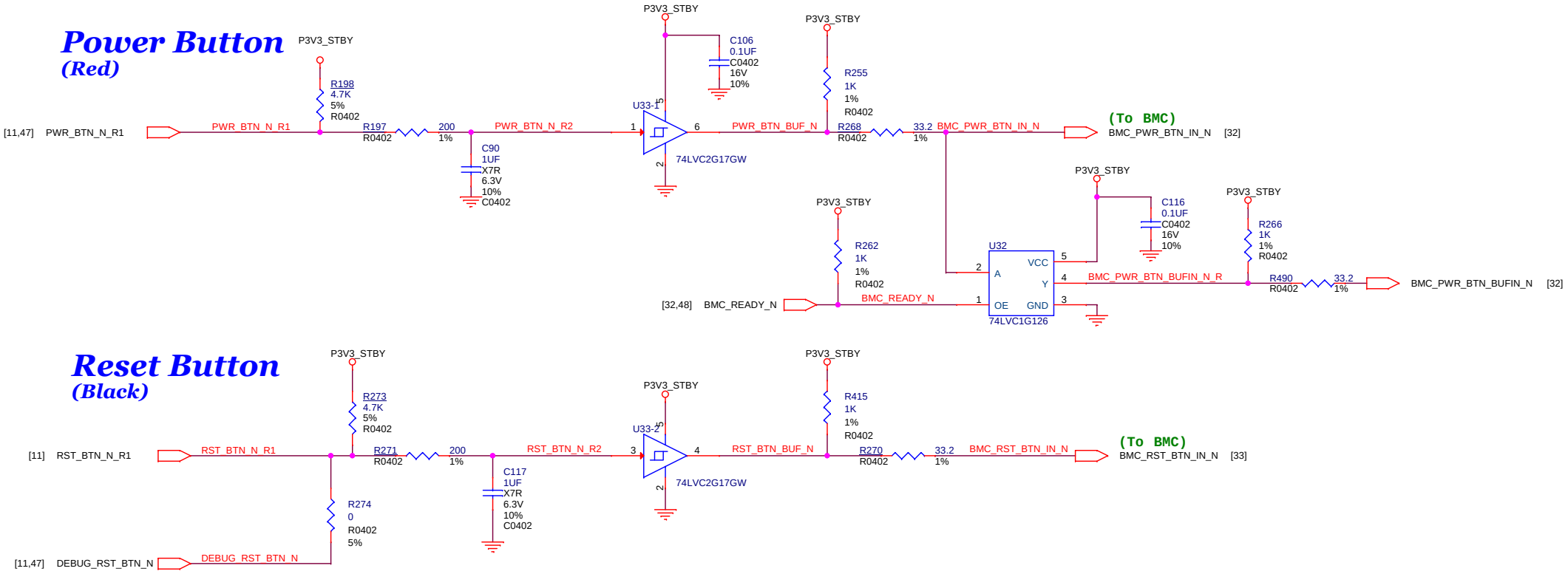

PWR/RST BUTTON

<Variant Name>

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Project: F09 Baseboard_fab4		Doc Number: <Doc>	Rev: V4.00
		Page Title: PWR/RST/SELECT BUTTON	
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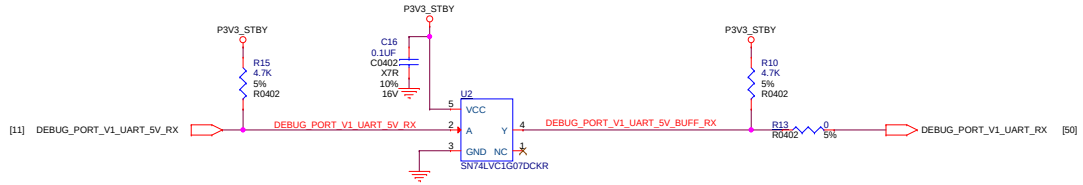
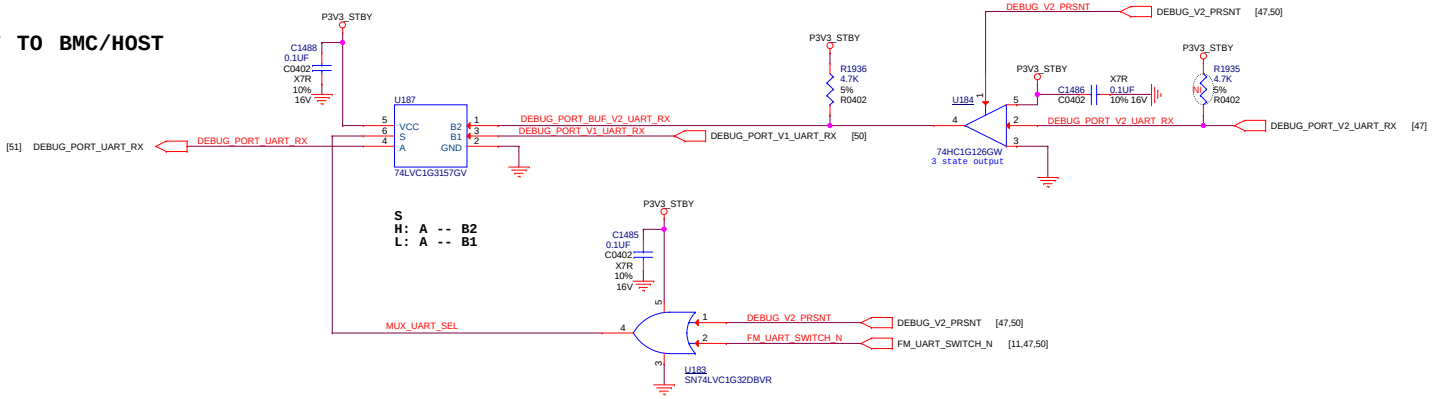
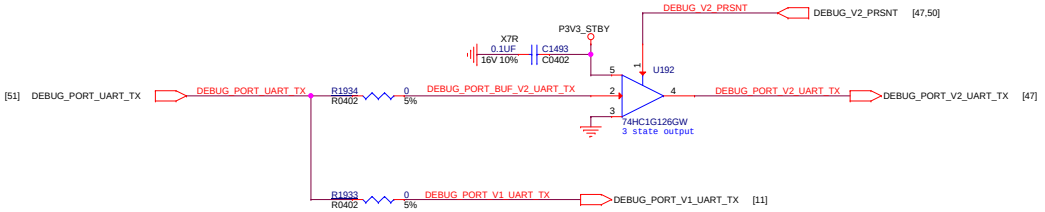


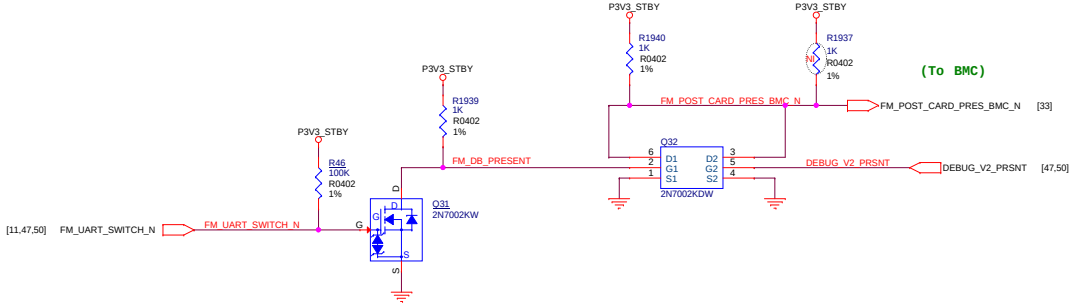
UART TO BMC/HOST



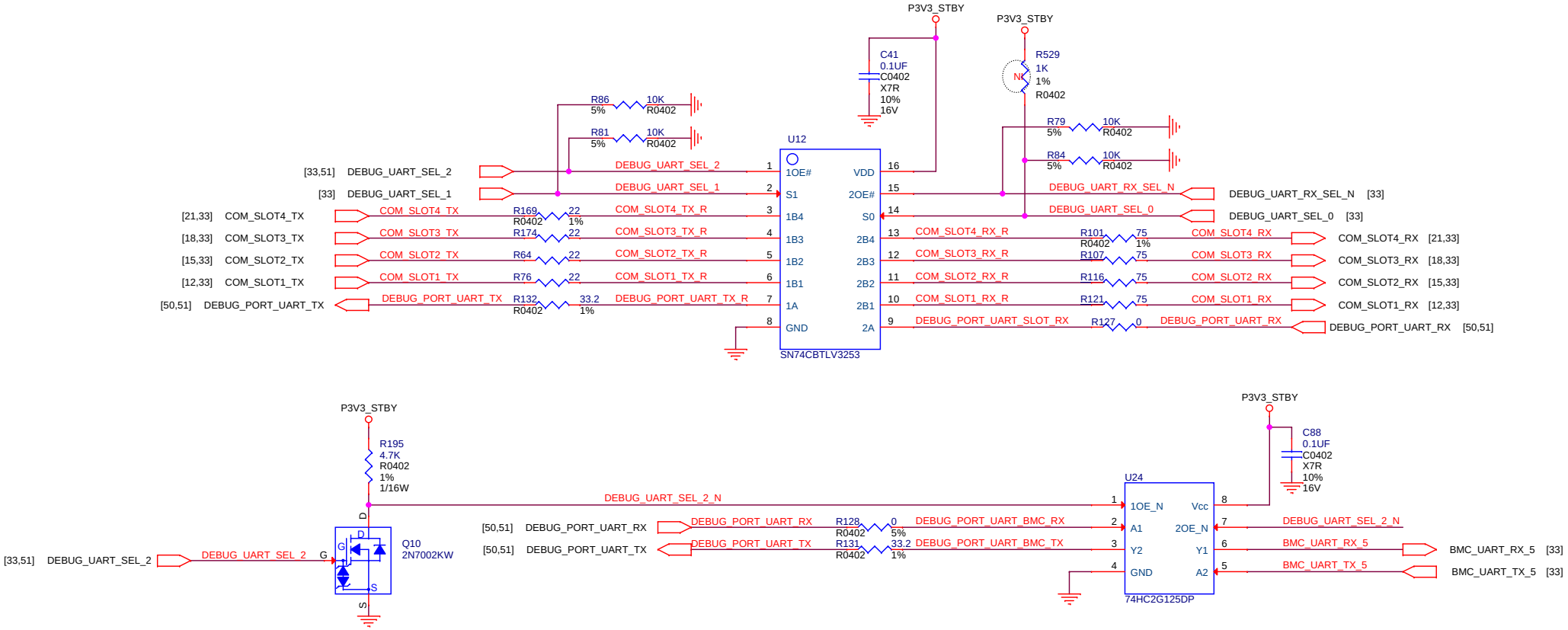
Status	FM_UART_SWITCH_N	DEBUG_V2_PRSNT	UART
V1(un-stuff)/ V2(un-stuff)	1	0	X
V1(stuff)/ V2(un-stuff)	0	0	DEBUG_PORT_V1_UART_RX
V1(un-stuff)/ V2(stuff)	1	1	DEBUG_PORT_V2_UART_RX
V1(stuff)/ V2(stuff)	0	1	DEBUG_PORT_V2_UART_RX

UART FROM BMC/HOST





DEBUG



SEL_2	*SEL_1*	*SEL_0*	*RX_SEL_N*	
0	0	0	0	SLOT1
0	0	1	0	SLOT2
0	1	0	0	SLOT3
0	1	1	0	SLOT4
0	X	X	1	SLOT RX Disable
1	0	0	1	BMC Debug

UART select table

UART

<Variant Name>

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	Page Title: UART		
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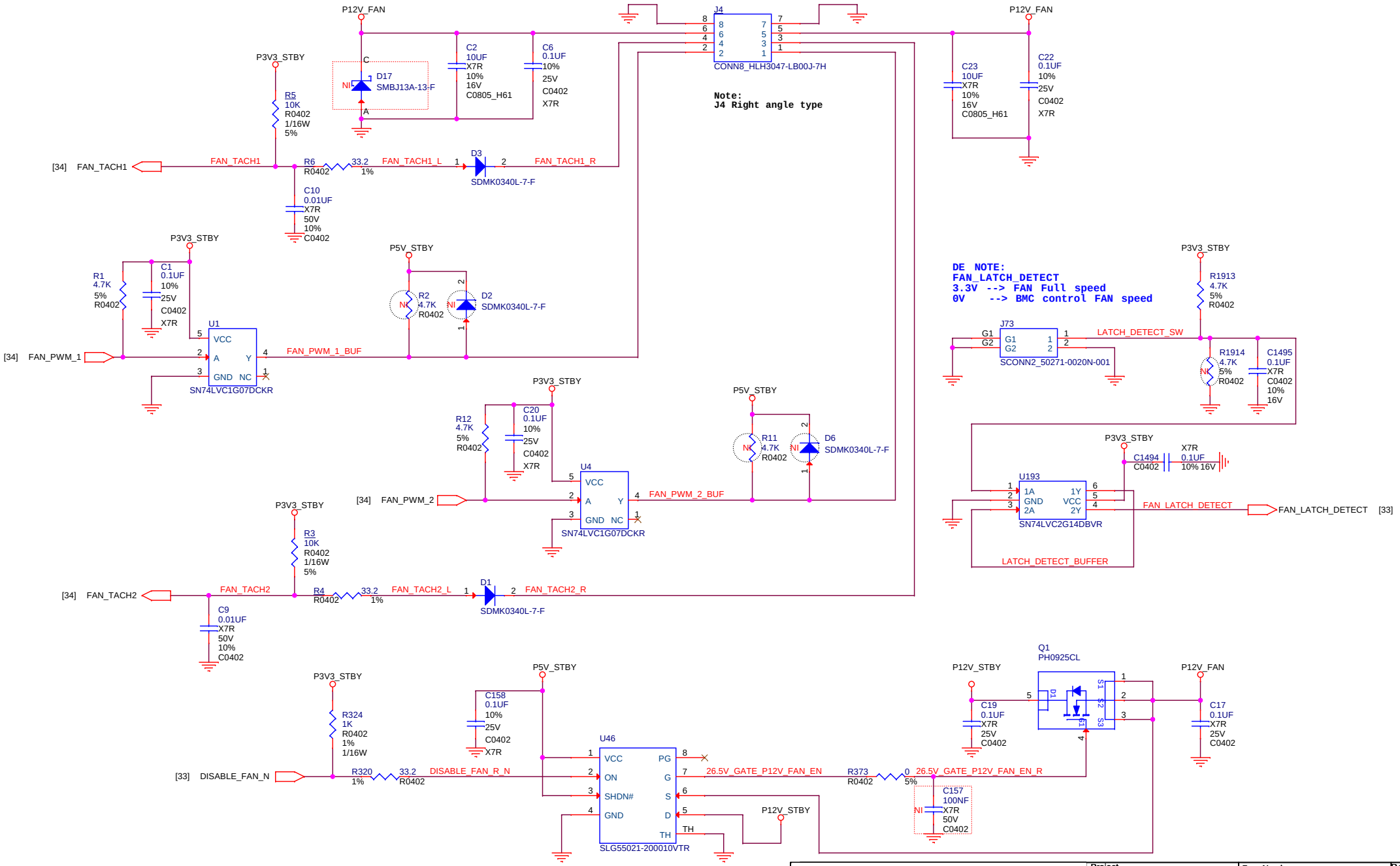

FAN CONN

<Variant Name>	Project: F09 Baseboard_fab4	Doc Number: <Doc>	Rev: V4.00
		Page Title: FAN CONN	
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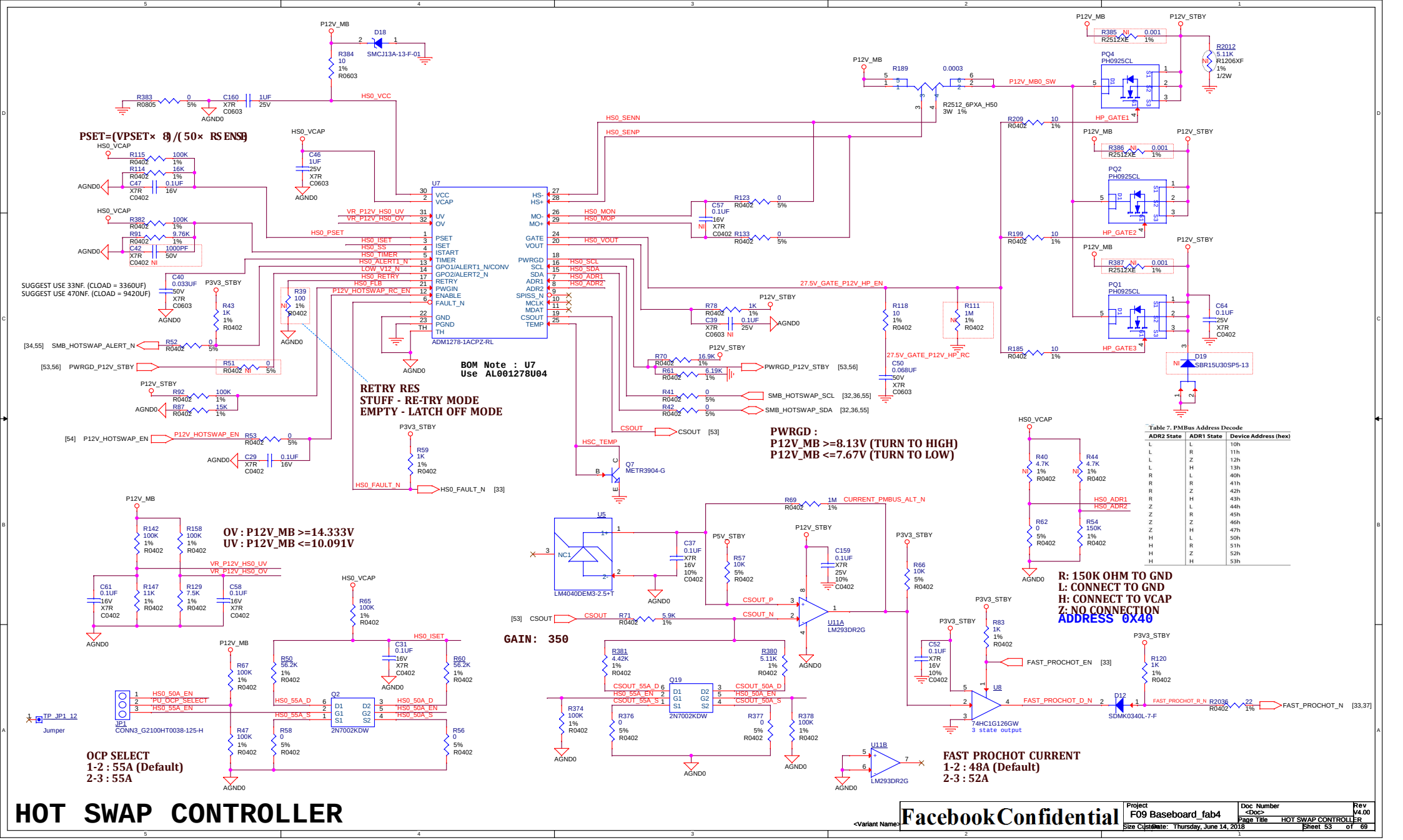

HOT SWAP CONTROLLER

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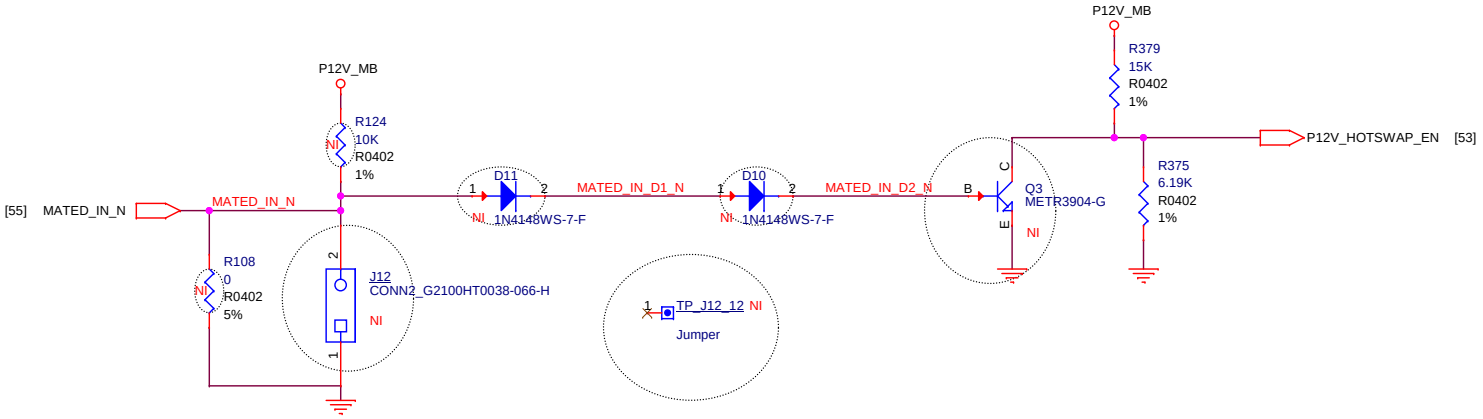
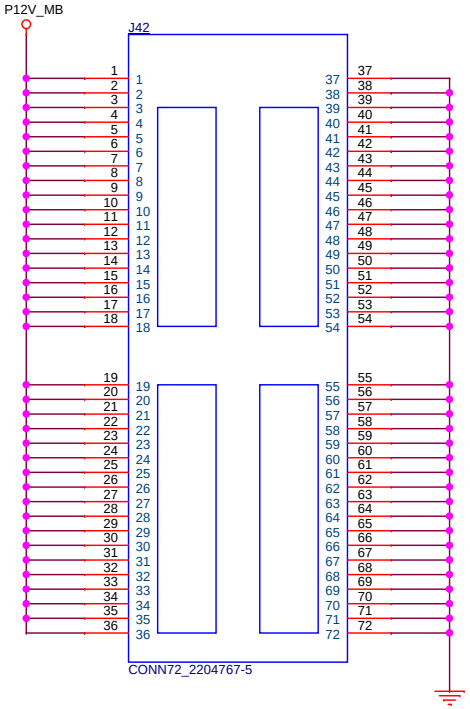
<Variant Name>	





BOM Note :
J42 change to DFAC04FS013
DFAC04FS013 (TYC hard tooling/ hybrid gold planting 13mm)
DFAC04FS008 (TYC hard tooling/ overall gold planting)
DFAC04FS009 (TYC hard tooling/ gold planting 2mm)
DFAC04FS011 (APL hard tooling/ hybrid gold planting 13mm)
DFAC04FS006 (APL hard tooling/ overall gold planting)
DFAC04FS007 (APL hard tooling/ gold planting 2mm)

POWER CONN

<Variant Name>

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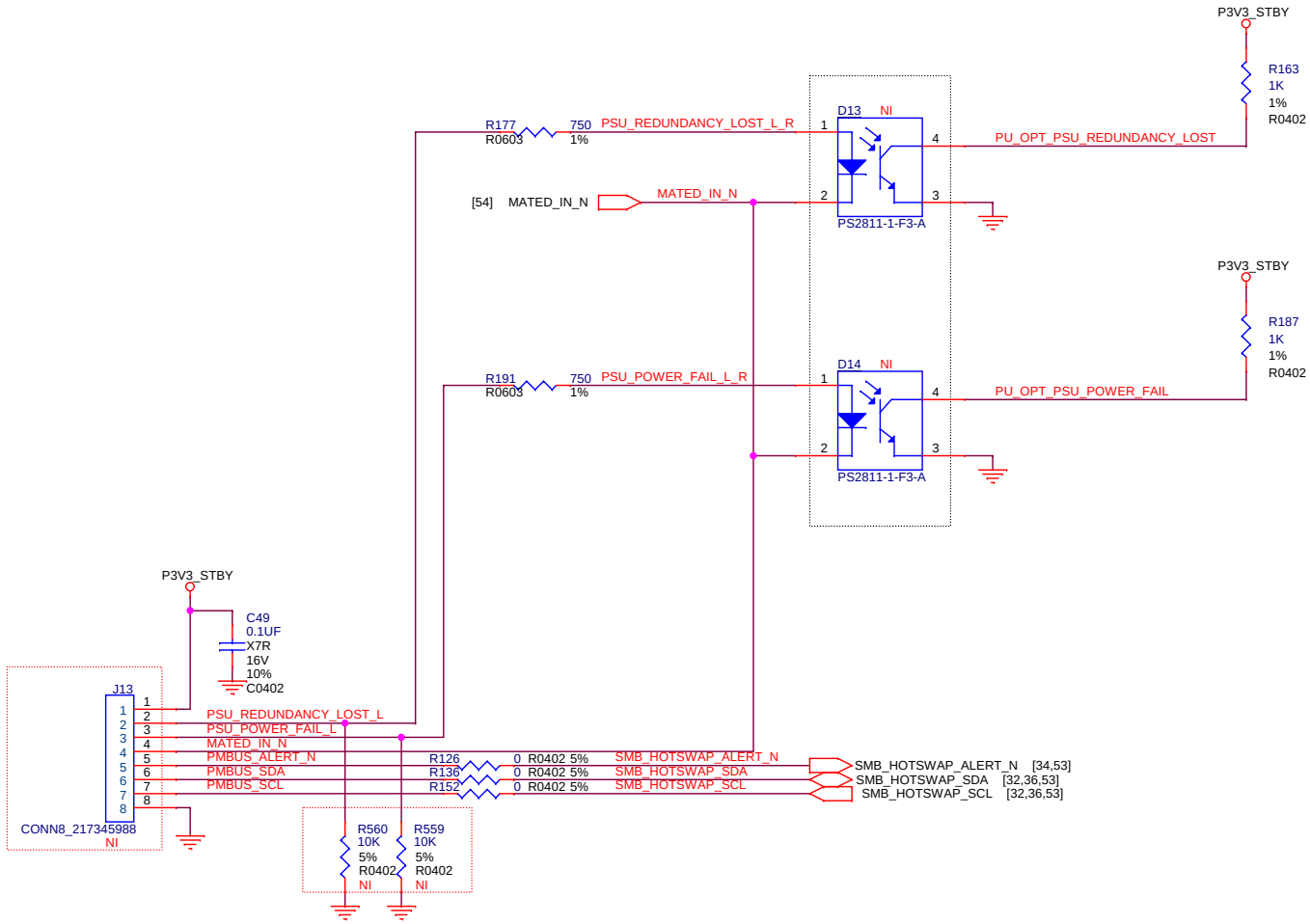

Power Side Band

<Variant Name>

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	Page Title: Power Side Band		
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Design specification

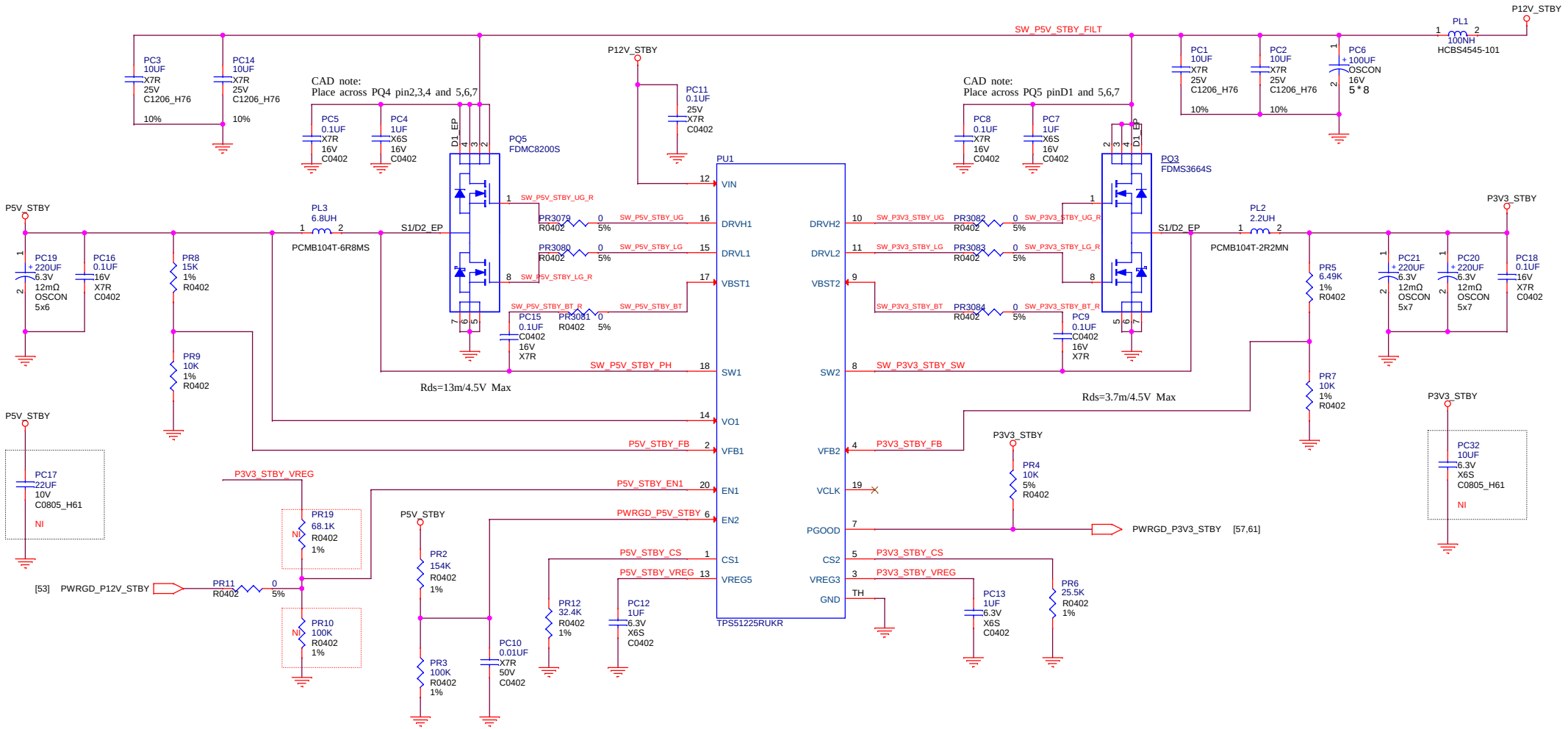
P5V_STBY

Output Voltage = 5V± 5 %
Output Ripple & Noise ± 0 5 %
Transient Tolerance = 500mV
TDC = 3A
Max current = 3A
Over-Current Protection(Max Rating × 1 5) = 4 5A
Slew Rate = 1.0A/us
Work Frequency = 300kHZ
Efficiency > 85% @TDC

Design specification

P3V3_STBY

Output Voltage = 3V3± 5 %
Output Ripple & Noise ± 0 5 %
Transient Tolerance = 330mV
TDC = 8.2A
Max current = 8.2A
Over-Current Protection(Max Rating × 1 5) =12 3A
Slew Rate = 1.0A/us
Work Frequency = 355kHZ
Efficiency > 85% @TDC



VR P5V_STBY & P3V3_STBY

<Variant Name>

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		<Doc>	V4.00
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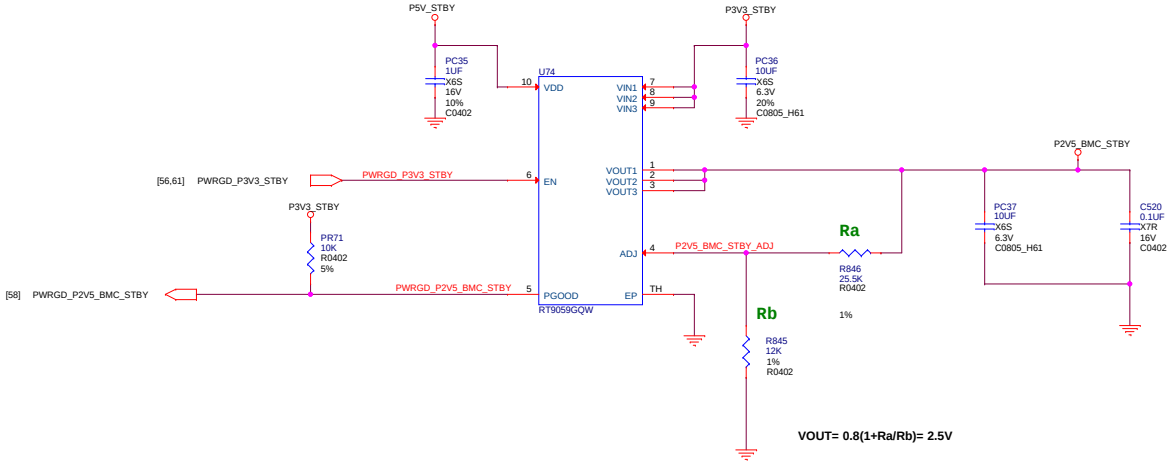
Design specification

Output Voltage = 2.5V± - 5 %
Output Ripple & Noise ± 0 5 %
Transient Tolerance = 250mV
Max current = 0.3A
PD = (3.3V - 2.5V) * 0.3A = 0.24W

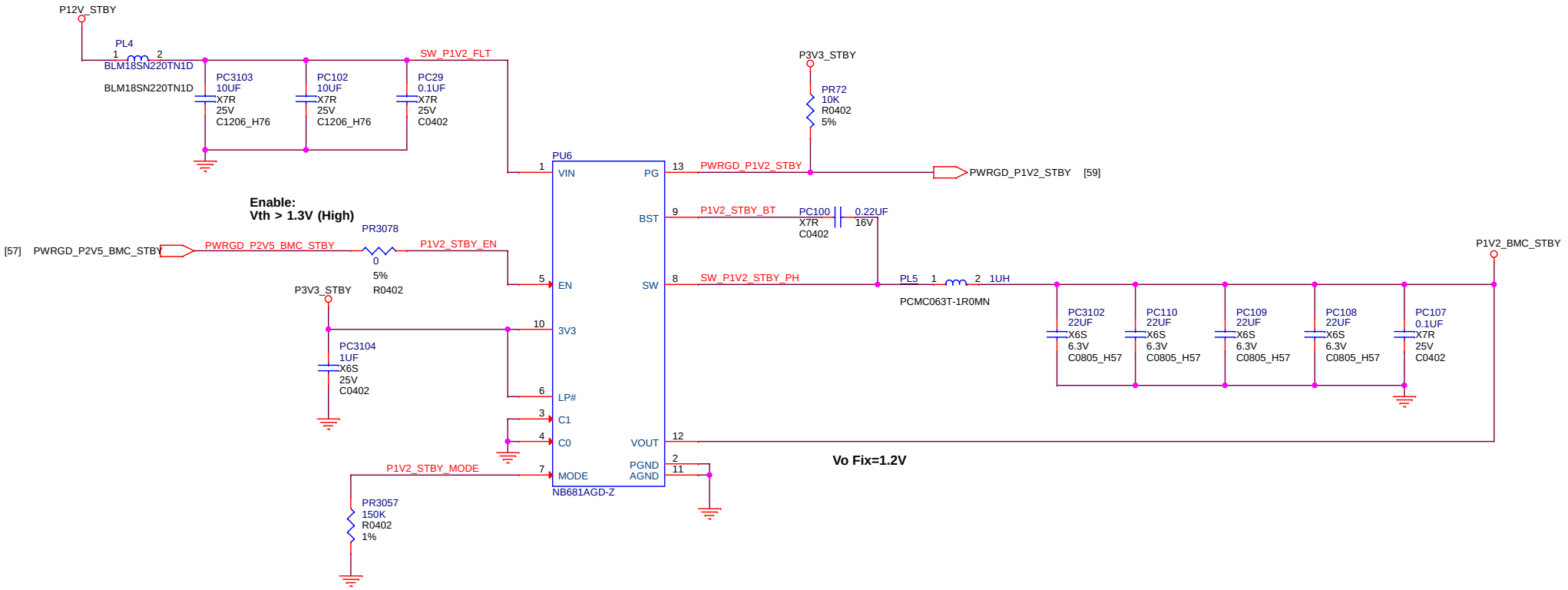


VR P2V5_BMC_STBY

<Variant Name>

Design specification

Output Voltage = 1.2V± 5 %
Output Ripple & Noise ± 2 %
Transient Tolerance = 120mV
TDC =1.114A
Max current =1.114A
Over-Current Protection(IC Rating) = 7A
Current Step = 0.5A
Slew Rate = 0.5A/us
Work frequency = 750KHZ
Efficiency > 85% @TDC



VR P1V2_BMC_STBY

<Variant Name>

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Project: F09 Baseboard_fab4		Doc Number: <Doc>	Rev: V4.00
		Page Title: VR P1V538_STBY & P1V26_STBY	
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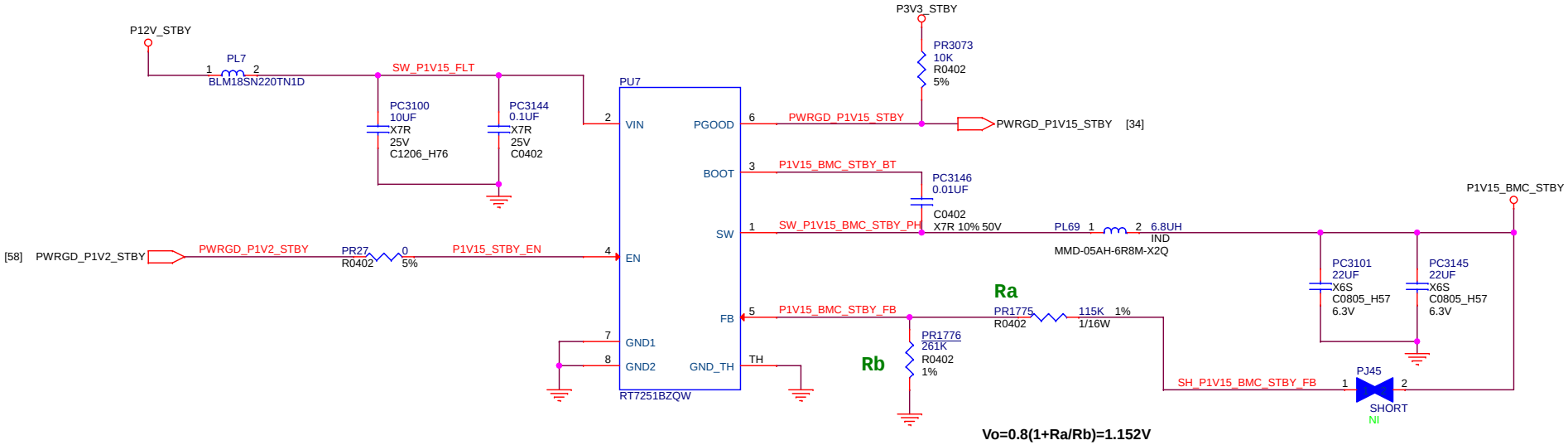
P1V15_BMC_STBY Design specification

Output Voltage = 1.15V± 5 %
Output Ripple & Noise ± 1 %
Transient Tolerance = 115mV
TDC = 0.619A
Max current = 0.619A
Over-Current Protection(IC Rating) = 2.6A
Current Step = 0.619A
Slew Rate = 2.5A/us
Work frequency = 800KHZ
Efficiency > 80% @TDC



VR P1V15_BMC_STBY

<Variant Name>

FacebookConfidential

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		Page Title: P1V15_STBY VR	
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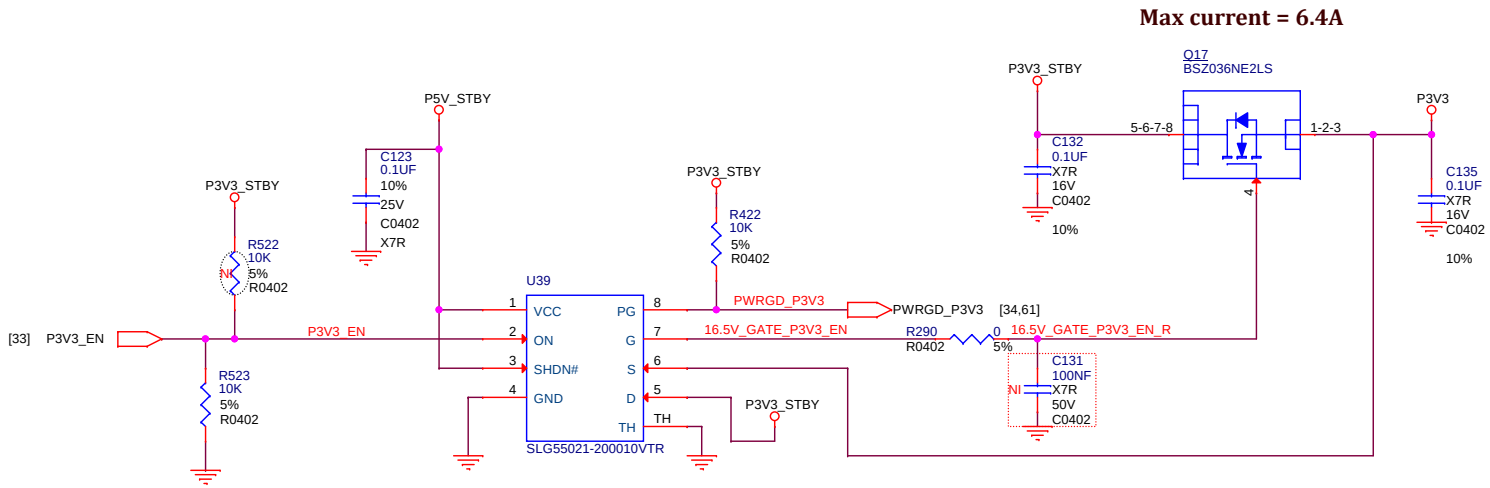

P3V3 Power Switch

<Variant Name>

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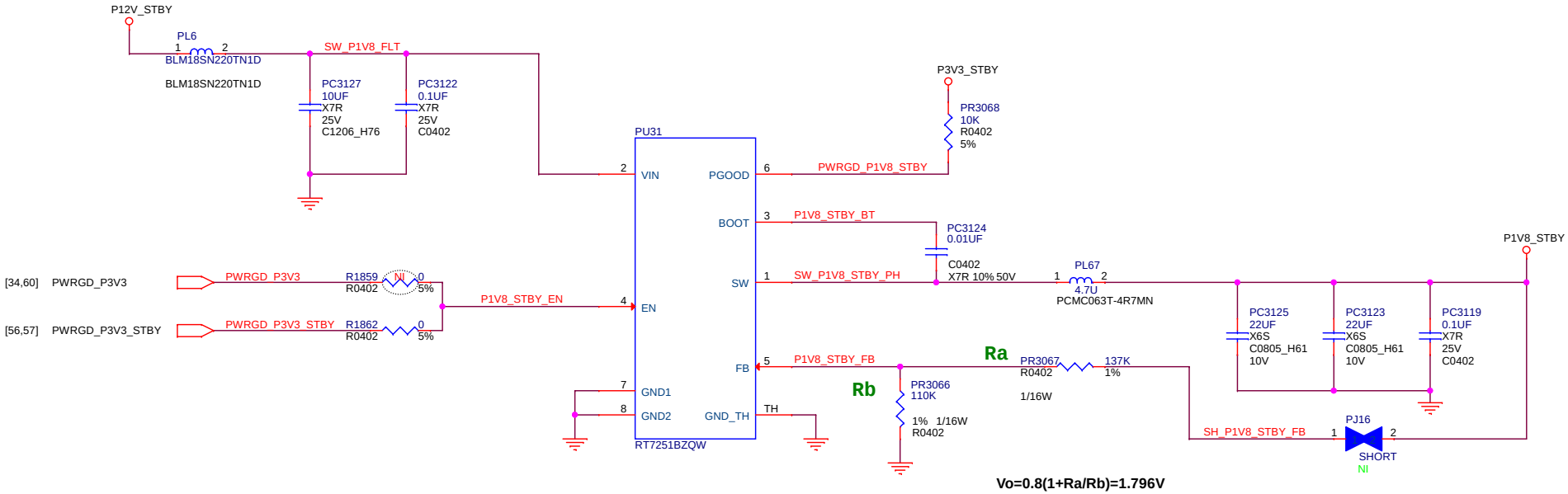
P1V8 Design specification

Output Voltage = 1.8V± 5 %
Output Ripple & Noise ± 1 %
Transient Tolerance = 180mV
TDC = 0.3A
Max current = 0.3A
Over-Current Protection(IC Rating) = 2.6A
Current Step = 0.25A
Slew Rate = 0.25A/us
Work frequency = 800KHZ
Efficiency > 80% @TDC



VR P1V8_STBY

<Variant Name>

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BLANK

SMBus MUX

<Variant Name>

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Function Tables

Table 3A. nOEA Configuration Table

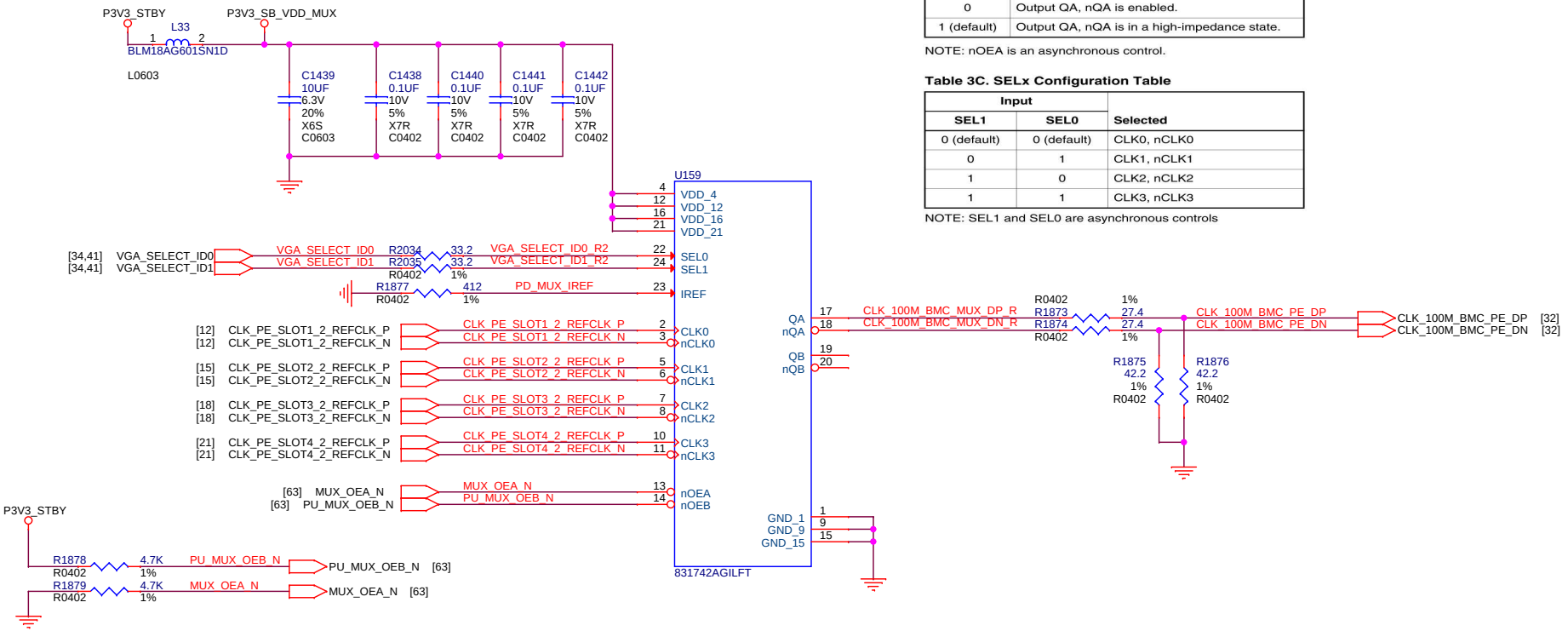
Input	
nOEA	**Operation**
0	Output QA, nQA is enabled.
1 (default)	Output QA, nQA is in a high-impedance state.

NOTE: nOEA is an asynchronous control.

Table 3C. SELx Configuration Table

Input		
SEL1	**SEL0**	**Selected**
0 (default)	0 (default)	CLK0, nCLK0
0	1	CLK1, nCLK1
1	0	CLK2, nCLK2
1	1	CLK3, nCLK3

NOTE: SEL1 and SEL0 are asynchronous controls



100MHz Clock MUX

<Variant Name>

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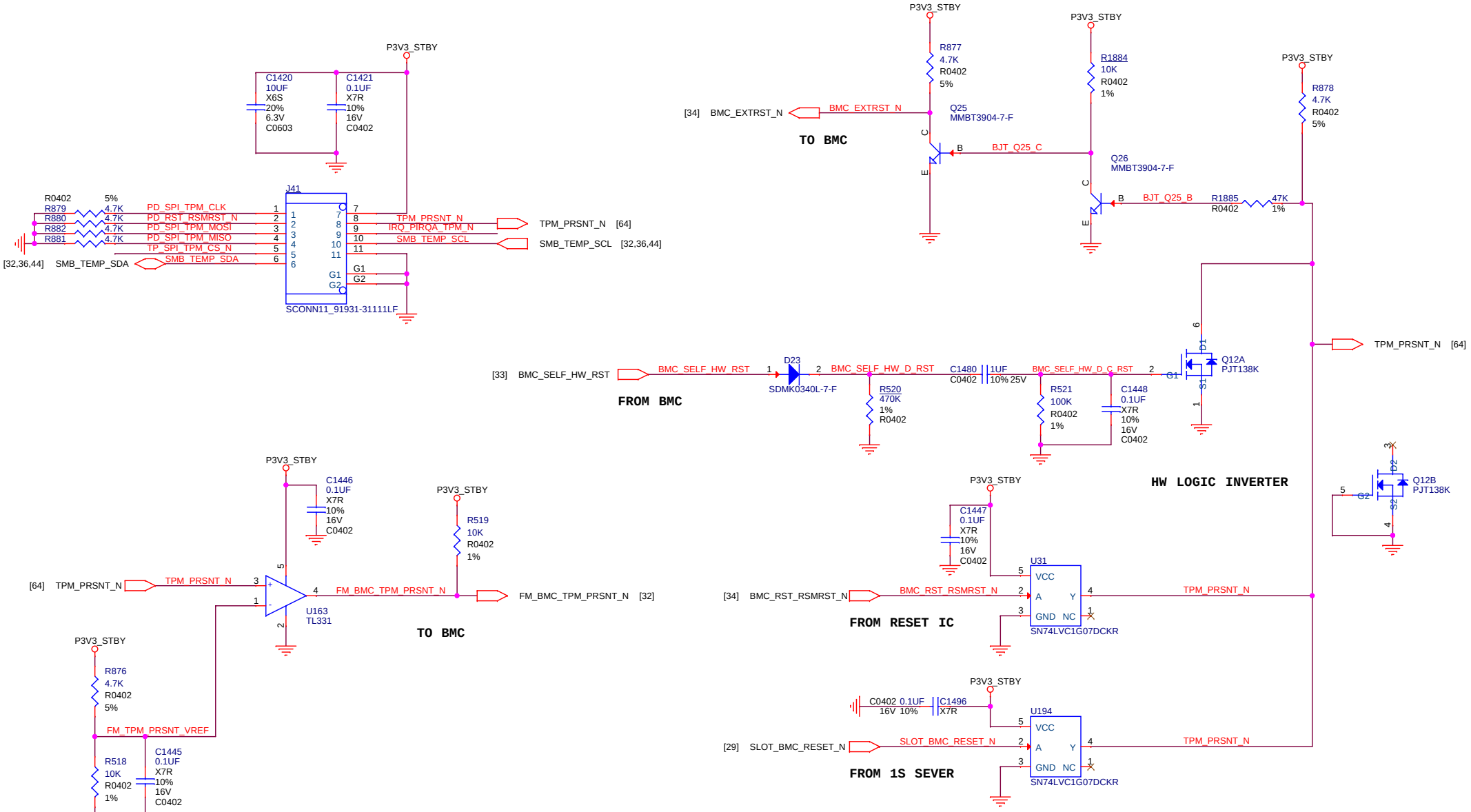

DE NOTE:
1. remove PCH_BMC_RST_N, because F09 baseboard doesn't have PCH
2. change BMC_SELF_HW_RST from F08 AST2500 Pin U22 to F09 AST2500 Pin T22

TPM connector

<Variant Name>

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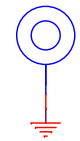
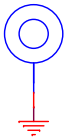
SMT THUMB SCREW * 1pcs

H9
HOLE_C10-2D5-6B10_OB12XC5B_NPB

1 TP_H9_SCREW
FBF09108010



H22
HOLE_C6D3-4B6_NPB



1 TP_H22_NUT

1 TP_TPM_SCREW
MS30040I250
NI

For TPM module

Key Holes * 14pcs

H10
HOLE_C6-8D3-2_7-2B10-8_OB8XC5-4_NPM_SPD

H11
HOLE_C6-8D3-2_7-2B10-8_OB8XC5-4_NPM_SPD

H12
HOLE_C6-8D3-2_7-2B10-8_OB8XC5-4_NPM_SPD

H13
HOLE_C6-8D3-2_7-2B10-8_OB8XC5-4_NPM_SPD

H14
HOLE_C6-8D3-2_7-2B10-8_OB8XC5-4_NPM_SPD

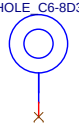
H6
HOLE_C6-8D3-2_8-2B10-8_OB8XC5-9T_C5-4B_NPM_SPD

H7
HOLE_C6-8D3-2_8-2B10-8_OB8XC5-9T_C5-4B_NPM_SPD

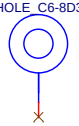
H15
HOLE_C6-8D3-2_8-2B10-8_OB8XC5-9T_C5-4B_NPM_SPD

H16
HOLE_C6-8D3-2_8-2B10-8_OB8XC5-9T_C5-4B_NPM_SPD

H17
HOLE_C6-8D3-2B6-8N_CUTA_NPM



H18
HOLE_C6-8D3-2B6-8N_CUTA_NPM



ICT Holes * 2pcs

H23
D2-54N

H24
D2-54N

Mechanical

<Variant Name>

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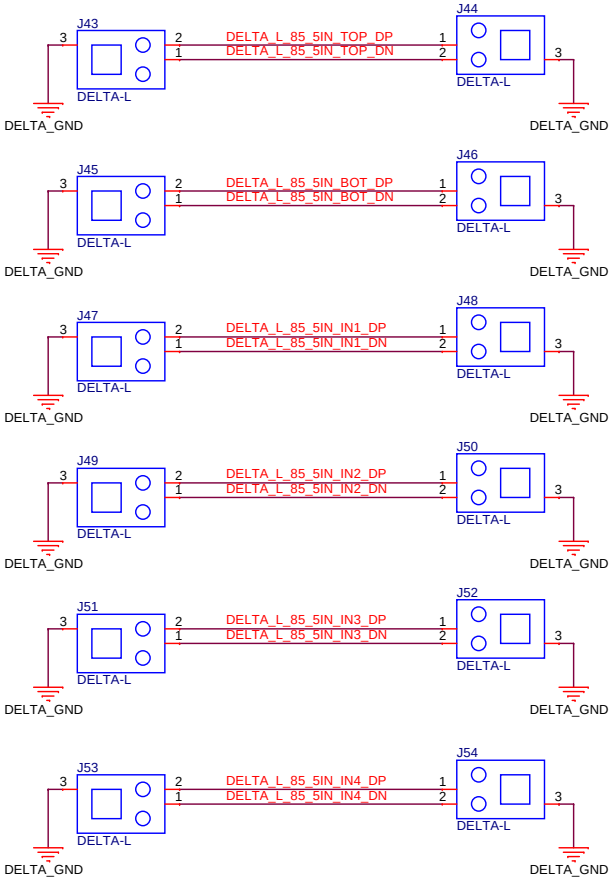
5 INCH



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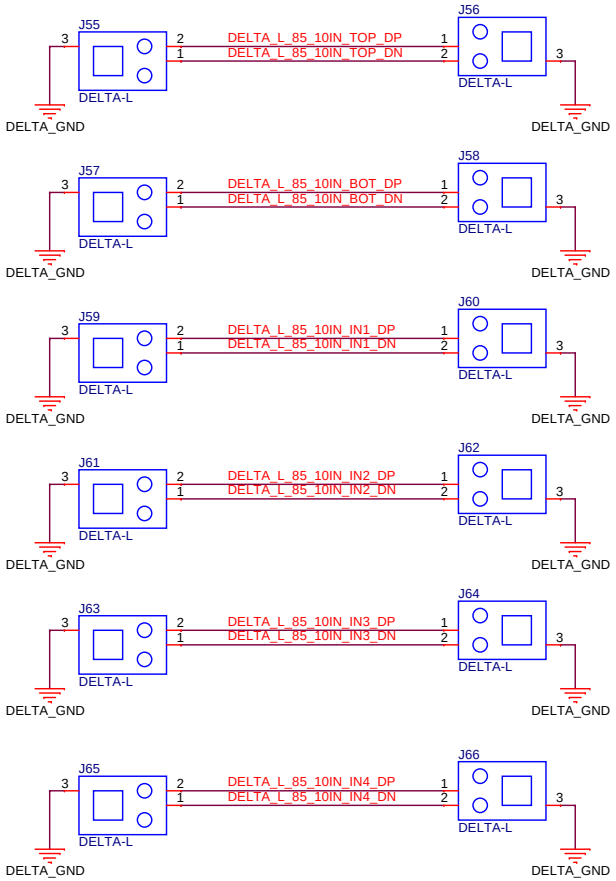

DELTA-L

<Variant Name>

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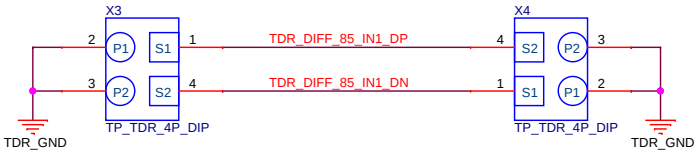

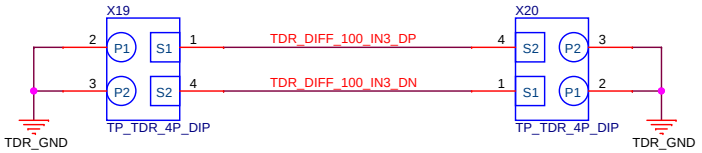

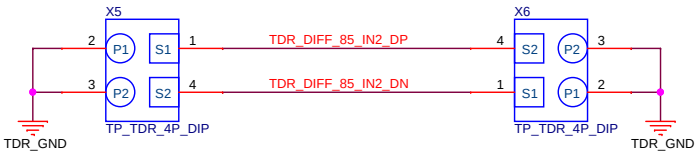

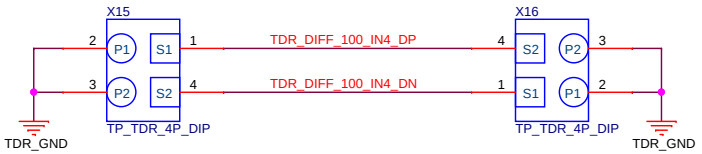

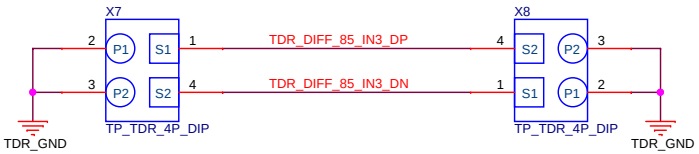

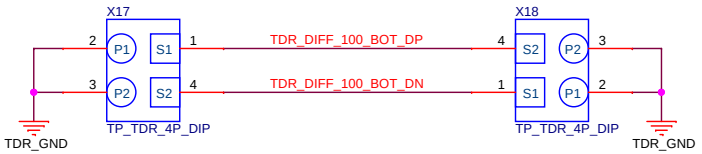

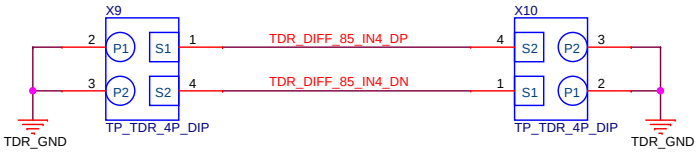

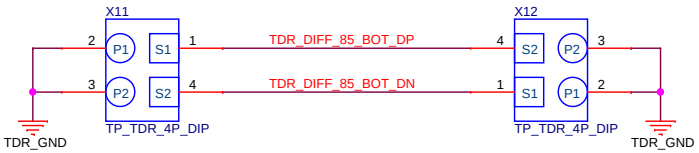

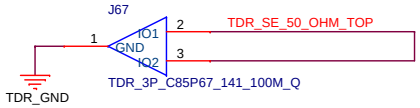

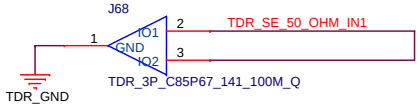

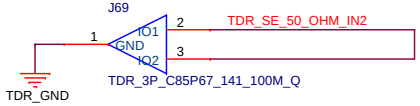

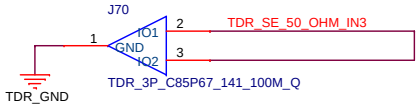

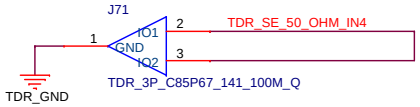

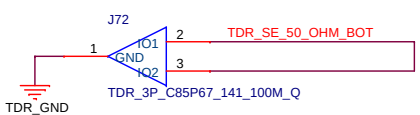

TDR

<Variant Name>

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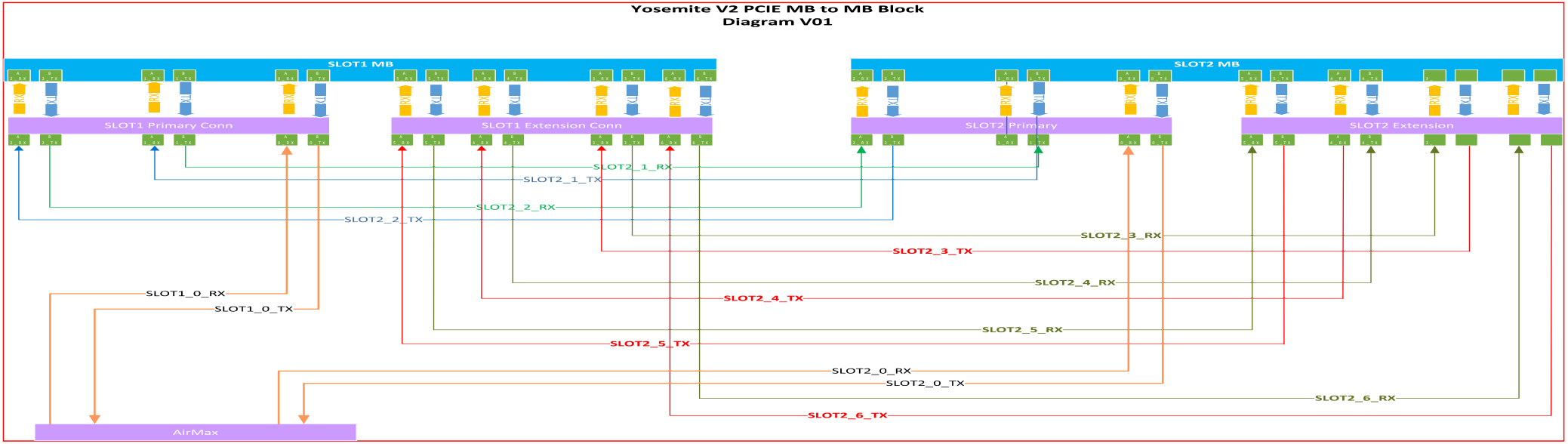

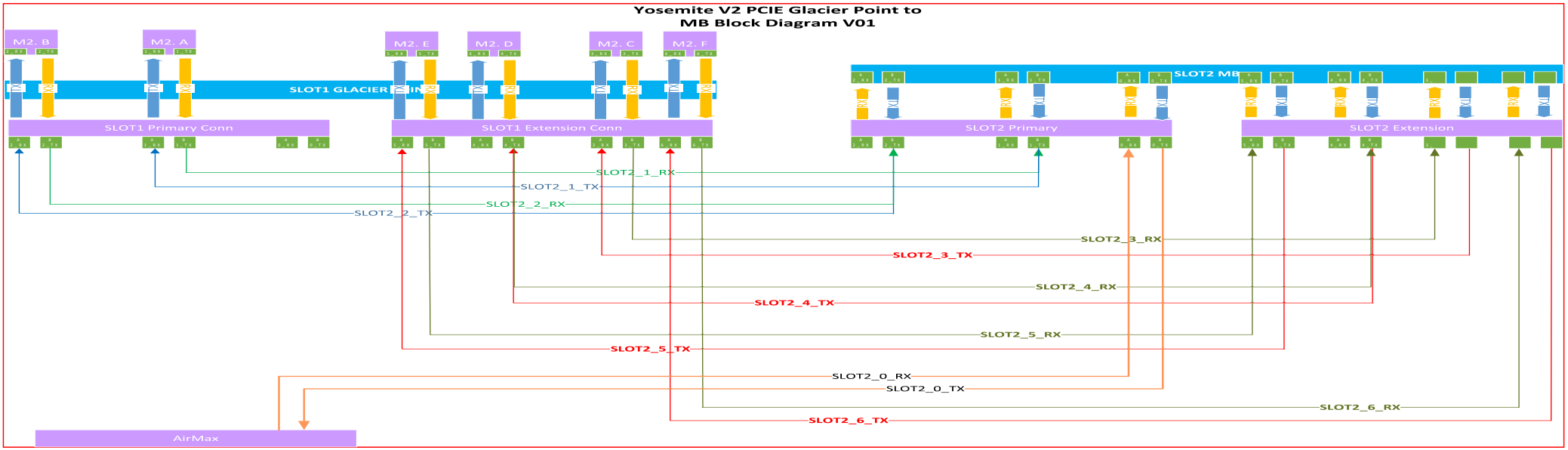

PCIE Diagram

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QUANTA_LOGO

DM1
DUMMY_SYMBOL
QUANTA_LOGO_7X26

WEEE

DM2
DUMMY_SYMBOL
WEEE

PB-E1

DM3
DUMMY_SYMBOL
PB-E1_SMALL

PCBA_LABEL

DM6
DUMMY_SYMBOL
PCBA_LABEL_15X5

BMC AMI LABEL

DM4
DUMMY_SYMBOL
BIOS-BMCLABEL_10-5X10-5

NI

BARCODE

DM7
DUMMY_SYMBOL
BARCODE_20X6

DM10
DUMMY_SYMBOL
BARCODE_20X6

PCB_VENDER_LOGO

DM5
DUMMY_SYMBOL
PCB_VENDOR_LOGO_15X8

Laser Mark

DM8
DUMMY_SYMBOL
LASER_MARK_LABELS_10X10B

DM9
DUMMY_SYMBOL
LASER_MARK_LABELS_10X60T

CE Logo

DM11
DUMMY_SYMBOL
CE_LOGO_5.8X5.08

UL Logo

DM12
DUMMY_SYMBOL
UL_LOGO_E142692_7.3X4.4

Dummy symbol

<Variant Name>

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