1.

Your company's internal studies show that a single-core system is sufficient for the demand on your processing power; however, you are exploring whether you could save power by using two cores.

> a. Assume your application is 80% parallelizable. By how much could you decrease the frequency and get the same performance?

$$\frac{f_0}{f_\delta} \times \frac{(1-80\%)+\frac{80\%}{2}}{1} = 1 \rightarrow f_\delta = 0.6 f_0$$

> b. Assume that the voltage may be decreased linearly with the frequency. Using the equation below, how much dynamic power would the dual-core system require as compared to the single-core system?

$$\text{Power}_{\text{dynamic}} \propto 1/2 \times \text{Capacitive load} \times \text{Voltage}^2 \times \text{Frequency switched}$$

$$\frac{P_1}{P_0} = \frac{(V \times 0.6)^2 \times f_\delta}{V^2 \times f_0} = 0.216$$

> c. Now assume the voltage may not decrease below 30% of the original voltage. This voltage is referred to as the *voltage floor*, and any voltage lower than that will lose the state. What percent of parallelization gives you a voltage at the voltage floor?

$$\frac{f_0}{f_0 \times (1-30\%)} \times \frac{(1-\Delta)+\frac{\Delta}{2}}{1} = 1 \rightarrow \Delta = 60\%$$

> d. Using the equation below, how much dynamic power would the dual-core system require as compared to the single-core system when taking into account the voltage floor?

$$\text{Power}_{\text{dynamic}} \propto 1/2 \times \text{Capacitive load} \times \text{Voltage}^2 \times \text{Frequency switched}$$

$$\frac{P_2}{P_0} = \frac{(V \times 0.7)^2 \times f_\delta}{V^2 \times f_0} = 0.294$$

2.

In a server farm such as that used by Amazon or eBay, a single failure does not cause the entire system to crash. Instead, it will reduce the number of requests that can be satisfied at any one time.

> If a company has 10,000 computers, each with a MTTF of 30 days, and it experiences catastrophic failure only if 1/3 of the computers fail, what is the MTTF for the system?

$$\frac{30 \times \frac{1}{3} \times 10000}{10000} = 10 days$$

3.

> Briefly explain the meaning of Moore's Law

Moore's Law refers to the observation that the number of transistors on a microchip doubles approximately every two years, leading to increased computing power and efficiency. This trend suggests that technology will continue to advance rapidly, ultimately making devices smaller, faster, and more affordable.

4.

> Briefly explain the meaning of Amdahl's Law.

Amdahl's Law is a principle that describes the potential speedup of a computing task when only part of the task can be parallelized. It states that the overall performance improvement is limited by the portion of the task that cannot be parallelized. Specifically, if a fraction of a task is sequential, the maximum speedup is constrained by that fraction, meaning that as you increase parallel processing, the benefits diminish.

5.

> Briefly explain what parts are included in the ISA.

An Instruction Set Architecture (ISA) includes several key components:

- Instructions: The set of operations that the processor can execute, such as arithmetic, logic, control flow, and data manipulation.
- Data Types: The formats for representing various kinds of data, such as integers, floating-point numbers, and characters.
- Addressing Modes: The methods for specifying the operands for instructions, such as immediate, direct, indirect, and register addressing.
- Registers: The small, fast storage locations within the CPU used to hold data and instructions temporarily.
- Memory Architecture: The organization of memory and how instructions interact with it, including how data is loaded and stored.
- Exceptions and Interrupts: Mechanisms for handling unexpected events and managing control flow.

6.

Assume a disk subsystem with the following components and MTTF:

- 10 disks, each rated at 1,000,000-hour MTTF
- 1 ATA controller, 500,000-hour MTTF -
- 1 power supply, 200,000-hour MTTF -
- 1 fan, 200,000-hour MTTF
- 1 ATA cable, 1,000,000-hour MTTF

> compute the MTTF of the system as a whole

$$MTTF_{system} = \frac{1}{\frac{10}{1000000} + \frac{1}{500000} + \frac{1}{200000} + \frac{1}{200000} + \frac{1}{1000000}} = 43478.26hour$$

7.

Suppose that we want to enhance the processor used for web serving. The new processor is 10 times faster on computation in the web serving application than the old processor. Assuming that the original processor is busy with computation 50% of the time and is waiting for I/O 50% of the time, what is the overall speedup gained by incorporating the enhancement?

$$Speed = \frac{T_{old}}{T_{new}} = \frac{1}{50\% \times \frac{1}{10} \times + 50\%} = 1.818$$

8.

Suppose we made the following measurements:

- Frequency of FP operations = 25%
- Average CPI of FP operations = 4.0
- Average CPI of other instructions = 1.33
- Frequency of FSQRT = 2%
- CPI of FSQRT = 20

> Assume that the two design alternatives are to decrease the CPI of FSQRT to 1.5 or to decrease the average CPI of all FP operations to 2. Compare these two design alternatives using the processor performance equation

$$CPI_{origin} = \sum_{i=1}^{n} CPI_i \times Percent = 4 \times 25\% + 1.33 \times 75\% = 2.0$$

$$CPI_1 = CPI_{origin} - 2\% \times (20 - 1.5) = 1.63$$

$$CPI_2 = \sum_{i=1}^{n} CPI_i \times Percent = 2 \times 25\% + 1.33 \times 75\% = 1.5$$

Obviously,the second idea is the best way in proving CPU.