1.

a. 1.5 GHz × .80 × .85 × 0.70 × 10 cores × 32/4 = 57.12 GFLOPs/s

b.

Option 1:

1.5 GHz × .80 × .85 × .70 × 10 cores × 32/2 = 114.24 GFLOPs/s (speedup = 114.24/57.12 = 2)

Option 2:

1.5 GHz × .80 × .85 × .70 × 15 cores × 32/4 = 85.68 GFLOPs/s (speedup = 85.68/57.12 = 1.5)

Option 3:

1.5 GHz × .80 × .95 × .70 × 10 cores × 32/4 = 63.84 GFLOPs/s (speedup = 63.84/57.12 = 1.11)

2.

$$\frac{512bits}{8 \times 8bits} = 8\text{elements}$$

$$\left\lceil \frac{524}{8} \right\rceil \times 4 = 264cycles$$

3.

A

B

A

4.

a

C0.0: (S,AC20,0020) return 0020

b

C0.0: (M,AC20,0080)

C3.0: (I,AC20,0020)

c.

C3.0: (M,AC20,0080)

d

C1.2: (S,AC10,0010) returns 0010

e

C0.1: (M,AC08,0048)

C3.1: (I,AC08,0008)

f

C0.2: (M,AC30,0078)

M: 110<- 0030 (write back)

5.

a

6个chimes

Vmul V*re , Va_re, Vb_re

Vld Va_im

Vld Vb_im

Vmul V*im, Va_im, Vb_im

Vsub Vc_re, V*re, V*im

Vst Vc_re

Vmul V*re_im, Va_re, Vb_im

Vld Va_re, next loop

Vmul V*im_re, Va_im, Vb_re

Vld Vb_re, next loop

Vadd Vc_im, V*re_im, V*im_re

Vst Vc_im

b

if 3 pipelined memory unit, still 6 chimes

Vld Va_re

Vld Vb_re

Vmul V*re, Va_re, Vb_re

Vld Va_im

Vld Vb_im

Vmul V*im, Va_im, Vb_im

Vsub Vc_re, V*re, V*im

Vst Vc_re

Vmul V*re_im, Va_re, Vb_im

Vmul V*im_re, Va_im, Vb_re

Vadd Vc_re, V*re, V*im

Vst Vc_re

2* (15 +8 +64) + 2* (15+ 5+64) + 2*(15+8+64)* = 487+ 2* 84 = 516

So no improvement

(2* (15+8+64) + (15 + 5 + 64))/64 =

Or

1. vmul
2. vmul
3. vsub vst
4. vmul
5. vmul vld
6. addvv.s vst vld vld vld

vld vld vld mul: 64 + 15 + 8

vld mul add: 64 + 15+ 8 + 5

vsd mul: 64 + 15+ 8

mul add vsd: 64 + 15 + 8 + 5

464 + *154* + *48* + *25* = 358