Microcoded Bus Selector and Von Neumann Architecture

Figure 1: Overview of Architecture.

Description of the Circuit

The complete microcoded bus selector consists of three functional subsystems:

1. **Encoder (Control Address Generator)** — Converts one-hot control input lines into a binary address.
2. **Programmable Control ROM** — Uses this address to decode a microinstruction, generating control signals that define the system state (bus enable, select lines, etc.).
3. **Data Multiplexer and Bus Enable** — Routes data from one of eight input channels to a shared system bus, under the direction of the ROM-generated control word.

Operationally, this circuit models a *microprogrammed control unit*. The encoder provides an address (similar to a *microinstruction counter*), the ROM acts as the *control store*, and the MUX functions as the *data path selector*. Each address corresponds to a specific **microstep** in the execution of an instruction. When the bus enable signal T is asserted, one of the data inputs D_n is passed through to the shared bus according to the three-bit select lines (S_2, S_1, S_0), implementing the transfer of data between registers, memory, and control elements.

Modeling the Von Neumann Architecture

This circuit mirrors the principles of the **Von Neumann architecture** by separating the control logic (ROM) from the data path (bus and registers) while unifying both through a common communication bus.

- The **ROM** represents the *control memory* in which each word defines the micro-operations required for a macroinstruction (i.e., a full CPU instruction).
- The **Address inputs** (A_2, A_1, A_0) correspond to the *current state or step* in a micro-program sequence.
- The **Control word outputs** (T, S_2, S_1, S_0) act as decoded *control register fields*, which directly steer the data path.

In a full processor, this architecture would iterate through *microinstructions* stored in ROM to carry out the fetch–decode–execute cycle. This prototype circuit represents one slice of that control store and bus system — where the bus selector forms the mechanism by which data is routed according to the currently addressed microinstruction.