Logic Derivations for Microcoded Bus Selector System

1. Encoder Equations

Given one-hot inputs I_0 through I_7, the 3-bit address lines (A_2, A_1, A_0) are defined by the binary index of the active input.

Active Input	A_2	A_1	A_0
I_0	0	0	0
I_1	0	0	1
I_2	0	1	0
I_3	0	1	1
I_4	1	0	0
I_5	1	0	1
I_6	1	1	0
I_7	1	1	1

Thus, by inspection of which inputs make each address bit high:

$$A_2 = I_4 + I_5 + I_6 + I_7,$$
$$A_1 = I_2 + I_3 + I_6 + I_7,$$
$$A_0 = I_1 + I_3 + I_5 + I_7.$$

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2. Decoder Equations

Each one-hot output Y_n corresponds to a unique address $(A_2A_1A_0)$.

$$Y_0 = \overline{A_2}\,\overline{A_1}\,\overline{A_0}, \quad Y_1 = \overline{A_2}\,\overline{A_1}\,A_0,$$
$$Y_2 = \overline{A_2}\,A_1\,\overline{A_0}, \quad Y_3 = \overline{A_2}\,A_1\,A_0,$$
$$Y_4 = A_2\,\overline{A_1}\,\overline{A_0}, \quad Y_5 = A_2\,\overline{A_1}\,A_0,$$
$$Y_6 = A_2\,A_1\,\overline{A_0}, \quad Y_7 = A_2\,A_1\,A_0.$$

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3. ROM (Control Word) Equations

The ROM converts active row lines Y_0–Y_7 into the 4-bit control word

$$(Q_3, Q_2, Q_1, Q_0) = (T, S_2, S_1, S_0).$$

The programmed mapping is:

A_2	A_1	A_0	Y_n	T	$(S_2S_1S_0)$
0	0	0	Y_0	1	000
0	0	1	Y_1	1	001
0	1	0	Y_2	1	010
0	1	1	Y_3	1	011
1	0	0	Y_4	1	100
1	0	1	Y_5	1	101
1	1	0	Y_6	1	110
1	1	1	Y_7	1	111

From this, we obtain:

$$\begin{aligned} T &= 1, \\ S_2 &= Y_4 + Y_5 + Y_6 + Y_7, \\ S_1 &= Y_2 + Y_3 + Y_6 + Y_7, \\ S_0 &= Y_1 + Y_3 + Y_5 + Y_7. \end{aligned}$$

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4. Multiplexer Equations

The multiplexer uses the select bits (S_2, S_1, S_0) to choose one of the data lines D_0–D_7.

Each channel term t_n is defined as:

$$\begin{aligned} t_0 &= \overline{S_2}\,\overline{S_1}\,\overline{S_0}\,D_0, \quad t_1 = \overline{S_2}\,\overline{S_1}\,S_0\,D_1, \\ t_2 &= \overline{S_2}\,S_1\,\overline{S_0}\,D_2, \quad t_3 = \overline{S_2}\,S_1\,S_0\,D_3, \\ t_4 &= S_2\,\overline{S_1}\,\overline{S_0}\,D_4, \quad t_5 = S_2\,\overline{S_1}\,S_0\,D_5, \\ t_6 &= S_2\,S_1\,\overline{S_0}\,D_6, \quad t_7 = S_2\,S_1\,S_0\,D_7. \end{aligned}$$

The multiplexer output before bus enable is:

$$Y = t_0 + t_1 + t_2 + t_3 + t_4 + t_5 + t_6 + t_7.$$

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5. Bus Enable Equation

The final bus output is gated by the enable bit T:

$$\boxed{\text{BUS\_OUT} = Y \cdot T}$$

When $T = 1$, the bus output follows the selected data line D_n. When $T = 0$, the bus is disabled (logic low).