School of Computer Science Engineering and Technology

Course- BCA	Type- Core
Course Code- CBCA101P	Course Name- Digital Design and CO
Year- 2022	Semester-odd
Date- …….	Batch- ALL

Assignment 5 – Digital Design and Computer Organization

Experiment No.	Name	CO1	CO2	CO3
5	Truth Table formation, Design and Analysis of Half Adder, Full Adder circuit using Verilog coding	✓	✓	---

In this lab, we shall learn about the procedures in Verilog, generation of modules from a truth table. We also further explore the "Module Instantiation", where a previously designed module will be used other modules.

Q1. Consider the following expressions. Here A, B, and C are acting as input.

X = A.B'.C + A'.B.C

Y = A'.B' + B.C

Z = X'.Y + Y'.X

i. Generate the truth table for each expression.

ii. Write down the modules for X and Y. use the instances of X and Y to implement the module for Z.

iii. Verify the same with the corresponding Testbench code.

Q2. Design a Verilog code for excess-3 to BCD code. Using behavioral design then test with test bench code.

a. Prepare truth table.
b. Identify Boolean function for each output using K-maps.
c. Write Verilog code for implement the module.
d. Check with test bench.

Q3. A half-adder is used to add two single bit inputs. It produces a single bit output and a possible carry bit. Below is the truth table for the same.

Input		**Output**	
A	B	Carry	Output
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

(i) Develop the Boolean expression and logic circuit for the given truth table.

(ii) Write a Verilog module for Universal NOR gate. Utilize the instances of NOR gate only to write a structural Verilog code for Half adder.
(iii) Verify it with respective testbench code.

Q.4 The half adder in the previous question can only add two one-bit numbers when there is no carry bit, which is not sufficient in many cases. While a full-adder has two one-bit inputs, a carry-in input, a sum output, and a carry-out output. Below truth table represents a full adder.

Full Adder Truth Table				
Input			**Output**	
A	B	Cin	Cout	Sum
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

(i) Utilize the above truth table to design the Boolean expression and digital circuit for the full adder.
(ii) Write the behavioral Verilog code for the full adder.
(iii) Verify it with respective Testbench code.

Submission Instructions:

- Prepare the submission file according to the following process:
    1. Copy the Verilog code, the Test Bench Code in a Word File.
    2. Take the ScreenShot of Waveform and paste into the same word file.
    3. Repeat Step 1 and 2 for all the programs.
    4. Copy and Paste all the Verilog code, Testbench Code and Waveform into a single word file as 1_verilog, 1_TestBench, 1_Waveform, 2_verilog, 2_TestBench, 2_Waveform… etc.
    5. Convert it into pdf file, name it as **RollNo_Assignment# (Example: E20CSE001_ Assignment3.pdf)**.
    6. Submit your file on LMS **within the deadline**.
- Write your **Name and Roll No. as comment before starting of each program**. Keep in mind this is **Mandatory**. Failing which you may lose your marks.
- Make it sure that in each program, **you have mentioned enough comments** regarding the explanation of program instructions.
- **Each student will submit their assignment on their corresponding group slot only.**
- Late submission will lead to penalty.
- Any form of plagiarism/copying from peer or internet sources will lead penalty.
- Following of all instructions at submission time is mandatory. Missing of any instructions at submission time will lead penalty.