School of Computer Science Engineering and Technology

Course- BCA	Type- Core
Course Code- CBCA101P	Course Name- Digital Design and CO
Year- 2022	Semester-odd
Date- …….	Batch- ALL

Lab Assignment 3 – Digital Design and Computer Organization

Experiment No.	Name	CO1	CO2	CO2
2	Implementation of circuits structural and behavioural Verilog coding	✓	---	---

1. Perform the following operation on a given Boolean expression:
   F(ABC) = ABC + A (B' + C')
   a. Write a truth table for each Boolean expression.
   b. Draw a schematic diagram for each Boolean expression.
   c. Write a Verilog code for each Boolean expression and then test using wave form and compare with truth table whether your circuit produced same output or not?

2. Perform the following operation on a given Boolean expression:
   F(ABC) = A'+ BC
   a. Write a truth table for each Boolean expression.
   b. Draw a schematic diagram for each Boolean expression.
   c. Write a Verilog code for each Boolean expression and then test using wave form and compare with truth table whether your circuit produced same output or not?

3. Representation of AND gate using only NAND gates and perform the following operations:
   a. Derive the Boolean expression.
   b. Write the truth table for the above expression
   c. Write a Verilog code for each Boolean expression and then test using wave form and compare with truth table whether your circuit produced same output or not?

4. For the given circuit diagram do the following:
   a. Derive the Boolean expression.
   b. Write the truth table for the above expression
   c. Write a Verilog code for each Boolean expression and then test using wave form and compare with truth table whether your circuit produced same output or not?

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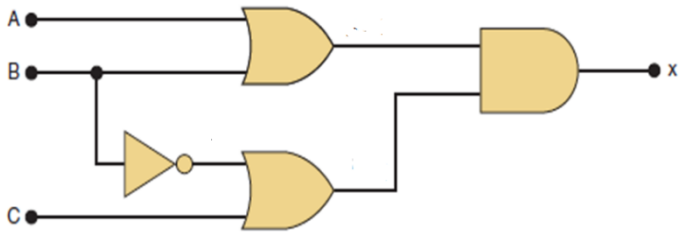

Submission Instructions:

- Prepare the submission file according to the following process:
    1. Copy the Verilog code, the Test Bench Code in a Word File.
    2. Take the ScreenShot of Waveform and paste into the same word file.
    3. Repeat Step 1 and 2 for all the programs.
    4. Copy and Paste all the Verilog code, Testbench Code and Waveform into a single word file as 1_verilog, 1_TestBench, 1_Waveform, 2_verilog, 2_TestBench, 2_Waveform… etc.
    5. Convert it into pdf file, name it as **RollNo_Assignment# (Example: E20CSE001_ Assignment2.pdf)**.
    6. Submit your file on LMS **within the deadline**.

- Write your **Name and Roll No. as comment before starting of each program**. Keep in mind this is **Mandatory**. Failing which you may lose your marks.
- Make it sure that in each program, **you have mentioned enough comments** regarding the explanation of program instructions.
- **Each student will submit their assignment on their corresponding group slot only.**
- Late submission will lead to penalty.
- Any form of plagiarism/copying from peer or internet sources will lead penalty.
- Following of all instructions at submission time is mandatory. Missing of any instructions at submission time will lead penalty.