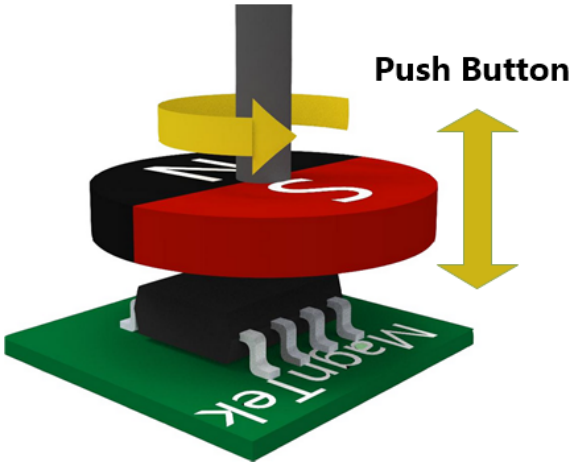
MT6701

Hall Based Angle Position Encoder Sensor

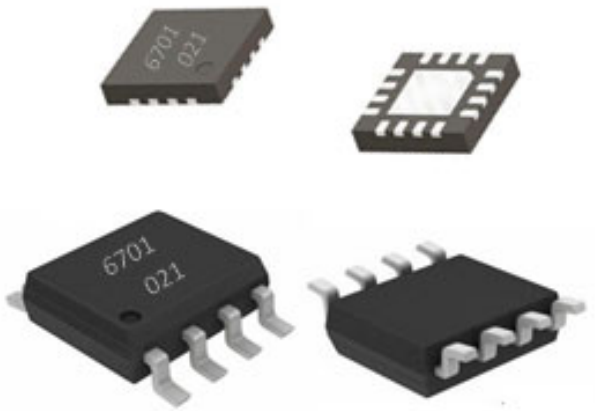
Features and Benefits

- Based on Hall Sensing Technology with 0°~360° Full Range Angle Sensing
- Independent Output Interface: I²C, SSI, ABZ, UVW, Analog/PWM and Push-Button Function on Z-Axis
- 14-bit Core Resolution
- Maximum Rotation Speed 55,000 RPM
- Output Propagation Delay 5 us
- Incremental ABZ Resolution 1~1024 Pulses per Revolution (PPR) User Programmable
- UVW Output Resolution 1~16 Pole-Pairs per Revolution User Programmable
- RoHS Compliant 2011/65/EU
- SOP-8 and QFN-16 Package



Applications

- Absolute Linear Position Sensor
- Robotics Control
- Contactless Knob
- Contactless Potentiometer
- Power Tools



General Description

The MagnTek rotary position sensor MT6701 is an IC based on Hall sensing technology. A rotating magnetic field in the x-y sensor plane delivers two sinusoidal output signals indicating the angle (α) between the sensor and the magnetic field direction.

The incremental ABZ output mode is available in this sensor series, making the chip suitable to replace various optical encoders. The maximum resolution is 1024 pulse/4096 steps per revolution in binary mode.

A standard I²C or SSI interface allows a host microcontroller to read the 14-bit absolute angle position data from MT6701. The absolute angle position is also provided as PWM output or linear analog signal proportional to VDD from a 12-bit DAC.

Additionally, the PUSH output indicates the fast air-gap changes between the MT6701 and magnet which can be used to implement a contactless pushbutton function in which the knob can be pressed to move the magnet toward the MT6701.

Table of Contents

1. Pin Configuration

1. 1 SOP-8 Package

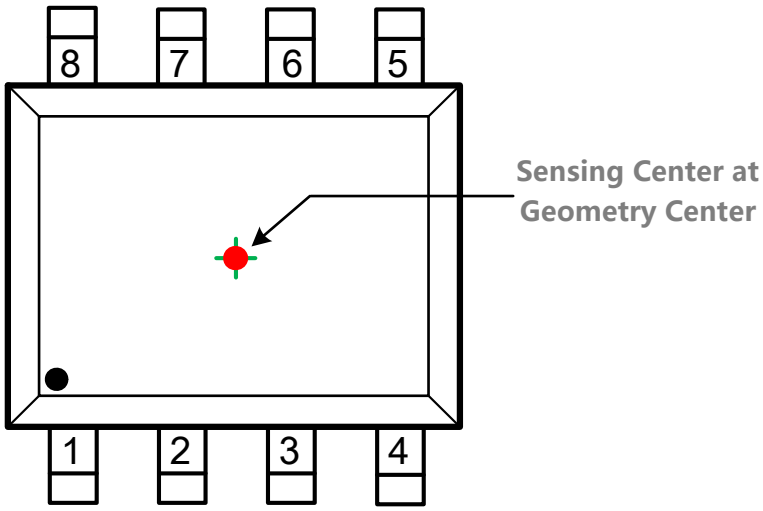


Figure 1: Pin Configuration for SOP-8 Package

Pin List

Name	#	Type	Description
VDD	1	Power Supply	3.3~5.0V Supply
MODE	2	Digital Input with Build in 200KΩ Pull-up Resistor	ABZ or I²C/SSI Selection
OUT	3	Analog/Digital Output	Analog or PWM Output
GND	4	Power Supply	Ground
PUSH	5	Digital Output	Push Button Function Output
A	6	Digital Input/output	Incremental Signal A/U or I²C Data 'SDA', or SSI Data 'DO'
B	7	Digital Input/output	Incremental Signal B/V or I²C Clock 'SCL', or SSI Clock 'CLK'
Z	8	Digital Input/output with Build in 200KΩ Pull-up Resistor	Incremental Signal Z/W or SSI 'CSN'

Family Members

Part Number	Description
MT6701CT-STD	SOP-8 Package, Tube Pack (100pcs/Tube) or Tape & Reel Pack (3000pcs/Reel)

SOP-8 Reflow Sensitivity Classification: MSL-3

1. 2 QFN-16 Package

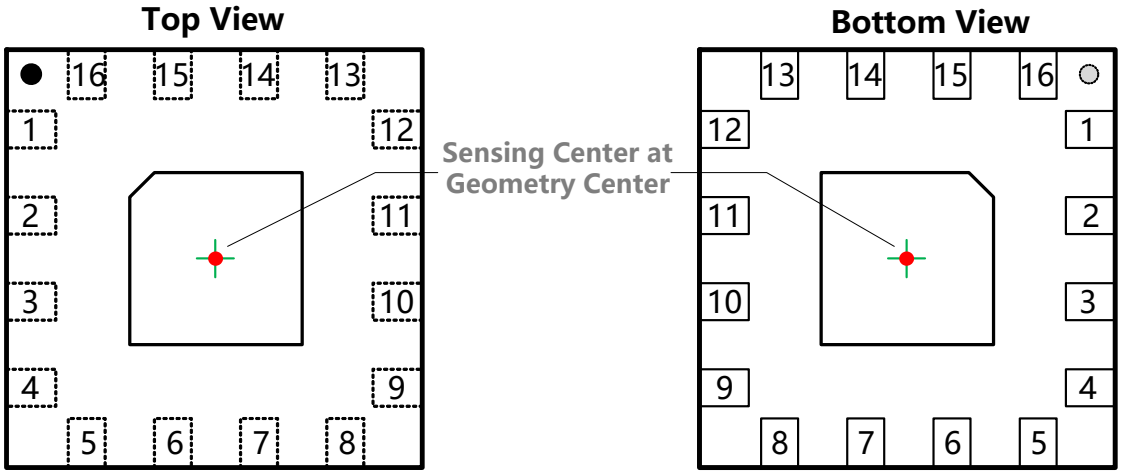


Figure 2: Pin Configuration for QFN-16 Package

Pin List

Name	#	Type	Description
NC	1	-	Not Connected
NC	2	-	Not Connected
NC	3	-	Not Connected
NC	4	-	Not Connected
PUSH	5	Digital Output	Push Button Function Output
A	6	Digital Input/output	Incremental Signal A, or I²C data 'SDA', or SSI data 'DO'
B	7	Digital Input/output	Incremental Signal B, or I²C clock 'SCL', or SSI clock 'CLK'
Z	8	Digital Input/output with Build in 200KΩ Pull-up Resistor	Incremental Signal Z, or SSI 'CSN'
W	9	Digital Output	Incremental Signal W or –Z
NC	10	-	Not Connected
U	11	Digital Output	Incremental Signal U or –A
V	12	Digital Output	Incremental Signal V or –B
VDD	13	Power Supply	3.3~5.0V Supply
MODE	14	Digital Input with Build in 200KΩ Pull-up Resistor	ABZ or I²C/SSI Selection
OUT	15	Analog/Digital Output	Analog or PWM Output
GND	16	Power Supply	Ground

Family Members

Part Number	Description
MT6701QT-STD	QFN-16 Package, Reel Pack (1000pcs/Reel)

QFN-16 Reflow Sensitivity Classification: MSL-1

2. Functional Diagram

The MT6701 is manufactured in a CMOS standard process and uses advanced magnet sensing technology to sense the magnetic field distribution across the surface of the chip. The integrated magnetic sensing element array is placed around the center of the device and delivers a voltage representation of the magnetic field at the surface of the IC.

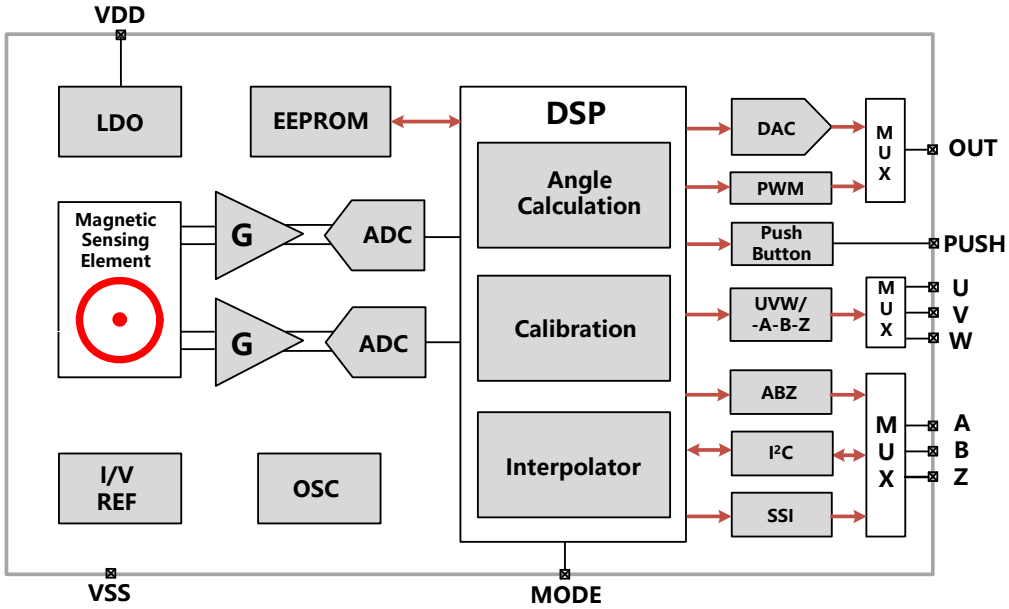


Figure 3: Block Diagram

Figure 3 shows a simplified block diagram of the chip, consisting of the magnetic sensing element modeled by two interleaved Wheatstone bridges to generate cosine and sine signals, gain stages, analog-to-digital converters (ADC) for signal conditioning, and a digital signal processing (DSP) unit for encoding. Other supporting blocks such as LDO, etc. are also included.

3. Absolute Maximum Ratings (Non-Operating)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Name	Min.	Max.	Unit
DC Voltage at Pin VDD	-0.5	7	V
Storage Temperature	-55	150	℃
Operating Temperature	-40	125	℃
Electrostatic Discharge (HBM)	-	±6.0	KV
Electrostatic Discharge (CDM)	-	±1.5	KV

4. Electrical Characteristics

Operation conditions: Ta=-40 to 125℃, VDD=3.0~5.5V unless otherwise noted.

Symbol	Parameter	Conditions/Notes	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	-	3.0	3.3~5.0	5.5	V
Idd	Supply Current	-		10.0	14.0	mA
LSB	Resolution (ABZ Mode)	N Steps per Cycle		360°/N	-	°
INL	Integral Non-Linearity	Note (1)	-	±1.0	±1.5	°
DNL	Differential Non-Linearity (ABZ Mode), Figure 4		-	±0.02	-	°
TN	Transition Noise (ABZ Mode)	25℃	-	0.01		°rms
Hyst	Hysteresis (ABZ Mode)		-	0.088	-	°
T_{PwrUp}	Power-Up Time	VDD Ramp<10us	-	-	1.0	ms
T_{Delay}	Propagation Delay	Constant Speed	-	5	-	us
Analog Output Specification						
R_{OUT}	Analog Output Resistance	-	-	15	30	Ω
R_L	Pull-Up or Pull-Down	-	10	-	-	KΩ
C_L	Loading Capacitor	-	-	-	1	nF
V_{Sat_High}	Saturation High Voltage	I_{load}=1mA	VDD-0.5	-	-	V
V_{Sat_Low}	Saturation Low Voltage	I_{load}=1mA	-	-	0.5	V
DAC_LSB	DAC LSB	12-bit DAC	-	0.025	-	%VDD
DAC_INL	DAC Integral Non-Linearity	-	-	-	±3.0	LSB
DAC_DNL	DAC Differential Non-Linearity	-	-	-	±1.0	LSB
V_{Noise}	Analog Output Noise	Ta=25℃, RMS Value excluding DAC Quantization Noise	-	-	0.5	mVrms
Erm	Ratiometric Error	Note (2)	-0.3	-	0.3	%
PWM Output Characteristics						
FPWM	PWM Frequency	Programmable	-5% @27℃	994.4 /497.2	+5% @27℃	Hz
T_{Rise}	Rising Time	C_L=1nF	-	-	1	us
T_{Fall}	Falling Time	C_L=1nF	-	-	1	us

Digital I/O Characteristics (Push-Pull Type in Normal Mode)						
V_{IH}	High Level Input Voltage	-	0.7*VDD	-	-	V
V_{IL}	Low Level Input Voltage	-	-	-	0.3*VDD	V
V_{OH}	GPIO Output High Level	Push-pull (Iout=2mA)	VDD-0.5	-	-	V
V_{OL}	GPIO Output Low Level	Push-pull (Iout=2mA)	-	-	0.5	V
I_{LK}	Input Leakage Current	-	-	-	±1	uA

Note (1): The typical error value can be achieved at room temperature and with no off-axis misalignment error. The maximum error value can be achieved over operation temperature range, at maximum air gap and with worst-case off-axis misalignment error.

Note (2): The analog output is by design ratiometric, i.e. it is proportional to the supply voltage VDD. The ratiometric error is calculated as follows.

$$\text{Erm} = [\frac{Vout(V_{DD})}{V_{DD}} - \frac{Vout(5\text{V})}{5V}] \cdot 100\%$$

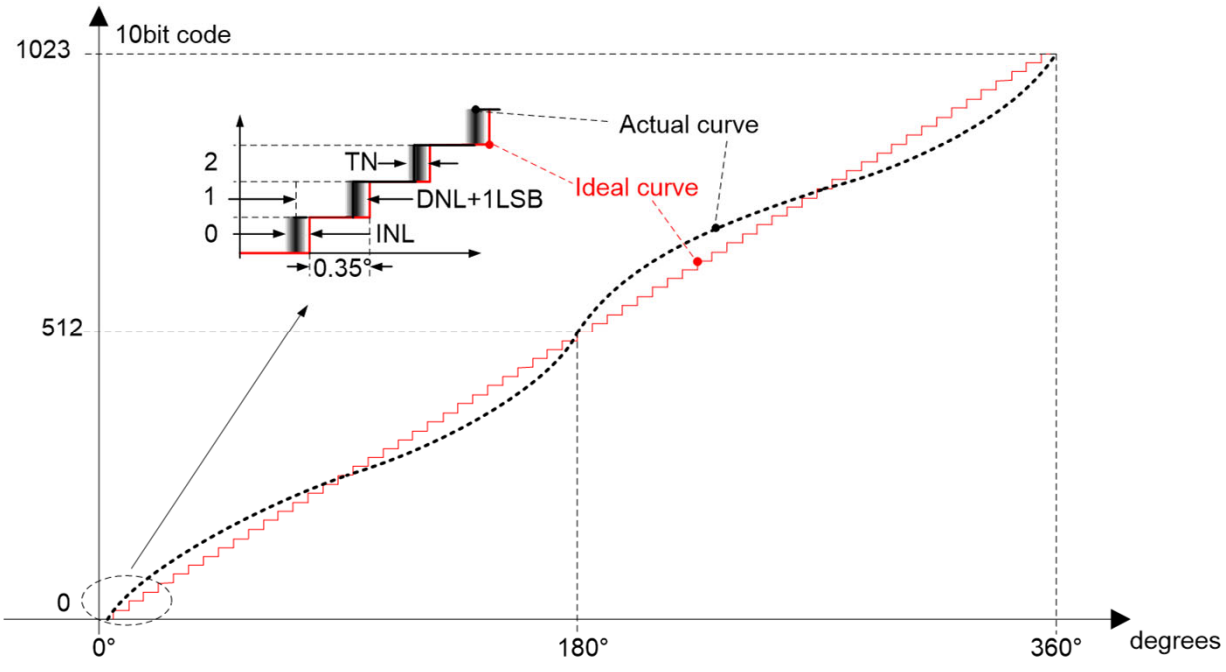


Figure 4: Drawing Illustration INL, DNL and TN (for 10-bit case)

5. Magnetic Input Specifications

Operation conditions: Ta=-40 to 125℃, VDD=3.0~5.5V unless otherwise noted, two-pole cylindrical diametrically magnetized source.

Symbol	Parameter	Conditions/Notes	Min.	Typ.	Max.	Unit
Dmag	Diameter of Magnet	Recommended Magnet: Ø6mm x 2.5mm for Cylindrical Magnets	-	6.0	-	mm
Tmag	Thickness of Magnet		-	2.5	-	mm
Bpk	Magnetic Input Field Amplitude	Measure at the IC Surface	200	-	1,000	Gauss
AG	Air Gap	Magnetic to IC Surface Distance	0.5	1.0	2.0	mm
RS	Rotation Speed		-	-	55,000	RPM
DISP	Off Axis Misalignment	Misalignment Error Between Sensor Sensing Center and Magnet Axis (See Figure 5)	-	-	0.3	mm
TCmag1	Recommended Magnet Material and Temperature Drift Coefficient	NdFeB (Neodymium Iron Boron)	-	-0.12	-	%/℃
TCmag2		SmCo (Samarium Cobalt)	-	-0.035	-	

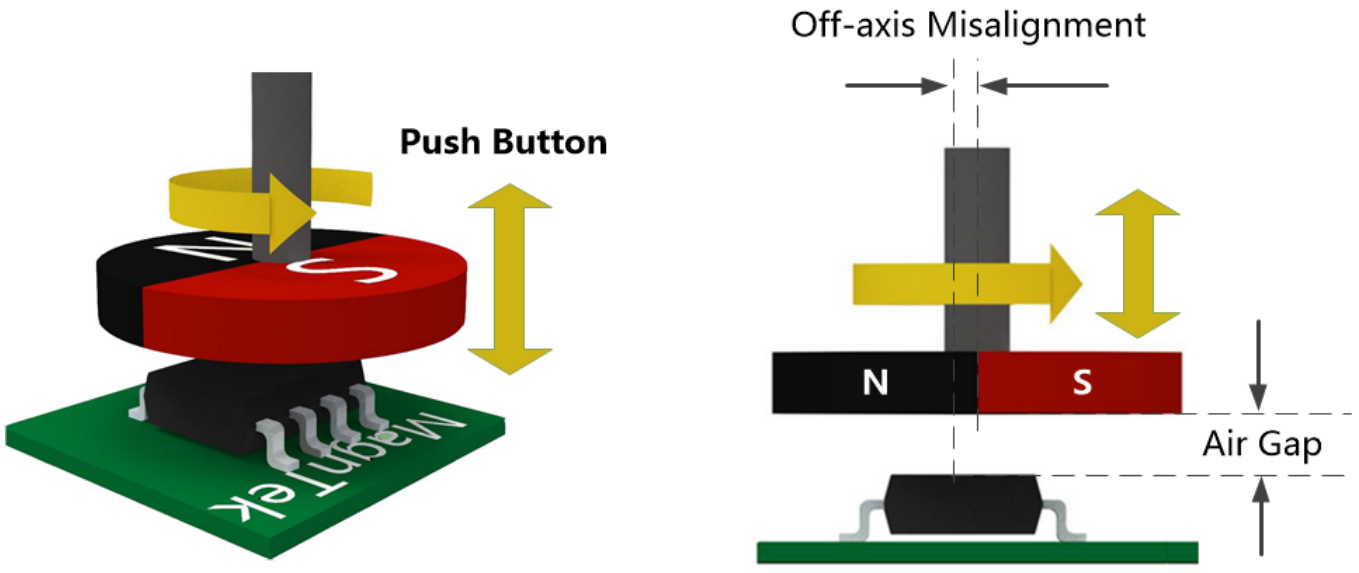


Figure 5: Magnet Arrangement

6. Output Mode

The MT6701 provides ABZ, UVW, Analog and PWM at output pins, also angle position data could be transferred by I²C or SSI interface. A PUSH output indicating pushbutton function is also provided.

6.1 I/O Pin Configuration

For SOP-8 package, ABZ/UVW (Single-end), I²C and SSI are configured to Pin.6, Pin.7 and Pin.8. Analog and PWM output is configured to Pin.3.

SOP-8 Package I/O Pin Configuration

Pin#	I²C	SSI	ABZ	UVW	PWM	Analog	Push
3					PWM	Analog	
5							Push
6	SDA	DO	A	U			
7	SCL	CLK	B	V			
8		CSN	Z	W			

For QFN-16 package, ABZ (Single-end), I²C and SSI are configured to Pin.6, Pin.7 and Pin.8. UVW and –A-B-Z are configured to Pin.11, Pin.12 and Pin.9. Analog and PWM output is configured to Pin.15.

QFN-16 Package I/O Pin Configuration

Pin#	I²C	SSI	ABZ	ABZ+UVW	ABZ Differential	PWM	Analog	Push
5								Push
6	SDA	DO	A	A	A			
7	SCL	CLK	B	B	B			
8		CSN	Z	Z	Z			
9				W	-Z			
11				U	-A			
12				V	-B			
15						PWM	Analog	

6.2 Reference Circuit for ABZ/UVW/PWM/Analog/Push Output

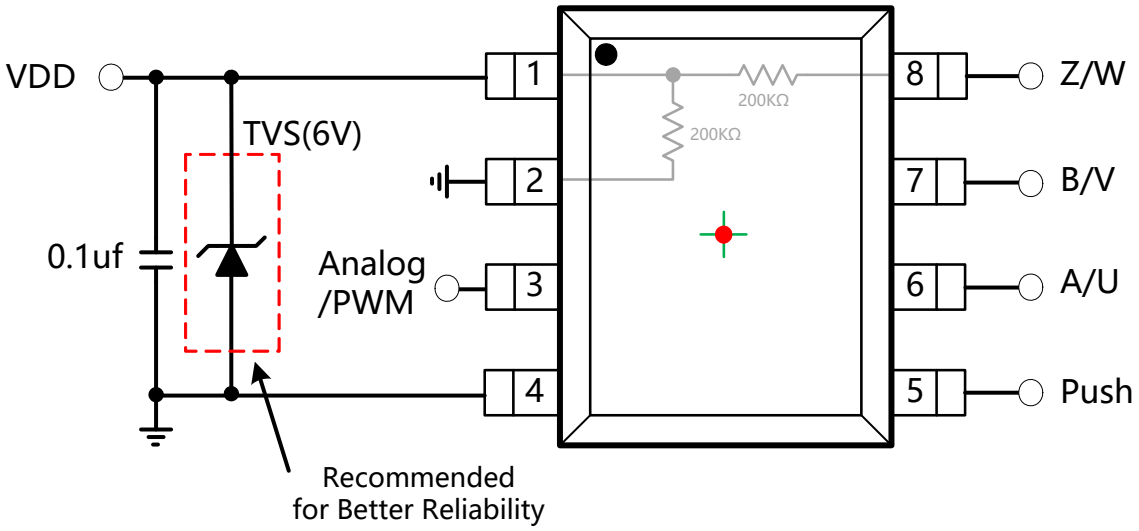


Figure 6: MT6701CT(SOP-8) Reference Circuit for ABZ/UVW/PWM/Analog/Push Output

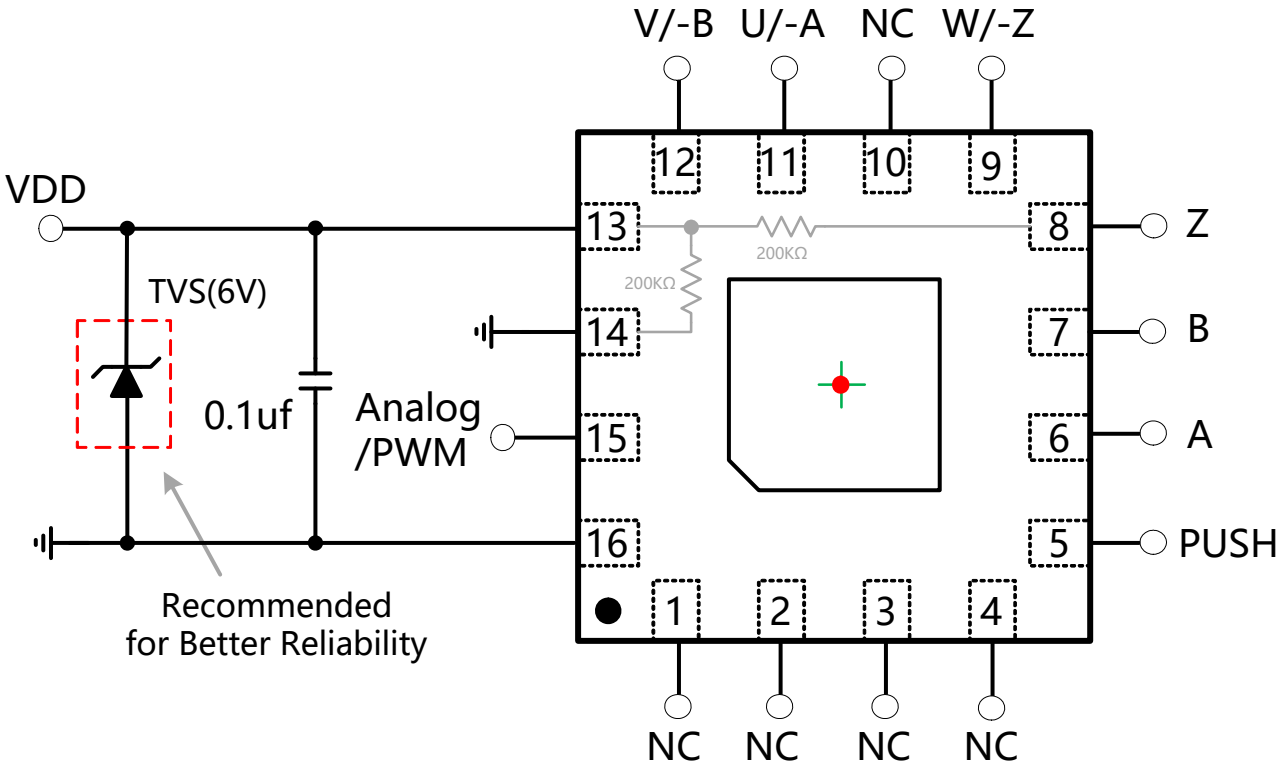


Figure 7: MT6701QT(QFN-16) Reference Circuit for ABZ/UVW/PWM/Analog/Push Output

6.3 Quadrature A, B and Index Output

As shown in Figure 8, when the magnet rotates counter-clock-wise (CCW), output B leads output A by 1/4 cycle, when the magnet rotates clock-wise (CW), output A leads output B by 1/4 cycle (or 1 LSB). Output Z indicates the zero position of the magnet.

After chip power-on, the ABZ output is blocked for 50ms to guarantee proper output.

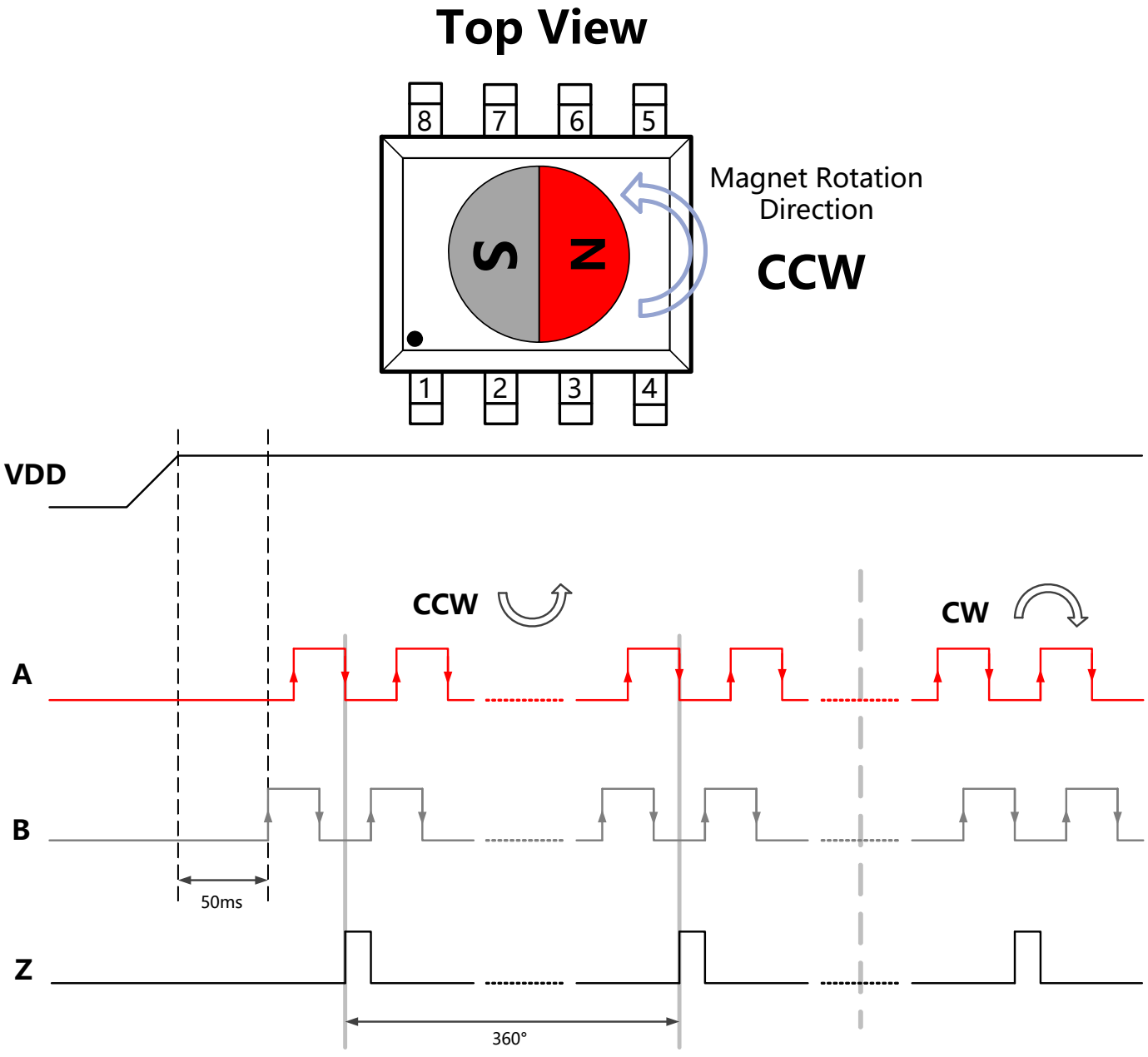


Figure 8: ABZ output with VDD Power-on

Output Z indicates the zero position of the magnet and it is user programmable. The pulse width of Z is selectable as 1, 2, 4, 8, 12, 16 LSBs and 180° as shown in Figure 9 and Figure 10. It is guaranteed that one Z pulse is generated for every rotation round.

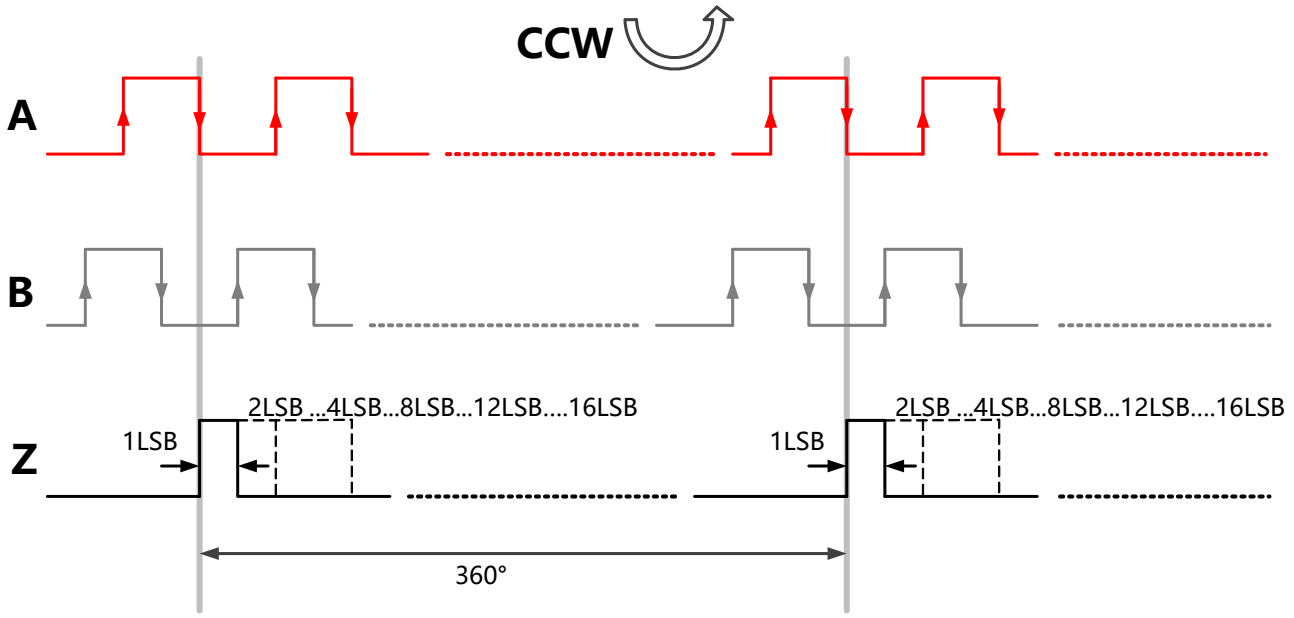


Figure 9: Typical ABZ Output w/i Z Pules Width=1,2,4,8,12 and 16 LSBs

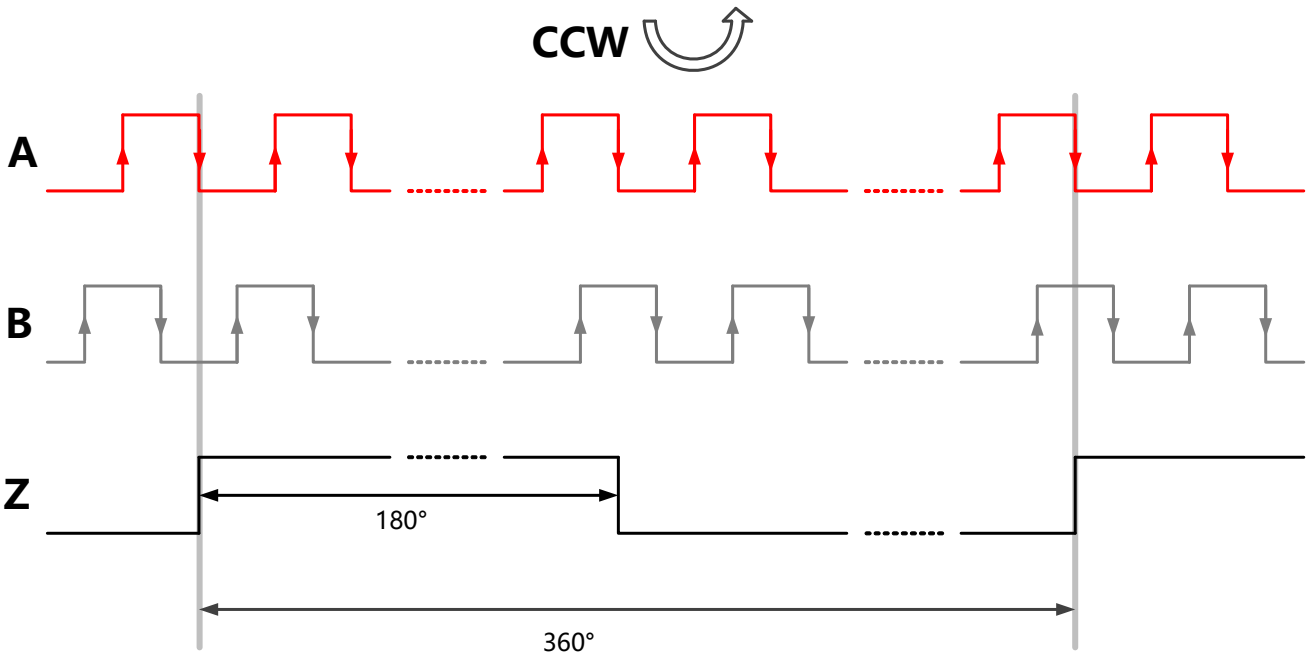
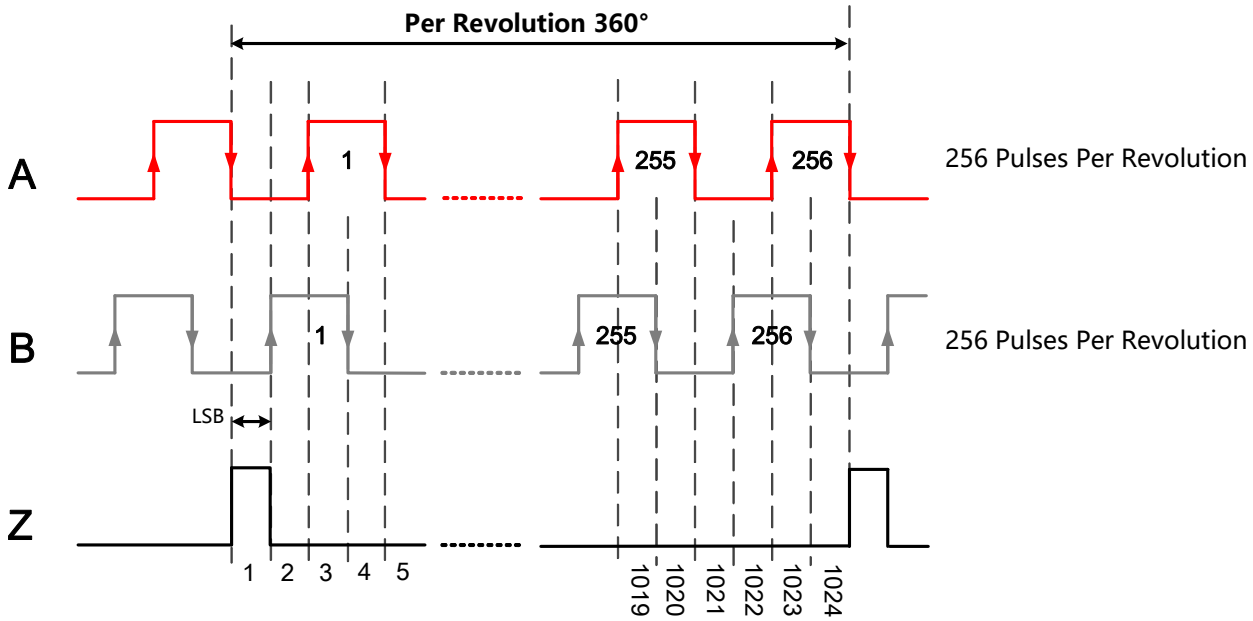


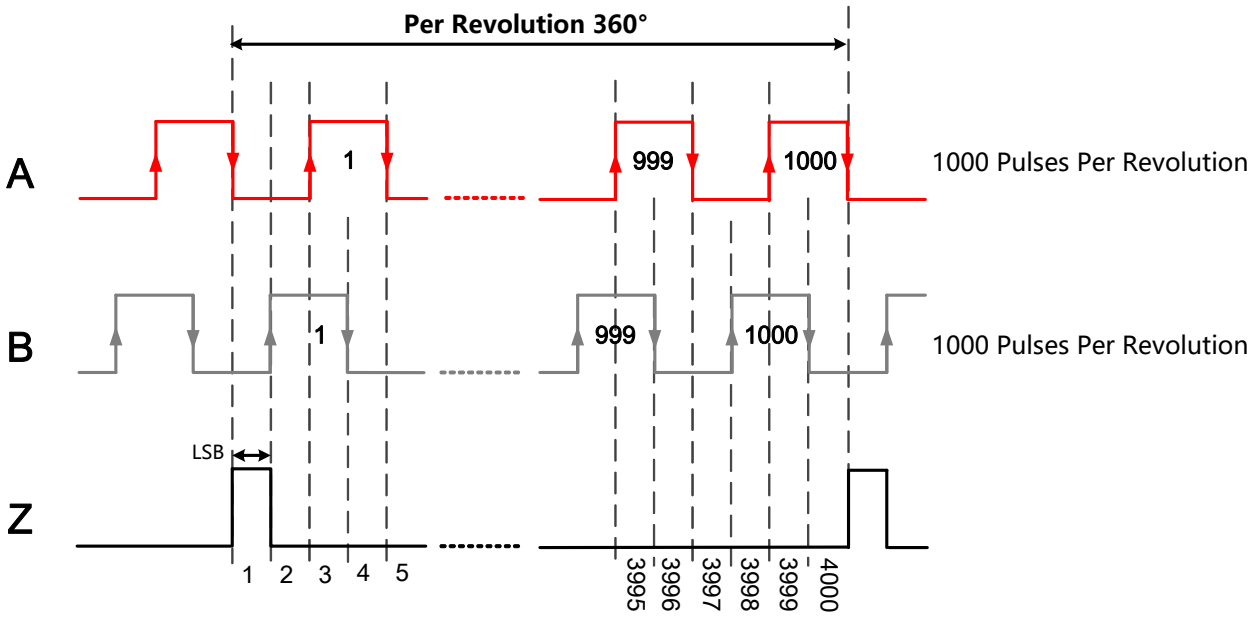
Figure 10: Typical ABZ Output w/i Z pules width=180°

ABZ resolution is user programmable as 1~1024 PPR any resolution. The relationship between binary bits, LSBs and PPR resolution of ABZ output are shown in Figure 11 and Figure 12.



10 bit=2^{10} LSBs=1024 Steps=256 PPR

Figure 11: ABZ Output Resolution=10 bit



1000 PPR=4000 Steps

Figure 12: ABZ Output Resolution=1000 PPR

The Z/Index pulse width could be programmed

Z/Index Pulse Width Register (EEPROM)

Reg. Z_Pulse_Width<2:0>	Width (LSBs)	Reg. Z_Pulse_Width<2:0>	Width (LSBs)
000	1	**100**	12
001	2	**101**	16
010	4	**110**	180°
011	8	**111**	1

The mechanical zero position could be programmed, it is a 12 bits data for 0~360°.

Zero Position Register (EEPROM)

Register	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Zero_MSB	NA	Z_PULSE_WIDTH<2:0>			ZERO<11:8>			
Zero_LSB	ZERO<7:0>							

The resolution of ABZ could be programmed by a 10-bit register 'ABZ_RES'

ABZ Resolution Register (EEPROM)

Register	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ABZ_RES	UVW_RES<3:0>				NA	NA	ABZ_RES<9:8>	
ABZ_RES	ABZ_RES<7:0>							

**** To program EEPROM, please refer Chapter-7***

6.4 UVW Output Mode

The MT6701 provides U, V and W pulses which are 120° (electrical) out of phase as shown in Figure 13. The cycles of UVW per rotation can be programmed.

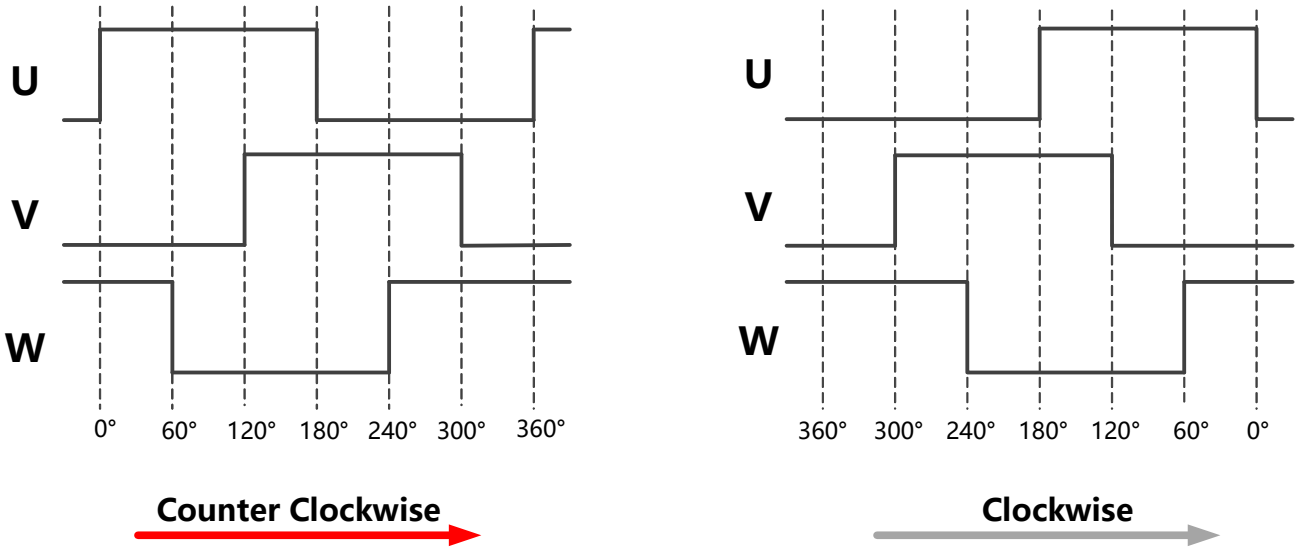


Figure 13: Typical Output Waveform for UVW Mode

UVW Pole Pairs Register (EEPROM)

Reg. UVW_RES<3:0>	UVW Pole Pairs
0000	1
0001	2
0010	3
0011	4
0100	5
0101	6
0110	7
0111	8
1000	9
1001	10
1010	11
1011	12
1100	13
1101	14
1110	15
1111	16

6.5 Analog Output Mode

The MT6701 provides a rail-to-rail linear analog output by a build-in 12 bit DAC as shown in Figure 14. It's a linear transfer function of absolute angle and output voltage. To enable analog output, register 'Output Mode' should be programmed to logic 'Low'.

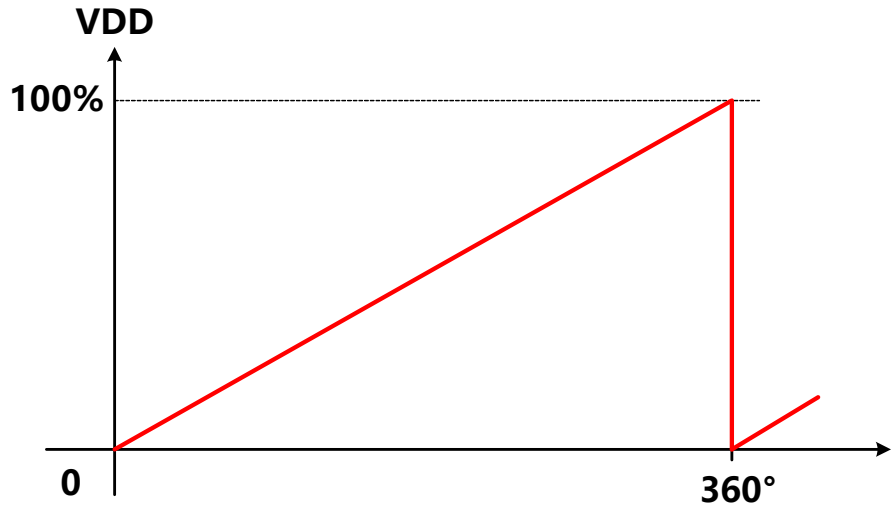


Figure 14: Default Analog Output

Analog or PWM Output Control Register (EEPROM)

Reg. Output Mode	Pin.3 (SOP-8), Pin.15 (QFN-16)
0	Analog
1	PWM

The angle and voltage value of start-point, Clamp_Low (0% or 10%) and Clamp_High (100% or 90%) could be user programmed, also the Zero Point could be user programmed as shown in Figure 15.

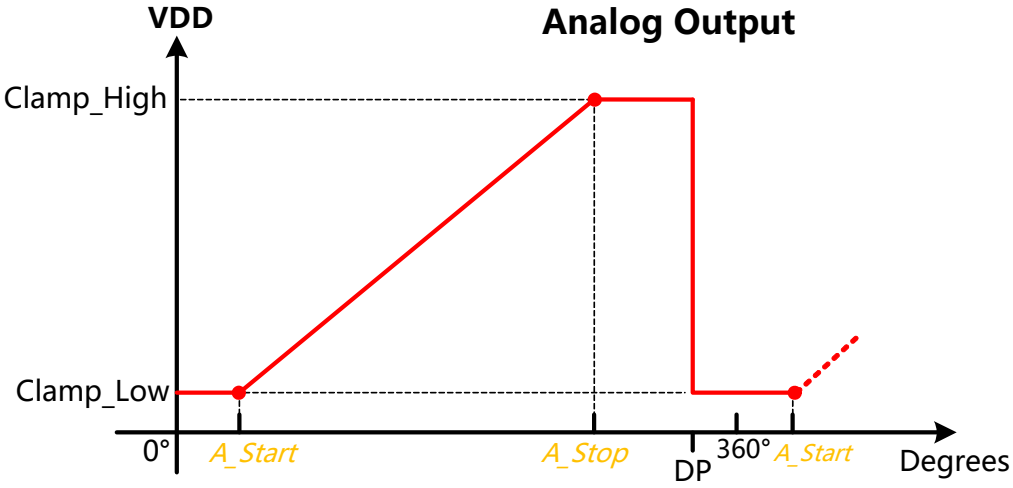


Figure 15: Analog Output Transfer Function

6.6 Pulse Width Modulation (PWM) Output Mode

The MT6701 provides a digital Pulse Width Modulation (PWM) output, whose duty cycle is proportional to the measured angle as shown in Figure 16. PWM is a default output of Pin.10.

The PWM output consists of a frame of 4119 PWM clock periods. The angle data is represented with 12-bit resolution in the frame. One PWM clock period represents 0.088° and has a typical duration of 244 ns which also could be programmed to be 122 ns.

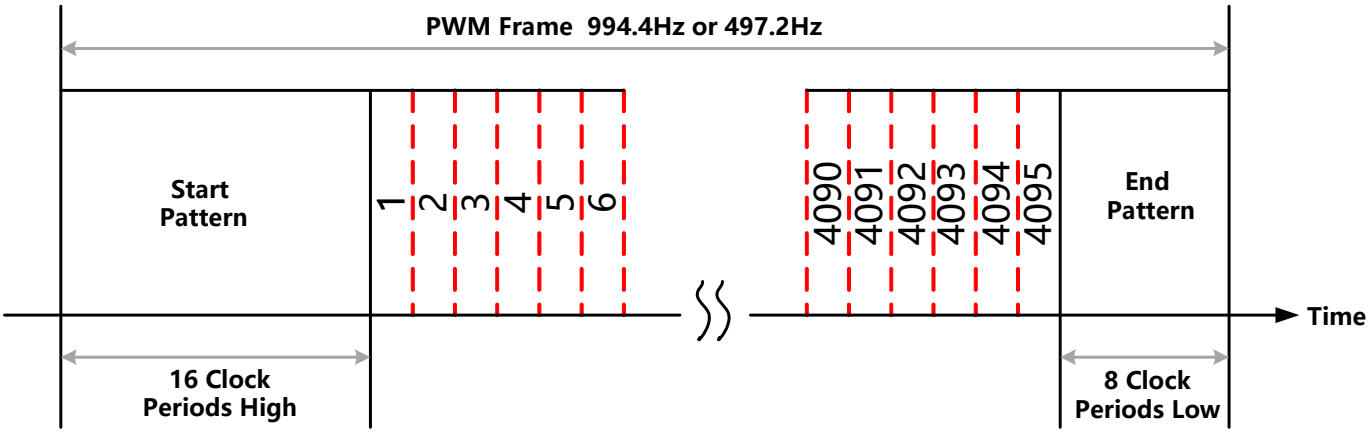


Figure 16: PWM Output Frame

PWM Frequency (EEPROM)

Reg. PWM_FREQ	PWM Frame Frequency
0	994.4 Hz
1	497.2 Hz

6.7 I²C Interface

The MT6701 provides a slave I²C interface for host MCU to read back digital absolute angle information from its internal registers. The reference circuit for I²C interface is shown in Figure 17, whether the need for pull-up resistor on SCL is determined by MCU, for MT6701 SCL is a digital input.

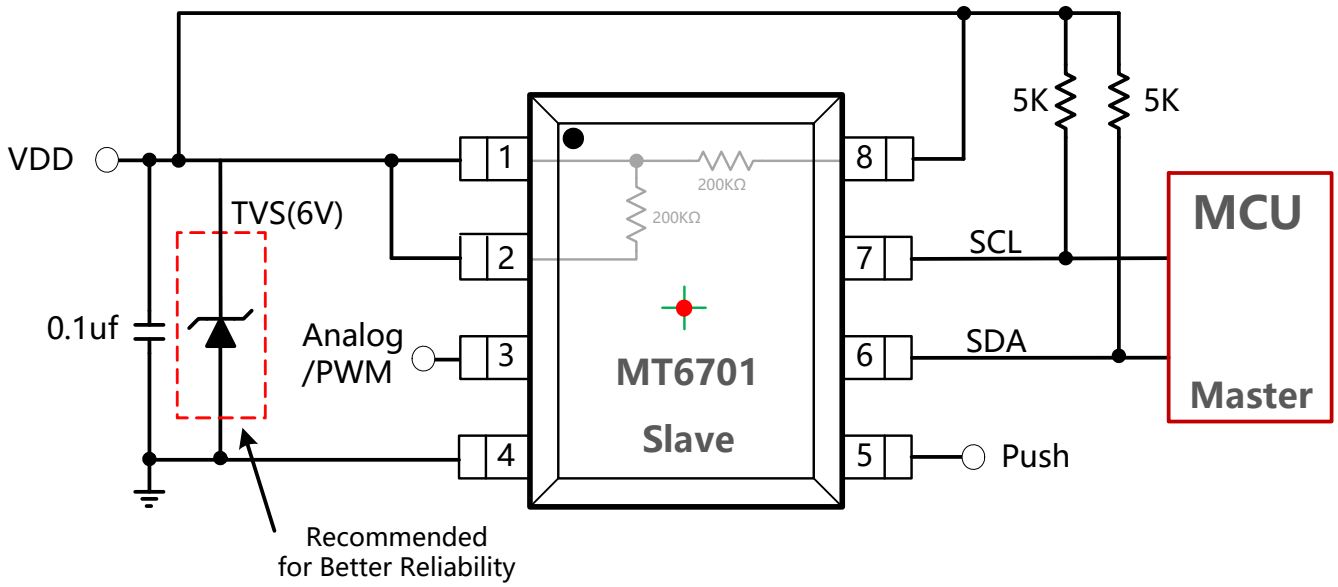


Figure 17: I²C Reference Circuit of SOP-8 Package

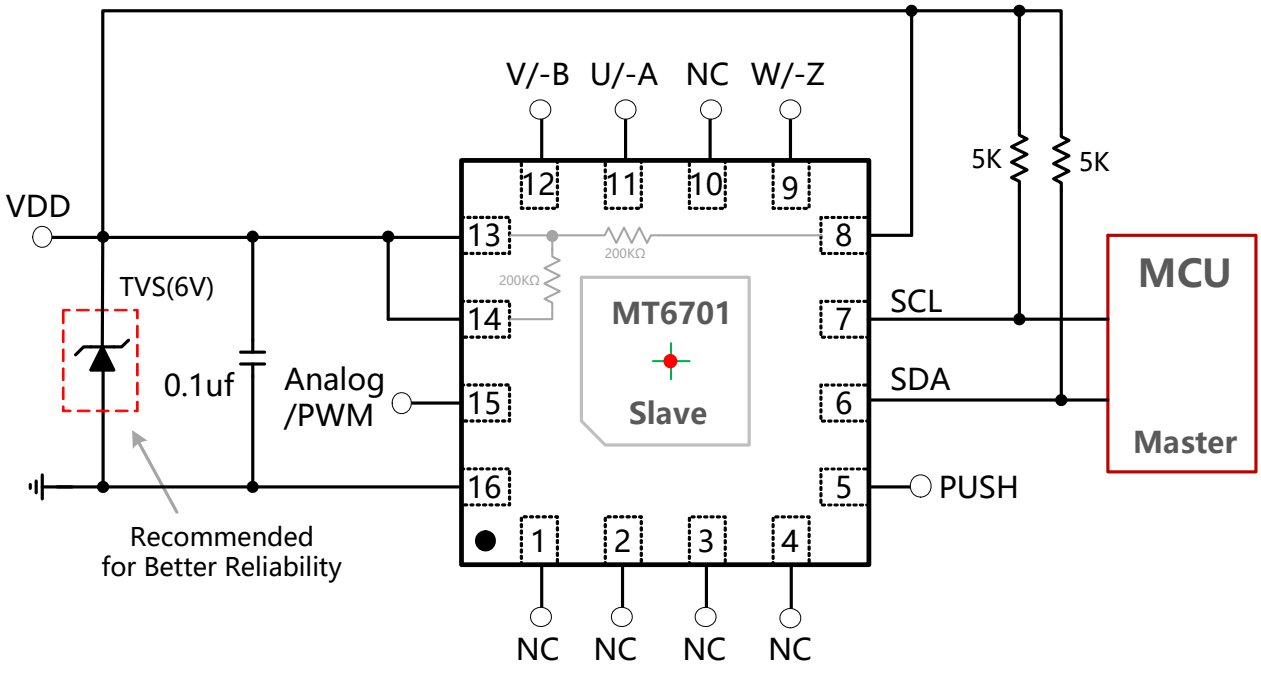


Figure 18: I²C Reference Circuit of QFN3x3 Package

6.7.1 I²C Timing Diagram

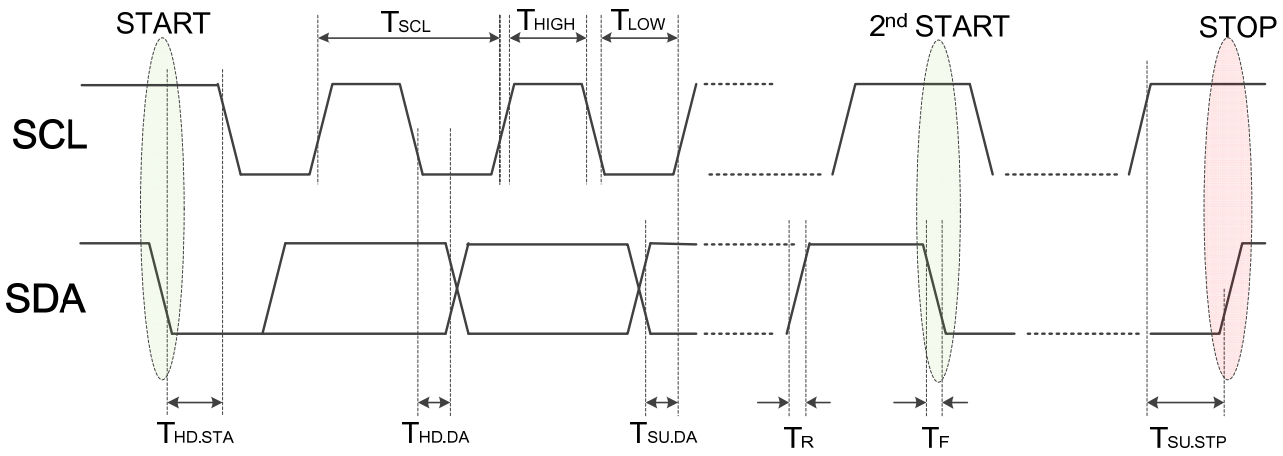


Figure 19: I²C Timing Diagram

I²C Timing Parameter

Parameter	Notes	Min.	Max.	Unit
T_{SCL}	SCL Clock Period	1	-	μs
$T_{HD.STA}$	Hold Time of 'START'	250	-	ns
T_{LOW}	Low Phase of SCL	250	-	ns
T_{HIGH}	High Phase of SCL	250	-	ns
$T_{SU.DA}$	Setup Time of SDA	100	-	ns
$T_{HD.DA}$	Hold Time of SDA	50	-	ns
T_R	Rising Time of SDA/SCL	-	150	ns
T_F	Falling Time of SDA/SCL	-	150	ns
$T_{SU.STP}$	Setup Time of 'Stop'	250	-	ns

6.7.2 I²C Read Angle Registers

The default slave ID of MT6701 is b' 0000110 in 7 bit binary form(It could be programmed to b' 1000110) . The 14 bits angle data is stored in internal register 0x03 and 0x04. Please follow the I²C timing of Figure 20 to read the angle data from 0x03 and 0x04 registers.

Note: Please read Register 0x03 first and then read 0x04

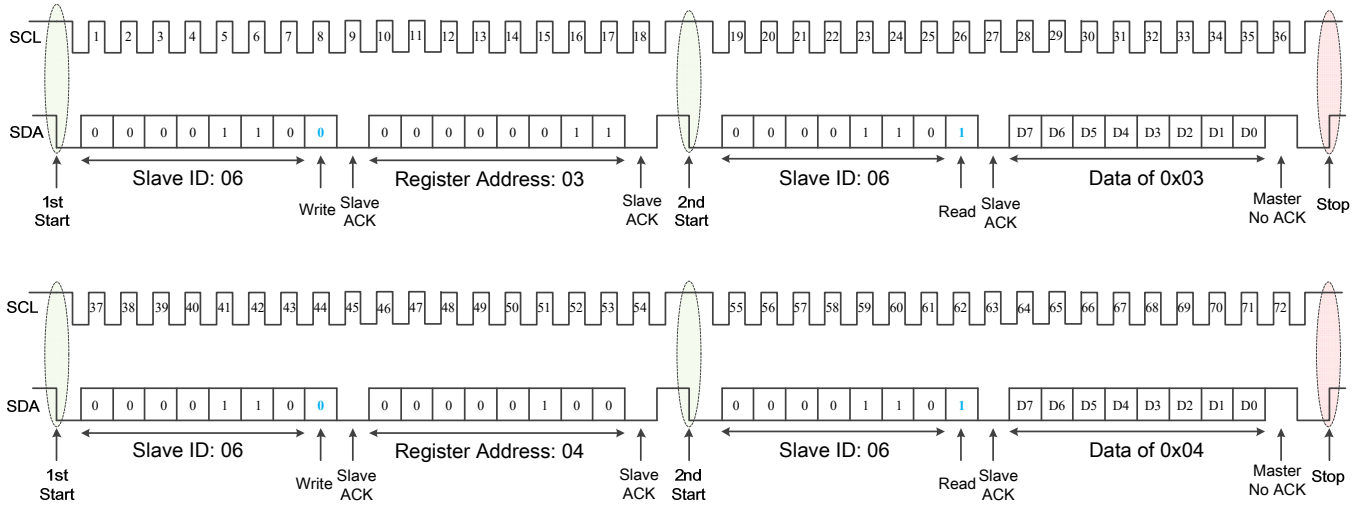


Figure 20: I²C Single Byte Read

Angle Data Register

Reg. Addresss	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	Angle<13:6>							
0x04	Angle<5:0>						NA	NA

0~360° absolute angle θ could be calculated by the below formula:

$$\theta = \frac{\sum_{i=0}^{13} Angle<i> \cdot 2^i}{16384} \cdot 360°$$

6.7.3 I²C Write

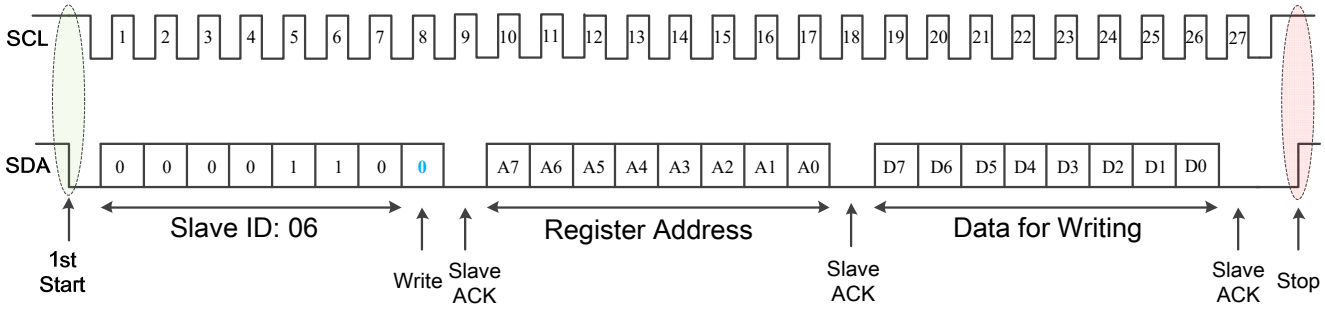


Figure 21: I²C Write

6.8 SSI Interface

The MT6701 also provides an SSI interface for host MCU to read back digital absolute angle information. The reference circuits for SSI interface are shown in Figure 22 and Figure 23.

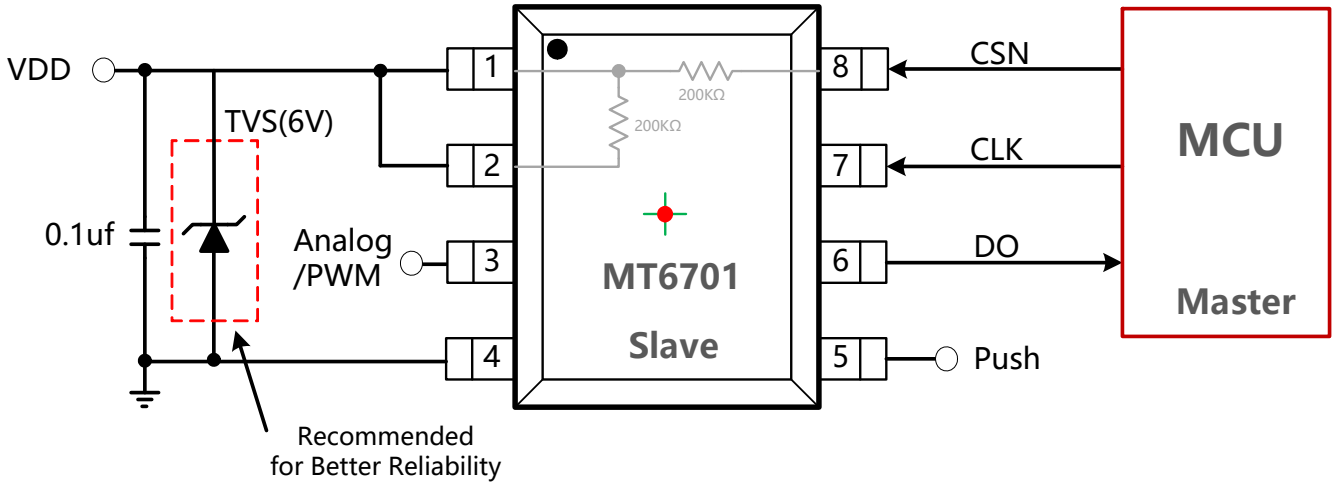


Figure 22: SSI Interface Reference Circuit of SOP-8 Package

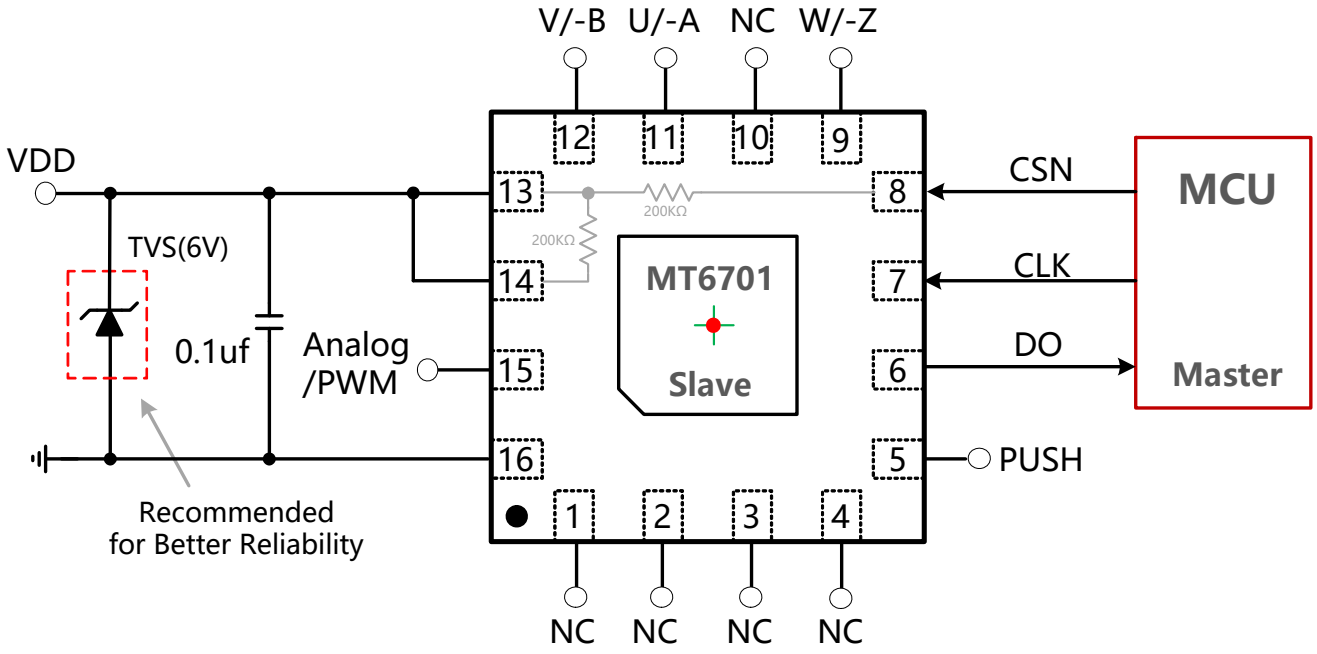


Figure 23: SSI Interface Reference Circuit of QFN-16 Package

6.8.1 SSI Timing Diagram

The MT6701 SSI is shown in Figure 24, a data transfer starts when CSN is pulled to logic 'Low'. The MT6701 transfers data on the falling edge of CLK, and the data transfer finally stops when CSN is pulled to logic 'High'

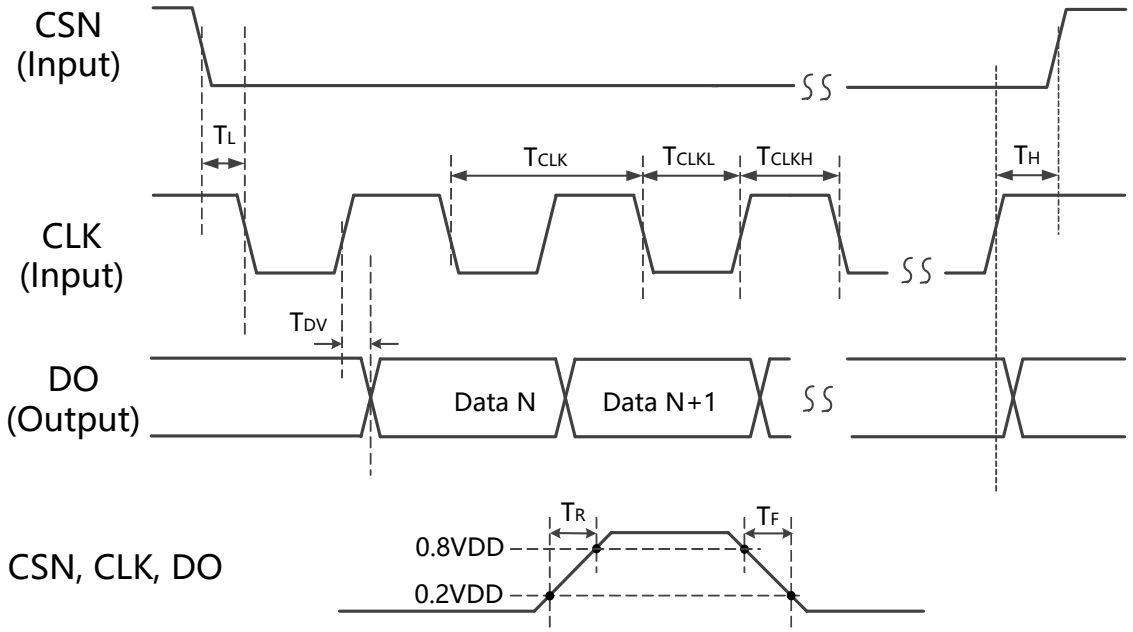


Figure 24: SSI Timing Diagram

SSI Timing Parameter

Symbol	Notes	Min.	Typ.	Max.	Unit
T_L	Time between CSN falling edge and CLK falling edge	100		-	ns
T_{CLK}	Clock period	64		-	ns
T_{CLKL}	Low period of clock	30		-	ns
T_{CLKH}	High period of clock	30		-	ns
T_H	Time between SCK last rising edge and CSN rising edge	$0.5 \cdot T_{CLK}$		-	ns
T_R	Rise Time of Digital Signal (with 20pf Loading Condition)	-	10	-	ns
T_F	Fall Time of Digital Signal (with 20pf Loading Condition)	-	10	-	ns
T_{DV}	Data valid time of MISO (with 20pf Loading Condition)	-	-	15	ns

6.8.2 SSI Read Angle

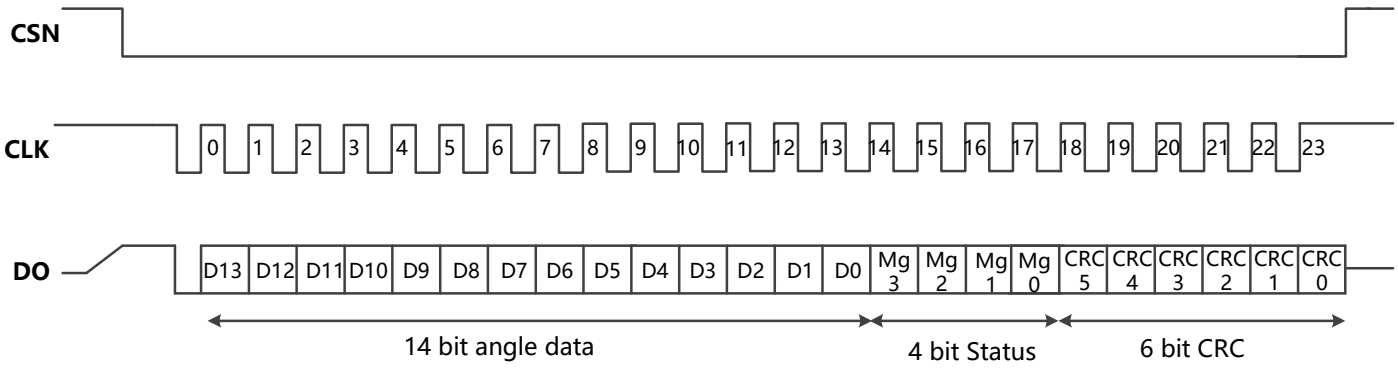


Figure 25: SSI Data Format

An SSI data transfer starts when CSN is pulled to logic 'Low', as shown in Figure 25. CLK is the Serial Port Clock and it is controlled by the SSI master; it is high when there is no SSI transmission. DO (Data Output) is the Serial Port Data Output from MT6701, it is driven at the rising edge of CLK and should be captured at the falling edge of CLK.

Bit 0-13: 14-bit Angle Data D[13:0]
Bit 14-17: 4-bit Magnetic Field Status Mg[3:0]
Bit 18-23: 6-bit CRC Code CRC[5:0]

0~360° absolute angle θ could be calculated by the below formula with D[13:0]:

$$\theta = \frac{\sum_{i=0}^{13} D<i> \cdot 2^i}{16384} \cdot 360°$$

Mg[3:0] Magnetic Field Status Truth Table:

Mg[1:0]	Status
0	Normal
1	Magnetic Field is too Strong
2	Magnetic Field is too Weak
3	-

Mg[2]	Status
0	Normal
1	Push Button is Detected

Mg[3]	Status
0	Normal
1	Loss of Track

CRC Data Range: D[13:0] and Mg[3:0] total 18-bit, D[13] is the MSB, Mg[0] is the LSB
CRC polynomials: X^6+X+1, MSB steam in first.

6.9 Pushbutton Output

The MT6701 implements a pushbutton detection function through a dynamic and relative measurement of the orthogonal magnetic field strength. This pushbutton detection function drives the PUSH output pin high when the MT6701 detects a fast (which is less than the time defined by 'PUSH_DIFF_DLY') increase of the magnetic field (which is larger than the percentage defined by 'PUSH_THRD'). After a fast decrease of the magnetic field, the PUSH output is driven low.

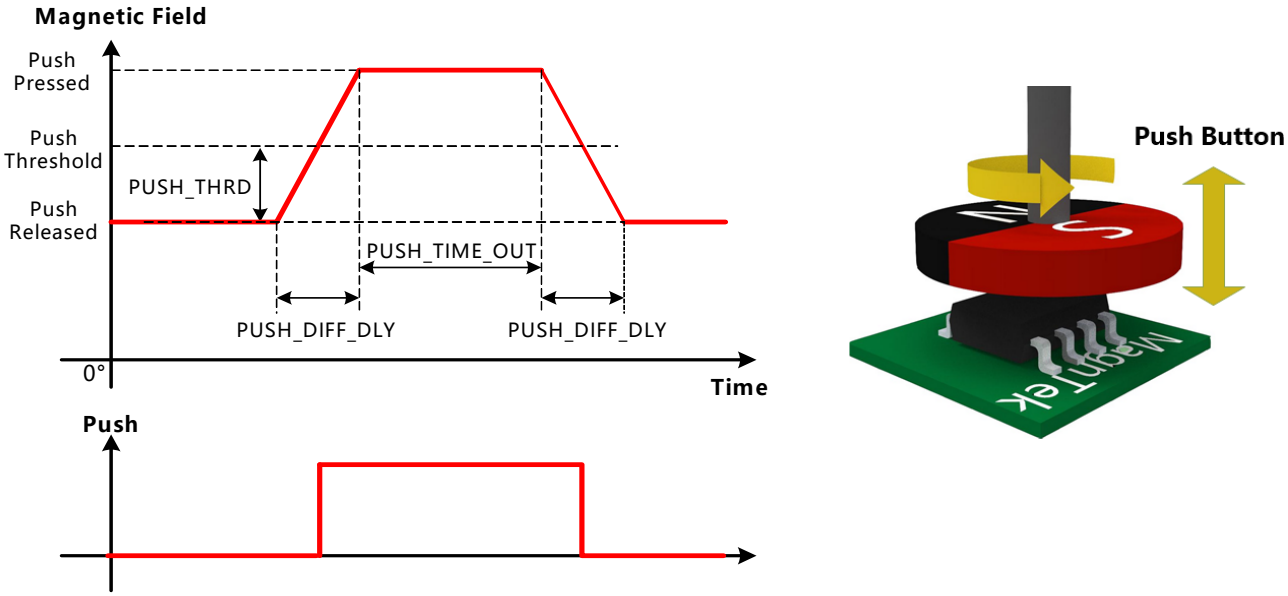


Figure 26: Pushbutton Function

PUSH_THRD Register (EEPROM)

Reg. PUSH_THRD	Change Percentage
0	+44%
1	+50%
2	+38%
3	+31%

PUSH_DIFF_DLY Register (EEPROM)

Reg. PUSH_DIFF_DLY	Time (Second)
0	0.5
1	0.25

PUSH_TIME_OUT Register (EEPROM)

Reg. PUSH_TIME_OUT	Time (Second)
0	8
1	16
2	4
3	2

7. Register Map & EEPROM Programming

7.1 EEPROM Register Map

Reg. Addr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x25	UVW_MUX							
0x29		ABZ_MUX					DIR	
0x30	UVW_RES[3:0]						ABZ_RES[9:8]	
0x31	ABZ_RES[7:0]							
0x32	HYST[2]	Z_PULSE_WIDTH[2:0]			ZERO [11:8]			
0x33	ZERO [7:0]							
0x34	HYST[1:0]							
0x38	PWM_FREQ	PWM_POL	OUT_MODE					
0x3E	A_STOP[11:8]				A_START[11:8]			
0x3F	A_START[7:0]							
0x40	A_STOP[7:0]							

Warning: the register bits which filled by ■ are reserved by MagnTek, please DO NOT change the value of these bits!!!

*UVW_MUX (Address 0x25[7])

UVW_MUX register contains the configuration data of UVW output type.

UVW_MUX	UVW Output Type(Only for QFN Package)
0x0	UVW
0x1	-A-B-Z

*ABZ_MUX (Address 0x29[6])

ABZ_MUX register contains data of ABZ output type.

ABZ_MUX	ABZ Output Type
0x0	ABZ
0x1	UVW

*DIR(Address 0x29[1])

DIR register contains the configuration data of output rotation direction

DIR	Output Direction
0x0	CCW
0x1	CW

*UVW_RES[3:0] (Address 0x30[7:4])

UVW_RES register contains the configuration data of UVW output resolution (Pole-Paris).

Reg. UVW_RES<3:0>	UVW Output Pole Pairs
0x0	1
0x1	2
0x2	3
.....	.....
0xD	14
0xE	15
0xF	16

*ABZ_RES[9:0] (Address 0x30[1:0] & 0x31[7:0])

ABZ_RES register contains the configuration data of ABZ output resolution (PPR).

Reg. ABZ_RES<9:0>	ABZ Resolution (Pulse per Round)
0x000	1
0x001	2
0x002	3
.....	.....
0x3FD	1022
0x3FE	1023
0x3FF	1024

*HYST[2:0] (Address 0x32[7] & 0x34[7:6])

HYST register contains the configuration data of hysteresis filter parameter.

HYST	Hysteresis (LSB)
0x0	1
0x1	2
0x2	4
0x3	8
0x4	0
0x5	0.25
0x6	0.5
0x7	1

*Z_PULSE_WIDTH[2:0] (Address 0x32[6:4])

Z_PULSE_WIDTH register contains the configuration data of Z pulse width (Fig.9 & Fig.10)

HYST	Z Pulse Width
0x0	1 LSB
0x1	2 LSB
0x2	4 LSB
0x3	8 LSB
0x4	12 LSB
0x5	16 LSB
0x6	180°
0x7	1 LSB

*ZERO[11:0] (Address 0x32[3:0] & 0x33[7:0])

ZERO register contains the configuration data of zero-degree position.

ZERO	Zero Degree Position
0x000	0°
0x001	0.088°
0x002	0.176°
...	...
0xFFD	359.736°
0xFFE	359.824°
0xFFF	359.912°

*PWM_FREQ (Address 0x38[7])

PWM_FREQ register contains the configuration data of PWM frame frequency

PWM_FREQ	PWM Frame Frequency
0x0	994.4 Hz
0x1	497.2 Hz

*PWM_POL (Address 0x38[6])

PWM_POL register contains data of PWM polarity.

PWM_POL	PWM Polarity
0x0	High Level Valid
0x1	Low Level Valid

*OUT_MODE(Address 0x38[5])

OUT_MODE register contains the configuration data of 'Out' Pin Mode

OUT_MODE	'Out' Pin Mode
0x0	Analog Output
0x1	PWM Output

*A_START[11:0] (Address 0x3E[3:0] & 0x3F[7:0])

A_START register contains the configuration data of start-point of analog output (Fig.15)

A_START	Analog/PWM Start Angle
0x000	0°
0x001	0.088°
0x002	0.176°
...	...
0xFFD	359.736°
0xFFE	359.824°
0xFFF	359.912°

*A_STOP[11:0] (Address 0x3E[7:4] & 0x40[7:0])

A_STOP register contains the configuration data of stop-point of analog output (Fig.15)

A_STOP	Analog/PWM Stop Angle
0x000	0°
0x001	0.088°
0x002	0.176°
...	...
0xFFD	359.736°
0xFFE	359.824°
0xFFF	359.912°

7.2 EEPROM Programming

Reg. Addr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x25	UVW_MUX							
0x29		ABZ_MUX					DIR	
0x30	UVW_RES[3:0]						ABZ_RES[9:8]	
0x31	ABZ_RES[7:0]							
0x32	HYST[2]	Z_PULSE_WIDTH[2:0]			ZERO [11:8]			
0x33	ZERO [7:0]							
0x34	HYST[1:0]							
0x38	PWM_FREQ	PWM_POL	OUT_MODE					
0x3E	A_STOP[11:8]				A_START[11:8]			
0x3F	A_START[7:0]							
0x40	A_STOP[7:0]							

Warning: the register bits which filled by ■ are reserved by MagnTek, please DO NOT change the value of these bits!!!

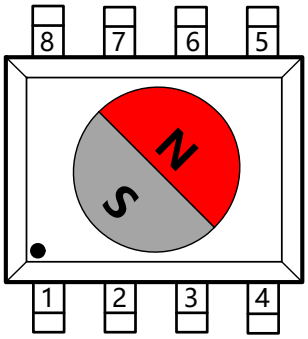
Customer can program the EEPROM registers by I²C interface (Fig.17 & Fig.18) and follow the below steps.

Step	Operation
Writing Register	Writing the right value to the target EEPROM registers (Do Not Change the ■ bits, customer should read out the ■ bits and logic these bits 'or' with others)
Programming Key	Write value '0xB3' to Register '0x09'
Programming Command	Write value '0x05' to Register '0x0A'
Programming	Waiting >600ms without any operation to MT6701
Check Programming Data	Power-down MT6701 and then power-up it again, read the EEPROM register to check if the data is successfully programmed

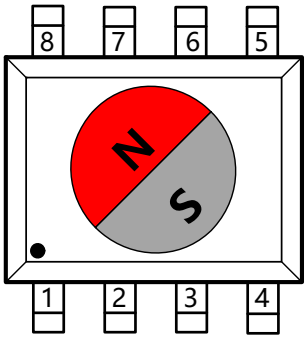
8. Mechanical Angle Direction

Top View

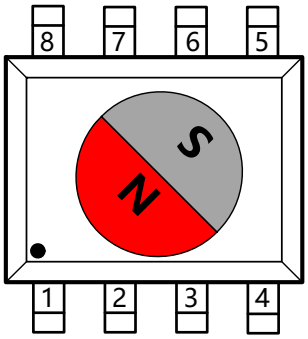
0 degree



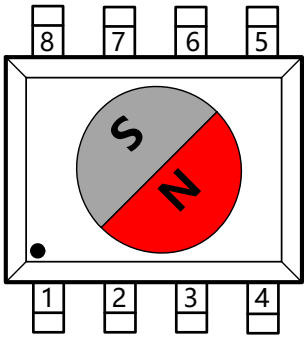
90 degree



180 degree

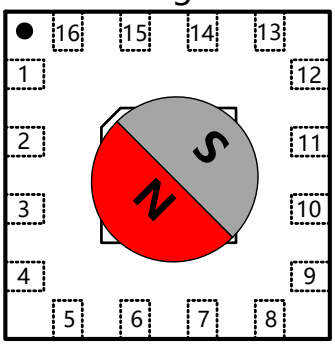


270 degree

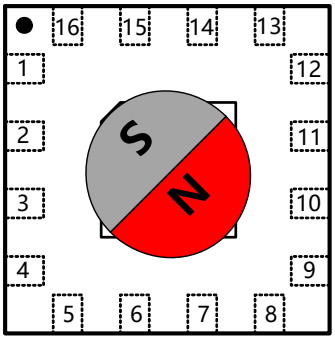


Top View

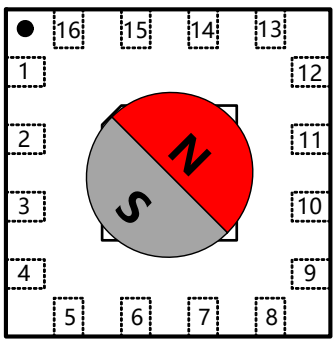
0 degree



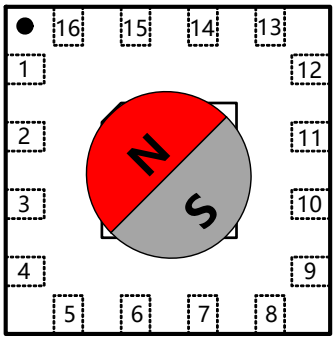
90 degree



180 degree

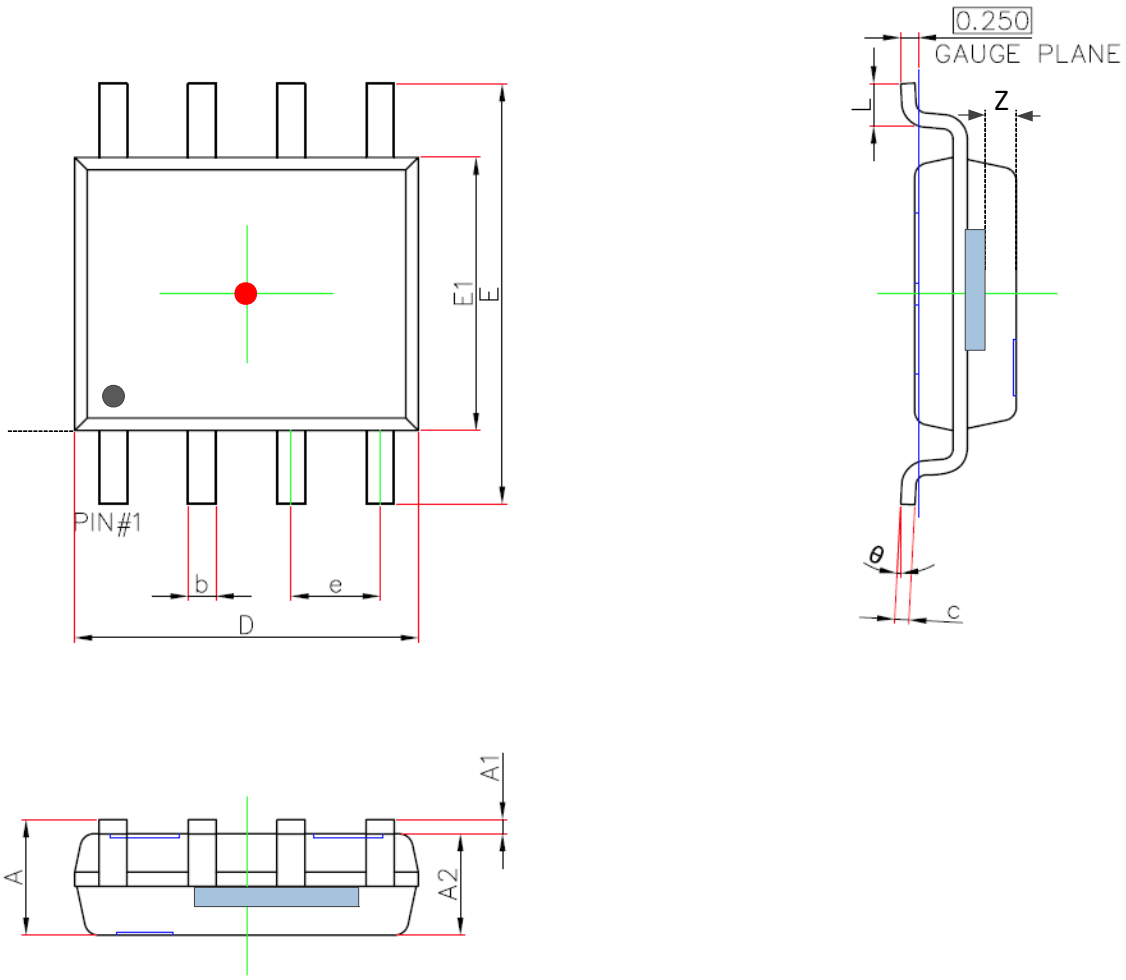


270 degree



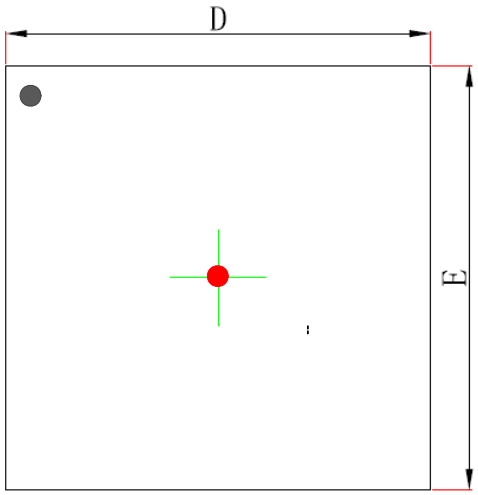
9. Package Information

9.1 SOP-8 Package

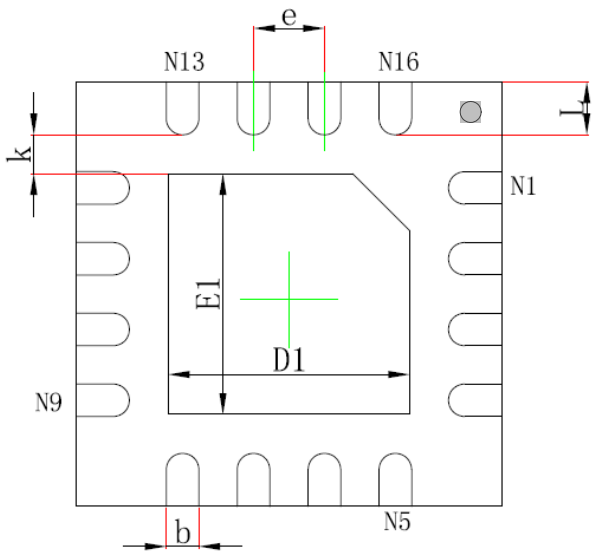


Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°
Z	0.42	0.62	0.016	0.024

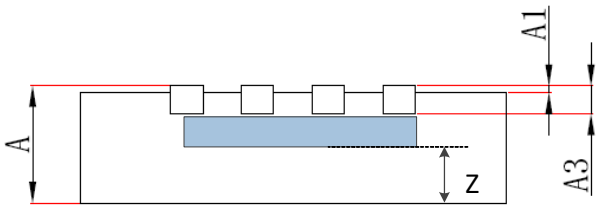
9.2 QFN-16 Package



Top View



Bottom View



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	1.600	1.800	0.063	0.071
k	0.275REF		0.011REF	
b	0.180	0.300	0.007	0.012
e	0.500REF		0.020REF	
L	0.300	0.500	0.012	0.020
Z	0.420	0.620	0.016	0.024

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11. Revision History

Revision Number	Date	Comments
1.0	2020.03	Initial Release