JMicron Technology Corporation

DATASHEET

JMS580
USB 3.1 Gen2 to SATA 6Gb/s Bridge Controller

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Revision History

Revision	Effective date	Description of revision		Author
		Reference	Detail of change	
0.10	11/18/2016	--	Initial release.	Seth Peng
0.20	02/09/2017	--	Grammar modifications	Seth Peng
0.30	03/06/2017	--	Modified VCCK/AVDDL voltage	Seth Peng
0.40	05/25/2017	--	Update typo and removed Vbus de-bounce description	Mika Cheng
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1.00	01/10/2017	2, 7.4	1. Update chapter 7.4 power dissipation 2. Removed feature “embedded 5V to 1.0V switch regulator”	Mika Cheng

Table of Contents

Figure List

Table List

1 Introduction

The JMS580 is JMicron's first USB 3.1 Gen 2 to SATA 6Gb/s bridge controller between USB host and SATA storage device. The USB 3.1 Gen 2 interface offers data transfer speed up to 10Gbps, doubling the USB Gen 1 data rate. Meanwhile, the downstream port of the JMS580 is compatible with storage device with SATA interface, such as HDD or SSD. The SATA port is compliant with SATA 6Gb/s specifications.

The JMS580 supports TRIM command for SSD and complies with USB Attached SCSI Protocol (UASP), providing much elevated performance for data transfer between USB and SATA devices.

USB Type-C™ connectivity is implemented in the JMS580 so that no additional component is required to enable Type-C™ connectivity when hardware system designers deploy this advanced controller. The built-in USB Type-C™ feature can save costs, PCB board space and development time for storage device developers.

Regarding power managements, the JMS580 is capable of working with specific power management controllers to develop a USB Power Delivery (PD) enabled device. For instance, a PD-enabled storage device with 3.5" HDDs can receive 12V from a PD-enabled host acting as the power provider to the device through the USB cable without additional plug-in. Designed with power management features, the JMS580 can meet the power consumption for a wide variety of applications such as data center, network attached storage (NAS), and thumb-sized Internet-of-Things (IoT) devices.

The JMS580 can be adopted with other JMicron SATA port multipliers, such as the JMB572, JMB575 to form medium-sized data storage for digital video recorder (DVR) and network video recorder (NVR) surveillance storages.

The JMS580 is compatible with the JMS576, and therefore provides a seamless upgrade to double USB bandwidth.

2 Features

- Integrates with USB Type-C™ multiplexer & configuration channel (CC) logic
- Complies with Serial ATA 6Gb/s Electrical Specification 3.2
- Supports TRIM for SSD
- Complies with USB 3.1 Specification Revision 1.0, USB BOT Specification
- Complies with USB UASP Specification
- Supports USB 2.0 High-Speed/Full-Speed Operation
- Supports USB2.0/USB 3.1 power saving modes
- Supports external SPI NVRAM for Vendor VID/PID of USB2.0/USB 3.1 device controller
- Supports ATA/ATAPI PACKET command set
- 12x GPIOs for customization
- Provides hardware controlled PWMs
- Provides software utilities for downloading the upgraded firmware code under USB2.0/USB 3.1
- Compatible with Windows 7, Windows 10 and MAC 10.10.5 or later version
- Supports 25MHz external crystal
- Supports 3.3V I/O
- Embedded 5V to 3.3V linear voltage regulator (LDO)
- QFN48 6x6 package

3 Block Diagram

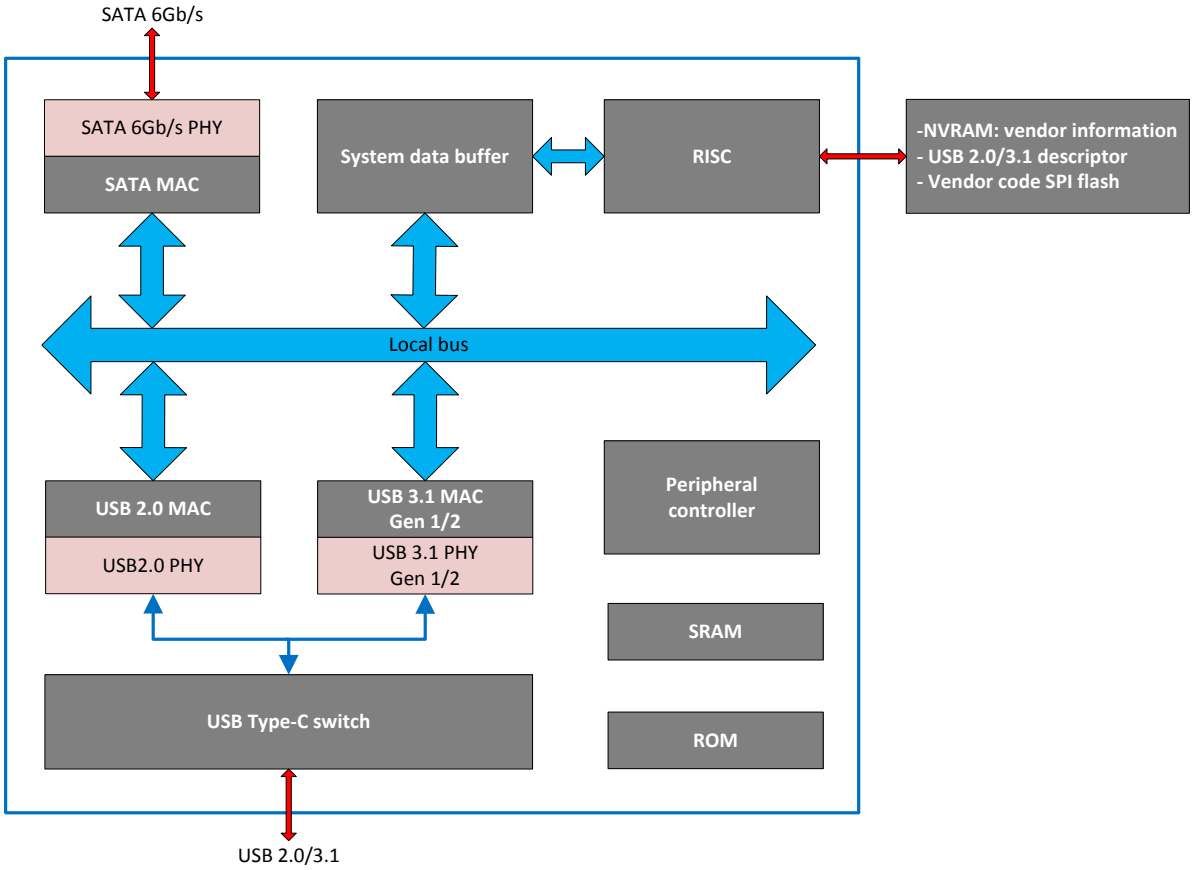
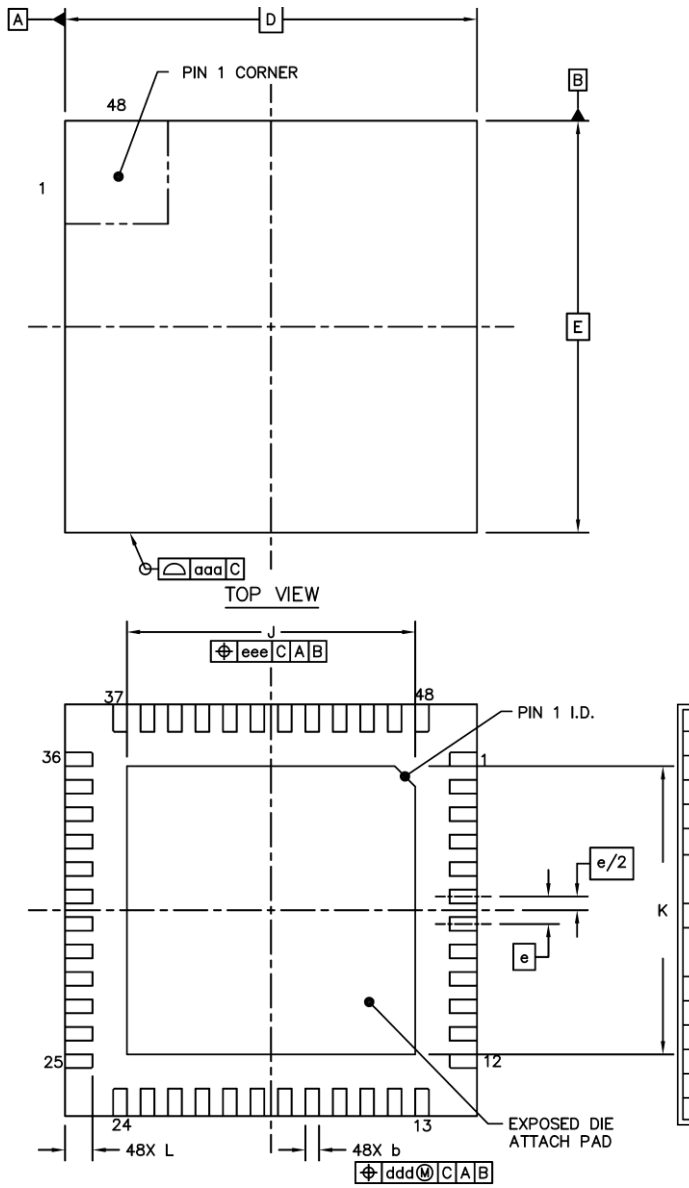


Figure 1 Block diagram

4 Package Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	4.1		4.4
	Y	K	4.1		4.4
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.1	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 2 Package outline drawing

5 Package Pin-out

5.1 Pin Assignment

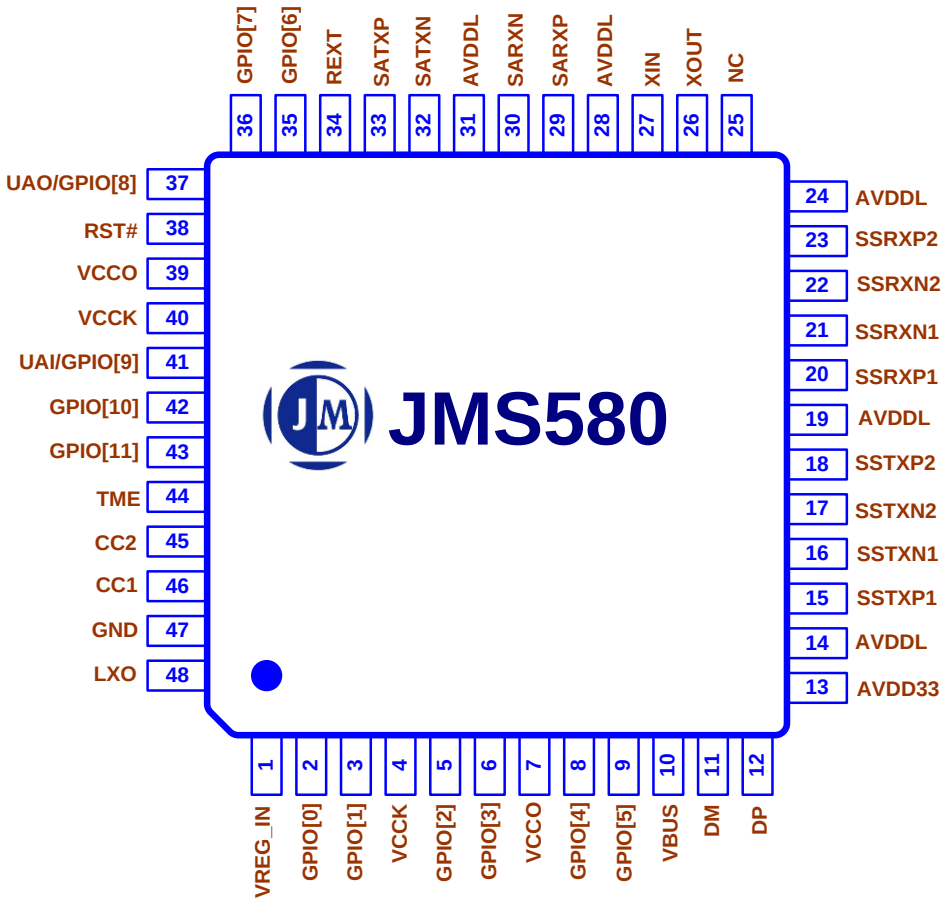


Figure 3 Pin assignment of JMS580

5.2 Pin Type Definition

Table 1 Pin type definition

Pin type	Definition
A	Analog
D	Digital
I	Input
O	Output
P	Power
IO	Bi-directional
L	Internal weak pull-low
H	Internal weak pull-high

5.3 Pin Description

5.3.1 Serial ATA Interface

Table 2 Pin description – Serial ATA interface

Signal name	QFN 48	Type	Description
SARXP	29	AI	**SATA Port RX+ Signal** A 10 nF capacitor should be placed between this pin and SATA connector.
SARXN	30	AI	**SATA Port RX- Signal** A 10 nF capacitor should be placed between this pin and SATA connector.
SATXN	32	AO	**SATA Port TX- Signal** A 10 nF capacitor should be placed between this pin and SATA connector.
SATXP	33	AO	**SATA Port TX+ Signal** A 10 nF capacitor should be placed between this pin and SATA connector.
REXT	34	AI	**External Reference Resistance** A 12 kΩ±1% external resistor should be connected to this pin.

5.3.2 USB 3.1 Interface

Table 3 Pin description – USB 3.1 interface

Signal name	QFN 48	Type	Description
SSRXP2	23	AI	**Super Speed RX+ 2 signal**
SSRXN2	22	AI	**Super Speed RX- 2 signal**
SSRXN1	21	AI	**Super Speed RX- 1 signal**
SSRXP1	20	AI	**Super Speed RX+ 1 signal**
SSTXP2	18	AO	**Super Speed TX+ 2 signal** A 100 nF capacitor should be placed between this pin and USB connector.
SSTXN2	17	AO	**Super Speed TX- 2 signal.** A 100 nF capacitor should be placed between this pin and USB connector.
SSTXN1	16	AO	**Super Speed TX- 1 signal.** A 100 nF capacitor should be placed between this pin and USB connector.
SSTXP1	15	AO	**Super Speed TX+ 1 signal.** A 100 nF capacitor should be placed between this pin and USB connector.

5.3.3 USB 2.0 Interface

Table 4 Pin description – USB 2.0 interface

Signal name	QFN 48	Type	Description
DM	11	AIO	USB 2.0 Bus D- Signal
DP	12	AIO	USB 2.0 Bus D+ Signal
VBUS	10	PI	USB 5V VBUS power for LDO input

Signal name	QFN 48	Type	Description
AV33O	13	PO	**USB 2.0 Analog 3.3V Output.** A capacitor to ground is recommended for this pin. The value should be 1 uF. The output voltage range is 3.3V±10%. **Note:** 1. This pin supplies power current lower than 100mA @ 3.3V. 2. This pin can only support internal power usage within the chip.

5.3.4 Crystal Interface

Table 5 Pin description – Crystal interface

Signal name	QFN 48	Type	Description
XIN	27	AI	**Crystal Input/Oscillator Input.** It is connected to a 25MHz crystal or crystal oscillator. The variation range should be around ±30ppm and the input voltage should lie within the range of 3.3V±5%.
XOUT	26	AO	**Crystal Output.** It is connected to a crystal. While crystal oscillator is applied, this pin should be reserved for No Connection (NC). The output variation range is around ±30ppm (input dependent) and the output voltage range should lie within 3.3V±5% (input dependent).

5.3.5 Switching Regulator Interface

Table 6 Pin description – Switching regulator interface

Signal name	QFN 48	Type	Description
VREG_IN	1	PI	**Voltage Regulator 5V Power Supply**
GND	47	P	**Voltage Regulator Ground**
LXO	48	PO	**Voltage Regulator 1.0V Output** Switch node. Connected with external power inductor with a value of 4.7 uH.

5.3.6 USB Type-C Configuration Channel

Table 7 Pin description - USB Type-C configuration channel

Signal name	QFN 48	Type	Description
CC1	46	AI	**CC pin1 input for voltage detection.** The maximum tolerant input voltage is 3.3V
CC2	45	AI	**CC pin2 input for voltage detection.** The maximum tolerant input voltage is 3.3V

5.3.7 Control and GPIO Interface

Table 8 Pin description – Control and GPIO interface

Signal name	QFN 48	Type	Description
RST#	38	DI	**System Global Reset Input.** Schmitt trigger input pin. Set active-low to reset the entire chip. An external RC should be connected to this pin.
TME	44	DI	**MP Test Mode Enable.** Schmitt trigger input pin. This pin is reserved for IC mass production testing. Keep this pin to logic “0” during normal operation.
GPIO[0]	2	DIOH	**Serial Flash (SO)** After power-on status detection, this pin becomes Data Output for serial flash. This pin is by default set to input.
GPIO[1]	3	DIOH	**Serial Flash (SCK)** This pin is Serial Flash Data Clock (SCK) of serial flash. This pin is set to output by default.
GPIO[2]	5	DIOH	**Serial Flash(SI)** Serial Flash Data Input (SI) of serial flash. This pin is set to output by default.
GPIO[3]	6	DIOH	**Serial Flash(CE0#)** This pin functions is configured as Chip Enable (CE0#) of Serial Flash
GPIO[4]	8	DIOH	**GPIO[4]** Configurable by customer firmware.
GPIO[5]	9	DIOH	**GPIO[5]** Configurable by customer firmware.
GPIO[6]	35	DIOH	**GPIO[6]** Configurable by customer firmware.
GPIO[7]	36	DIOH	**GPIO[7]** Configurable by customer firmware.

Signal name	QFN 48	Type	Description
UAO/GPIO[8]	37	DIOH	**RISC UART TX interface/GPIO[8]** Configurable by customer firmware.
UAI/GPIO[9]	41	DIOH	**RISC UART RX interface/GPIO[9]** Configurable by customer firmware.
GPIO[10]	42	DIOH	**GPIO[10]** Configurable by customer firmware.
GPIO[11]	43	DIOH	**GPIO[11]** Configurable by customer firmware.

5.3.8 Power Supply

Table 9 Pin description – Power supply interface

Signal name	QFN 48	Type	Description
VCCO	7, 39	PI	3.3V I/O power supply
VCCK	4, 40	PI	1.0V core power supply
NC	25		No connect
AVDDL	14, 19, 24, 28, 31	PI	Analog 1.0V power supply
GND	E-PAD	P	Ground

5.4 LED Indicator

By default, GPIO [4] is used as the LED for disk access indicator. If the user/system designer has a different application for LED indicator, please contact JMicron's AE before conducting PCB layout.

5.5 GPIO Initial Value

All GPIOs are set as input mode and internal pull-up function is disabled upon reset. Once reset, the firmware will program all GPIOs as input mode. Afterward, the initial value of GPIOs is read and stored in the system RAM for future use.

6 Clock and Reset

6.1 Crystal Input

Single crystal input (25MHz) is required.

Table 10 Crystal electrical specification

Parameter	Symbol	Min.	Typical	Max.	Unit
Crystal start up time v.s AVDDL	$\mathbf{T}_{Crystal}$			150	mS
Crystal Frequency	f_{clk}		25		MHz
Long term stability (Crystal Only)	$\Delta\mathbf{f}_{MAX\_Crystal}$	-30		30	ppm
Long term stability (On Board)	$\Delta\mathbf{f}_{MAX\_OnBoard}$	-150		150	ppm
Equivalent Series Resistance	**ESR**			55	Ω

6.2 Reset Input

All functions will be initialized upon reset except the Analog Power-On Reset Circuit, which is varied depending on the Power on-off. The reset input pin is the Schmitt trigger input pin. VT+ Schmitt Trigger Low to High threshold point is 2.2V and VT- Schmitt Trigger High to Low threshold point is 0.7V.

Table 11 Reset voltage

Parameter	Symbol	Condition	Min.	Typical	Max.	Unit
Reset voltage	V_{T+}	Low to High	2.2			V
Reset voltage	V_{T-}	High to Low			0.7	V

7 Electrical Characteristics

7.1 Absolute Maximum Rating

Table 12 Absolute maximum rating

Parameter	Symbol	Condition	Min.	Max.	Unit
Digital 3.3V	$VCCO_{(ABS)}$		-0.3	3.63	V
Digital 1.0V	$VCCK_{(ABS)}$		-0.3	1.1	V
Switching regulator	$AVDDS_{(ABS)}$		-0.3	5.5	V
Analog 1.0V	$AVDDL_{(ABS)}$		-0.3	1.1	V
USB VBUS	VBUS		4.0	5.5	V
Digital I/O input voltage	$V_{I(D)}$		-0.3	3.63	V
Storage temperature	$T_{STORAGE}$		-40	150	^{o}C

7.2 Operating Voltage and Temperature

Table 13 Operating voltage and temperature

Parameter	Symbol	Condition	Min.	Typical	Max.	Unit
Digital 3.3V power supply	VCCO		3.0	3.3	3.6	V
Digital 1.0V power supply	VCCK		1	1.05	1.1	V
Analog 1.0V power supply	AVDDL		1	1.05	1.1	V
Digital I/O input voltage	$V_{I(D)}$		0	3.3	3.6	V
Ambient operation temperature	T_A		0		70	^{o}C
Case operation temperature	T_C		0		105	^{o}C
Junction Temperature	T_J				125	^{o}C

7.3 External Clock Source Conditions

Table 14 External clock source conditions

Parameter	Symbol	Condition	Min.	Typical	Max.	Unit
External reference clock				25		MHz
Clock Duty Cycle			45	50	55	%

7.4 Power Dissipation

7.4.1 USB 2.0 to SATA mode

7.4.1.1 Idle

Table 15 Power dissipation – USB 2.0 to SATA idle mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @3.3V		3	5	mA
Digital 1.0V	VCCK	Operate @1.05V		60	80	mA
Analog 1.0V	AVDDL	Operate @1.05V		200	250	mA

7.4.1.2 Operating

Table 16 Power dissipation – USB 2.0 to SATA operating mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		3	5	mA
Digital 1.0V	VCCK	Operate @ 1.05V		62	80	mA
Analog 1.0V	AVDDL	Operate @ 1.05V		200	250	mA

7.4.1.3 Suspend

Table 17 Power dissipation – USB 2.0 to SATA suspend mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		1	3	mA
Digital 1.0V	VCCK	Operate @ 1.05V		8	15	mA
Analog 1.0V	AVDDL	Operate @ 1.05V		2.5	5	mA

7.4.2 USB 3.1 Gen1 to SATA mode

7.4.2.1 Idle

Table 18 Power dissipation – USB 3.1 Gen1 to SATA idle mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @3.3V		3	5	mA
Digital 1.0V	VCCK	Operate @1.05V		70	80	mA
Analog 1.0V	AVDDL	Operate @1.05V		255	285	mA

7.4.2.2 Operation

Table 19 Power dissipation – USB 3.1 Gen1 to SATA operation mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		3	5	mA
Digital 1.0V	VCCK	Operate @ 1.05V		81	100	mA
Analog 1.0V	AVDDL	Operate @ 1.05V		259	285	mA

7.4.2.3 Suspend

Table 20 Power dissipation –USB 3.1 Gen1 to SATA suspend mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		1	3	mA
Digital 1.0V	VCCK	Operate @ 1.05V		8	15	mA
Analog 1.0V	AVDDL	Operate @ 1.05V		3	6	mA

7.4.3 USB 3.1 Gen2 to SATA mode

7.4.3.1 Idle

Table 21 Power dissipation – USB 3.1 Gen2 to SATA idle mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @3.3V		3	5	mA
Digital 1.0V	VCCK	Operate @1.05V		97	120	mA
Analog 1.0V	AVDDL	Operate @1.05V		298	330	mA

7.4.3.2 Operation

Table 22 Power dissipation – USB 3.1 Gen2 to SATA operation mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		3	5	mA
Digital 1.0V	VCCK	Operate @ 1.05V		112	140	mA
Analog 1.0V	AVDDL	Operate @ 1.05V		302	330	mA

7.4.3.3 Suspend

Table 23 Power dissipation – USB 3.1 Gen2 to SATA suspend mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		1	3	mA
Digital 1.0V	VCCK	Operate @ 1.05V		8	15	mA
Analog 1.0V	AVDDL	Operate @ 1.05V		3	6	mA

7.5 I/O DC Characteristics

Table 24 I/O DC characteristics

Parameter	Symbol	Condition	Min.	Typical	Max.	Unit
Input low voltage	V_{IL}				0.7	V
Input high voltage	V_{IH}		1.5			V
Output low voltage	V_{OL}				0.3	V
Output high voltage	V_{OH}		1.9			V
Output Current	I_o				24	mA

7.6 V_{BUS} Detector

There are two parts for V_{BUS} de-bounce by VBUS (pin 10): One is hysteresis, and another is logic glitch filter.

Hysteresis:

- Switching threshold is 2.45V for high to low
- Switching threshold is 3.08V for low to high

7.7 Internal Linear Regulator

Table 25 Internal linear regulator specification

Parameter	Symbol	Condition	Min.	Typical	Max.	Unit
Input Voltage Range	V_{IN_LINEAR}			5		V
Output Voltage Range	V_{OUT_LINEAR}			3.3		V
Max Output Current	I_{MAX}		-	-	100	mA

7.8 Power-on Sequence

The power-on sequence is defined in **Figure 4** Designers should follow the following rules for external power designs.

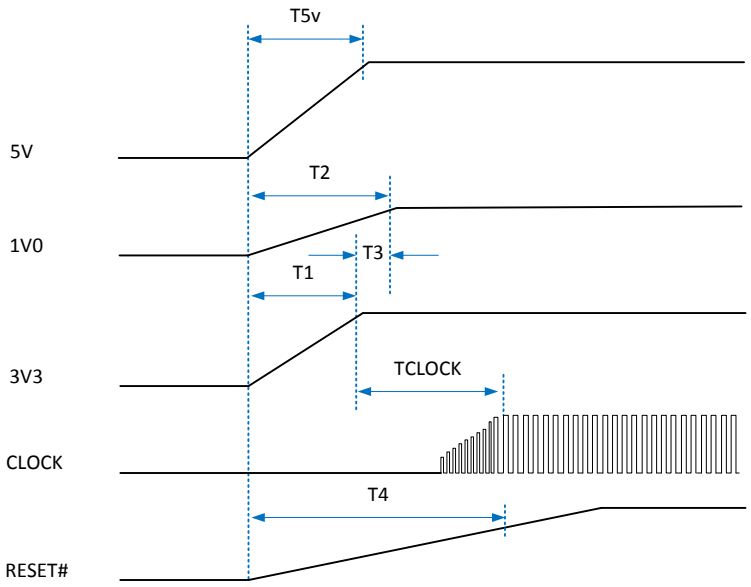


Figure 4 Power-on sequence

T_{5V}: Rise time for 5V power rail from 10% to 90%

T1: Rise time for 3V3 power rail from 10% to 90%

T2: Rise time for 1V0 power rail from 10% to 90%

T3: Time interval between 3V3 power and 1V0 Power

T4: Rise time for RST# signal from 0V to 2V2

$T_{Clock:}$ Time interval between 3V3 and 90% clock swing

Note: Clock must meet 25MHz +/-30ppm during the sequence.

The recommended power sequence and timing requirements are listed in **Table 2626**.

Table 26 Power-on timing requirements

Time Interval	Minimum	Maximum
T_{5V}	-	20 ms
T1	0.0 ms	10 ms
T2	0.0 ms	10 ms
T3	-5ms	5ms
T4	150 ms	500 ms
T_{CLOCK}	-	150.0 ms

The RESET timing constraint is based on the external RC reset circuits. To control the charge and discharge time for RC circuits, minimum and maximum requirements are defined. If designers apply timing control chip to control the reset signal, simply follow the minimum value. The maximum value can be ignored without further issues.

8 Product Naming Rule and Ordering Information

8.1 Format of the Part Number

The part number covers the information of the provider, product category, device number, package type, material type, product grade (based on operating temperature), mask ROM version and device version. The format of the part number is illustrated in **Figure 5** below.

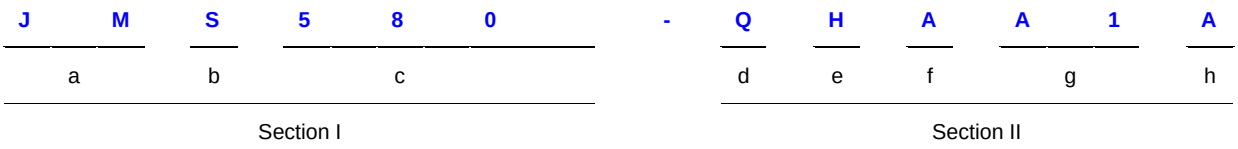


Figure 5 Format of the part number

8.2 Definition of the Part Number

Table 27 defines each section of the part number illustrated in **Figure 5**.

Table 27 Explanation of the part number

Section	Length	Designation	Code(s)	Definition
a	2 digits	Brand name	JM	**JM**icron
b	1 digit	Product category	S	**S**uper**S**peed USB
c	3 digits	Device number	580	The serial number assigned randomly to form the device name "**JMS580**" in conjunction with brand name and product category.
d	1 digit	Package type	Q	**Q**FN
e	1 digit	Material & grade	H	Ro**H**S compliant green product with JEDEC MSL 3 and commercial-grade operating temperature ranging from 0 to 70°C.
f	1 digit	Internal bonding type	A	Wire bonding option **A**
g	2 digit	Version of mask ROM	A1	Version **A1**
h	1 digit	Version of the IC	A	Version **A**