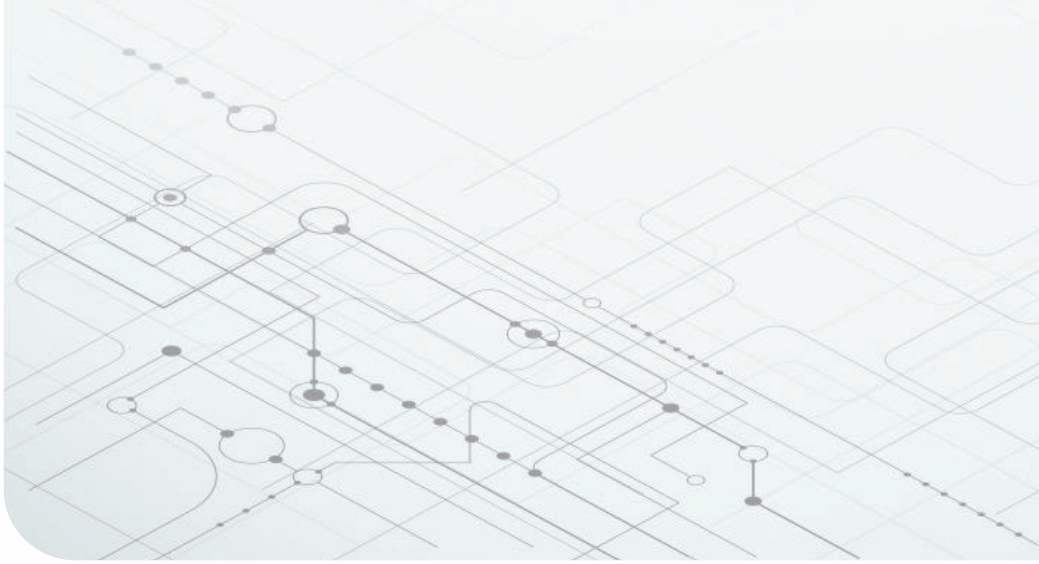
Overcoming Low-I_Q Challenges in Low-Power Applications

Keith Kunz
Distinguished Member Technical Staff
Design Engineer & Technologist, Linear Power

Stefan Reithmaier
Distinguished Member Technical Staff
Analog Design Manager, Boost & Multi Channel/Phase DCDC



TI POWER

Designers of ultra-low-power electronics today make constant trade-offs between higher performance and longer battery life. Despite improved battery capacities, the fundamental challenge remains: How do we achieve higher performance for longer periods of time?

At a glance

This paper examines the need for and associated challenges and solutions to reduce quiescent current (I_Q).

1 **What is I_Q?**

I_Q is the no-load quiescent current, and the most important bottleneck to overcome for duty-cycled low-power systems. Low I_Q enables longer battery life.

2 **Why low I_Q creates new challenges**

Reducing I_Q creates trade-offs in transient noise performance, die package area and output power range.

3 **How to break low-I_Q Barriers**

Reducing I_Q by decades without sacrificing performance or area requires a reexamination of both silicon technologies and circuit techniques.

Minimizing quiescent current (I_Q) is a key factor to reduce power consumption and manage battery life. An Internet-of-Things (IoT) sensor node is one of the best examples of why it's important to minimize I_Q to extend battery life. For example, in the low-power IoT application shown in **Figure 1**, the SimpleLink™ MCU controls a door lock via Bluetooth®, a Wi-Fi® connection or both.

Because these types of systems spend the majority (>99%) of the time in standby mode, as shown in **Figure 2**, the I_Q in standby or sleep mode tends to be the limiting factor for battery life. Careful optimization of low-I_Q power-management blocks makes it possible to extend battery life from two years to more than five years.

Standby I_Q has long been a concern, but historically solutions were limited to a narrow set of low-power systems. Recent breakthroughs reduced the I_Q in power-management building blocks like DC/DC converters, power switches, low-dropout regulators (LDOs) and supervisors, widening the use of these blocks to end equipment such as industrial meter applications, automotive sensors and personal wearables.

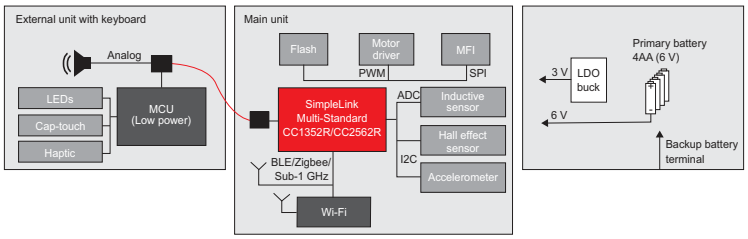


Figure 1. *Smart e-lock block diagram.*

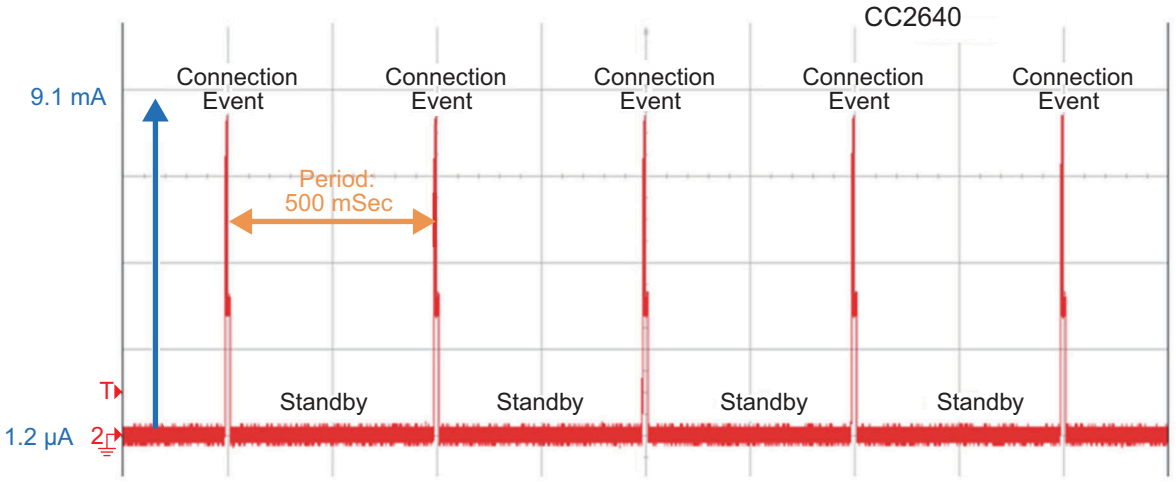


Figure 2. *Current consumption vs. time in a smart e-lock.*

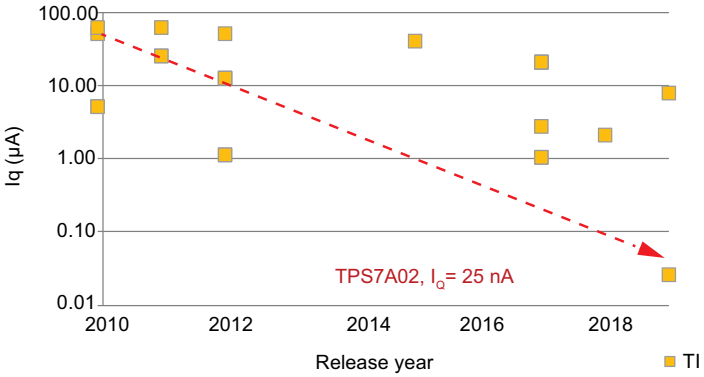


Figure 3. *5-V LDO I_Q over time.*

As **Figure 3** illustrates, the I_Q in 5-V LDOs has approximately reduced 90% every three years over the past 10 years. Both circuit improvements and optimized process technologies have enabled the reduction of solution area and improved transient-noise performance, while simultaneously reducing I_Q.

Contributors to I_Q

I_Q is the amount of current used when the integrated circuit (IC) is enabled but not switching nor supporting an external load current. Shutdown current (I_{SHDN}) is the current drawn from the supply when the device is disabled.

The I_Q of always-on functions such as power regulators contribute to the overall I_Q of systems with long standby times. Inside the power regulators themselves, the voltage reference, error amplifier, output voltage divider and protection circuits all have their own operating currents.

To determine the total I_Q drawn from a battery or power supply, you must consider the always-on functions and leakage sources from capacitors, resistors and inductors.

For the I_Q of switching converters, we must make some distinctions. Switching converters usually include a power-save mode that enables a longer non-switching period, thereby reducing average I_Q. But because the I_Q does not include switching currents or the efficiency component of currents drawn from the voltage output (V_{OUT}), like in the example of a boost converter in **Figure 4**, we can use **Equation 1** to calculate a superset of the input-referred no-load operating currents for almost any regulator as:

$$I_{I(standby)} = I_Q(V_{in}) + I_{Leakage}(V_{in}) + \frac{V_{out}}{V_{in} \, x \, \eta 1} \, x \left[I_Q(V_{OUT}) + I_{FB} + I_{LOAD} \right] \quad (1)$$

Currents and voltages are explained in **Figure 4**, where:

- I_Q (V_{IN}) is the V_{IN}-referred I_Q (the IC data-sheet value).
- ILeakage(V_{IN}) is the leakage drawn on the V_{IN} pin from capacitors, inductors, diodes or switches.
- V_{OUT} is the output voltage.
- V_{IN} is the battery voltage (the input voltage to the LDO, boost or buck-boost converter).

- $\eta 1$ is the DC/DC efficiency when the converter is switching.
- I_Q (V_{OUT}) is the I_Q drawn on the switching converter's V_{OUT} pin. For an LDO, I_Q (V_{OUT}) = 0.
- I_{FB} is the current of the feedback resistor divider, if applicable.
- I_{Load} is the load current potentially present on V_{OUT} in standby mode.

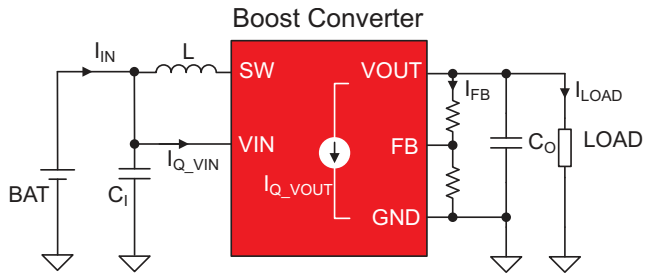


Figure 4. *Currents in a boost converter system.*

If you know the battery capacity and have calculated the input-referred standby current, **Equation 2** estimates the battery life for a heavily duty-cycled low-power system in standby mode >99.9% of the time as:

$$Battery\ Lifetime = \frac{Battery\ Capacity}{I_{I(standby)} + I_{Battery\ leakage}} \qquad (2)$$

For example, the battery of a duty-cycled system with 1.2 µA of standby current can last as 8.7 years on a 100-mAh coin-cell battery.

Why low I_Q creates new challenges

Let's look at some of the reasons why it's so challenging to reduce I_Q.

Transient response

Power-supply accuracy is often limited by its transient response, which is characterized by its maximum voltage drop, settling time and voltage error integral (**Figure 5**).

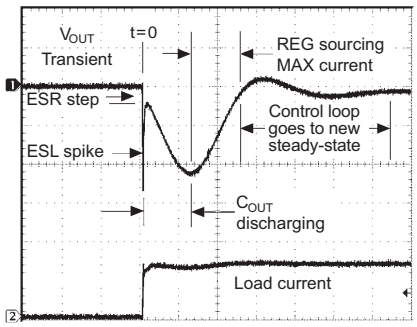


Figure 5. *An output voltage transient.*

The response time measures how fast a power device regulates back to the targeted output voltage after an abrupt change in load current or supply voltage. The response time comprises three stages: a delay time to react to the change, a recovery time from a dip or overshoot, and a settling time.

Low-I_Q devices suffer from longer response times because the internal parasitic capacitors need to be charged to new operating points with relatively less current. The worst case is usually a step from no load to the maximum allowed load current. Such cases necessitate reactivating circuits that had been deactivated or reduced in power, causing an additional delay.

More importantly, the settling time itself suffers from reduced bias conditions. For a conventional differential input stage, the gain reduces linearly with the bias current, which causes a reduction in bandwidth and increased settling time.

Calculating figures of merit (FOMs) helps the designer judge the overall performance of a power regulator. **Equation 3** calculates a transient response dip FOM, normalizing the I_Q by the maximum output current of the converter, the load current step (ΔI_O), the induced voltage drop (ΔV_O) and the output capacitor (C_O). **Figure 6** shows how FOM changes over time for a 5-V buck-boost converter. The smaller the FOM, the better the regulator's performance.

$$transient\ response\ dip\ FOM = \frac{I_Q \cdot \Delta V \cdot C_O}{I_{O\_MAX} \cdot \Delta I_O} \qquad (3)$$

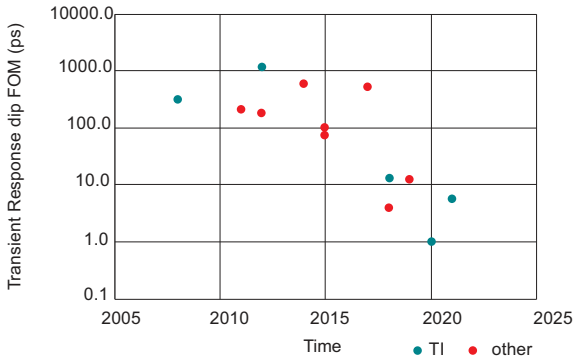


Figure 6. *Transient response dip FOM over time for a 5-V buck-boost converter.*

Ripple

Another way to enable lower I_Q is to enter different power-save modes depending on the load current. While the transition between these modes is usually automatic, the implementation and performance differ significantly. Two points of concern are the voltage ripple during the transition between power-save modes and the output-voltage accuracy. Because operating conditions (such as in an error amplifier) are usually different in each power-save mode, the transition time required to adjust to the different operating points can directly result in errors on the output voltage. Additionally, comparator delays will be longer at lower biasing currents, potentially causing inaccuracies for both the voltage threshold and zero-current detection, which could result in higher output-voltage ripple.

Noise

Another hurdle to overcome is the increased self-noise in amplifiers that accompany lower I_Q biasing. The internal blocks seen in **Figure 7** contributing the most noise in LDOs are the reference system (band gap), error amplifier and resistor-divider that scales the output voltage. **Figure 8** shows a typical noise profile vs frequency. The two main types of noise generated from these blocks are:

- Thermal noise (also called 4kTR noise) is a particular concern for ultra-low-I_Q designs because it is linearly proportional to the resistance used. Both resistor-derived bias currents used in the error amplifier and reference blocks, and the resistance used in resistor dividers, are dominant contributors to thermal noise at frequencies >1 kHz.
- Flicker noise (also called 1/f noise) is a low-frequency noise <100 Hz, that can be mitigated by increasing the sizes of differential pairs in the reference system and error amplifiers. This larger sizing however creates obstacles for nano-power designs, as they increase self-induced leakage and add more capacitance, which slows down response times.

A simple method to evaluate the resultant noise for a given I_Q is to multiply the integrated noise over the frequency range of concern and the I_Q at the operating point of interest. You can usually find both numbers on device data sheets.

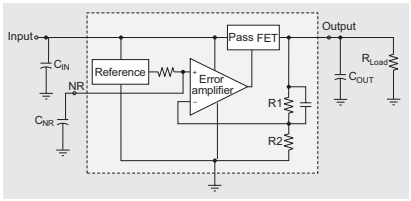


Figure 7. *Simplified LDO block diagram.*

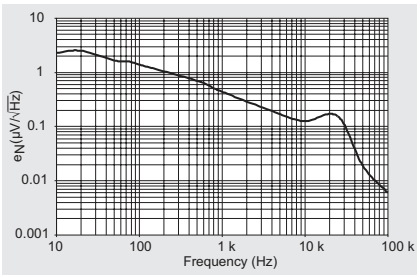


Figure 8. *Spectral noise density example.*

Die size and solution area

Decreased I_Q may also result in increased board area required for larger passives or IC package sizes. Larger external passives such as large-value capacitors for both LDOs and DC/DC converters are common in nanopower devices and typically used to compensate for poorer transient performance. Larger package areas are directly attributable to larger die areas.

Upon visual inspection of die teardowns with an I_Q <1 μA, resistors and capacitors make up more than

20% of the internal non-field-effect-transistor (FET) die area. While there are multiple solutions to solve I_Q-area problems, an easy method to filter out the best solutions on the market is to apply a simple FOM: I_Q multiplied by the smallest package area. You can access the FOM by pulling relevant information from data sheets; looking at the smallest package offered provides clues about smaller die areas.

Choosing the device with both the lowest I_Q and smallest package available usually means good I_Q-area efficiency.

Leakage and subthreshold operation

The goals of a nanopower process can conflict with the goals of high-performance deep-submicron technologies, which prioritize speed and gate density over I_Q reduction. While process technologies may vary, the vast majority of leakages come from large digital circuits, memory and high-power FETs. The accuracy of always-on circuitry tends to be limited to the controllability of components like resistors and capacitors and a mismatch between transistors. Not having the right components to address the leakage and control of always-on circuits manifests itself in large typical and worst-case I_Q and I_{SHDN} ratios across temperature. A dedicated low-power process technology with the right components can provide a clear manufacturing advantage.

One fundamental challenge is to reliably operate components biased in the subthreshold region. One common problem seen is increased random threshold voltage (V_T) mismatch. **Figure 9** shows a mechanism reported in literature that increases random mismatch by a thinning of oxide in the shallow trench isolation (STI) at the edge of the transistor. This parallel low-V_T edge transistor seen in **Figure 9**, distorts the V_T of the intentional transistor, resulting in much higher random mismatch for the most basic analog circuits like differential pairs and current mirrors. These mismatches can degrade the output voltage or mode control accuracy over temperature which can be clearly observed in the data sheet.

How to break low I_Q barriers

Optimizing I_Q requires the resolution of multiple, conflicting design challenges. You must meet all of the critical performance specifications in transient response, noise and accuracy, while reducing I_Q by orders of magnitude. Before assessing the trade-offs in performance specifications, you must quantify the I_Q and power losses over the entire output load range. For DC/DC switching converters, look at the power efficiency over load current, while for LDOs, look at current efficiency over load current.

As an example, **Figure 10** shows the efficiency of TI's **TPS63900** buck-boost converter versus competition. The efficiency for TPS63900 stays above 80% over six decades of load current, starting at 1 µA and hitting a peak efficiency of 96%.

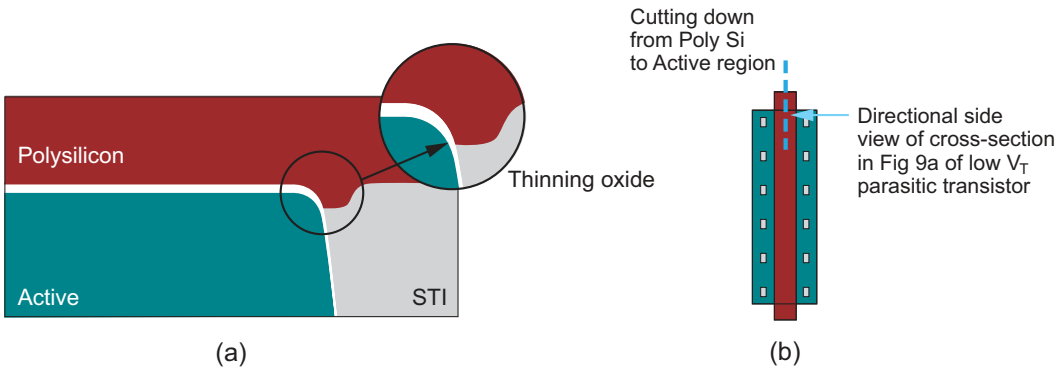


Figure 9. *Oxide-thinning-induced parasitic low-V_T in 2D cross-section (a); and layout view (b).*

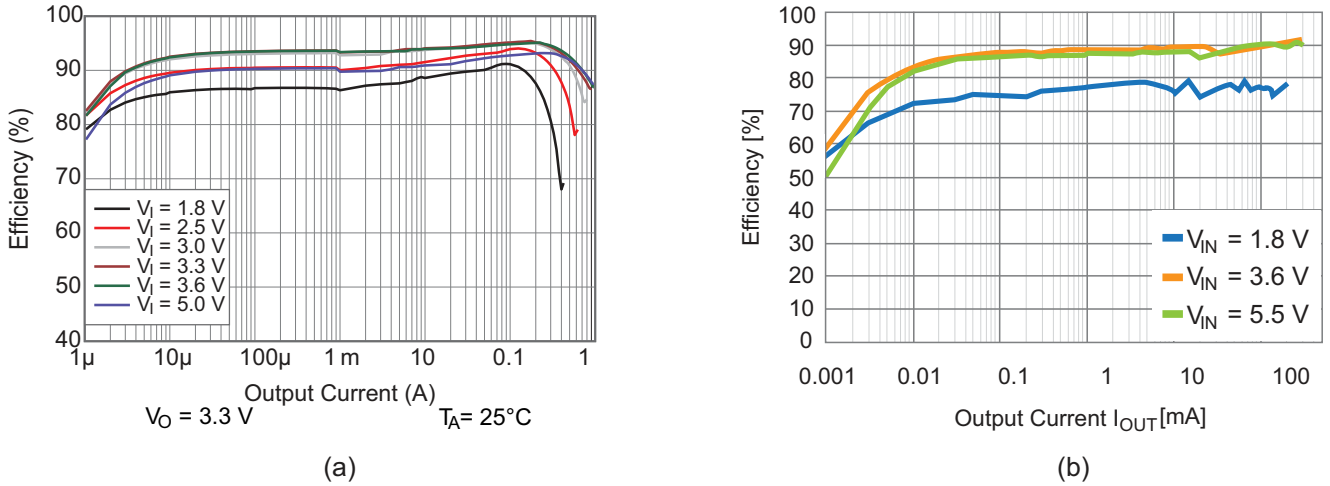


Figure 10. *Efficiency of the TPS63900 (a) and competition (b). (Source: TI and competitor data sheets).*

Addressing transient response issues

The key to improving the transient response is to start with the best topology. For example, the TPS61094 supports low I_Q and fast transient response. The TPS61094 is a bi-directional buck/boost converter that has a low I_Q of 60 nA in supercapacitor-charging (buck) and supercapacitor-discharging (boost) modes. The TPS61094 monitors dv/dt slopes at the output and adjusts its regulation behavior to optimize the transient performance at any given moment. This allows to quickly detect an output voltage drop while maintaining low I_Q at the same time. As a result, the output voltage will remain nearly constant when the TPS61094 starts supporting backup power or peak load support from a supercapacitor.

You must reduce the number of current-consuming blocks as much as possible, so the simpler the topology, the better. For example, the TPS63900 four-switch buck-boost converter, which has an I_Q of 75 nA, uses one single mode to regulate the output voltage above, below or equal to the input level. Besides the core architecture, using sample-and-hold techniques when entering light load minimizes the I_{SHDN} of all internal support functions.

You can conserve even more current with a zero-current feedback divider, digital assisted control and dynamic biasing. Dynamic biasing is a well-known technique, but becomes challenging when operating with just a few nanoamperes. To avoid the gain falloff at low bias currents, optimally shaping both the transconductance and output resistance as a function of the bias current achieves an I_Q-efficient constant gain amplifier.

Another technique uses fast startup circuits. By reducing the startup time of the sample-and-hold reference systems, the on time of the band-gap core and scaling amplifier circuits are reduced significantly. This improves the on-to-off time ratio, thus bringing the average current down in the nanoampere range while maintaining noise and accuracy levels.

To improve the line transient response, feed-forward techniques are applied to the voltage regulation loop in an energy-efficient way. Using transient detection circuits to adjust bias currents or enable circuitry further reduces both voltage dips at the output and settling times.

Figure 11 illustrates the application of these techniques in the TPS63900. The line transient is barely visible on the output voltage and far below the switching ripple, whereas other devices show 100-mV changes.

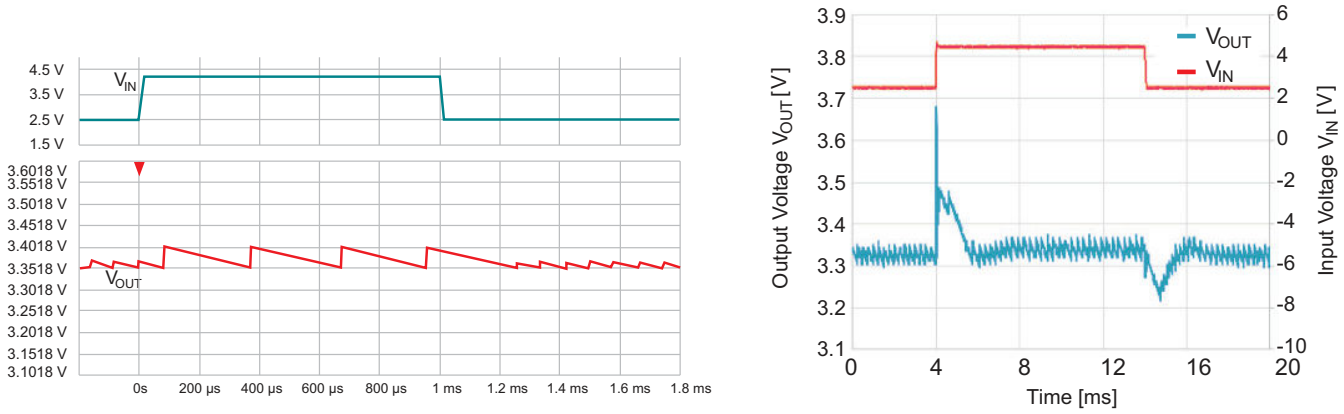


Figure 11. *Line transient response with V_{IN} = 2.5 V to 4.2 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA: TPS63900 (a); competing device (b).*

Addressing switching-noise issues

When designing a high-precision data application, one priority is to control the switching noise of the DC/DC converter, especially in power-save modes with transient bursts that generate a high output voltage ripple. One way to reduce ripple is to minimize the energy package sent to the output in a switching cycle. But what if that's not enough?

The **TPS62840** buck converter, which has an I_Q of 60 nA, has a STOP pin that immediately stops the regulator switching after the current switching cycle, opening a window of complete switching silence (see **Figure 12**).

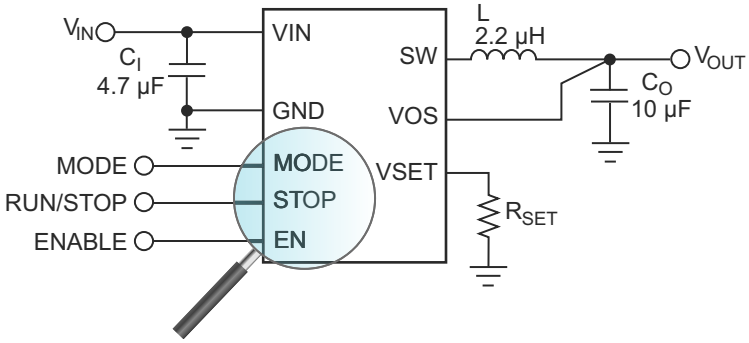


Figure 12. *Zero switching noise on the TPS62840 from the STOP pin feature.*

Addressing other noise issues

Beyond switching noise, continuous self-noise, with thermal and flicker noise components in the range of 0.1 Hz to 100 kHz, are of concern at lower I_Q biasing. Because the reference is usually the largest noise contributor, choosing integrated versions of sample-and-hold techniques to create both voltage and current references offer a compelling trade-off between area, noise, I_Q and robust performance (no drift) over the life of the device. The drawback of such sample-and-hold circuits are the small ripple errors created.

Figure 13 illustrates a design using TI's precision digital-to-analog converter (DAC) and operational amplifier families that attempts to optimize sample-and-hold operation so that any glitch created is well within the noise floor of the regulator in question. Some of these techniques are employed to remove the glitch and unwanted tones in **TPS7A02** LDO design. As shown in **Figure 14**, the TPS7A02 device's sample-and-hold noise-shaping reduces integrated noise >40% in the 10- to 100-Hz frequency band.

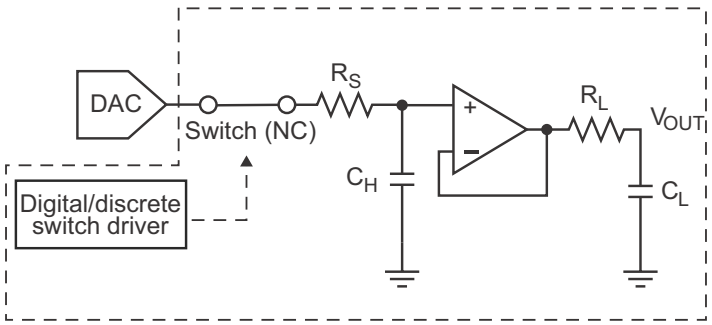


Figure 13. *Discrete sample-and-hold DAC system.*

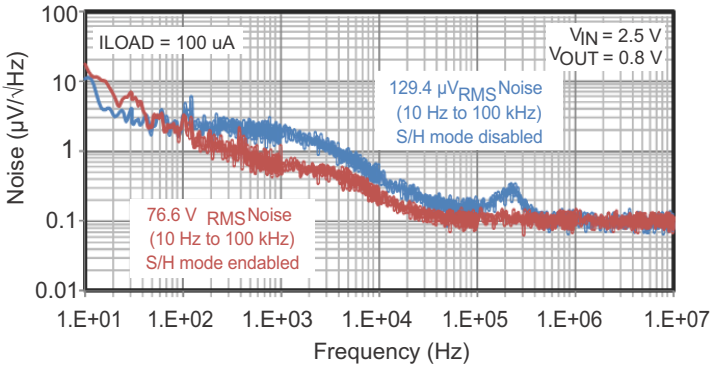


Figure 14. *Noise spectrum with and without a sample-and-hold reference on the TPS7A02. (Source: TI internal silicon measurements on the TPS7A02).*

Addressing die size and solution area issues

One of the largest-area blocks in nanopower regulators is the current reference, which is responsible for creating 1- to 10-nA bias legs. The current bias generation area within the current reference block is dominated by resistor components. Applying smaller voltage biases across small-value resistors will reduce resistor values. One technique generates $\Delta V_{gst}/R$ or $\Delta V_{be}/R$ circuits when forming a reference bias current.

Figure 15 shows a clever implementation of an almost zero-temperature coefficient bias current, creating positive and negative coefficient temperature bias currents with a small voltage bias across resistors R_1 and R_{bias}.

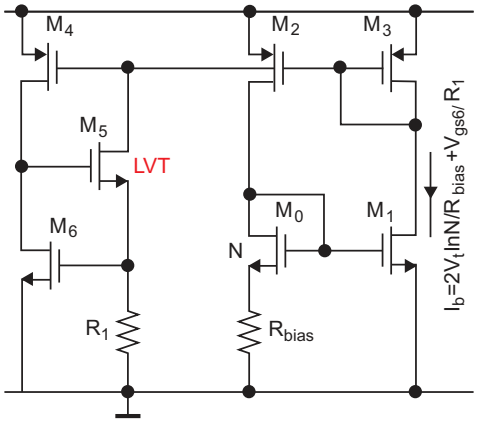


Figure 15. *Circuit diagram of low-area 1-nA current reference.*

These techniques enable a lower passive area, and effectively a smaller die area. The I_Q-multiplied-by-smallest-package-area FOM is the best way to compare the area efficiency of such techniques. The TPS7A02 device was released in a 1-mm-by-1-mm dual-flat-no-leads (DQN) package in 2019, while its wafer chip-scale package (WCSP) counterpart released in 2021. This LDO boasts one of the industry's lowest-I_Q-package-area-efficiency FOMs at <10 nA-mm^2. **Figure 16** demonstrates a side-by-side comparison of the typical 0402 capacitor vs the DQN and WCSP package offered for TPS7A02.

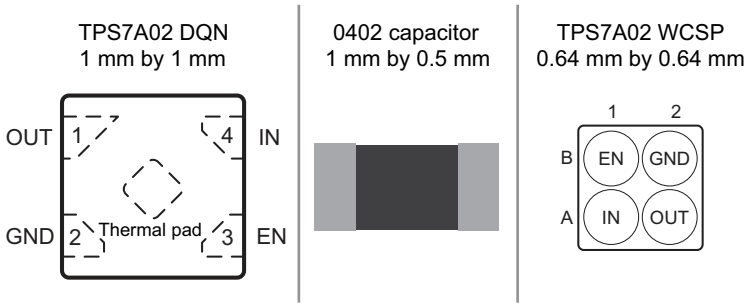


Figure 16. *Side-by-side size comparison of TPS7A02 in a DQN package, 0402 capacitor and WCSP package.*

When applying similar area-reduction techniques to supply voltage supervisors, the primary challenge will be how to sense voltages >10 V and still achieve I_Q levels <0.5 µA. Capacitive sensing of the monitored voltage, combined with sample-and-hold techniques, can reduce the die area and improve the response time. The **TPS3840** nanopower high-input voltage supervisor has an I_Q <350 nA, achieving a reset propagation delay as low as 15 µs while directly monitoring 10-V rails.

One of the most compelling ways to save board area is to integrate more functions onto a single die. This integration enables blocks like the supervisor, reference system, LDO, battery charger and DC/DC converter to share common building blocks while reducing the combined I_Q. **Figure 17** demonstrates the ability of the **BQ25125**, a battery charge management IC, to integrate and flexibly control multiple low-I_Q functions with I_2C, which gives it a key advantage to bring an entire power-management system to wearable, metering and automotive sensor IoT applications.

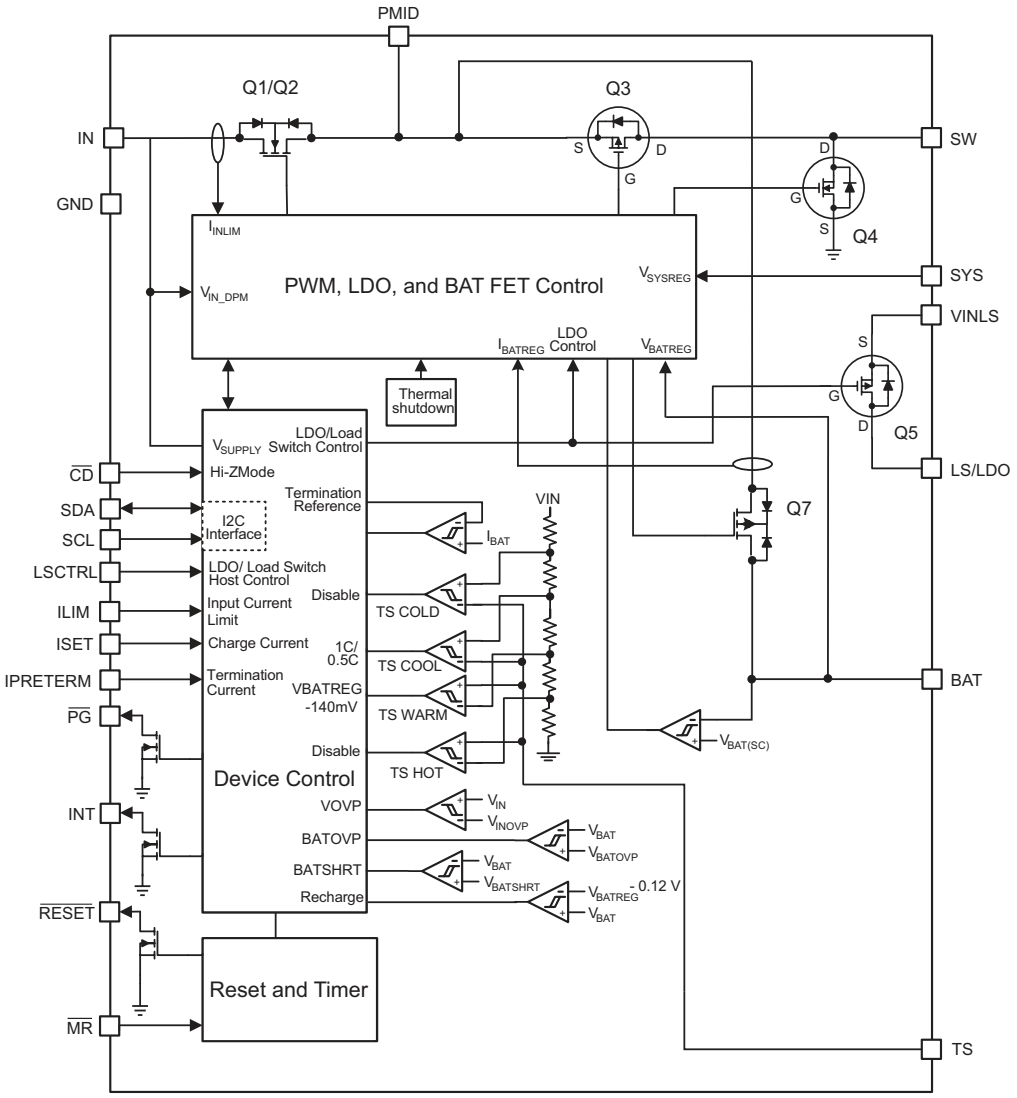


Figure 17. *System-level diagram of a nanoampere charger system.*

Addressing leakage and subthreshold operation issues

TI power process technologies feature optimized low-power design components. High-density resistors and capacitors combined with novel circuit techniques enable a reduction in both I_Q and die area. Power FETs and digital logic provide low-leakage transistors while simultaneously being optimized for speed; thus, I_{SHDN} and area are not exclusively compromised. Additionally, accurate modeling of subthreshold operation at lower V_{GS}-V_T levels – as shown in **Figure 18** – enables reliable operation down to the picoampere/micrometer biasing level.

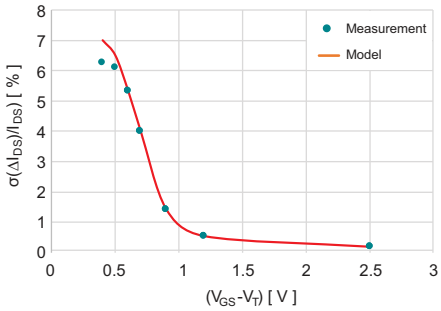


Figure 18. *Sigma IDS percentage mismatch vs. V_{GS}-V_T .*

Electrical Characteristics

Specified at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

Parameter		Test Conditions		Min	Typ	Max	Unit
	Nominal accuracy	TJ = 25°C, V_{OUT} ≥ 1.5 V, 1 µA(1) ≤ I_{OUT} ≤ 1 mA		-1		1	%
		TJ = 25°C; V_{OUT} < 1.5 V		-15		15	mV
	Accuracy over temperature	V_{OUT} ≥ 1.5 V	T_J = –40°C to +125°C	-1.5		1.5	%
		V_{OUT} ≥ 1.5 V		-20		20	mV
(ΔV_{IN})	Line regulation	$V_{OUT(nom)}$+ 0.5 V ≤ V_{IN} ≤ 6.0 V[1]	T_J = –40°C to +125°C			5	mV
ΔV_{OUT} (ΔI_{OUT})	Line regulation[2]	1 mA ≤ I_{OUT} ≤ 200 mA, V_{IN} = $V_{OUT(nom)}$ + 0.5 V[(2)]	T_J = –40°C to +85°C		20	38	mV
			T_J = –40°C to +125°C			50	
I_{GND}	Ground current	I_{OUT} = 0 mA	T_J = 25°C		25	46	nA
			T_J = –40°C to +85°C			60	
I_{GND}/I_{OUT}	Ground current vs load current	5 µA ≤ I_{OUT} < 1 mA	T_J = 25°C		1		%
		1 mA ≤ I_{OUT} < 100 mA			0.25		
		I_{OUT} ≥ 100 mA			0.15		
$I_{GND(DO)}$	Ground currentin dropout[3]	I_{OUT} = 0 mA, V_{IN} = 95% x $V_{OUT(nom)}$	T_J = 25°C		25		nA
I_{SHDN}	Shutdown current	V_{EN} = 0 V, 1.5 V ≤ V_{IN} ≤ 5.0 V, T_J = 25°C	T_J = 25°C		3	10	nA

Table 1. *Variation of I_{GND} and I_{SHDN} in the TPS7A02 data sheet.*

Variations in I_{Q-GND}, I_{SHDN} and V_{OUT} accuracy are all good indicators of the manufacturability of a process technology's components. **Table 1**, from the TPS7A02 data sheet, lists that I_{GND} at no load varies 25 nA to 60 nA over a -40°C to 85°C temperature range. This variation across temperature is representative of current mirror mismatch and I_{BIAS} generation control. The I_{SHDN}, which varies from 3 nA to 10 nA at room temperature, is a good indicator of power FET and digital logic leakage control. V_{OUT} accuracy is <1.5% over temperature, which is a good indicator of subthreshold mismatch control.

Avoiding potential system pitfalls in a low-I_Q designs

The leakage of external capacitors is a concern. Both the input and output capacitors of any regulator adds to I_Q. An excellent way to evaluate the leakage of external capacitors is described in **Figure 19**, where the voltage droop is measured on the capacitor vs. time for different capacitor insulation resistance (Rp) specifications. It's a good idea to measure the leakage on the capacitors independent of what the data sheet says. Charging a capacitor to a known voltage and monitoring the droop over time is an excellent way to quantify and compare different capacitor options. The capacitor with the largest insulation resistance will show the least droop over time.

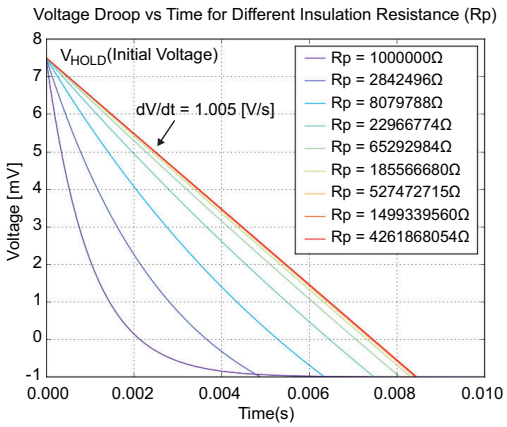


Figure 19. *Voltage droop vs. time for different insulation resistances.*

[1] V_{IN} = 2.0 V for V_{OUT} ≤ 1.5 V.
[2] Load Regulation is normalized to the output voltage at I_{OUT} = 1 mA.
[3] Specified by design

Besides capacitor leakages, the input impedance of a voltmeter can play a significant role in low-I_Q measurement setups and lead to incorrect results. Placed at the input or output of the power regulator, a typical 10-MΩ impedance voltmeter contributes 500 nA in the case of a 5-V supply or output voltage. This external leakage is 20 times more than the internal self-consuming I_Q of the 25-nA I_Q for the TPS7A02 LDO.

It is possible to avoid measurement errors with the correct measurement methods and the correct placement of volt and current meters. **Figure 20** shows the impact on efficiency with different test setups, which become quite significant already lower than a 0.1 mA load. For tips on the best options to avoid setup issues for ultra-low I_Q measurements, see the Analog Design Journal article, **" Accurately measuring efficiency of ultra-low-I $_Q$ devices**."

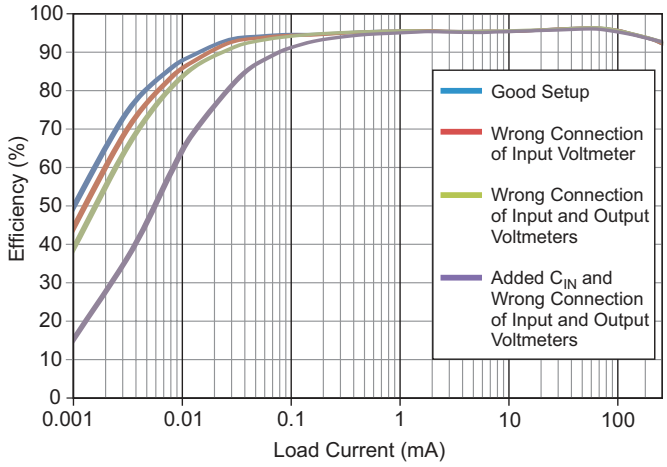


Figure 20. *Different efficiency measurement results dependent on the setup.*

Achieving low I_Q, but not losing flexibility

Flexibility is key in a low-power application design. One such example is changing the output voltage value. The traditional way is to use an adjustable external feedback divider, but this will cause not just higher inaccuracy but also higher I_Q. Modern nanoampere power converters use R2D interfaces (**Figure 21**), which enable the digitized setting of output voltages without consuming extra current, since the function will shut down after booting the device.

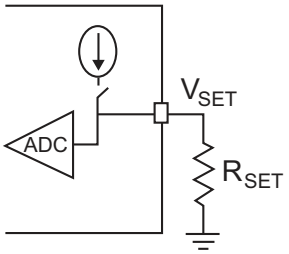


Figure 21. *R2D interface.*

Reducing external component count to lower I_Q in automotive applications

In harsh automotive environments, external resistors limit I_Q at the system level. Given requirements to prevent leakage, resistors are usually limited to lower than 100 kΩ. But you don't have to abandon your low-I_Q and I_{SHDN} ambitions. An external feedback divider monitoring 12 V will result in an I_Q in the >100 µA range. You could use an internal feedback divider with higher resistance to reduce the divider current, but at the cost of losing programmability.

The **LM5123-Q1** wide V_{IN} boost controller achieves lower I_Q by swapping the classical external feedback resistor and internal low-voltage reference, thus enabling low-value resistors at little expense. With this innovative placement of the voltage reference and feedback resistor, the 300-µA I_Q in the previous example drops by more than a factor of 20. See **Figure 22**.

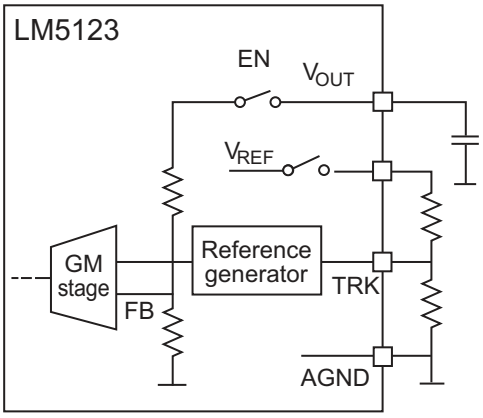


Figure 22. *Flexible programming in a low-IQ automotive environment.*

Similar to the LM5123-Q1, the LMR43610/20 36-V, 1-A/2-A buck converter utilizes a novel approach to minimizing I_Q by integrating the feedback network. The

LMR43610/20 runs an impedance check at startup on the VOUT/FB pin, which senses the presence of an external feedback network that engineers can employ to leverage the adjustable output voltage feature. If no external feedback resistors are detected, the device will automatically utilize the integrated feedback network that sets a fixed 3.3-V or 5-V output voltage. This minimizes leakages through the feedback network and lowers I_Q

Many switch-mode power devices like LMR43610/20 use an internal LDO to provide power to the internal circuitry for the IC. Low-voltage applications will typically supply this internal LDO directly from the input voltage. However, this method of powering the internal LDO poses a unique challenge in designs that operate across wide input voltage as the power loss from the LDO is directly proportional to input voltage.

To address it, rather than drawing power from the input, the LMR43610/20 leverages the same voltage from the VOUT/FB pin to power the internal LDO, which then biases all internal circuitry in order to minimize the total I_Q_VIN. This decreases the internal LDO current by a factor of V_{OUT} / (V_{IN} * η1). These features, paired with the methods discussed throughout this paper, enable the LMR43610/20 to have best-in-class I_Q of <3 µA (max.) at 150°C T_J, and light-load efficiency of almost 90% at 1 mA for nominal 12-V_{IN}, 3.3-V_{OUT}, 2.2-MHz conversions.

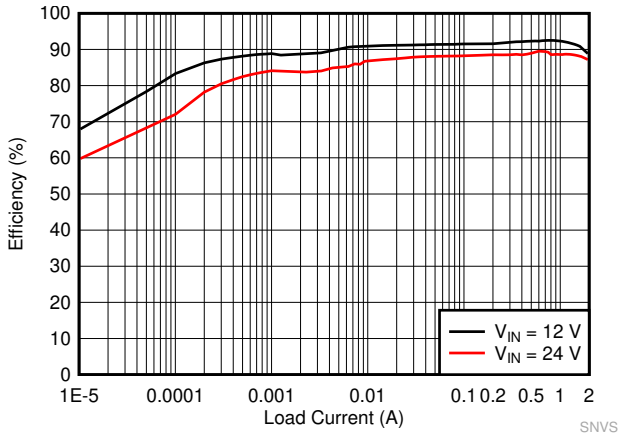


Figure 23. *Efficiency: VOUT = 3.3 V (Fixed), 2.2 MHz*

Smart on or enable features supporting low-I_Q at the system level

Device-level improvements can simplify system-level designs. One such example is the smart enable feature found on the **TPS22916**, a 60-mΩ, 10-nA leakage load switch. In addition to the ultra-low leakage and I_Q performance, this device also offers a smart way to turn the switch on. Usually there is an internal pulldown at the ON pin to ensure that the power switch does not turn on accidentally in case the microcontroller controlling the switch goes into a high impedance state. These pullup and pulldown resistors unfortunately negatively impact system-level I_Q.

As shown in **Figure 24**, the TPS22916, like many nano-I_Q products, has smart on or enable circuity that opens the pulldown path after soft start, eliminating the previous always-on I_Q and still guaranteeing a known low impedance state when the device is powered off.

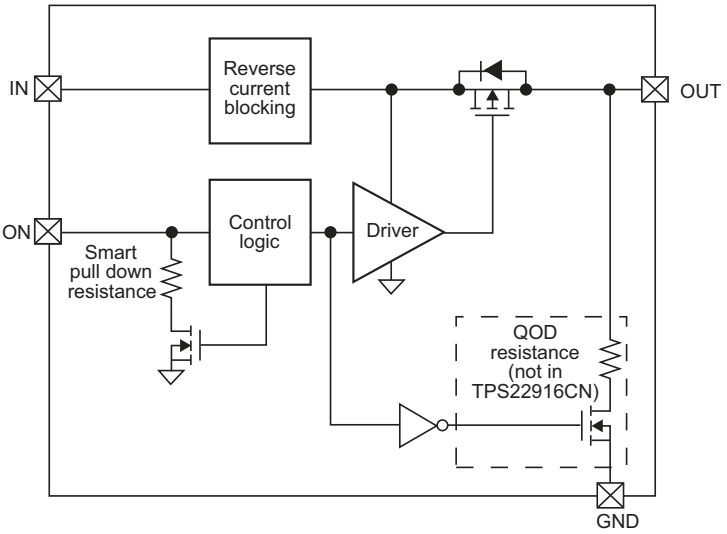


Figure 24. *Smart-enabled circuit guaranteeing low impedance for the ON pin when device is turned off.*

Conclusion

The trend toward lower currents is clear. The need to achieve high efficiency at no- or light-load conditions requires power solutions to tightly regulate the output while maintaining ultra-low supply current. With TI's portfolio of ultra-low I_Q technologies and products, you can maximize your battery run time and enable low power consumption in your next design.

The key benefits of TI technologies for low I_Q include:

- Low, always-on power — long battery run times, enabled by ultra-low leakage process technologies and novel control topologies.
- Fast response times — fast wake-up comparators and zero-I_Q feedback control enable fast dynamic responses without compromising low power consumption.
- Reduced form factors — area reduction techniques for resistors and capacitors facilitate integration into space-constrained applications while not affecting quiescent power

See **ti.com/lowiq** to learn more about how TI can help you extend battery and shelf life without compromising system performance.

Key product categories for low I_Q:

- **Battery charger ICs**
- **Buck-boost & inverting regulators**
- **Linear regulators (LDO)**
- **Power switches**
- **Series voltage references**
- **Shunt voltage references**
- **Step-down (buck) regulators**
- **Step-up (boost) regulators**
- **Supervisors & reset ICs**

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265