JMicron Technology Corporation

PCB LAYOUT GUIDE

JMS580
USB 3.1 Gen 2 to SATA 6Gb/s Bridge Controller

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Revision History

Revision number	Effective date	Description of revision		Author
		Reference	Description of change	
1.0	11/15/2016	--	Initial release.	Mika
1.1	05/22/2017	--	Delete CB17, Add C20 (7.1 Figure)	Mika
1.2	08/04/2017	--	Add rule for remove area under capacitors	Jason
1.3	09/19/2017	--	Add trace length limit for SATA3.0	Jason

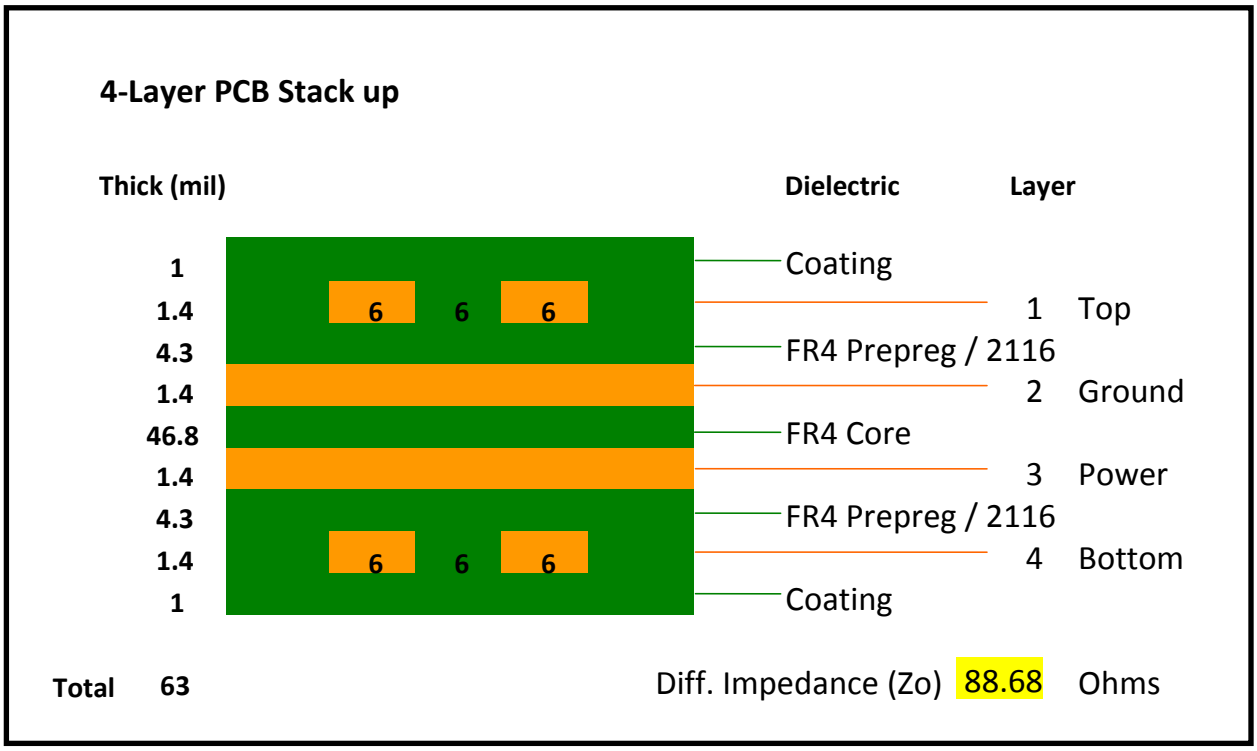
Table of Contents

1 Overview

1.1 Description

This layout guide includes USB3.1, SATA3.0, USB2.0, Power plane, Crystal and Switching Regulator.

1.2 PCB stack up



2 USB3.1 layout guide

2.1 Relative net name & pairs

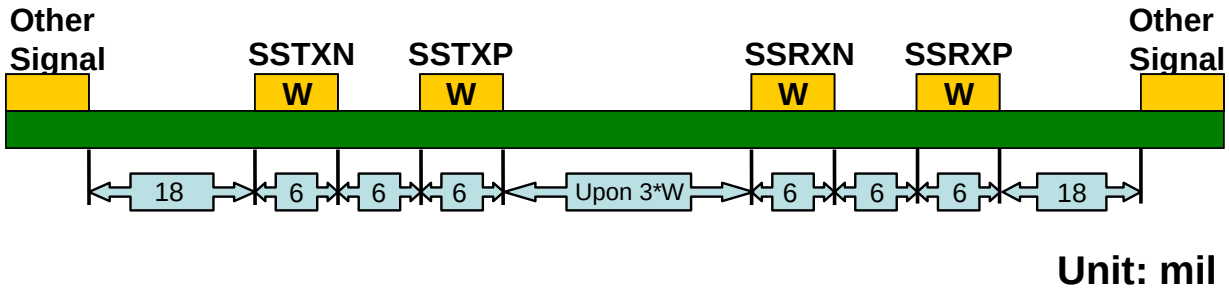
USB3.1 have 2 differential signal pair，detailed information is as follows:

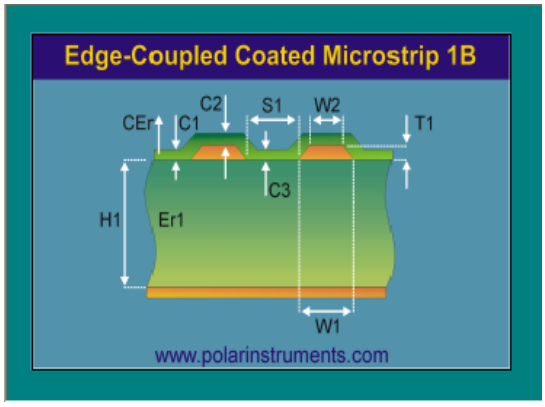
Net name	Routing layer	Reference layer
SSTXP, SSTXN, SSRXN, SSRXP	1st layer	2nd layer (GND)

2.2 Net spacing & trace length rule

- USB Trace : Trace width / trace separation / pair separation ＝ 6 / 6 / 18.0 mil

  Target differential impedance: 89 Ω





				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	4.3000	+/-	0.0000	4.3000	4.3000
Substrate 1 Dielectric	Er1	4.3000	+/-	0.0000	4.3000	4.3000
Lower Trace Width	W1	6.0000	+/-	0.0000	6.0000	6.0000
Upper Trace Width	W2	6.0000	+/-	0.0000	6.0000	6.0000
Trace Separation	S1	6.0000	+/-	0.0000	6.0000	6.0000
Trace Thickness	T1	1.4000	+/-	0.0000	1.4000	1.4000
Coating Above Substrate	C1	1.0000	+/-	0.0000	1.0000	1.0000
Coating Above Trace	C2	1.0000	+/-	0.0000	1.0000	1.0000
Coating Between Traces	C3	1.0000	+/-	0.0000	1.0000	1.0000
Coating Dielectric	CEr	3.4000	+/-	0.0000	3.4000	3.4000
Differential Impedance	Zdiff	88.68			88.68	88.68

- USB3.1 trace length mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.
- Route all SuperSpeed USB signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Do not route SuperSpeed USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

3 SATA3.0 layout guide

3.1 Related net name & pairs

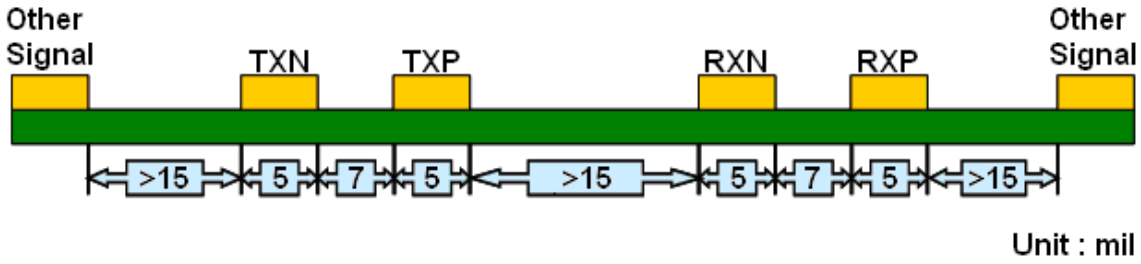
SATA3.0 have 2 differential signal pair，detailed information is as follows:

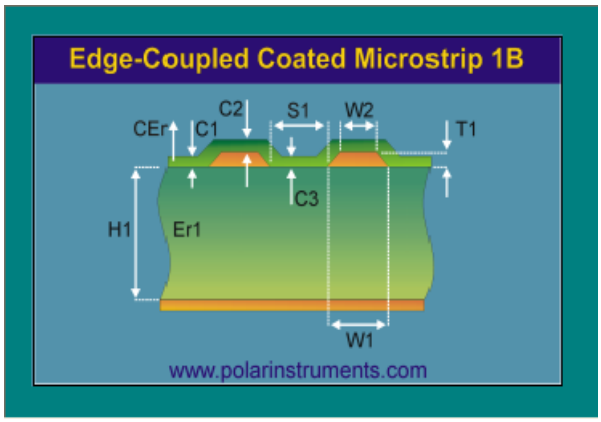
Net name	Routing layer	Reference layer
TXP, TXN, RXN, RXP	1st layer	2nd layer (GND)

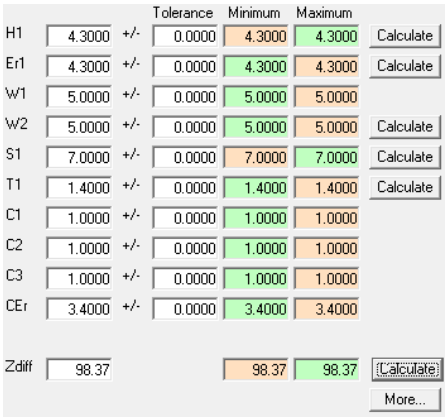
3.2 Net spacing & trace length rule

- SATA Trace : Trace Width / Trace Separation / Pair Separation ＝ 5 / 7 / 15 mil]

  Target differential impedance: 98 Ω







- SATA3.0 trace length should be between 700mil and 1800mil, and trace mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.
- Route all SATA signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Do not route SATA traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

4 USB2.0 layout guide

4.1 Related net name & pairs

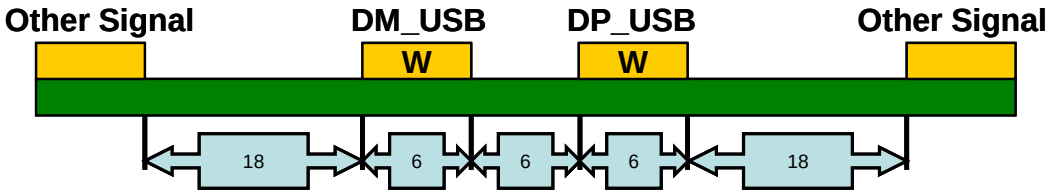
USB2.0 have a differential signal pair，detailed information is as follows:

Net name	Routing layer	Reference layer
DP_USB, DM_USB	1st layer	2nd layer (GND)

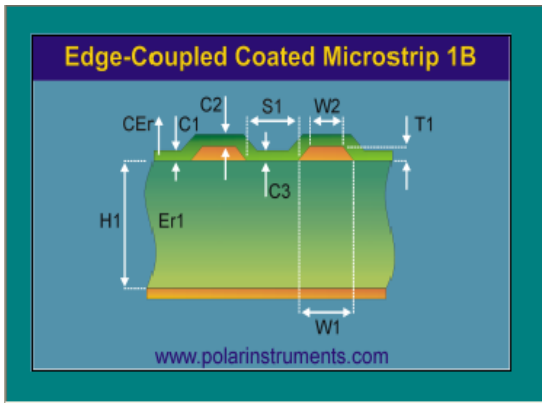
4.2 Net spacing & trace length rule

- USB Trace : Trace width / trace separation / pair separation ＝ 6 / 6 / 18 mil

  Target differential impedance: 89 Ω



Unit: mil



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	4.3000	+/-	0.0000	4.3000	4.3000
Substrate 1 Dielectric	Er1	4.3000	+/-	0.0000	4.3000	4.3000
Lower Trace Width	W1	6.0000	+/-	0.0000	6.0000	6.0000
Upper Trace Width	W2	6.0000	+/-	0.0000	6.0000	6.0000
Trace Separation	S1	6.0000	+/-	0.0000	6.0000	6.0000
Trace Thickness	T1	1.4000	+/-	0.0000	1.4000	1.4000
Coating Above Substrate	C1	1.0000	+/-	0.0000	1.0000	1.0000
Coating Above Trace	C2	1.0000	+/-	0.0000	1.0000	1.0000
Coating Between Traces	C3	1.0000	+/-	0.0000	1.0000	1.0000
Coating Dielectric	CEr	3.4000	+/-	0.0000	3.4000	3.4000
Differential Impedance	Zdiff	88.68			88.68	88.68

- USB2.0 trace length mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.
- Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Do not route high-speed USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

5 Crystal layout guide

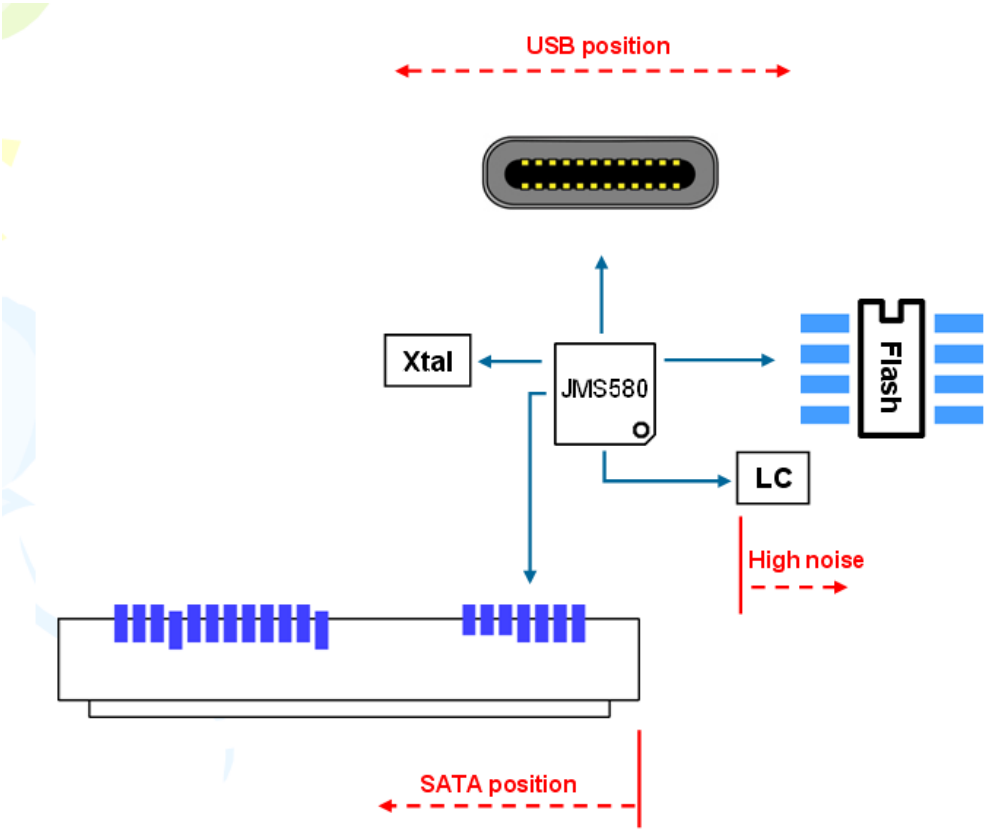
5.1 Related net name & pairs

The Oscillator/Crystal detailed information is as follows:

Net name	Routing layer	Reference layer
XIN, XOUT	1st layer	2nd layer (GND)

5.2 Layout rule

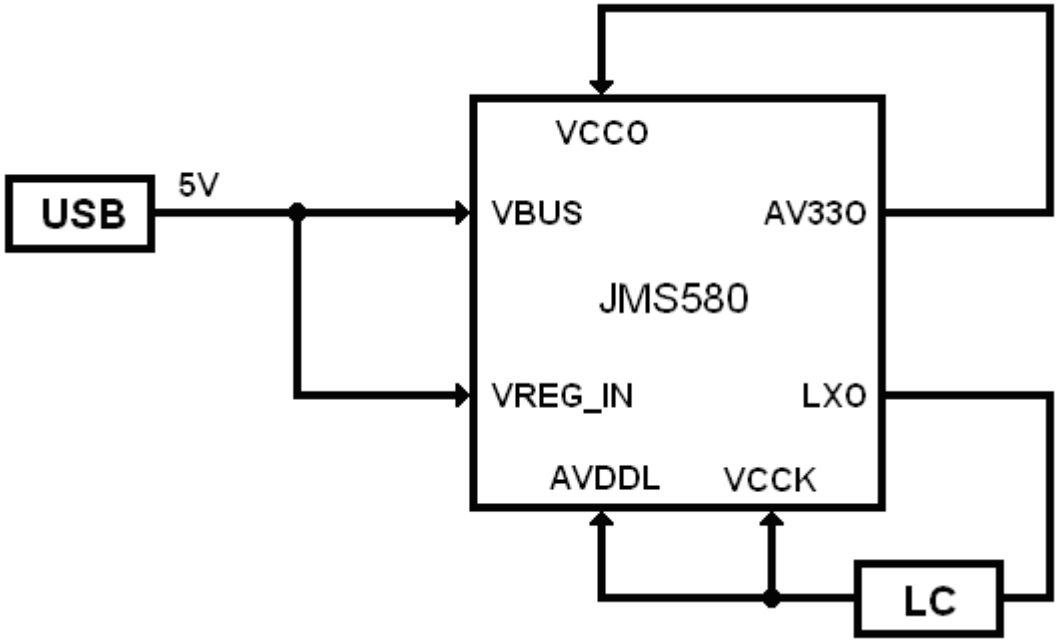
- The crystal unit should then be placed as close as possible to the XIN and XOUT pins to minimize etch lengths.
- Ensure that the ground plane under the IC and its components are of good quality.
- Avoid placing a separate ground under the oscillator and connecting it to the general ground through a single point.
- Avoid long connections to the crystal and to the load capacitor that create a large loop on the PCB.
- Use a short connection between the two crystal load capacitors and route the common connection to the IC ground reference.



6 Power layout guide

6.1 Related net name

Power detailed information is as follows:

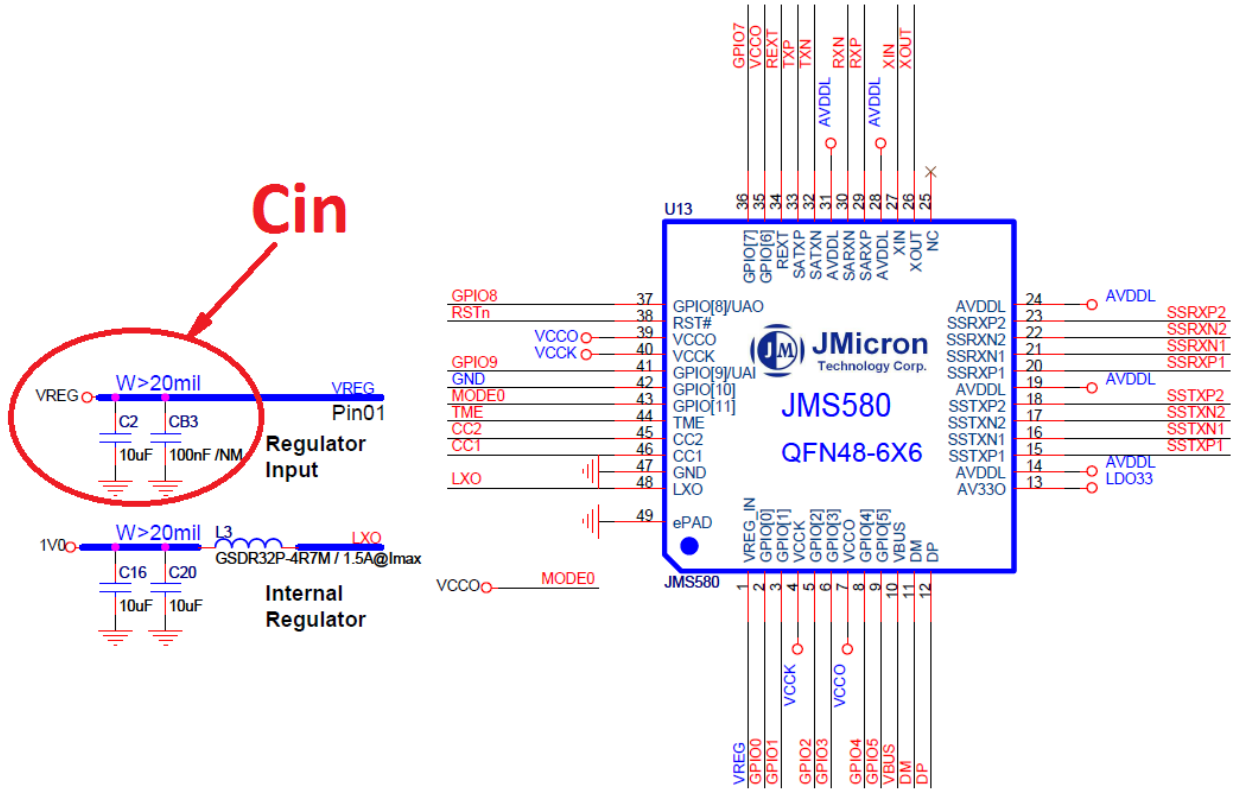


6.2 Layout rule

- The width of 5V ≧ 60 mil (suggest 80mil)
- The width of AV33O , VCCO ≧ 15 mil (suggest 30 mil)
- The width of VREG_IN , LXO , VCCK , AVDDL ≧ 30 mil (suggest 40 mil)

7 Switching regulator LC layout guide

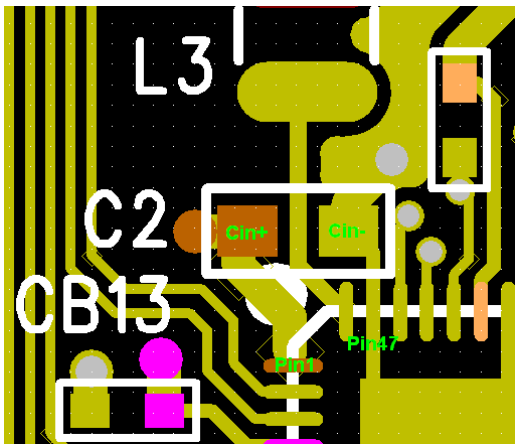
7.1 Related component location



7.2 LC layout rule

- Place the Cin(C2) as close as possible to Pin1 and Pin47.
- C16,C20,L3 Away from the JMS580
- C2, CB3, C16, C20, L3 Away from USB signal and SATA signal.

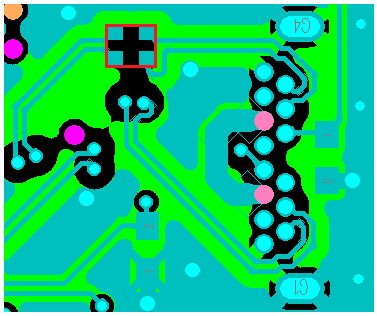
Layout example for Cin:



Note: 1. Cin- as close as possible to Pin47

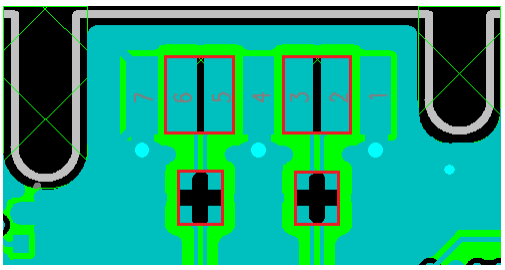
2. Cin+ as close as possible to Pin1

Layout example for USB connector:



Note: Remove area under capacitors

Layout example for SATA connector:



Note: Remove area under capacitors and SATA signals pins