Functional electronic circuits

Laboratory work 2 «Design of data path functional blocks»

1. Develop three types of implementations for device: one-cycle, multi-cycle, pipelined. The device should perform the function according to the variant. The signal interface is presented in Figure 1 and contents such signals as:
   1.1. **x** – 32 bit input value;
   1.2. **start** – signal to start calculation;
   1.3. **rst** – reset signal;
   1.4. **clk** – clock signal;
   1.5. **y** – the 32 bit result value;
   1.6. **rdy** – the ready signal. It is asserted when the device is ready for computation.

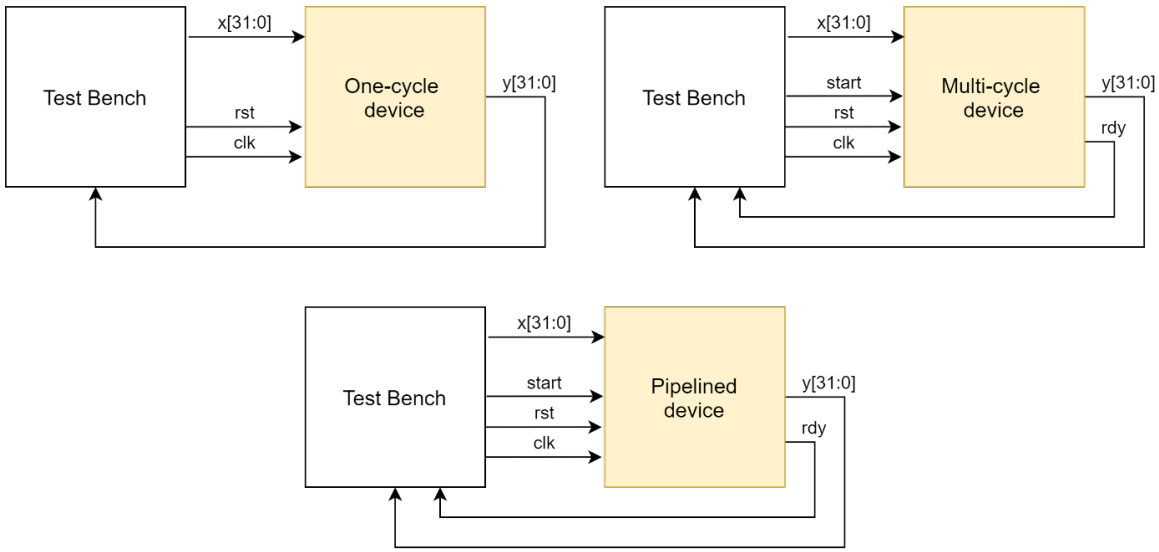

Figure 1 The developing systems

2. Develop a testbench of the device and test the device.
3. Calculate the calculation time of each implementation.
4. Draw a microarchitecture of your device.
5. Put results in the report. The report should consist:
   5.1. Student Name and Student ID
   5.2. The picture with microarchitecture of each implementation
   5.3. The timing diagram with simulation results
   5.4. Code of the testbench and the device.
6. Upload the report by this form: https://forms.yandex.ru/u/64425ea1c09c0201fdb452ec/

Variants

№	Device function	№	Device function	№	Device function
0	$y = x^4 + x$	2	$y = x^3 + x^2$	4	$y = x^4 + x^3$
1	$y = x^2 + x^5$	3	$y = x^5 + x^3$	5	$y = x^2 + x^4$
6	y =	7		8	
9		10		11	