Functional electronic circuits

Laboratory work 1 «Verilog HDL Basics»

1. Develop the device that can read N values (x values) from the external memory and perform the operations according the variant task. The signal interface is presented in Figure 1 and contents such signals as:
   1.1. **x** – 32 bit input value;
   1.2. **rd** – read signal;
   1.3. **start** – signal to start calculation;
   1.4. **rst** – reset signal;
   1.5. **clk** – clock signal;
   1.6. **y** – the 32 bit result value;
   1.7. **rdy** – the ready signal. It is asserted when the device is ready for computation.

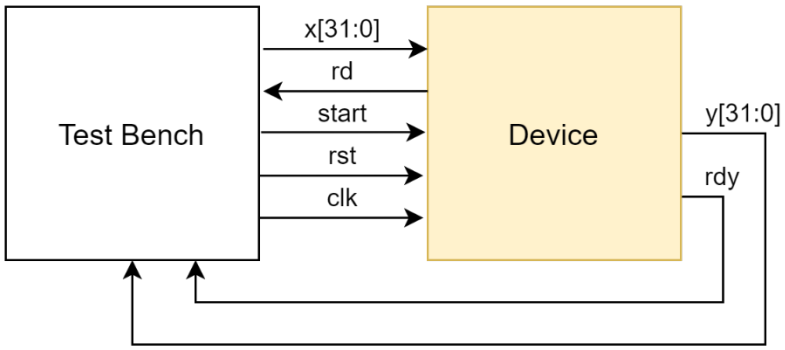

Figure 1. The developing system

2. Draw a microarchitecture of your device.
3. Put results in the report. The report should consist:
   3.1. Student Name and Student ID
   3.2. The picture with microarchitecture
   3.3. The timing diagram with simulation results
   3.4. Code of the testbench and the device.
4. Upload the report by this form: https://forms.yandex.ru/u/642fa91d5056900badef4398/

Variants

№	Device function	N
0	Calculate the sum of elements	5
1	Find the greatest element	7
2	Find the lowest element	6
3	Calculate the sum of elements that greater 2	7
4	Count zeros in input data	5
5	Perform cyclic shift of the value 1 to the right. The input value (x value) should be used as a count of shift operations.	8
6	Perform cyclic shift of the value 1 to the left. The input value (x value) should be used as a count of shift operations.	10