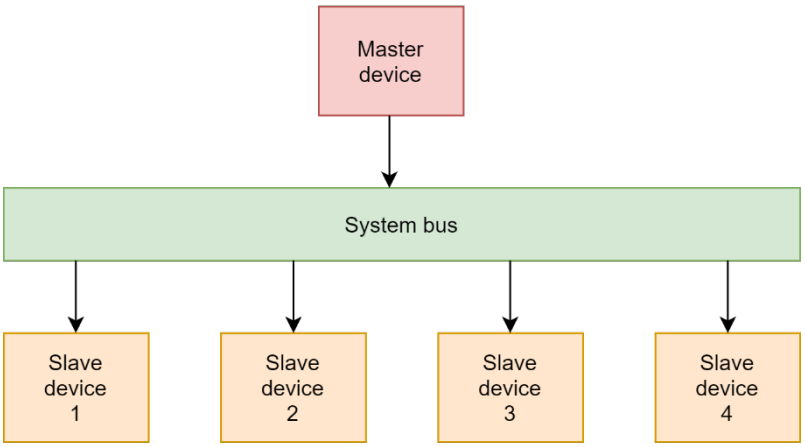
Functional electronic circuits

Laboratory work 4 «System bus design»

1. Develop the system with master device, slave device and interconnection matrix according to the scheme, timing diagram and memory map presented below.



Memory map

Addresses	Device
0x00 - 0x1F	Slave 1
0x20 - 0x2F	Slave 2
0x30 - 0x3F	Slave 3
0x40 - 0x4F	Slave 4
0x50 - ...	Reserved

Figure 1 – Scheme of the system and memory map

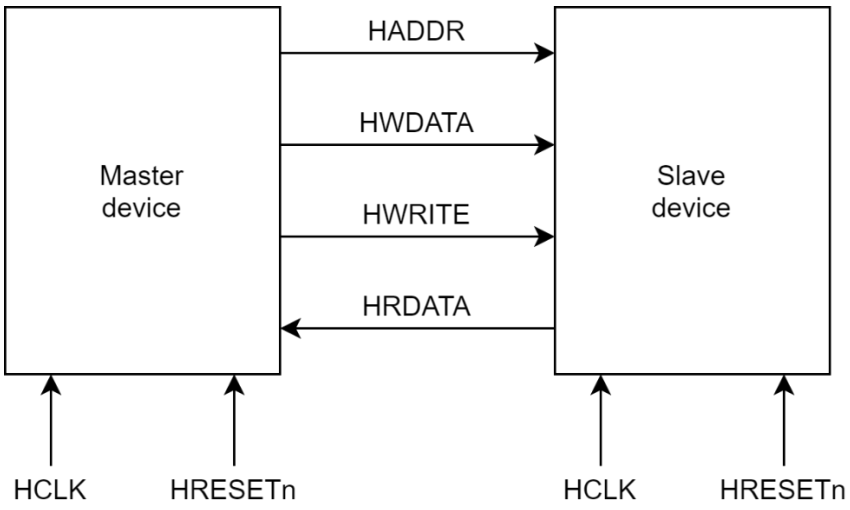


Figure 2 – The interface between master and slave device

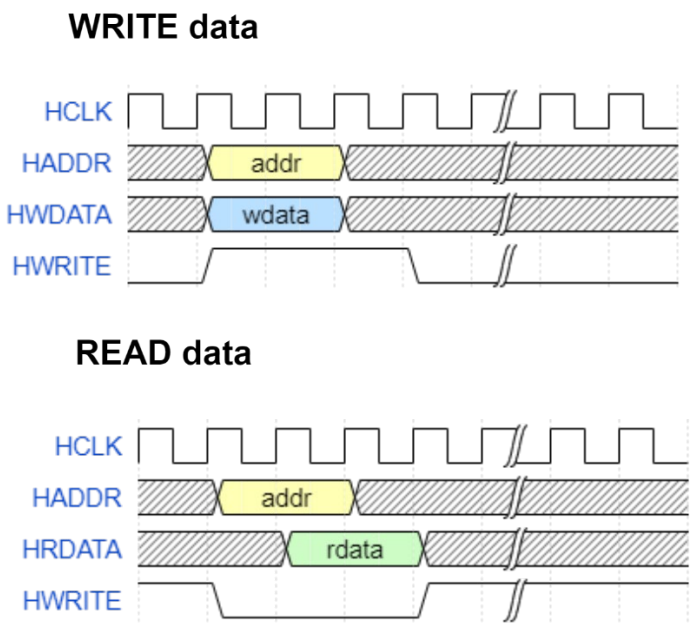


Figure 3 – Timing diagrams of write and read operations

2. Develop a testbench for the system and test the system.
3. Put results in the report. The report should consist:
   3.1. Student Name and Student ID
   3.2. The picture of the system
   3.3. The timing diagram with simulation results
   3.4. Code of the testbench and the device.
4. Upload the report by this form: https://forms.yandex.ru/u/645e08b3c769f175ad7c6e64/