A 56-ps Multi-phase Clock Time-to-Digital Convertor based on Artix-7 FPGA

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***Abstract*—The time-to-digital converter(TDC) is an equipment which aims to measure the accurate time of the edges of the input signal. Our work present an I/O Tile based multi-phase clock time-to-digital TDC, which is implemented in Field-Programmable-Gate-Array(FPGA). A hit signal is sampled by 8 equidistant phase-shifted clocks in the I/O Tile. A differential I/O standard input signal connecting to the I/O Tile is buffered by an input buffer and split into two complementary outputs before feeding to two adjacent ISERDESes. The ISERDESes are configured as the oversample mode, which is used to capture 2 phase DDR data. One ISERDES is driven by 45° and 135° clocks, with the other ISERDES driven by 90° and 180° clocks. Four more clocks are produced by locally inverting logic in the two ISERDESes. An internal PLL is used to generate the clocks. This architecture makes the transmission line more stable and increases the frequency of the sampling clock.**

To evaluate the TDC's performance, we built a verification system with Xilinx Artix-7 XC7A100T-1 FPGA, which is integrated with 2 TDCs and a readout unit. Tests have been conducted on the performance of the I/O Tile based TDC. Results indicated that the integral nonlinearity is lower than 1 LSB, and the differential nonlinearity is lower than 0.32 LSB. The measurement resolution of 56ps (RMS) is archived.

I. Introduction

A. Background

High-resolution time-to-digital converter (TDC) has been applied in a number of measurement systems, such as nuclear science detectors, medical imaging equipments, laser rangefinders and aerospace systems [1]–[4]. Modern TDC systems require both good resolution(i.e. below 1ns) and high integration level(i.e., integrating more TDC into single ASIC or FPGA). In the Large Area Water Cherenkov Array (LAWCA) project which is proposed to be built in China, the readout system-on-chip (SoC) requires the time measurement resolution at least 500ps, and integrates 36 TDC channels in single FPGA [5], a high resolution TDC design should be integrates. In addition to multiple-channel TDC, the SoC also consists of processor, memory controller, ethernet controller, and digital signal process units. Based on our design, the TDC provides high resolution and low resources usage, which is critical for the whole system.

This work was supported by the Knowledge Innovation Program of the Chinese Academy of Sciences under Grant KJCX2-YW-N27 and the National Natural Science Foundations of China under Grant 11175174, 11079003.

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B. A Brief Introduction to TDC

There are two ways to implement TDC in FPGA, which based on the same principle. Briefly, a single flip-flop is used to sample the external hit signal, and a counter to record the accurate time. In this case, the width of the least significant bit (LSB) of the counter equals the sampling clock period and limited to the maximum frequency of the system.

Two improvement strategies have been used commonly in real time convertor. Instead of single flip-flop, a modified sampling unit is added and aims for reducing the LSB to less than the sampling clock period. Numerous of flip-flops which is driven by the same clock to sample the hit signal have been applied to the taped delay chain architecture which is shown as Fig.1(a). The arriving time of the hit signals to every flip-flops are equidifferent. By analyzing the Flip-flop's output (BIN code), the accurate time of the hit signal can be calculated. This architecture provides the best RMS error which is only 10ps, but hard to achieve due to the delay taps being implemented by carry logic inside FPGA(slice carry-chain). The delay value is uncontrollable with the temperature or voltage changes. To reduce the violation of the delay taps affected by the voltage and temperature, a complex calibration mechanism is required.

The other strategy is the multi-phase clock architecture which is shown in Fig.1(b). The same input signal is sampled with flip-flops clocked by a set of equidistant phase-shift clocks. The clocks are generated by a Phase-locked loops (PLL) inside FPGA, the skewing between clocks are stable with temperature and voltage changes. The same hit signal fans out to each flip-flop, sampled by different clock. This architecture requires that the routing delay to the flip-flops are equivalent, which is also hard to archive. In summary, traditional multi-phase clock TDC does not show decent property.

C. Related Works

A couple of groups have designed TDC based on FPGA technology. J. Wu from Fermi national accelerator laboratory presented an taped delay chain TDC [1],with the RMS around 10ps, which achieves the best performance of TDC based on

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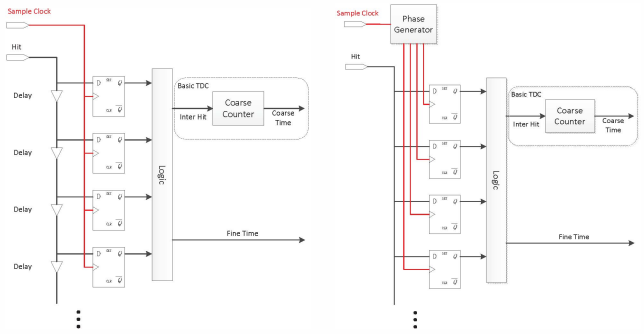


(a) Architecture of Taped Delay Chain TDC (b) Architecture of Multi-Phase TDC

Fig. 1: Two Improvement Strategies of Real Time TDC

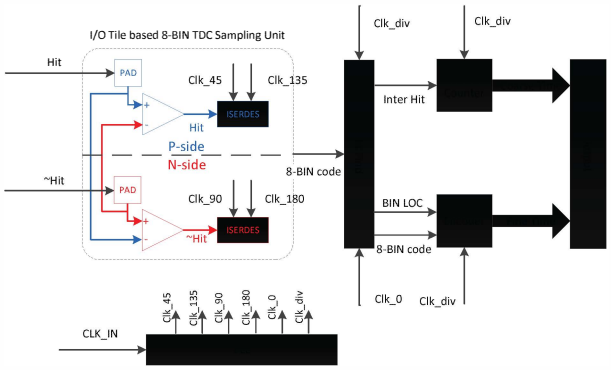


Fig. 2: Structure of TDC

FPGA, while the RMS result may changes under varies voltage and temperature conditions. Furthermore, the architecture occupies 1618 flip-flops, and most of the flip-flops must be adjacent and ordered, which is difficult to be integrated in a SoC.

According to Z. Yin's work, a multi-phase clock TDC [6] is produced. The RMS is around 363 ps, but the architecture only occupies 103 flip-flops, which is easy to integrate multiple channels.

Mark D. Fries from General Electrical Medical Systems also produces a multi-phase clock TDC [7]. The RMS is around 455 ps.

D. Goals

In our work, we describe a new architecture of multi-phase clock TDC, which shows better RMS compared with the traditional multi-phase clock sampling architecture, and provides higher level of integration than taped delay chain architecture.

II. TDC Architecture

In contrast with traditional multi-phase clock TDC, our architecture integrates the sampling unit in an I/O Tile pin pair(including positive and negative pins), instead of implementing in general resources in FPGA. The sampling unit uses 8 equidistant phase-shifted clocks to collect the input hit signal, and generate the BIN code.

A. I/O Tile based 8-BIN TDC Structure

The TDC consists of sampling unit, data synchronization unit, measurement unit, and clock generation unit, which is shown as Fig.2. The sampling unit is based on multi-phase clock structure, using 8 equidistant phase-shifted clocks to sample the hit signal. The data synchronization unit synchronizes the BIN code to a slow clock region. The measurement unit counts the hit signal arrive time. The clock generation unit provides the clocks which drive the TDC.

The sampling unit is the core of the TDC, the I/O Tile based sampling unit can improve the performance significantly. This structure utilizes dedicated logic in the Xilinx I/O Tile, which consists of a differential input buffer with complementary outputs (IBUFDS_DIFF_OUT) and two dedicated serial-to-parallel converters (ISERDESes). The structure is shown in the left part of Fig.2. The IBUFDS_DIFF_OUT connects two pins from the device pads showing the P and N channel pins in a differential pair, and two complementary outputs(P-side and N-side) into FPGA [8]. An ISERDES from P-side connects the output of P-side, while a N-side's ISERDES connects N-side's output.

There exist two clock domains in the TDC structure, the sampling clock domain and slow clock domain. The clock frequency in sampling clock domain is 8 times faster than the clock frequency in slow clock domain. The sampling unit works at the sampling clock domain, while the coarse counter and encoder work at the slow clock domain. The Data Synchronization unit crosses the two clock domains, synchronizes the BIN code from sampling clock domain to slow clock domain.

All the clocks in the TDC should be generated by single Phase-locked loops (PLL), so they shares a same routing delay from PLL to global clock buffer. Tab.I summaries the parameters of the clocks.

TABLE I: Parameters of PLL Generating Clocks

Name	Frequency Factor	Phase Shift Factor
Clk_0	8x	0
Clk_45	8x	45
Clk_90	8x	90
Clk_135	8x	135
Clk_180	8x	180
Clk_div	1x	0

B. ISERDES Configuration

The ISERDES is a dedicated serial-to-parallel converter with specific clocking and logic features designed to facilitate the implementation of high-speed source-synchronous applications. The ISERDES avoids the additional timing complexities encountered when designing deserializers in the FPGA fabric [8]. The ISERDES is configured as oversample mode, which is used to capture two phases DDR data. In this mode, the ISERDES has two clock input port CLK and OCLK with 90° phase difference between them. It captures input data on both the rising and falling edge of the two clocks [8]. So a hit signal is sampled by 4 equidistant phase-shifted clocks in one

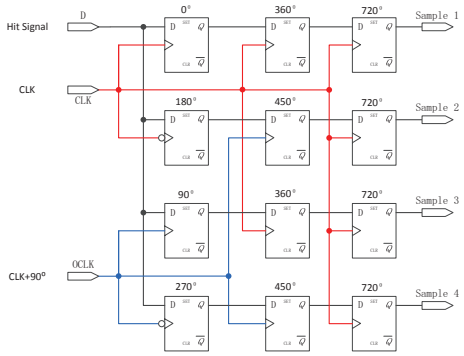


Fig. 3: The Sampling Strategy based on SelectIO

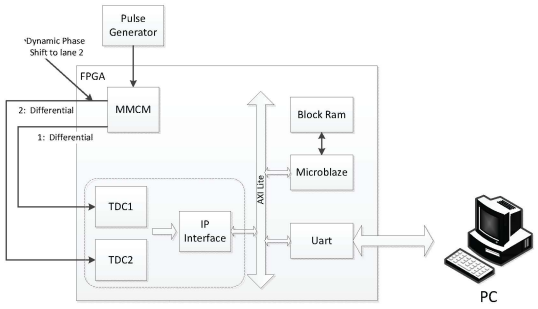


Fig. 4: Schematic of the Verification System base on single FPGA

ISERDES. As shown in Fig.3, how an ISERDES samples hit signals and synchronizes the data to CLK is illustrated.

The two ISERDESes can be considered as a 8 equidistant phase-shifted clocks TDC, with driving the first one with $45°$, $135°$ clocks and the second on with $90°$, $180°$ clocks.

The outputs of the two ISERDESes are BIN code. Each one bit in the BIN code has a width of 1 in 8th of sampling clock period, and the frequency of sampling clocks are 8 times higher than the slow clock. So the resolution the BIN code is 64 times better than the coarse time.

III. Results

A. Performance Parameters of TDCs

There are 3 parameters which evaluates the performance of TDCs: differential nonlinearity (DNL), integral nonlinearity (INL), and root-mean-square (RMS).

The DNL indicates the maximum deviation between measured BIN width and theoretical BIN width (LSB), which is determined by statistical code-density test. The timestamps of a large number of random hits is measured, and the number of hits falling in each time bin is filled in a histogram. As the theoretical number of events in every bin is knows, the normalized DNL can be calculated.

The INL describes the maximum deviation between the ideal time and the measured time of a TDC. The transfer function of a TDC should ideally be a line, so the INL is the maximum distance between the ideal line selected and the actual transfer function. The actual transfer function is also determined by statistical code-density test.

The RMS error represents the sample standard deviation of the differences between predicted values and observed values. The RMS error is calculated by cable-delay test [9]–[12]. The deviation between two TDCs with related hits of a large number is measured, and fill in a histogram, while the RMS error can be calculated.

B. Verification System

For evaluating the TDC's performance, we should implement two independent TDC channels which triggered by two related signal whose phase relationship are adjustable. Traditionally, a digital delay generator is used to adjust those two signals. While FPGA as its reconfigurability, can integrate a powerful hit signal generate unit reaches the satisfied precision as the digital delay generator. The whole verification system can be implemented in single FPGA.

Fig.4 is the Schematic of the system based on single FPGA. The two TDCs are instantiated as a peripheral of the embedded system, the results of the TDCs are sent to PC via the UART interface.

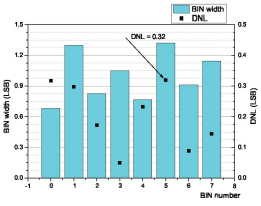
A MMCM is used to generate phase related periodic signals as the hit signals of TDCs. A clock from pulse generator feds to the MMCM. Two clock lanes with same frequency and same initial phase are generated by the MMCM, while lane 2 enables dynamic phase shift mode. The loopback transmission line are connected outside FPGA from the MMCM to the TDC, since the 2-ISERDES based sampling units need hit signals coming from outside FPGA.

C. Test Results

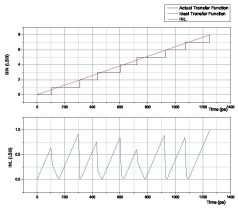
The verification system is implemented in a Xilinx Artix-7 XC7A100T-1 FPGA. The sampling clock of TDCs is $800MHz$, while the slow clock is 1/8th of the sampling clock equals $100MHz$. The period of hit signals are $100.1ns$. The VCO of MMCM is $1.28GHz$, which means the phase difference of the two lanes varies in steps of 1/56th of the VCO period equals 14ps approximately.

Fig.5(a) shows the result for BIN width and DNL of TDC. The DNL is 0.32 LSB. Fig.5(b) shows the result for Transfer Function and INL of TDC. In our architecture, the INL is 1 LSB.

Fig.6(a) is a typical RMS measurement result. The abscissa represents the time interval of two channels, the ordinate represents the probability density for each time interval. In

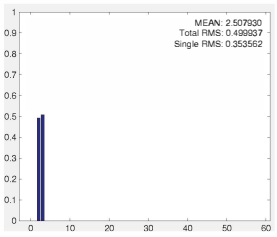


(a) BIN width and DNL

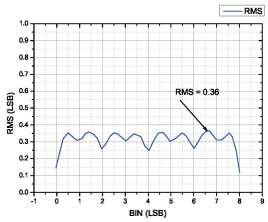


(b) Transfer Function and INL

Fig. 5: DNL and INL



(a) A typical RMS Measurement



(b) RMS Results

Fig. 6: RMS Measurement and Results

this figure, the mean value is 2.51 LSB, the total RMS is equal to 0.50 LSB. It should be noted that the cable-delay test consists of two independent TDC, the total RMS error includes two coincident ingredients for each TDC. The RMS of single TDC can be calculated by the equation:

$$RMS_{Total}{}^2 = 2 \times RMS_{Single}{}^2 \quad (1)$$

So the single RMS is equal to 0.35 LSB.

Fig.6(b) shows the RMS for single TDC around 8 BIN delay. In the ideal case, the minima would be zero and the maxima were about 0.35 LSB [13]. In our architecture, the RMS error is 0.36 LSB.

D. 100-Hour Long Term Test

A 100-hour term test of TDC has been done to verify whether the TDC works stable at this frequency. Fig.7 shows the MEAN value and RMS value measured in the 100-hour term TDC Test. The RMS value almost remains a constant value in 100 hours, while the swing of the MEAN value is better than 0.02 LSB.

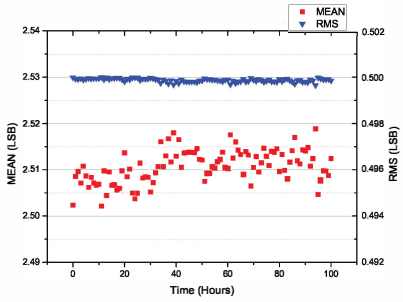


Fig. 7: 100-Hour term TDC Measurement Result

IV. Discussions

The SelectIO based multi-phase clock Sampling TDC has been studied. Parameters of several types of TDC schemes are compared in Tab.II.

The SeletcIO based multi-phase clock TDC has better performance in BIN width, DNL, INL, and RMS error than the best results of the traditional Multi-Phase Clock TDC. In contrast to the taped delay chain TDC, our TDC has lower resources occupation, and its performance doesn't change with temperature and voltage.

TABLE II: Parameters of Several TDC Architectures

	Taped Delay Chain [1]	**General FFs based Multi-Phase Clock [6]**	**SelectIO Based Multi-Phase Clock**
BIN width	30ps	758ps	156ps
RMS	10ps	363ps	56ps
LUT Usage	1621	104	109
Flip-Flop Usage	1621	103	238

V. Conclusion

In summary, we proposed a 2-ISERDES based TDC architecture. The sampling unit of the TDC consists of 2 ISERDESes, in which dedicate ISERDESes are used instead of standard flip-flops. This architecture reduces the performance deterioration caused by the difference between the routing delays from IO to the sampling unit, and a 8 phase-shifted sampling clocks can be obtained. In contrast to traditional TDCs, this architecture requires less resource than the taped delay chain TDCs, while archiving better performance than the general flip-flops based multi-phase clock sampling TDC.To evaluate the performance, a verification system was built. The results indicate that the the integral nonlinearity is better than 1 LSB, the differential nonlinearity is better than 0.32 LSB, the RMS is around 0.36 LSB(56 ps).A 100-hour long term test has been conducted to verify the reliability of the system,demonstrating that the TDC works reliably in 100 hours.

References

[1] Wu, Jinyuan, and Zonghan Shi. "The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay." Nuclear Science Symposium Conference Record, 2008. NSS'08. IEEE. IEEE, 2008.

[2] Wu, Jinyuan, Sten Hansen, and Zonghan Shi. "ADC and TDC implemented using FPGA." Nuclear Science Symposium Conference Record, 2007. NSS'07. IEEE. Vol. 1. IEEE, 2007.

[3] Qin, Xi, et al. "Development of a High Resolution TDC for Implementation in Flash-Based and Anti-Fuse FPGAs for Aerospace Application." Nuclear Science, IEEE Transactions on 60.5 (2013): 3550-3556.

[4] Shen, Qi, et al. "An FPGA-Based TDC for Free Space Quantum Key Distribution." (2013): 1-8.

[5] SHANG L F. *Research of Clock Distribution and Data Transmission in LAWCA Readout Electronics*. Dissertation for doctors degree. University of Science and Technology of China, 2013.

[6] YIN Z J C, LIU S B, HAO X J, et al. "A High-Resolution Time-to-Digital Converter Based on Multi-Phase Clock Implement in Field-Programmable-Gate-Array", IEEE NPSS Real Time Conference (RT), 2012

[7] Fries, Mark D., and John J. Williams. "High-precision TDC in an FPGA using a 192 MHz quadrature clock." Nuclear Science Symposium Conference Record, 2002 IEEE. Vol. 1. IEEE, 2002.

[8] Xilinx. "7 Series FPGAs SelectIO Resources User Guide." Oct 31, 2012.

[9] Christiansen J, CERN Digital Microelectronics Group, 2004.

[10] Song, Jian, Qi An, and Shubin Liu. "A high-resolution time-to-digital converter implemented in field-programmable-gate-arrays." Nuclear Science, IEEE Transactions on 53.1 (2006): 236-241.

[11] Mota, M., et al. "A flexible multi-channel high-resolution time-to-digital converter ASIC." Nuclear Science Symposium Conference Record, 2000 IEEE. Vol. 2. IEEE, 2000.

[12] Szplet, Ryszard, Jozef Kalisz, and Rafal Szymanowski. "Interpolating time counter with 100 ps resolution on a single FPGA device." Instrumentation and Measurement, IEEE Transactions on 49.4 (2000): 879-883.

[13] F. Baronti et al. "On the differential nonlinearity of time-to-digital converters based on delay-locked-loop delay lines", IEEE Trans. Nucl. Sci. 48 (2001) 2424.