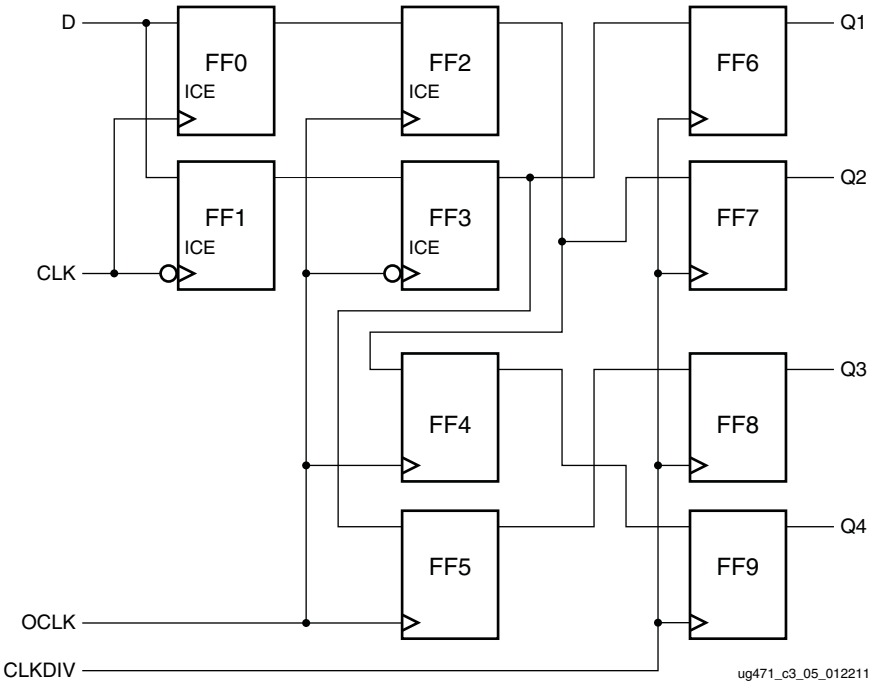

Figure 3-5: **Internal Connections of ISERDESE2 When in MEMORY Mode**

NUM_CE Attribute

The NUM_CE attribute defines the number of clock enables (CE1 and CE2) used. The possible values are 1 and 2 (default = 2).

SERDES_MODE Attribute

The SERDES_MODE attribute defines whether the ISERDESE2 module is a master or slave when using width expansion. The possible values are MASTER and SLAVE. The default value is MASTER. See ISERDESE2 Width Expansion.

ISERDESE2 Clocking Methods

NETWORKING Interface Type

The phase relationship of CLK and CLKDIV is important in the serial-to-parallel conversion process. CLK and CLKDIV are (ideally) phase-aligned within a tolerance. There are several clocking arrangements within the FPGA to help the design meet the phase relationship requirements of CLK and CLKDIV.

The CLK and CLKDIV inputs must be nominally phase-aligned. For example, if CLK and CLKDIV in Figure 3-6 were inverted by the designer at the ISERDESE2 inputs, then although the clocking arrangement is an allowed BUFIO/BUFR configuration, the clocks would still be out of phase. This also prohibits using DYNCLKINVSEL and DYNCLKDIVINVSEL.

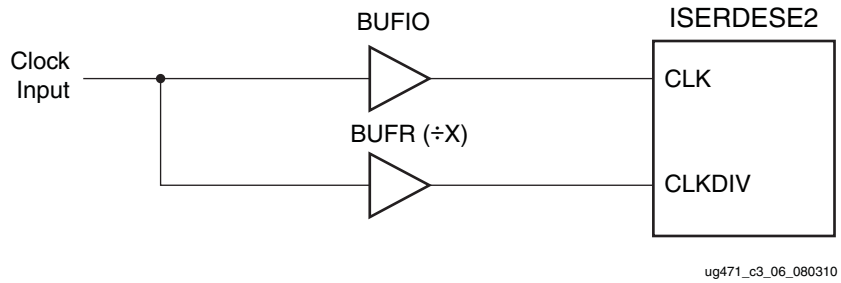

Figure 3-6: **Clocking Arrangement Using BUFIO and BUFR**

The only valid clocking arrangements for the ISERDESE2 block using the networking interface type are:

- CLK driven by BUFIO, CLKDIV driven by BUFR
- CLK driven by MMCM or PLL, CLKDIV driven by CLKOUT[0:6] of same MMCM or PLL

When using a MMCM to drive the CLK and CLKDIV of the ISERDESE2, the buffer types suppling the ISERDESE2 can not be mixed. For example, if CLK is driven by a BUFG, then CLKDIV must be driven by a BUFG as well. Alternatively, the MMCM can drive the ISERDESE2 though a BUFIO and BUFR.

MEMORY Interface Type

The only valid clocking arrangements for the ISERDESE2 block using the memory interface type are:

- CLK driven by BUFIO, OCLK driven by BUFIO, and CLKDIV driven by BUFR
- CLK driven by MMCM or PLL, OCLK driven by MMCM or PLL, and CLKDIV driven by CLKOUT[0:6] of same MMCM or PLL
- CLK driven by BUFG, OCLK driven by a BUFG, CLKDIV driven by a different BUFG

The OCLK and CLKDIV inputs must be nominally phase-aligned. No phase relationship between CLK and OCLK is expected. Calibration must be performed for reliable data transfer from CLK to OCLK domain. High-Speed Clock for Strobe-Based Memory Interfaces and Oversampling Mode - OCLK gives further information about transferring data between CLK and OCLK.

MEMORY_QDR Interface Type

The MEMORY_QDR mode has a complex clocking structure as a result of the QDR memory requirements. This INTERFACE_TYPE attribute setting is only supported when using the MIG tool.

OVERSAMPLE Interface Type

The OVERSAMPLE mode is used to capture two phases DDR data. Figure 3-7 shows a more detailed logical representation of the ISERDESE2 and how data is captured on both the rising and falling edge of CLK and OCLK. As shown in Figure 3-7, there must be a 90°offset phase relationship between CLK and OCLK as the data is captured on both CLK and OCLK but is clocked out of the ISERDESE2 on the CLK domain. CLKDIV is not used in this mode. The only valid clocking arrangements for the OVERSAMPLE interface type are:

• CLK and CLKB are driven by a BUFIO. OCLK and OCLKB are driven by a BUFIO that is phase shifted by 90°. The two BUFIOs are driven from a single MMCM.

• CLK and CLKB are driven by a BUFG. OCLK and OCLKB are driven by a BUFG that is phase shifted by 90°. The BUFGs are driven from a single MMCM. In either case, the effective clocking is:

- CLK: 0°
- OCLK: 90°
- CLKB: 180°
- OCLKB: 270°

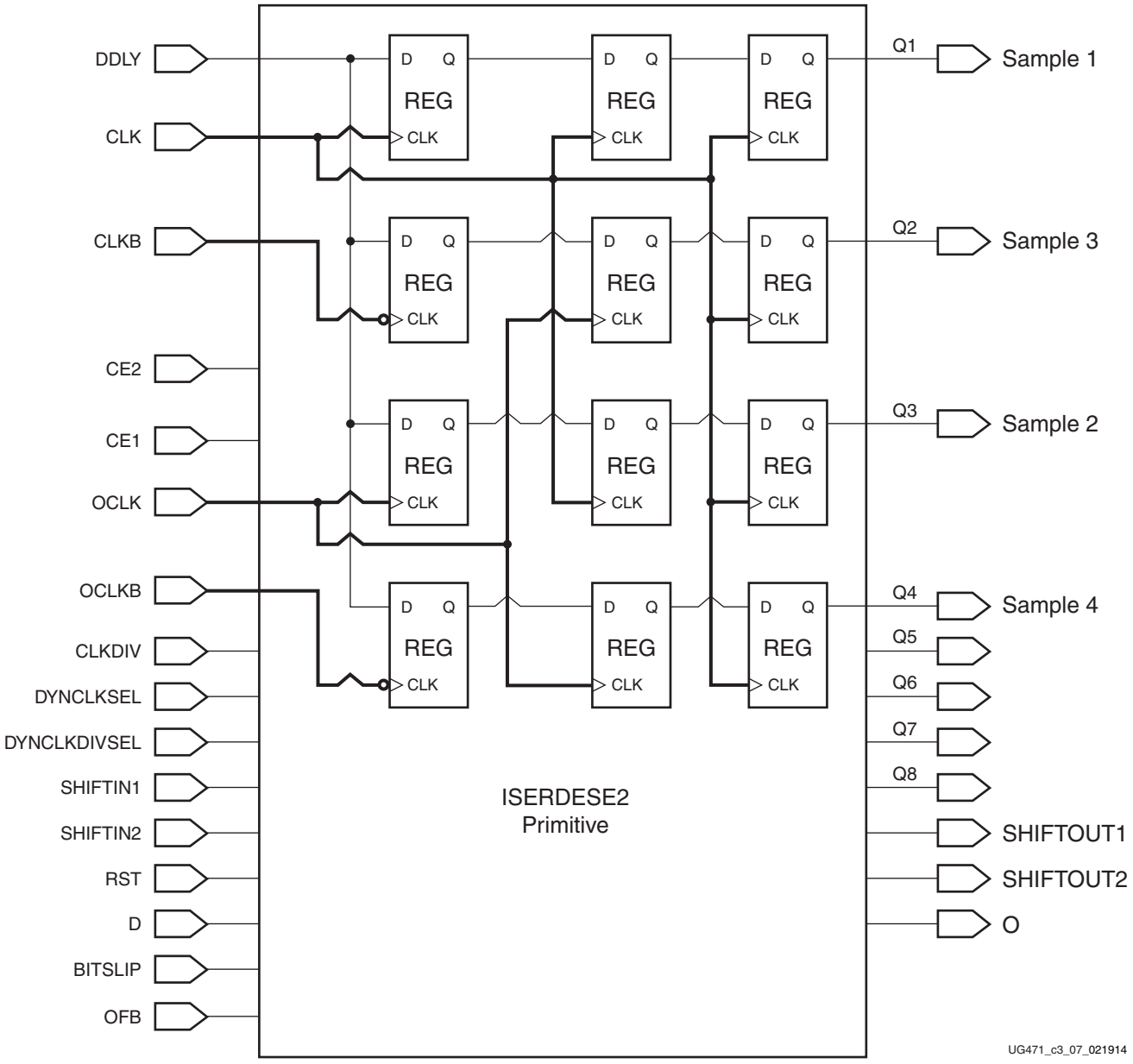

Figure 3-7: **Logical View of ISERDESE2 Primitive in Oversample Mode**