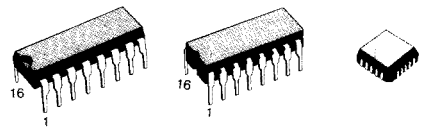
SGS-THOMSON MICROELECTRONICS

M54HC595
M74HC595

8-BIT SHIFT REGISTER WITH OUTPUT LATCHES (3-STATE)

PRELIMINARY DATA

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS FOR QA to QH
  10 LSTTL LOADS FOR QH'
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6mA MIN. FOR QA to QH
  4mA Min. FOR QH'
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS595

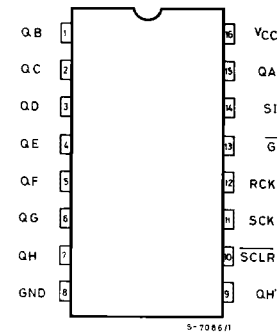


B1N Plastic Package | **F1** Ceramic Package | **C1** Chip Carrier

ORDERING NUMBERS:

M54HC595 F1 | M74HC595 F1
M74HC595 B1N | M74HC595 C1

PIN CONNECTIONS (top view)



NC = No Internal Connection

DESCRIPTION

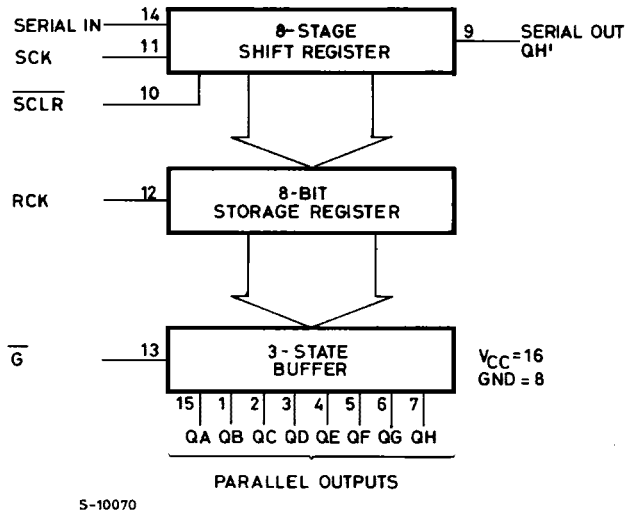
The M54/74HC595 is a high speed CMOS 8-BIT SHIFT REGISTERS/OUTPUT LATCHES (3-STATE) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register.
The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TRUTH TABLE

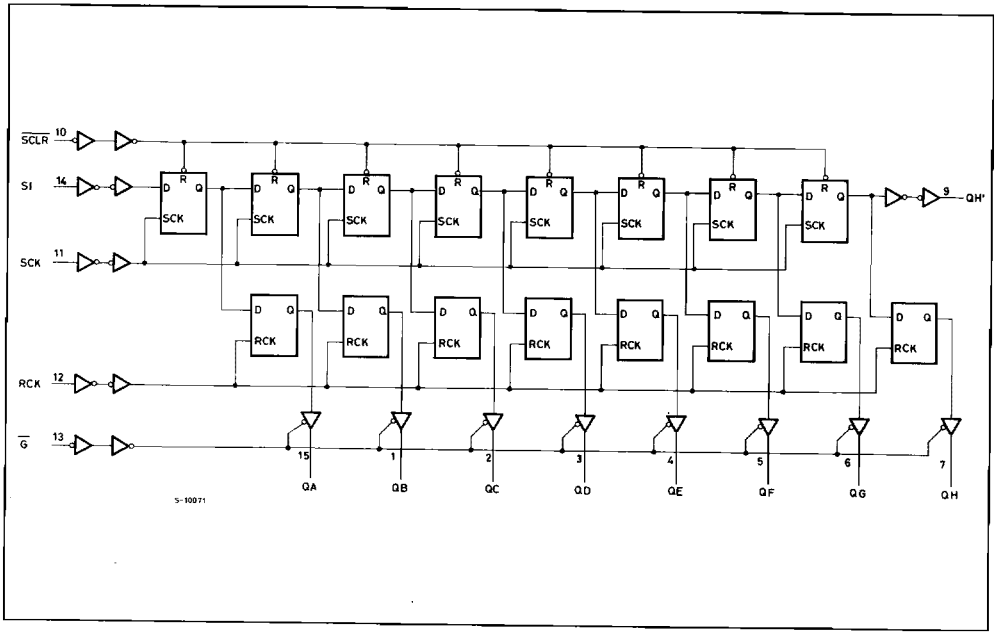
INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA THRU QH OUTPUTS DISABLE
X	X	X	X	L	QA THRU QH OUTPUTS ENABLE
X	X	L	X	X	SHIFT REGISTER IS CLEARED
L	↑	H	X	X	FIRST STAGE OF S.R. BECOMES "L". OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
H	↑	H	X	X	FIRST STAGE OF S.R. BECMOSE "H". OTHER STAGE STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
X	↓	H	X	X	STATE OF S.R. IS NOT CHANGED
X	X	X	↑	X	S.R. DATA IS STORED INTO SOTRAGE REGISTER
X	X	X	↓	X	STORAGE REGISTER STATE IS NOT CHANGED

X: DON'T CARE

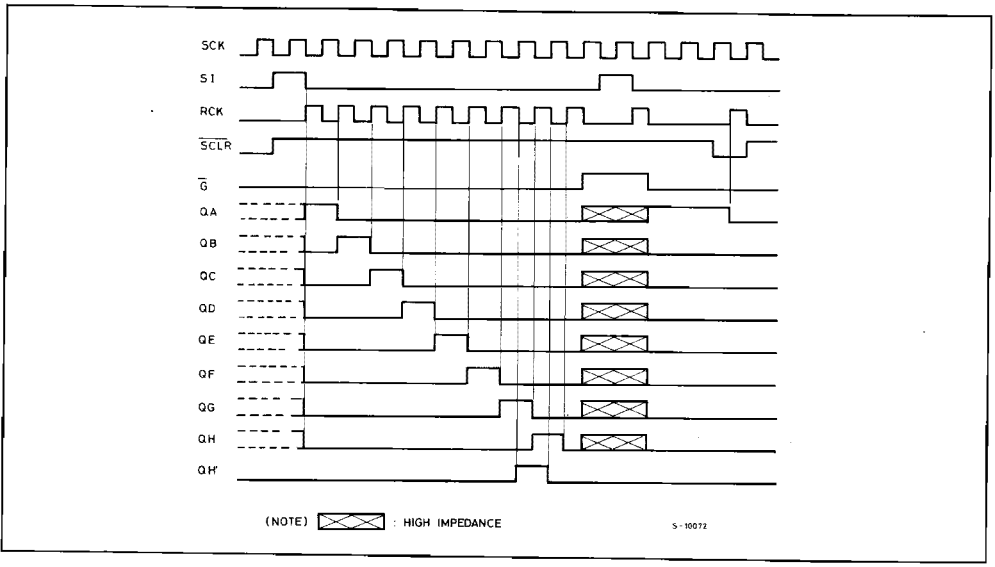
BLOCK DIAGRAM



LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current Per Pin QA-QH	± 35	mA
I_O	DC Output Current Per Pin QH'	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C
T_L	Lead Temperature 10 sec	300	°C

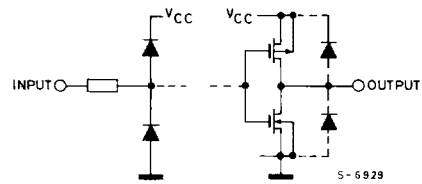
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage QA-QH	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage QA-QH	2.0	V_{IN}	I_{OH}	—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
V_{OH}	High Level Output Voltage QH'	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage QH'	2.0	V_{IN}	I_{OH}	—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-State Output Off state Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±0.5	—	±10	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (QA-QH) PARALLEL	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{TLH} t_{THL}	Output Transition Time (QH') SERIAL	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (SCK-QH')	2.0		—	80	160	—	200	—	240	ns
		4.5		—	20	32	—	40	—	40	
		6.0		—	17	27	—	34	—	41	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK-QH)	2.0		—	88	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
t_{PHL}	Propagation Delay Time ($\overline{SCLR}$-QH')	2.0		—	88	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
f_{MAX}	Maximum Clock Frequency	2.0		6	12	—	5	—	4	—	MHz
		4.5		30	50	—	25	—	20	—	
		6.0		35	59	—	28	—	24	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (SCK, RCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{SCLR}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time (SI-SCK)	2.0		—	20	50	—	65	—	75	ns
		4.5		—	5	10	—	13	—	15	
		6.0		—	4	9	—	11	—	13	
t_s	Minimum Set-up Time (SCK-RCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time ($\overline{SCLR}$-RCK)	2.0		—	44	100	—	125	—	150	ns
		4.5		—	11	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Clear Removal Time	2.0		—	10	50	—	65	—	75	ns
		4.5		—	2	10	—	13	—	15	
		6.0		—	2	9	—	11	—	13	

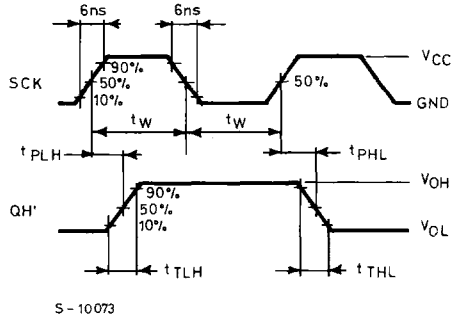
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0 4.5 6.0	$R_L = 1k\Omega$	— — —	68 17 14	135 27 23	— — —	170 34 29	— — —	205 41 35	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0 4.5 6.0	$R_L = 1k\Omega$	— — —	64 21 18	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	254	—	—	—	—	—	pF

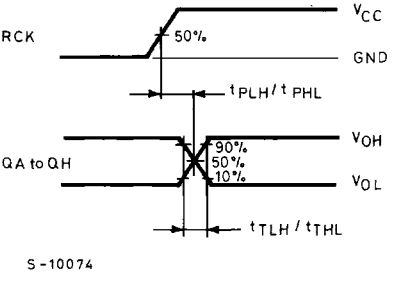
Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average opeating current is: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

WAVEFORM 1

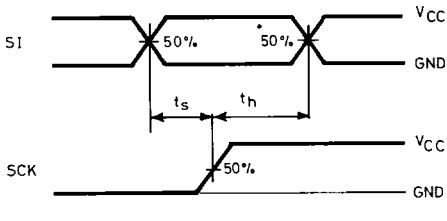


WAVEFORM 2



SWITCHING CHARACTERISTICS TEST WAVEFORM

WAVEFORM 3



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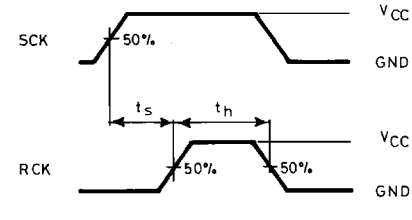
WAVEFORM 4



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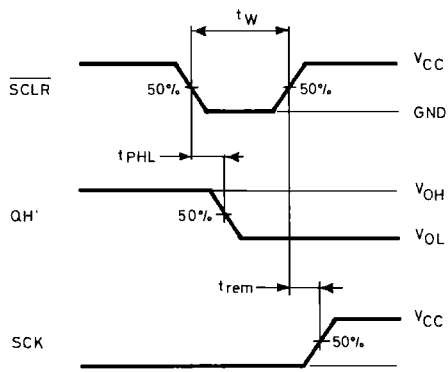
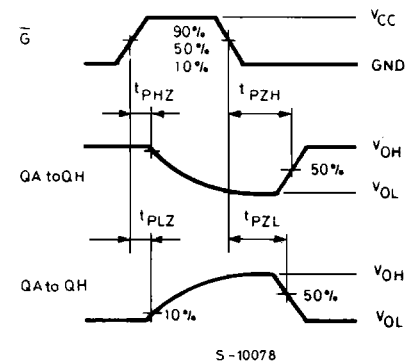
WAVEFORM 5



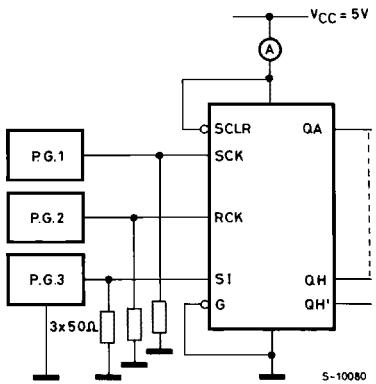
S-10077

WAVEFORM 6



S-10078

TEST CIRCUIT I_{CC} (Opr.)



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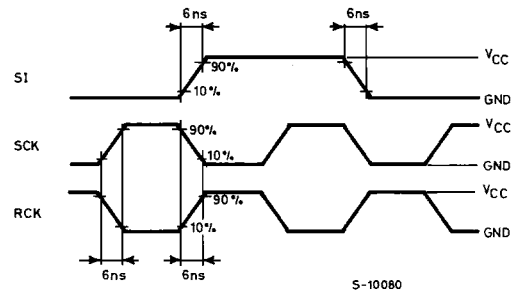
INPUT WAVEFORM



S-10080