MP2384C
24V, 4A, Low I$_Q$, Synchronous Buck Converter with Forced Continuous Conduction Mode (CCM)

DESCRIPTION

The MP2384C is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter. The MP2384C offers a highly compact solution that achieves 4A of continuous output current.

The MP2384C operates at high efficiency over a wide output current load range based on MPS's proprietary switching loss reduction technique and internal low R$_{DS(ON)}$ power MOSFETs.

Adaptive constant-on-time (COT) control mode provides fast transient response and eases loop stabilization. The DC auto-tune loop combines with the remote differential sense to provide good load and line regulation.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The converter requires a minimal number of external components, and is available in a QFN-11 (2mmx2mm) package.

FEATURES

- Wide 4.5V to 24V Operating Input Range
- 105µA Low Quiescent Current
- 4A Continuous Output Current
- Adaptive Constant-On-Time (COT) Control for Fast Transient
- DC Auto-Tune Loop
- Low R$_{DS(ON)}$ Internal Power MOSFETs
- Forced PWM Operation
- Power Good (PG) Indication
- Fixed 700kHz Switching Frequency
- Stable with POSCAP and Ceramic Capacitors
- 1% Reference Voltage
- Internal Soft Start (SS)
- Output Discharge
- OCP, OVP, UVP, and Thermal Shutdown with Auto-Retry
- Available in a QFN-11 (2mmx2mm) Package

APPLICATIONS

- Security Cameras
- Portable Devices, XDSL Devices
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- General Purposes

TYPICAL APPLICATION

Efficiency
V$_{OUT}$ = 3.3V, L = 3.3µH, DCR = 9mΩ
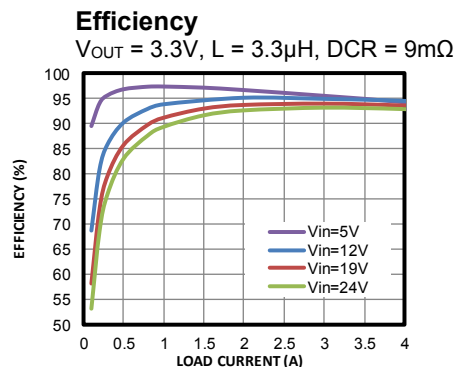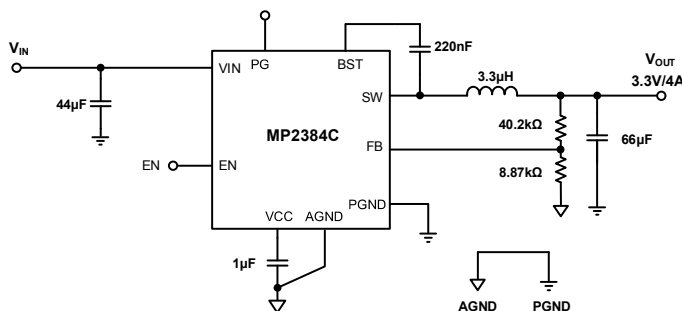
ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2384CGG	QFN-11 (2mmx2mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MP2384CGG–Z).

TOP MARKING

<div align="center">

JZY
LLL

</div>

JZ: Product code of MP2384CGG
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

QFN-11 (2mmx2mm)
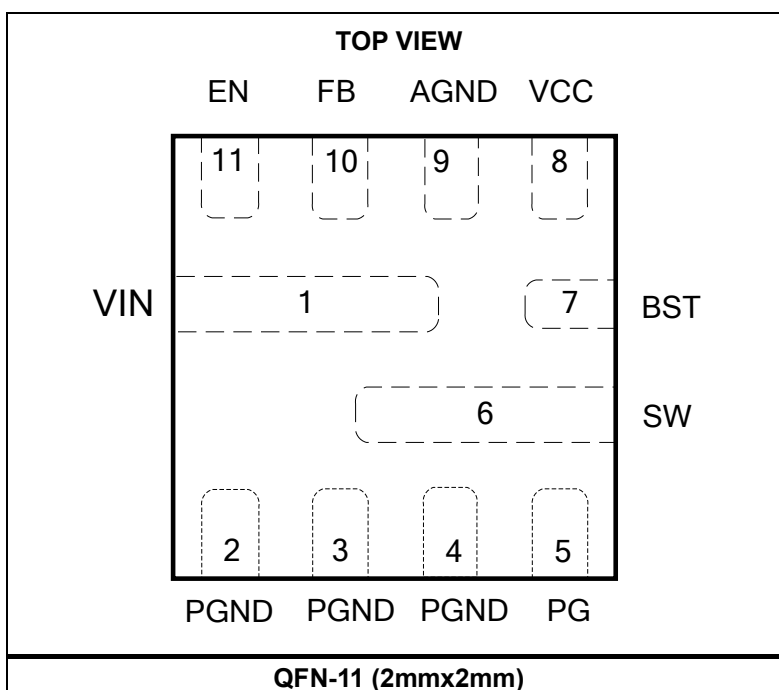
PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Supply voltage.** VIN supplies power to the internal MOSFET and regulator. The MP2384C operates from a 4.5V to 24V input rail. An input capacitor is required to decouple the input rail. Connect VIN with wide PCB traces and multiple vias. Apply at least two layers to this input trace.
2, 3, 4	PGND	**Power ground.** Connect PGND with wide PCB traces and multiple vias.
5	PG	**Power good output.** The output of PG is an open drain.
6	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on time of the PWM duty cycle. The inductor current drives SW negative during the off time. The on resistance of the low-side switch and the internal diode fixes the negative voltage. Connect SW with wide and short PCB traces. Minimize the area of the SW pattern.
7	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
8	VCC	**Internal 3V3 VCC LDO output.** VCC powers the driver and control circuits. Decouple VCC with a minimum 1µF ceramic capacitor placed as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
9	AGND	**Signal logic ground.** AGND is the Kelvin connection to PGND.
10	FB	**Feedback.** An external resistor divider from the output to GND, tapped to FB, sets the output voltage. Place the resistor divider as close to FB as possible. Avoid vias on the FB traces and V_{SEN} trace. Route the V_{SEN} trace away from the SW node.
11	EN	**Buck enable pin.** EN is a digital input that turns the buck regulator on or off. When the power supply of the control circuit is ready, drive EN high to turn on the buck regulator. Drive EN low to turn off the buck regulator. Connect EN to VIN through a resistive voltage divider for automatic start-up. The EN voltage must not exceed 4.5V. Do not float EN.

ABSOLUTE MAXIMUM RATINGS [1]

Supply voltage (V_{IN}) 26V
V_{SW} (DC).................................. -1V to V_{IN} + 0.3V
V_{SW} (25ns)............................ -3.6V to V_{IN} + 4V [2]
V_{BST}..V_{SW} + 4.5V
All other pins .... -0.3V to +4.5V
Continuous power dissipation…(T_A = 25°C) [3] [5]
QFN-11 (2mmx2mm) 3.6W
Junction temperature .... 150°C
Lead temperature..................................... 260°C
Storage temperature.................-65°C to +150°C

ESD Rating

Human-body model (HBM) 1.8kV
Charged-device model (CDM)......................2kV

Recommended Operating Conditions [4]

Supply voltage (V_{IN}) .... 4.5V to 24V
Output voltage (V_{OUT})....................... 0.6V to 13V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance $θ_{JA}$ $θ_{JC}$

QFN-11 (2mmx2mm)
EV2384C-G-00A [5] .... 34 .... 9 .... °C/W
JESD51-7 [6] .... 80 .... 16 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Measured by using differential oscilloscope probe.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance $θ_{JA}$, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / $θ_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EV2384C-G-00A, 4-layer PCB, 64mmx64mm.
6) The value of $θ_{JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

Electrical CharacteristicS

V_{IN} = 12V, T_J = -40°C to +125°C [7], typical value is tested at T_J = 25°C, unless otherwise noted.

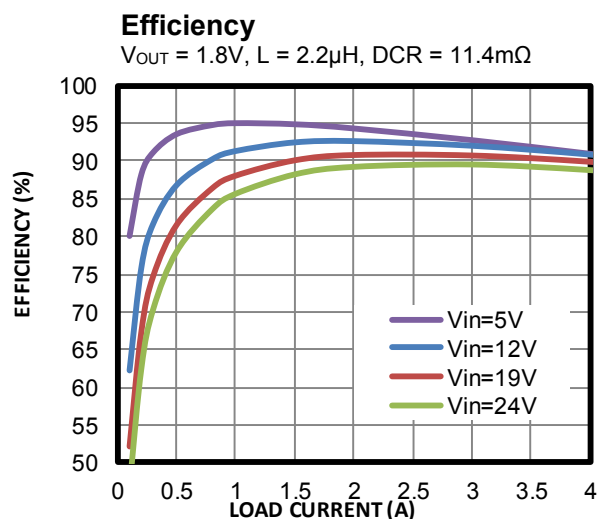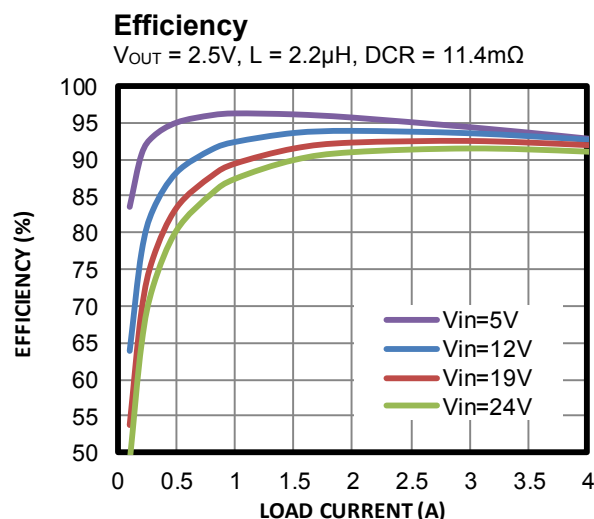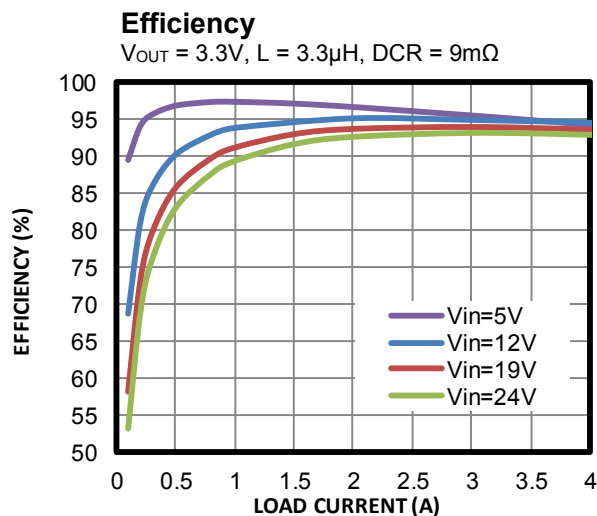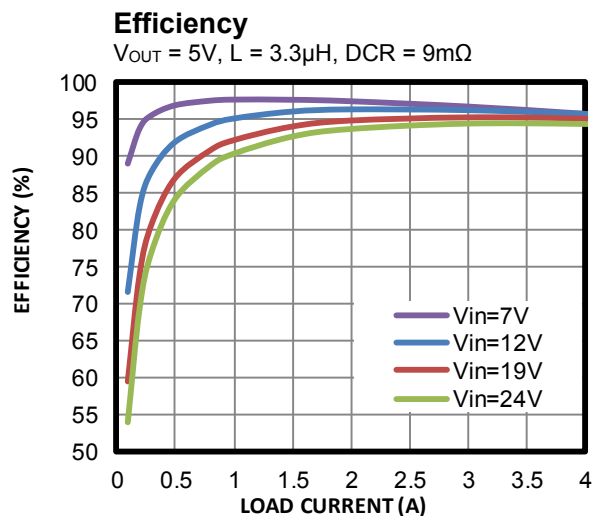| Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (quiescent)	I_{IN}	V_{EN} = 3.3V, V_{FB} = 0.62V		105	145	µA
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			2	µA
MOSFET						
High-side switch on resistance	HS_{RDS-ON}			60		mΩ
Low-side switch on resistance	LS_{RDS-ON}			20		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V		0	5	µA
Current Limit						
Low-side valley current limit	I_{LIMIT_LS}		4.5	6.5	8	A
Negative current limit	I_{NEG}	V_{OUT} = 3.3V, L_O = 2.2µH, T_J = 25°C	-2	-1.5	-1	A
Switching Frequency and Minimum Off Timer						
Switching frequency	f_{SW}		600	700	800	kHz
Minimum on time [8]	t_{ON_Min}			50		ns
Minimum off time [8]	t_{OFF_Min}			200		ns
Over-Voltage and Under-Voltage Protection (OVP, UVP)						
OVP threshold	V_{OVP}	V_{FB}	125%	130%	135%	V_{REF}
UVP-1 threshold	V_{UVP}	V_{FB}	70%	75%	80%	V_{REF}
UVP-1 hold off timer [8]	t_{OC}	V_{OUT} = 60% of V_{REF}		32		µs
UVP-2 threshold	V_{UVP}	V_{FB}	45%	50%	55%	V_{REF}
Reference and Soft Start (REF, SS)						
REF voltage	V_{REF}		590	600	610	mV
Soft-start time [8]	t_{SS}		1.1	1.7	2.3	ms
Enable and UVLO (EN, UVLO)						
Enable rising threshold	V_{EN_Rising}		1.15	1.25	1.35	V
Enable hysteresis	V_{EN_HYS}			150		mV
Enable input current	I_{EN}	V_{EN} = 3.3V		3.3		µA
VCC UVLO rising threshold	VCC_{Vth_R}		3.1	3.3	3.5	V
VCC UVLO hysteresis threshold	VCC_{HYS}			420		mV
VIN UVLO rising threshold	VIN_{VTH_R}		4.2	4.35	4.48	V
VIN UVLO hysteresis threshold	VIN_{HYS}			550		V
VCC Regulator						
VCC voltage	V_{CC}		3.45	3.65	3.85	V
VCC load regulation	V_{CC_Reg}	I_{VCC} = 5mA		5		%
Thermal Protection						
Thermal shutdown [8]	T_{SD}			150		°C
Thermal shutdown hysteresis [8]	T_{SD_HYS}			25		°C

Notes:

7) Not tested in production. Guaranteed by over-temperature correlation.
8) Guaranteed by engineering sample characterization.

TYPICAL CHARACTERISTICS
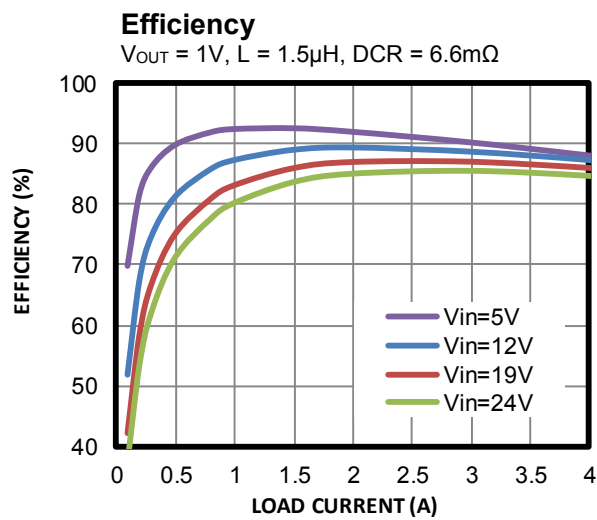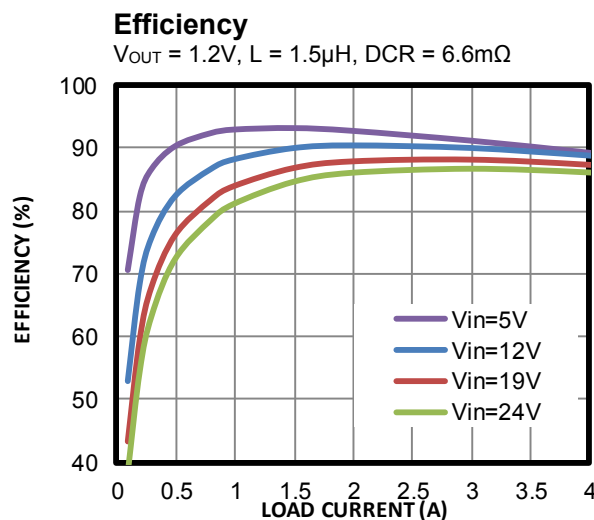
V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

Efficiency
V_{OUT} = 5V, L = 3.3µH, DCR = 9mΩ

Efficiency
V_{OUT} = 3.3V, L = 3.3µH, DCR = 9mΩ

Efficiency
V_{OUT} = 2.5V, L = 2.2µH, DCR = 11.4mΩ

Efficiency
V_{OUT} = 1.8V, L = 2.2µH, DCR = 11.4mΩ

Efficiency
V_{OUT} = 1.2V, L = 1.5µH, DCR = 6.6mΩ

Efficiency
V_{OUT} = 1V, L = 1.5µH, DCR = 6.6mΩ

TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

Load Regulation
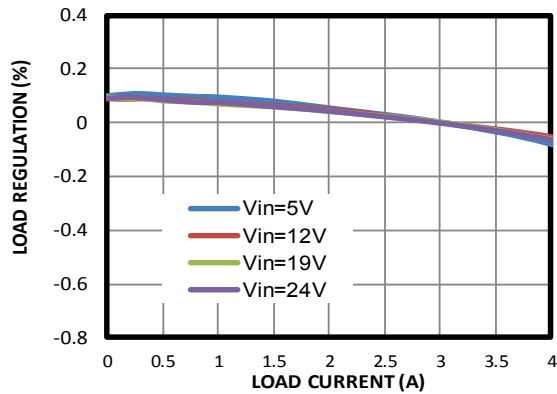
Enabled Supply Current vs. Input Voltage
V_{EN} = 3.3V, V_{FB} = 0.62V
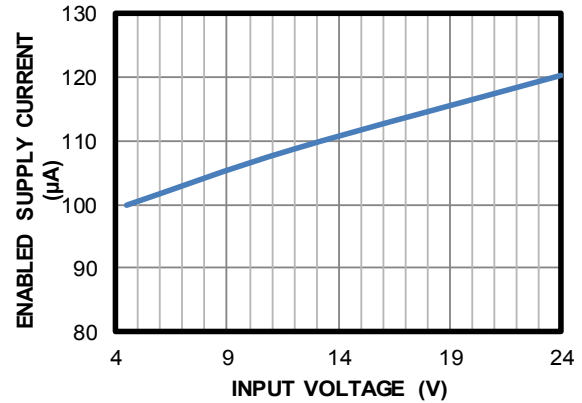
Disabled Supply Current vs. Input Voltage
V_{EN} = 0V
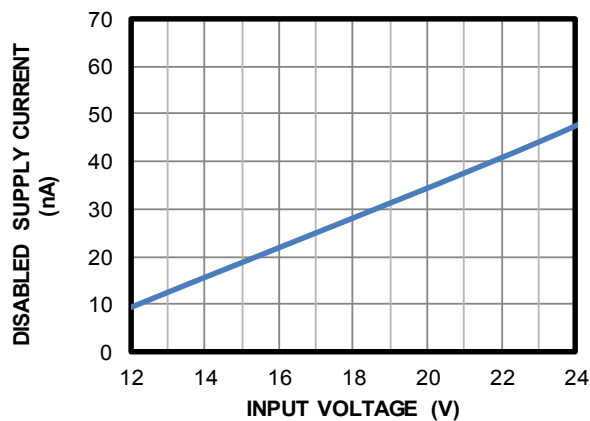
Input Voltage Threshold vs. Temperature
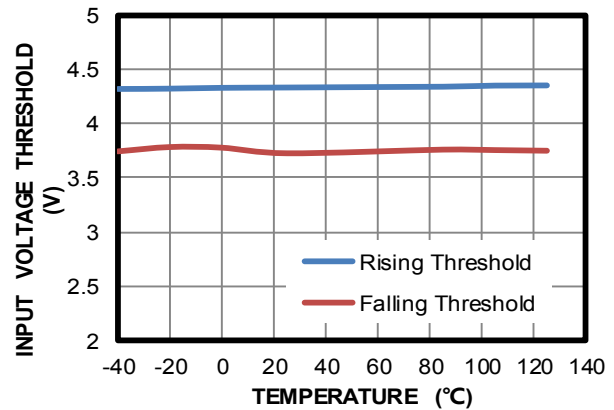
Case Temperature Rise vs. Load Current
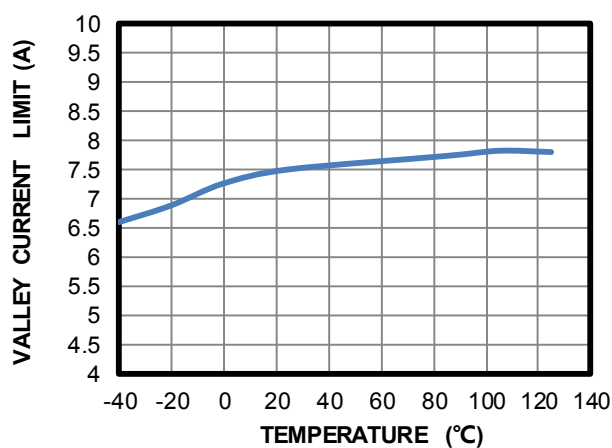V_{IN} = 19V, V_{OUT} = 3.3V
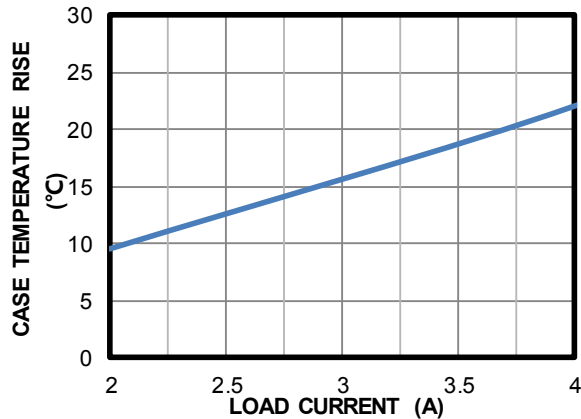
Input Voltage Threshold vs. Temperature
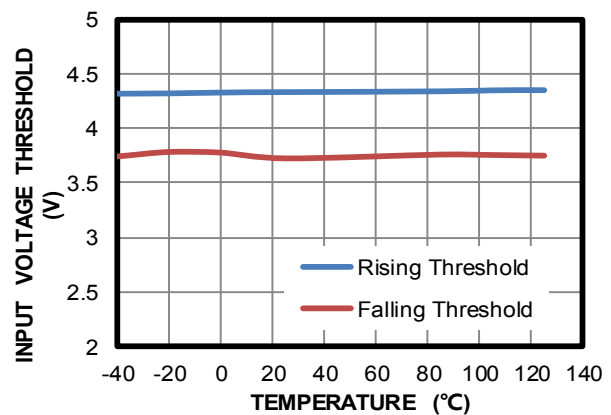
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

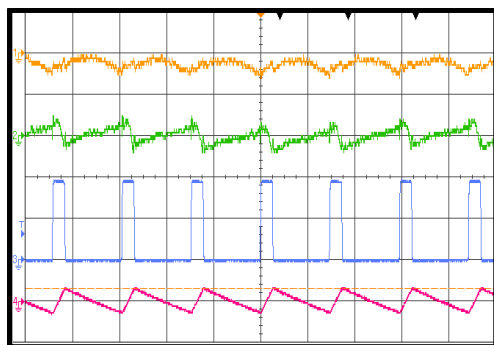**FB Voltage vs. Temperature**
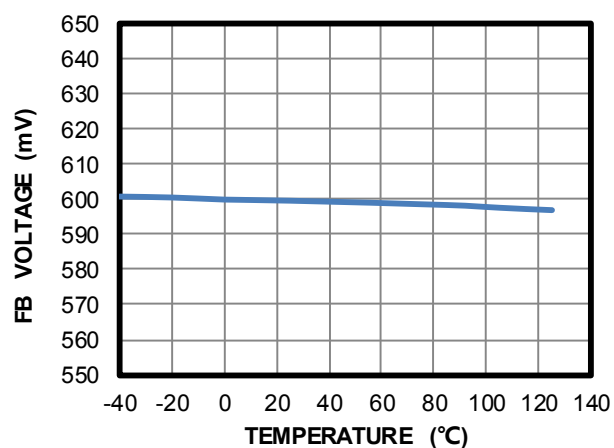
Valley Current Limit vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

Input/Output Ripple
I_{OUT} = 0A

CH1:
V_{OUT}/AC
20mV/div.

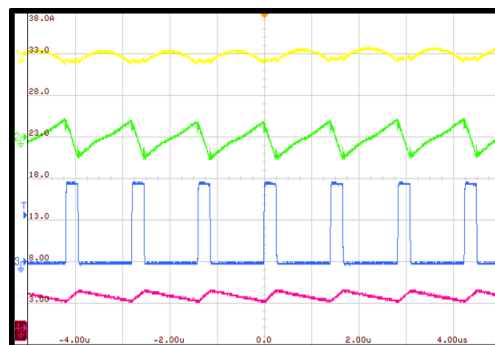CH2: V_{IN}/AC
20mV/div.

CH3: V_{SW}
10V/div.

CH4: I_L
2A/div.

1µs/div.

Input/Output Ripple
I_{OUT} = 4A

CH1:
V_{OUT}/AC
20mV/div.

CH2: V_{IN}/AC
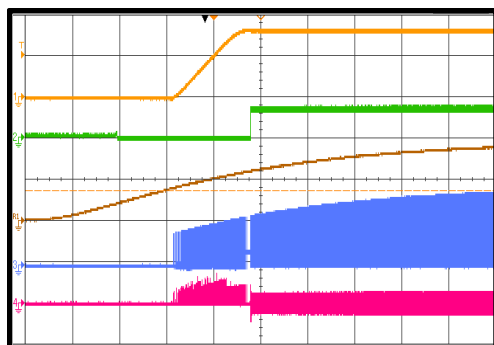200mV/div.

CH3: V_{SW}
10V/div.

CH4: I_L
5A/div.

1µs/div.

Start-Up through Input Voltage
I_{OUT} = 0A

CH1: V_{OUT}
2V/div.

CH2: V_{PG}
5V/div.

R1: V_{IN}
10V/div.

CH3: V_{SW}
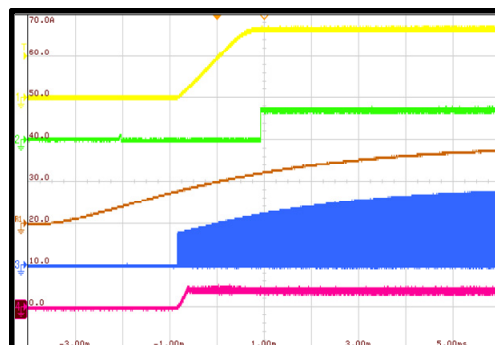10V/div.

CH4: I_L
2A/div.

1ms/div.

Start-Up through Input Voltage
I_{OUT} = 4A

CH1: V_{OUT}
2V/div.

CH2: V_{PG}
5V/div.

R1: V_{IN}
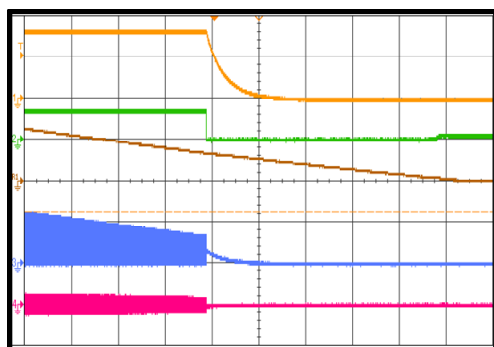10V/div

CH3: V_{SW}
10V/div.

CH4: I_L
10A/div.

2ms/div.

Shutdown through Input Voltage
I_{OUT} = 0A

CH1: V_{OUT}
2V/div.

CH2: V_{PG}
5V/div.

R1: V_{IN}
10V/div.

CH3: V_{SW}
10V/div.
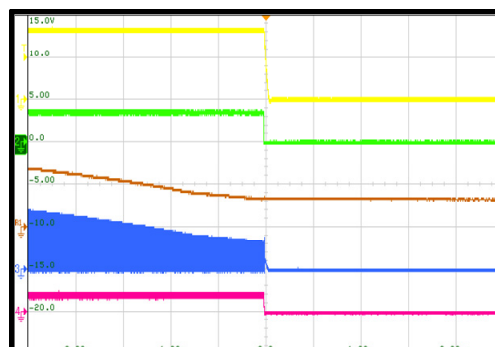
CH4: I_L
2A/div.

10ms/div.

Shutdown through Input Voltage
I_{OUT} = 4A

CH1: V_{OUT}
2V/div.

CH2: V_{PG}
5V/div.

R1: V_{IN}
10V/div.
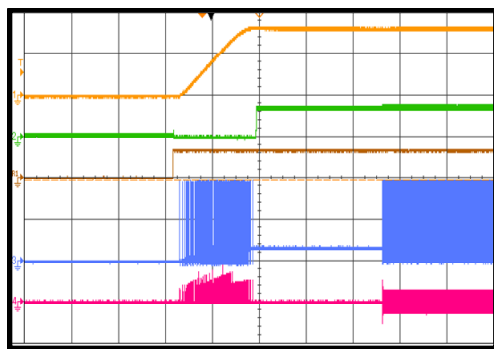
CH3: V_{SW}
10V/div.

CH4: I_L
10A/div.

2ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

Start-Up through Enable
I_{OUT} = 0A

CH1: V_{OUT}
2V/div.

CH2: V_{PG}
5V/div.

R1: V_{EN}
5V/div.

CH3: V_{SW}
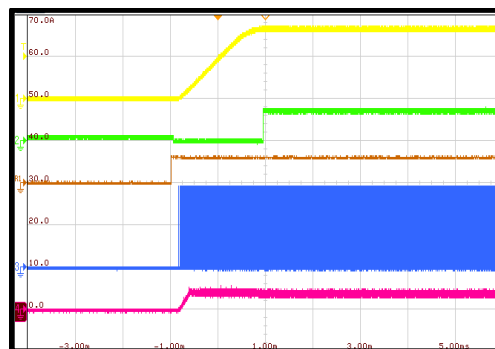10V/div.

CH4: I_L
2A/div.

1ms/div.

Start-Up through Enable
I_{OUT} = 4A

CH1: V_{OUT}
2V/div.

CH2: V_{PG}
5V/div.

R1: V_{EN}
5V/div.

CH3: V_{SW}
10V/div.
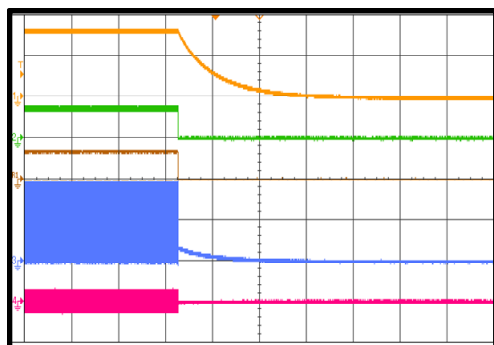
CH4: I_L
10A/div.

1ms/div.

Shutdown through Enable
I_{OUT} = 0A

CH1: V_{OUT}
2V/div.

CH2: V_{PG}
5V/div.

R1: V_{EN}
5V/div.

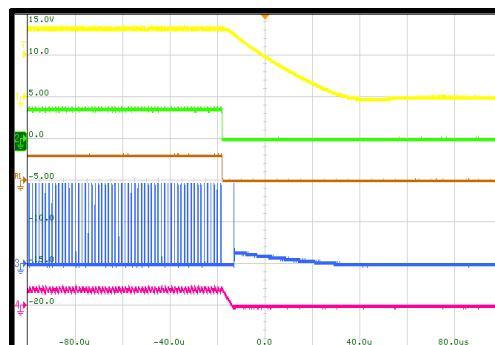CH3: V_{SW}
10V/div.

CH4: I_L
2A/div.

5ms/div.

Shutdown through Enable
I_{OUT} = 4A

CH1: V_{OUT}
2V/div.

CH2: V_{PG}
5V/div.

R1: V_{EN}
5V/div

CH3: V_{SW}
10V/div.

CH4: I_L
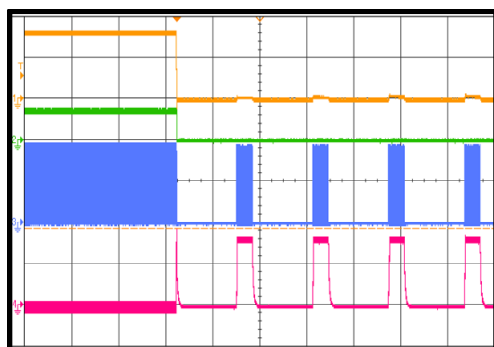10A/div.

400µs/div.

Short-Circuit Entry
I_{OUT} = 0A

CH1: V_{OUT}
2V/div.

CH2: V_{PG}
5V/div.

CH3: V_{SW}
10V/div.

CH4: I_L
5A/div.

5ms/div.

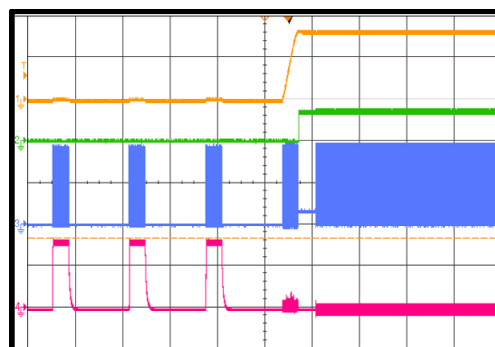**Short-Circuit Recovery**
I_{OUT} = 0A

CH1: V_{OUT}
2V/div.

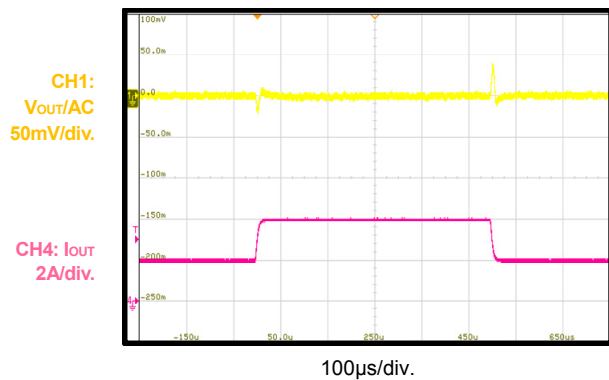CH2: V_{PG}
5V/div.

CH3: V_{SW}
10V/div.

CH4: I_L
5A/div.

5ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

Load Transient
I_{OUT} = 2A to 4A

100µs/div.

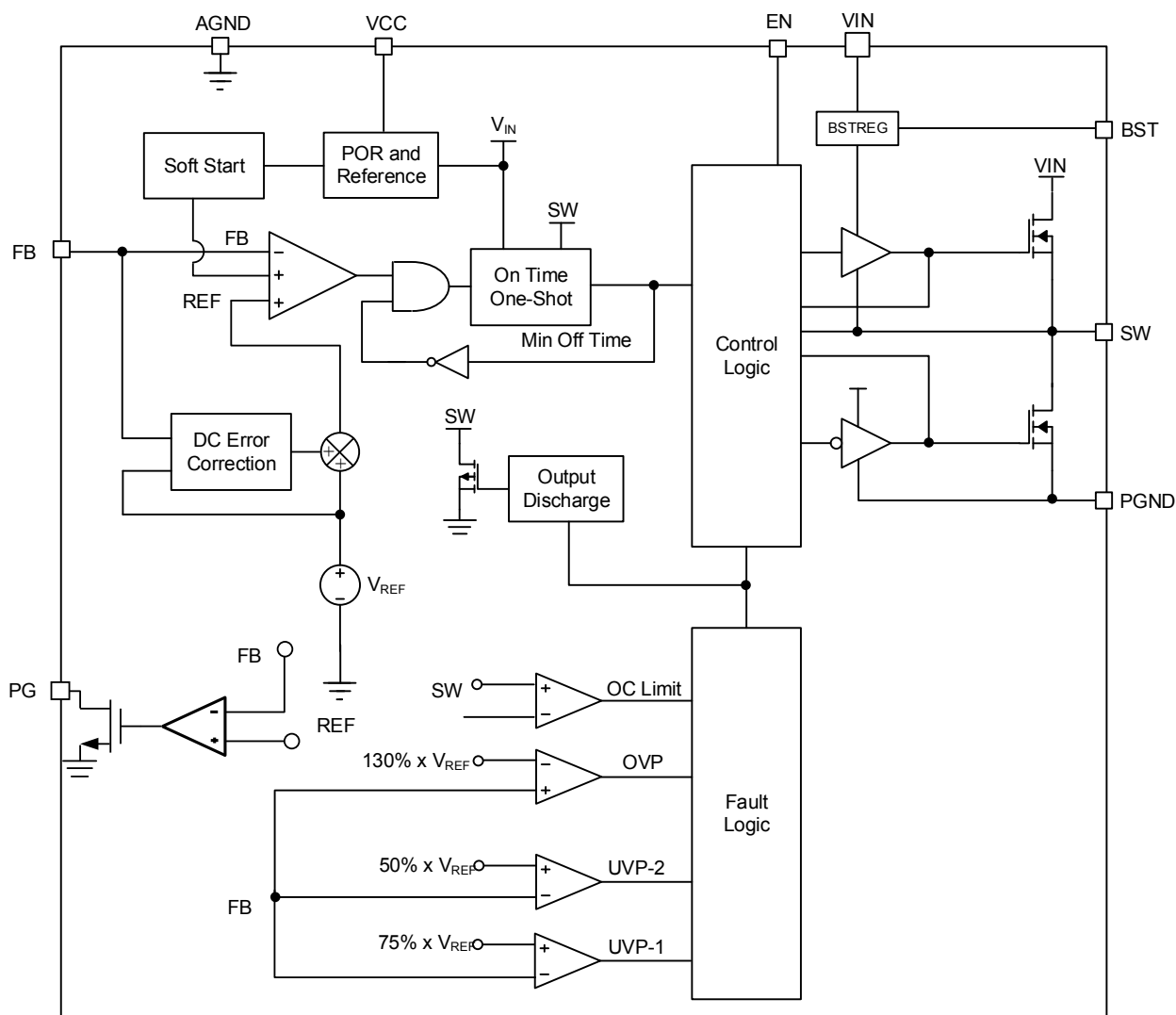## FUNCTIONAL BLOCK DIAGRAM

Figure 1: Functional Block Diagram

OPERATION

The MP2384C is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control provides fast transient response and eases loop stabilization.

Pulse-Width Modulation (PWM) Operation

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}) and indicates that there is an insufficient output voltage. The on period is determined by the output voltage and input voltage to maintain a constant switching frequency across the input voltage range.

The MP2384C operates in forced continuous conduction mode (CCM). The LS-FET turns on when the HS-FET is off to minimize conduction loss. If both the HS-FET and LS-FET are turned on at the same time, there is a dead short between the input and GND. This is called shoot-through. To prevent shoot-through, a dead time is generated internally between the time when the HS-FET turns off and the LS-FET turns on, or vice versa.

Internal compensation is applied for COT control to provide more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

Large Duty Cycle Operation

When V_{IN} is below 7V and V_{OUT} is above 4.2V, the MP2384C reduces the switching frequency to about 280kHz to support large duty cycle operation. If V_{OUT} drops below 3.9V, the MP2384C returns to the normal switching frequency.

Jitter and FB Ramp

Jitter occurs in both PWM and skip mode when noise in the V_{FB} ripple propagates a delay to the HS-FET driver (see Figure 2 and Figure 3). Jitter can affect system stability with noise immunity that is proportional to the steepness of V_{FB}'s downward slope. Therefore, the jitter in DCM is usually greater than that in CCM. However, the V_{FB} ripple does not directly affect noise immunity.
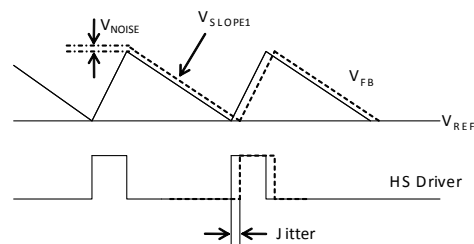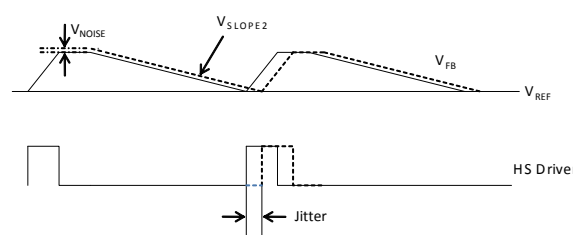

Figure 2: Jitter in PWM Mode

Figure 3: Jitter in Skip Mode

Operating with External Ramp Compensation

The MP2384C can typically support ceramic output capacitors without an external ramp. However, in some cases, the internal ramp may not be enough to stabilize the system, or the jitter may be too large. In these cases, external ramp compensation is required. See the Setting the Output Voltage with External Compensation section on page 15 for design steps using external ramp compensation.

Configuring the EN Control

The enable pin (EN) enables or disables the entire chip. Pull EN high to turn the regulator on; pull EN low to turn it off. Do not float EN.

For automatic start-up, EN can be pulled up to the input voltage through a resistive voltage divider. Choose the values of the pull-up resistor (R_{UP} from VIN to EN) and the pull-down resistor (R_{DOWN} from EN to GND) to calculate the automatic start-up voltage with Equation (1):

$$V_{IN-START} = 1.25 \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} (V) \qquad (1)$$

For example, when R_{UP} = 150kΩ and R_{DOWN} = 51kΩ, $V_{IN-START}$ is 4.92V.

To avoid damaging the internal circuit, the EN voltage must not exceed 4.5V.

Power Good (PG)

The power good (PG) pin indicates whether the output voltage is in the normal range compared to the internal reference voltage. PG is an open-drain structure, and requires an external pull-up supply. During power-up, the PG output is pulled low. This indicates that the system must remain off and keep the load on the output to a minimum, which reduces inrush current during start-up.

When the output voltage is between 95% and 115% of the internal reference voltage after soft start finishes, the PG signal is pulled high. When the output voltage is below 90% of the internal reference voltage after soft start finishes, the PG signal remains low. When the output voltage exceeds 115% of the internal reference, PG switches low. The PG signal rises high again after the output voltage drops below 105% of the internal V_{REF}. The PG output is pulled low when EN under-voltage lockout (UVLO), input UVLO, over-current protection (OCP), or over-temperature protection (OTP) is triggered.

Soft Start (SS)

The MP2384C employs a soft start (SS) mechanism to ensure a smooth output during power-up. When EN rises high, the internal V_{REF} ramps up gradually, and the output voltage ramps up smoothly as well. Once V_{REF} reaches its target value, soft start finishes, and the device enters steady-state operation.

If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the FB node.

Over-Current Limit

The MP2384C has cycle-by-cycle over-current limit (OCL) control. The current-limit circuit employs a valley current-sensing algorithm. The MP2384C uses the LS-FET $R_{DS(ON)}$ as a current-sensing element. If the magnitude of the current-sense signal exceeds the current-limit threshold, the PWM cannot initiate a new cycle, even if FB is below REF. Figure 4 shows the detailed operation of the valley-current limit.
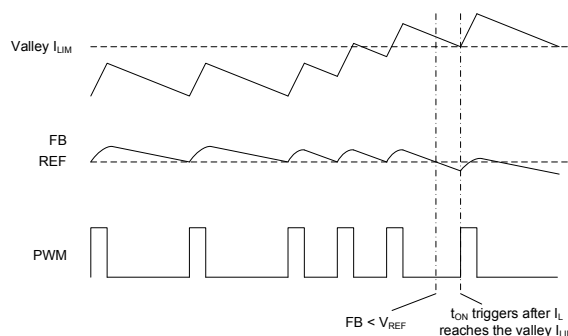

Figure 4: Valley Current-Limit Control

Since the comparison is done during the low-side on state, the OC trip level sets the valley level of the inductor current. The maximum load current at the over-current threshold (I_{OC}) can be calculated with Equation (2):

$$I_{OC} = I_{LIMIT} + \frac{\Delta I_{inductor}}{2} \qquad (2)$$

The OCL itself limits the inductor current and does not latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor, making the output voltage fall off. Eventually, the current crosses the under-voltage protection (UVP) threshold, and the MP2384C enters hiccup protection mode.

Over-Voltage (OV) and Under-Voltage (UV) Protection

The MP2384C monitors a resistor-divided feedback voltage to detect over-voltage (OV) and under-voltage (UV) conditions. When V_{FB} rises above 130% of the target voltage, the over-voltage protection (OVP) comparator output goes high, and the circuit latches as the HS-FET driver turns off. The LS-FET then turns on and acts as a current source.

When V_{FB} is between 50% and 75% of V_{REF}, the UVP-1 comparator output goes high, and the MP2384C enters hiccup mode if V_{FB} remains in this range for about 32µs. The LS-FET remains on until the inductor current drops to zero. During this period, the valley current limit controls the inductor current.

When V_{FB} drops below 50% of V_{REF}, the UVP-2 comparator output goes high, and the MP2384C enters hiccup mode directly after the comparator and logic delay.

UVLO Protection

The MP2384C has two types of under-voltage lockout (UVLO) protection: VCC UVLO and V_{IN} UVLO. The MP2384C starts up only when both VCC and V_{IN} exceed their respective UVLO thresholds. The MP2384C shuts down when either VCC is below the UVLO falling threshold voltage, or VIN is below the V_{IN} falling threshold. These are both non-latch protections.

If an application requires a higher UVLO, use EN and two external resistors to adjust the input voltage UVLO (see Figure 5).
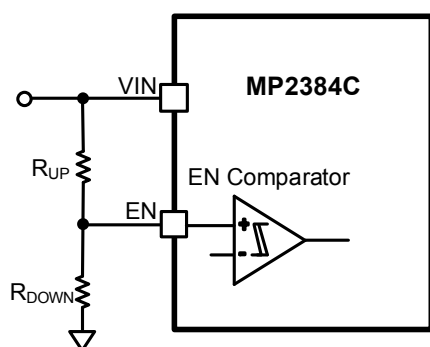

Figure 5: Adjustable UVLO

Thermal Shutdown

The MP2384C has a thermal shutdown function. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. This is a non-latch protection. There is a hysteresis of about 25°C. Once the junction temperature drops to about 125°C, soft start initiates.

Output Discharge

The MP2384C discharges the output when the controller is turned off by a protection function (UVP, OCP, OVP, UVLO, or thermal shutdown). The discharge resistor on the output is typically 6Ω.

APPLICATION INFORMATION

Setting the Output Voltage without External Compensation

The MP2384C does not require ramp compensation for applications using POSCAP or ceramic capacitors as output capacitors. The output voltage is set by feedback resistors R1 and R2 (see Figure 6).
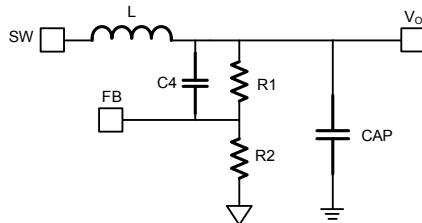

Figure 6: Simplified Circuit without an External Ramp

First, choose a value for R2. If R2 has a low resistance, it may lead to considerable quiescent current loss. If R2 has a high resistance, it makes FB noise-sensitive. Set R2 between 5kΩ and 100kΩ. Use a higher-value R2 when V_{OUT} is low and a lower-value R2 when V_{OUT} is high. Considering the output ripple, R1 can be estimated with Equation (3):

$$R_1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_2 \qquad (3)$$

C4 acts as a feed-forward capacitor that improves the transient. It can be set between 100pF and 1nF. A higher capacitance improves transient but contributes to noise sensitivity.

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Parameter Selection for Common Output Voltages [9]

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)	L (µH)
5	40.2	5.49	33	3.3
3.3	40.2	8.87	33	3.3
2.5	40.2	12.7	33	2.2
1.8	40.2	20	33	2.2
1.5	40.2	26.7	33	1.5
1.2	40.2	40.2	33	1.5
1	40.2	60.4	33	1.5

Note:

9) For additional component parameters, see the Typical Application Circuits on pages 18, 19, and 20.

Setting the Output Voltage with External Compensation

If the system is not stable or the jitter is too great when ceramic capacitors are used in the output, an external voltage ramp should be added to FB through resistor R4 and capacitor C4. Since an internal ramp has already been added in the system, a 1MΩ (R4), 220pF (C4) ramp is sufficient for the ramp.
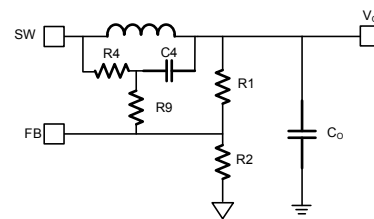

Figure 7: Simplified Circuit with External Ramp

The output voltage is influenced by R4, in addition to the R1 and R2 divider (see Figure 7). If R2 has a low resistance, it may lead to considerable quiescent current loss. If R2 has a high resistance, it makes FB noise-sensitive. Set R2 between 5kΩ and 100kΩ. Use a higher-value R2 when V_{OUT} is low and a lower-value R2 when V_{OUT} is high. R1 can then be calculated with Equation (4):

$$R_1 = \frac{1}{\frac{V_{REF}}{V_{OUT} - V_{REF}} - \frac{R2}{R4}} \times R_2 \qquad (4)$$

Usually, R9 is set to 0Ω. To get a pole for improved noise immunity, R9 can be set using Equation (5):

$$R_9 = \frac{1}{2\pi \times C_4 \times 2f_{SW}} \qquad (5)$$

Set R9 between 100Ω and 1kΩ to reduce its influence on the ramp.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance, and should be placed as close to VIN as possible. Capacitors with X5R and X7R ceramic

dielectrics are recommended since they are fairly stable with temperature fluctuations.

The capacitors must have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (6):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \qquad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (7):

$$I_{CIN} = \frac{I_{OUT}}{2} \qquad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \qquad (8)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (9):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \qquad (9)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (10)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \qquad (11)$$

The output voltage ripple caused by ESR is very small, and requires an external ramp to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4.

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR dominates the output ripple. The output ripple can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \qquad (12)$$

The maximum output capacitor limitation should also be considered in the design application. The MP2384C has a soft-start time of about 1.6ms. If the output capacitance is too high, then the output voltage cannot reach the design value during the soft-start time and fails to regulate. The maximum output capacitor value (C_{O_MAX}) can be estimated with Equation (13):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{ss} / V_{OUT} \qquad (13)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and t_{ss} is the soft-start time.

Selecting the Inductor

An inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage. However, they are also physically larger, have a higher series resistance, and have a lower saturation current.

A good rule to determine the inductance value is to design the peak-to-peak ripple current in the inductor to be between 30% and 50% of the maximum output current, and ensure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated with Equation (14):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \qquad (14)$$

Where ΔI_L is the peak-to-peak inductor ripple current. The inductor should not saturate under

the maximum inductor peak current, including short current. I_{SAT} should remain below 9A.

Design Example

Table 2 lists a design example when ceramic capacitors are applied.

Table 2: Design Example

V_{IN}	8V to 24V
V_{OUT}	3.3V
I_{OUT}	4A

For detailed application schematics, see the Typical Application Circuits on pages 18, 19, and 20. For typical performance waveforms, see the Typical Characteristics section on pages 5 to 10. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is recommended for improved thermal performance. For the best results, refer to Figure 8 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, SW) very close to the device with short, direct, and wide traces.

2. Place the input capacitors as close to VIN and GND as possible.

3. Place the decoupling capacitor as close to VCC and GND as possible.

4. Keep the switching node (SW) short and route away from the feedback network.

5. Keep the BST voltage path as short as possible.

6. Keep the VIN and GND pads connected with large copper pours to improve thermal performance.

7. Add several vias close to the VIN and GND pads to improve thermal dissipation.
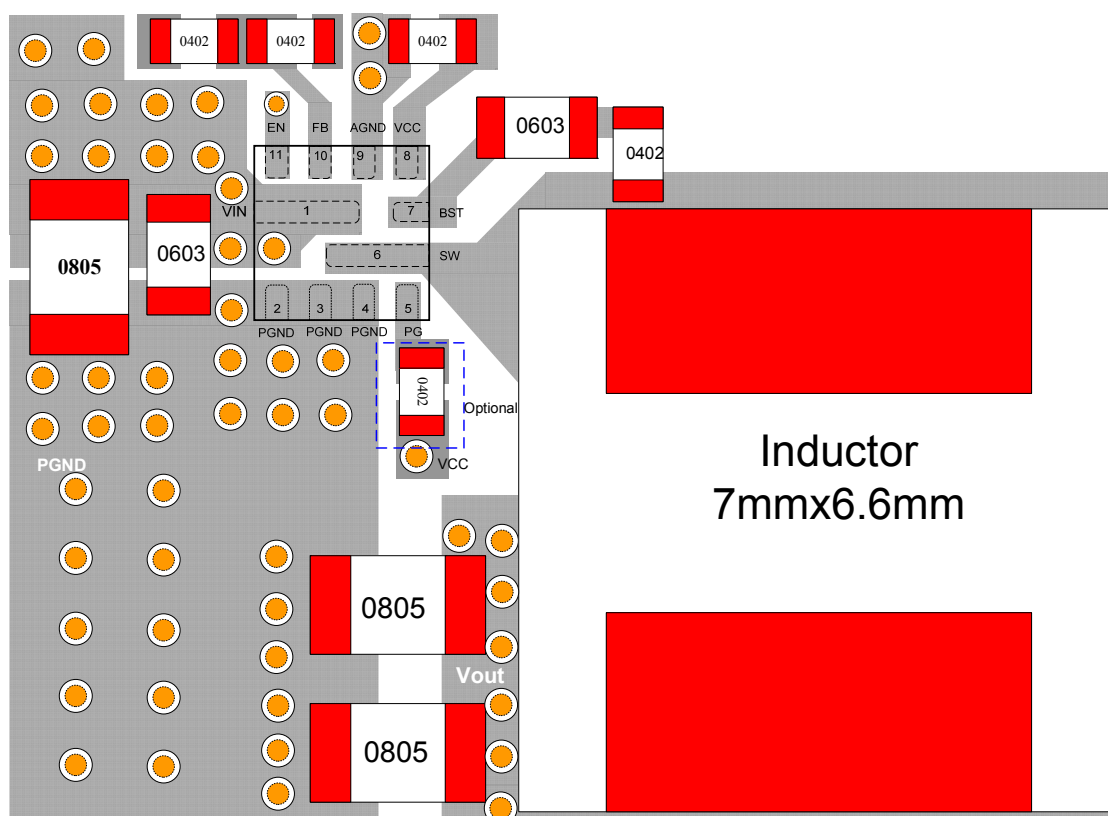
Figure 8: Recommended PCB Layout
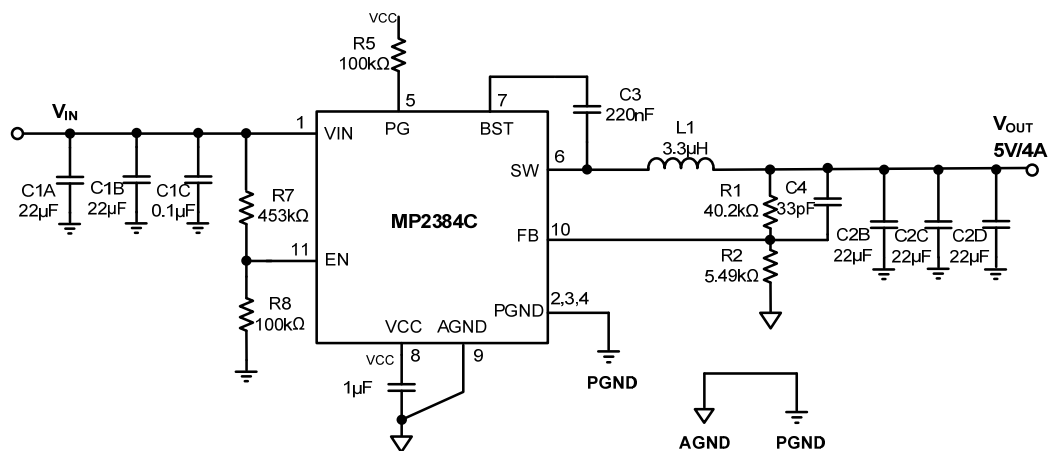
TYPICAL APPLICATION CIRCUITS [10]

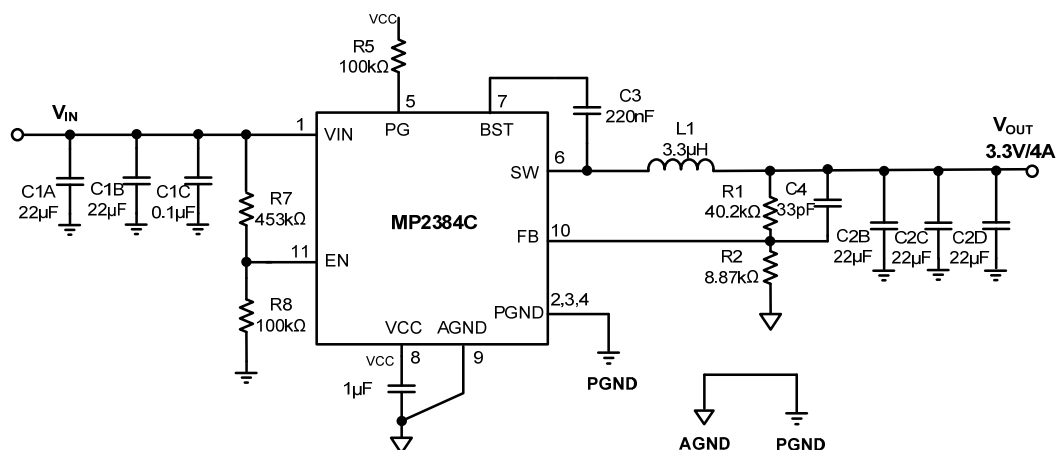**Figure 9: V_{IN} = 19V, V_{OUT} = 5V/4A**
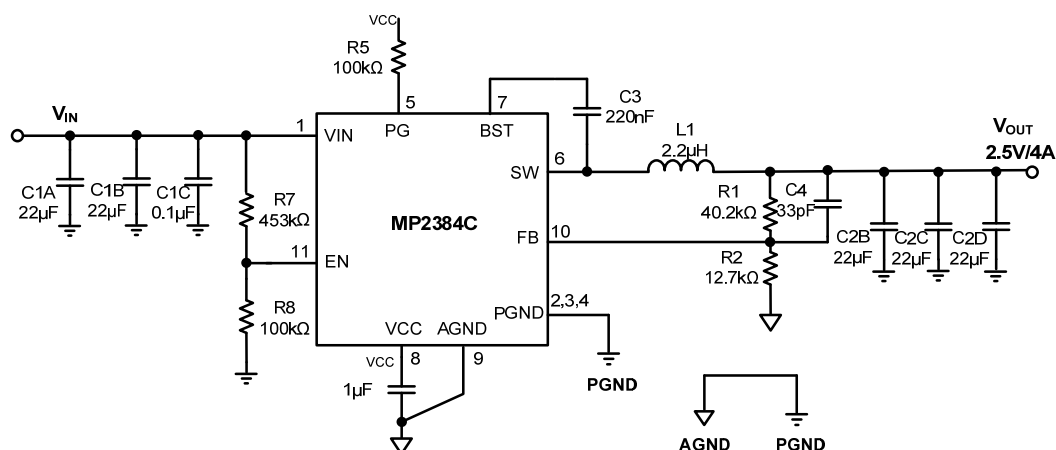

Figure 10: V_{IN} = 19V, V_{OUT} = 3.3V/4A

Figure 11: V_{IN} = 19V, V_{OUT} = 2.5V/4A
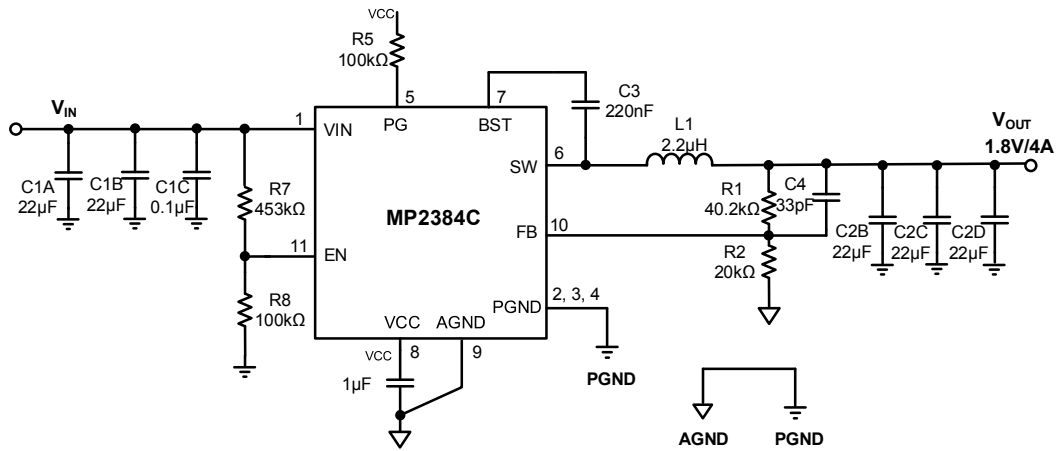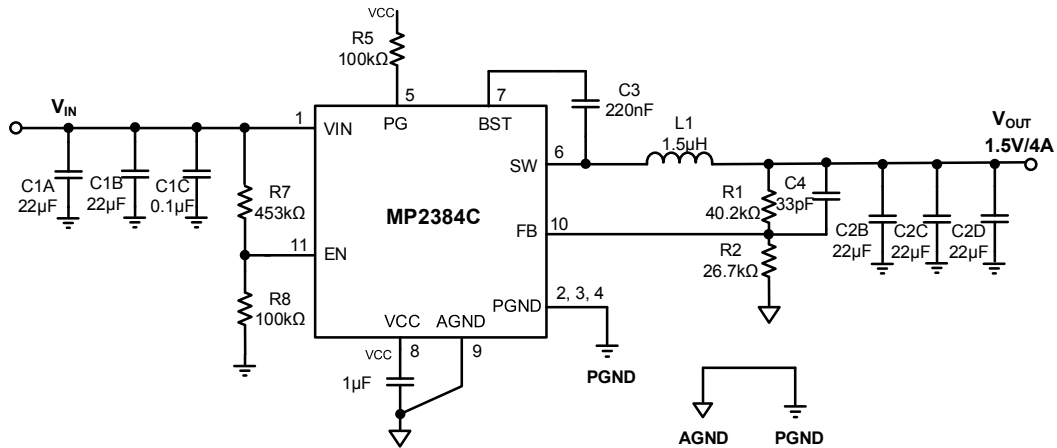
TYPICAL APPLICATION CIRCUITS [10] *(continued)*

Figure 12: V$_{IN}$ = 19V, V$_{OUT}$ = 1.8V/4A
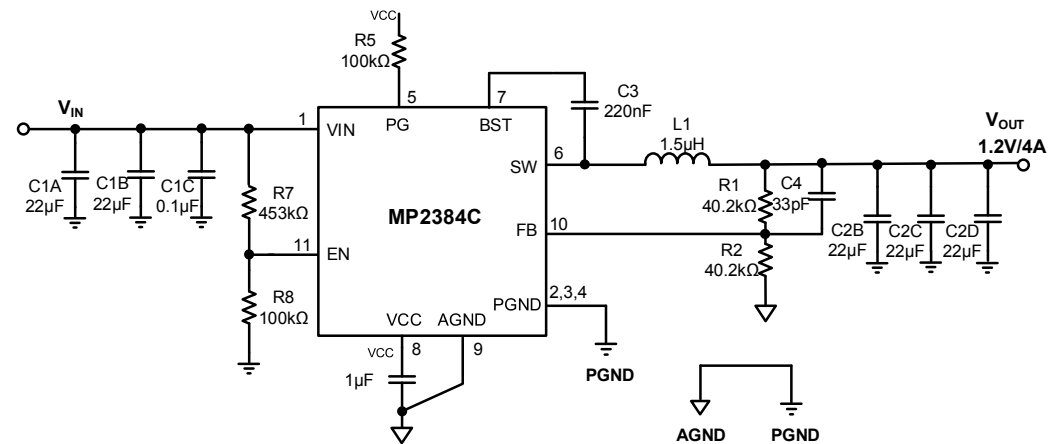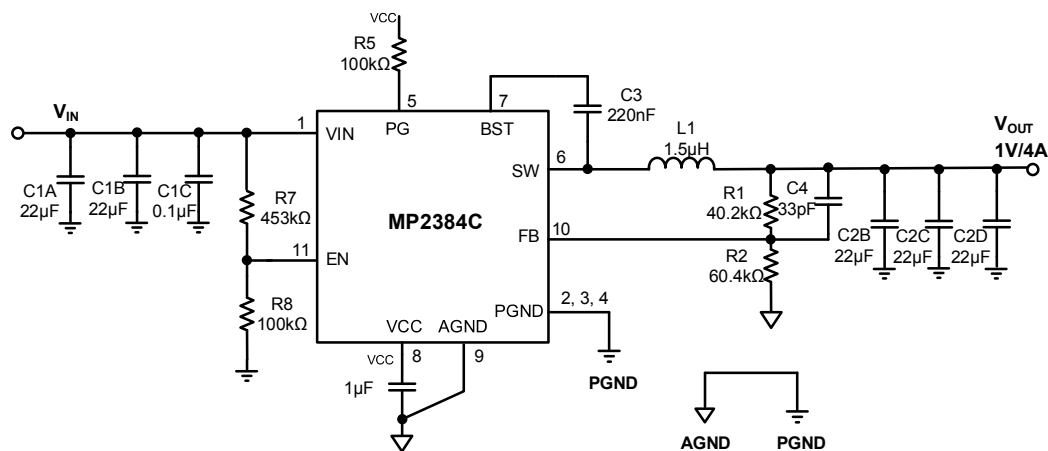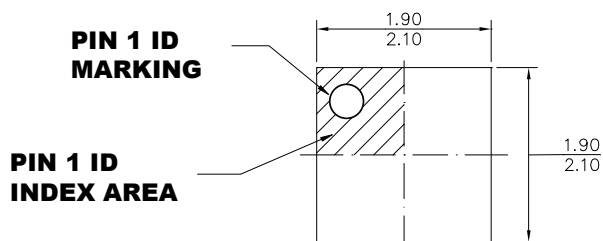

Figure 13: V$_{IN}$ = 19V, V$_{OUT}$ = 1.5V/4A

Figure 14: V$_{IN}$ = 19V, V$_{OUT}$ = 1.2V/4A

TYPICAL APPLICATION CIRCUITS [10] *(continued)*

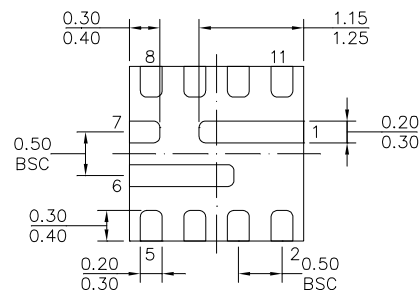**Figure 15: V_{IN} = 19V, V_{OUT} = 1V/4A**

Note:

10) The EN resistor divider sets the VIN threshold to 7.5V. For 5V input applications, change the EN resistor accordingly.
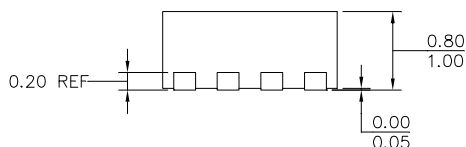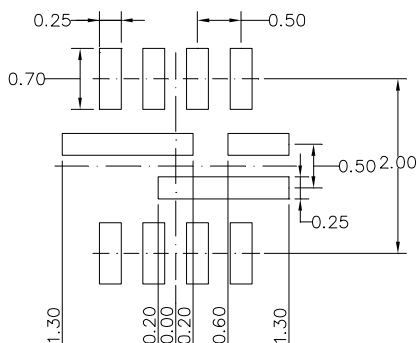
PACKAGE INFORMATION

QFN-11 (2mmx2mm)

PIN 1 ID
MARKING

PIN 1 ID
INDEX AREA

1.90
2.10

1.90
2.10

TOP VIEW

0.30
0.40

1.15
1.25

8   11

7   1   0.20
0.30

0.50
BSC

6

0.30
0.40

0.20
0.30   5   2   0.50
BSC

BOTTOM VIEW

0.80
1.00

0.20 REF

0.00
0.05

SIDE VIEW

0.25   0.50

0.70

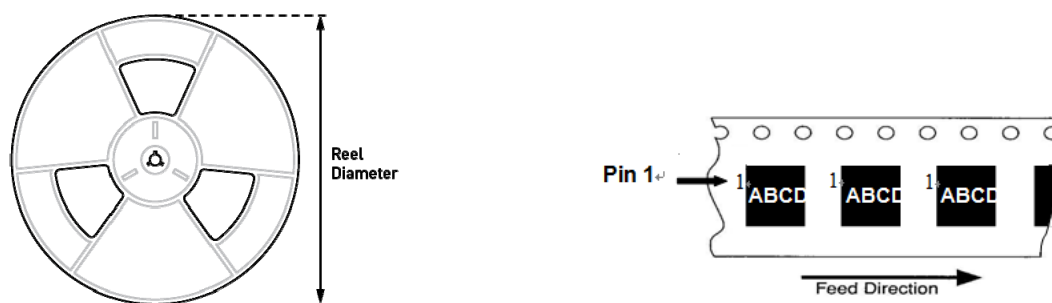0.50 2.00

0.25

1.30   0.20 0.00 0.20 0.60   1.30

RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1 AND PIN6 HAVE THE SAME LENGTH AND WIDTH
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220, VARIATION VCCD.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION

Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2384CGG-Z	QFN-11 (2mmx2mm)	5000	N/A	13in	12mm	8mm

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  [MP2384CGG-P](#) [MP2384CGG-Z](#)