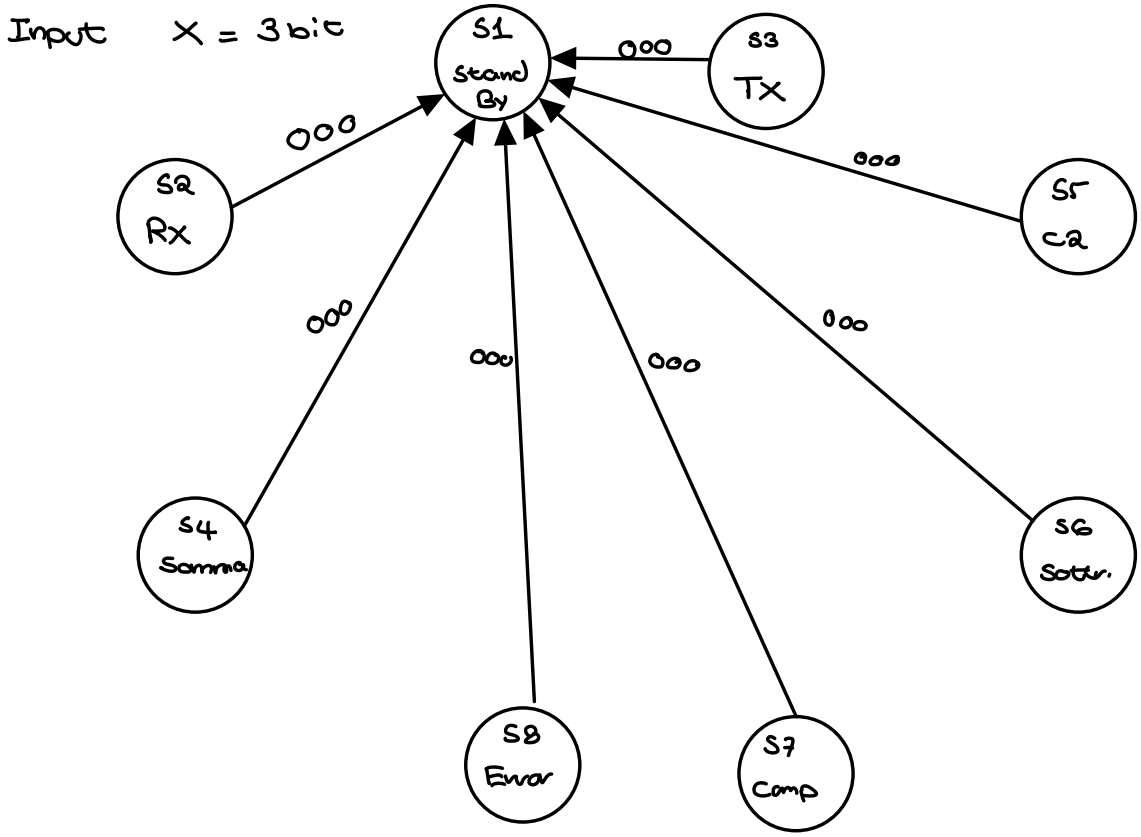
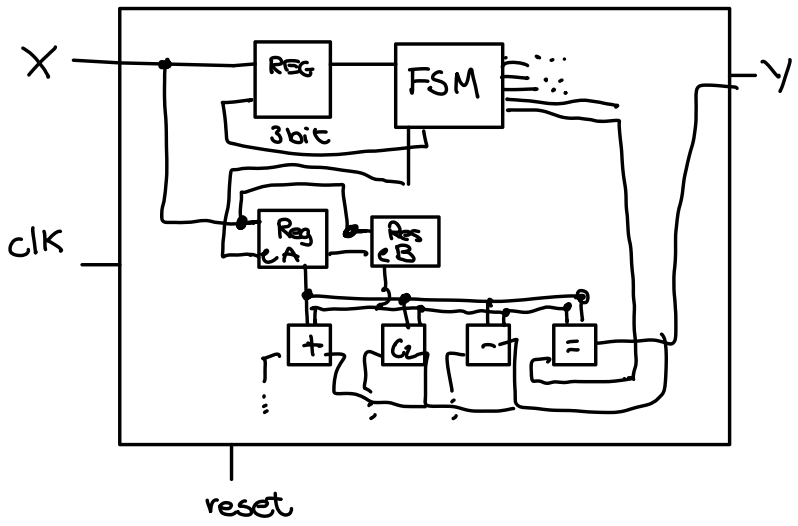

Input X = 3 bit
S1
Stand By
000
S3
TX
000
S2
RX
000
S5
c2
000
000
000
000
S4
Somma
S6
Sottr.
S8
Error
S7
Comp


X
REG
FSM
Y
3bit
clk
Reg cA
Reg cB
+
<
-
=
reset

1° Registro → D SIPO → scelto così la mia FSM riceve come parametro in input una sola variabile (X=001)

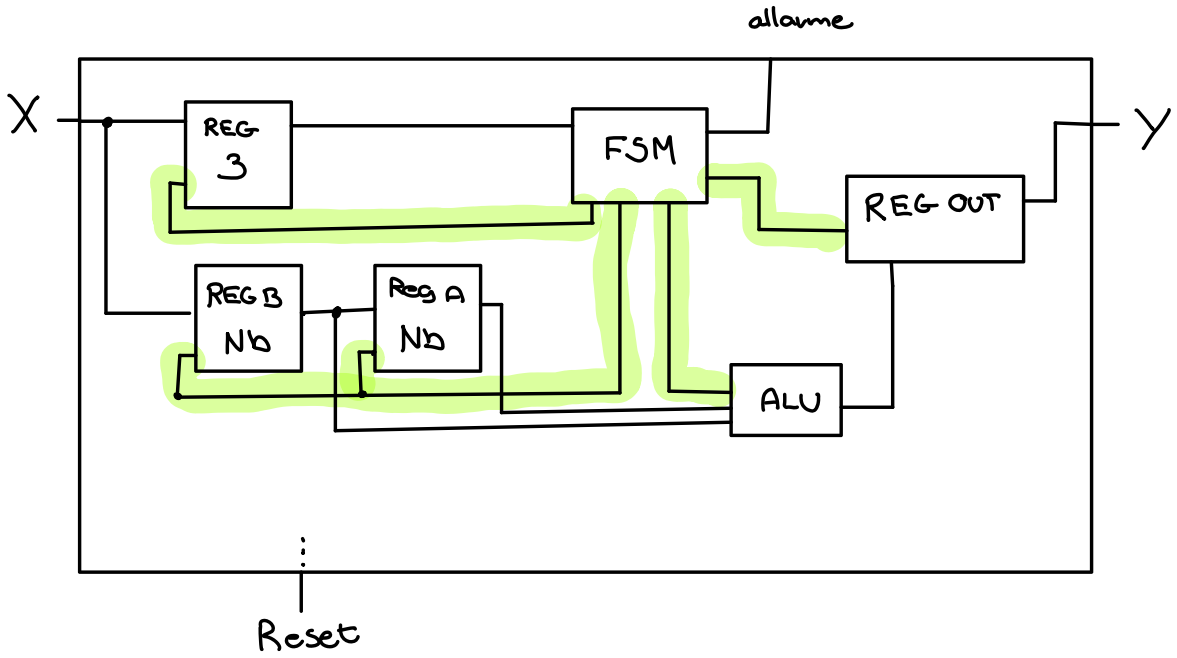
I registri sono composti da D-Flip-Flop

D : in
clk : in
enable : in
Q : out

enable?
se reset 1
enableRO 1

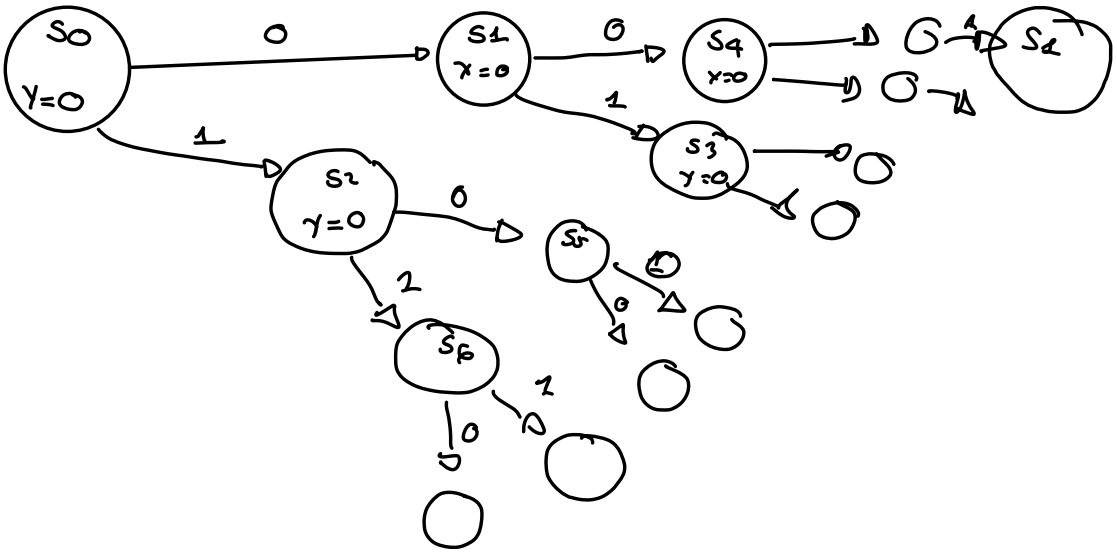
enableRX
enableTX
enable S+
enable S-
enable C2
enable EQ

3 sipo → 1 da 3 bit → X
3 sipo → 2 da N0 bits → A e B



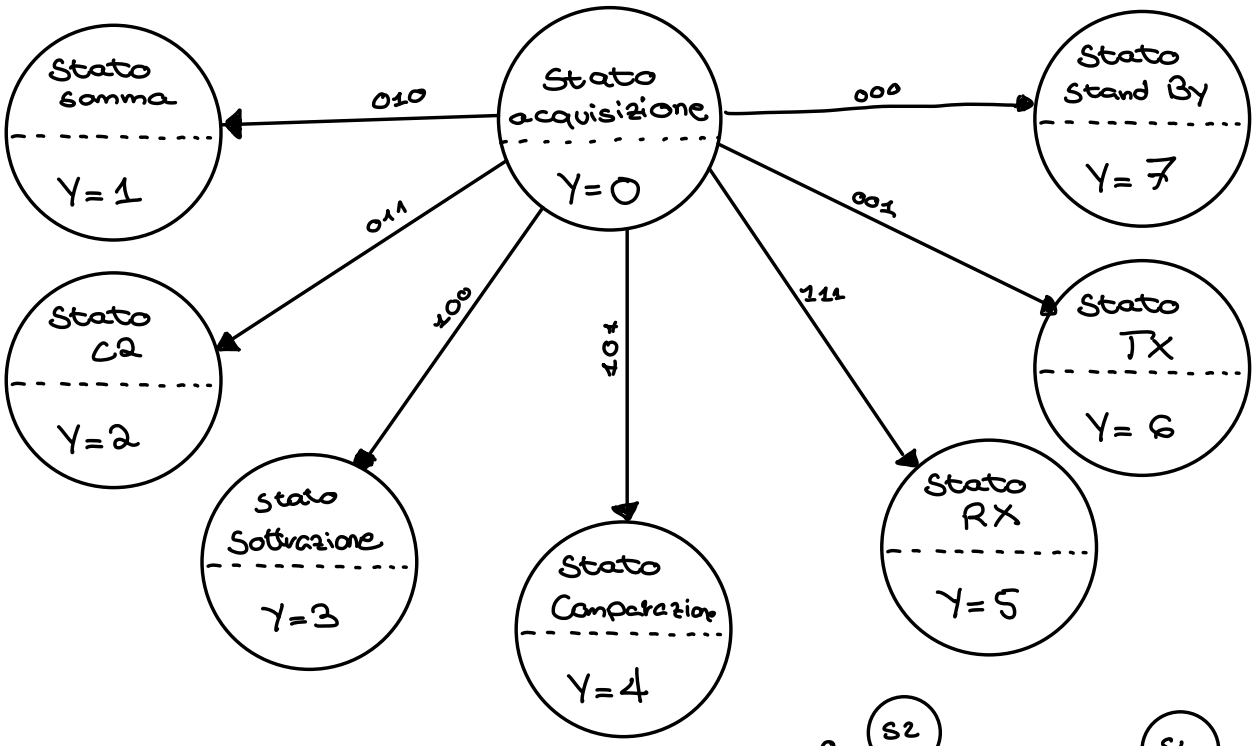
Ogni Enable é in AND con Reset

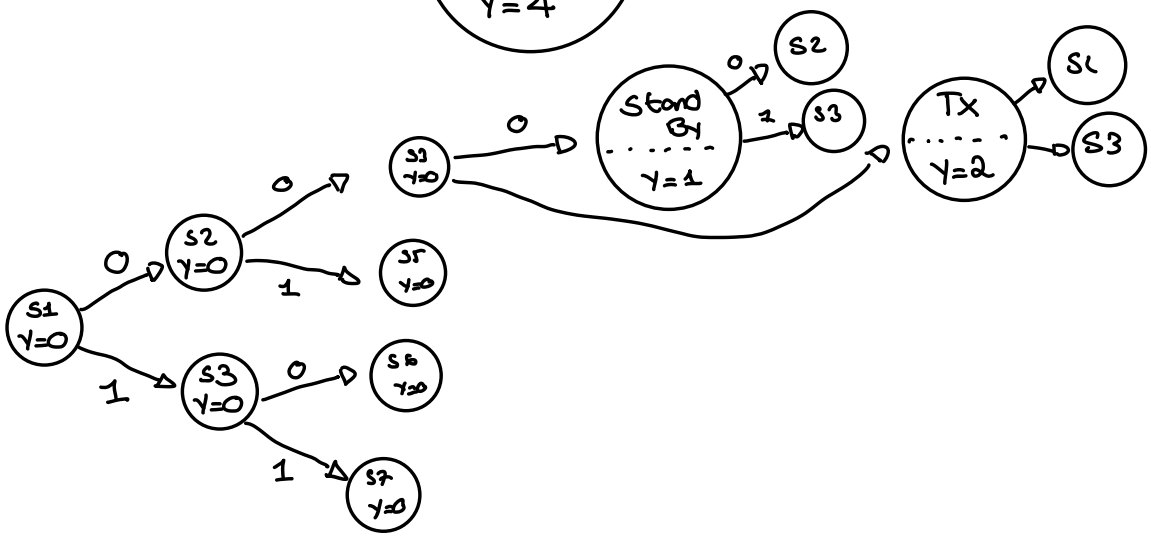
0 → enable stand by
1 → enable RX
2 → enable TX
3 → enable +
4 → enable −
5 → enable C2
6 → enable comp
7 → errore!

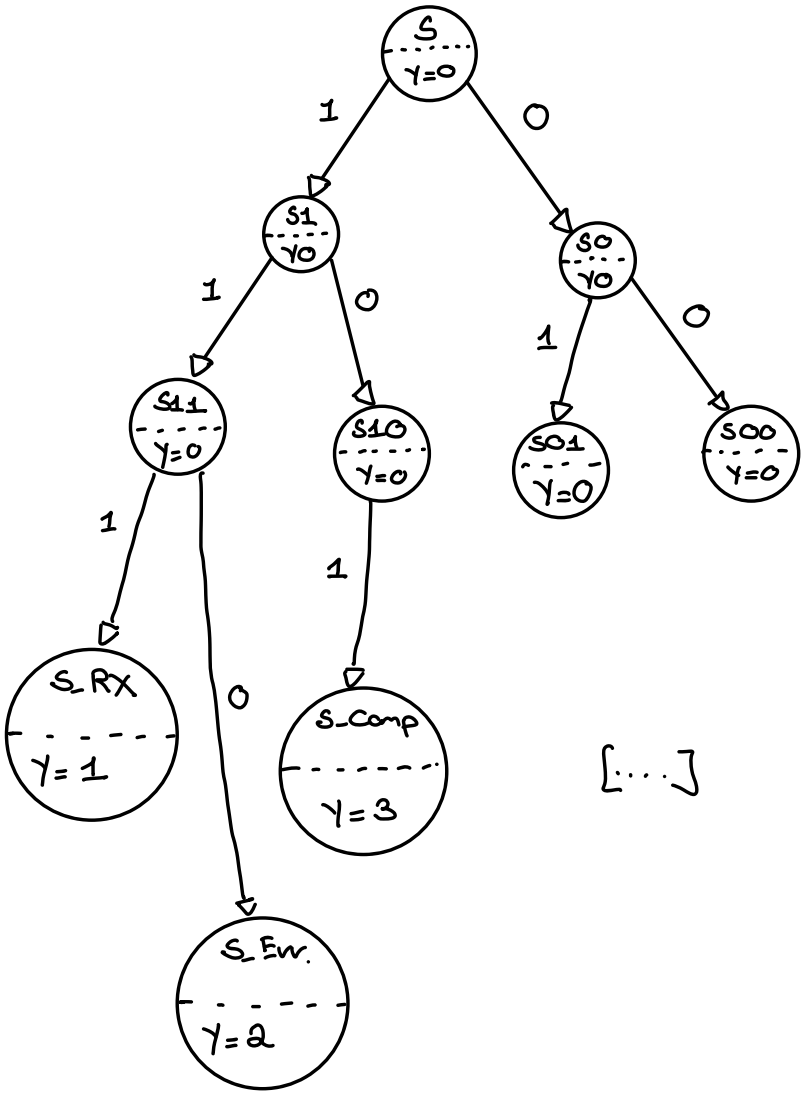


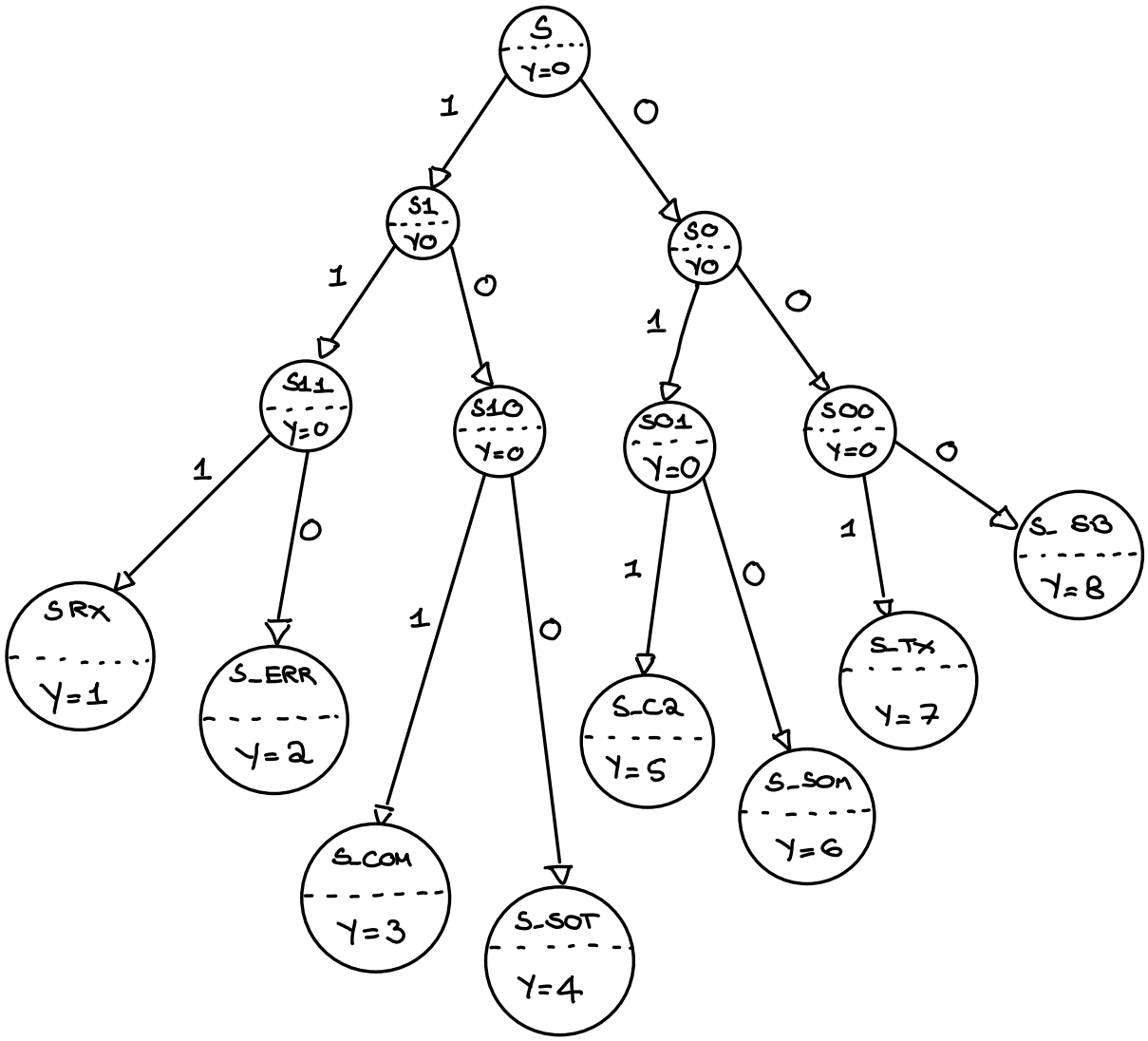
State
RX

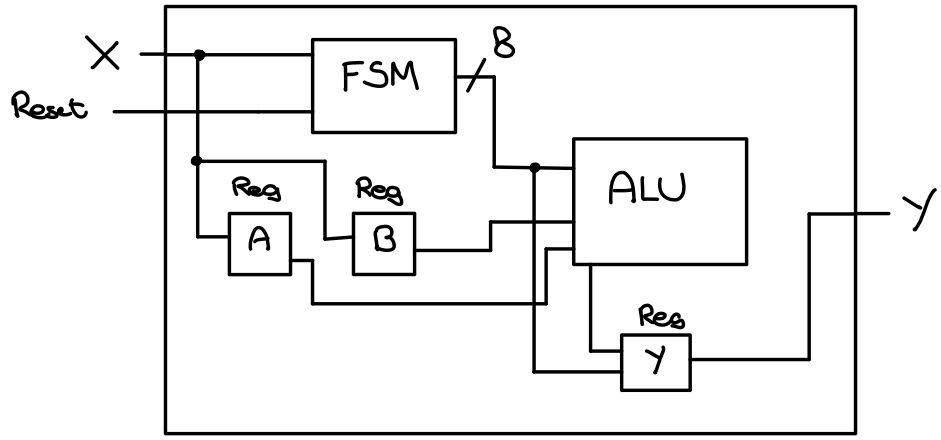
State
Tx

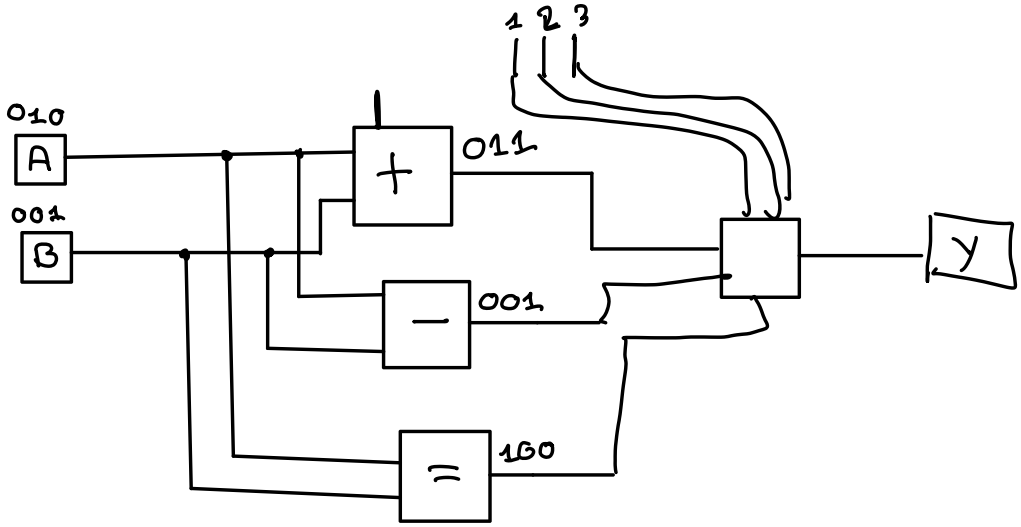

Stato somma
Y=1
010
Stato acquisizione
Y=0
000
Stato Stand By
Y=7
011
Stato C2
Y=2
100
101
111
001
Stato TX
Y=6
Stato Sottrazione
Y=3
Stato Comparazione
Y=4
Stato RX
Y=5

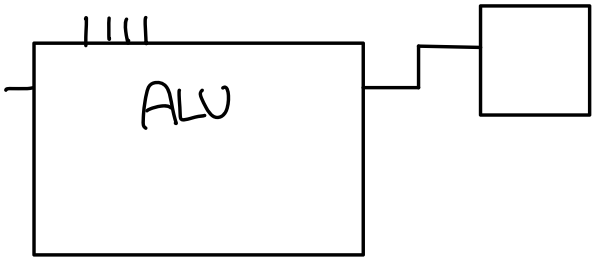

S1 Y=0
0
Stand By
Y=1
0
S2
1
S3
TX
Y=2
S1
S3
S1 Y=0
0
S2 Y=0
1
S5 Y=0
0
S3 Y=0
1
S6 Y=0
1
S7 Y=0

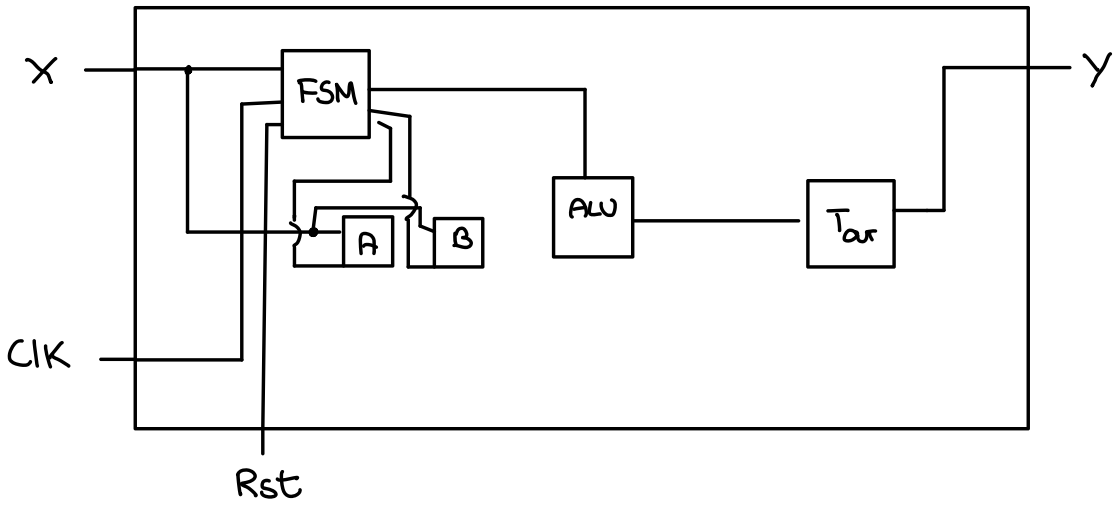

S
Y=0
1
0
S1
Y0
S0
Y0
1
0
1
0
S11
Y=0
S10
Y=0
S01
Y=0
S00
Y=0
1
1
S_RX
Y=1
0
S_Comp
Y=3
S_Err.
Y=2
[...]

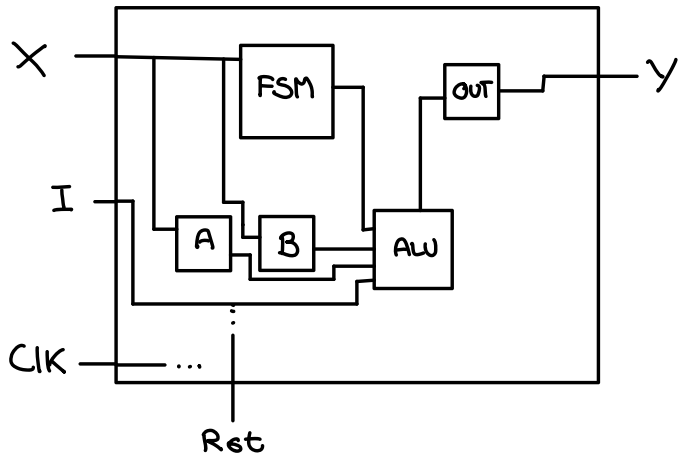

S
Y=0
1
0
S1
Y0
S0
Y0
1
0
1
0
S11
Y=0
S10
Y=0
S01
Y=0
S00
Y=0
1
0
1
0
1
0
SRX
Y=1
S_ERR
Y=2
S_COM
Y=3
S_SOT
Y=4
S_C2
Y=5
S_SOM
Y=6
S_TX
Y=7
S_SB
Y=8

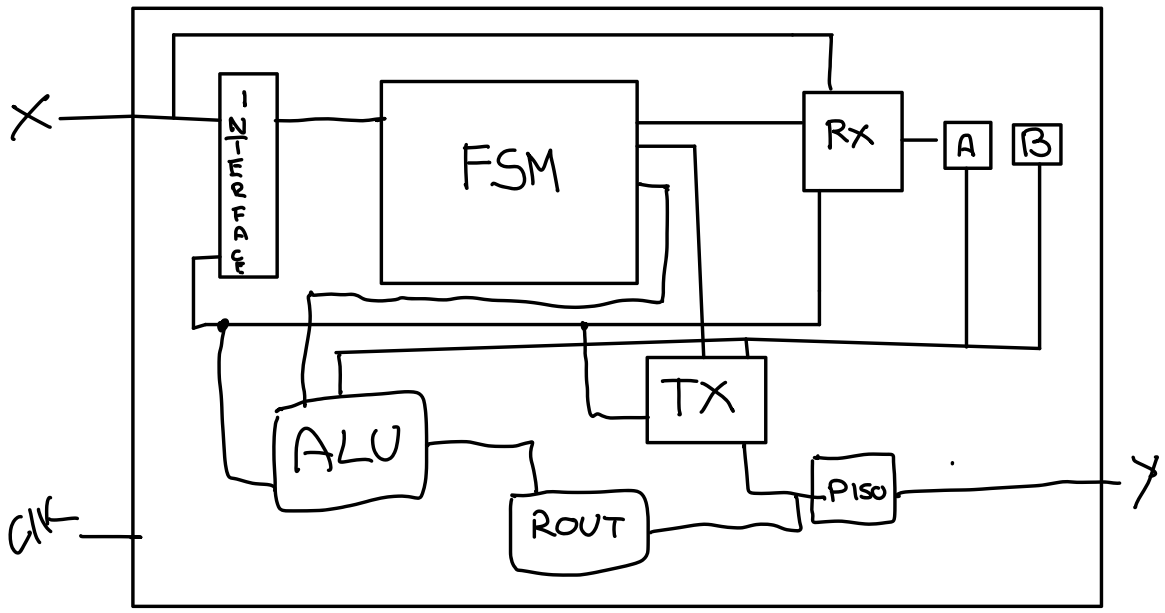

X
Reset
FSM
8
Reg
A
Reg
B
ALU
Y
Reg
Y


1 2 3
010
A
001
B
+
011
−
001
=
100
Y

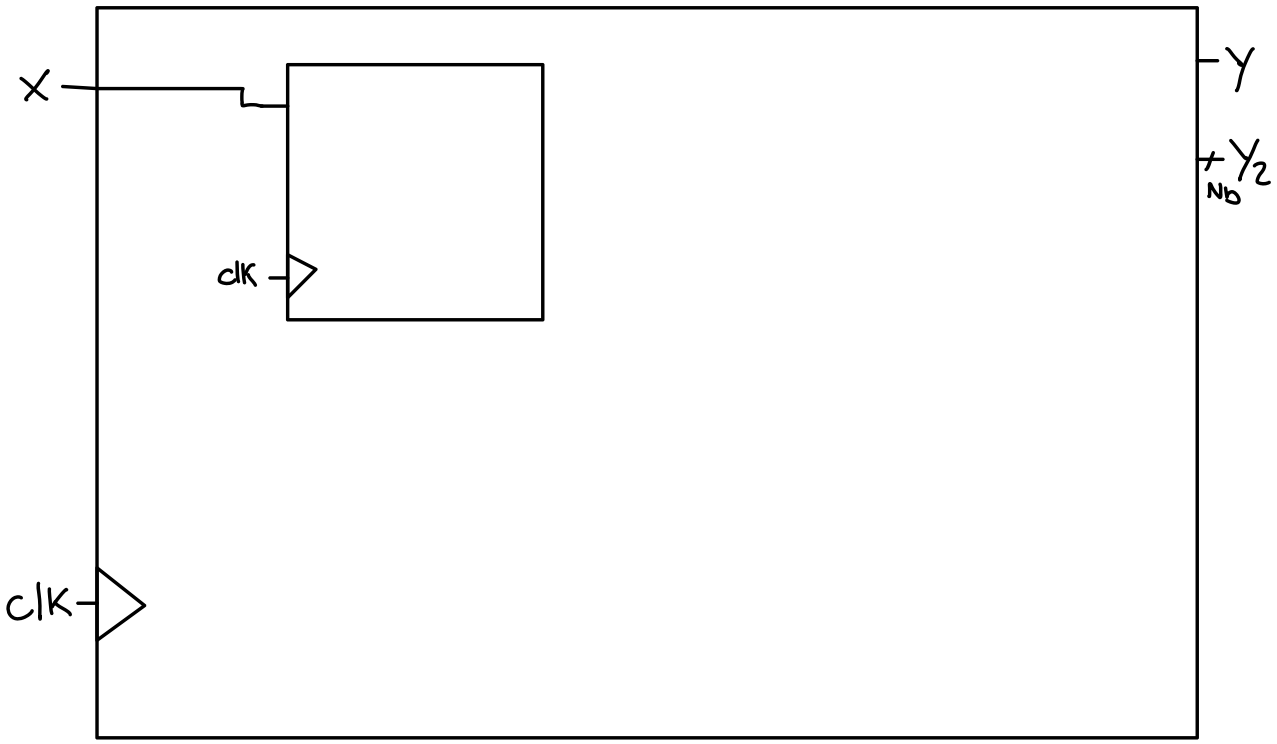

1111
ALU


X
FSM
Y
A
B
ALW
Tar
CLK
Rst


X
FSM
OUT
Y
I
A
B
ALW
CLK
...
Rst



fsm Done


X
clk
clk
Y
+
N_b
Y_2