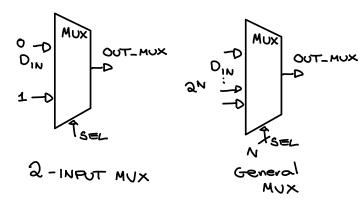
-D Multiplexer Symbol



Signal	Direction	Resolution
Div	H Z	No
SEL	IN	Logz(ND)
OUT_MUX	OUT	1

"ho quindi una word di n ingressi e scelgo quale bit leggere."

I Multiplexers selezionano uno specifico segnale di bitlbus di ingresso e farniscono tale segnale in uscita. "

PSEUDO - CODICE

if SEL=0

then

out_mux= Din(0)

ELSE OUT_mux = Din(1)

end if;

Sel e' il numero dell'
ingresso da leggere

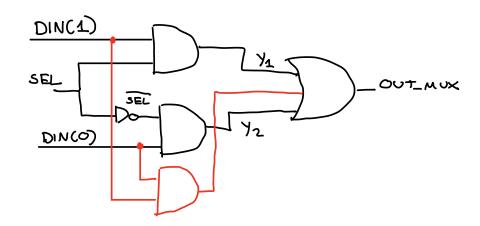
può essere formato
da più ingressi
bit per il numero

Tabella di verita

Kmap

DIN(T)	DINO	SEL	OUTN	\ <u>4×</u>	OUT_MUX	DIN(1) DINCO)
0	0	Q	0		SEL O	00 01 11 10
0	0	1	0		SEL 1	0 1 1 0
0	1	0	1			
O	7	1	0	OUT	IMUX =	
1	0	0	0		SEL . D	M(0)
1	0	1	1		55, 5	(1)
1	1	0	1 9	jabiasi in SEL	SEL .	,
1	1	1	٦.	1	DINCO)·Din(1)

Schema



MUX - 1x2

OUT_MUX = SEL. O1 + SEL DO

MUX - 2×4

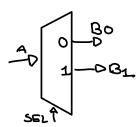
OUT_MUX = SEL(A).SEL(O).D3+SEL(A).SEL(O).D2
+SEL(1).SEL(O).D1+ SEL(1).SEL(O).D0

POSSO vicostruirlo utilizzondo 3 MUX 1x2!

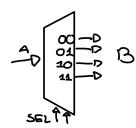
D NX2" MUX pué esseve costrito utilizzano 2N-1 1x2 MUX

-D Demultiplexer Symbol

DEMUX 2×1

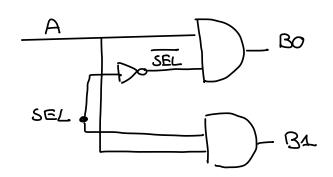


DEMUX 4×2



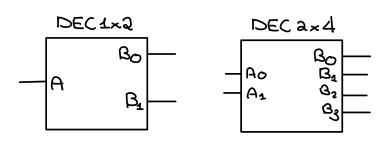
Pseudo-codice

IN	TUPIT	OUTF	TU	
A	SEL	ઉ૦	B 1	
0	0	0	×	
0	1	~	0	
1	0	1	× 、	
1	1	×	1	à non defini∕∞



Azione contravion del multiplexer.

-D Decoder



Signal	Direction	Resolution
D	H S	L092 (NO)
\mathcal{B}	٥٠٢	Nb

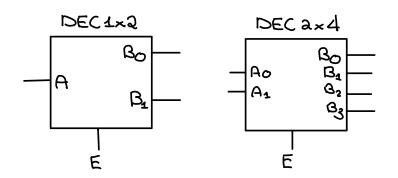
Codice per DEC1×2

if
$$A=0$$
 then $B_0=1$ $B_1=0$

_
else
Bo = 0
B1 = 1
endif;

INF	INPUT		ОИТРИТ		
A 1	A 0	В3	B2	B1	B0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

-1> Decoder con Enable

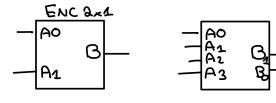


50	gnal	Direction	Resolution
	А	ZY V	Log2 (NO)
	B	٥٠٢	Nb
_	E	Ιν	1

Pseudo-code
if enable = 1 then
= al precede
else B0=0; B1=0j
end if;

INPUT			OUT	ΓPUT		
ENABLE	A 1	Α0	В3	B2	B1	B0
0	х	х	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

-D Encoder



Sig	امر	Direction	Resolution
<u></u>	+	Ιη	20
	3	Out	L092(ND)

Pseudo-code ENC 4×2

Switch A

case '001: B=X

case '01': B=0

case '10': B=1

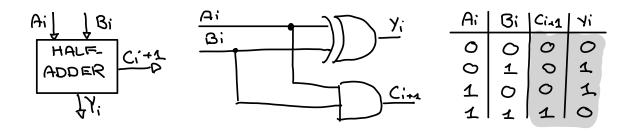
case 1111: B=x

end

INPUT				ОUТ	PUT
А3	A 2	A1	Α0	B1	В0
0	0	0	0	х	х
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

1 Contravio del Multiplexer!

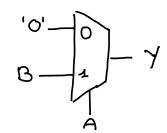
-D Half-Adder



Esercizio 1

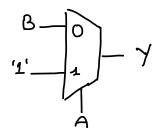
"Sintetizzare logicomente AND, OR, NAND, NOR e XOR usando 1x2-MUX e INVERTER."

-LOGIC AND



A B Y 0 0 0 0 1 0 0 1 1 1

- LOGIC OR



A	B	Υ
0	0	0
O	ュ	1
1	0	1
ュー	1	1

-LOGIC NAND

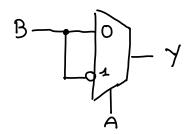
$$A = SEL$$

 $Y = \overrightarrow{A \cdot B} = \begin{cases} 1 & \text{if } SEL = '0' \\ \overrightarrow{B} & \text{if } SEL = '1' \end{cases}$

'1' —	0	~ /
B —	1	Y
'	A	

А	B	7
0	0	1
0	ィ	1
1	0	1
1	1	0

- LOGIC XOR



$$A = SEL$$

$$Y = A \oplus B = \begin{cases} B & \text{if } SEL = '0' \\ \hline O & O & O \\ \hline A & B & Y \\ \hline O & O & O \\ \hline A & B & Y \\ \hline O & O & O \\ \hline A & D & A \\ \hline A & B & Y \\ \hline O & O & O \\ \hline A & B & Y \\ \hline O & O & O \\ \hline A & D & A \\ \hline A & D & D \\ A & D & D \\ \hline A & D & D$$

- LOGIC NOR

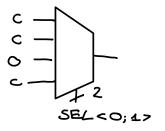
Esercizio 2

Sintetizzare con 2x4 MUX e Invertor la sequente funzione logica:

Genevic MUX-2×4

Fix SEL <1>= A SEL <0>=B

W1 puó essere scritta come



Esercizio 3

Sintetizzare con 2x4 MUX e Invertor la sequente funcione logica:

$$W_{1} = A \cdot B \cdot C + \overline{A} \overline{G} \overline{C}$$

$$SEL<0>= A$$

$$G = A$$

$$G =$$

Esercizio 4

Design un prime Number Detector (PND) usando un 3x8 Mux e INVERTERs

1) Facciamo la tabella di verita!

Int	Аз	Aa	A	Ao	4
0	0	0	0	0	0 0
1	0	0	0	1	0
a	0	0		0	1.
3	0	0	ュ	1	ヹ
4	Č	1	0	40404	0 1
1 2 3 4 5	0000000	0000 + + + + +	00440044	エ	1
6	~	,	ا ہا	0	0
		<u> </u>	7	ا ہا	4
7	0	1	7	_	.
:	:	;	;	;	
11	1	0	1	1	1
:	:	:	:	:	:
13	1	1	0	1	1
:	:	-	·	.	
•	'	,	•	. 1	'

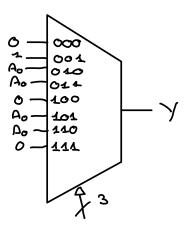
@ Scrivo la funcione y Non minimizzata

(3) Minimizziamdo

4) Tabella

Int	selection Word Code	Ω	Value
0	A3 · AZ · A1	D ₀₀ 0	0
<u>ર</u> 3	A3 A2. A1	Q001	1
4 5	A3. A2 A2	D010	Ao
•	:	:	;





SEL < 0: 27 = 4 A3 AZ A17

RICORDO

Nella mappa di K-Map il passaggio in diagonale è inutile