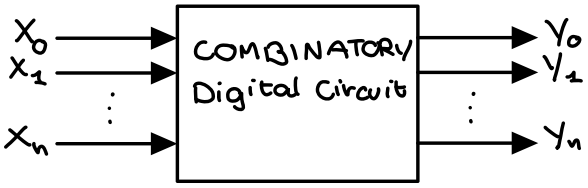
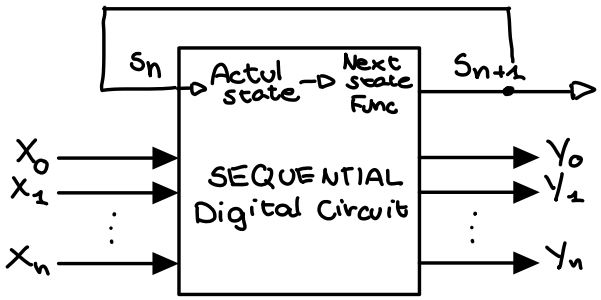
→ Sequential Digital Circuits



- Circuito combinatorio evolve i segnali di ingresso (temporalmente)
- Dimenticano gli eventi passati.
- No Memory elements



→ FSM

- Circuiti digitali sequenziali operano come una funzione di
  - segnali input (time-evolution) X
  - actual / present State (S_n)
- Output:
  - → Il risultato dei segnali digitali Y
  - the future state S_{n+1}

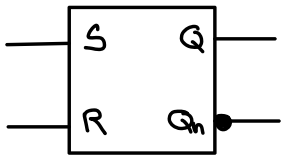
FSM → Input Signals (x), Output Signal (Y)

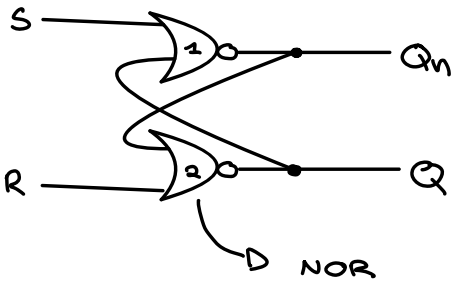
Actual State, output function (f_{OUT})
Next-State function (f_{NS})

→ Memory Elements

Set-Reset Latch (SRL)

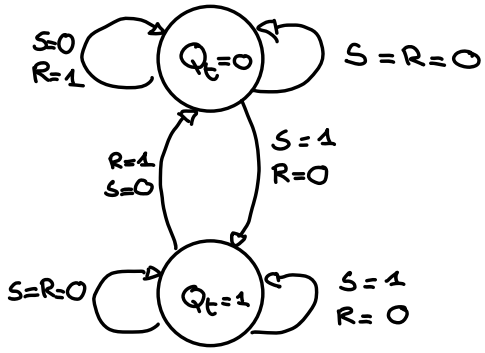
no lo stato → Q_{t-1}



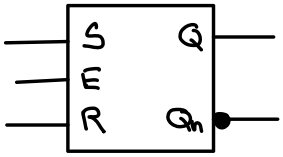


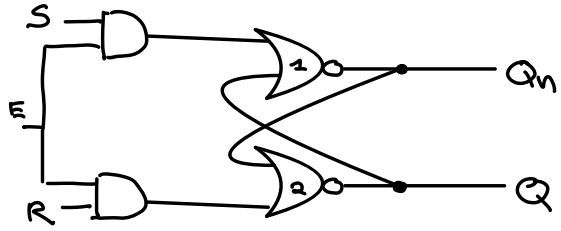
INPUT			OUTPUT	
S	R	Q_{t-1}	Q_t	Q_{nt}
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	und	und
1	1	1	und	und

diagramma a stati. →



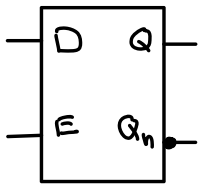
Set-Reset Latch con Enable

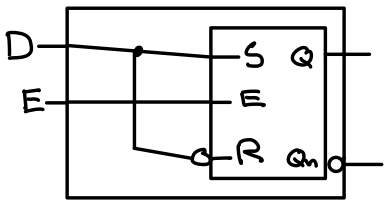




INPUT				OUTPUT	
E	S	R	Q_{t-1}	Q_t	Q_{nt}
0	x	x	0	0	1
0	x	x	1	1	0
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	und	und
1	1	1	1	und	und

DLatch Symbol con Enable





INPUT		OUTPUT	
E	D	Qt	Qnt
0	x	Qt-1	Qnt-1
0	0	0	1
0	1	1	0
1	0	0	1
1	1	1	0

Data Latch (DL) memorizza un bit specifico e opera sotto l'enable.

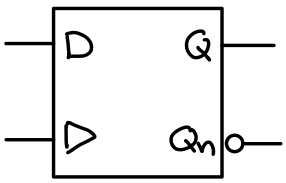
- se é 0 lo stato non cambia.
- se é a 1 posso cambiare lo stato del bit

SET = D

RESET = not(D)

⚠ Con il diagramma-tempo Q é uguale D quando Enable é alto (=1)

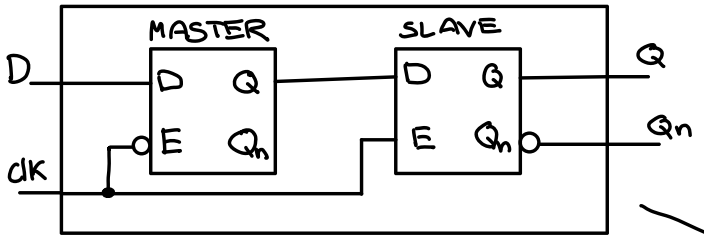
Edge-Triggered D-Flip-Flop



DFF puó essera attivato dal fronte di salita o il fronte di discesa

INPUT			OUTPUT
D	Qt-1	CIK	Qnt
0	0	↑	0
0	0	↓	0
0	1	↑	0
0	1	↓	1
1	0	↑	1
1	0	↓	0
1	1	↑	1
1	1	↓	0

Master-Slave Edge-Triggered D-Flip-Flop



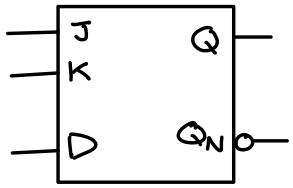
	INPUT		OUTPUT	
	D	Edge	Qt	Qnt
NO TOGGLE	0	↑	0	1
	1	↑	1	0

Il master al segnale clock invertito

sono 2 DFF in cascata

⚠ Quando il master lavora lo slave tiene l'output, quando lo slave lavora il master è spento.

JK-Flip-Flop



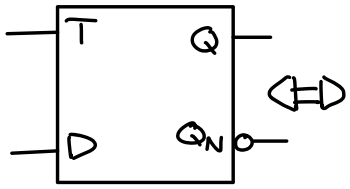
JK Flip-Flop (JK-FF) può essere attivato dal fronte di salita/discesa.

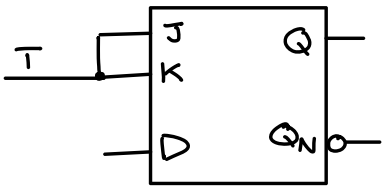
	INPUT			OUTPUT	
	J	K	Qt-1	Qt	Qnt
no toggle	0	0	0	0	1
	0	0	1	1	0
reset	0	1	0	0	1
	0	1	1	0	1
set	1	0	0	1	1
	1	0	1	1	0
toggle	1	1	0	1	0
	1	1	1	0	1

J fa il set
K fa il reset

→ se J = K = 1 allora Qt = not(Qt-1)

T-Flip-Flop - Truth Table





JK-Flip-Flop

Toggle Flip-Flop (TFF) può essere attivato con il fronte di salita o discesa

Se T=1 allora

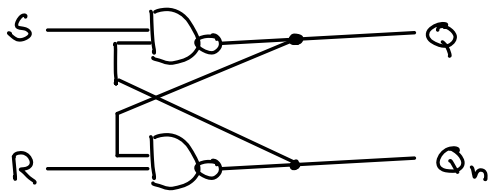
$Q_t = not(Q_{t-1})$

Se T=0 allora

$Q_t = Q_{t-1}$

Esercizi

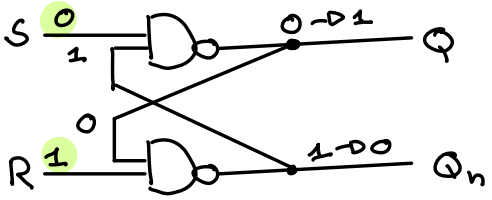
1)



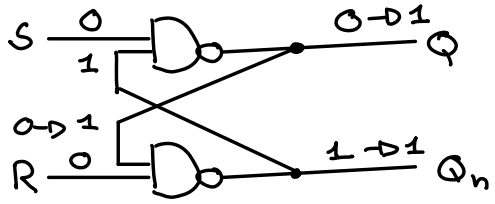
NAND port è 0 quando entrambi sono a 1

NAND		
A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

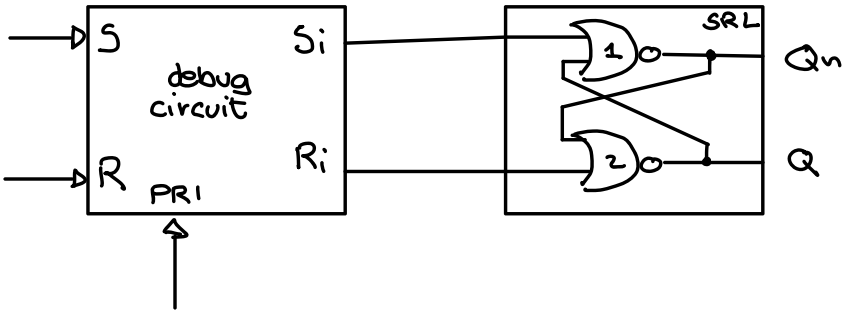
	INPUT			OUTPUT	
	S	R	Q_{t-1}	Q_t	Q_{nt}
undefined	0	0	0	X	X
	0	0	1	X	X
reset	0	1	0	1	0
	0	1	1	1	0
set	1	0	0	0	1
	1	0	1	0	1
hold	1	1	0	0	1
	1	1	1	1	0



- la condizione (S=0 e R=0) porta a due modalità operative contraddittorie



2) Design un circuito logico che ha l'obiettivo di eliminare lo stato indefinito (U) nel NOR-SRL



INPUT			OUTPUT		
S	R	PRI	Si	Ri	
0	0	0	0	0	} hold
0	0	1	0	0	
0	1	0	0	1	} reset
0	1	1	0	1	
1	0	0	1	0	} set
1	0	1	1	0	
1	1	0	0	1	} unde.
1	1	1	1	0	

Si

PRI \ SR	00	01	11	10
0	0	0	0	1
1	0	0	1	1

$S_i = S \cdot \overline{R} + \overline{PRI} \cdot S$

$R_i = R \cdot \overline{PRI} + \overline{S} \cdot R$