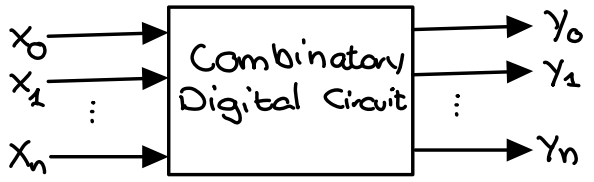
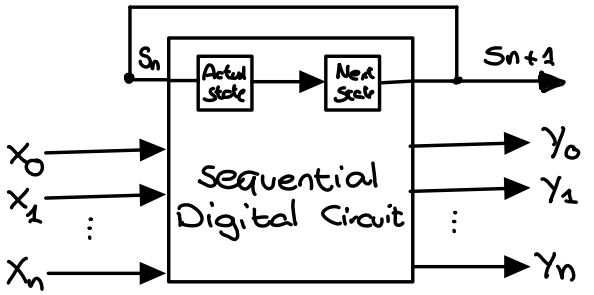
→ Finite-State-Machines (FSMs)



dato un Input elaboro e ridó un output

no memoria

dimentica di eventi passati



→ possono essere:

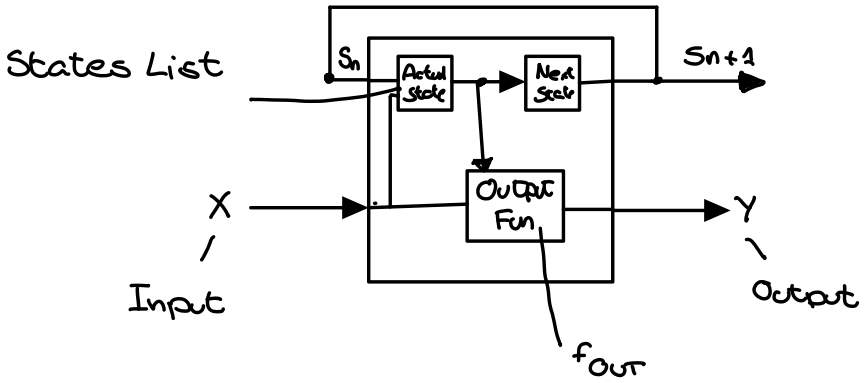
- **Sincroni** → usano un clock
- **Asincroni** → usano elementi di memoria (latches)

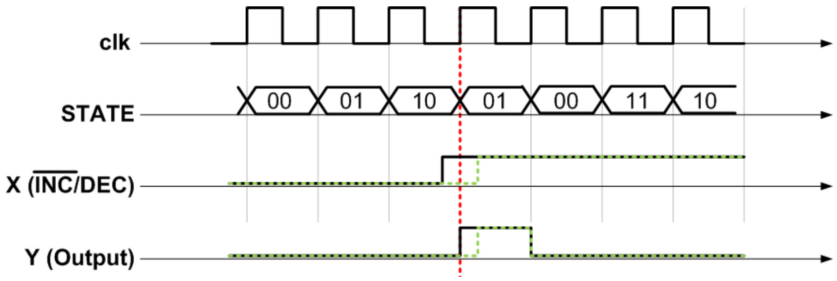
Più sicuri, più robusti!

Abbiamo:

- Segnali di Input (x)
- Segnali di Output (y)
- Lista degli stati (Actual State)
- Funzione Output (f_{out})
- Next-State Funzione (f_{NS})

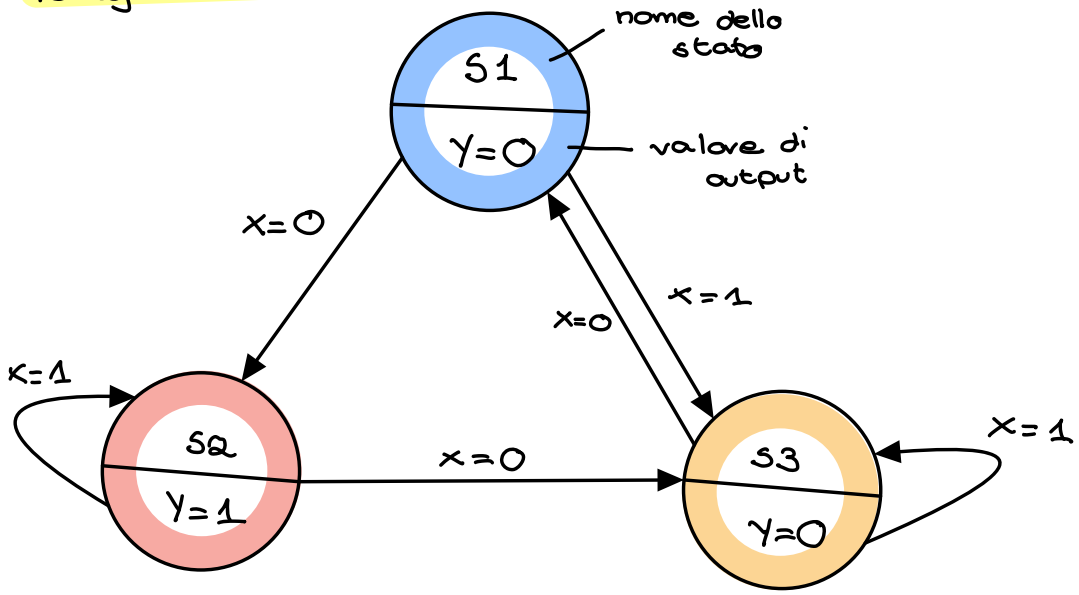
Mealy FSMs





Output Logic Function: $Y = f_{OUT}(S_n, X) = \overline{S_n(1)} \cdot S_n(0) \cdot X$

Diagrammi a stati



ACTUAL STATE S_n			INPUT	NEXT STATE S_{n+1}			OUTPUT
	$S_n(1)$	$S_n(0)$	X		$S_{n+1}(1)$	$S_{n+1}(0)$	Y
S1	0	0	0	S2	0	1	1
S1	0	0	1	S3	1	1	0
S2	0	1	0	S3	1	1	0
S2	0	1	1	S2	0	1	1
S3	1	1	0	S1	0	0	0
S3	1	1	1	S3	1	1	0

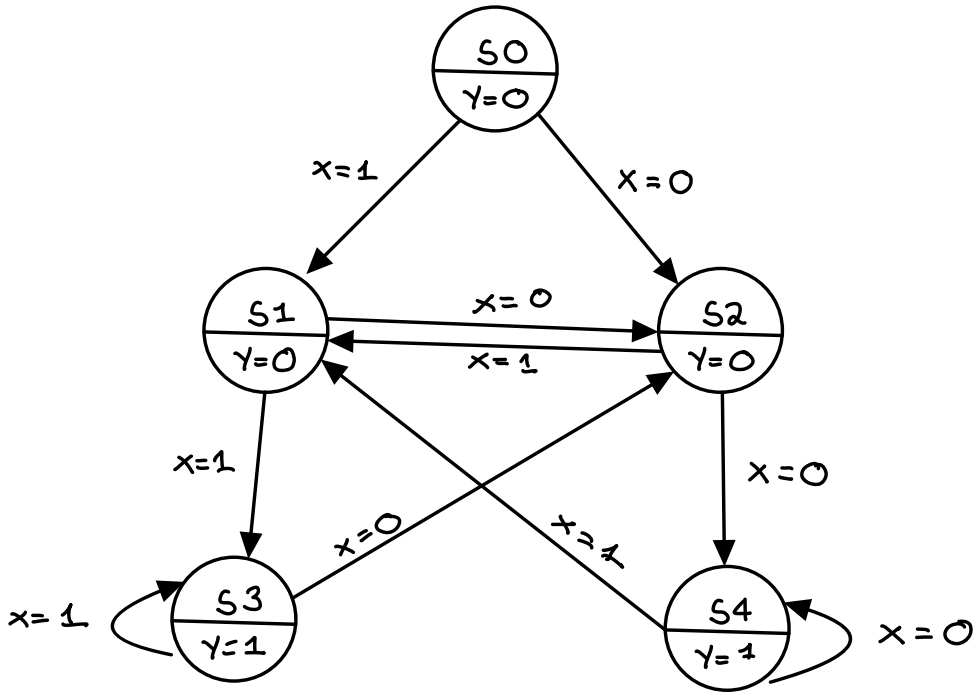
Esercizi

1) Design a logic circuit able to detect two equal consecutive bits. In case of positive event, the Y output signal is 1, otherwise is 0. The circuit receives one single bit (X) and uses one single clock. Implement by Moore-FSM.

FSM Design Procedure

- Definive
  - Segnali di Input (X)
  - Segnali di Output (Y)
  - Lista degli Stati
- State-Diagram
  - Rappresentazione grafica di tutti gli stati e transizioni
- State-Table
  - Una tabella con due colonne S_n e S_{n+1}, X e Y.
- Next-State Function f_{NS}
  - $S_{n+1} = f_{NS}(X, S_n)$

State - Diagram



State - Table

ACTUAL STATES				INPUT	NEXT STATES				OUTPUT
State Name	$S_n(2)$	$S_n(1)$	$S_n(0)$	X	State Name	$S_{n+1}(2)$	$S_{n+1}(1)$	$S_{n+1}(0)$	Y
S0	0	0	0	0	S2	0	1	0	0
S0	0	0	0	1	S1	0	0	1	0
S1	0	0	1	0	S2	0	1	0	0
S1	0	0	1	1	S3	0	1	1	1
S2	0	1	0	0	S4	1	0	0	1
S2	0	1	0	1	S1	0	0	1	0
S3	0	1	1	0	S2	0	1	0	0
S3	0	1	1	1	S3	0	1	1	1
S4	1	0	0	0	S4	1	0	0	1
S4	1	0	0	1	S1	0	0	1	0

Next-State Function f_{NS}

$$S_{n+1} = f_{NS}(X, S_n)$$

$S_{n+1}(2)$		$S_n(2)\,S_n(1)$ 00	01	11	10
$S_n(0)X$	00	0	0	x	0
	01	0	1	x	1
	11	0	0	x	x
	10	0	0	x	x

$$S_{n+1}(2) = S_n(1)\cdot\overline{S_n(0)}\cdot X + S_n(2)\cdot X$$

$$S_{n+1}(1) = S_n(0) + \overline{S_n(2)}\cdot\overline{S_n(1)}\cdot X$$

$$S_{n+1}(0) = \bar{X}$$

$$Y = S_n(2) + S_n(1)\cdot S_n(0)$$