6. Appendix: Customer Register Map

Addr	RegName	Bits	Label	Default (Hex)	Access	Description
0x0D	LOAD_CFG	5:0	RESERVED	0x0	RW	Reserved
		6	HEAVY_LOAD_HYS	0x0	RW	Light load=Heavy_Load_Set - Heavy_Load_Hys 00:30mA 01:50mA
		7	DUMMY_LOAD_HYS	0x0	RW	ASK_dummy_load = No_ASK_dummy_load + Dummy_Load_Hys 00:10mA 01:20mA
0x0E	FUN_EN&CFG	0	VBAT_TRK_EN	0x0	RW	If AP set this bit to "1", disable output tracking VBAT function, set this bit to "0", enable output tracking VBAT function
		1	RVS_EN	0x0	RW	If AP set this bit to "1", disable external resistance to set Vout function, set this bit to "0", enable external resistance to set Vout function
		2	INV_MODULATION_EN	0x0	RW	If AP set this bit to "0", enable inv_modulation function, set this bit to "1", disable inv_modulation function
		3	RESERVED	0x0	RW	Reserved
		5:4	VRECT_OVP1_TH	0x0	RW	The limit of VRECT_OVP1 protection. 00:10V 01:11V 10:12V 11:13V
		7:6	VRECT_OVP2_TH	0x1	RW	The limit of VRECT_OVP2 protection. 00:14V 01:15V 10:16V 11:13V
0x10	CHIP_ID_L	7:0	CHIP_ID_L	0x20	RO	Chip ID low byte
0x11	CHIP_ID_H	7:0	CHIP_ID_H	0x45	RO	Chip ID high byte

Addr	RegName	Bits	Label	Default (Hex)	Access	Description
0x12	CHIP_REV	7:0	CHIP_REV	0x48	RO	Chip revision of RxIC. 0x40 - A0; 0x48 - A1; etc.
0x13	QI VERSION	3:0	MINOR_VERSION_B0	0x3	RW	The format of the message contained in an Identification Packet.
		7:4	MAJOR_VERSION_B0	0x1	RW	The format of the message contained in an Identification Packet.
0x14	MFG_CODE_B2	7:0	MFG_CODE_B2	0x18	RW	Power Receiver Manufacturer Codes, Wireless Power Consortium
0x15	MFG_CODE_B1	7:0	MFG_CODE_B1	0x00	RW	Power Receiver Manufacturer Codes, Wireless Power Consortium
0x16	STATUS	0	I2C_READY	0x0	RO	I2C_Ready changes to "1" when work in I2C connection mode, will not set to '0'.
		1	STAT_VOUT	0x0	RO	stat_Vout changes to "1" when mLDO turn on , change to '0' when mLDO turn off
		2	VRECT_OVP1	0x0	RO	Set to 1 when trigger Vrect_OVP1,
		3	VRECT_OVP2	0x0	RO	Set to 1 when trigger Vrect_OVP2,
		4	OCP	0x0	RO	Set to 1 when trigger OCP
		5	OTP	0x0	RO	Set to 1 when trigger OTP,
		6	TX_DATA RECEIVED	0x0	RO	Set to 1 when received Tx FSK packet,
		7	AC_MISSING	0x0	RO	If AC signal not detected during Rx mode, set this bit to 1, otherwise, set it to '0'.
0x17	INT	0	I2C_READY	0x0	RO	1: indicates a pending interrupt for work in I2C connection mode. Reading it will clear the bit.
		1	STAT_VOUT	0x0	RO	1: indicates a pending interrupt for mldo state has been changed. Reading it will clear the bit.

Addr	RegName	Bits	Label	Default (Hex)	Access	Description
		2	VRECT_OVP1	0x0	RO	1: indicates a pending interrupt for Vrect OVP1 event. Reading it will clear the bit.
		3	VRECT_OVP2	0x0	RO	1: indicates a pending interrupt for Vrect OVP2 event. Reading it will clear the bit.
		4	OCP	0x0	RO	1: indicates a pending interrupt for OCP event. Reading it will clear the bit.
		5	OTP	0x0	RO	1: indicates a pending interrupt for OTP event. Reading it will clear the bit.
		6	TX_DATA RECEIVED	0x0	RO	1: indicates a pending interrupt for received fsk packet from Tx. Reading it will clear the bit.
		7	AC_MISSING	0x0	RO	1: indicates a pending interrupt for AC missing event. Reading it will clear the bit.
0x18	CMD&FUNC_EN	0	SEND_DATA_EN	0x0	RW	If AP set this bit to "1", IC send PPP after next CEP or RPP packet, and IC sets this bit to "0".
		1	LDO_Toggle_EN	0x0	RW	If AP set this bit to "1", IC toggles LDO state and IC sets this bit to "0".
		2	DUMMY_LOAD_EN	0x1	RW	If AP set this bit to "0", do not add dummy load in light load no matter non-packet and packet, set this bit to "1", add dummy load in light load
		3	CE_LARGE_EN	0x0	RW	If AP set this bit to "1", Define CE=0 at (Vrect_ADC-Vrect_target) between (+75mV,-40mV)
		5:4	SYNC_ON_SEL	0x0	RW	SR mode control in light load mode 00:full sync+1/4 LS Ron 01:HS half-sync 10: LS half-sync 11: full sync

Addr	RegName	Bits	Label	Default (Hex)	Access	Description
		6	FASTOFF_EN	0x1	RW	If AP set this bit to "1", enable fastoff protect function, set this bit to "0", disable fastoff protect function.
		7	RESERVED	0x0	RO	Reserved
0x19	VOUT_SET_L	7:0	VOUT_SET_L	0x88	RW	Main LDO Vout set value low byte
0x1A	VOUT_SET_H	7:0	VOUT_SET_H	0x13	RW	Main LDO Vout set value high byte
0x1B	THRESHOLD	1:0	ILIM_SET	0x0	RW	The limit of over current protection. 00:1.4A 01:1.1A 10:0.8A 11:0.5A
		3:2	CE_LIMIT	0x0	RW	The limit of maximum of control error 00:55 01:35 10:25 11:15
		5:4	VBAT	0x0	RW	The minimum limit of Vbat voltage when using battery tracking function 00:3.5V 01:3.4V 10:3.2V 11:3.6V
		6	MCU_RESET	0x0	RW	CPS4520 can be reset by AP
		7	RESERVED	0x0	RO	Reserved
0x1C	CONFIG	3:0	DUMMY_LOAD_SET	0x3	RW	Dummy load at light load. 0000:0mA 0001:5mA 0010:10mA 0011:15mA 0100:20mA 0101:25mA 0110:30mA 0111:35mA 1000:40mA

Addr	RegName	Bits	Label	Default (Hex)	Access	Description
						1001:45mA 1010:50mA
		7:4	VBAT_DELTA	0x2	RW	The difference between Vout and the VBAT Pin voltage. 0000:100mV 0001:200mV 0010:300mV 0011:400mV 0100:500mV 0101:600mV
0x1D	HEAVY_LOAD_SET	7:0	HEAVY_LOAD_SET	0x78	RW	Heavy Load: Iout value for SR mode control and dummy load setting. Unit: mA , LSB:1mA. default:120mA
0x1E	DROP_MIN	7:0	DROP_MIN	0x50	RW	Vrect and Vout minimum voltage difference Setting default:80mV Unit: 1mV Range: 1~255
0x1F	DROP_MAX_L	7:0	DROP_MAX_L	0x20	RW	Vrect and Vout maximum voltage difference Setting default:800mV Unit: 1mV Range: 1~2000
0x20	DROP_MAX_H	7:0	DROP_MAX_H	0x03	RW	Vrect and Vout maximum voltage difference Setting Unit: 1mV Range: 1~2000
0x21	DROP_MIN_CUR	7:0	DROP_MIN_CUR	0x78	RW	DROP_MIN current node set default:120mA Unit: 1mA Range: 1~255

Addr	RegName	Bits	Label	Default (Hex)	Access	Description
0x22	DROP_MAX_CUR	7:0	DROP_MAX_CUR	0x5A	RW	DROP_MAX current node set default:90mA Unit: 1mA Range: 1~255
0x23	FOD_GAIN	7:0	FOD_GAIN	0x00	RW	FOD adjustable parameter - gain. Unit: 1, LSB:0.01. Range: 1~255
0x24	FOD_OFFESET1	7:0	FOD_OFFESET1	0x00	RW	FOD adjustable parameter in heavy load - Int8_t, offset. Unit: mW, LSB:20mW. Range: -128~127
0x25	FOD_OFFESET2	7:0	FOD_OFFESET2	0x00	RW	FOD adjustable parameter in light load - Int8_t, offset. Unit: mW, LSB:20mW. Range: -128~127
0x26	ADC_VRECT_L	7:0	ADC_VRECT_L	0x00	RO	Current Vrect ADC value, low byte. Unit: mV, LSB:1mV.
0x27	ADC_VRECT_H	7:0	ADC_VRECT_H	0x00	RO	Current Vrect ADC value, high byte
0x28	ADC_IOUT_L	7:0	ADC_IOUT_L	0x00	RO	Current MLDO Iout ADC value, low byte. Unit: mA, LSB:1mA.
0x29	ADC_IOUT_H	7:0	ADC_IOUT_H	0x00	RO	Current MLDO Iout ADC value, high byte
0x2A	ADC_VOUT_L	7:0	ADC_VOUT_L	0x00	RO	Current MLDO Vout ADC value, low byte. Unit: mV, LSB:1mV.
0x2B	ADC_VOUT_H	7:0	ADC_VOUT_H	0x00	RO	Current MLDO Vout ADC value, high byte
0x2C	ADC_VBAT_L	7:0	ADC_VBAT_L	0x00	RO	Current Vbat ADC value, low byte. Unit: mV, LSB:1mV.
0x2D	ADC_VBAT_H	7:0	ADC_VBAT_H	0x00	RO	Current Vbat ADC value, high byte
0x2E	ADC_DIE_TEMP	7:0	ADC_DIE_TEMP	0x00	RO	Die temperature from ADC sample. Unit: 1°C Range: -128~127
0x2F	ADC_ FOD_GAIN	7:0	ADC_GAIN	0x00	RO	Configure the gain of FOD with internal 20uA going through the GAIN pin during start up. LSB:0.01.

Addr	RegName	Bits	Label	Default (Hex)	Access	Description
0x30	ADC_ FOD_OFFSET1	7:0	ADC_ FOD_OFFSET1	0x00	RO	Configure the offset of FOD with internal 20uA going through the OS1 pin during start up. LSB:20mW
0x31	ADC_ FOD_OFFSET2	7:0	ADC_ FOD_OFFSET2	0x00	RO	Configure the offset of FOD with internal 20uA going through the nINT/OS2 pin during start up. LSB:20mW
0x32	ADC_HEAVY_LOAD _SET	7:0	ADC_HEAVY_LOAD_SET	0x00	RO	Configure the heavy load with internal 20uA going through the SCL/HL_Load_set pin during start up.LSB:8mV
0x33	ADC_DUMMY_LOA D_SET	7:0	ADC_DUMMY_LOAD_SET	0x00	RO	Configure the dummy load with internal 20uA going through the SDA/Dummy_Load_set pin during start up.LSB:8mV
0x34	ADC_VS_VBAT_DE LTA	7:0	ADC_VS_VBAT_DELTA	0x00	RO	Configure the Vout set or the headroom between Vout and Vbat with internal 20uA going through the VS/VBAT_Delta pin.LSB:8mV
0x35	TARGET_VRECT_L	7:0	TARGET_VRECT_L	0x00	RO	Target of VRECT voltage, low byte. Unit: mV, LSB:1mV.
0x36	TARGET_VRECT_H	7:0	TARGET_VRECT_H	0x00	RO	Target of VRECT voltage, high byte
0x37	PPP_HEADER	7:0	PPP_HEADER	0x00	RW	The implementation allows up to five data bytes to be include in the PPP(AP of RX send to AP of Tx)
0x38	PPP_DATA0	7:0	PPP_DATA0	0x00	RW	First data byte of the proprietary packet
0x39	PPP_DATA1	7:0	PPP_DATA1	0x00	RW	Second data byte of the proprietary packet
0x3A	PPP_DATA2	7:0	PPP_DATA2	0x00	RW	Third data byte of the proprietary packet
0x3B	PPP_DATA3	7:0	PPP_DATA3	0x00	RW	Forth data byte of the proprietary packet
0x3C	PPP_DATA4	7:0	PPP_DATA4	0x00	RW	Fifth data byte of the proprietary packet

Addr	RegName	Bits	Label	Default (Hex)	Access	Description
0x3D	BC_HEADER	7:0	BC_HEADER	0x00	RO	Header of back channel packet(AP of Tx send to AP of Rx)
0x3E	BC_DATA0	7:0	BC_DATA0	0x00	RO	First data byte of the back channel packet
0x3F	BC_DATA1	7:0	BC_DATA1	0x00	RO	Second data byte of the back channel packet
0x40	BC_DATA2	7:0	BC_DATA2	0x00	RO	Third data byte of the back channel packet
0x41	BC_DATA3	7:0	BC_DATA3	0x00	RO	Forth data byte of the back channel packet
0x42	BC_DATA4	7:0	BC_DATA4	0x00	RO	Fifth data byte of the back channel packet
0x45	FSK_BIT_LOTH	7:0	FSK_BIT_LOTH	0x07	RW	FSK bit loth for different FSK depth
0x47	FSK_POLARITY/DEPTH	1:0	RESERVED	0x0	RO	Reserved
		2	FSK_POLARITY	0x0	RW	FSK_polarity 0:Positive 1:Negative
		4:3	FSK_DEPTH	0x0	RW	FSK_depth 00:0 01:1 10:2 11:3
		7:5	RESERVED	0x0	RO	Reserved
0x48	FREQ_L	7:0	FREQ_L	0x00	RO	Rx operation frequency ={freq_h, freq_l}/10 , unit kHz
0x49	FREQ_H	4:0	FREQ_H	0x0	RO	Rx operation frequency ={freq_h, freq_l}/10 , unit kHz
		7:5	RESERVED	0x0	RO	Reserved
0x4A	GENERAL_CTRL	2:0	RESERVED	0x0	RO	Reserved
		4:3	CLAMP_TH	0x0	RW	The limit of CLAMP protection. 00: 50mA 01: fully on 10: 80mA 11: 30mA
		7:5	RESERVED	0x0	RO	Reserved
0x5C	IC_WORK_MODE	4:0	RESERVED	0x0	RO	Reserved
		5	IC_WORK_MODE	0x0	RO	IC work mode 1: I2C mode

Addr	RegName	Bits	Label	Default (Hex)	Access	Description
						0: Resistor configure mode
		7:6	RESERVED	0x0	RO	Reserved
0x61	SSP_VALUE	7:0	SSP_VALUE	0x00	RO	Signal strength packet value
0x62	CEP_VALUE	7:0	CEP_VALUE	0x00	RO	Control error packet value
0x63	RPP_VALUE	7:0	RPP_VALUE	0x00	RO	8-bit received power packet value