5W Highly Integrated Wireless Power Receiver

Descriptions

CPS4520 is a highly integrated wireless charging power receiver IC. It supports high efficiency AC-DC voltage regulation, receiver-to-transmitter communication, I2C interface for communication with MCU, as well as reliable over-voltage / current / temperature protection schemes. Junction temperature sensor is integrated for temperature sense and compensation.

It includes a full-bridge synchronized rectifier, ultra-low dropout linear regulator, communication modulator, a multi-channel 10-bit ADC, FSM and on-chip E-fuse.

CPS4520 is available in a QFN-20, 3mm x 3mm package. This product is rated over an operating temperature range of -40°C to 85°C.

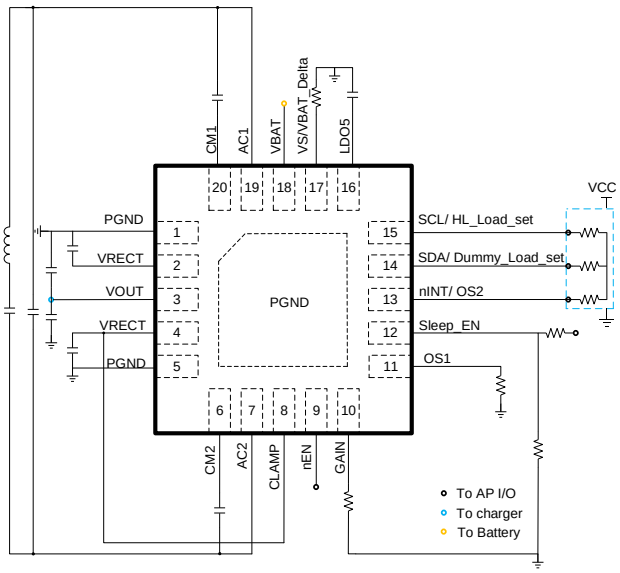
Features

- WPC Qi 1.3 compliant wireless power receiver
- Delivers up to 5W continuous output power
- Integrated fully synchronous rectifier with low RDS(on) FET
- Ultra-low dropout linear (MLDO) regulator with programmable output voltage with 20mV step
- Programmable FOD parameter gain and offset
- 10-bit SAR ADC
- Support I2C interface for system configuration
- nINT output for interrupt indication
- Over voltage/current protection
- Thermal shutdown
- Small size with QFN-20 3mm x 3mm
- RoHS，Halogen-Free and Lead-Free Compliant

Applications

- Mobile accessories
- TWS case
- Wearable Device

Figure 1: Typical Application Diagram



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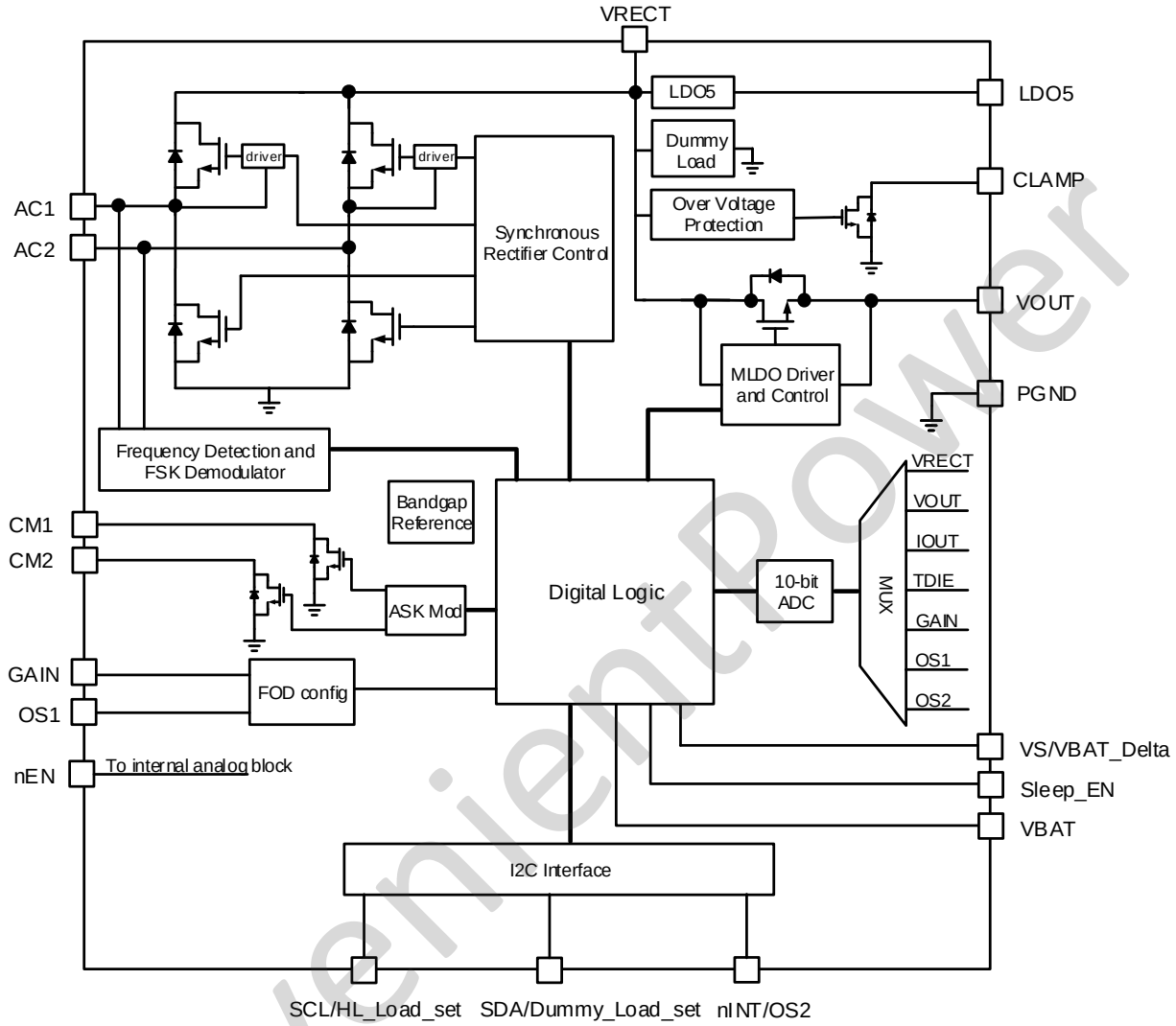


Figure **2: Block Diagram**

2. Pin Assignment

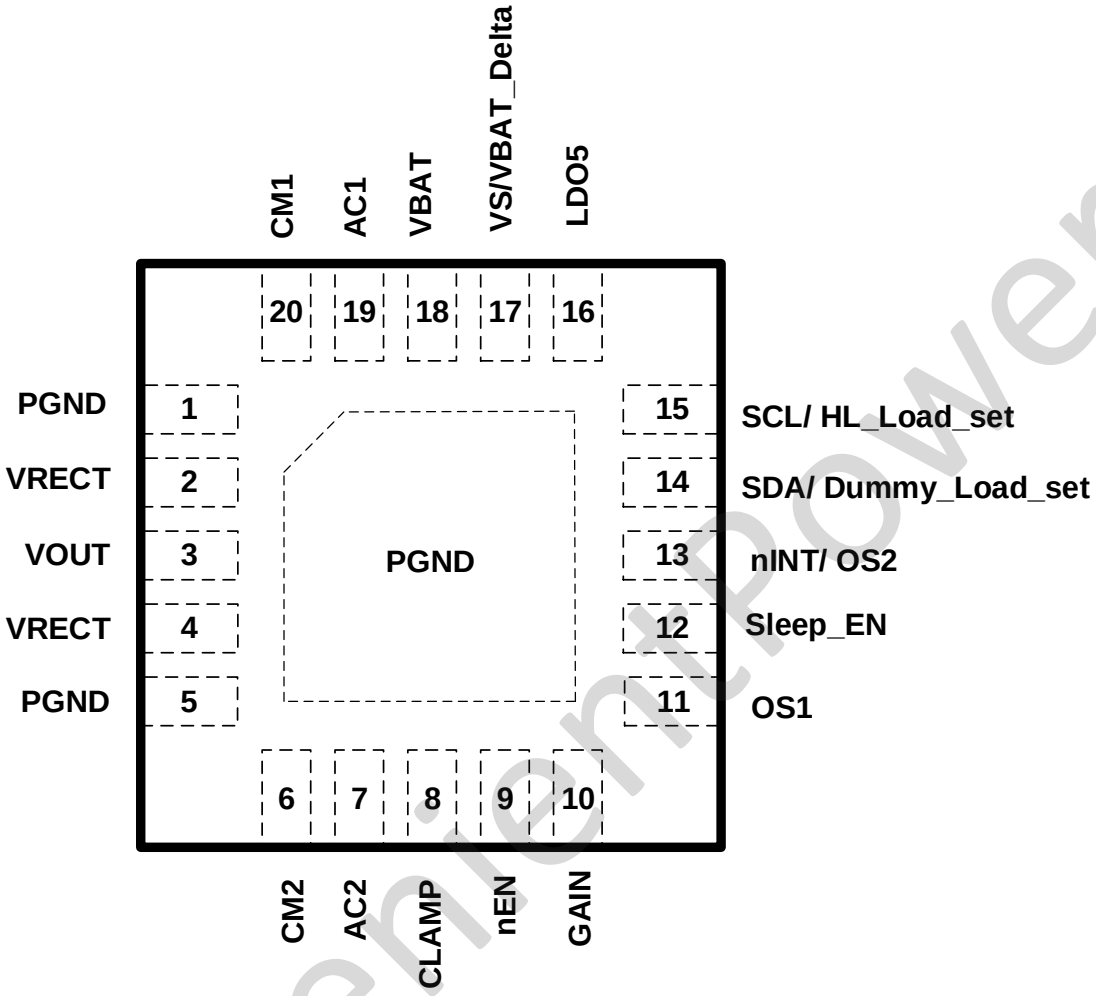


Figure 3: CPS4520 Pin-out (Top View)

3. Pin Descriptions

Table 1 Pin Descriptions

Pin	Name	Type	Function
1,5	PGND	GND	Power block GND.
2,4	VRECT	O	Full bridge Rectifier output pin. Connect at least a 10uF capacitor to PGND.
3	VOUT	O	Low dropout regulator(MLDO) output. Connect at least a 10uF capacitor to PGND.
6	CM2	O	Open-drain modulation FET. Connect a capacitor between AC2 and CM2.
7	AC2	I	AC2 input power for rectifier.
8	CLAMP	O	Over voltage clamp pin. Connect a 0.5W resistor between CLAMP and VRECT pin.
9	nEN	I	Active low enable input. Pull high will shut down the IC.
10	GAIN	I	FOD gain set input.
11	OS1	I	FOD offset at heavy load set input.
12	Sleep_EN	I	Control CE timeout if Sleep_EN pull up to 1.2V. Control MLDO VOUT turn off if Sleep_EN pull up higher than 1.5V. If not use, suggest to connect to GND.
13	nINT/OS2	I/O	Active low interrupt pin or FOD offset at light load set input. If used as interrupt I/O, please pull up to external system power rail. If not use, suggest to connect to GND.
14	SDA/Dummy_Load_set	I/O	SDA of I2C serial interface or VRECT dummy load at light load mode set pin. If not use, suggest to connect to GND.
15	SCL/HL_Load_set	I/O	SCL of I2C serial interface or heavy load threshold set pin. If not use, suggest to connect to GND.
16	LDO5	O	LDO5 output. Connect a 1uF capacitor to GND.
17	VS/VBAT_Delta	I	MLDO output voltage setting. Or it can be configured as dropout between VOUT and VBAT pin voltage. If not use, suggest to connect to GND.

Pin	Name	Type	Function
18	VBAT	I	Battery voltage sense pin, used to regulate the MLDO output voltage to track the battery voltage. If not use, suggest to connect to GND.
19	AC1	I	AC1 input power for rectifier
20	CM1	O	Open-drain modulation FET. Connect a capacitor between AC1 and CM1.

4. Specification

4.1. Absolute Maximum Ratings

Table 2 **Absolute maximum ratings**

Parameter		Min	Max	Unit
Power voltage	AC1/2, CM1/2, VRECT, CLAMP	-0.3	17	V
Power voltage	VO	-0.3	17	V
Power voltage	LDO5,VBAT	-0.3	6	V
Control pin voltage	nEN, nINT/OS2, SDA/Dummy_Load_set, SCL/HL_Load_set	-0.3	6	V
All Other Pin	GAIN, OS1, VS/VBAT_Delta, Sleep_EN	-0.3	6	V
Maximum RMS Current from pin	CM1/2, CLAMP		0.5	A
Maximum RMS Current from pin	AC1/2		2	A

Note: These are the stress ratings only. Stresses that exceeds the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at these or any other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

4.2. ESD Ratings

Table 3 **ESD Information**

Parameter	Value	Unit	Note
ESD tolerance	±2000	V	Human Body Model (HBM)
	±500	V	Charge Device Model (CDM)

4.3. Recommended Operation Conditions

Table 4 **Recommended operation range**

Parameter		Minimum	Typical	Maximum	Unit
V_{RECT}	Power voltage range	3		10	V
V_{cc}	Logic voltage range	-	4.6	5.5	V
I_C	Continuous MLDO output current	-	1	1.2	A
V_{OD}	Open drain pin Voltage	0		5.5	V

4.4. Thermal Information

Table 5 **Thermal Information**

Symbol	Parameter	Value	Units
T_J	Operating junction temperature. [a]	-40 to 125	°C
T_A	Operating ambient temperature. [a]	-40 to 85	°C
T_{STG}	Storage temperature	-55 to 155	°C
T_{BUMP}	Maximum Soldering Temperature	260	°C

[a] Actual thermal resistance is affected by the PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

4.5. Electronics Characteristics

VRECT=5V, T_J=-40 to 125℃. Typical values are at room temperature unless otherwise noted.

Table 6 Electronics Characteristics

Symbol	Parameter	Note	Min	Typical	Max	Unit
Quiescent Current						
$I_{VRECT\_SHUTDOWN}$	Shutdown current	nEN=high		137.5	180	μA
I_{VRECT_SUPPLY}	Supply current	nEN=low, no load		4	5	mA
$I_{VO\_SHUTDOWN}$	Vo shutdown current	nEN=high		150	270	μA
I_{VBAT}	VBAT≦4.5V	nEN=low/high VRECT=5V; VBAT=4V		0.5	2	μA
Input Supply						
V_{RECT}	VRECT voltage		3		10	V
V_{RECT_UVLO}	VRECT UVLO threshold	Rising		2.49		V
		Falling		2.33		V
		Hysteresis		160		mV
Internal LDO Regulator						
V_{LDO5}	LDO5 output voltage	Programmable 3.7V/4.2V/4.6V/5V	3.7	4.6	5	V
Accuracy	LDO5 output voltage regulation	I_{OUT5}=10mA, V_{RECT}>5.5V	5%		5%	V
I_{LDO5_max}	LDO5 maximum output current	V_{LDO5}=4.6V	20			mA
Synchronous Rectifier						
I_{SYNC_TH}	light load to heavy load threshold	Rising, Programmable		120		mA
		Hysteresis, Programmable		30		mA
R_{DSON_CM}	Modulation FET resistance	CM1/2		0.55	1	Ω
Main LDO(MLDO)						
V_{OUT}	MLDO output voltage	Programmable	3.5	5	9	V
V_{OUT_STEP}	Regulated output voltage step	Step		20		mV
ACC_{VOUT}	Output voltage accuracy		-2		2	%
I_{OUT_MAX}	Output current capability			1	1.2	A
V_{OUT_LNR}	Line regulation	VRECT = 5.3V to 10V, VOUT=5V, Iload=1mA	-0.5		0.5	%
V_{OUT_LDR}	Load regulation	VRECT=5.3V, VOUT=5V, IOUT = 1mA to 1A	-0.5		0.5	%
V_{OUT_PSRR}	PSRR in regulation	VRECT=5.3V, VOUT=5V,		-40		dB

Symbol	Parameter	Note	Min	Typical	Max	Unit
	mode	IOUT = 1A@1KHz				
V_{OUT_SS}	LDO start up slew-rate	Programmable		5		mV/us
VRECT Dummy Load						
I_{DUMMY}	Dummy Load Capacity	5mA step	0		50	mA
ACC_{IDUMMY}	Dummy Load Accuracy	<30mA	-2		+2	mA
		30mA to 50mA	5		5	%
Clamp						
I_{CLAMP}	Clamp current limit mode	Programmable 50mA/fully on /100mA/70mA		50	100	mA
I_{LKG_CLAMP}	CLAMP pin leakage current	CLAMP=5.5V	-1		1	uA
R_{ON_CLAMP}	Internal CLAMP FET Ron				1	Ω
Over-Voltage Protection						
V_{RECT_OV1}	VRECT OVP1 threshold	1V/step	10		13	V
$V_{RECT\_OV1\_HYS}$	VRECT OVP1 hysteresis			2		V
V_{RECT_OV2}	VRECT OVP2 threshold		14	15	16	V
$V_{RECT\_OV1\_HYS}$	VRECT OVP2 hysteresis			6		V
Thermal protection						
T_{SD}	T_J shutdown temperature			140		℃
ACC_{TEMP}	Temperature Accuracy	T_J from 0℃ to 125 ℃	-5		+5	℃
ADC						
N	Resolution			10		Bit
F_{sample}	ADC Sampling rate	F_{CLOCK_ADC} =250KHz		10		kHz
Channel	Number of channels			11		
V_{IN_FS}	ADC full scale			2.048		V
VRECT/VO Voltage Sense						
V_{RECT_ACC}	VRECT voltage sense accuracy	V_{RECT} from 5V to 12V	-1		1	%
		Vrect<5V	-50		50	mV
VSR_{RECT}	V_{RECT} sense range		3		12	V
V_{O_ACC}	VO voltage sense accuracy	V_O from 5V to 10V	-1		+1	%
		V_O <5V	-50		50	mV
VSR_O	VO sense range		3.5		10	V
Current Sense						

Symbol	Parameter	Note	Min	Typical	Max	Unit
I_{OUT_ACC}	IOUT current sense accuracy	0A ≤ Io ≤ 0.6A	-10		10	mA
		0.6A < Io ≤ 1A	-15		15	mA
		1A < Io ≤ 1.6A	-1.5		1.5	%
CSR_{IOUT}	Current sense range		0		1.6	A
BIAS Current for SDA/SCL/nINT/GAIN/OS1/VS parameters configure						
I_{BIAS1}	Current flow through pins and resister	Test on nINT, GAIN,OS1 pins	19.6	20	20.4	uA
I_{BIAS2}	Current flow through pins and resister	Test on SDA,SCL,VS pins	19	20	21	uA
nEN						
V_{IH_nEN}	nEN input high			0.7		V
V_{IL_nEN}	nEN input low			0.5		V
R_{PD_nEN}	nEN pull down resistance			1		MΩ
nINT						
V_{OL}	Output logic low	I_{OL} = 4mA			0.36	V
I_{LKG}	Leakage current		-1		1	uA
Sleep_EN						
$R_{PD\_Sleep\_EN}$	Sleep_EN pull down resistance			1		MΩ
I_{LKG}	Leakage current	Sleep_EN=5V		5		uA
I2C (SCL, SDA)						
CLK_{I2C}	I2C clock frequency				1	MHz
V_{IH}	Input high voltage			0.7		V
V_{IL}	Input low voltage			0.55		V
I_{LKG}	Leakage current		-1		1	uA
V_{OL}	Output logic low	I_{OL} = 4mA			0.36	V
T_{LOW}	Clock low			1.3		uS
T_{HIGH}	Clock high			0.6		uS

5. Typical Performance Characteristics

The following performance characteristics were taken under below condition:

Wireless power transmitter IC: CPS8601, transmitter coil: A11a, Z distance: 4mm; Wireless power receiver IC: CPS4520, receiver coil: ICTC-48031-9R0. Efficiency measured from transmitter Vpa to receiver Vout. $T_{AMBIENT}$ = 25°C, unless otherwise noted.

Figure 4: System Efficiency VS Output Power, Vout=5V

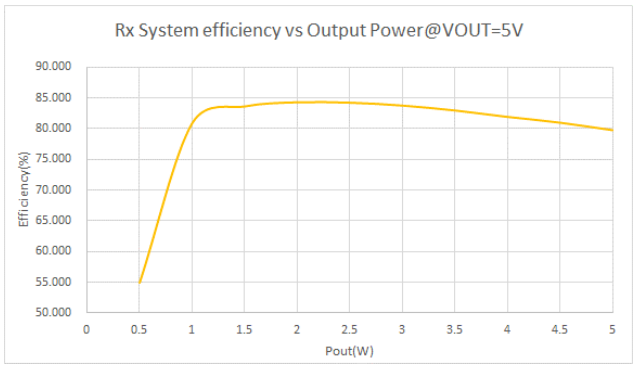


Figure 5: System Efficiency VS Output Power, Vout=9V

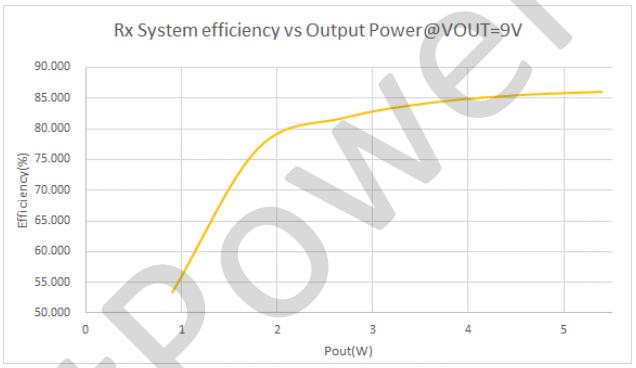


Figure 6: Rx Mode, Start up, Iout=0A

Figure 7: Rx Mode, Start up, Iout=1A

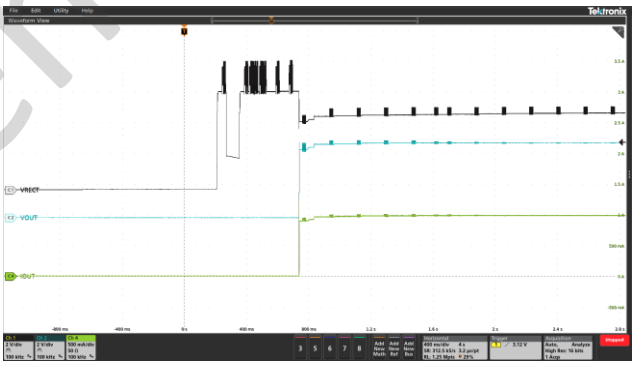


Figure 8: Rx Mode, AC Waveforms

(Iout=1A, Vrect=5.1V，Vout=5V)

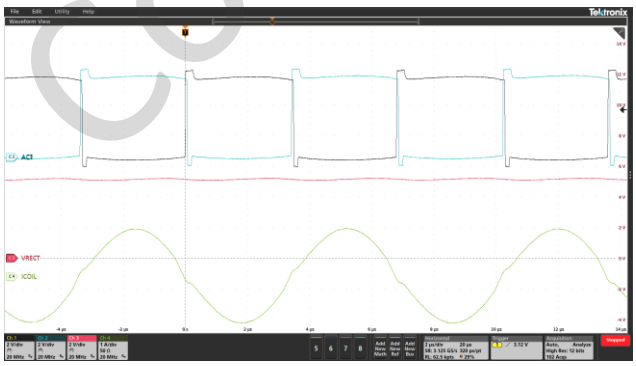
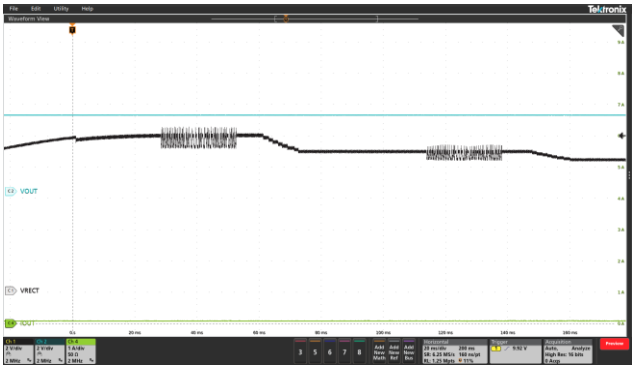


Figure 9: Rx Mode, Over-Voltage Protection

(Iout=0A, Vout=5V, Vrect_OVP1=10V)



6. Theory of Operation

6.1. Theory of Operation Overview

CPS4520 is a highly integrated wireless power receiver IC for low-power wearable applications. It can receive up to 5W in WPC Qi BPP or proprietary mode. This IC is not needed to be programmed so it can be easily designed in.

6.2. Synchronized Rectifier

In receiver mode, the rectifier receives AC power from LC tank via AC1 and AC2 pins and rectified to VRECT. It works in passive mode (all 4 FETs are OFF) during initial startup. When VRECT rises above UVLO, the full-bridge rectifier may work in half synchronous mode or full synchronous mode, depending on the loading condition.

6.3. Main LDO(MLDO)

CPS4520 integrates a main LDO to regulate the rectified voltage. After Rx is powered by Tx, CPS4520 FSM(finite-state machine) will enable main LDO when system can provide adequate energy for initiating power transfer. The main LDO also has soft start feature to ensure smooth turn on.

In receiver mode, the dropout voltage between VRECT and VOUT is set and dynamically adjusted by CPS4520 FSM, based on the load current.

The output voltage of the main LDO can be programed through I2C interface. The programmable voltage range is from 3.5V to 9V with 20mV step. And the output voltage also can be set by external resistor through VS pin.

If it's work under battery tracking mode, or for optimize system efficiency purpose, VOUT voltage can also be set based on the sensed VBAT voltage plus a adjustable headroom.

6.4. Internal Current Sense

The current sense circuit is used for main LDO current monitoring and over current protection. The current sense accuracy is ±15mA when Iout<1A for better FOD performance. For over-current protection, if the MLDO output current exceeds the pre-set current threshold, then an OC alarm is triggered and CPS4520 will send EPT OCP to end power transfer.

CPS4520 senses VRECT voltage and main LDO current periodically to obtain the real time output power. RP packet is calculated by them to represent the received power by Rx device, including CPS4520 output power, IC internal power consumption, Rx coil loss, as well as magnetic power loss.

6.5. Over-Voltage Protection

In the event of the VRECT voltage is above the pre-programmed OVP rising threshold (VRECT_OV1), CPS4520 will clamp the energy through the additional internal current load while sending OVP interrupt to Application Processor for further actions. The internal current load will release when the VRECT voltage falls below the OVP falling threshold. The maximum internal current load is 100mA. When the VRECT voltage is above another pre-programmed OVP rising threshold (VRECT_OV2), CPS4520 will send EPT OV to end

power transfer.

6.6. Over-Temperature Protection

CPS4520 supports on-die over-temperature protection. The internal die temperature is monitored by CPS4520 and will reports an over-temperature interrupt if die temperature exceeds 140°C. CPS4520 will turn-off main LDO and send EPT OT until the transmitter cut off the power. Power will resume when the transmitter re-applies the PING and the process will repeat.

6.7. WPC Qi Rx mode

At receiver (Rx) mode, alternating wireless power is picked up by the integrated full-wave synchronized rectifier from AC1/AC2 pins. The rectified DC voltage/energy is stored in the capacitors connected to VRECT pins and the capacitors also serve as a low-pass filter to reduce the ripple on VRECT. Then the integrated main LDO will provide a programmable, regulated output voltage VOUT for the subsequent system load such as a charger.

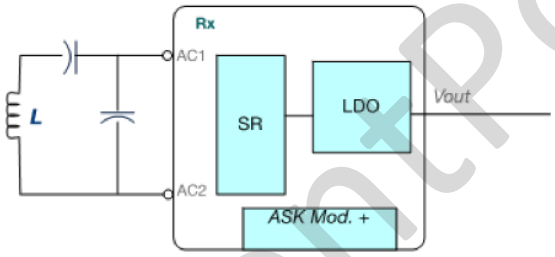


Figure 10: CPS4520 in Rx mode

The charging protocol is fully implemented by CPS4520 FSM. It supports standard WPC Qi v1.3 spec.

Below figure illustrates the relationship among Qi BPP phases. The solid arrows indicate transitions which Tx initiates, and the dash-dotted arrows indicate transitions that the Rx initiates. The implementation and transition of each phase is accomplished by CPS4520.

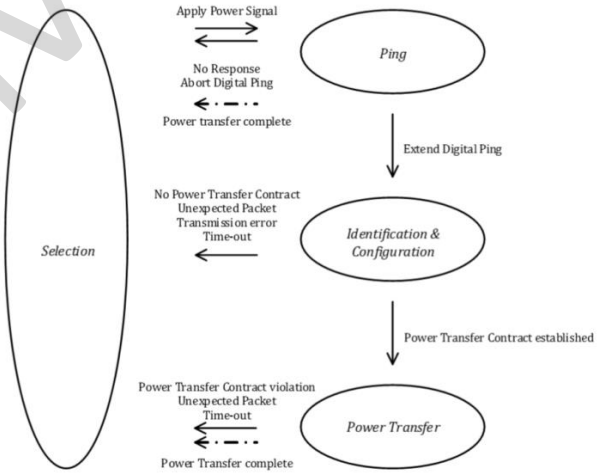


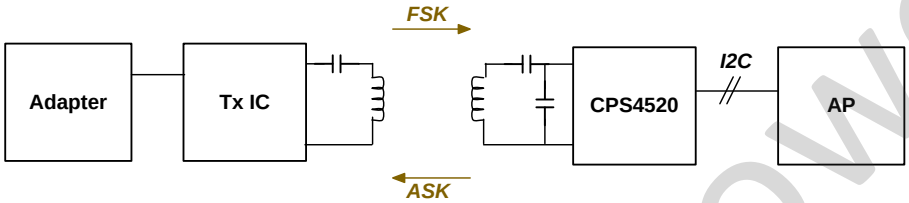
Figure 11: WPC Qi state diagram

6.8. ASK Communication

The power receiver communicates to the power transmitter by using Amplitude Shift Keying (ASK). This

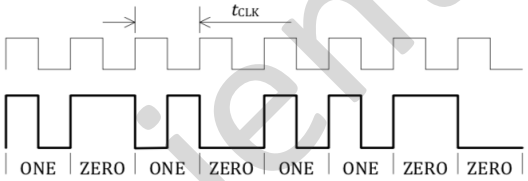
appears as an impedance change to the power transmitter, which results in measurable variations of the LC circuit voltage and current. CPS4520 has two modulation FETs to support in-band communication. When a required bit needs to be sent, CPS4520 will turn on internal modulation FETs for AC modulation. CPS4520 will detect the modulation direction by sample the Vout voltage during packet-sending and no-packet time. If the negative modulation is detected, FSM will control the reverse modulation register to change the system work condition. Then the modulation direction will change from negative to positive. The amplitude changes in the coil current and voltage can be detected by the transmitter for de-modulation. The communication protocol is implemented in CPS4520.

Figure 12: WPC Qi In-band Communication (Bi-directional)



CPS4520 uses bi-phase encoding scheme for data communication according to WPC Qi specification. The data-rate is 2kbp, as shown below.

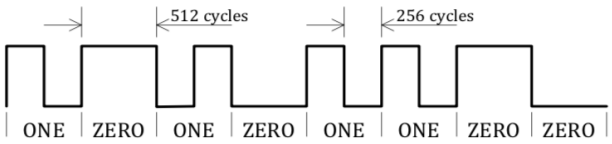
Figure 13: WPC Qi ASK Bi-Phase Encoding Scheme



6.9. Frequency Detector and FSK De-modulation

The power transmitter communicates to the power receiver by using Frequency Shift Keying (FSK), in which the transmitter modulates the operating frequency of the power signal. The FSK bit-encoding scheme is as shown below per WPC Qi specification. CPS4520 implements frequency detector and FSK demodulation circuitry to effectively de-code this in-band communication.

Figure 14: WPC Qi FSK Bit-Encoding Scheme



7. Applications Information

7.1. Wireless Power Receiver coil

For Qi compliant wireless power wearable device applications, the coil is the key part to get high system efficiency. CPS typically recommends a coil with following spec: Ls = 8μH to 10μH, DCR = < 0.3Ω and ACR = < 0.4Ω.

7.2. nEN

nEN is the CPS4520 chip enable pin. When nEN is logic low, CPS4520 will be enabled for any mode of operation. When nEN is pulled to logic high, the CPS4520 enters shutdown mode, and all functional blocks are disabled.

7.3. AC1/AC2

In the receiver mode, both series resonant capacitor and parallel resonant capacitor need to be selected carefully, due to the nature of WPC Qi defined magnetic induction system. In typical applications, multi-layer ceramic capacitors (MLCC) are used as the resonant capacitors, due to its small package and low profile. An MLCC with small footprint (e.g. 0402) and DC voltage rating of 50V is preferred for both series and parallel capacitors. Low ESR or impedance at specific frequency means less power loss on the capacitor, and thus better efficiency.

7.4. VRECT

When works in receiver mode, capacitor between VRECT and PGND is used to reduce the ripple that is generated by AC rectification. CPS typically recommends 2*10uF MLCC with a DC voltage rating of 25V or higher.

7.5. VOUT

When works in receiver mode, main LDO output is designed to function with low ESR MLCCs, for better efficiency and stability purpose. CPS typically recommends 2*10uF MLCC with a DC voltage rating of 16V or higher.

7.6. LDO5

The LDO5 generates a supply source for all the internal analog and digital circuit. The LDO5 default output voltage is 4.6V. The LDO5 pin must connect a 1μF capacitor to GND. This pin must not be externally loaded.

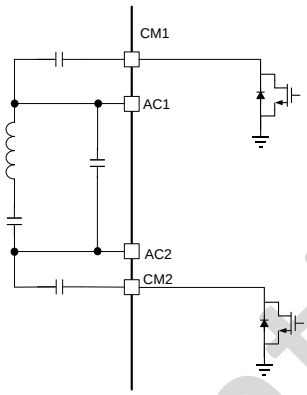
7.7. CLAMP

CPS4520 supports additional power dissipation path through external resistor and CLAMP pin. In this case, VRECT is connected to the CLAMP pin via a 200Ω resistor with higher than 1/4W power rating. When the VRECT voltage is higher than the Vrect_OV1 threshold, CPS4520 will turn on the clamp circuit to dump the energy from VRECT, the clamp circuit is released when the VRECT voltage falls below the VRECT OVP falling level.

7.8. CM1, CM2

During wireless charging stage, ASK in-band communication data is sent by the receiver modulating the load on the receiver coil. In the event of ASK data sending, CPS4520 turns on the internal FETs that are connected to load modulation pins (CM1, CM2), and the capacitor between AC pin and load modulation pin becomes a capacitive load seen by Tx coil. Figure 15 below shows the internal connection for modulation pins. Depending on different application scenarios, a high voltage MLCC with the capacitance range from 10nF to 47nF is typically recommended as the load modulation capacitor.

Figure 15: ASK Modulation and Communication



7.9. nINT/ OS2

The important function of pin nINT/ OS2 is to detect whether it's under I2C connection mode or resistor configure mode.

When this pin is pulled down by external resistor to GND, it will work in resistor configure mode, it's used to set the offset of FOD parameter at light load, see chapter 7.15 FOD configuration for more information.

When this pin is pulled up by external resistor to external power supply, it will work in I2C connection mode, and it will output logic low status for about 5ms when any interrupt event happens.

nINT interrupt definition:

- I2C_Ready: detection of work in I2C connection mode
- Stat_Vout: after turn on MLDO
- OVP : trigger Vrect OVP1&OVP2
- OCP: trigger MLDO OCP& fastoff
- OTP: trigger IC die over temperature
- TX Data Received: receive any Tx FSK packet
- AC missing: no AC signal detected

7.10. SCL/ HL_Load_set

SCL/ HL_Load_set pin is a multi-function pin. SCL/ HL_Load_set pin shall work in resistor configure more or I2C mode is determined by the external voltage level of the pin nINT/OS2.

When nINT/OS2 pin is pulled up by external resistor to external power supply, SCL/ HL_Load_set pin will work as the SCL line of I2C interface.

When nINT/OS2 pin is pulled down by external resistor to GND, SCL/ HL_Load_set pin will work in resistor configure mode, it's used to set the heavy load mode and light load mode switch threshold.

The CPS4520's heavy load threshold (I_{SYNC}_falling) is set by different pull down resistor, and the light load threshold= heavy load threshold - 30mA. The heavy load threshold will determine the rectifier working mode as well as the time when will VRECT dummy load take effect.

Heavy load threshold can be set from 60mA to 200mA (default is 120mA). Table 7 below shows the different set for heavy load threshold.

Table 7 **Rset vs Heavy load threshold**

Rset _typ (kohm)	1	10	30	51	75	100
Heavy load threshold (mA)	120	60	80	100	150	200

7.11. SDA/ Dummy_Load_set

SDA/Dummy_Load_set pin is a multi-function pin. SDA/Dummy_Load_set pin shall work in resistor configure more or I2C mode is determined by the external voltage level of the pin nINT/OS2.

When nINT/OS2 pin is pulled up by external resistor to external power supply, SDA/Dummy_Load_set pin will work as the SDA line of I2C interface.

When nINT/OS2 pin is pulled down by external resistor to GND, SDA/Dummy_Load_set pin will work in resistor configure mode, it's used to set the dummy load threshold under light load condition.

Under light load condition, VRECT dummy load is effective, otherwise VRECT dummy load will be turn off under heavy load condition.

VRECT dummy load threshold can be set from 5mA to 30mA (default is 15mA) through external resistor. Table 8 below shows the different set for dummy load threshold.

Table 8 **Rset vs Dummy load threshold**

Rset _typ (kohm)	1	10	30	51	75	100
Dummy load threshold (mA)	15	5	10	20	25	30

CPS4520 has a fixed I2C slave address of 0x30.

Note: If there is address conflict in application, please contact CPS.

CPS4520's SCL, SDA, and nINT are open-drain pins, if work in I2C mode, they need external pull-up resistors to connect to IO power rail.

7.12. VS/VBAT_Delta

VS/VBAT_Delta is a multi-function pin contains setting of MLDO output voltage(VOUT) and setting of the difference between VOUT and VBAT voltage(VBAT_Delta).

CPS4520 MLDO's default output voltage is 5.0V, if application requires a different value, VS/VBAT_Delta pin can be used to change the default voltage by connect a pull down resistor to GND, Table 9 below shows the different set for MLDO output voltage.

Table 9 Rset vs VOUT Set/VBAT_Delta

Rset _typ (kohm)	1	10	30	51	75	100
VOUT (V)	5.0	4.6	4.7	4.8	5.2	5.6
VBAT_Delta (mV)	300	100	200	400	500	600

For battery tracking mode, VBAT_Delta is used set the headroom between VOUT and VBAT, with a default value of 300mV. VBAT_Delta setting only works in battery tracking mode.

7.13. VBAT

VBAT pin is used to sense battery voltage under battery tracking mode. If application don't use battery tracking mode，suggest to connect this pin to GND.

7.14. Sleep_EN

CPS4520 supports external MLDO output and ASK modulation disable. If Sleep_EN pin voltage is pulled higher than 1.2V but below 1.5V (Sleep_EN pin is pulled up to high at least 10ms), CPS4520's FSM will stop the Qi state. If Sleep_EN pin voltage is pulled higher than 1.5V, CPS4520's FSM will turn off MLDO.

Table 10 Sleep_EN function definition

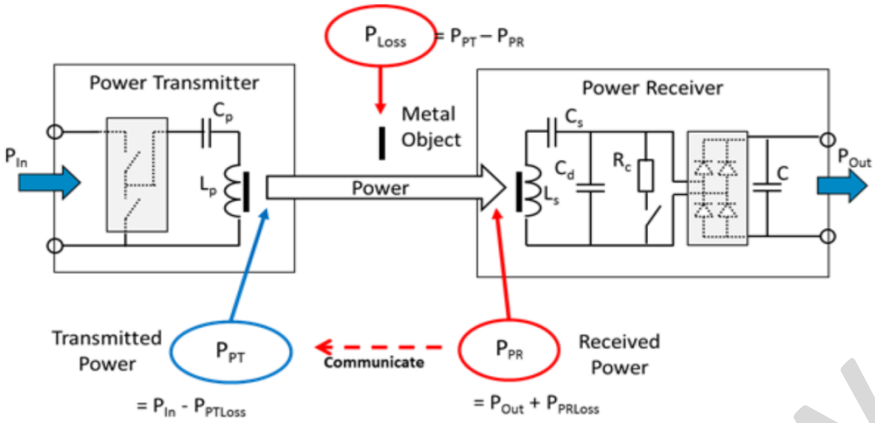
Sleep_EN	MLDO turn on?	Qi state?
Sleep_EN<1.2V	Y	Y
1.2V≤Sleep_EN<1.5V	Y	N
Sleep_EN≥1.5V	N	Y

7.15. FOD Configuration

FOD detect is a critical case for Qi compliance and inter-operability test, the FOD parameters(gain and offset) can be used for adjust foreign object detection threshold.

In realistic application, the FOD configuration needs adjustment case by case because of different coil designs like inductance, ACR, operation frequency as well as the friendly metal in the mechanical case. To cover different application atmosphere, CPS4520 use GAIN pin and OS1/OS2 pin for FOD gain and offset set.

Figure 16: Power loss illustrated



After get the receiver's output voltage and current, CPS4520 will communicate with Qi compatible transmitter and report its power information.

The resistor connected to GAIN pin to GND has an equation as below (R_{gain} max value is 100k):

$$FOD_{gain} = \frac{Rgain(k\Omega)}{50}$$

The resistor connected to OS1/OS2 pin to GND has an equation as below:

$$FOD_{offset1}(mW) = 40 * R_{OS1}(k\Omega) - 1000$$

$$FOD_{offset2}(mW) = 40 * R_{OS2}(k\Omega) - 1000$$

R_{OS1}/ R_{OS2} need to set from 7.5K to 87.5K, that means $FOD_{offset1}$/ $FOD_{offset2}$ can support from -0.7W to 2.5W through external resistor.

When nINT/OS2 pin is pulled up by external resistor to external power supply, CPS4520 FSM will auto use R_{OS1} value for RP value calculated both in heavy load and light load state. And support I2C to change $FOD_{offset1}$/ $FOD_{offset2}$ value through register.

When nINT/OS2 pin is pulled down by external resistor to GND, CPS4520 FSM will use R_{OS1} value for RP value calculated in heavy load state, and use R_{OS2} value for RP value calculated in light load state. And support I2C to change $FOD_{offset1}$/ $FOD_{offset2}$ value through register.

8. Typical Application Schematic

Figure 17: Typical Application Schematic

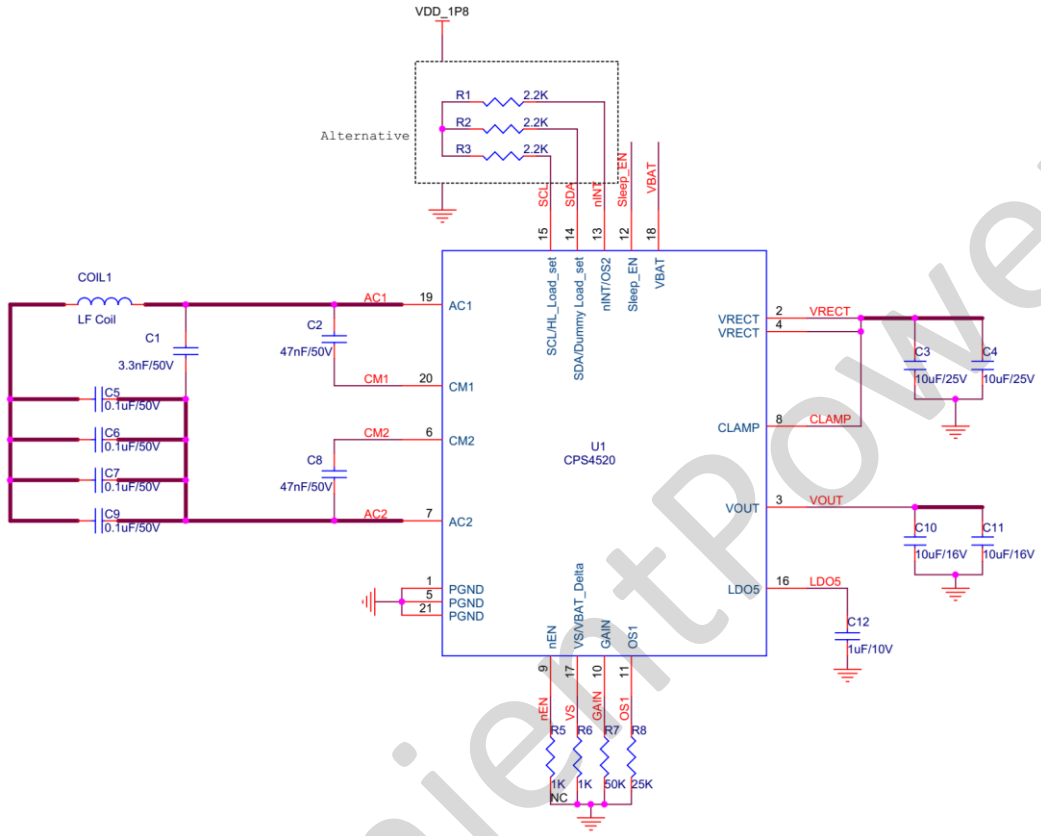
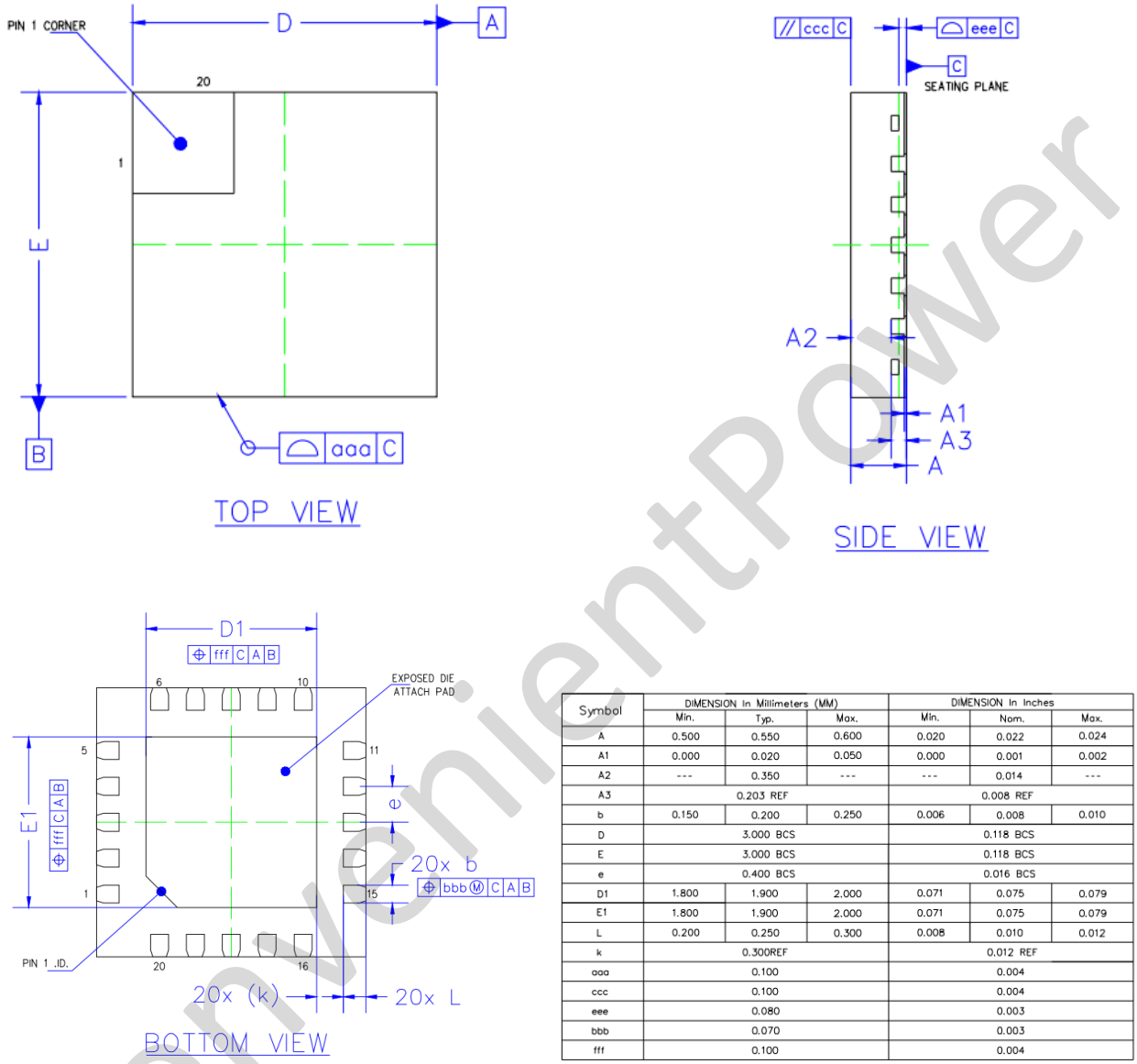


Table 11 Bill of Materials

Item	Quantity	Reference	Part	PCB footprint
1	1	COIL1	LF Coil	
2	1	C1	CAP, 0402 3.3nF 10% 50V X7R	C0402
3	2	C2,C8	CAP, 0402 47nF 10% 50V X7R	C0402
4	2	C3,C4	CAP, 0603 10uF 20% 25V X5R	C0603
5	4	C5,C6,C7,C9	CAP, 0402 0.1uF 10% 50V X7R	C0402
6	2	C10,C11	CAP, 0603 10uF 20% 16V X5R	C0603
7	1	C12	CAP, 0402 1uF 10% 10V X5R	C0402
8	3	R1,R2,R3	RES, 0201 2.2 KOhm 1% 1/20W	R0201
9	2	R5,R6	RES, 0201 1 KOhm 1% 1/20W	R0201
10	1	R7	RES, 0201 50 KOhm 1% 1/20W	R0201
11	1	R8	RES, 0201 25 KOhm 1% 1/20W	R0201
12	1	U1	CPS4520	QFN20,3mm*3mm

9. Package Outline Dimensions

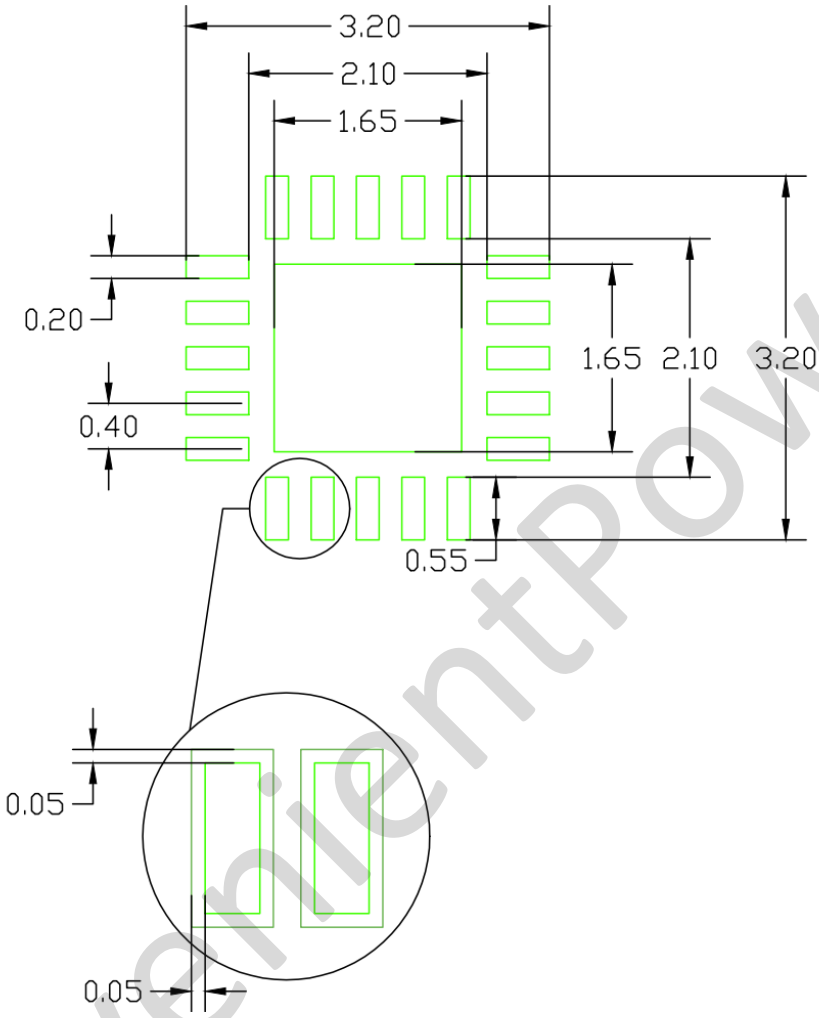
Figure 18: Package Information



Symbol	DIMENSION In Millimeters (MM)			DIMENSION In Inches		
	Min.	Typ.	Max.	Min.	Nom.	Max.
A	0.500	0.550	0.600	0.020	0.022	0.024
A1	0.000	0.020	0.050	0.000	0.001	0.002
A2	---	0.350	---	---	0.014	---
A3	0.203 REF			0.008 REF		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	3.000 BCS			0.118 BCS		
E	3.000 BCS			0.118 BCS		
e	0.400 BCS			0.016 BCS		
D1	1.800	1.900	2.000	0.071	0.075	0.079
E1	1.800	1.900	2.000	0.071	0.075	0.079
L	0.200	0.250	0.300	0.008	0.010	0.012
k	0.300REF			0.012 REF		
aaa	0.100			0.004		
ccc	0.100			0.004		
eee	0.080			0.003		
bbb	0.070			0.003		
fff	0.100			0.004		

10. Land Pattern Date

Figure 19: Recommended Land Pattern

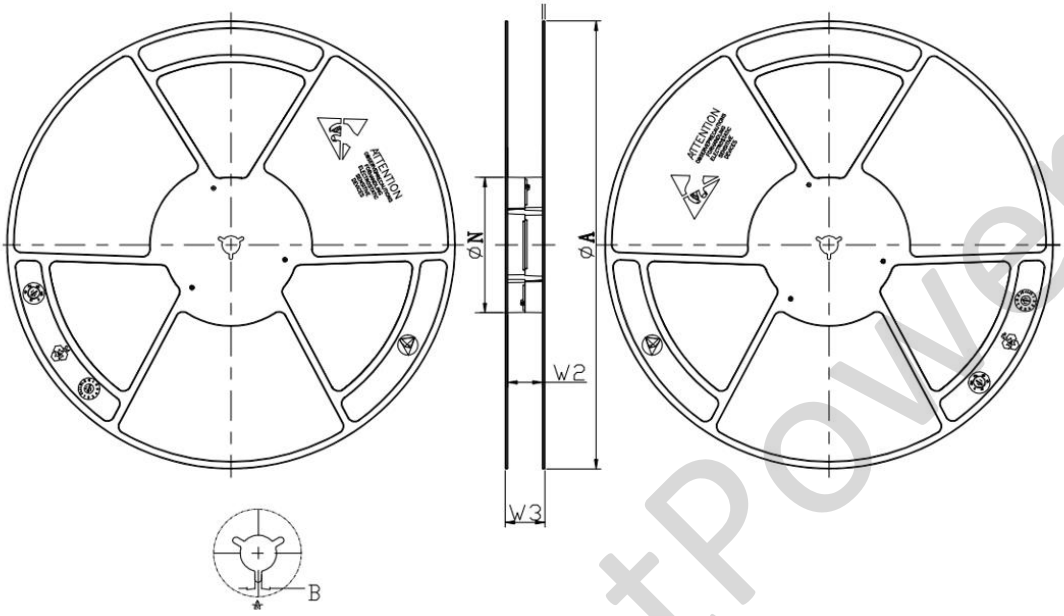


Note: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

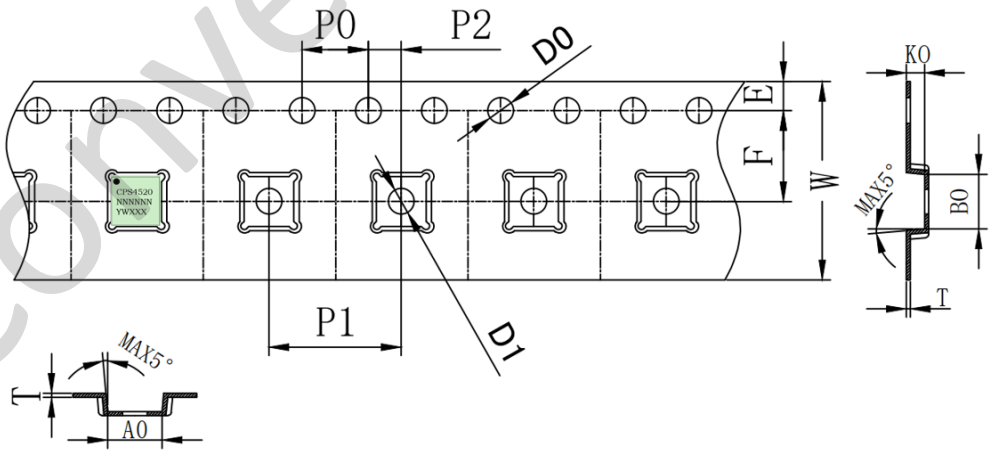
11. Tape and Reel Information

Figure 20: Reel Information



TYPE WIDTH	ØA	ØN	W1	W2	W3	B	Weight
13*12	330^{+2}_{-2}	100^{+2}_{-2}	2^{+1}_{-1}	13.5^{+2}_{-1}	18.5^{+2}_{-2}	$2.4^{+0.3}_{-0.3}$	200±10g

Figure 21: Carrier Tape Information



SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	3.30±0.10	3.30±0.10	0.85±0.10	4.00±0.10	8.00±0.10	2.00±0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.25±0.03	1.75±0.10	5.50±0.05	1.55±0.05	1.55±0.05	$12.00\ \pm^{0.3}_{0.1}$

12. Ordering Information

Table 12 Ordering Information

Part Number	Package	MSL Rating	Shipping
CPS4520HR	QFN3X3_20L	3	5000/Tape&Reel

13. Marking Diagram

1. CPS4520: The part number
2. “NNNNNN” is CPS Lot ID
3. Y= Last one digit of year; W=Work week of assembly;
   XXX=Trace Code, use capital (AA, AB… ZZ)

14. Important Notice

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