

Assignment 05 – UART RX

Documentation

Assignment Protocol

Fachhochschule Vorarlberg
ET-Dual

HDL – Hardware Description Layer

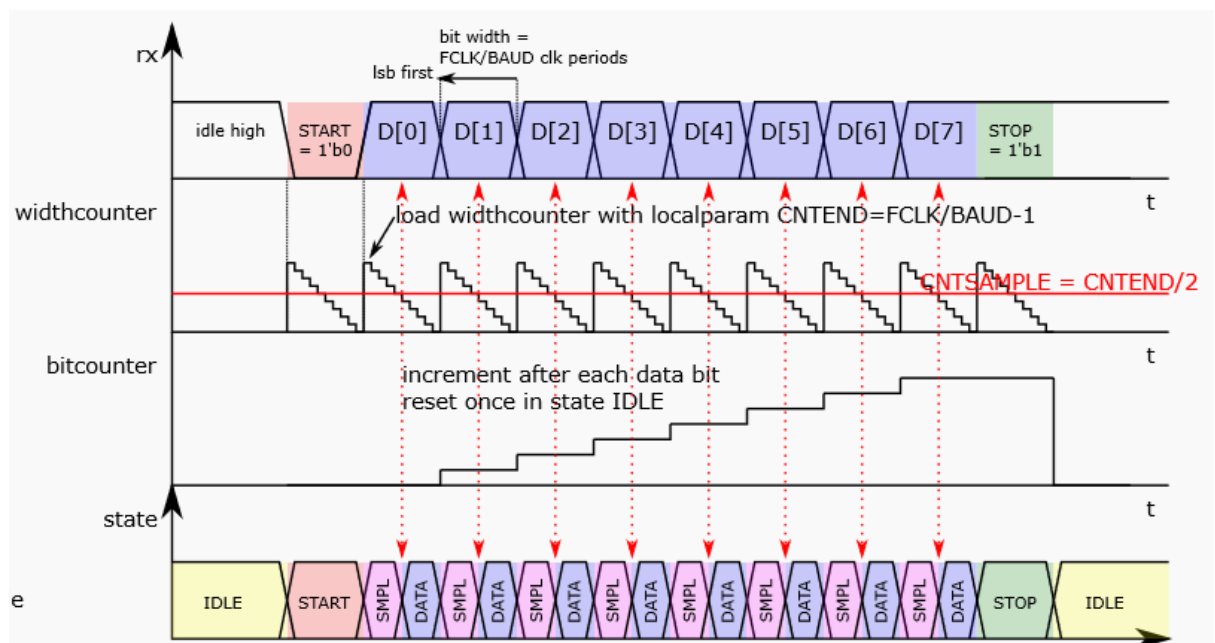


Figure 1: Function of UART RX (Src.: Mitterbacher)

Author:
Stefan Duenser

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1. Task description

UART is a digital serial interface that is often used for data exchange between CPU and external peripherals.

After implementing the UART Transmit interface during the lecture, the goal of this 5th assignment was to implement the corresponding Receive interface. This way data can not only be sent.

Data should be received as follows:

- from an idle state the state transitions to the start state via a start bit.
- then 8 data bits follow
- followed by a stop bit before the state changes back to the IDLE state.

The data bits are handled in such a way that the data is sampled after half of the data bit width has elapsed.

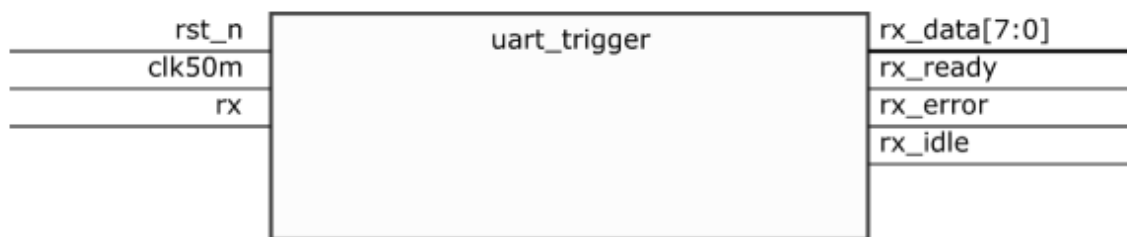


Figure 2: UART RX input and outputs (Src.: Mitterbacher)

The block diagram in Fig. 3 clearly shows which stages the UART RX must pass through to successfully receive data. Fig. 1 also shows how the communication is structured.

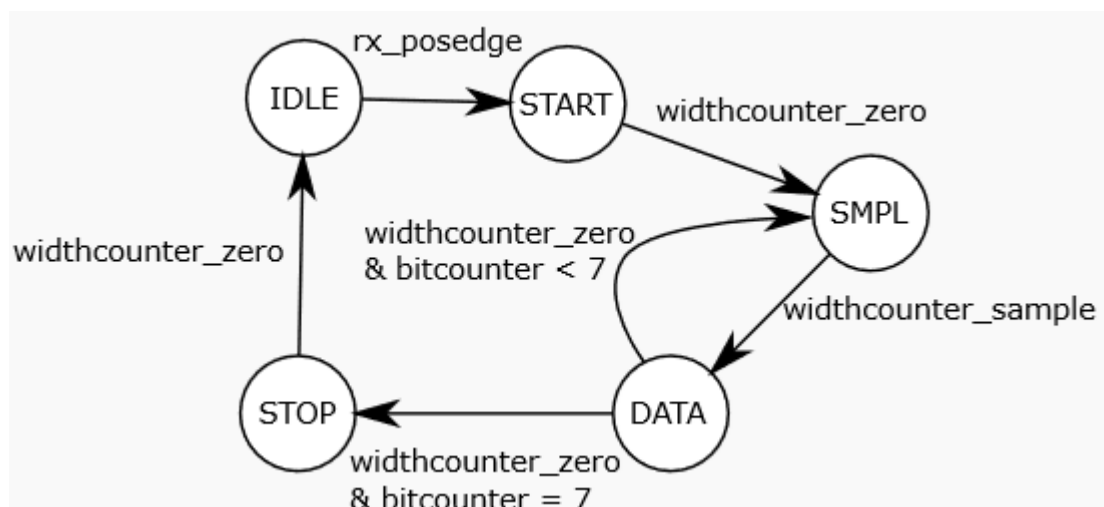


Figure 3: Block diagram of UART RX (Src.: Mitterbacher)

2. Source code

The UART RX is implemented via a finite state machine (FSM). The width of the bits as well as the number (counter) of the bits is solved via memory blocks in an always_ff. The states rx_ready (ready to receive data) and rx_error (framing error) are also stored. Therefore, logic temporary variables were needed to set the information in the combinatorial part (Fig. 6) so that it could be stored later. To save memory space, the logic was implemented in an always_comb (Fig. 6).

In comparison to the UART TX, and also to separate the states cleanly, the state SMPL (sample) was introduced for the UART RX. Fig. 1 shows when the data is sampled. The block diagram (Fig. 3) shows the switching condition for the next state.

```
8 module uart_rx
9 #(
10     parameter WIDTH = 8,
11     parameter FCLK = 50000000, // 50 MHz clock
12     parameter FBAUD = 115200
13 )
14 (
15     input logic rst_n,
16     input logic clk50m,
17     input logic rx,
18
19     output logic [WIDTH-1:0] rx_data,
20     output logic rx_ready,
21     output logic rx_idle,
22     output logic rx_error
23 );
24
25 // --- localparameters ---
26 localparam WIDTHCNT_INIT = ((FCLK / FBAUD) - 1);
27 localparam WIDTHCNT_WIDTH = $clog2(WIDTHCNT_INIT);
28 localparam SAMPLECNT_INIT = WIDTHCNT_INIT / 2;
29
30 // --- local signals ---
31 logic widthcnt_zero;
32 logic widthcnt_load;
33 logic [WIDTHCNT_WIDTH-1:0] widthcnt;
34 logic bitcnt_inc;
35 logic bitcnt_init;
36 logic [2:0] bitcnt;
37 logic widthcnt_sample;
38
39 logic receive_ready;
40 logic receive_error;
41
42 // --- FSM ---
43 enum logic [2:0] {IDLE, START, SMPL, DATA, STOP} state, state_next;
44 assign widthcnt_sample = (widthcnt == SAMPLECNT_INIT);
```

Figure 4: UART RX inputs and calculation of UART bit widthcount

```
50 always_ff @(negedge rst_n or posedge clk50m) begin : fsm_seq
51     if(~rst_n) begin
52         state <= IDLE;
53     end
54     else begin
55         state <= state_next;
56     end
57 end
58
59 // --- WIDTHCNT counter ---
60 always_ff @(negedge rst_n or posedge clk50m) begin : widthcnt_counter
61     if(~rst_n) begin
62         widthcnt <= '0;
63     end
64     else if(widthcnt_load) begin
65         widthcnt <= WIDTHCNT_INIT;
66     end
67     else if(~widthcnt_zero) begin
68         widthcnt <= widthcnt - 1'b1;
69     end
70 end
71 assign widthcnt_zero = (widthcnt == '0);
72
73 // --- BITCNT counter ---
74 always_ff @(negedge rst_n or posedge clk50m) begin : bitcnt_counter
75     if(~rst_n) begin
76         bitcnt <= '0;
77     end
78     else if(bitcnt_init) begin
79         bitcnt <= '0;
80     end
81     else if(bitcnt_inc) begin
82         bitcnt <= bitcnt + 1'b1;
83     end
84 end
85
86 // --- FF to save flag rx_ready ---
87 always_ff @(negedge rst_n or posedge clk50m) begin : rx_ready_flag
88     if(~rst_n || ~receive_ready) begin
89         rx_ready <= 1'b0;
90     end
91     else if(receive_ready) begin
92         rx_ready <= 1'b1;
93     end
94     else begin
95         rx_ready <= rx_ready;
96     end
97 end
98
99 // --- FF to save flag rx_error ---
100 always_ff @(negedge rst_n or posedge clk50m) begin : rx_error_flag
101     if(~rst_n || ~receive_error) begin
102         rx_error <= 1'b0;
103     end
104     else if(receive_error) begin
105         rx_error <= 1'b1;
106     end
107     else begin
108         rx_error <= rx_error;
109     end
110 end
```

Figure 5: Definition of finite state machine (FSM) of the UART RX

```

119 always_comb begin : fsm_comb
120     // Default values
121     state_next      = state;
122     rx_idle         = 1'b0;    // Flag is just one if idel state is present
123     widthcnt_load   = 1'b0;
124     bitcnt_init     = 1'b0;
125     bitcnt_inc      = 1'b0;
126     case(state)
127     IDLE: begin
128         rx_idle      = 1'b1;
129         bitcnt_init   = 1'b1;
130         if(rx == 1'b0) begin
131             state_next = START;
132             receive_error = '0;
133             widthcnt_load = 1'b1;
134         end
135     end
136     START: begin
137         receive_error = 1'b0;    // Cleared as soon as a new frame startes
138         receive_ready = 1'b0;    // Cleared as soon as a new frame startes
139         if(widthcnt_zero) begin
140             state_next = SMPL;
141             widthcnt_load = 1'b1;
142             bitcnt_init = 1'b1;
143         end
144     end
145     SMPL: begin
146         if(widthcnt_sample) begin
147             state_next = DATA;
148             rx_data[bitcnt] = rx;
149         end
150     end
151     DATA: begin
152         if((widthcnt_zero) && (bitcnt < 3'd7)) begin
153             state_next = SMPL;
154             widthcnt_load = 1'b1;
155             bitcnt_inc = 1'b1;
156         end
157         else if((widthcnt_zero) && (bitcnt >= 3'd7)) begin
158             state_next = STOP;
159             widthcnt_load = 1'b1;
160         end
161         else if (widthcnt_sample == SAMPLECNT_INIT) begin
162             state_next = SMPL;
163         end
164     end
165     STOP: begin
166         if(rx == 1'b0) begin
167             receive_error = 1'b1;
168         end
169         if(widthcnt_zero) begin
170             state_next = IDLE;
171             receive_ready = 1'b1;
172         end
173     end
174     default: begin
175         state_next = IDLE;
176     end
177 endcase
178 end
179
180 endmodule

```

Figure 6: Implementation of block diagram

3. Testbench

The UART RX was tested in a corresponding testbench. The UART TX, already described in the lecture, was used to send constant default values (default assignment). The function `check_uart_rx` serves to simplify the general queries whether the reception of the data worked as expected or not.

New in contrast to the previous assignments was that combinatorial logic was also required in the testbench. The purpose of this was to provoke a framing error in the testbench. In Fig. 8 you can see that the combinatorial logic checks whether an error is present or not. When checking the correctness of the data reception, it can then be reacted to.

The test should always be terminated when a byte has been successfully received. This is the case when the state changes back to IDLE after the stop bit as recognition for the end of the reception. Afterwards a waiting time was inserted, in order to be able to keep the individual test bytes better apart.

```
8 module tb_uart_rx
9 ();
10
11 // (1) DUT wiring
12 localparam WIDTH_TB = 8;
13 localparam FCLK_TB = 50000000;
14 localparam FBAUD_TB = 115200;
15
16 // Input and output parameters for the UART RX
17 logic rst_n;
18 logic clk50m;
19 logic rx;
20 logic [WIDTH_TB-1:0] rx_data;
21 logic rx_ready;
22 logic rx_idle;
23 logic rx_error;
24
25 // Input and output parameters for the UART TX - just additional parameters
26 logic [WIDTH_TB-1:0] tx_data;
27 logic tx_start;
28 logic tx;
29 logic tx_idle;
30
31
32
33
34 // (2) DUT instance
35 uart_rx #(.WIDTH (WIDTH_TB), .FCLK (FCLK_TB), .FBAUD (FBAUD_TB)) uart_rx (.*);
36
37 uart_tx #(.WIDTH (WIDTH_TB), .FCLK (FCLK_TB), .BAUD (FBAUD_TB)) uart_tx (
38     .rst_n_i (rst_n),
39     .clk_i (clk50m),
40     .data_i (tx_data),
41     .tx_start_i (tx_start),
42     .tx_o (tx),
43     .idle_o (tx_idle)
44 );
45
```

Figure 7: Modulation of the testbench for the UART RX

```
48 // (3) DUT stimulation
49 // --- local parameter ---
50 int error_cnt = 0;
51 int bitwidth = 0;
52 logic run_sim = 1'b1;
53 logic rx_error_active = 1'b0;
54 logic error = 1'b0;
55
56
57 // Define the system clock for the testbench
58 initial begin
59     clk50m = 1'b0;
60     while (run_sim == 1'b1) begin
61         #10ns;
62         clk50m = ~clk50m;
63     end
64 end
65
66 // Check if an rx error is currently active
67 always_comb begin : error_check
68     if (rx_error_active == 1'b1) begin
69         rx = error;
70     end
71     else begin
72         rx = tx;
73     end
74 end
75
76
77 // Function to check the UART RX
78 function int check_uart_rx(int error_cnt, logic [WIDTH_TB-1:0] rx_data, logic rx_ready, logic rx_error, logic rx_idle);
79     int errorCount;
80     errorCount = error_cnt;
81     assert(rx_data == tx_data) begin
82         $display("Received UART message equals Sent UART message");
83         $display("UART RX: %h", rx_data);
84         $display("UART TX: %h", tx_data);
85         $display("Flag ready: %b", rx_ready);
86         $display("Flag error: %b", rx_error);
87         $display("Flag idle: %b", rx_idle);
88     end
89     else begin
90         $error("Error during receiving UART message occurred");
91         $display("UART RX: %h", rx_data);
92         $display("UART TX: %h", tx_data);
93         $display("Flag ready: %b", rx_ready);
94         $display("Flag error: %b", rx_error);
95         $display("Flag idle: %b", rx_idle);
96         errorCount++;
97     end
98     return errorCount;
99 endfunction

```

Figure 8: Clock definition, frame error manipulation and check function

```

130     $display("-----");
131     $display("Check for 0x5A");
132     @(negedge clk50m);
133     tx_data    = 8'h5A;
134     tx_start   = 1'b1;
135     #100ns;
136     tx_start   = 1'b0;
137     @(posedge rx_idle);
138     @(negedge clk50m);
139     error_cnt = check_uart_rx(error_cnt, rx_data, tx_data, rx_ready, rx_idle, rx_error);
140     #10us;
141
142     $display("-----");
143     $display("Check for 0x00");
144     @(negedge clk50m);
145     tx_data    = 8'h00;
146     tx_start   = 1'b1;
147     #100ns;
148     tx_start   = 1'b0;
149     @(posedge rx_idle);
150     @(negedge clk50m);
151     error_cnt = check_uart_rx(error_cnt, rx_data, tx_data, rx_ready, rx_idle, rx_error);
152     #10us;
153
154     $display("-----");
155     $display("Check for 0xFF");
156     @(negedge clk50m);
157     tx_data    = 8'hFF;
158     tx_start   = 1'b1;
159     #100ns;
160     tx_start   = 1'b0;
161     @(posedge rx_idle);
162     @(negedge clk50m);
163     error_cnt = check_uart_rx(error_cnt, rx_data, tx_data, rx_ready, rx_idle, rx_error);
164     #10us;
165
166     $display("-----");
167     $display("Check for a forced framing fault");
168     @(negedge clk50m);
169     tx_data    = 8'h00;
170     tx_start   = 1'b1;
171     #100ns;
172     tx_start   = 1'b0;
173
174     #85us;
175     rx_error_active = 1'b1;
176     error = 1'b0;
177     #1us;
178     rx_error_active = 1'b0;
179     @(posedge rx_idle);
180     @(negedge clk50m);
181     error_cnt = check_uart_rx(error_cnt, rx_data, tx_data, rx_ready, rx_idle, rx_error);
182     #10ns;
183
184     $display("-----");
185     $display("Check if the fault is cleared when a new frame starts");
186     @(negedge clk50m);
187     tx_data    = 8'hFF;
188     tx_start   = 1'b1;
189     #100ns;
190     tx_start   = 1'b0;
191     @(posedge rx_idle);
192     @(negedge clk50m);
193     error_cnt = check_uart_rx(error_cnt, rx_data, tx_data, rx_ready, rx_idle, rx_error);
194

```

Figure 9: Test of the UART RX

4. Verification

In the Wave Window you can see very well that the counters for the bit width and the bit counter are displayed in analog form. This makes it easier to recognize the exact intersection points of the individual signal entries.

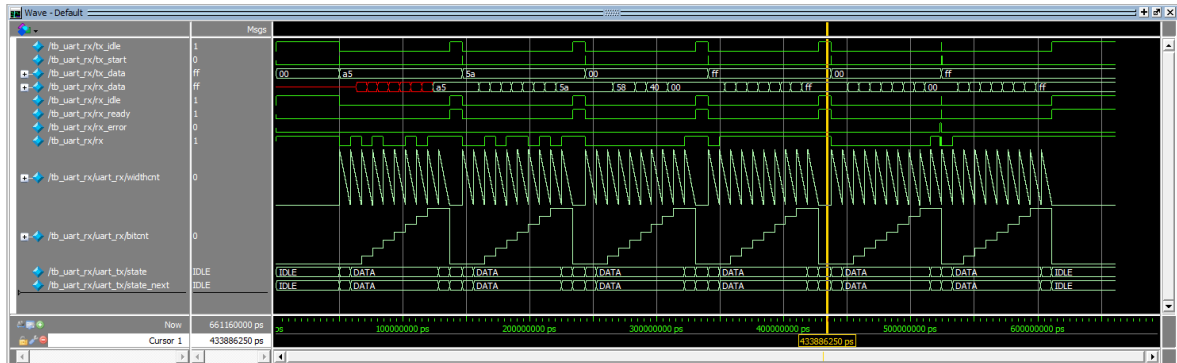


Figure 10: Wave form of the UART RX

```
# *****
# Welcome to the testbench for an UART Receive (tb_uart_rx)
# -----
# Start with a reset
# -----
# Check for 0xA5
# Received UART message equals Sent UART message
# UART RX: a5
# UART TX: a5
# Flag ready: 1
# Flag error: 0
# Flag idle: 1
# -----
# Check for 0x5A
# Received UART message equals Sent UART message
# UART RX: 5a
# UART TX: 5a
# Flag ready: 1
# Flag error: 0
# Flag idle: 1
# -----
# Check for 0x00
# Received UART message equals Sent UART message
# UART RX: 00
# UART TX: 00
# Flag ready: 1
# Flag error: 0
# Flag idle: 1
# -----
# Check for 0xFF
# Received UART message equals Sent UART message
# UART RX: ff
# UART TX: ff
# Flag ready: 1
# Flag error: 0
# Flag idle: 1
# -----
# Check for a forced framing fault
# Received UART message equals Sent UART message
# UART RX: 00
# UART TX: 00
# Flag ready: 1
# Flag error: 1
# Flag idle: 1
# -----
# Check if the fault is cleared when a new frame starts
# Received UART message equals Sent UART message
# UART RX: ff
# UART TX: ff
# Flag ready: 1
# Flag error: 0
# Flag idle: 1
# -----
# Errors occurred during the testing: 0
# -----
# Testbench for the UART Receive finished (tb_uart_rx)
# *****
```

Figure 11: Log file of the UART RX