MOD-I2C-GPIO

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1 Description

MOD-I2C-GPIO implements simple GPIO expander. The project is based on PIC16F18324 with following capabilities:

- 8 GPIOs
  - Input level can be ether CMOS or TTL
  - Output can be OD or PP
  - All pins supports weak-pull ups
  - Interrupts can be used on all pins
- 1 configurable DAC
- 1 configurable ADC

2 Memory map

The device has memory map as shown on Figure 1.

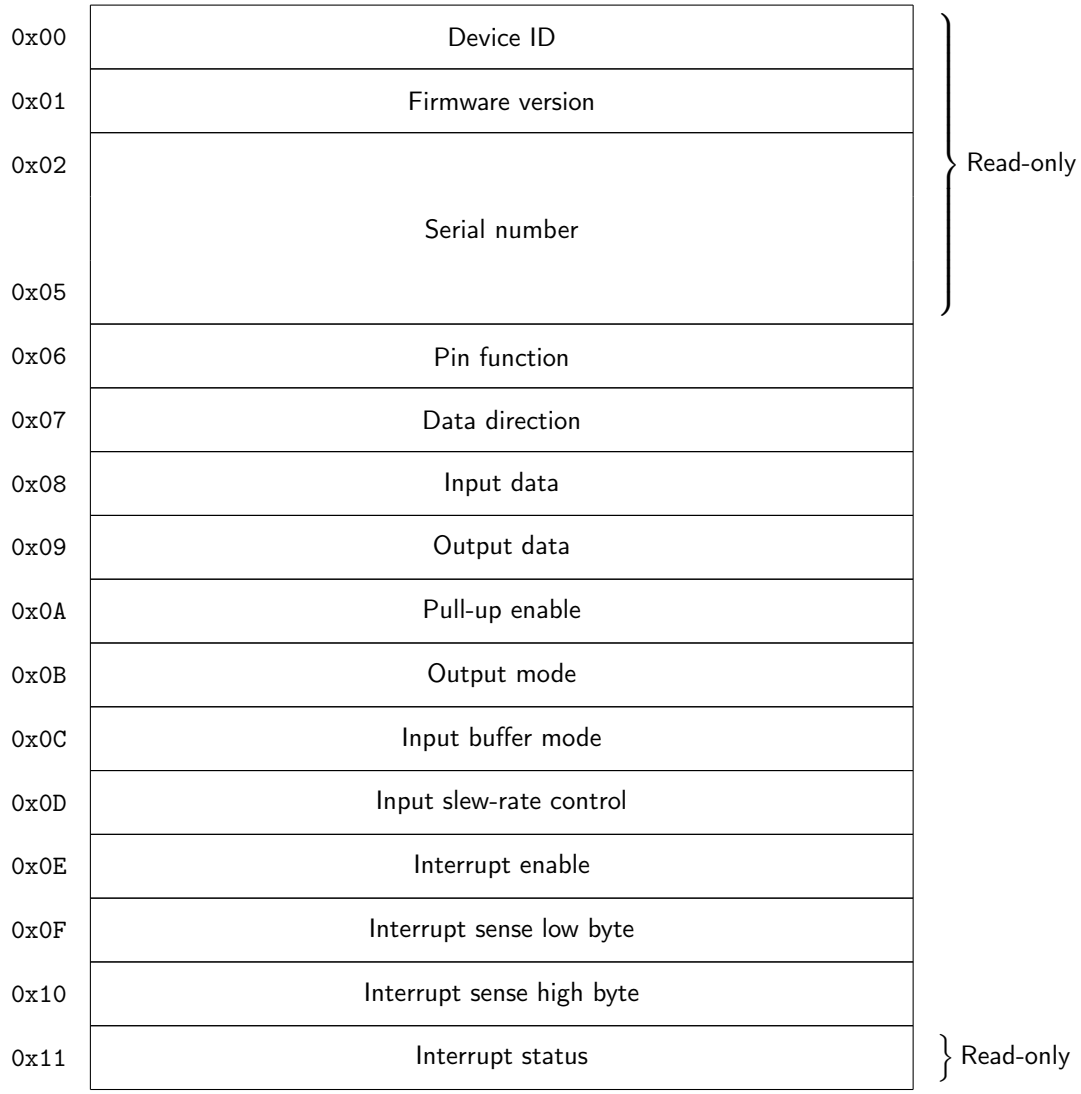

Figure 1: Memory layout

3 Device registers

sdasd

3.1 Device ID

This register holds the unique device identification. It can be used for detection. The register is read-only, so it cannot change.

Address: 0x00
Default: 0x43

7	6	5	4	3	2	1	0
ID							

Figure 2: Device ID register

3.2 Firmware version

Each new firmware release has its own revision. It's stored to this read-only register. The first release is 0x01, the second - 0x02, etc.

Address: 0x01
Default: -

7	6	5	4	3	2	1	0
FW							

Figure 3: Firmware revision register

3.3 Serial number

This is unique serial number. The length is 4 bytes.

Address: 0x02
Default: -

7	6	5	4	3	2	1	0
SN [31:24]							
SN [23:16]							
SN [15:8]							
SN [7:0]							

Figure 4: Serial number register

3.4 Pin function

Some of the GPIOs can be configure as alternative function: DAC and ADC. The register allows this to be configured. By default all function is GPIO.

Address: 0x06
Default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	FUN2	-	FUN0

Figure 5: Pin function register

- **FUN2**: PIN2 function control bit
  - 1: Setup PIN2 as ADC
  - 0: Setup PIN2 as GPIO
- **FUN0**: PIN0 data direction control bit
  - 1: Setup PIN0 as DAC
  - 0: Setup PIN0 as GPIO

3.5 Data direction

Each GPIO can be input or output. Setting a bit will make the corresponding pin input. Clearing it - output.

Address: 0x07
Default: 0x00

7	6	5	4	3	2	1	0
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0

Figure 6: Data direction register

- **DIR7**: GPIO7 data direction control bit
  - 1: Setup GPIO7 as input
  - 0: Setup GPIO7 as output
- **DIR6**: GPIO6 data direction control bit
  - 1: Setup GPIO6 as input
  - 0: Setup GPIO6 as output
- **DIR5**: GPIO5 data direction control bit
  - 1: Setup GPIO5 as input
  - 0: Setup GPIO5 as output
- **DIR4**: GPIO4 data direction control bit
  - 1: Setup GPIO4 as input
  - 0: Setup GPIO4 as output
- **DIR3**: GPIO3 data direction control bit
  - 1: Setup GPIO3 as input
  - 0: Setup GPIO3 as output
- **DIR2**: GPIO2 data direction control bit
  - 1: Setup GPIO2 as input
  - 0: Setup GPIO2 as output
- **DIR1**: GPIO1 data direction control bit
  - 1: Setup GPIO1 as input
  - 0: Setup GPIO1 as output
- **DIR0**: GPIO0 data direction control bit
  - 1: Setup GPIO0 as input
  - 0: Setup GPIO0 as output

3.6 Input data

This register holds input levels.

Address: 0x08
Default: - - - -

7	6	5	4	3	2	1	0
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Figure 7: Input data register

- **IN7**: GPIO7 input value
  - 0: Input level on GPIO7 is low
  - 1: Input level on GPIO7 is high
- **IN6**: GPIO6 input value
  - 0: Input level on GPIO6 is low
  - 1: Input level on GPIO6 is high
- **IN5**: GPIO5 input value
  - 0: Input level on GPIO5 is low
  - 1: Input level on GPIO5 is high
- **IN4**: GPIO4 input value
  - 0: Input level on GPIO4 is low
  - 1: Input level on GPIO4 is high
- **IN3**: GPIO3 input value
  - 0: Input level on GPIO3 is low
  - 1: Input level on GPIO3 is high
- **IN2**: GPIO2 input value
  - 0: Input level on GPIO2 is low
  - 1: Input level on GPIO2 is high
- **IN1**: GPIO1 input value
  - 0: Input level on GPIO1 is low
  - 1: Input level on GPIO1 is high
- **IN0**: GPIO0 input value
  - 0: Input level on GPIO0 is low
  - 1: Input level on GPIO0 is high

3.7 Output data

This register sets output GPIO level.

Address: 0x09
Default: 0x00

7	6	5	4	3	2	1	0
OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Figure 8: Output data register

- **OUT7**: GPIO7 output value
  - 0: Drive GPIO low
  - 1: Drive GPIO high
- **OUT6**: GPIO6 output value
  - 0: Drive GPIO low
  - 1: Drive GPIO high
- **OUT5**: GPIO5 output value
  - 0: Drive GPIO low
  - 1: Drive GPIO high
- **OUT4**: GPIO4 output value
  - 0: Drive GPIO low
  - 1: Drive GPIO high
- **OUT3**: GPIO3 output value
  - 0: Drive GPIO low
  - 1: Drive GPIO high
- **OUT2**: GPIO2 output value
  - 0: Drive GPIO low
  - 1: Drive GPIO high
- **OUT1**: GPIO1 output value
  - 0: Drive GPIO low
  - 1: Drive GPIO high
- **OUT0**: GPIO0 output value
  - 0: Drive GPIO low
  - 1: Drive GPIO high

3.8 Pull-up enable

All GPIOs has internal weak pull-up resistors. They are enabled by default, to minimize noise and power consumption. The can be disabled by either writing 0 to the corresponding bit or making the direction output.

Special case is when GPIO is configure as open-drain. If the bit for given GPIO is set, then the pull-up is enabled is DAT bit is set. On DAT clear, the pull-up becomes inactive.

Address: 0x0A
Default: 0xFF

7	6	5	4	3	2	1	0
PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0

Figure 9: Pull-up control register

- **PU7**: GPIO7 data direction control bit
  - 0: Disables GPIO7 internal pull-up resistor
  - 1: Enables GPIO7 internal pull-up resistor
- **PU6**: GPIO6 data direction control bit
  - 0: Disables GPIO6 internal pull-up resistor
  - 1: Enables GPIO6 internal pull-up resistor

- **PU5**: GPIO5 data direction control bit
  - 0: Disables GPIO5 internal pull-up resistor
  - 1: Enables GPIO5 internal pull-up resistor
- **PU4**: GPIO4 data direction control bit
  - 0: Disables GPIO4 internal pull-up resistor
  - 1: Enables GPIO4 internal pull-up resistor
- **PU3**: GPIO3 data direction control bit
  - 0: Disables GPIO3 internal pull-up resistor
  - 1: Enables GPIO3 internal pull-up resistor
- **PU2**: GPIO2 data direction control bit
  - 0: Disables GPIO2 internal pull-up resistor
  - 1: Enables GPIO2 internal pull-up resistor
- **PU1**: GPIO1 data direction control bit
  - 0: Disables GPIO1 internal pull-up resistor
  - 1: Enables GPIO1 internal pull-up resistor
- **PU0**: GPIO0 data direction control bit
  - 0: Disables GPIO0 internal pull-up resistor
  - 1: Enables GPIO0 internal pull-up resistor

3.9 Output mode

All outputs can be configured either as push-pull or open-drain.

Address: 0x0B
Default: 0x00

7	6	5	4	3	2	1	0
OM7	OM6	OM5	OM4	OM3	OM2	OM1	OM0

Figure 10: Output mode control register

- **OM7**: GPIO7 output mode control bit
  - 0: Drive GPIO7 as push-pull
  - 1: Drive GPIO7 as open-drain
- **OM6**: GPIO6 output mode control bit
  - 0: Drive GPIO6 as push-pull
  - 1: Drive GPIO6 as open-drain
- **OM5**: GPIO5 output mode control bit
  - 0: Drive GPIO5 as push-pull
  - 1: Drive GPIO5 as open-drain
- **OM4**: GPIO4 output mode control bit
  - 0: Drive GPIO4 as push-pull
  - 1: Drive GPIO4 as open-drain
- **OM3**: GPIO5 output mode control bit
  - 0: Drive GPIO3 as push-pull

  - 1: Drive GPIO3 as open-drain
- **OM2**: GPIO2 output mode control bit
  - 0: Drive GPIO2 as push-pull
  - 1: Drive GPIO2 as open-drain
- **OM1**: GPIO1 output mode control bit
  - 0: Drive GPIO1 as push-pull
  - 1: Drive GPIO1 as open-drain
- **OM0**: GPIO0 output mode control bit
  - 0: Drive GPIO0 as push-pull
  - 1: Drive GPIO0 as open-drain

3.10 Input buffer

Input levels can be configured for either CMOS or TTL operation.

Address: 0x0C
Default: 0xFF

7	6	5	4	3	2	1	0
IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0

Figure 11: Input buffer control register

- **IB7**: GPIO7 input buffer control bit
  - 0: TTL input on GPIO7
  - 1: CMOS ST input on GPIO7
- **IB6**: GPIO6 input buffer control bit
  - 0: TTL input on GPIO6
  - 1: CMOS ST input on GPIO6
- **IB5**: GPIO5 input buffer control bit
  - 0: TTL input on GPIO5
  - 1: CMOS ST input on GPIO5
- **IB4**: GPIO4 input buffer control bit
  - 0: TTL input on GPIO4
  - 1: CMOS ST input on GPIO4
- **IB3**: GPIO3 input buffer control bit
  - 0: TTL input on GPIO3
  - 1: CMOS ST input on GPIO3
- **IB2**: GPIO2 input buffer control bit
  - 0: TTL input on GPIO2
  - 1: CMOS ST input on GPIO2
- **IB1**: GPIO1 input buffer control bit
  - 0: TTL input on GPIO1
  - 1: CMOS ST input on GPIO1
- **IB0**: GPIO0 input buffer control bit

  - 0: TTL input on GPIO0
  - 1: CMOS ST input on GPIO0

3.11 Input slew-rate control

Address: 0x0D
Default: 0xFF

7	6	5	4	3	2	1	0
SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

Figure 12: Input slew-rate control register

- **SR7**: GPIO7 input slew-rate control bit
  - 0: Port pin slews at maximum rate
  - 1: Port pin slew rate is limited
- **SR6**: GPIO6 input slew-rate control bit
  - 0: Port pin slews at maximum rate
  - 1: Port pin slew rate is limited
- **SR5**: GPIO5 input slew-rate control bit
  - 0: Port pin slews at maximum rate
  - 1: Port pin slew rate is limited
- **SR4**: GPIO4 input slew-rate control bit
  - 0: Port pin slews at maximum rate
  - 1: Port pin slew rate is limited
- **SR3**: GPIO3 input slew-rate control bit
  - 0: Port pin slews at maximum rate
  - 1: Port pin slew rate is limited
- **SR2**: GPIO2 input slew-rate control bit
  - 0: Port pin slews at maximum rate
  - 1: Port pin slew rate is limited
- **SR1**: GPIO1 input slew-rate control bit
  - 0: Port pin slews at maximum rate
  - 1: Port pin slew rate is limited
- **SR0**: GPIO0 input slew-rate control bit
  - 0: Port pin slews at maximum rate
  - 1: Port pin slew rate is limited