UNIVERSITY OF ABERDEEN SESSION 2013/2014

CS1520/KL159C Computer Architecture

Date 28th May 2014 Time 15:00 - 17:00

Candidates are not permitted to leave the Examination Room during the first or last half hours of the examination.

There are three questions.
You choose to answer TWO questions. The marks for each part of a question are shown in brackets.

Question 1:

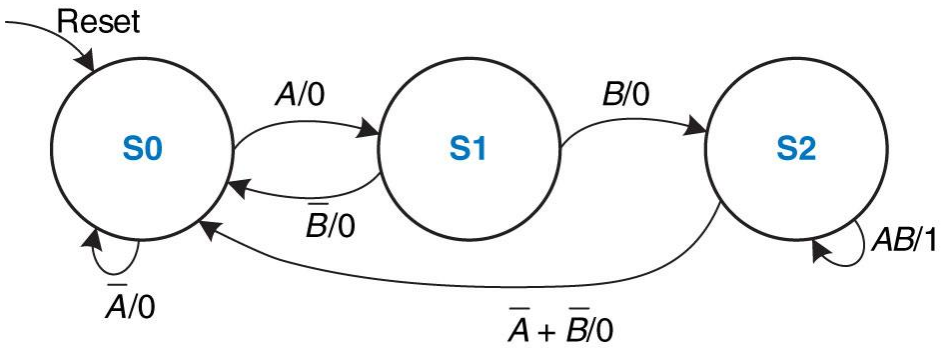
(a) In the 8086 assembly language, what is the difference between a macro program and a sub-program? What are their relative advantages?

[3 marks]

(b) Alice Wood will enjoy her picnic on sunny days that have no ants. She will also enjoy her picnic any day she sees a hummingbird, as well as on days where there are ants and ladybugs. Write a Boolean equation for her enjoyment (E) in terms of sun (S), ants (A), hummingbirds (H), and ladybugs (L).

[2 marks]

(c) (i) Describe in words what the state machine in the Figure below does. (ii) Using binary state encodings, complete a state transition table and output table for the finite state machine (FSM). (iii) Write Boolean equations for the next state and output and sketch a schematic of the FSM.



[10 marks]

PLEASE TURN OVER

(d) Design 4-bit left and right rotators. Sketch a schematic of your design.

[5 marks]

(e) (i) Find a minimal Boolean equation for the function in the Figure below. Remember to take advantage of the don't care entries.

A	*B*	*C*	*D*	*Y*
0	0	0	0	X
0	0	0	1	X
0	0	1	0	X
0	0	1	1	0
0	1	0	0	0
0	1	0	1	X
0	1	1	0	0
0	1	1	1	X
1	0	0	0	1
1	0	0	1	0
1	0	1	0	X
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	X
1	1	1	1	1

(ii) Sketch a circuit for the above function.

[5 marks]

Question 2

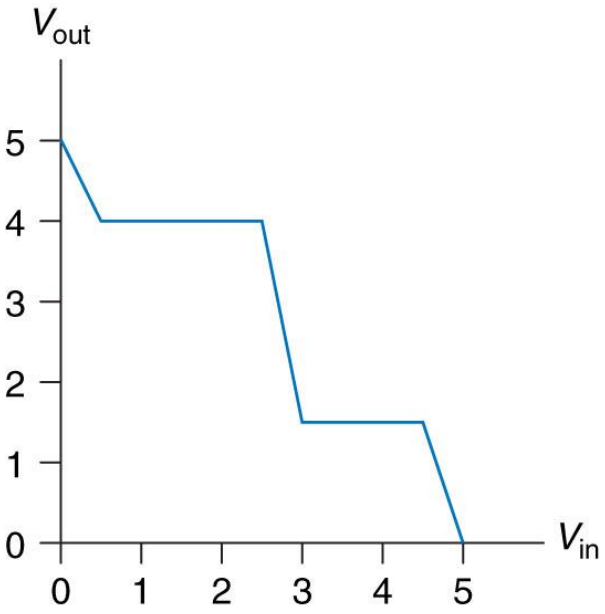
(a) What errors are present in the following code:

```
mov 23, ax
mov cx, ch
inc ax, 2
```

[3 marks]

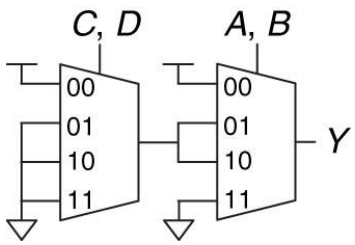
(b) Is it possible to assign logic levels so that a device with the transfer characteristics shown in the following figure would serve as an inverter? If so, what are the input and output low and high levels (VIL, VOL, VIH, VOH) and noise margins (NML, and NMH)? If not, explain why not.

[4 marks]



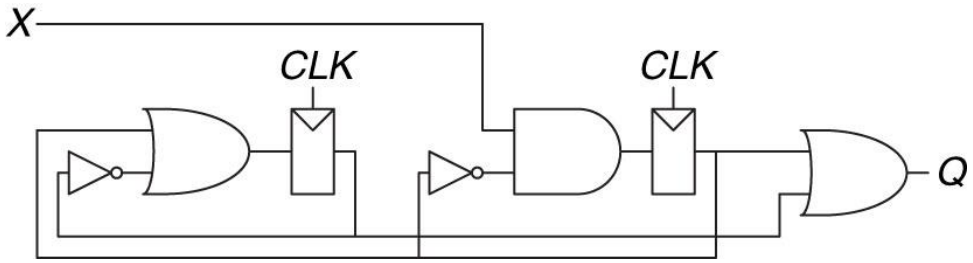
(c) Write a minimized Boolean equation for the function performed by the circuit in the Figure below:

[3 marks]



(d) Analyse the FSM shown in the figure below. (i) Write the state transition and output tables and sketch the state transition diagram. (ii) Describe in words what the FSM does.

[10 marks]



(e) An incrementer adds 1 to an N-bit number. Draw a diagram of an 8-bit incrementer using half-adders.

[5 marks]

PLEASE TURN OVER

Question 3

(a) Assume that each two-input gate delay is 150ps and that a full adder delay is 450ps.
What is the delay for the following type of 64-bit adder?
Adder type: A carry-lookahead adder with 4-bit blocks

[2 marks]

(b) Write a code fragment in 8086 to display the characters from 'a' to 'z' on the screen, given the sub-program to display character is "putc". Note that the ASCII codes forms a collating sequence. This means that the code for 'b' is one greater than the code for 'a' and the code for 'c' is one greater than that for 'b' and so on.

[5 marks]

(c) (i) Simplify the following Boolean equation.
Y = B C + not(A) not(B) not (C) + B not(C)
(ii) Then implement the above simplified equation using a 2:1 multiplexer, one OR gate, and an inverter.

[5 marks]

(d) Implement the following functions using a 4 x 8 x 3 PLA. You may use dot notation.

I. $X = AB + B\overline{C}D + \overline{A}\overline{B}$

II. $Y = AB + BD$

III. $z = A + B + C + D$

[8 marks]

(e) Design a "not equal" comparator for 32-bit numbers. Sketch the schematics.
[Hint: use XOR and OR gates]

[5 marks]

END OF PAPER