1 General

This document is the specification for the TM96.1B GENIE Explorer I development and TM96.1A GENIE Explorer I demonstrator modules, which combine the HMT7742 GENIE IO-Link Device PHY with an Atmel ATmega328P microcontroller running an IO-Link V1.1 conformal Mini-stack and demonstration application from HMT microelectronic AG.

1.1 Use cases

- ***HMT7742 GENIE IO-Link Device PHY hardware/software orientation platform***

  The HMT IO-Link protocol mini-stack and demo application source code demonstrate how one can control the full feature set of the HMT7742 GENIE IO-Link Device PHY. These include source code examples of:

  - Multi-Octet UART Mode
  - Transparent Mode
  - device configuration
  - Single-Octet UART Mode
  - interrupt handling
  - device monitoring

- ***HMT7742 development platform for sensor or actuator applications***

  Combining the HMT7742 GENIE IO-Link Device PHY, a supported Atmel µC and the HMT IO-Link protocol mini-stack.

  The customer develops the sensor or actuator application, using the TM96.1B hardware together with the HMT IO-Link mini-stack and demonstration application source code' as a base. Suitable I/O's on the µC are made available for the connection of a customer specific application.

- ***HMT7742 GENIE IO-Link DUAL PHY demonstrator***

  The small format TM96.1A running a mini-stack and default application from HMT demonstrates; the physical (PHY) characteristics, the ability to drive SIO loads and the handling of error conditions.

- ***EMC demonstrator platform***

  EMC testing carried out on the small format TM96.1A hardware placed in a realistic sensor enclosure, demonstrates the HMT7742's conformity to:

  - surge
  - conducted disturbance
  - ESD
  - burst
  - radiated disturbance
  - reverse polarisation

- **Atmel microcontroller demonstrator**

  The TM96.1A and TM96.1B running the HMT IO-Link mini-stack and default application demonstrates the capacity of the µC to support the IO-Link stack and PHY, and demonstrates the availability of free resources.

1.2 References

1.2.1 TM96.1 GENIE Explorer I

[1] HMT7742 datasheet (Please see HMT website for latest version)

[2] Atmel ATmega328P 8-bit AVR Microcontroller datasheet

1.2.2 HMT IO-Link Mini-stack and Demo-application

[3] DATASHEET and Source Code IO-Link mini-stack

[4] DATASHEET and Source Code demo-application

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1.3 Overview

1.3.1 TM96.1 GENIE Explorer Variant B

A block diagram of the TM141.0 test module can be seen in Fig. 1 The positioning of each block is consistent with the hardware layout and contains the following:

- **HMT7742 GENIE IO-Link Device PHY in a DFN12L 3mm x 4mm package**
- **ATmega328P 8-bit AVR microcontroller †**
- **2 x LED's [1 x Red, 1x green]**
- **push button switch (digital stimulus)**
- **rotary potentiometer (analog stimulus)**
- **connection to IO-Link master over standard M5 3-Pole connector**
- **connection for microcontroller programming over SPI**
- **SPI connection to the HMT7742 for further Atmel microcontroller development applications**
- **expansion ports for complex sensor applications**

† The TM96.1B is populated with the ATmega328P per default, but may also be populated with the pin compatible ATtiny88 (ATtiny88 -MU [MLF Package]).

Test module Variant B is intended to allow simplified connection for developments kits. The component platform is a 4-layer, 1mm, standard FR4 PCB.

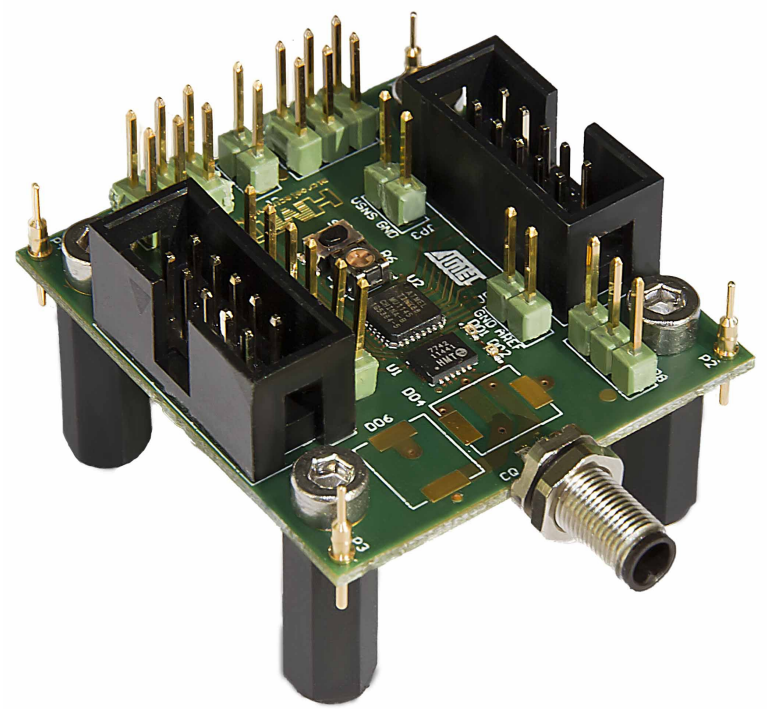

Illustration 1: TM96.1 GENIE Explorer I Variant B (Development)

Customers using the TM96.1 Variant B have the freedom to choose their software development platform. On-board ATMEL microcontrollers may be programmed with customer specific applications via an Atmel AVR ISP, JTAG-mkII and AVR Dragon programmers.

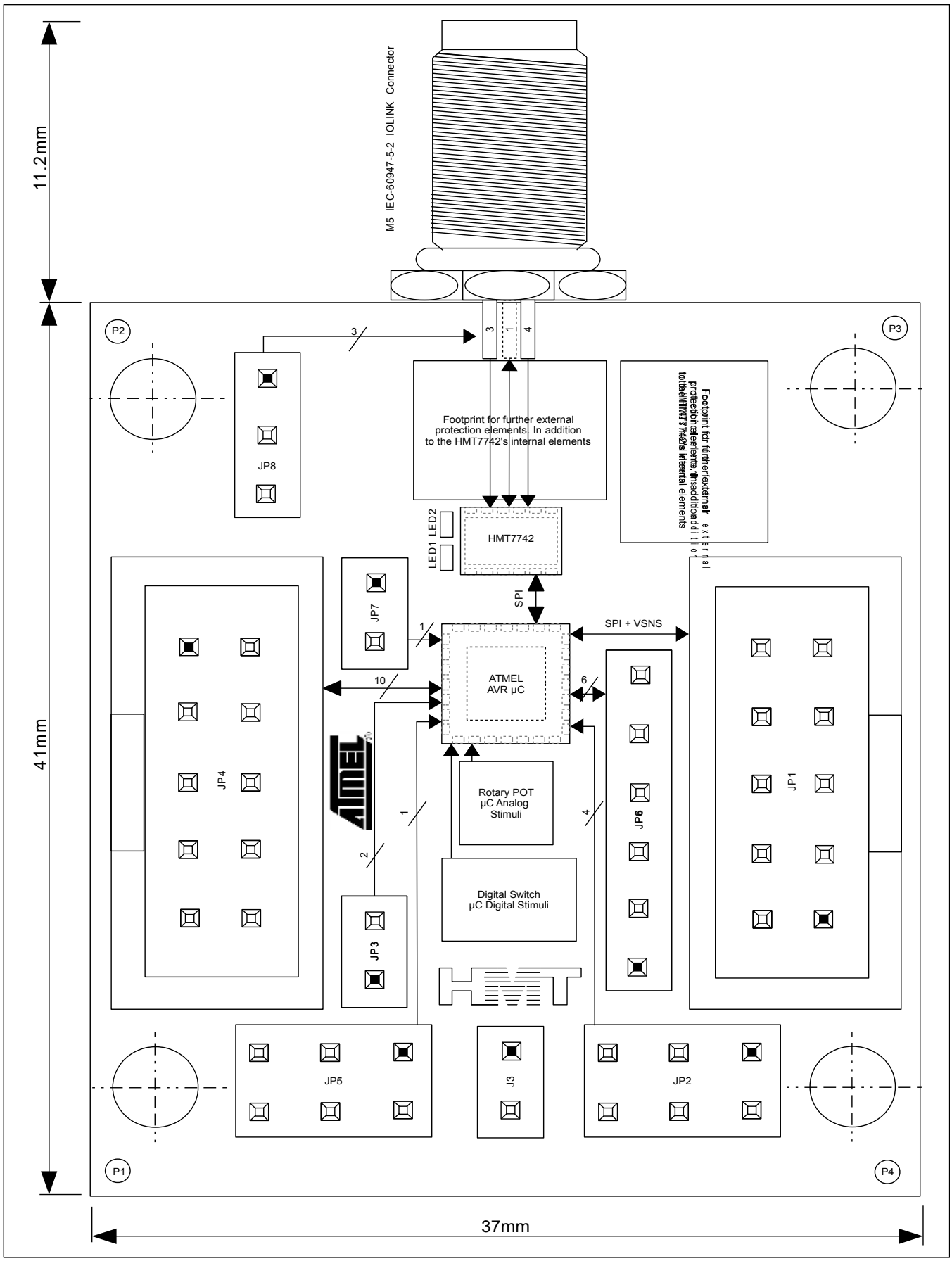

Fig. 1: TM96.1 (GENIE Explorer I) Variant B

Rev.:	Date:	Name:	Checked:		Project Number:	Project Name:	Scale:
Created:	31.01.12	R.D.Edgerley	Date:	Name:	TM96.1A/B	GENIE IO-LINK PHY SPECIFICATION	-
A	01.03.12	R.D.Edgerley					
B	30.07.14	R.D.Edgerley					
HMT microelectronic AG					Drawing Number: 5-SIS1-TM96.1-01	Rev: B	Page: 5/19

1.3.2 TM96.1 GEINE Explorer Variant A

TM96.1A is intended for testing in the smallest format, for demonstration and EMC testing. The component platform is a 4-layer, 1mm, standard FR4 PCB.

A block diagram of the TM96.1A test module can be seen in Fig. 2.The positioning of each block is consistent with the hardware layout and contains the following:

- ***HMT7742 GENIE IO-Link Device PHY in a DFN12L 3mm x 4mm package***
- ***ATmega328P 8-bit AVR microcontroller in a MLF32L 4mm x 4mm package †***
- ***2 x LED's [1 x Red, 1x green]***
- ***push button switch (digital stimulus)***
- ***rotary potentiometer (analog stimulus)***
- ***connection to IO-Link master over standard M5 cable***
- ***probe pads for microcontroller programming and test***

† The TM96.1A is populated with the ATmega328P per default, but may also be populated with the pin compatible ATtiny88 (ATtiny88 -MU [MLF Package]).

Illustration 2: TM96.1 GENIE Explorer I Variant A (Demonstrator)

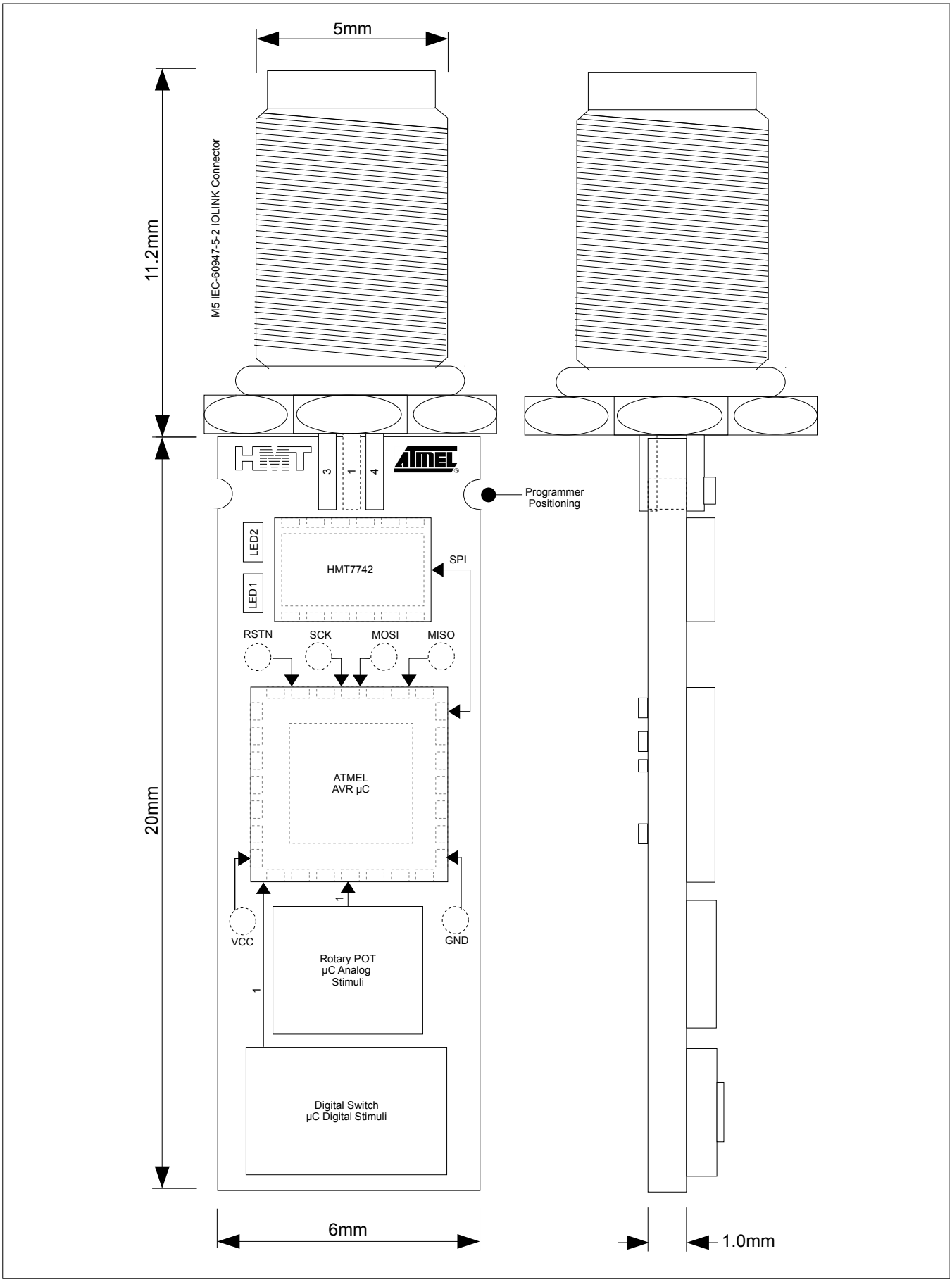

Fig. 2: TM96.1 (GENIE Explorer I) Variant A

Rev.:	Date:	Name:	Checked:		Project Number:	Project Name:	Scale:
Created:	31.01.12	R.D.Edgerley	Date:	Name:	TM96.1A/B	GENIE IO-LINK PHY SPECIFICATION	-
A	01.03.12	R.D.Edgerley					
B	30.07.14	R.D.Edgerley					
HMT microelectronic AG					Drawing Number: 5-SIS1-TM96.1-01	Rev: B	Page: 7/19

1.4 Descriptions

1.4.1 HMT7742 GENIE IO-Link Device PHY

Technical information on the HMT7742 GENIE IO-Link Device PHY may be found in reference [1].

1.4.2 Atmel AVR Microcontrollers

The TM96.1 test module can accept either the ATtiny88 (8kB flash) or the ATmega328P(32kB flash) microcontroller. Where these pin-outs are dissimilar, solder bridges are used in order to allow complete compatibility of both devices.

In order to support sensor applications where accurate A/D conversion is critical, filtering of the analogue supply has been implemented. For conversion, the ADC voltage reference should be set to the 1.1V internal VREF as shown in Table 1. Alternatively, if the external voltage reference pin is to be used (ATmega328P & Variant B only) then the capacitor C2 should be removed.

Bit 7:6 – REFS1:0: Reference Selection Bits in AVR microcontroller

REFS1	REFS0	Voltage Reference Selection
0	0	A_{REF}, internal V_{REF} switched off
0	1	A_{VCC} with external capacitor at A_{REF} pin
1	0	Reserved
1	1	Internal 1.1V voltage reference with external capacitor at A_{REF} pin

Table 1: Voltagte reference selections for ADC

Please refer to the appropriate microcontroller data sheet for more information.

1.4.3 Sensors

Both analogue and digital stimuli have been implemented on the the TM96.1 test module, in the form on a simple bush button switch and rotary potentiometer. More complex sensors may be used together with TM96.1 Variant B module via the JP4 and/or JP6 and JP7 connectors.

2 Interconnections

2.1 Power connections

Power to the HMT7742 GENIE IO-Link Device PHY is applied over the M5 IEC 60947-5-2 cable by an IO-Link master. The internal voltage regulator output from the HMT7742, VSNS, then supplies both the sensor and the microcontroller. This voltage is configurable to either 5 or 3.3V. Please refer to reference [1] for further information.

2.1.1 JP3 Microcontroller power & JTAG V_{REF} connector – Variant B

Where Atmel microcontrollers are to be programmed using the AVR JTAGICE mkII programming and debug tool, on the SPI interface (JP2), a separate microcontroller power and ground connection is implemented. This connection functions only to supply the microcontroller when programming, and to provide a reference voltage for the JTAGICE mkII programmer.

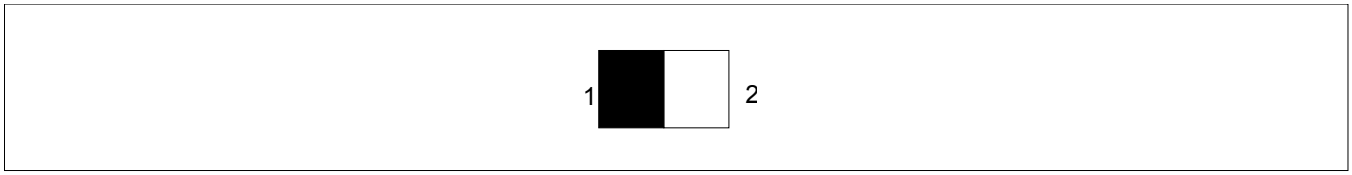

Fig. 3: JP3 Microcontroller power & AVR JTAGICE reference voltage

PIN	Signal	Comment	Pad	Signal	Comment
1	VCC	µC power, JTAG V_{REF}	2	GND	µC & JTAG ground

Table 2: JP3 Pin assignment

Do not connect both IO-LINK master supply and programming supply

2.1.2 JP7 ATmega328P external analog reference voltage AVREF

Fig. 4: JP7 External analog reference voltage for microcontroller analog I/P

PIN	Signal	Comment	Pad	Signal	Comment
1	AREF	Analog REF voltage	2	GND	Ground

Table 3: JP7 Pin assignment

2.2 External Connectors

2.2.1 JP1 10-pin SPI Connection to other-Atmel microcontrollers – Variant B

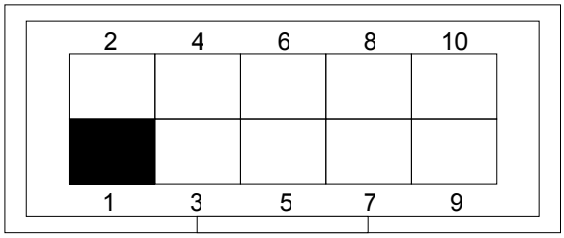

Fig. 5: JP1 10-pin SPI Connector to other-Atmel microcontrollers

Pin	Signal	Comment	Pin	Signal	Comment
1	GND	Ground	2	INT	Interrupt
3	GND	Ground	4	SCK	SPI Clock
5	GND	Ground	6	MISO	Master Input Slave Output
7	GND	Ground	8	MOSI	Master Output Slave Input
9	VSNS	µC and sensor supply	10	SS	Slave Select

Table 4: JP1 Pin assignment

2.2.2 JP4 10-pin Development connector I to spare microcontroller pins – Variant B

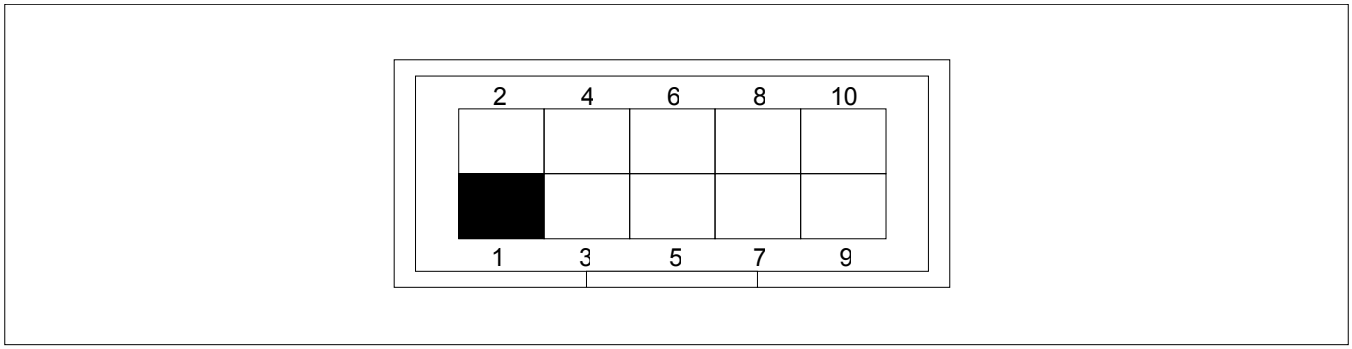

Fig. 6: JP4 10-pin development connector to spare microcontroller pins

Pin	Signal TM96	Signal ATtiny88	Signal ATmega328P	Pin	Signal TM96	Signal ATtiny88	Signal ATmega328P
1	SPA0	PINPA0(ADC6/PCINT24)	ADC6	2	SPA1	PC1(ADC1/PCINT9)	PC1(ADC1/PCINT9)
3	SPA2	PC2(ADC2/PCINT10)	PC2(ADC2/PCINT10)	4	SPA3	PC3(ADC3/PCINT11)	PC3(ADC1/PCINT11
5	SPA4	PC4(ADC4/SDA/PCINT12)	PC4(ADC4/SDA/PCINT12)	6	SPA5	PC5(ADC5/SCL/PCINT13	PC5(ADC5/SCL/PCINT13
7	SPD0	PD0(PCINT16)	PD0(RXD/PCINT16)	8	SPD1	PD1(PCINT17)	PD1(TXD/PCINT17)
9	SPD3	PD3(INT1/PCINT19)	PD3(PCINT19/OC2B/INT1)	10	CLKI	PB6(CLKI/PCINT6)	PB6(OSC1/XTAL1/PCINT6)

Table 5:JP4 Pin assignment

2.2.3 6-pin Development connector II to spare microcontroller pins – Variant B

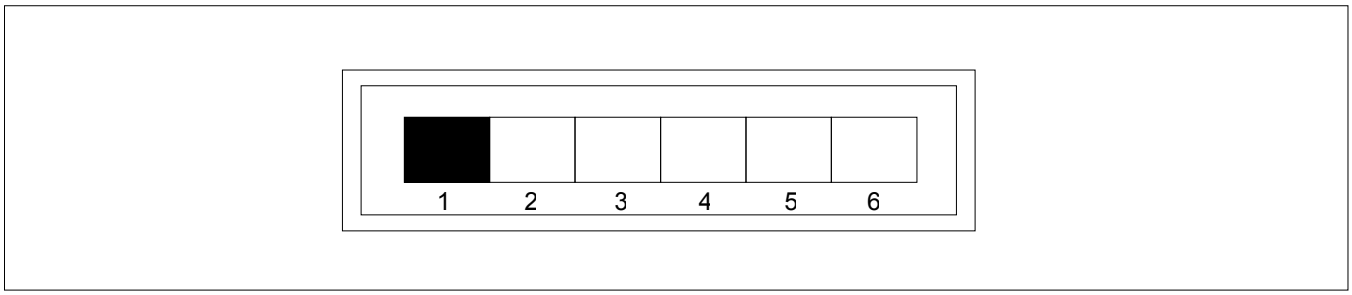

Fig. 7: JP6 6-pin development connector to spare microcontroller pins

Pin	Signal TM96	Signal ATtiny88	Signal ATmega328P	Pin	Signal TM96	Signal ATtiny88	Signal ATmega328P
1	SPD4	PD4(T0/PCINT20)	PD4(T0/OSC2B/PCINT19)	2	SPD5	PD5(T1/PCINT21)	PD5(T1(OS0B/PCINT21)
3	SPD6	PD6(AIN0/PCINT22)	PD6(AIN0/OC0A/PCINT22)	4	SPD7	PD7(AIN1/PCINT23)	PD7((AIN1/PCINT23)
5	SPD8	PB0(ICP1/CLK0/PCINT0)	PB0(ICP1/CLK0/PCINT0)	6	SPD9	PB1(OC1A/PCINT1)	PB1(OC1A/PCINT1)

Table 6: JP6 pin assignment

2.2.4 I1 IEC 60947-5-2 M5 IO-Link Connector

Fig. 8 shows the standard slave/master interface connector for IO-Link. The pin assignment for this connector may be seen in Table 7. The M5 variant of this connector is used to keep the PCB board size to a minimum.

NOTE: The IO-Link plug is female on the master and male on the slave

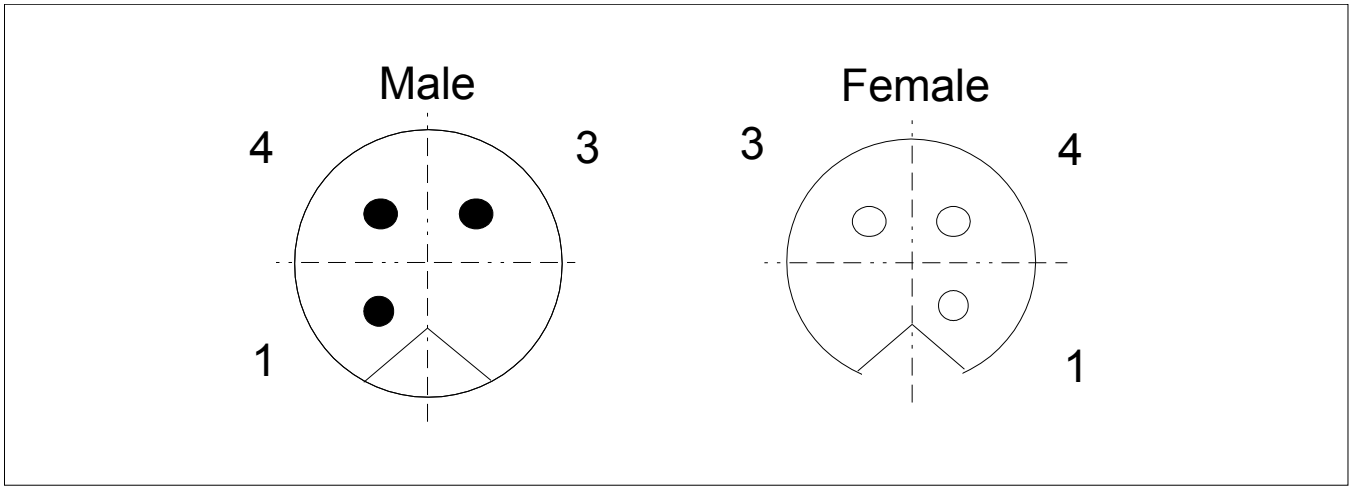

Fig. 8: I1 IEC 60947-5-2 M5 IO-Link cable connector, front view

Pin	Signal	Comment	Pin	Signal	Comment
1	L+	Power Supply	-	-	-
3	L-	Ground	4	C/Q	SIO/SDCI

Table 7: I1 Pin assignment

2.2.5 JP8 IO-Link connector access points (L+, C/Q, L-) - TM96.1B

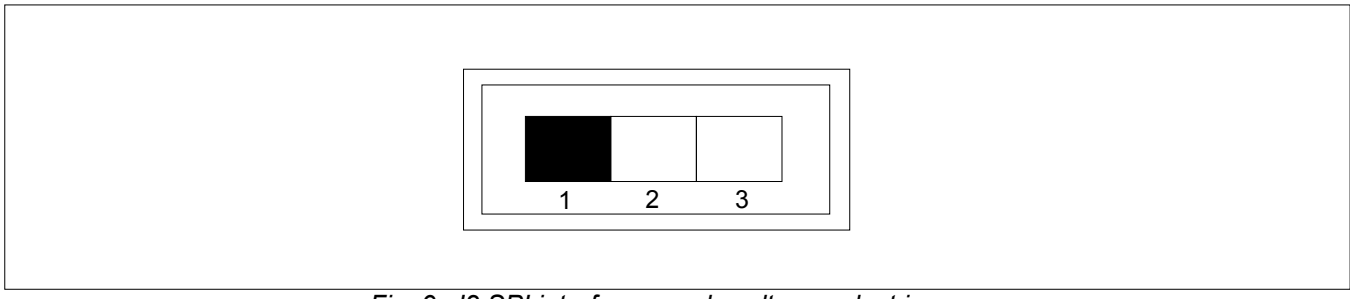

Fig. 9: J2 SPI interface supply voltage select jumper

PIN	Signal	Comment	Pad	Signal	Comment
1	L+	VPLUS on HMT7742	2	C/Q	Communication channel
3	L-	PGND on HMT7742	-	-	-

2.2.6 P1-P6 Microcontroller programming – TM96.1A

The TM96.1 Variant A is not intended for customer programming, as programming will erase the pre-installed IO-Link protocol stack and demo application. However, should the customer wish, the microcontroller may be re-programmed with an alternative application via the probing pads on the PCB. These probing pads are located on the underside of the PCB, close to the microcontroller with approximately 1.27mm of separation. See Fig. 10. The pad assignments, along with their corresponding coordinates may be found in tables 8 & 9 respectively.

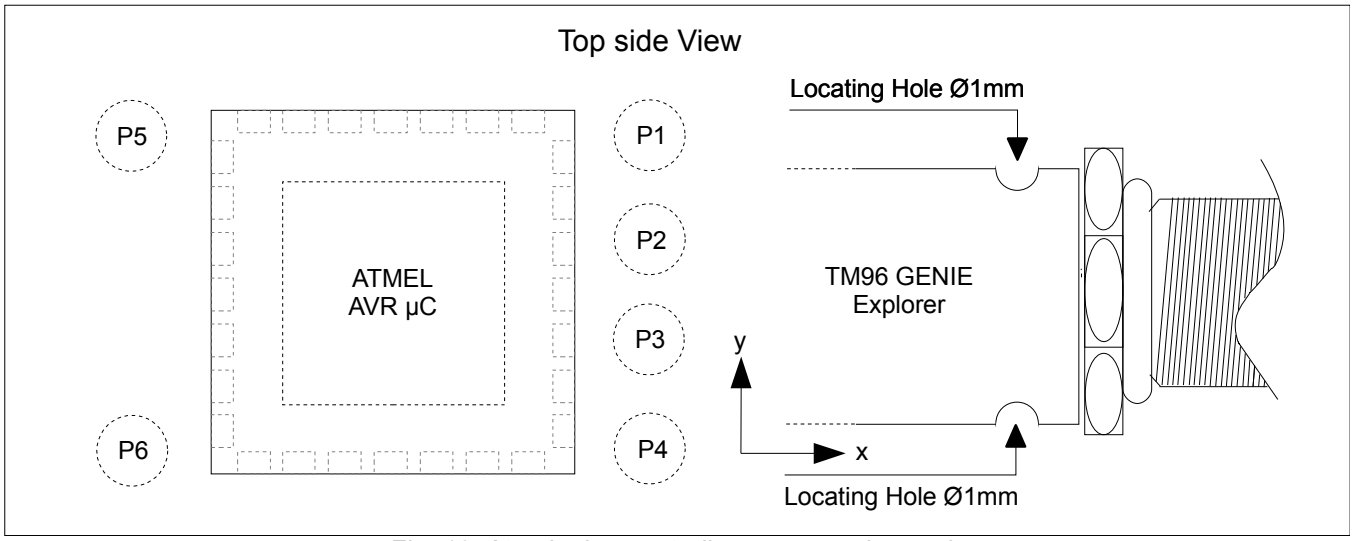

Fig. 10: Atmel microcontroller programming pads

Pad	Signal	Comment	Pad	Signal	Comment
P1	RSTn	µC reset	P2	SCK	SPI Clock
P3	MOSI	Master Out Slave In	P4	MISO	Master In Slave Out
P5	VCC	µC power	P6	GND	µC ground

Table 8: P1-P6 Pad assignment

Pin Name	Pin Number	PCB Layer	X_Coord. [mm]	Y_Coord. [mm]
RSTn	P1	bottom	12.8	5.2
SCK	P2	bottom	12.8	3.7
MOSI	P3	bottom	12.8	2.2
MISO	P4	bottom	12.8	0.7
VCC	P5	bottom	6.4	5.2
GND	P6	bottom	6.4	0.6

Table 9: P1-P6 Pad coordinates

2.2.7 JP2 Interface connector to Atmel AVR ISP programmer – Variant B

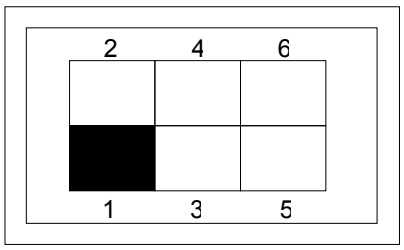

Fig. 11: JP2 Atmel AVR ISP programming interface

Pad	Signal	Comment	Pad	Signal	Comment
1	MISO_uC	Master Out Slave In	2	VCC	Programmer V_{REF}
3	SCK	SPI Clock	4	MOSI	Master Out Slave In
5	RESET	Debug	6	GND	Programmer GND

Table 10: JP2 Pin assignment

2.2.8 JP5 Microcontroller debug connector – Variant B

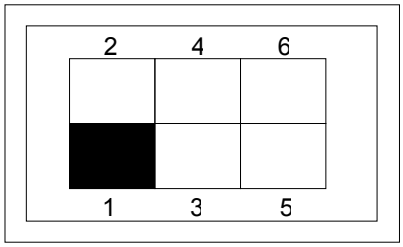

Fig. 12: JP5 Microcontroller debug

Pad	Signal	Comment	Pad	Signal	Comment
1	N/C	Not connected	2	VCC	Programmer V_{REF}
3	N/C	Not connected	4	N/C	Not connected
5	RESET	Debug	6	GND	Programmer GND

Table 11: JP5 Pin assignment

2.3 Other Connections – Variant A

Pad	Signal	Comment	Location	Size
E1	ESD Ground	Not Connected	Bottom Layer	2mm x 4mm

Table 12: Other connections TM96.1A

2.4 Other Connections – Variant B

2.4.1 J3 R_{WAKE} enable jumper

Fig. 13: J3 R_{WAKE} enable jumper for V_{SNS} start-up level

PIN	Signal	Comment	Pad	Signal	Comment
1	SS	Slave-select	2	R_{WAKE}	Connection to 10k R_{WAKE} pull-down

Table 13: JP7 Pin assignment

Remove R_{WAKE} before programming over JTAG ICE

2.4.2 Ground pins

Probe	Signal	Comment	Probe	Signal	Comment
P1	GND	Oscilloscope GND	P2	GND	Oscilloscope GND
P3	GND	Oscilloscope GND	P4	GND	Oscilloscope GND

Table 14 GND pinsTM96.1B

3 Programming & Debug Sequence – Variant B

3.1 SPI access to AVR

In order to program the microcontroller, please follow the programming procedure below.

[1] Remove R_{WAKE} enable jumper (J3)

[2] Connect IO-Link master via I1 M5 connector

- alternatively, supply the TM96.1B board via connector JP3

[3] Connect microcontroller programming hardware [AVR JTAGICE mkII], (JP2)

[4] Program microcontroller (JP2)

[5] Remove programming hardware (JP2)

3.2 Debug access to AVR

In order to set the debug access to the AVR microcontroller via the reset pin, the appropriate fuses must be blown after programming of the AVR is complete. Further information on how to do this may be found in references 2] . A dedicated connector on the TM96.1B, JP5, provides direct access to the reset pin, along with the required programmer reference voltage.

Note: when using the dedicated debug connector, JP5, the programmer and the IO-Link master may be connected simultaneously in this case.

4 Transparent Mode

The HMT7742 supports a mode for transparent communication of UART frames. In this mode, the frames are received and transmitted from a UART peripheral in the microcontroller, and the function of the PHY device is reduced to that of a physical level converter. This mode is supported by dual use of the MOSI and MISO pins, maintaining the low overall pin-count and a restricted use of microcontroller resources. For further information please refer to reference [1].

4.1 Transparent Mode enable jumpers

If transparent mode is requested, then resistors R5 and R6 should be present. Note: This feature is supported by the TM96.1B development module only.

5 Application Examples

5.1 TM96.1A – IO-Link Demonstrator & EMC

Fig. 14 Shows a TM96.1A module running the HMT IO-Link Mini-stack and demo application on an Atmel AVR microcontroller.

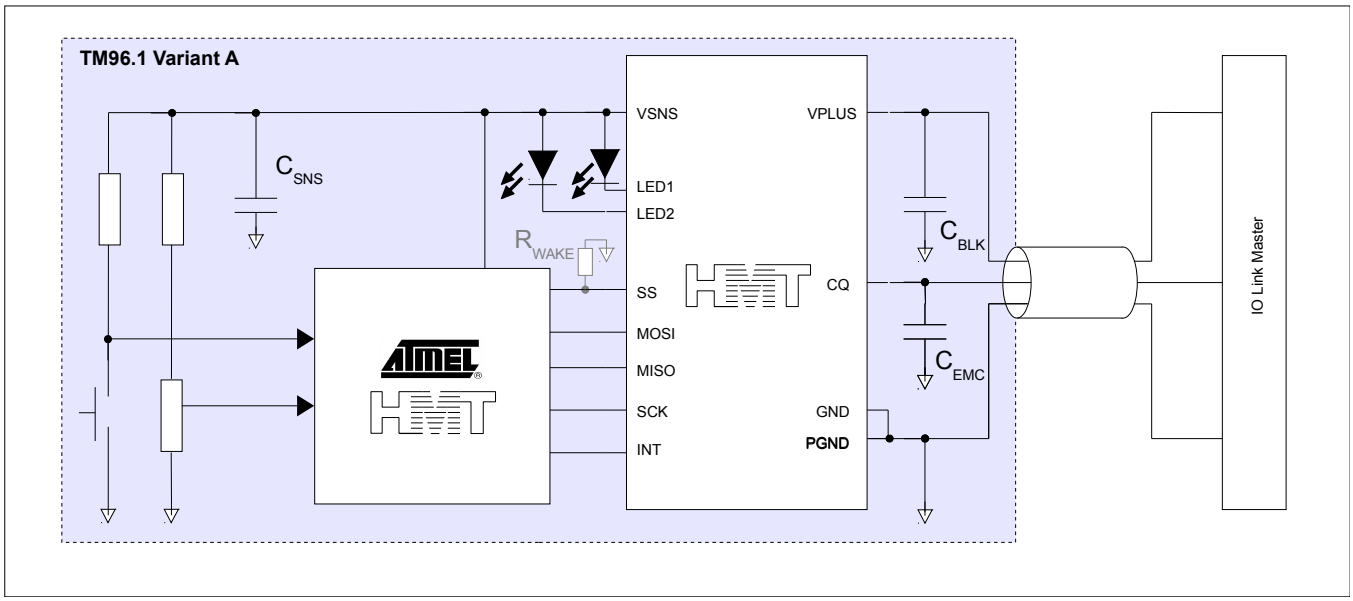

Fig. 14: HMT7742 + Atmel µC + HMT IO-Link Mini-stack and demo-application

5.2 TM96.1B – IO-Link sensor/actuator application development platform

Fig. 15 Illustrates how a customer hardware/software applications may be developed by introducing application specific sensors and/or further microcontrollers together with the HMT IO-Link Mini-stack and demo application.

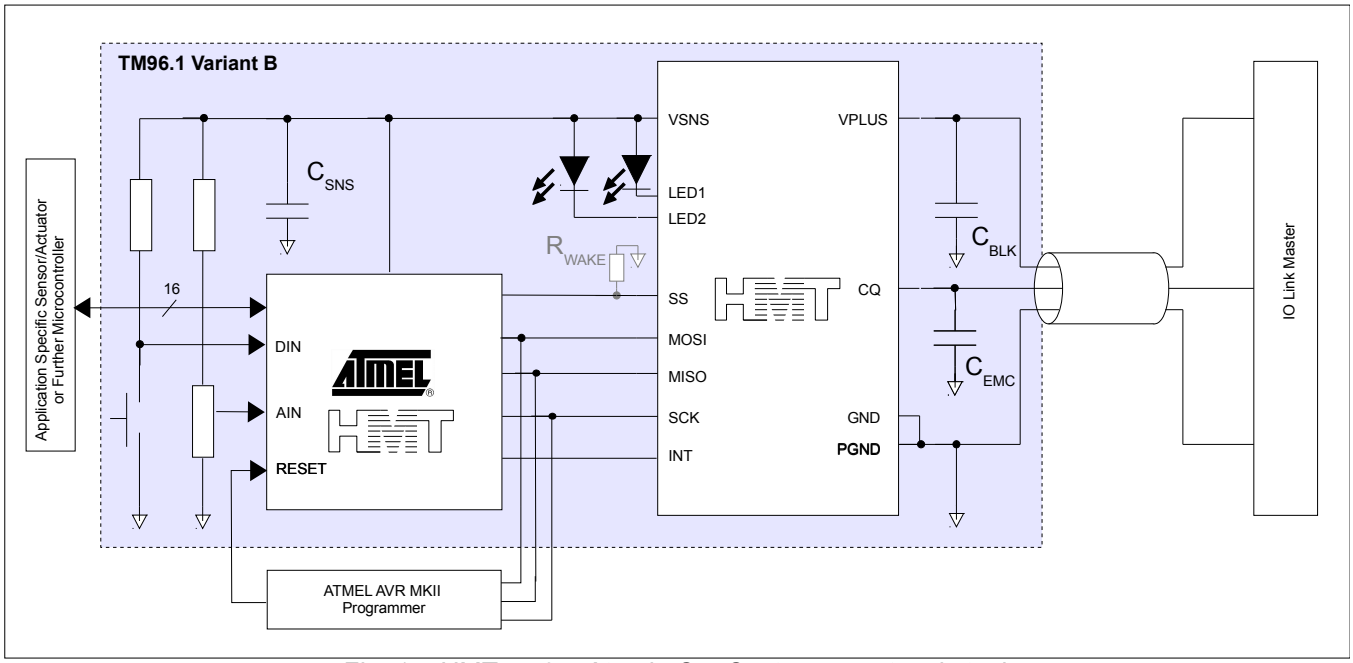

Fig. 15: HMT7742 + Atmel µC + Customer protocol stack

5.3 TM96.1B – IO-Link stack development platform

Fig. 16 Illustrates how an Atmel microcontroller may be programmed with a customer specific IO-Link protocol stack using an Atmel AVR MKII programmer.

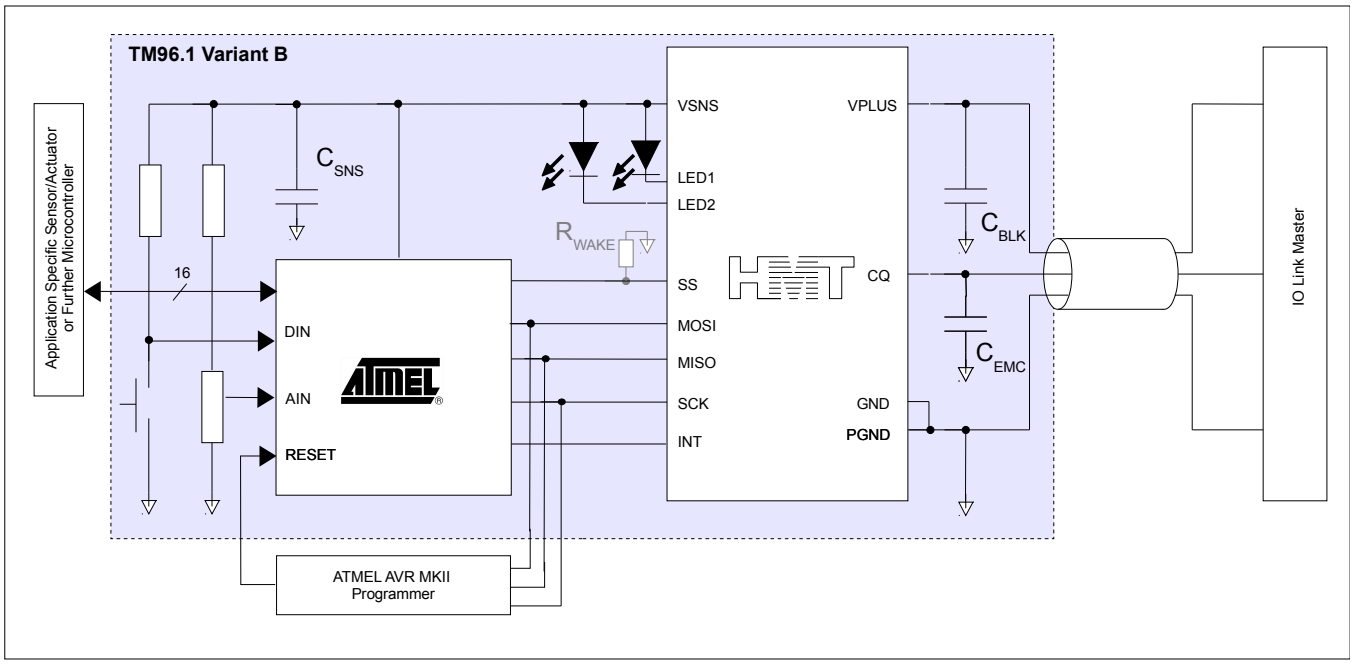

Fig. 16: HMT7742 + Atmel µC + Customer protocol stack and application

5.4 TM96.1B – Choice of Microcontroller

Fig. 17 Illustrates how alternative Atmel microcontrollers may be connected to the HMT7742 by piggy back connector via the SPI interface socket.

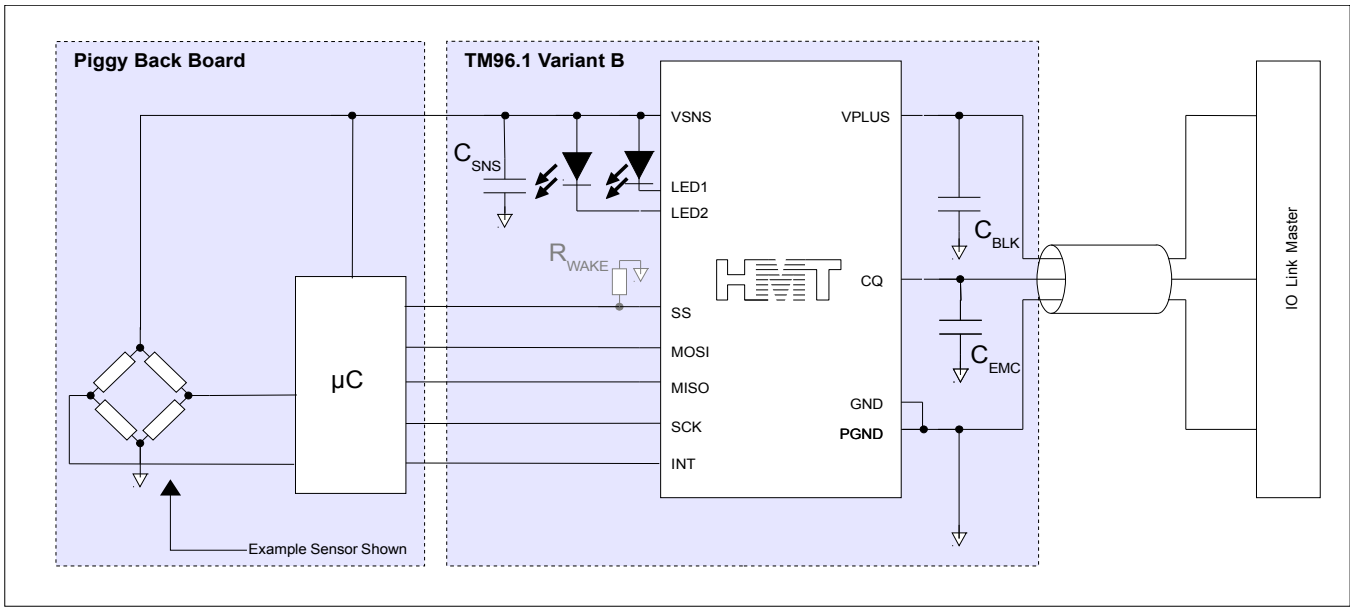

Fig. 17: HMT7742 + External µC

5.5 Piggy back connector for other Atmel microcontroller development

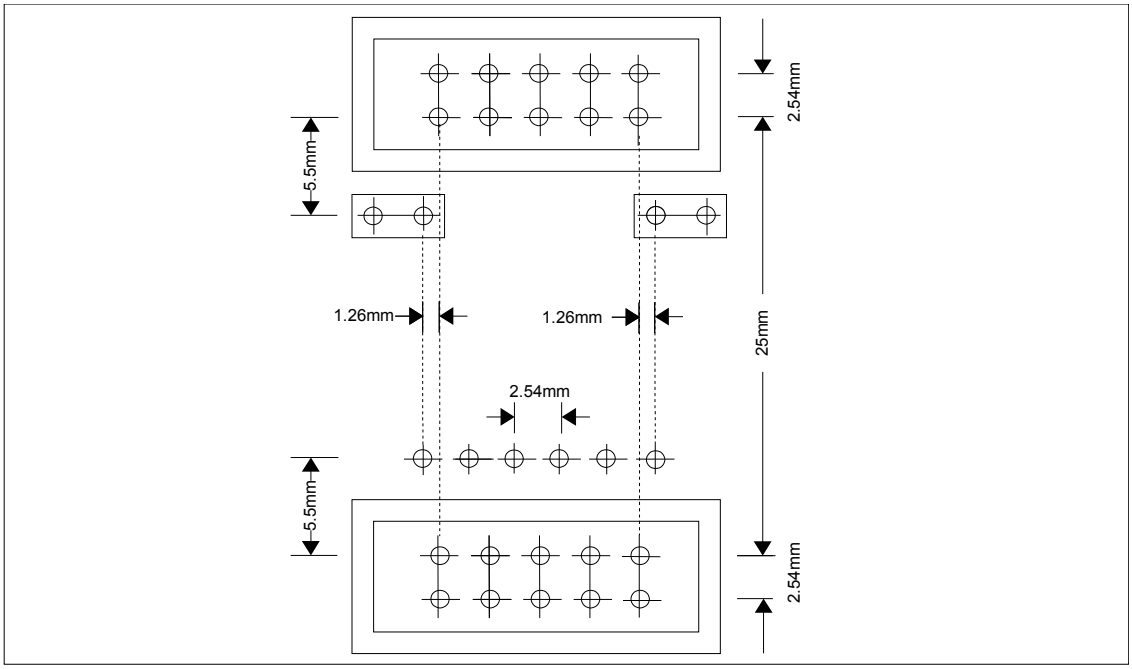

Fig. 18: Piggy-back connector dimensioning

6 IO-Link IEC60947-5-2 M5 Mounting

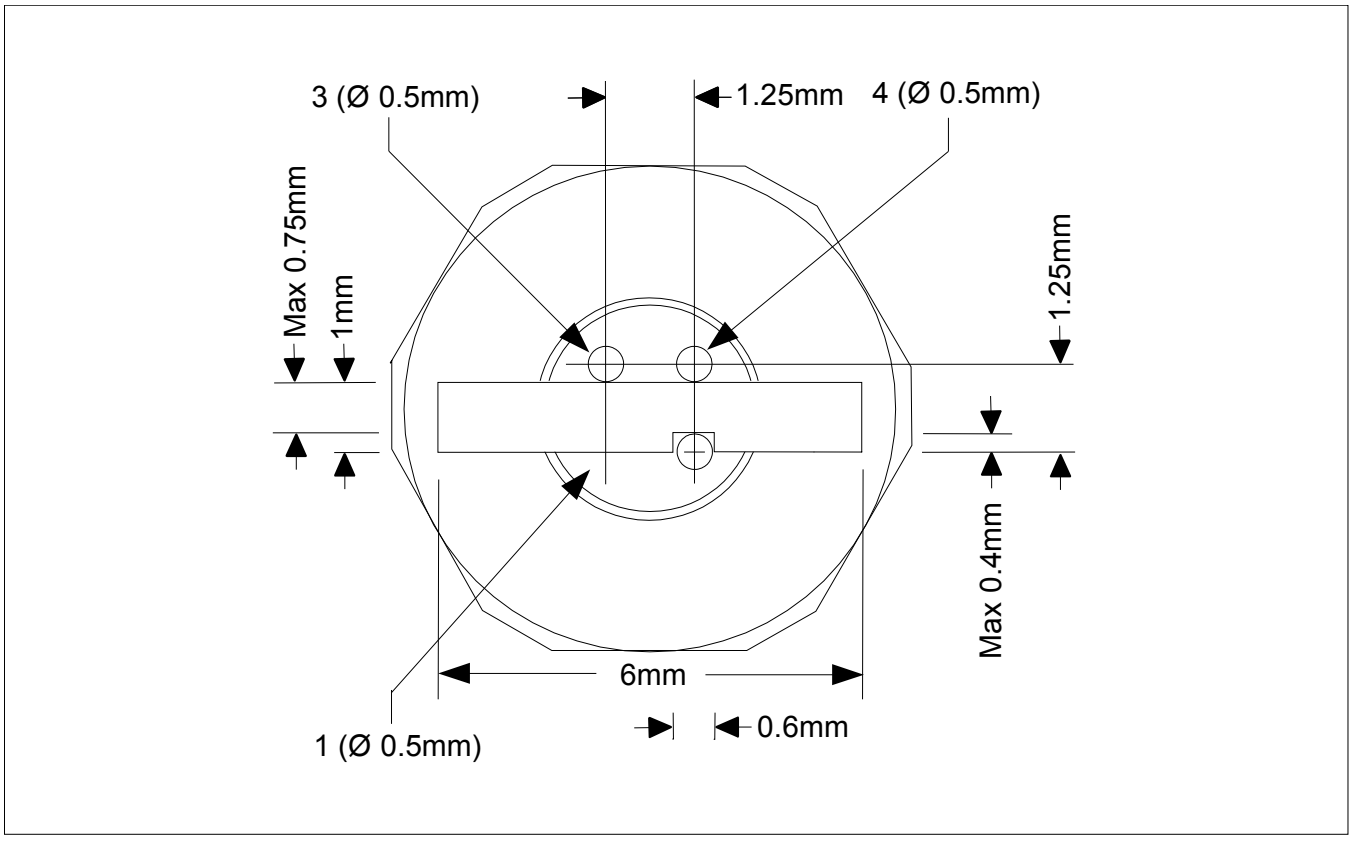

Fig. 19: IEC-60947-5-2 Mounting to TM96.1 GENIE Explorer I VARIANT A

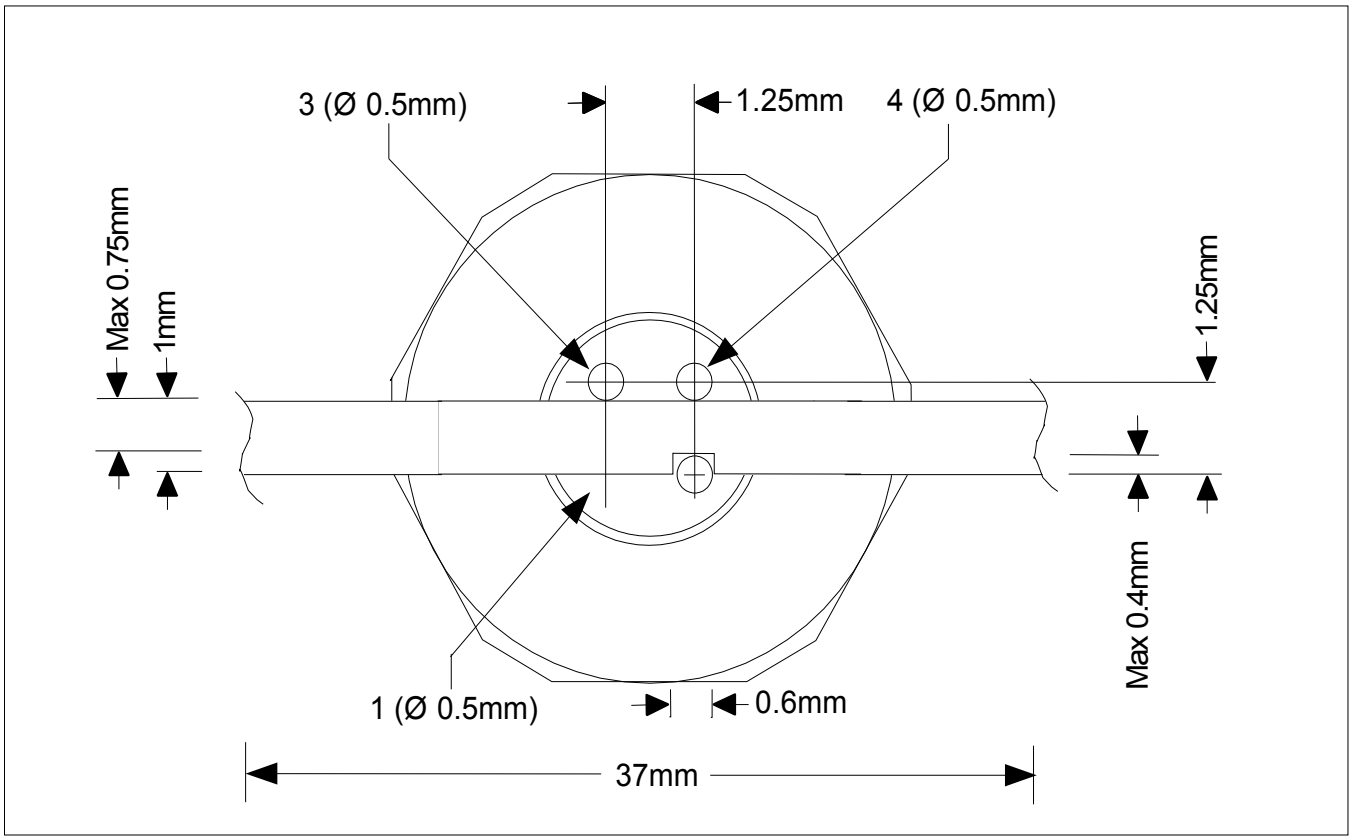

Fig. 20: IEC-60947-5-2 Mounting to TM96.1 GENIE Explorer I VARIANT B

7 Technical Data

7.1 Remarks

- All values refer to GND unless otherwise specified
- Operation of the module above the absolute maximum rating may lead to instantaneous device failure.
- Operation of the module between the operating rating and the absolute maximum rating leads to a reduced operating lifetime.

7.2 Absolute Maximum Ratings

Parameter	Commet	Min.	Typ.	Max.	Unit
HMT7742					
Pin voltage	VPLUS	-40		40	V
Pin voltage	CQ	-40		40	V
Pin voltage	PGND	Shorted on the board to GND			
Atmel ATMega328P & ATtiny88 Microcontrollers					
Pin voltage	VCC	1.8		5.5	V

Table 15: Absolute maximum ratings

7.3 Operating Parameters

	Min.	Typ.	Max.	Unit
HMT7742 GENIE IO-Link Device PHY				
VPLUS supply voltage, VSNS = 3.3V, ISNS = 50mA	5	24	30	V
VPLUS supply voltage, VSNS = 5V, ISNS = 50mA	7	24	30	V
Blocking capacitor on VPLUS, C_{BLK}	100			nF
Maximum load capacitor, C_{LOAD_CQ}			200	nF
EMC capacitor on CQ	470pF			
Atmel Microcontroller				
Supply voltage (supplied externally), no IO-Link master	1.8		5.5	V

Table 16: Operating parameters

7.4 Electrical Parameters

Parameter	Comment	Min.	Typ.	Max.	Unit
Analogue I/P [Potentiometer]					
Pin voltage	VSNS = 3.3V	0		0.66	V
Pin voltage	VSNS = 5.0V	0		1.1	V
Current	VSNS = 3.3V	220		330	µA
Current	VSNS = 5.0V	333		500	µA
Digital I/P [Push button switch]					
Pin voltage	VSNS = 3.3V	0		3.3	V
Pin voltage	VSNS = 5.0V	0		5	V
Current	VSNS = 3.3V			700	µA
Current	VSNS = 5.0V			1.06	mA

Table 17: Electrical parameters

8 Microcontroller Part Numbers

- ATmega328P [MLF Package]