

Όνομα : Στέφανος Τζαφέρης

ΑΜ : 1115202200183

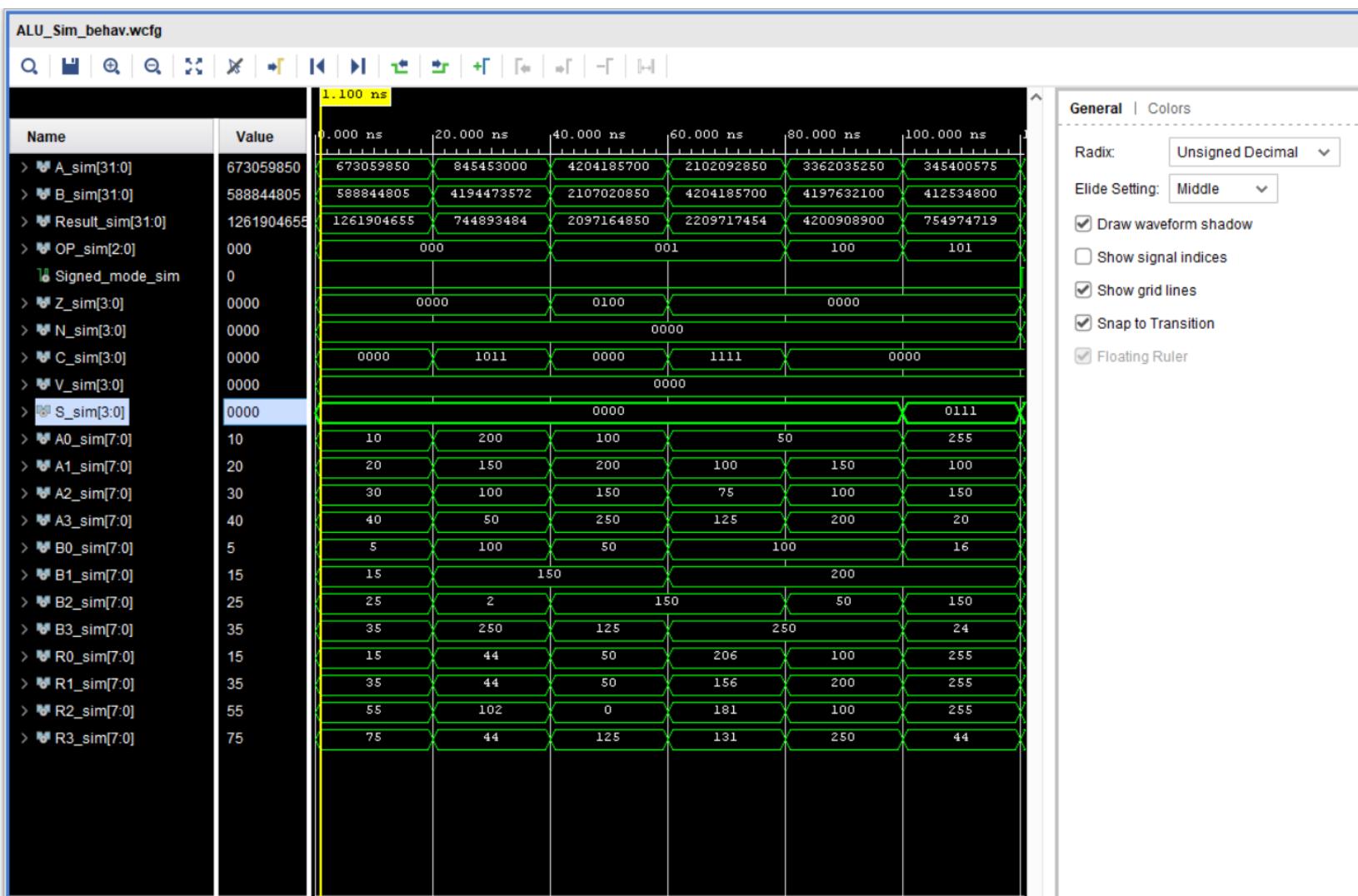
Εργασία 1

Ερώτημα 3_1 :

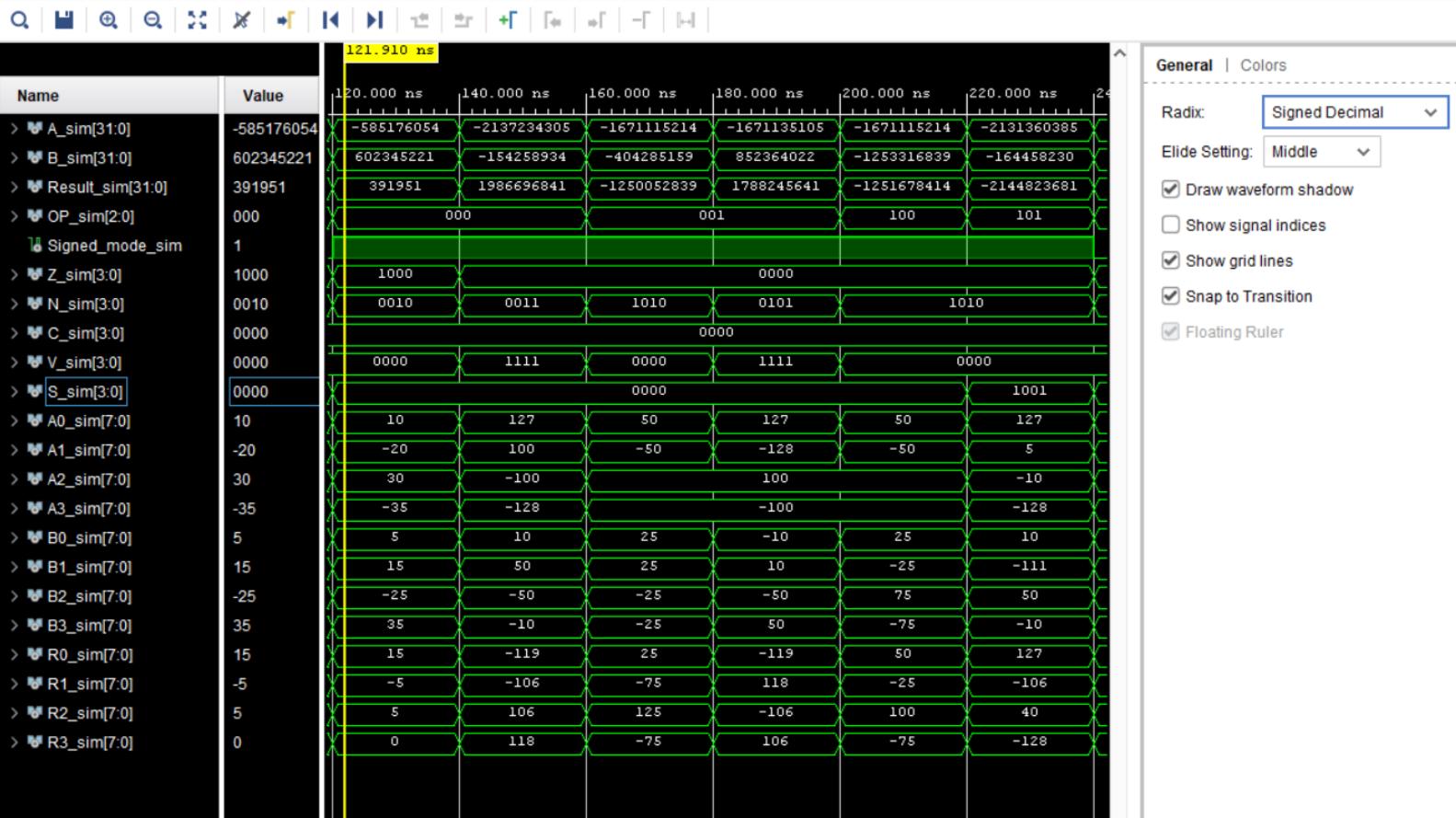
Behavioral and Post synthesis timing Simulation:

*Στον κώδικα της προσομοίωσης γράφω σε σχόλια τα αναμενόμενα αποτελέσματα και τα αναμενόμενα flags.

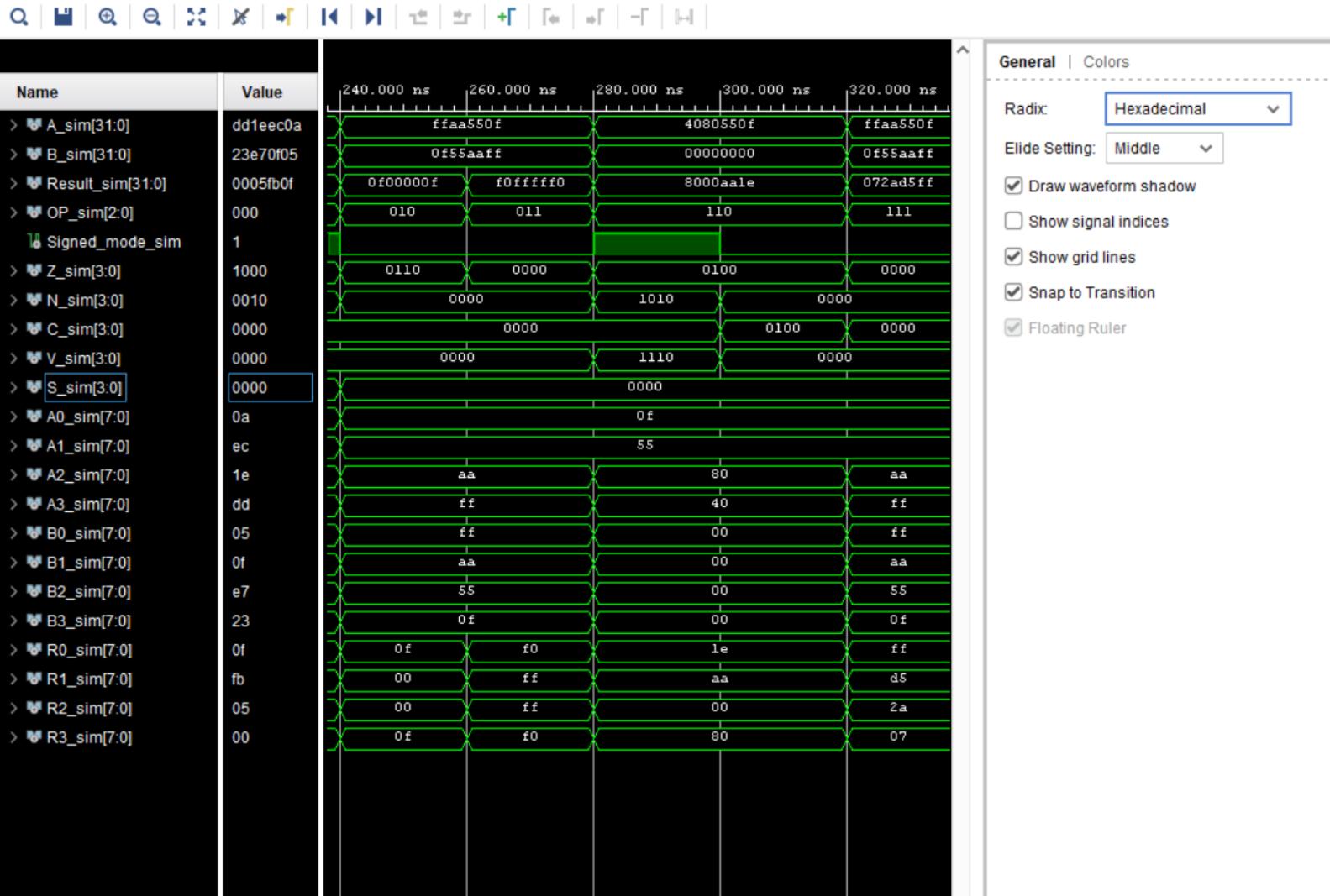
** Η πρώτη φωτογραφία είναι με radix decimal unsigned (γίνονται όλες οι unsigned δοκιμές μαζί), μετά όλες οι signed δοκιμές μαζί και στην 3^η φωτογραφία είναι όσες έχουν να κάνουν με πράξεις bit οπότε για ευκολία το θέτω σε 16αδικό.

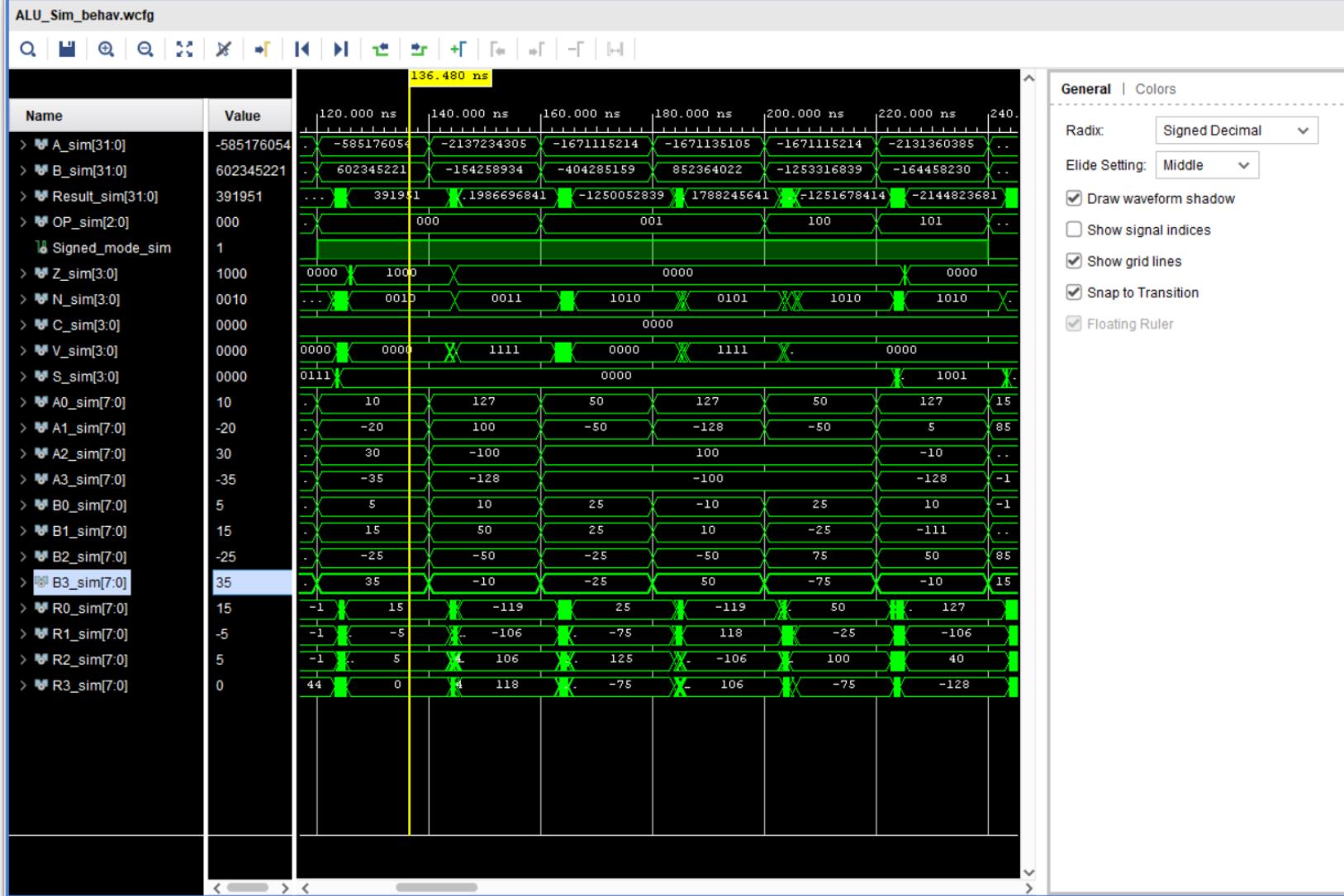
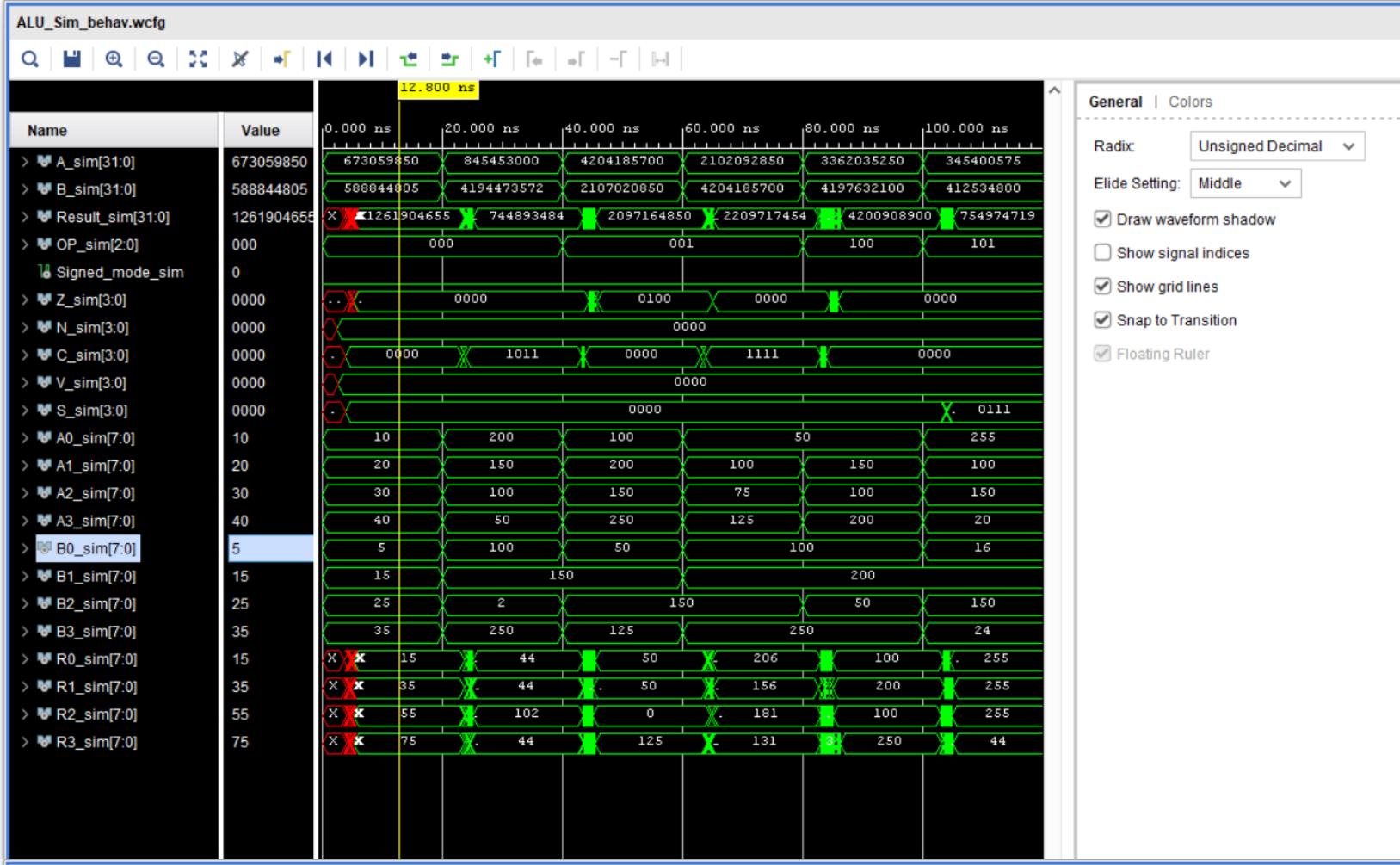


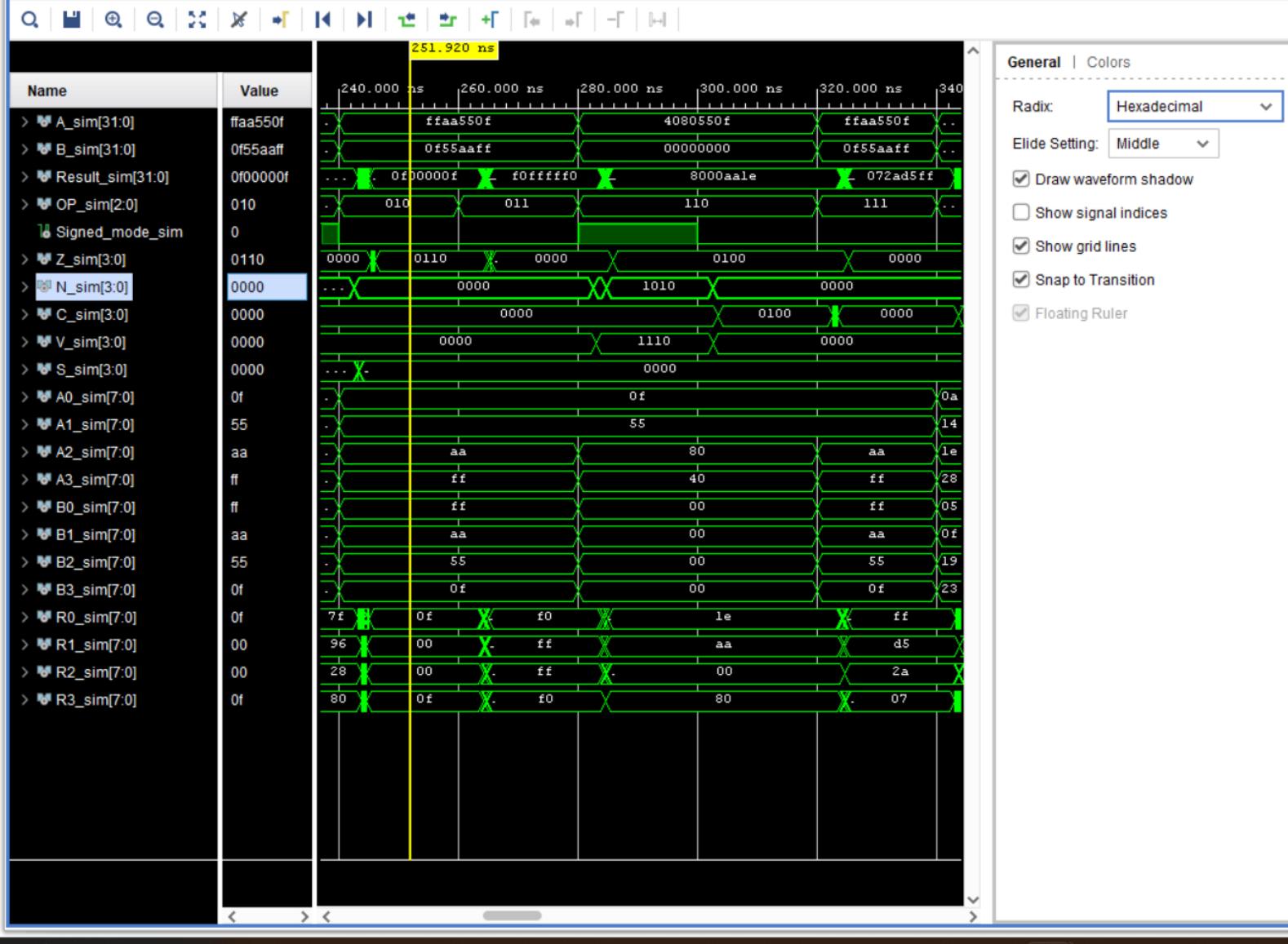
ALU_Sim_behav.wcfg



ALU_Sim_behav.wcfg







DET - BOS
Βαθμολογία παι..



Οι 3 τελευταίες φωτογραφίες αφορούν Post synthesis timing Simulation

Ερώτημα 3_2 :

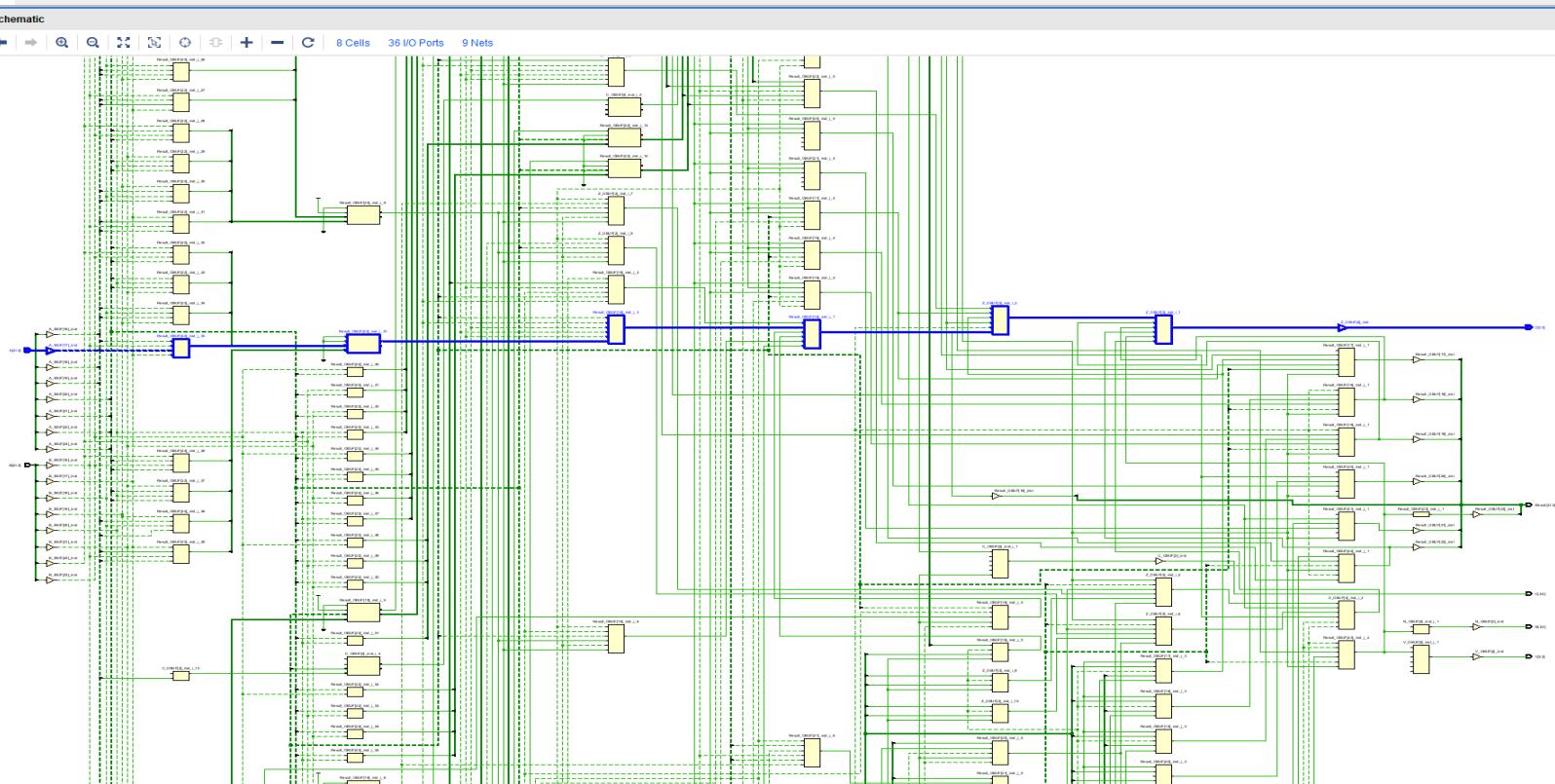
Καθυστέρηση διάδοσης:

Είναι το Path 11 –το πιο αργό (απομονωμένο και σε ολόκληρο το synthesized device)

The screenshot shows the Vivado 2022.2 interface with the following details:

- Left Sidebar:** Contains sections for SIMULATION, RTL ANALYSIS, SYNTHESIS, and IMPLEMENTATION.
- Synthesis Project:** "SYNTHESIZED DESIGN - xc7z020csg484-1".
- Path Properties (Path 11):** Summary table showing:
 - Name: Path 11
 - Slack: ∞ ns
 - Source: A[17] (input port)
 - Destination: Z[2] (output port)
 - Path Group: (none)
 - Path Type: Max at Slow Process Corner
 - Requirement: ∞ ns
 - Data P.. Delay: 9.821ns (logic 4.728ns (48.13%) route 5. Logic Levels 8 (CARRY4=1 IBUF=1 LUT4=1 LUT6=4 OE=1))
- Schematic View:** Shows the logic path from A[17] through various IBUF, LUT4, LUT6, and OBIF blocks to Z[2].
- Timing Analysis:** Timing Checks - Setup table showing:

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exception	Clock
Path 11	∞	8	8	25	A[17]	Z[2]	9.821	4.728	5.093	48.1	51.9	∞	input port clock			
Path 12	∞	8	8	25	A[25]	Z[3]	9.796	4.728	5.068	48.3	51.7	∞	input port clock			
Path 13	∞	8	8	25	A[9]	Z[1]	9.791	4.728	5.063	48.3	51.7	∞	input port clock			
Path 14	∞	8	8	15	B[0]	Z[0]	9.787	4.720	5.067	48.2	51.8	∞	input port clock			
Path 15	∞	8	8	25	A[9]	N[1]	9.139	4.728	4.411	51.7	48.3	∞	input port clock			
Path 16	∞	8	8	25	A[9]	V[1]	9.139	4.728	4.411	51.7	48.3	∞	input port clock			
Path 17	∞	8	8	25	A[17]	N[2]	9.134	4.728	4.406	51.8	48.2	∞	input port clock			
Path 18	∞	8	8	25	A[17]	Result[23]	9.134	4.728	4.406	51.8	48.2	∞	input port clock			



Καθυστέρηση μόλυνσης:

Όλα τα paths από 1-10 έχουν την ίδια ελάχιστη καθυστέρηση.

ALU - [C:/Users/stzaf/Projects/Vivado/Sxfiakwn_Syftmatwn/ALU/ALU.xpr] - Vivado 2022.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

SYNTHESIZED DESIGN - xc7z020csg484-1

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design
- Constraints Wizard
- Edit Timing Constraints
- Set Up Debug
- Report Timing Summary
- Report Clock Networks
- Report Clock Interaction
- Report Methodology
- Report DRC
- Report Noise
- Report Utilization
- Report Power
- Schematic

Netlist Path Properties

SYNTHESIZED DESIGN - xc7z020csg484-1

Project Summary Path 1 - timing_1 Schematic

Nets (1220) Leaf Cells (791)

- A_IBUF[0]_inst (IBUF)
- A_IBUF[1]_inst (IBUF)
- A_IBUF[2]_inst (IBUF)
- A_IBUF[3]_inst (IBUF)
- A_IBUF[4]_inst (IBUF)
- A_IBUF[5]_inst (IBUF)
- A_IBUF[6]_inst (IBUF)
- A_IBUF[7]_inst (IBUF)
- A_IBUF[8]_inst (IBUF)
- A_IBUF[9]_inst (IBUF)
- A_IBUF[10]_inst (IBUF)
- A_IBUF[11]_inst (IBUF)
- A_IBUF[12]_inst (IBUF)
- A_IBUF[13]_inst (IBUF)
- A_IBUF[14]_inst (IBUF)

IBUF A[31:0] I O C[3:0]

C_OBUF[0]_inst_i_1 LUT6

OBUF C[3:0]

Tcl Console Messages Log Reports Design Runs Timing

Timing Checks - Hold

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exception	Skew	Clock
Path 1	∞	3	4	20	A[7]	C[0]	1.971	1.297	0.674	65.8	34.2	- ∞	input port clock				
Path 2	∞	3	4	22	A[15]	C[1]	1.971	1.297	0.674	65.8	34.2	- ∞	input port clock				
Path 3	∞	3	4	22	A[23]	C[2]	1.971	1.297	0.674	65.8	34.2	- ∞	input port clock				
Path 4	∞	3	4	22	A[31]	C[3]	1.971	1.297	0.674	65.8	34.2	- ∞	input port clock				
Path 5	∞	3	4	72	Signed_mode[N 0]	N[1]	1.971	1.297	0.674	65.8	34.2	- ∞	input port clock				
Path 6	∞	3	4	72	Signed_mode[N 1]	N[2]	1.971	1.297	0.674	65.8	34.2	- ∞	input port clock				
Path 7	∞	3	4	72	Signed_mode[N 2]		1.971	1.297	0.674	65.8	34.2	- ∞	input port clock				
Path 8	∞	3	4	24	A[0]	Result[0]	1.971	1.297	0.674	65.8	34.2	- ∞	input port clock				
Path 9	∞	3	4	26	A[10]	Result[10]	1.971	1.297	0.674	65.8	34.2	- ∞	input port clock				
Path 10	∞	3	4	26	A[11]	Result[11]	1.971	1.297	0.674	65.8	34.2	- ∞	input port clock				

Report Timing - timing_1

21/25 17°C Εντονες νεφώσεις. ENG 11/27/2025

