Όνομα : *Στέφανος Τζαφέρης*

ΑΜ : *1115202200183*

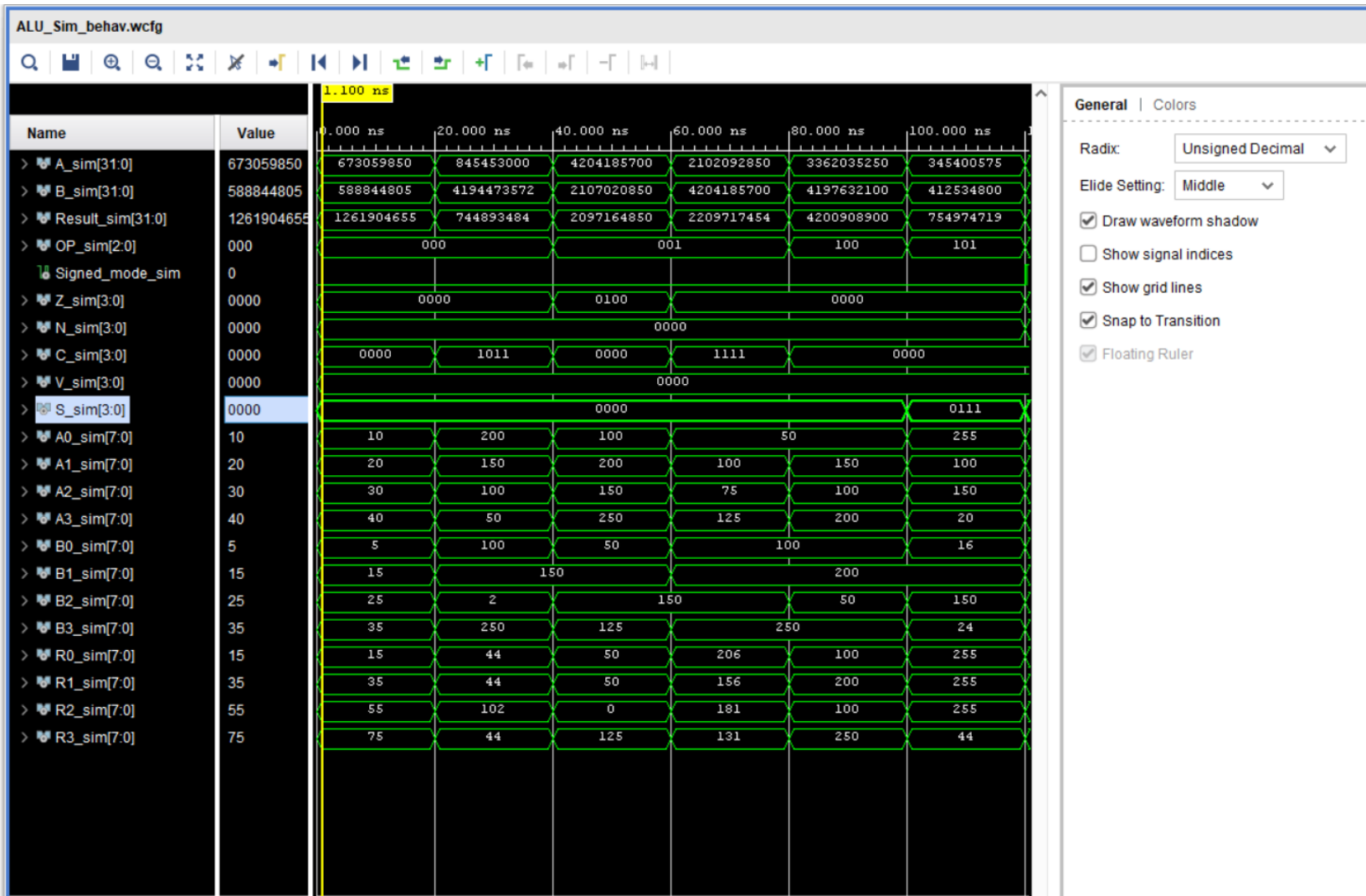
Εργασία 1

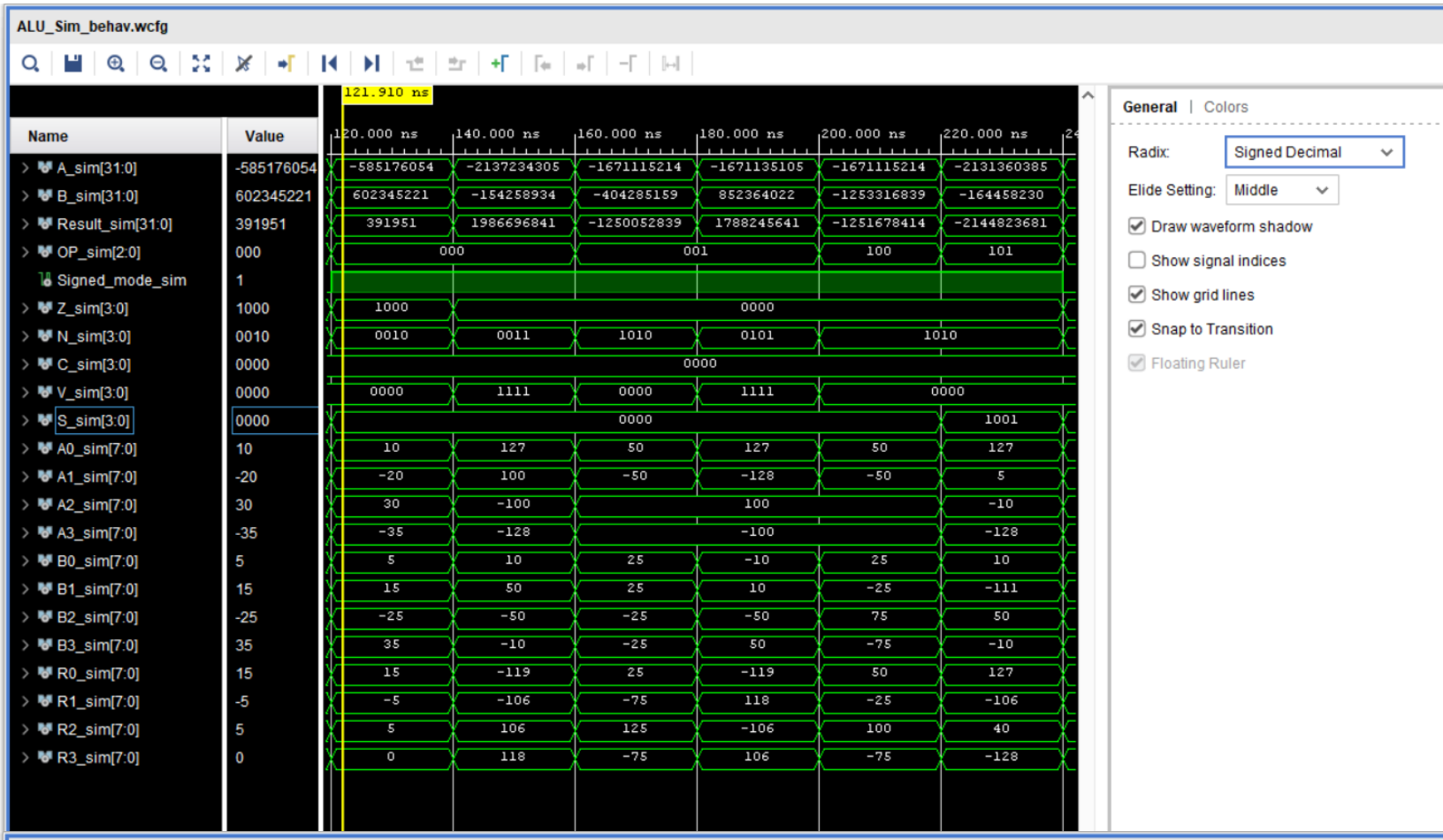
Ερώτημα 3_1 :

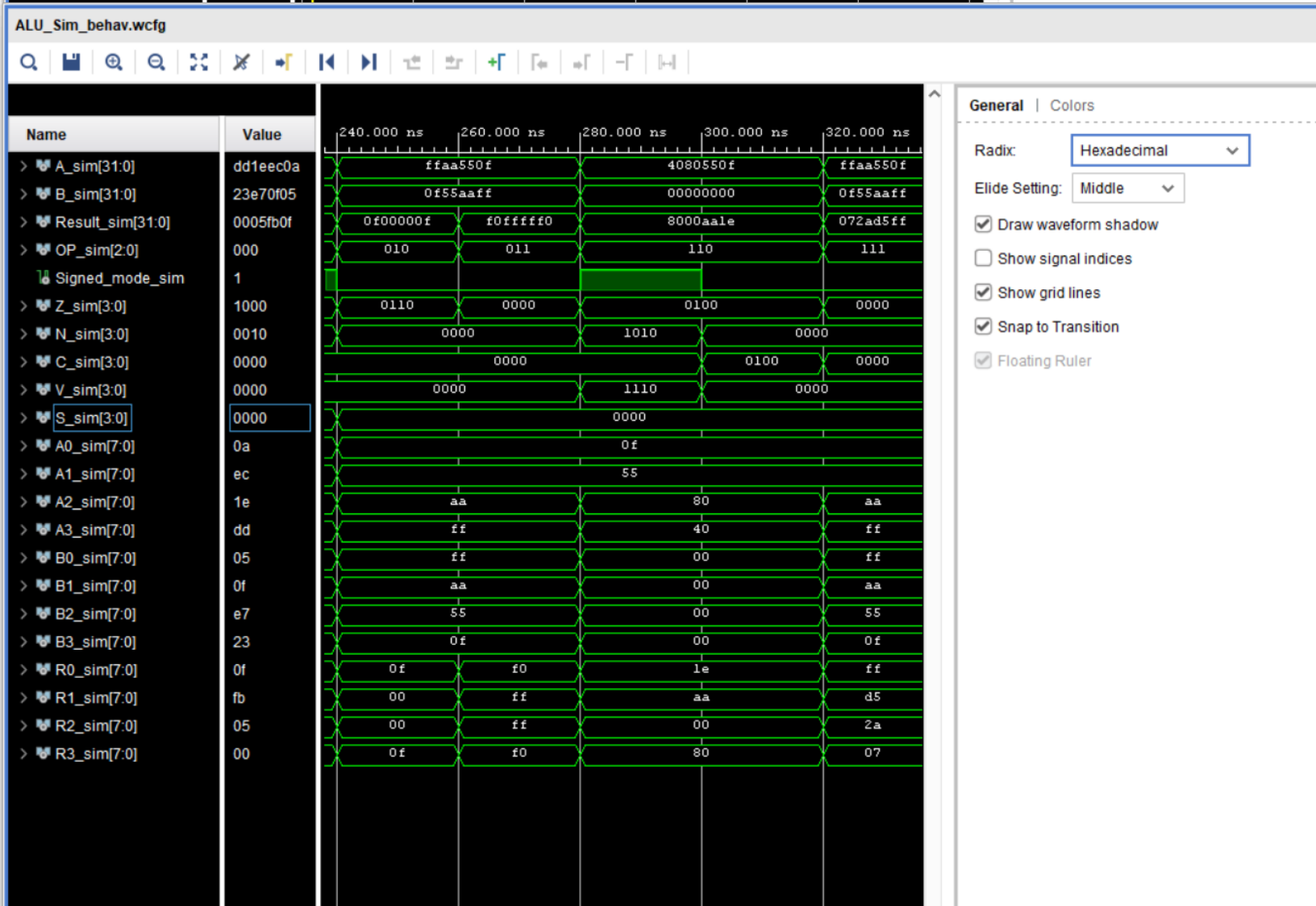
Behavioral and Post synthesis timing Simulation:

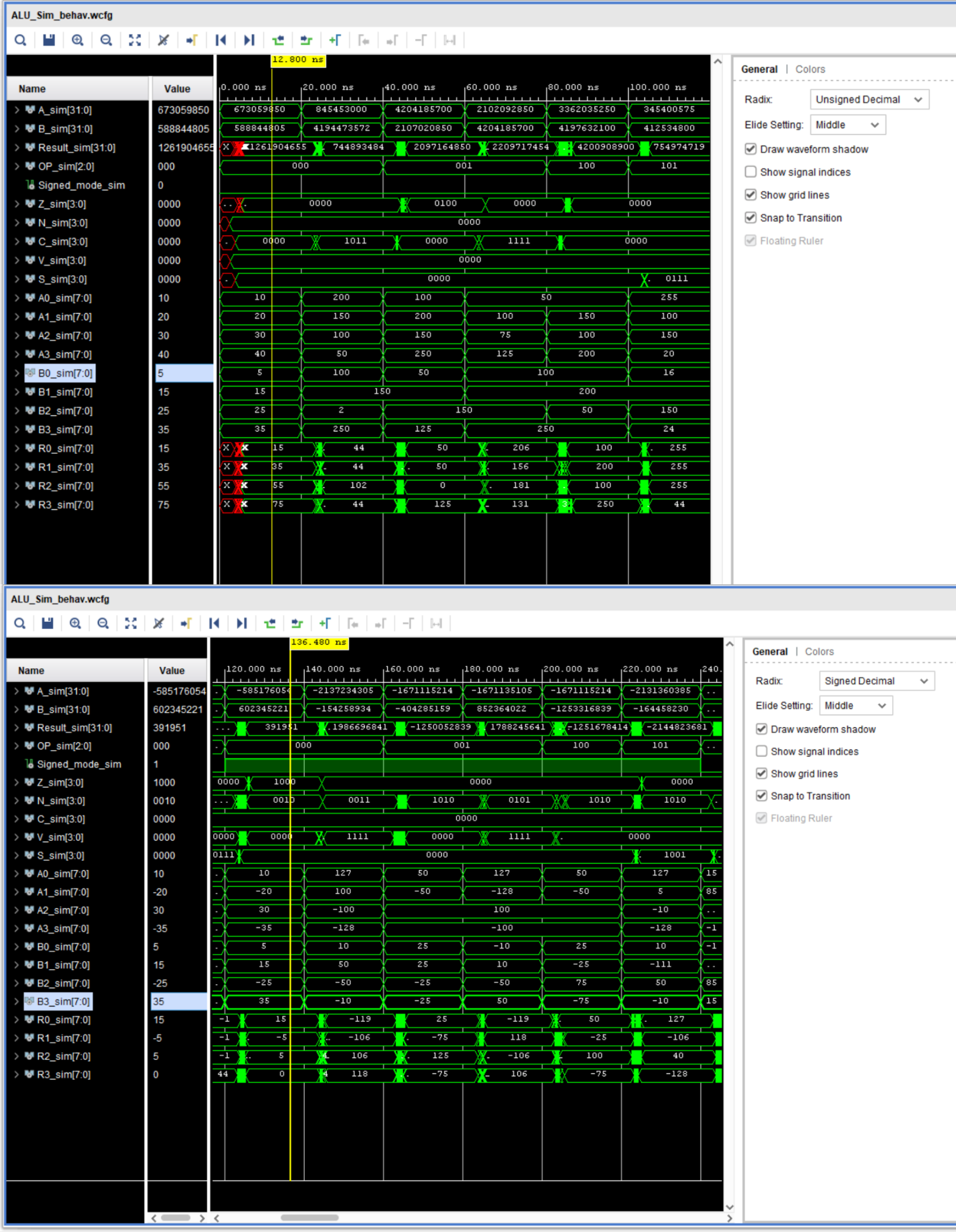
*Στον κώδικα της προσομοίωσης γράφω σε σχόλια τα αναμενόμενα αποτελέσματα και τα αναμενόμενα flags.

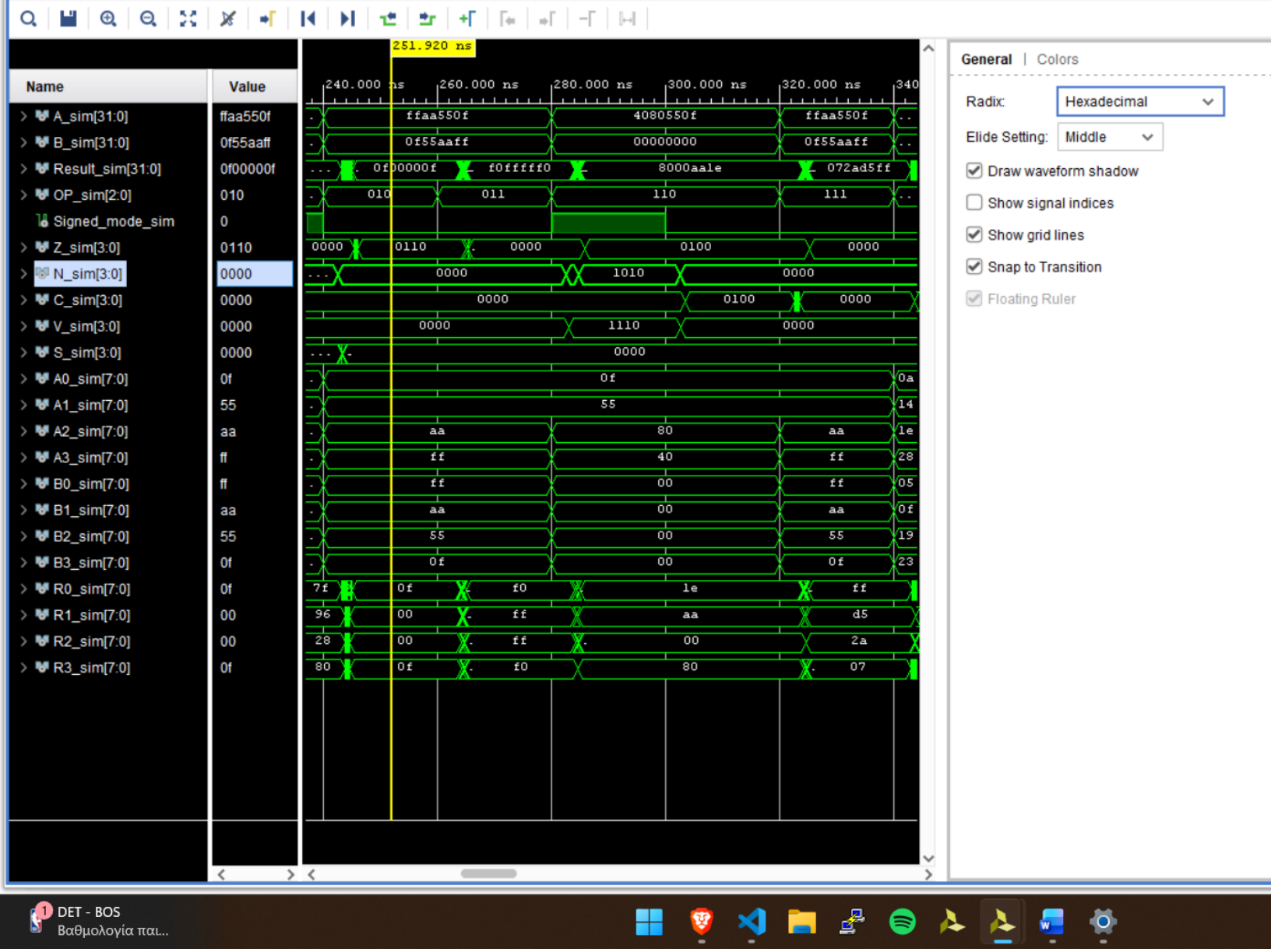
** Η πρώτη φωτογραφία είναι με radix decimal unsigned (γίνονται όλες οι unsigned δοκιμές μαζί), μετά όλες οι signed δοκιμές μαζί και στην 3η φωτογραφία είναι όσες έχουν να κάνουν με πράξεις bit οπότε για ευκολία το θέτω σε 16αδικό.




ALU_Sim_behav.wcfg
121.910 ns
120.000 ns
140.000 ns
160.000 ns
180.000 ns
200.000 ns
220.000 ns
Name
Value
A_sim[31:0] -585176054
B_sim[31:0] 602345221
Result_sim[31:0] 391951
OP_sim[2:0] 000
Signed_mode_sim 1
Z_sim[3:0] 1000
N_sim[3:0] 0010
C_sim[3:0] 0000
V_sim[3:0] 0000
S_sim[3:0] 0000
A0_sim[7:0] 10
A1_sim[7:0] -20
A2_sim[7:0] 30
A3_sim[7:0] -35
B0_sim[7:0] 5
B1_sim[7:0] 15
B2_sim[7:0] -25
B3_sim[7:0] 35
R0_sim[7:0] 15
R1_sim[7:0] -5
R2_sim[7:0] 5
R3_sim[7:0] 0
General | Colors
Radix: Signed Decimal
Elide Setting: Middle
Draw waveform shadow
Show signal indices
Show grid lines
Snap to Transition
Floating Ruler


ALU_Sim_behav.wcfg
240.000 ns
260.000 ns
280.000 ns
300.000 ns
320.000 ns
Name
Value
A_sim[31:0] dd1eec0a
B_sim[31:0] 23e70f05
Result_sim[31:0] 0005fb0f
OP_sim[2:0] 000
Signed_mode_sim 1
Z_sim[3:0] 1000
N_sim[3:0] 0010
C_sim[3:0] 0000
V_sim[3:0] 0000
S_sim[3:0] 0000
A0_sim[7:0] 0a
A1_sim[7:0] ec
A2_sim[7:0] 1e
A3_sim[7:0] dd
B0_sim[7:0] 05
B1_sim[7:0] 0f
B2_sim[7:0] e7
B3_sim[7:0] 23
R0_sim[7:0] 0f
R1_sim[7:0] fb
R2_sim[7:0] 05
R3_sim[7:0] 00
General | Colors
Radix: Hexadecimal
Elide Setting: Middle
Draw waveform shadow
Show signal indices
Show grid lines
Snap to Transition
Floating Ruler


ALU_Sim_behav.wcfg
12.800 ns
Name
Value
A_sim[31:0]
673059850
B_sim[31:0]
588844805
Result_sim[31:0]
1261904655
OP_sim[2:0]
000
Signed_mode_sim
0
Z_sim[3:0]
0000
N_sim[3:0]
0000
C_sim[3:0]
0000
V_sim[3:0]
0000
S_sim[3:0]
0000
A0_sim[7:0]
10
A1_sim[7:0]
20
A2_sim[7:0]
30
A3_sim[7:0]
40
B0_sim[7:0]
5
B1_sim[7:0]
15
B2_sim[7:0]
25
B3_sim[7:0]
35
R0_sim[7:0]
15
R1_sim[7:0]
35
R2_sim[7:0]
55
R3_sim[7:0]
75
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
General | Colors
Radix:
Unsigned Decimal
Elide Setting:
Middle
Draw waveform shadow
Show signal indices
Show grid lines
Snap to Transition
Floating Ruler
ALU_Sim_behav.wcfg
136.480 ns
Name
Value
A_sim[31:0]
-585176054
B_sim[31:0]
602345221
Result_sim[31:0]
391951
OP_sim[2:0]
000
Signed_mode_sim
1
Z_sim[3:0]
1000
N_sim[3:0]
0010
C_sim[3:0]
0000
V_sim[3:0]
0000
S_sim[3:0]
0000
A0_sim[7:0]
10
A1_sim[7:0]
-20
A2_sim[7:0]
30
A3_sim[7:0]
-35
B0_sim[7:0]
5
B1_sim[7:0]
15
B2_sim[7:0]
-25
B3_sim[7:0]
35
R0_sim[7:0]
15
R1_sim[7:0]
-5
R2_sim[7:0]
5
R3_sim[7:0]
0
120.000 ns
140.000 ns
160.000 ns
180.000 ns
200.000 ns
220.000 ns
General | Colors
Radix:
Signed Decimal
Elide Setting:
Middle
Draw waveform shadow
Show signal indices
Show grid lines
Snap to Transition
Floating Ruler

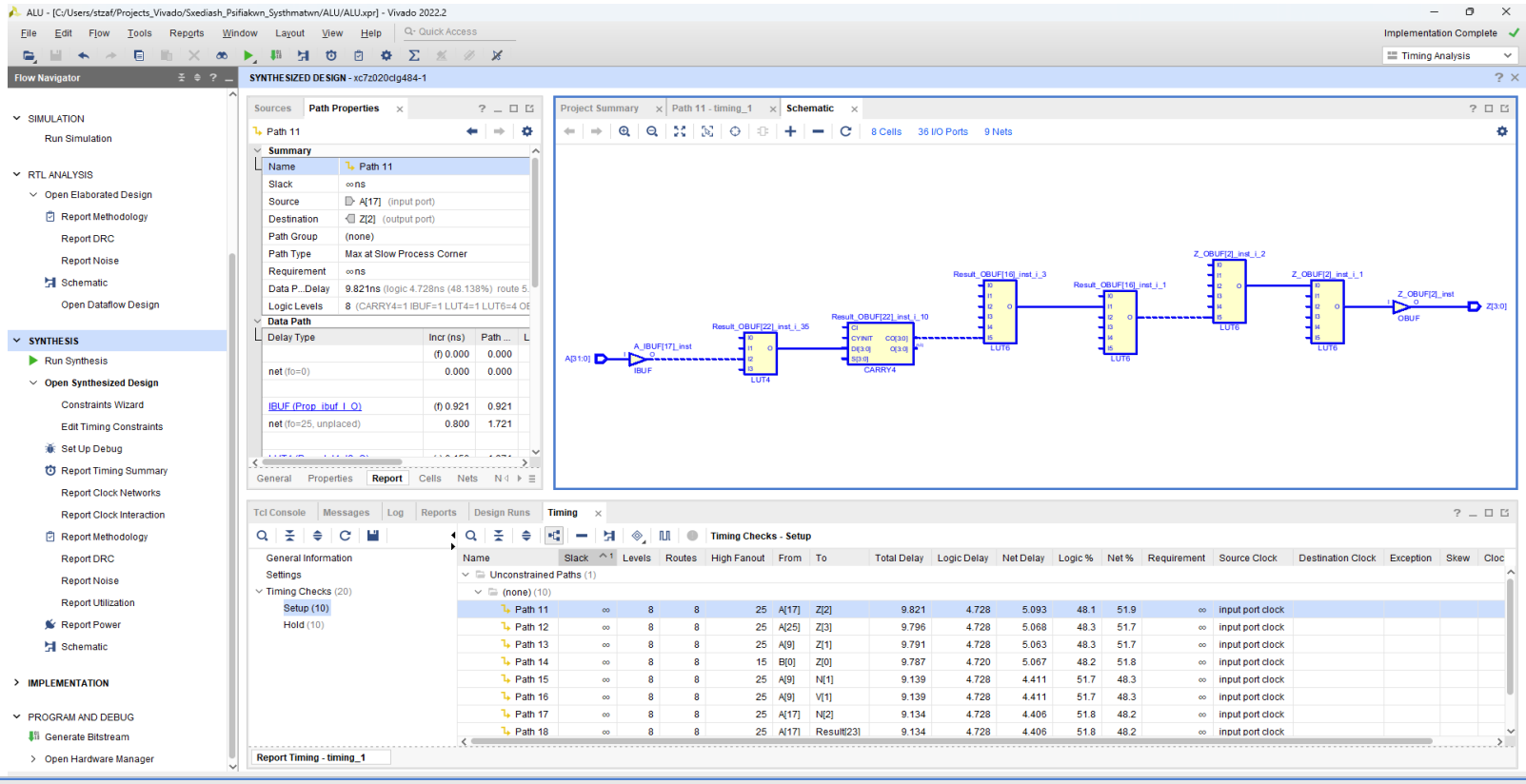


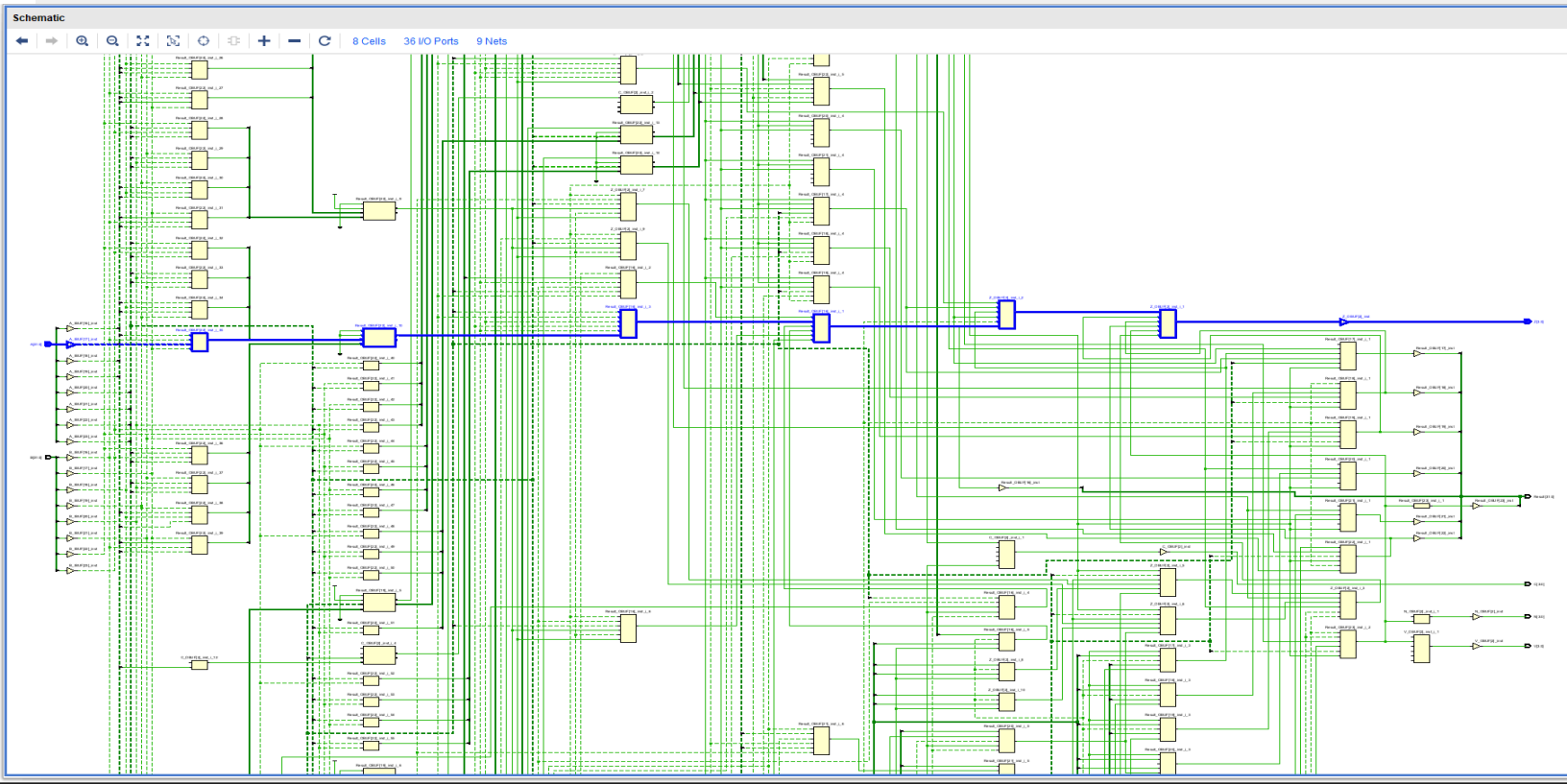
Οι 3 τελευταίες φωτογραφίες αφορούν Post synthesis timing Simulation

Ερώτημα 3_2 :

<u>Καθυστέρηση διάδοσης :</u>

Είναι το Path 11 –το πιο αργό (απομονωμένο και σε ολόκληρο το synthesized device)





Καθυστέρηση μόλυνσης:

Όλα τα paths από 1-10 έχουν την ίδια ελάχιστη καθυστέρηση.