

Όνομα : Στέφανος Τζαφέρης

ΑΜ : 1115202200183

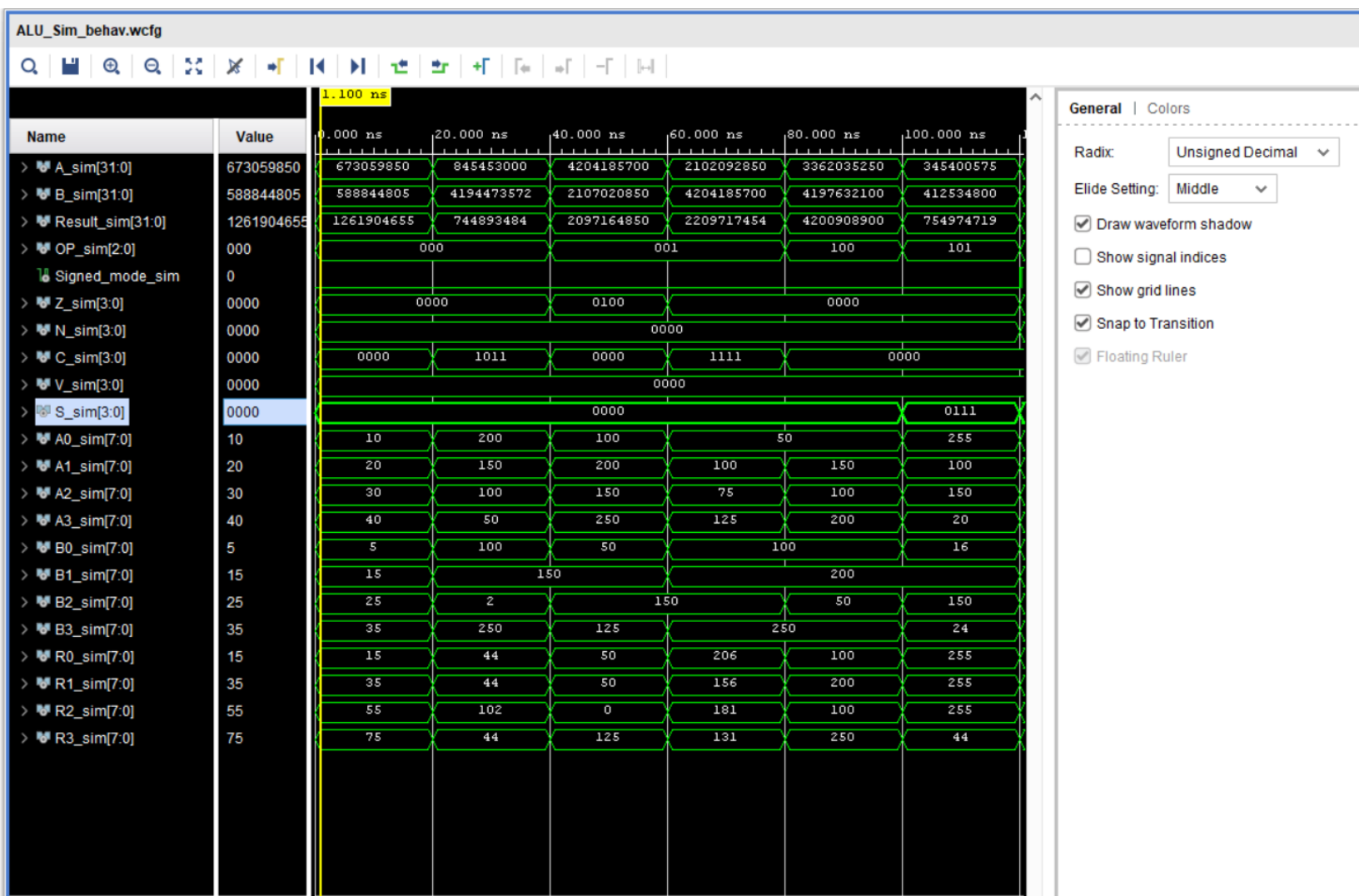
Εργασία 1

Ερώτημα 3_1 :

Behavioral and Post synthesis timing Simulation:

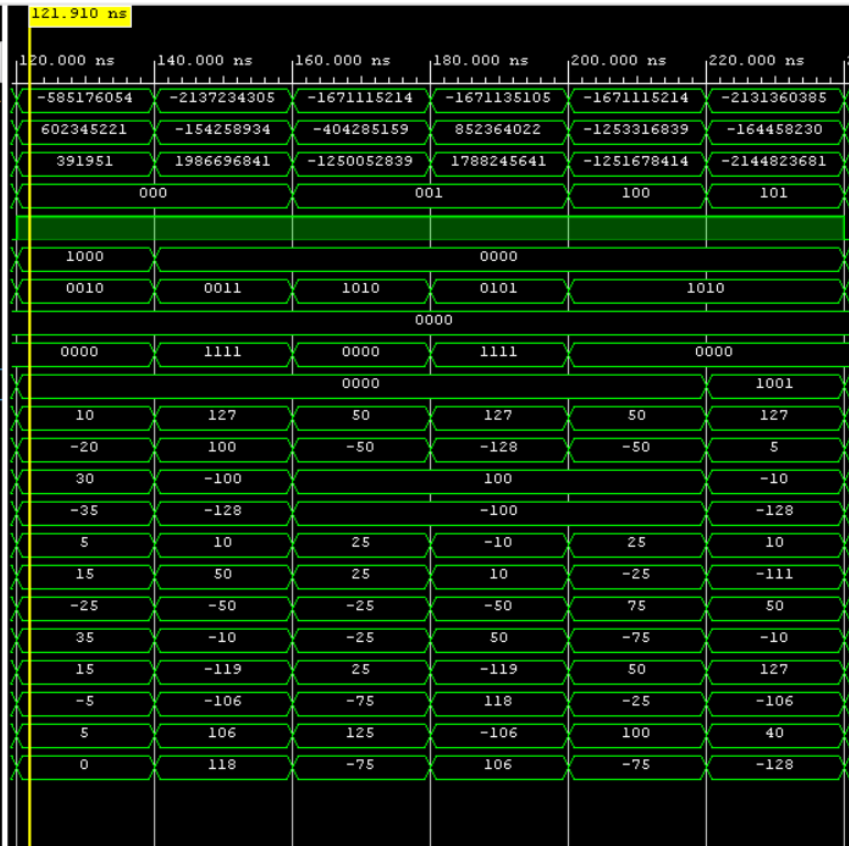
*Στον κώδικα της προσομοίωσης γράφω σε σχόλια τα αναμενόμενα αποτελέσματα και τα αναμενόμενα flags.

** Η πρώτη φωτογραφία είναι με radix decimal unsigned (γίνονται όλες οι unsigned δοκιμές μαζί), μετά όλες οι signed δοκιμές μαζί και στην 3^η φωτογραφία είναι όσες έχουν να κάνουν με πράξεις bit οπότε για ευκολία το θέτω σε 16αδικό.





Name	Value
> A_sim[31:0]	-585176054
> B_sim[31:0]	602345221
> Result_sim[31:0]	391951
> OP_sim[2:0]	000
> Signed_mode_sim	1
> Z_sim[3:0]	1000
> N_sim[3:0]	0010
> C_sim[3:0]	0000
> V_sim[3:0]	0000
> S_sim[3:0]	0000
> A0_sim[7:0]	10
> A1_sim[7:0]	-20
> A2_sim[7:0]	30
> A3_sim[7:0]	-35
> B0_sim[7:0]	5
> B1_sim[7:0]	15
> B2_sim[7:0]	-25
> B3_sim[7:0]	35
> R0_sim[7:0]	15
> R1_sim[7:0]	-5
> R2_sim[7:0]	5
> R3_sim[7:0]	0

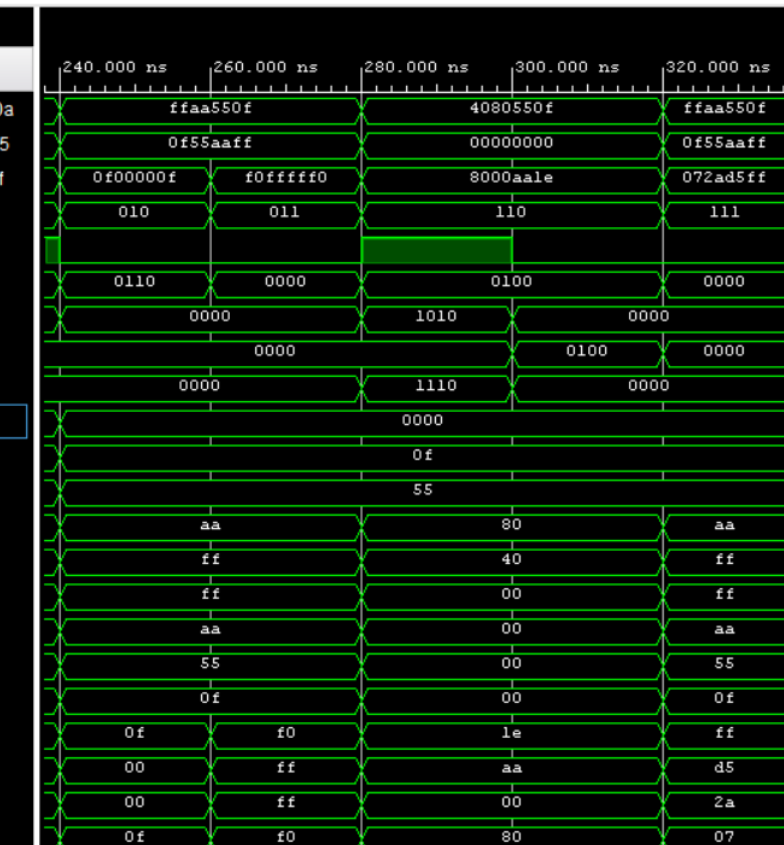


General | Colors

- Radix: Signed Decimal
- Elide Setting: Middle
- ☒ Draw waveform shadow
- ☐ Show signal indices
- ☒ Show grid lines
- ☒ Snap to Transition
- ☒ Floating Ruler

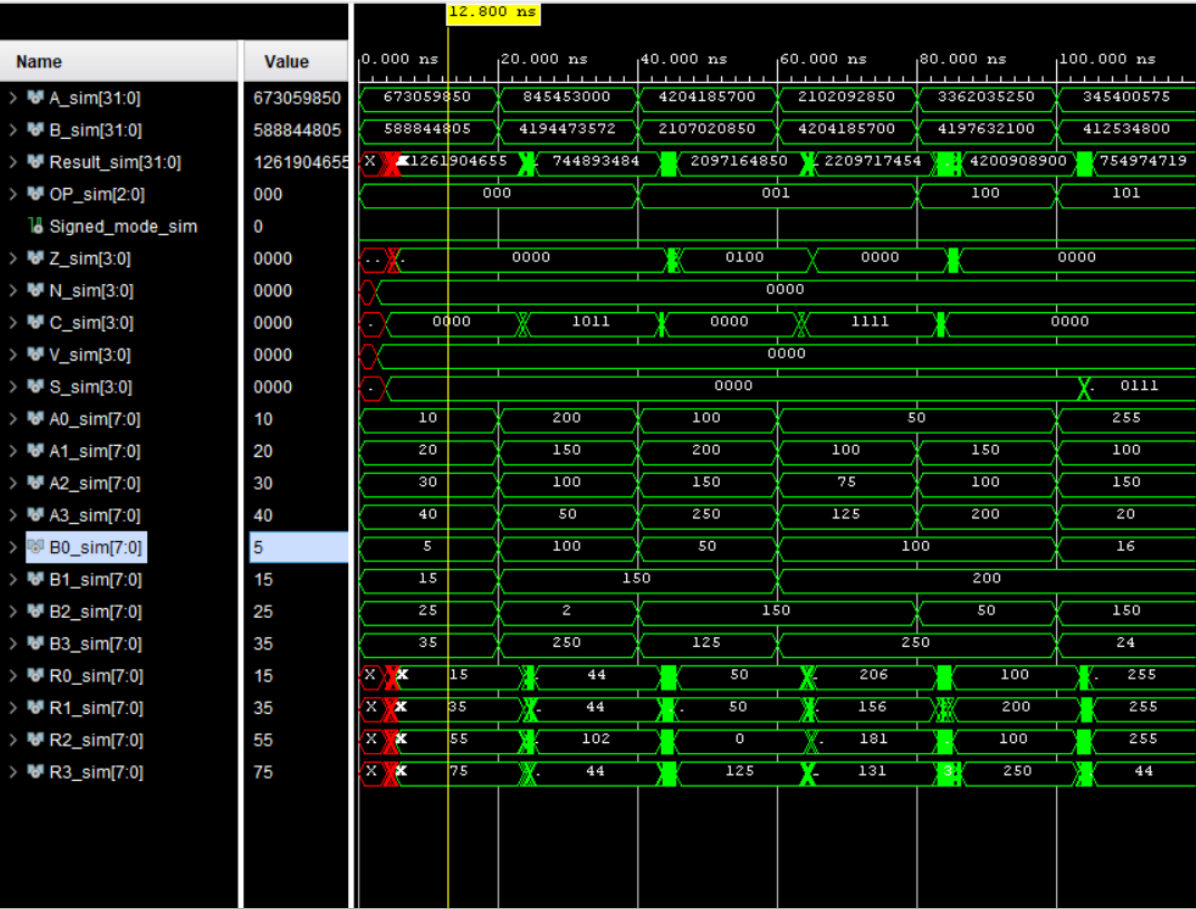


Name	Value
> A_sim[31:0]	dd1eec0a
> B_sim[31:0]	23e70f05
> Result_sim[31:0]	0005fb0f
> OP_sim[2:0]	000
> Signed_mode_sim	1
> Z_sim[3:0]	1000
> N_sim[3:0]	0010
> C_sim[3:0]	0000
> V_sim[3:0]	0000
> S_sim[3:0]	0000
> A0_sim[7:0]	0a
> A1_sim[7:0]	ec
> A2_sim[7:0]	1e
> A3_sim[7:0]	dd
> B0_sim[7:0]	05
> B1_sim[7:0]	0f
> B2_sim[7:0]	e7
> B3_sim[7:0]	23
> R0_sim[7:0]	0f
> R1_sim[7:0]	fb
> R2_sim[7:0]	05
> R3_sim[7:0]	00



General | Colors

- Radix: Hexadecimal
- Elide Setting: Middle
- ☒ Draw waveform shadow
- ☐ Show signal indices
- ☒ Show grid lines
- ☒ Snap to Transition
- ☒ Floating Ruler



General | Colors

Radix: Unsigned Decimal

Elide Setting: Middle

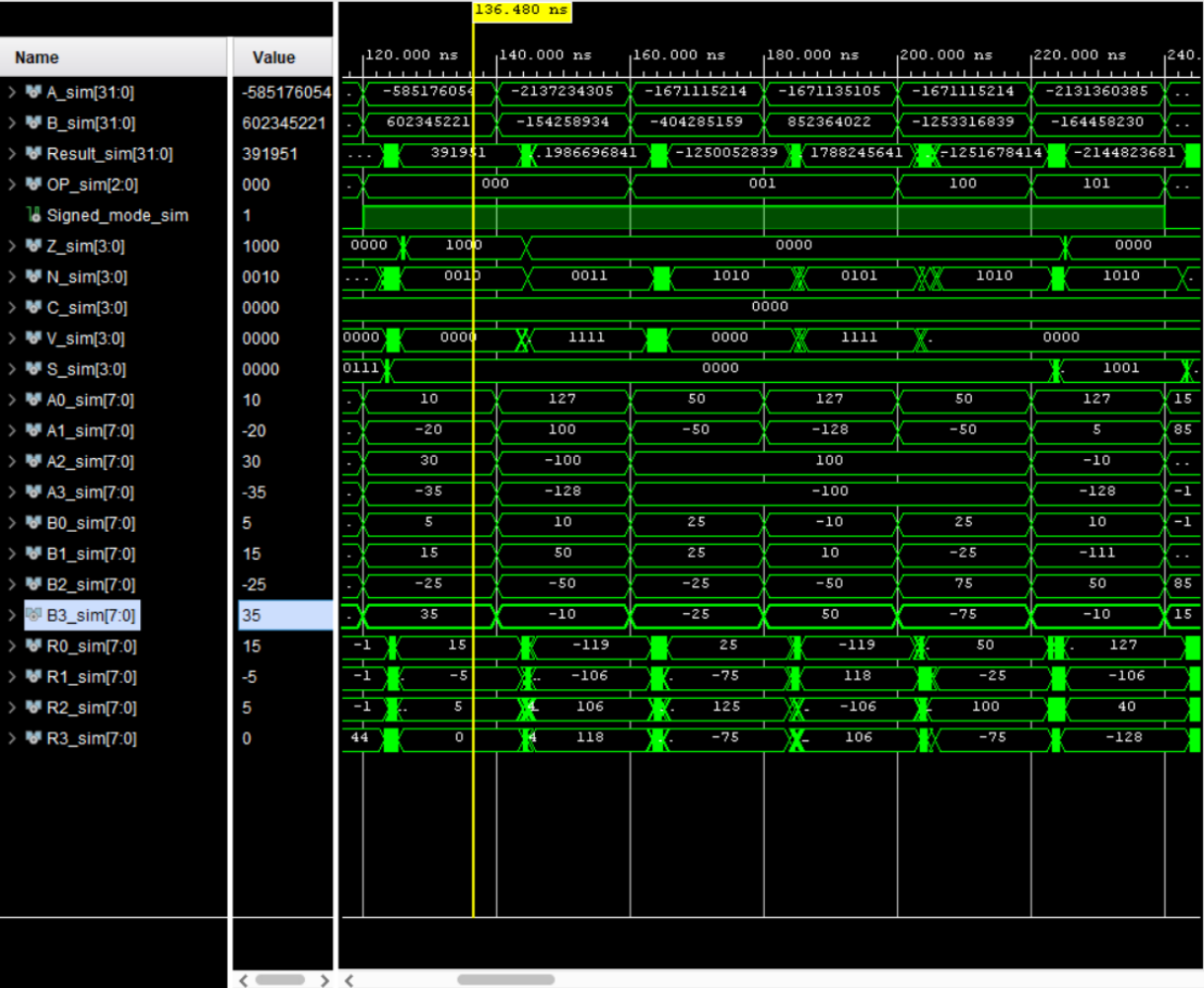
☒ Draw waveform shadow

☐ Show signal indices

☒ Show grid lines

☒ Snap to Transition

☒ Floating Ruler



General | Colors

Radix: Signed Decimal

Elide Setting: Middle

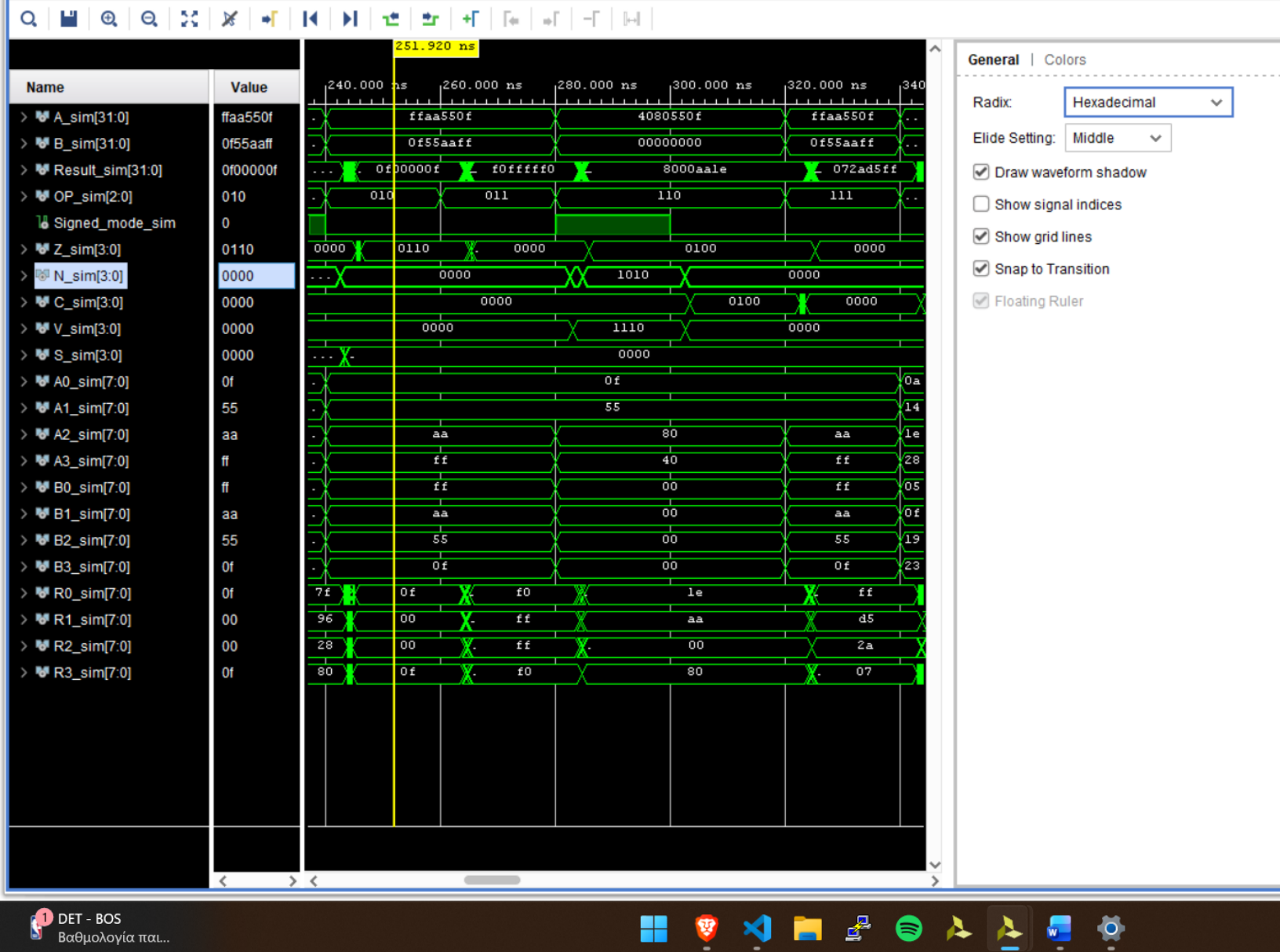
☒ Draw waveform shadow

☐ Show signal indices

☒ Show grid lines

☒ Snap to Transition

☒ Floating Ruler

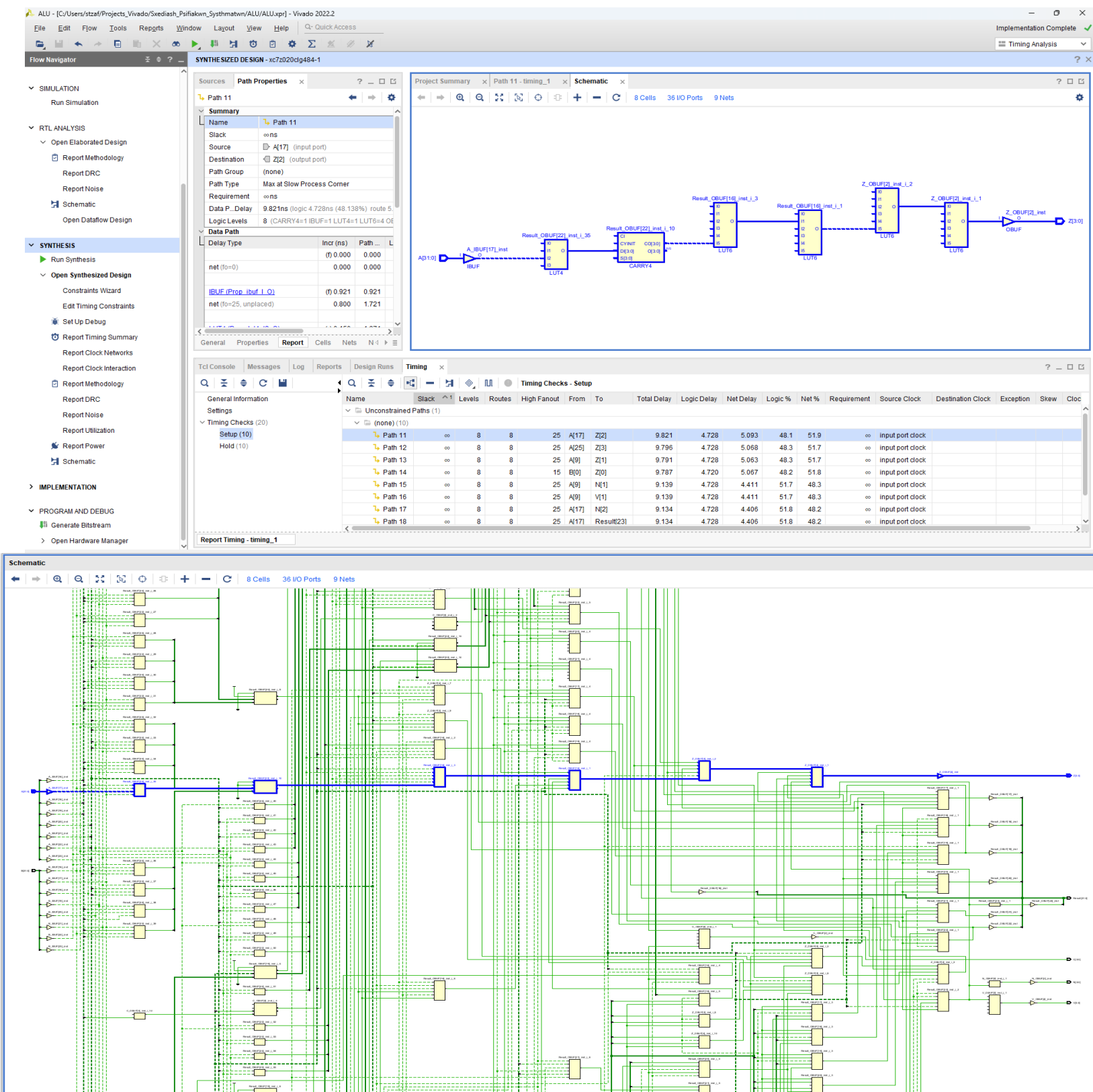


Οι 3 τελευταίες φωτογραφίες αφορούν Post synthesis timing Simulation

Ερώτημα 3_2 :

Καυστέρηση διάδοσης :

Είναι το Path 11 –το πιο αργό (απομονωμένο και σε ολόκληρο το synthesized device)



Καθυστέρηση μόλυνσης:

Όλα τα paths από 1-10 έχουν την ίδια ελάχιστη καθυστέρηση.

ALU - [C:/Users/stzaf/Projects/Vivado/Sxediash_Psihakiwn_Synthmatwn/ALU/ALU.xpr] - Vivado 2022.2

Implementation Complete
Timing Analysis

Project Manager
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design

SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic

Sources Netlist Path Properties

Nets (1220)
Leaf Cells (791)
A_IBUF[0]_inst (IBUF)
A_IBUF[1]_inst (IBUF)
A_IBUF[2]_inst (IBUF)
A_IBUF[3]_inst (IBUF)
A_IBUF[4]_inst (IBUF)
A_IBUF[5]_inst (IBUF)
A_IBUF[6]_inst (IBUF)
A_IBUF[7]_inst (IBUF)
A_IBUF[8]_inst (IBUF)
A_IBUF[9]_inst (IBUF)
A_IBUF[10]_inst (IBUF)
A_IBUF[11]_inst (IBUF)
A_IBUF[12]_inst (IBUF)
A_IBUF[13]_inst (IBUF)
A_IBUF[14]_inst (IBUF)

Project Summary Path 1 - timing_1 Schematic

3 Cells 36 I/O Ports 4 Nets

A[31:0] I A_IBUF[7]_inst IBUF O C_OBUF[0]_inst i 1 C_OBUF[0]_inst O C[3:0]

LUT6

Tcl Console Messages Log Reports Design Runs Timing

Timing Checks - Hold

General Information
Settings
Timing Checks (20)
Setup (10)
Hold (10)

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exception	Skew	Clock
Unconstrained Paths (1)																	
(none) (10)																	
Path 1	∞	3	4	20	A[7]	C[0]	1.971	1.297	0.674	65.8	34.2	-∞	input port clock				
Path 2	∞	3	4	22	A[15]	C[1]	1.971	1.297	0.674	65.8	34.2	-∞	input port clock				
Path 3	∞	3	4	22	A[23]	C[2]	1.971	1.297	0.674	65.8	34.2	-∞	input port clock				
Path 4	∞	3	4	22	A[31]	C[3]	1.971	1.297	0.674	65.8	34.2	-∞	input port clock				
Path 5	∞	3	4	72	Signed_mode	N[0]	1.971	1.297	0.674	65.8	34.2	-∞	input port clock				
Path 6	∞	3	4	72	Signed_mode	N[1]	1.971	1.297	0.674	65.8	34.2	-∞	input port clock				
Path 7	∞	3	4	72	Signed_mode	N[2]	1.971	1.297	0.674	65.8	34.2	-∞	input port clock				
Path 8	∞	3	4	24	A[0]	Result[0]	1.971	1.297	0.674	65.8	34.2	-∞	input port clock				
Path 9	∞	3	4	26	A[10]	Result[10]	1.971	1.297	0.674	65.8	34.2	-∞	input port clock				
Path 10	∞	3	4	26	A[11]	Result[11]	1.971	1.297	0.674	65.8	34.2	-∞	input port clock				

Report Timing - timing_1

17°C
Εντονες νεφώσεις.

21:35
11/27/2025

