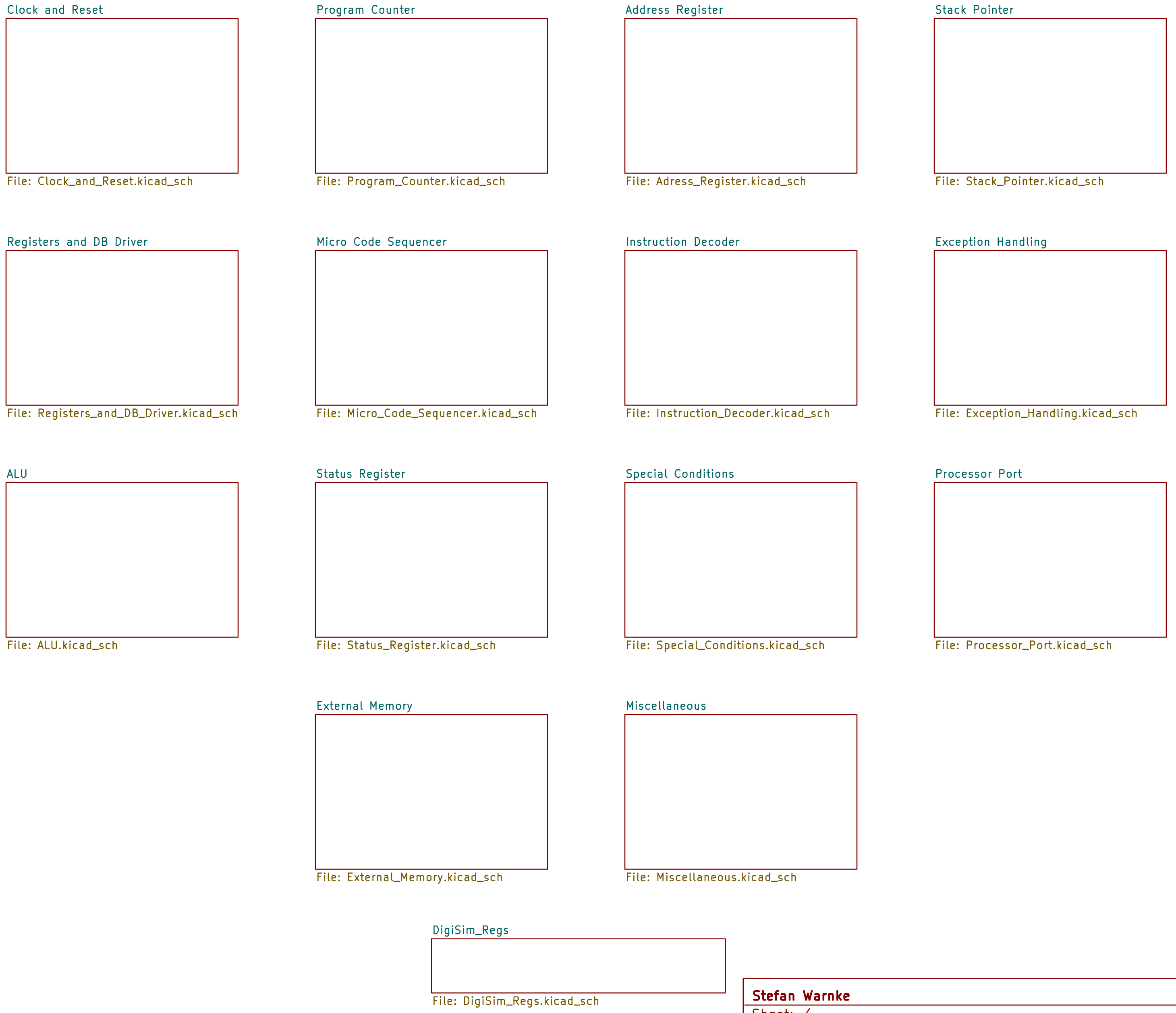
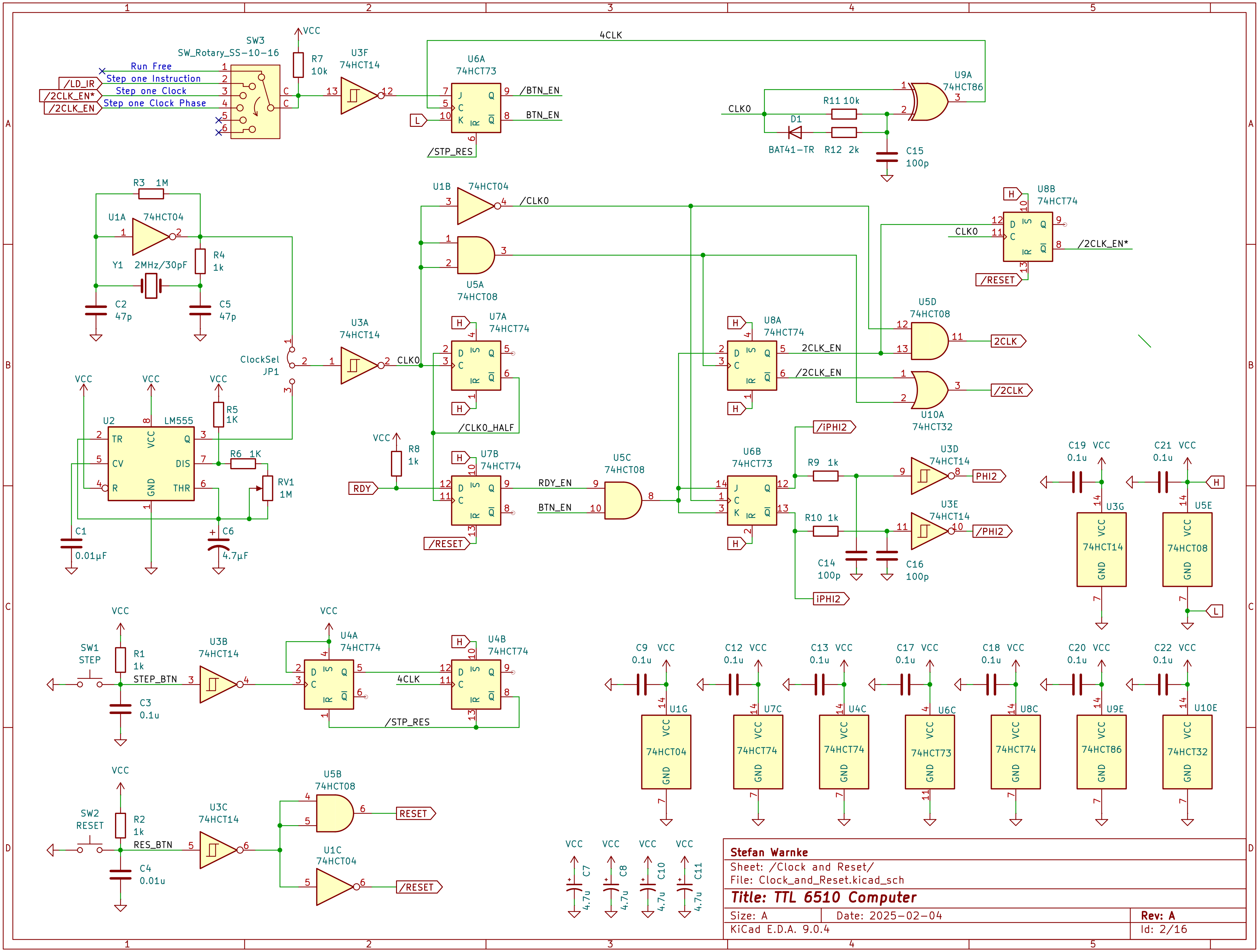

Clock and Reset
File: Clock_and_Reset.kicad_sch
Program Counter
File: Program_Counter.kicad_sch
Address Register
File: Adress_Register.kicad_sch
Stack Pointer
File: Stack_Pointer.kicad_sch
Registers and DB Driver
File: Registers_and_DB_Driver.kicad_sch
Micro Code Sequencer
File: Micro_Code_Sequencer.kicad_sch
Instruction Decoder
File: Instruction_Decoder.kicad_sch
Exception Handling
File: Exception_Handling.kicad_sch
ALU
File: ALU.kicad_sch
Status Register
File: Status_Register.kicad_sch
Special Conditions
File: Special_Conditions.kicad_sch
Processor Port
File: Processor_Port.kicad_sch
External Memory
File: External_Memory.kicad_sch
Miscellaneous
File: Miscellaneous.kicad_sch
DigiSim_Regs
File: DigiSim_Regs.kicad_sch

Stefan Warnke
Sheet: /
File: TTL 6510 Computer.kicad_sch

Title: TTL 6510 Computer

Size: A	Date: 2025-02-04	**Rev: A**
KiCad E.D.A. 9.0.4		Id: 1/16

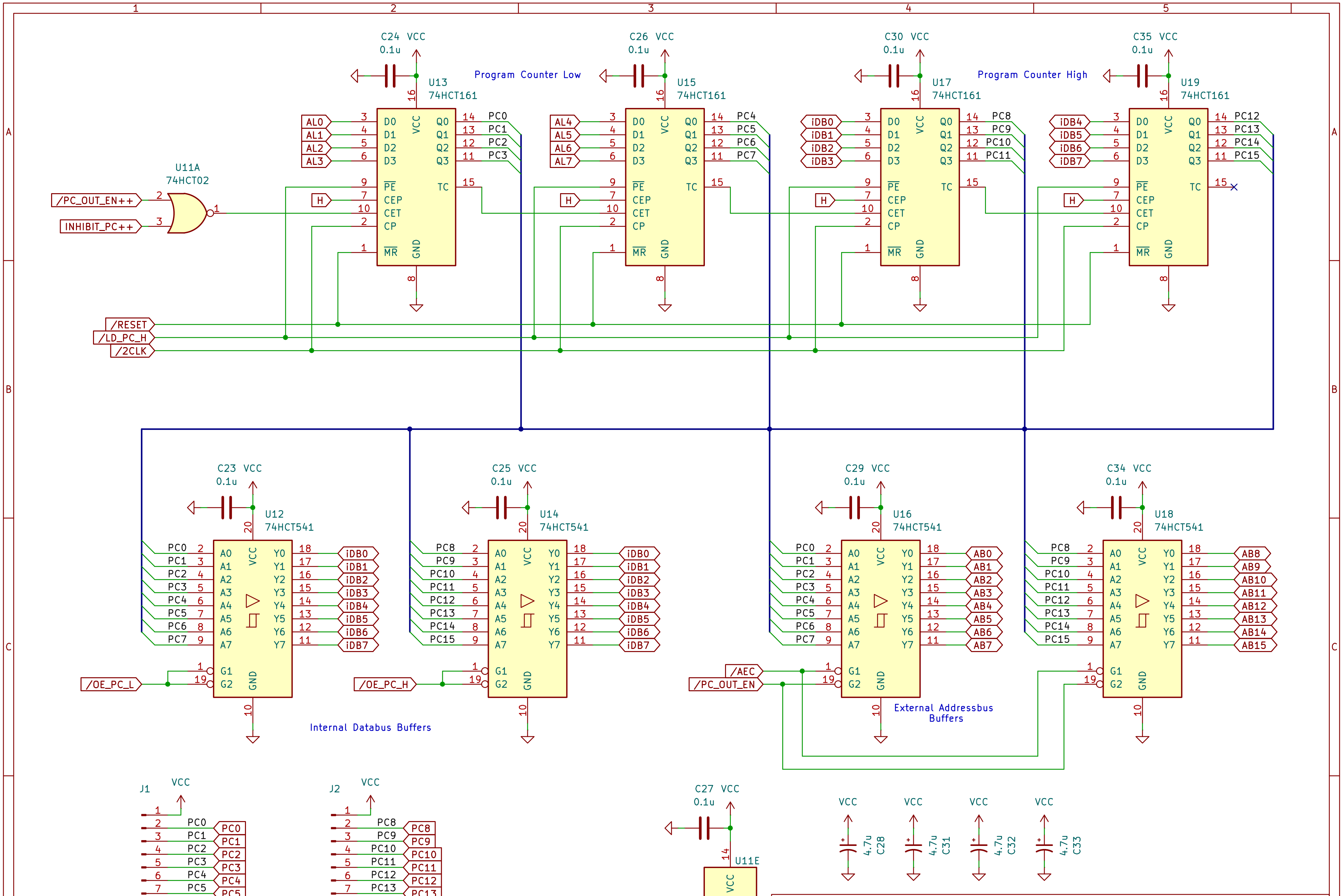

1
2
3
4
5
A
B
C
D
SW3
SW_Rotary_SS-10-16
Run Free
Step one Instruction
Step one Clock
Step one Clock Phase
/LD_IR
/2CLK_EN*
/2CLK_EN
VCC
R7
10k
U3F
74HCT14
U6A
74HCT73
4CLK
/BTN_EN
BTN_EN
L
/STP_RES
U9A
74HCT86
CLK0
R11 10k
D1
BAT41-TR
R12 2k
C15
100p
R3 1M
U1A
74HCT04
R4
1k
Y1 2MHz/30pF
C2
47p
C5
47p
U1B
74HCT04
/CLK0
U5A
74HCT08
U8B
74HCT74
H
/RESET
U5D
74HCT08
2CLK
U10A
74HCT32
/2CLK
U8A
74HCT74
2CLK_EN
/2CLK_EN
ClockSel
JP1
U3A
74HCT14
CLK0
U7A
74HCT74
/CLK0_HALF
U2
LM555
TR
CV
R
Q
DIS
THR
GND
R5
1K
R6 1K
RV1
1M
C1
0.01µF
C6
4.7µF
VCC
R8
1k
RDY
U7B
74HCT74
RDY_EN
BTN_EN
U5C
74HCT08
U6B
74HCT73
/iPHI2
R9 1k
U3D
74HCT14
PHI2
R10 1k
U3E
74HCT14
/PHI2
C14
100p
C16
100p
iPHI2
C19 0.1u
C21 0.1u
U3G
74HCT14
U5E
74HCT08
SW1
STEP
R1
1k
STEP_BTN
C3
0.1u
U3B
74HCT14
U4A
74HCT74
U4B
74HCT74
4CLK
/STP_RES
SW2
RESET
R2
1k
RES_BTN
C4
0.01u
U3C
74HCT14
U5B
74HCT08
RESET
U1C
74HCT04
/RESET
C9 0.1u
C12 0.1u
C13 0.1u
C17 0.1u
C18 0.1u
C20 0.1u
C22 0.1u
U1G 74HCT04
U7C 74HCT74
U4C 74HCT74
U6C 74HCT73
U8C 74HCT74
U9E 74HCT86
U10E 74HCT32
C7 4.7u
C8 4.7u
C10 4.7u
C11 4.7u

Stefan Warnke

Sheet: /Clock and Reset/
File: Clock_and_Reset.kicad_sch

Title: TTL 6510 Computer

Size: A
Date: 2025-02-04
Rev: A
KiCad E.D.A. 9.0.4
Id: 2/16


1
2
3
4
5
A
B
C
D
Program Counter Low
Program Counter High
C24 VCC 0.1u
U13 74HCT161
C26 VCC 0.1u
U15 74HCT161
C30 VCC 0.1u
U17 74HCT161
C35 VCC 0.1u
U19 74HCT161
D0 D1 D2 D3 PE CEP CET CP MR VCC GND Q0 Q1 Q2 Q3 TC
AL0 AL1 AL2 AL3
AL4 AL5 AL6 AL7
iDB0 iDB1 iDB2 iDB3
iDB4 iDB5 iDB6 iDB7
PC0 PC1 PC2 PC3
PC4 PC5 PC6 PC7
PC8 PC9 PC10 PC11
PC12 PC13 PC14 PC15
H
U11A 74HCT02
/PC_OUT_EN++
INHIBIT_PC++
/RESET
/LD_PC_H
/2CLK
C23 VCC 0.1u
U12 74HCT541
C25 VCC 0.1u
U14 74HCT541
C29 VCC 0.1u
U16 74HCT541
C34 VCC 0.1u
U18 74HCT541
A0 A1 A2 A3 A4 A5 A6 A7 G1 G2 Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
iDB0 iDB1 iDB2 iDB3 iDB4 iDB5 iDB6 iDB7
AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7
AB8 AB9 AB10 AB11 AB12 AB13 AB14 AB15
/OE_PC_L
/OE_PC_H
/AEC
/PC_OUT_EN
Internal Databus Buffers
External Addressbus Buffers
J1 VCC
PCL
J2 VCC
PCH
C27 VCC 0.1u
U11E 74HCT02
VCC 4.7u C28
VCC 4.7u C31
VCC 4.7u C32
VCC 4.7u C33

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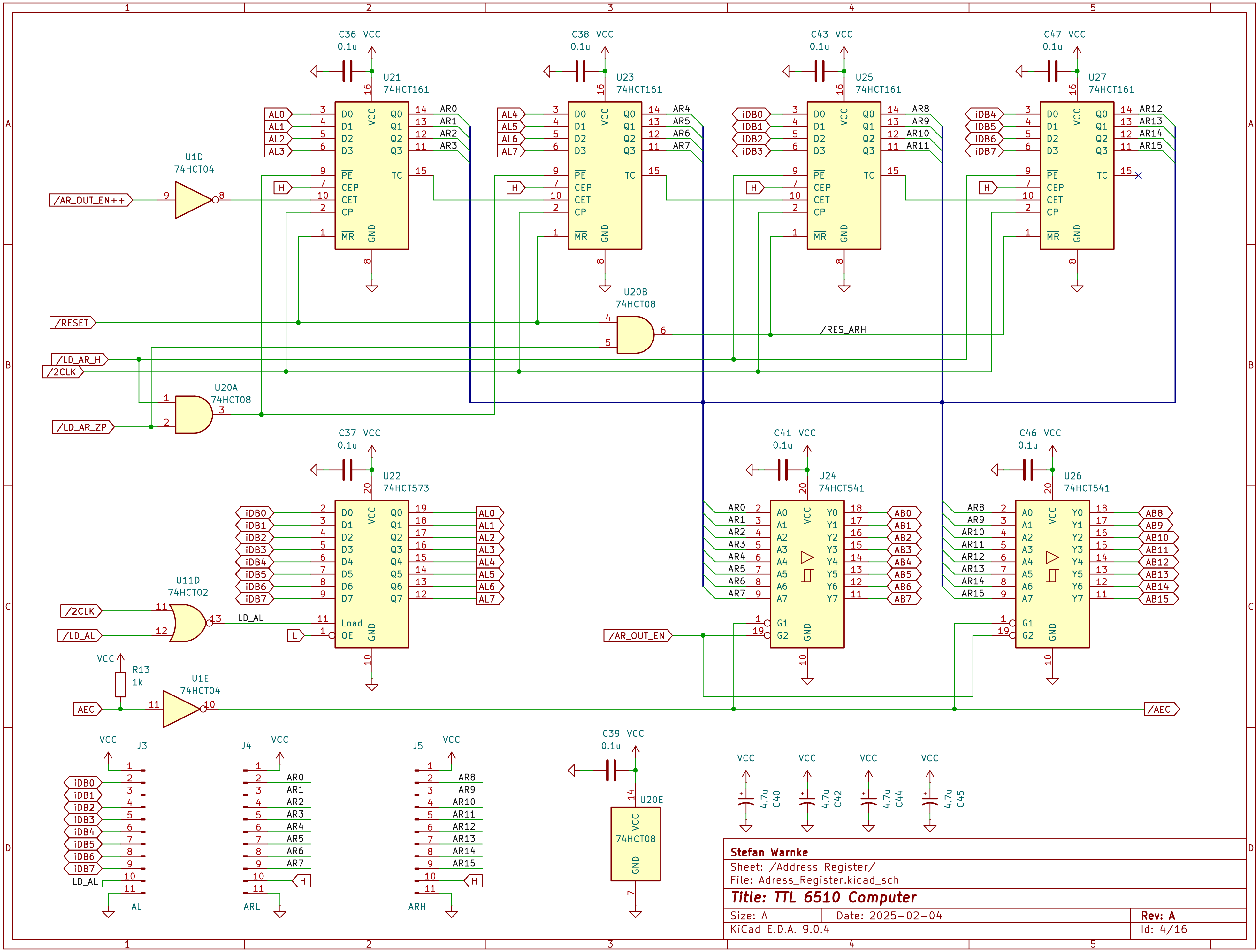
Sheet: /Program Counter/
File: Program_Counter.kicad_sch

Title: TTL 6510 Computer

Size: A
Date: 2025-02-04
Rev: A
KiCad E.D.A. 9.0.4
Id: 3/16


1
2
3
4
5
A
B
C
D
C36 0.1u
VCC
U21 74HCT161
C38 0.1u
U23 74HCT161
C43 0.1u
U25 74HCT161
C47 0.1u
U27 74HCT161
AL0
AL1
AL2
AL3
AL4
AL5
AL6
AL7
iDB0
iDB1
iDB2
iDB3
iDB4
iDB5
iDB6
iDB7
D0
D1
D2
D3
PE
CEP
CET
CP
MR
Q0
Q1
Q2
Q3
TC
GND
AR0
AR1
AR2
AR3
AR4
AR5
AR6
AR7
AR8
AR9
AR10
AR11
AR12
AR13
AR14
AR15
H
U1D 74HCT04
/AR_OUT_EN++
/RESET
U20B 74HCT08
/RES_ARH
/LD_AR_H
/2CLK
U20A 74HCT08
/LD_AR_ZP
C37 0.1u
U22 74HCT573
D4
D5
D6
D7
Q4
Q5
Q6
Q7
Load
OE
LD_AL
L
U11D 74HCT02
/LD_AL
C41 0.1u
U24 74HCT541
C46 0.1u
U26 74HCT541
A0
A1
A2
A3
A4
A5
A6
A7
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
G1
G2
AB0
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AB8
AB9
AB10
AB11
AB12
AB13
AB14
AB15
/AR_OUT_EN
R13 1k
U1E 74HCT04
AEC
/AEC
J3
AL
J4
ARL
J5
ARH
C39 0.1u
U20E
74HCT08
4.7u C40
4.7u C42
4.7u C44
4.7u C45

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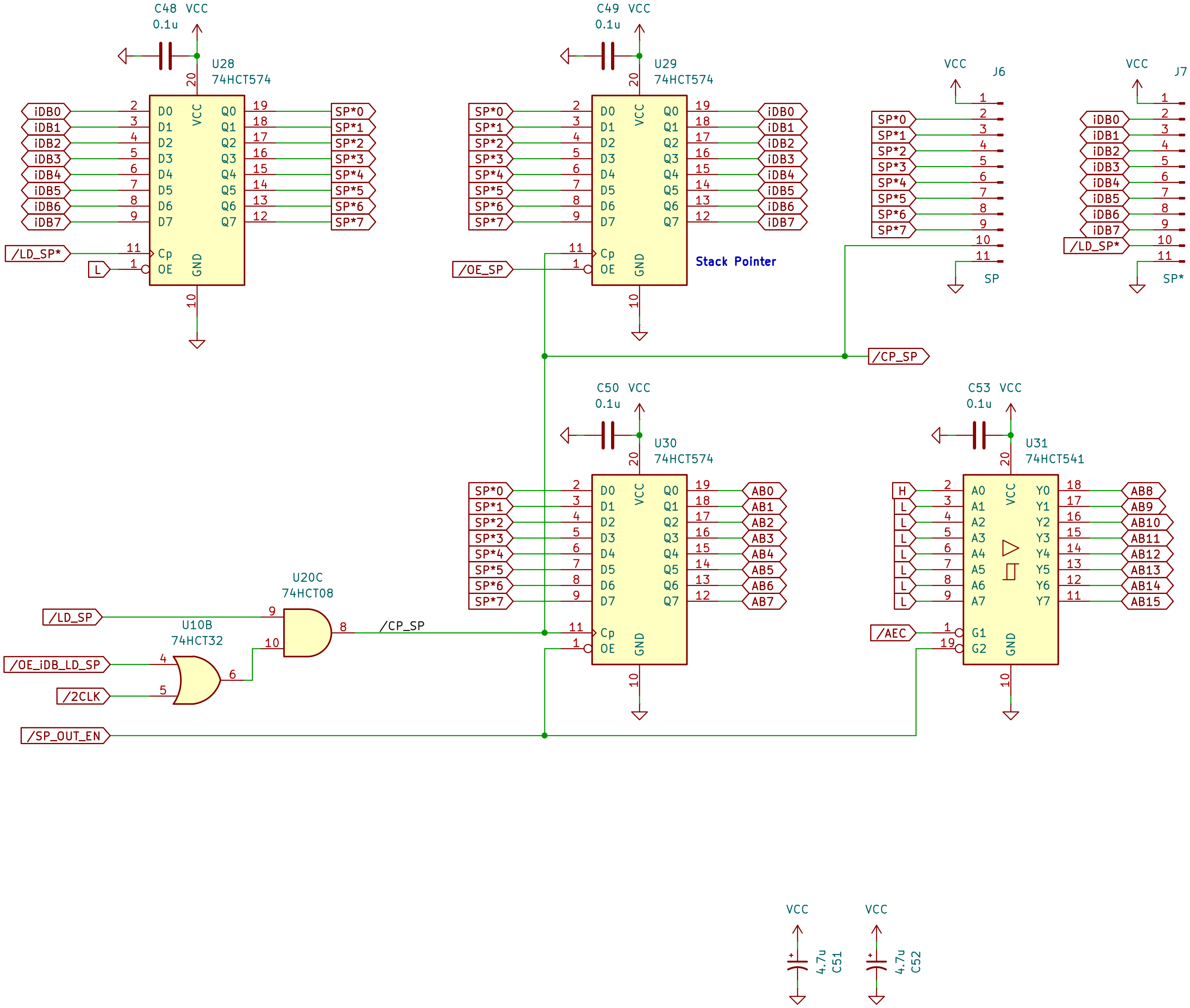
Sheet: /Address Register/
File: Adress_Register.kicad_sch

Title: TTL 6510 Computer

Size: A	Date: 2025-02-04	**Rev: A**
KiCad E.D.A. 9.0.4		Id: 4/16


C48 0.1u VCC
U28 74HCT574
iDB0 iDB1 iDB2 iDB3 iDB4 iDB5 iDB6 iDB7
D0 D1 D2 D3 D4 D5 D6 D7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
SP*0 SP*1 SP*2 SP*3 SP*4 SP*5 SP*6 SP*7
/LD_SP*
L
Cp
OE
VCC
GND
C49 0.1u VCC
U29 74HCT574
/OE_SP
Stack Pointer
J6
VCC
SP
J7
VCC
/LD_SP*
SP*
/CP_SP
C50 0.1u VCC
U30 74HCT574
AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7
C53 0.1u VCC
U31 74HCT541
H
A0 A1 A2 A3 A4 A5 A6 A7
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
AB8 AB9 AB10 AB11 AB12 AB13 AB14 AB15
/AEC
G1 G2
U20C 74HCT08
/LD_SP
/CP_SP
U10B 74HCT32
/OE_iDB_LD_SP
/2CLK
/SP_OUT_EN
VCC
4.7u C51
VCC
4.7u C52

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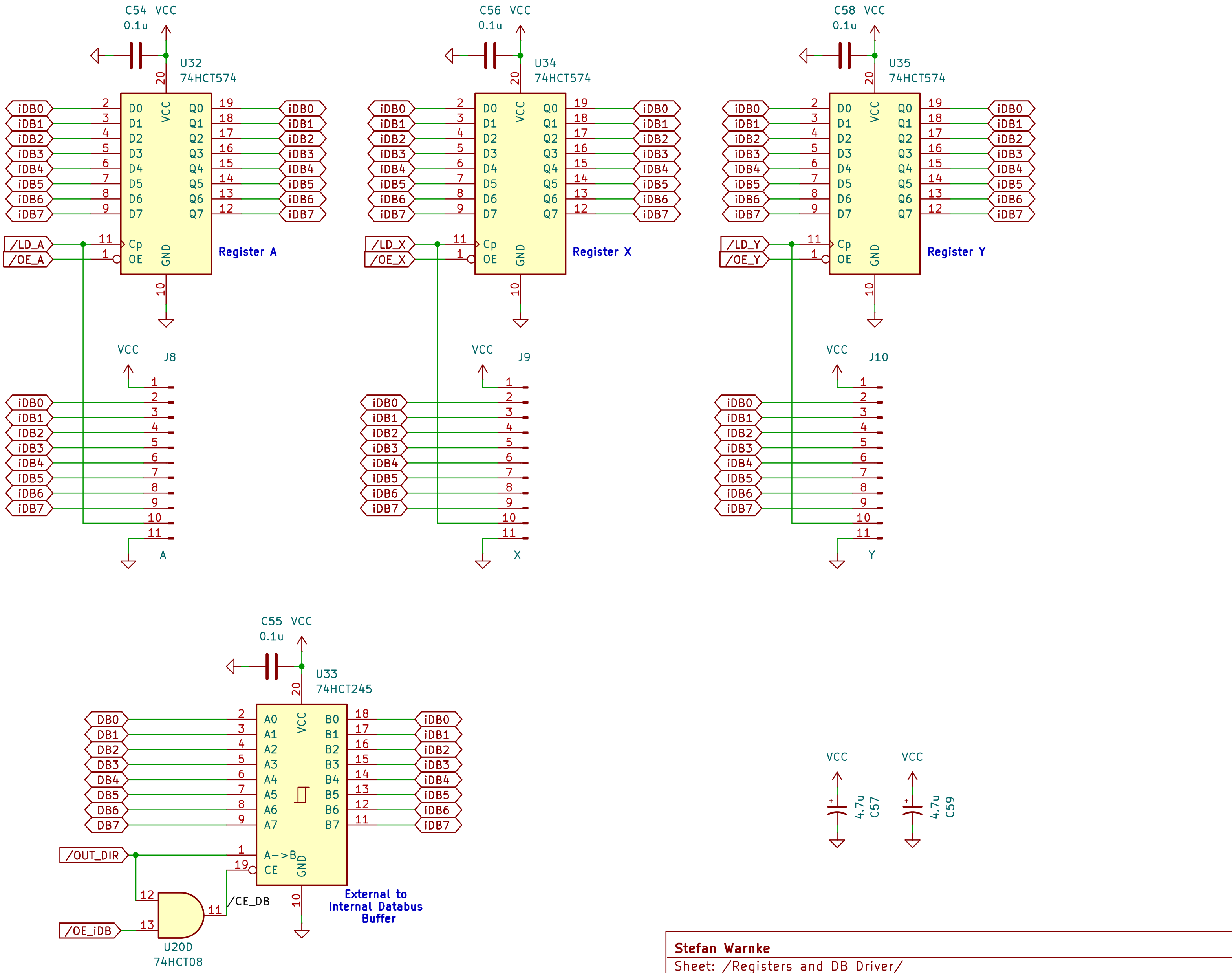
Sheet: /Stack Pointer/
File: Stack_Pointer.kicad_sch

Title: TTL 6510 Computer

Size: A	Date: 2025-02-04	**Rev: A**
KiCad E.D.A. 9.0.4		Id: 5/16


C54 VCC
0.1u
U32
74HCT574
Register A
iDB0 iDB1 iDB2 iDB3 iDB4 iDB5 iDB6 iDB7
D0 D1 D2 D3 D4 D5 D6 D7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
VCC GND Cp OE
/LD_A
/OE_A
C56 VCC
0.1u
U34
74HCT574
Register X
/LD_X
/OE_X
C58 VCC
0.1u
U35
74HCT574
Register Y
/LD_Y
/OE_Y
VCC J8
A
VCC J9
X
VCC J10
Y
C55 VCC
0.1u
U33
74HCT245
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7
A->B
CE
/OUT_DIR
/OE_iDB
/CE_DB
U20D
74HCT08
External to
Internal Databus
Buffer
VCC
4.7u
C57
VCC
4.7u
C59

Stefan Warnke

Sheet: /Registers and DB Driver/
File: Registers_and_DB_Driver.kicad_sch

Title: TTL 6510 Computer

Size: A
Date: 2025-02-04
Rev: A
KiCad E.D.A. 9.0.4
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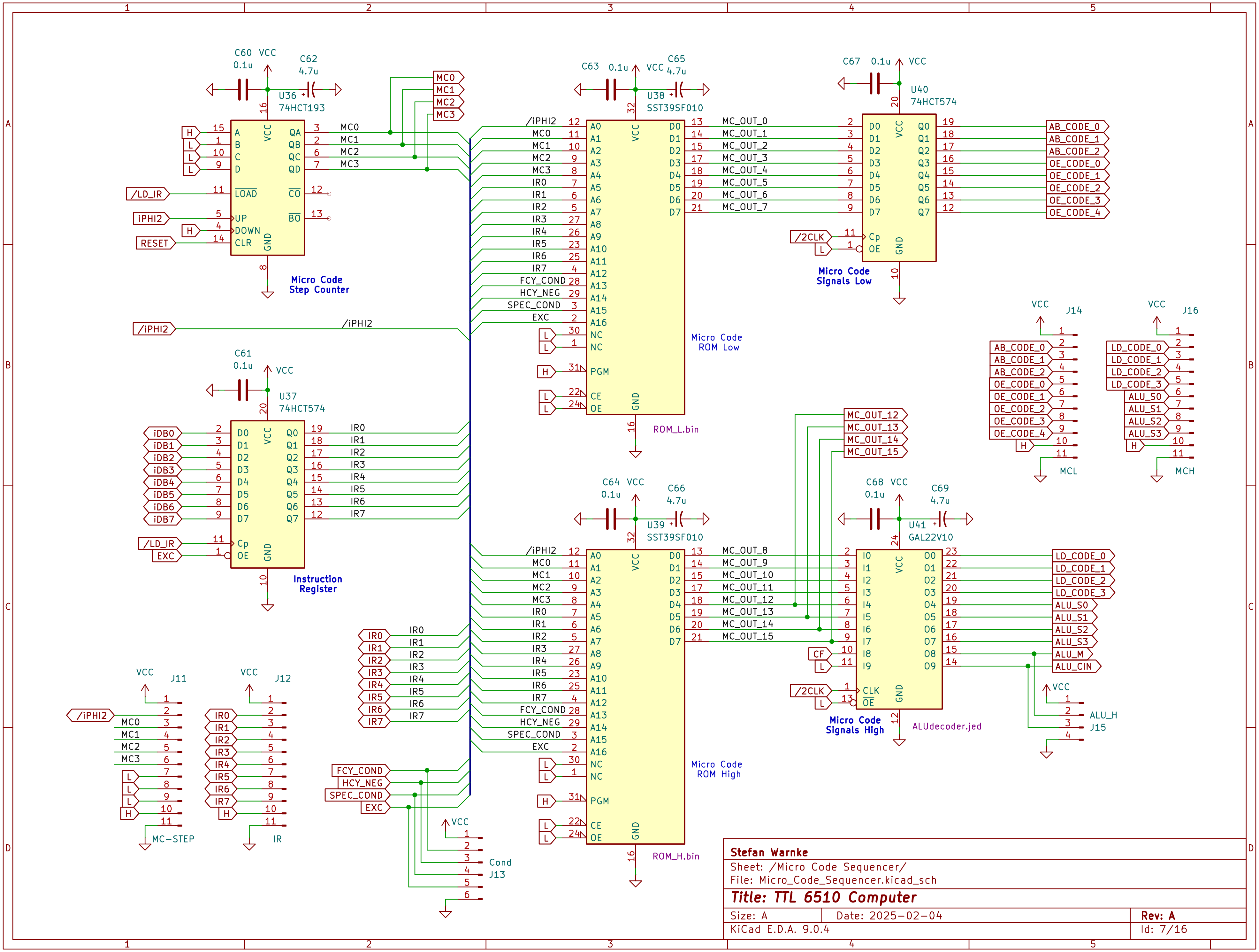

U36 74HCT193
C60 0.1u
C62 4.7u
VCC
A B C D
LOAD
UP
DOWN
CLR
QA QB QC QD
CO
BO
/LD_IR
iPHI2
RESET
Micro Code Step Counter
MC0 MC1 MC2 MC3
U37 74HCT574
C61 0.1u
iDB0 iDB1 iDB2 iDB3 iDB4 iDB5 iDB6 iDB7
IR0 IR1 IR2 IR3 IR4 IR5 IR6 IR7
Cp
OE
EXC
Instruction Register
/iPHI2
U38 SST39SF010
C63 0.1u
C65 4.7u
FCY_COND
HCY_NEG
SPEC_COND
NC
PGM
CE
Micro Code ROM Low
ROM_L.bin
MC_OUT_0 MC_OUT_1 MC_OUT_2 MC_OUT_3 MC_OUT_4 MC_OUT_5 MC_OUT_6 MC_OUT_7
U40 74HCT574
C67 0.1u
/2CLK
Micro Code Signals Low
AB_CODE_0 AB_CODE_1 AB_CODE_2
OE_CODE_0 OE_CODE_1 OE_CODE_2 OE_CODE_3 OE_CODE_4
J14 MCL
J16 MCH
LD_CODE_0 LD_CODE_1 LD_CODE_2 LD_CODE_3
ALU_S0 ALU_S1 ALU_S2 ALU_S3
U39 SST39SF010
C64 0.1u
C66 4.7u
Micro Code ROM High
ROM_H.bin
MC_OUT_8 MC_OUT_9 MC_OUT_10 MC_OUT_11 MC_OUT_12 MC_OUT_13 MC_OUT_14 MC_OUT_15
U41 GAL22V10
C68 0.1u
C69 4.7u
CF
CLK
Micro Code Signals High
ALUdecoder.jed
ALU_M
ALU_CIN
ALU_H
J15
J11 MC−STEP
J12 IR
J13 Cond
GND
H
L

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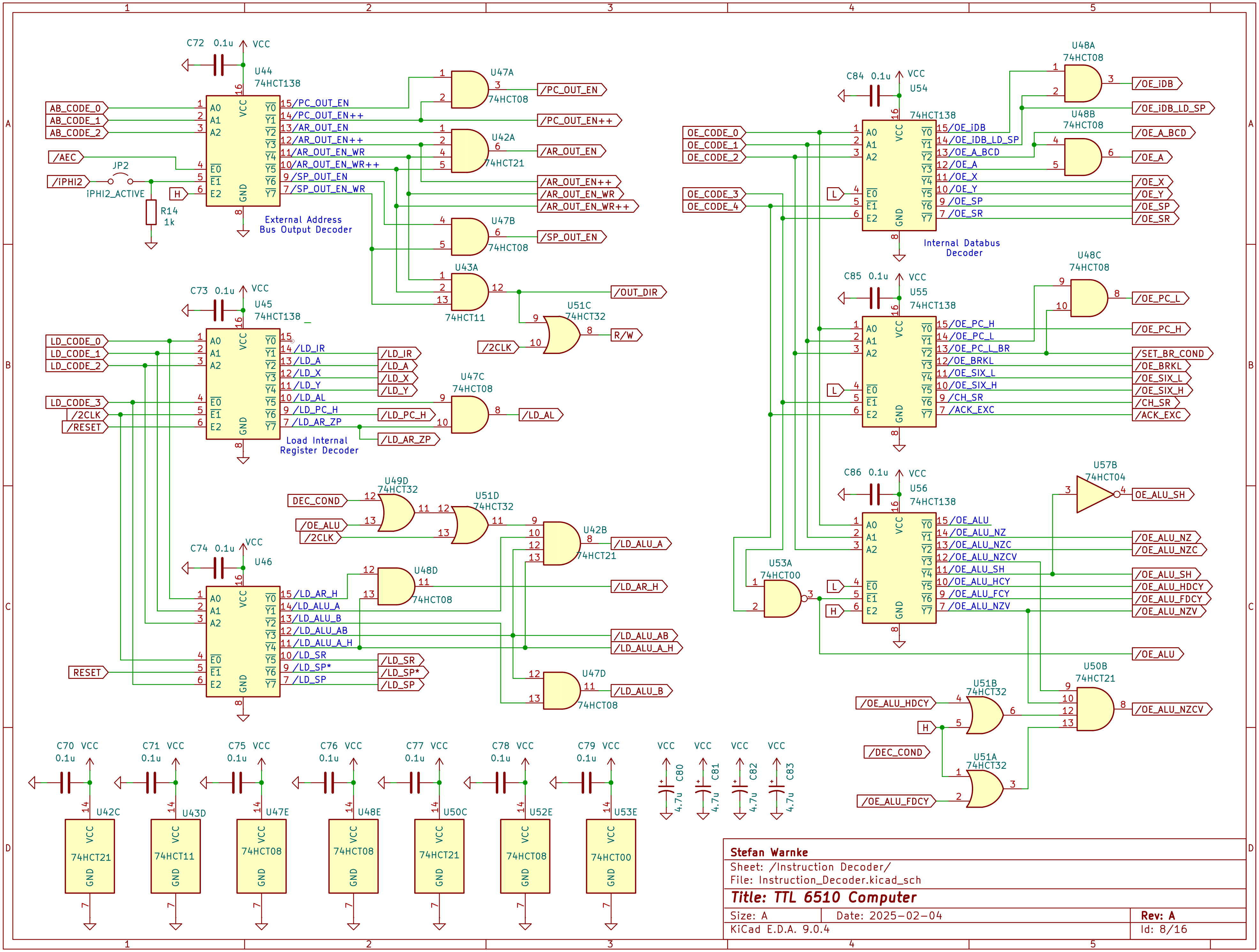
Sheet: /Micro Code Sequencer/

File: Micro_Code_Sequencer.kicad_sch

Title: TTL 6510 Computer

Size: A	Date: 2025-02-04	Rev: A
KiCad E.D.A. 9.0.4		Id: 7/16

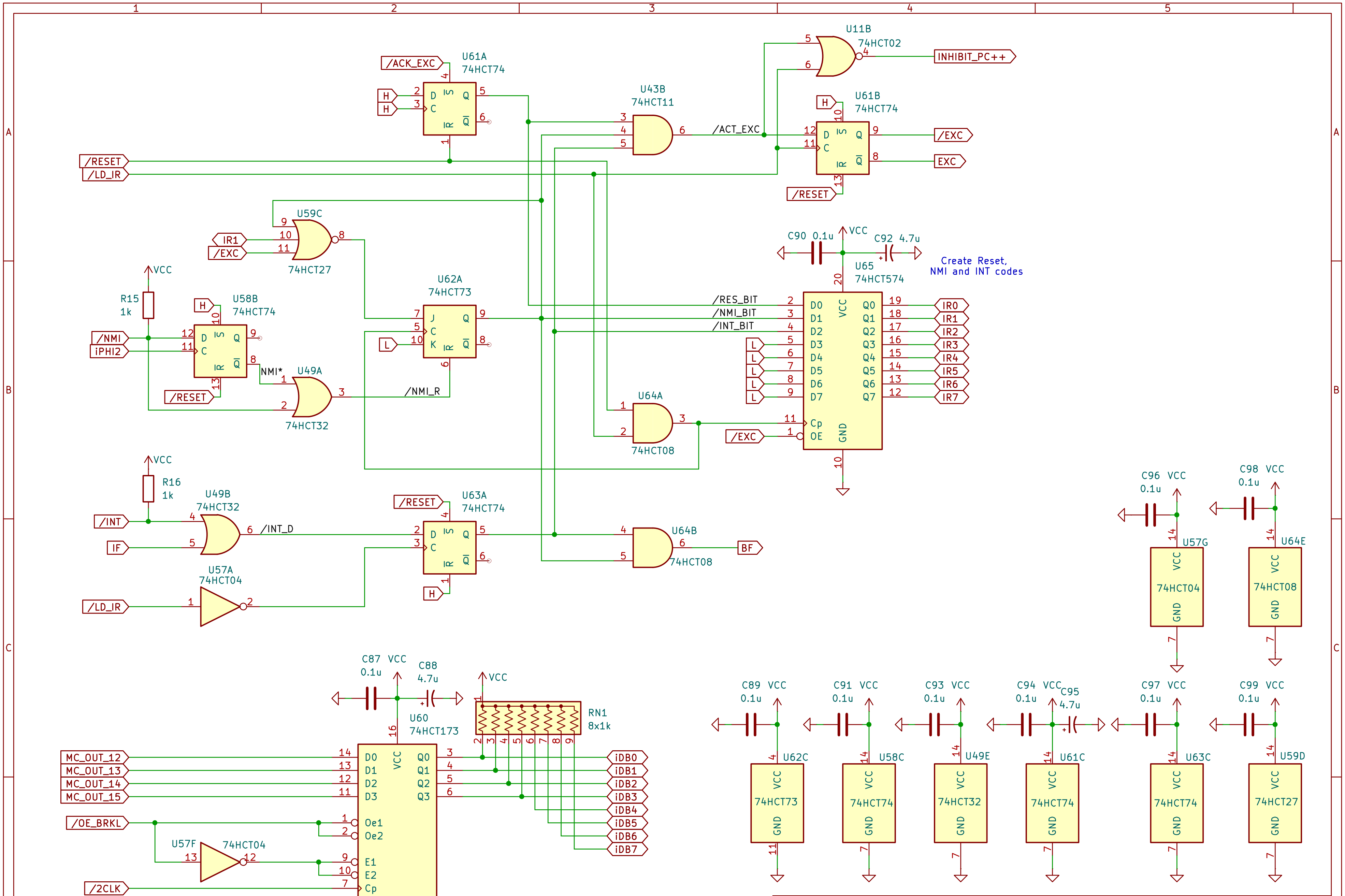


C72 0.1u
VCC
U44
74HCT138
AB_CODE_0
AB_CODE_1
AB_CODE_2
/AEC
/iPHI2
JP2
iPHI2_ACTIVE
R14
1k
H
A0
A1
A2
E0
E1
E2
VCC
GND
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
15 /PC_OUT_EN
14 /PC_OUT_EN++
13 /AR_OUT_EN
12 /AR_OUT_EN++
11 /AR_OUT_EN_WR
10 /AR_OUT_EN_WR++
9 /SP_OUT_EN
7 /SP_OUT_EN_WR
External Address
Bus Output Decoder
U47A
74HCT08
/PC_OUT_EN
/PC_OUT_EN++
U42A
74HCT21
/AR_OUT_EN
/AR_OUT_EN++
/AR_OUT_EN_WR
/AR_OUT_EN_WR++
U47B
74HCT08
/SP_OUT_EN
U43A
74HCT11
/OUT_DIR
U51C
74HCT32
/2CLK
R/W
C73 0.1u
VCC
U45
74HCT138
LD_CODE_0
LD_CODE_1
LD_CODE_2
LD_CODE_3
/2CLK
/RESET
14 /LD_IR
13 /LD_A
12 /LD_X
11 /LD_Y
10 /LD_AL
9 /LD_PC_H
7 /LD_AR_ZP
/LD_IR
/LD_A
/LD_X
/LD_Y
/LD_PC_H
/LD_AR_ZP
U47C
74HCT08
/LD_AL
Load Internal
Register Decoder
DEC_COND
/OE_ALU
/2CLK
U49D
74HCT32
U51D
74HCT32
U42B
74HCT21
/LD_ALU_A
C74 0.1u
VCC
U46
RESET
15 /LD_AR_H
14 /LD_ALU_A
13 /LD_ALU_B
12 /LD_ALU_AB
11 /LD_ALU_A_H
10 /LD_SR
9 /LD_SP*
7 /LD_SP
U48D
74HCT08
/LD_AR_H
/LD_ALU_AB
/LD_ALU_A_H
/LD_SR
/LD_SP*
/LD_SP
U47D
74HCT08
/LD_ALU_B
C84 0.1u
VCC
U54
74HCT138
OE_CODE_0
OE_CODE_1
OE_CODE_2
OE_CODE_3
OE_CODE_4
L
15 /OE_iDB
14 /OE_iDB_LD_SP
13 /OE_A_BCD
12 /OE_A
11 /OE_X
10 /OE_Y
9 /OE_SP
7 /OE_SR
Internal Databus
Decoder
U48A
74HCT08
/OE_iDB
/OE_iDB_LD_SP
U48B
74HCT08
/OE_A_BCD
/OE_A
/OE_X
/OE_Y
/OE_SP
/OE_SR
C85 0.1u
VCC
U55
74HCT138
15 /OE_PC_H
14 /OE_PC_L
13 /OE_PC_L_BR
12 /OE_BRKL
11 /OE_SIX_L
10 /OE_SIX_H
9 /CH_SR
7 /ACK_EXC
U48C
74HCT08
/OE_PC_L
/OE_PC_H
/SET_BR_COND
/OE_BRKL
/OE_SIX_L
/OE_SIX_H
/CH_SR
/ACK_EXC
C86 0.1u
VCC
U56
74HCT138
15 /OE_ALU
14 /OE_ALU_NZ
13 /OE_ALU_NZC
12 /OE_ALU_NZCV
11 /OE_ALU_SH
10 /OE_ALU_HCY
9 /OE_ALU_FCY
7 /OE_ALU_NZV
U57B
74HCT04
OE_ALU_SH
/OE_ALU_NZ
/OE_ALU_NZC
/OE_ALU_SH
/OE_ALU_HDCY
/OE_ALU_FDCY
/OE_ALU_NZV
U53A
74HCT00
/OE_ALU
U50B
74HCT21
/OE_ALU_NZCV
U51B
74HCT32
/OE_ALU_HDCY
/DEC_COND
U51A
74HCT32
/OE_ALU_FDCY
C70 VCC 0.1u
C71 VCC 0.1u
C75 VCC 0.1u
C76 VCC 0.1u
C77 VCC 0.1u
C78 VCC 0.1u
C79 VCC 0.1u
U42C 74HCT21
U43D 74HCT11
U47E 74HCT08
U48E 74HCT08
U50C 74HCT21
U52E 74HCT08
U53E 74HCT00
VCC
C80 4.7u
C81 4.7u
C82 4.7u
C83 4.7u
1
2
3
4
5
A
B
C
D

Stefan Warnke
Sheet: /Instruction Decoder/
File: Instruction_Decoder.kicad_sch

Title: TTL 6510 Computer

Size: A	Date: 2025-02-04	**Rev: A**
KiCad E.D.A. 9.0.4		Id: 8/16

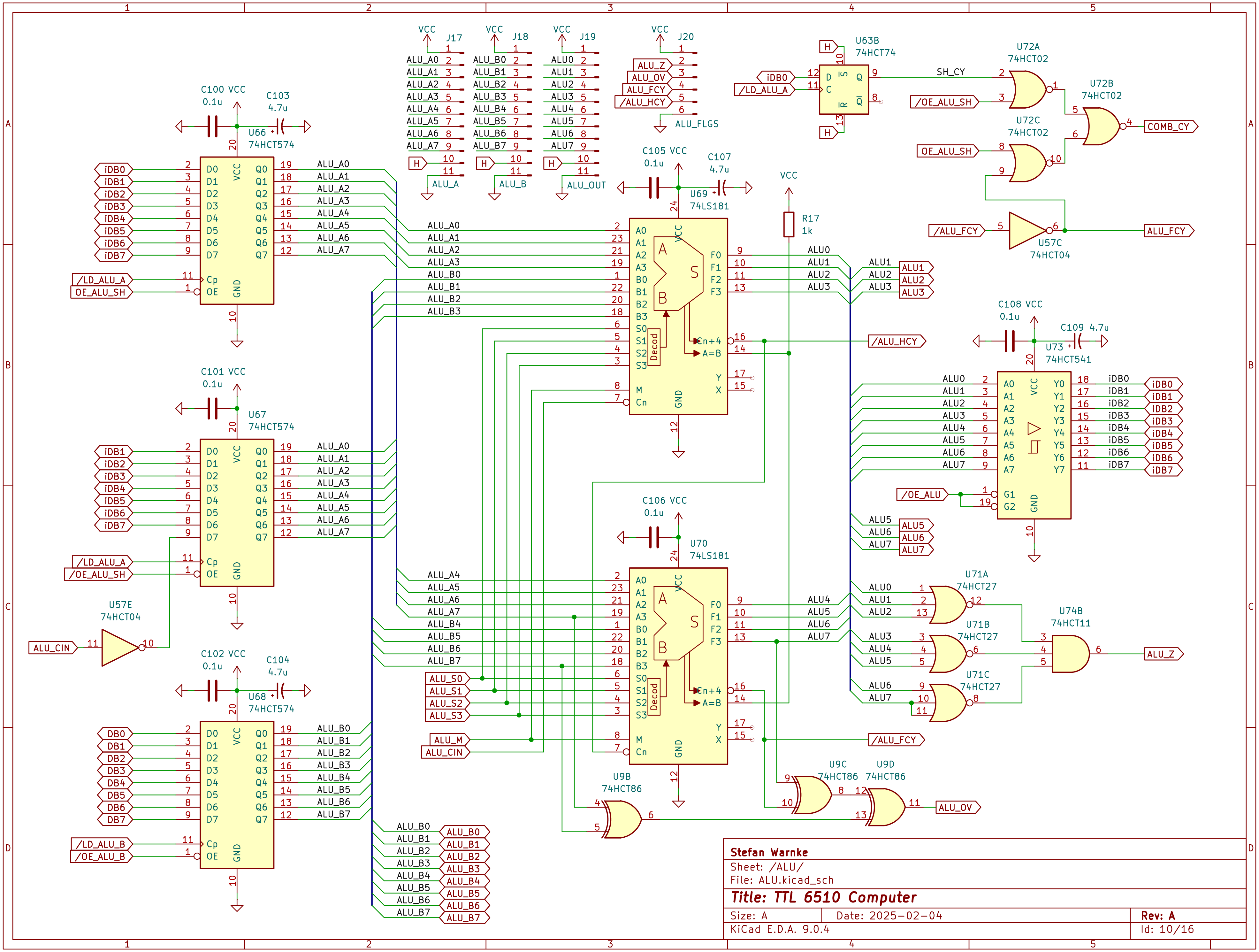

/ACK_EXC
U61A
74HCT74
U11B
74HCT02
INHIBIT_PC++
U43B
74HCT11
/ACT_EXC
U61B
74HCT74
/EXC
EXC
/RESET
/LD_IR
U59C
74HCT27
IR1
/EXC
C90 0.1u
VCC
C92 4.7u
U65
74HCT574
Create Reset,
NMI and INT codes
R15
1k
U58B
74HCT74
/NMI
iPHI2
NMI*
U62A
74HCT73
U49A
74HCT32
/NMI_R
/RES_BIT
/NMI_BIT
/INT_BIT
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
U64A
74HCT08
R16
1k
U49B
74HCT32
/INT
IF
/INT_D
U63A
74HCT74
U64B
74HCT08
BF
U57A
74HCT04
C96 0.1u
C98 0.1u
U57G
74HCT04
U64E
74HCT08
C87 0.1u
C88 4.7u
U60
74HCT173
RN1
8x1k
MC_OUT_12
MC_OUT_13
MC_OUT_14
MC_OUT_15
/OE_BRKL
U57F
74HCT04
/2CLK
RESET
iDB0
iDB1
iDB2
iDB3
iDB4
iDB5
iDB6
iDB7
Create Reset,
NMI and Int addresses
C89 0.1u
C91 0.1u
C93 0.1u
C94 0.1u
C95 4.7u
C97 0.1u
C99 0.1u
U62C
74HCT73
U58C
74HCT74
U49E
74HCT32
U61C
74HCT74
U63C
74HCT74
U59D
74HCT27

Stefan Warnke

Sheet: /Exception Handling/
File: Exception_Handling.kicad_sch

Title: TTL 6510 Computer

Size: A
Date: 2025-02-04
Rev: A
KiCad E.D.A. 9.0.4
Id: 9/16


U66
74HCT574
U67
74HCT574
U68
74HCT574
U69
74LS181
U70
74LS181
U73
74HCT541
U63B
74HCT74
U72A
74HCT02
U72B
74HCT02
U72C
74HCT02
U57C
74HCT04
U57E
74HCT04
U71A
74HCT27
U71B
74HCT27
U71C
74HCT27
U74B
74HCT11
U9B
74HCT86
U9C
74HCT86
U9D
74HCT86
C100 VCC
0.1u
C101 VCC
0.1u
C102 VCC
0.1u
C103
4.7u
C104
4.7u
C105 VCC
0.1u
C106 VCC
0.1u
C107
4.7u
C108 VCC
0.1u
C109 4.7u
R17
1k
J17
J18
J19
J20
VCC
ALU_A
ALU_B
ALU_OUT
ALU_FLGS
iDB0
iDB1
iDB2
iDB3
iDB4
iDB5
iDB6
iDB7
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
/LD_ALU_A
OE_ALU_SH
/OE_ALU_SH
/LD_ALU_B
/OE_ALU_B
ALU_CIN
ALU_A0
ALU_A1
ALU_A2
ALU_A3
ALU_A4
ALU_A5
ALU_A6
ALU_A7
ALU_B0
ALU_B1
ALU_B2
ALU_B3
ALU_B4
ALU_B5
ALU_B6
ALU_B7
ALU0
ALU1
ALU2
ALU3
ALU4
ALU5
ALU6
ALU7
ALU_Z
ALU_OV
ALU_FCY
/ALU_FCY
/ALU_HCY
ALU_S0
ALU_S1
ALU_S2
ALU_S3
ALU_M
SH_CY
COMB_CY
/OE_ALU
H
Decod
Cn+4
A=B
D0 D1 D2 D3 D4 D5 D6 D7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
Cp
OE
A0 A1 A2 A3 B0 B1 B2 B3
S0 S1 S2 S3
M
Cn
F0 F1 F2 F3
Y
X
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
G1
G2
GND
1 2 3 4 5
A B C D

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Sheet: /ALU/
File: ALU.kicad_sch

Title: TTL 6510 Computer

Size: A
Date: 2025-02-04
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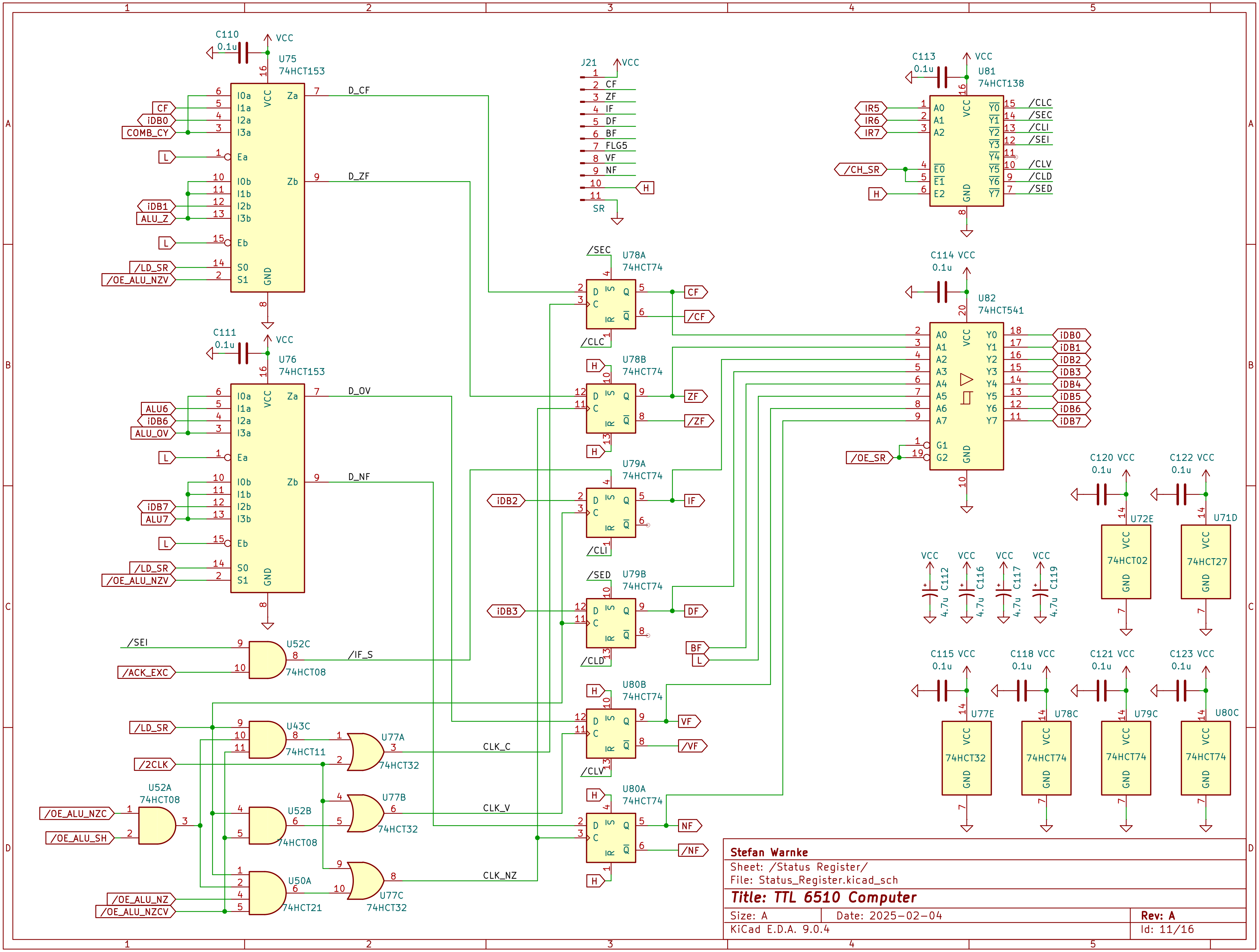
1
2
3
4
5
A
B
C
D
C110
0.1u
VCC
U75
74HCT153
I0a
I1a
I2a
I3a
Ea
I0b
I1b
I2b
I3b
Eb
S0
S1
Za
Zb
GND
CF
iDB0
COMB_CY
L
iDB1
ALU_Z
/LD_SR
/OE_ALU_NZV
D_CF
D_ZF
C111
0.1u
U76
74HCT153
ALU6
iDB6
ALU_OV
iDB7
ALU7
D_OV
D_NF
/SEI
/ACK_EXC
U52C
74HCT08
/IF_S
U43C
74HCT11
/2CLK
U77A
74HCT32
CLK_C
U52A
74HCT08
/OE_ALU_NZC
/OE_ALU_SH
U52B
74HCT08
U77B
74HCT32
CLK_V
U50A
74HCT21
/OE_ALU_NZ
/OE_ALU_NZCV
U77C
74HCT32
CLK_NZ
J21
VCC
1
2 CF
3 ZF
4 IF
5 DF
6 BF
7 FLG5
8 VF
9 NF
10
11
SR
H
/SEC
U78A
74HCT74
/CF
/CLC
U78B
74HCT74
ZF
/ZF
U79A
74HCT74
iDB2
IF
/CLI
/SED
U79B
74HCT74
iDB3
DF
/CLD
BF
U80B
74HCT74
VF
/VF
/CLV
U80A
74HCT74
NF
/NF
C113
0.1u
U81
74HCT138
IR5
IR6
IR7
/CH_SR
A0
A1
A2
E0
E1
E2
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
/CLC
/SEC
/CLI
/SEI
/CLV
/CLD
/SED
C114 VCC
0.1u
U82
74HCT541
A0
A1
A2
A3
A4
A5
A6
A7
G1
G2
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
iDB0
iDB1
iDB2
iDB3
iDB4
iDB5
iDB6
iDB7
/OE_SR
C120 VCC
0.1u
C122 VCC
0.1u
U72E
74HCT02
U71D
74HCT27
C112
4.7u
C116
4.7u
C117
4.7u
C119
4.7u
C115 VCC
0.1u
C118 VCC
0.1u
C121 VCC
0.1u
C123 VCC
0.1u
U77E
74HCT32
U78C
74HCT74
U79C
74HCT74
U80C
74HCT74

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Sheet: /Status Register/
File: Status_Register.kicad_sch

Title: TTL 6510 Computer

Size: A
Date: 2025-02-04
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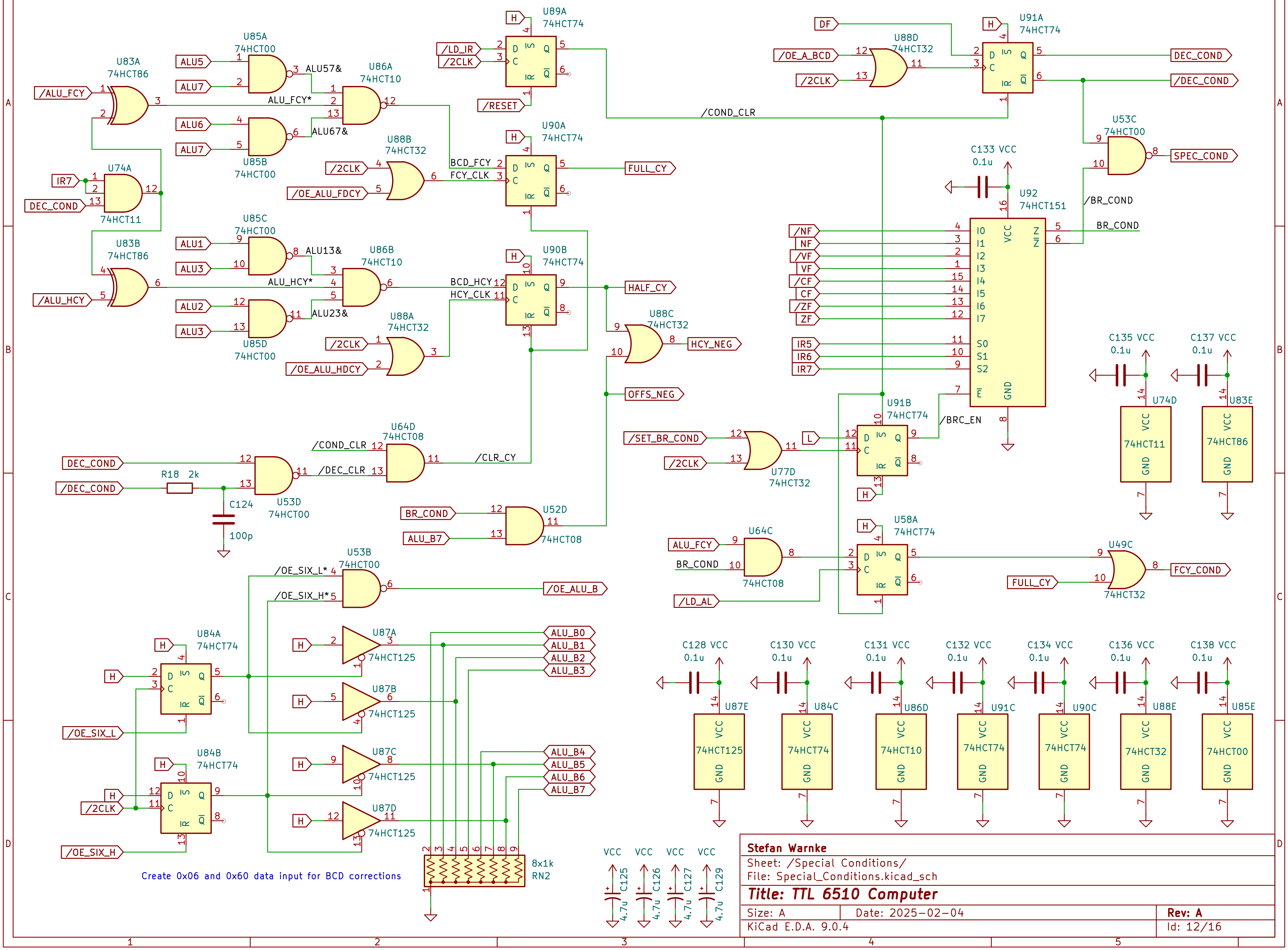
U83A 74HCT86
/ALU_FCY
U85A 74HCT00
ALU5
ALU7
ALU57&
U86A 74HCT10
ALU_FCY*
ALU6
ALU67&
U85B 74HCT00
IR7
U74A
DEC_COND
74HCT11
U89A 74HCT74
H
/LD_IR
/2CLK
/RESET
U88B 74HCT32
/OE_ALU_FDCY
BCD_FCY
FCY_CLK
U90A 74HCT74
FULL_CY
/COND_CLR
U83B 74HCT86
/ALU_HCY
U85C 74HCT00
ALU1
ALU3
ALU13&
U86B 74HCT10
ALU_HCY*
ALU2
ALU23&
U85D 74HCT00
U88A 74HCT32
/OE_ALU_HDCY
BCD_HCY
HCY_CLK
U90B 74HCT74
HALF_CY
U88C 74HCT32
HCY_NEG
OFFS_NEG
U64D 74HCT08
/CLR_CY
/DEC_CLR
/DEC_COND
R18 2k
C124 100p
U53D 74HCT00
BR_COND
ALU_B7
U52D 74HCT08
U53B 74HCT00
/OE_SIX_L*
/OE_SIX_H*
/OE_ALU_B
U84A 74HCT74
/OE_SIX_L
U84B 74HCT74
/OE_SIX_H
U87A 74HCT125
U87B 74HCT125
U87C 74HCT125
U87D 74HCT125
ALU_B0
ALU_B1
ALU_B2
ALU_B3
ALU_B4
ALU_B5
ALU_B6
8x1k RN2
DF
/OE_A_BCD
U88D 74HCT32
U91A 74HCT74
DEC_COND
/DEC_COND
U53C 74HCT00
SPEC_COND
C133 VCC 0.1u
U92 74HCT151
/BR_COND
/NF
NF
/VF
VF
/CF
CF
/ZF
ZF
IR5
IR6
IR7
I0 I1 I2 I3 I4 I5 I6 I7
S0 S1 S2
E
Z
VCC
GND
U91B 74HCT74
/BR_EN
/SET_BR_COND
L
U77D 74HCT32
U58A 74HCT74
ALU_FCY
U64C 74HCT08
/LD_AL
U49C 74HCT32
FCY_COND
C135 VCC 0.1u
C137 VCC 0.1u
U74D 74HCT11
U83E 74HCT86
C128 VCC 0.1u
C130 VCC 0.1u
C131 VCC 0.1u
C132 VCC 0.1u
C134 VCC 0.1u
C136 VCC 0.1u
C138 VCC 0.1u
U87E 74HCT125
U84C 74HCT74
U86D 74HCT10
U91C 74HCT74
U90C 74HCT74
U88E 74HCT32
U85E 74HCT00
C125 4.7u
C126 4.7u
C127 4.7u
C129 4.7u
1 2 3 4 5
A B C D

Create 0x06 and 0x60 data input for BCD corrections

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Sheet: /Special Conditions/

File: Special_Conditions.kicad_sch

Title: TTL 6510 Computer

Size: A Date: 2025-02-04 **Rev: A**

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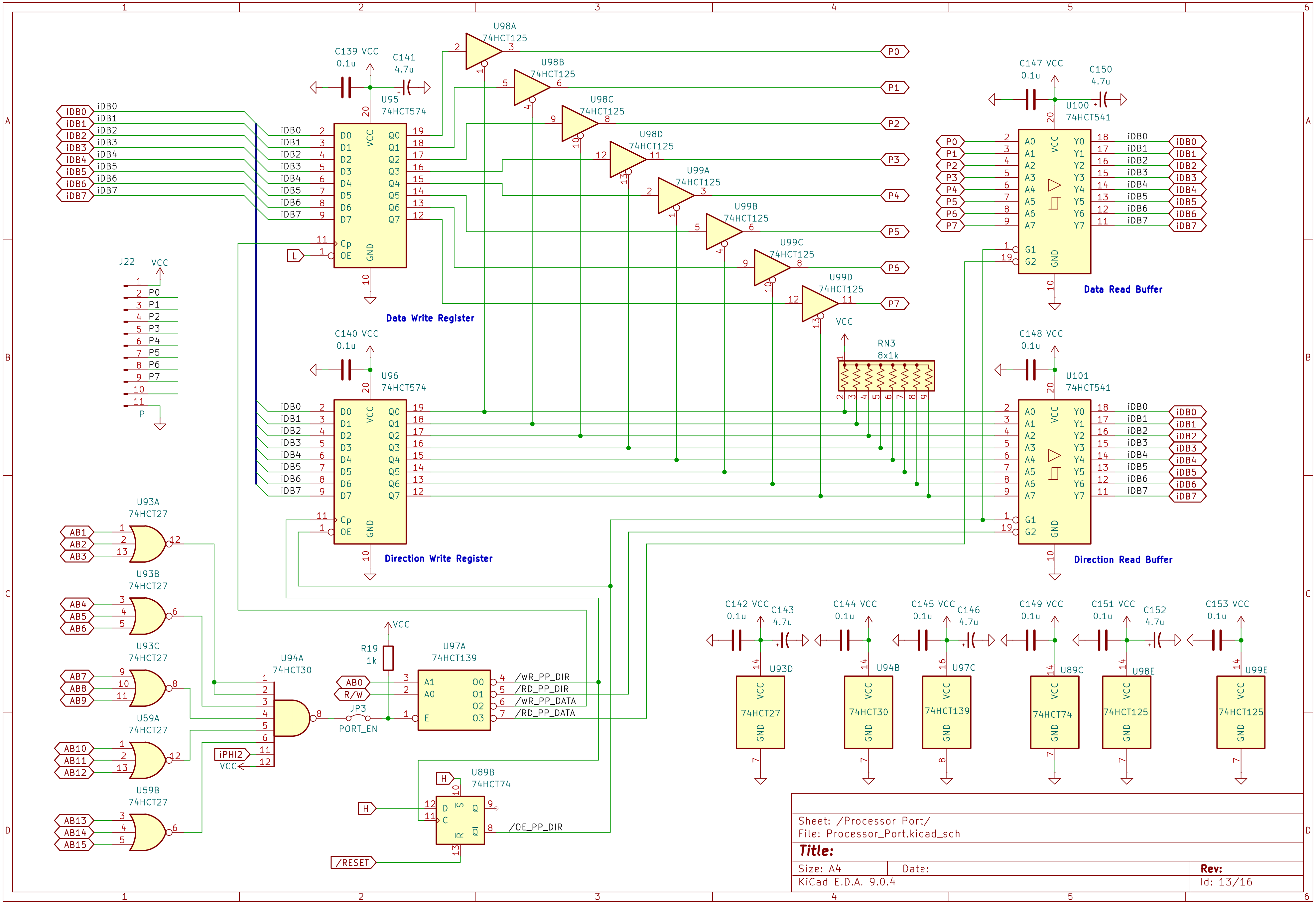
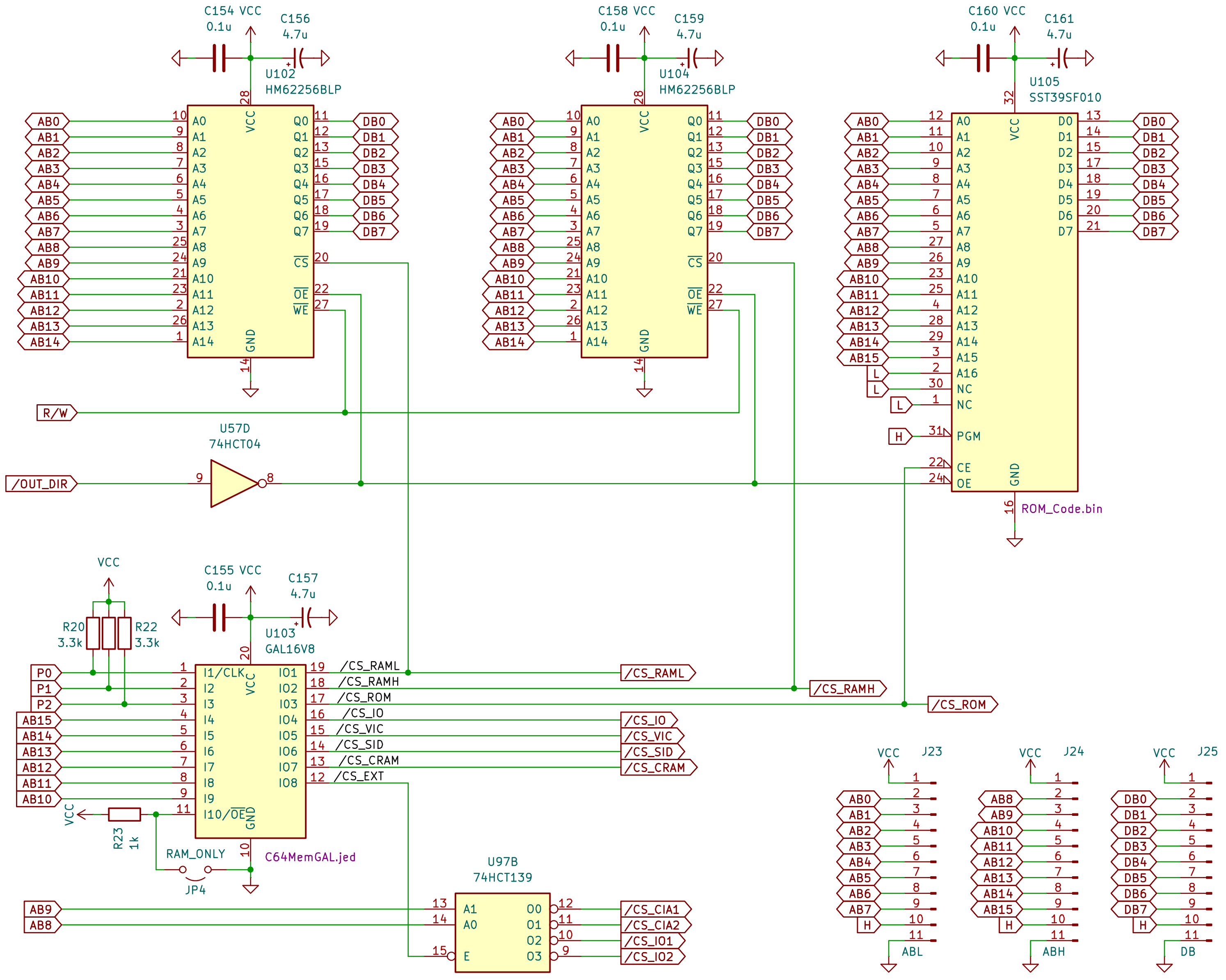

Data Write Register
U95
74HCT574
C139 VCC
0.1u
C141
4.7u
iDB0
iDB1
iDB2
iDB3
iDB4
iDB5
iDB6
iDB7
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Cp
OE
VCC
GND
L
U98A
U98B
U98C
U98D
U99A
U99B
U99C
U99D
74HCT125
P0
P1
P2
P3
P4
P5
P6
P7
J22
VCC
P
Direction Write Register
U96
74HCT574
C140 VCC
0.1u
Data Read Buffer
U100
74HCT541
C147 VCC
0.1u
C150
4.7u
A0
A1
A2
A3
A4
A5
A6
A7
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
G1
G2
Direction Read Buffer
U101
74HCT541
C148 VCC
0.1u
RN3
8x1k
U93A
U93B
U93C
U59A
U59B
74HCT27
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AB8
AB9
AB10
AB11
AB12
AB13
AB14
AB15
U94A
74HCT30
iPHI2
R19
1k
JP3
PORT_EN
U97A
74HCT139
AB0
R/W
E
O0
O1
O2
O3
/WR_PP_DIR
/RD_PP_DIR
/WR_PP_DATA
/RD_PP_DATA
U89B
74HCT74
H
D
C
S
R
Q
/OE_PP_DIR
/RESET
C142 VCC
0.1u
C143
4.7u
U93D
74HCT27
C144 VCC
0.1u
U94B
74HCT30
C145 VCC
0.1u
C146
4.7u
U97C
74HCT139
C149 VCC
0.1u
U89C
74HCT74
C151 VCC
0.1u
C152
4.7u
U98E
74HCT125
C153 VCC
0.1u
U99E
74HCT125

Sheet: /Processor Port/
File: Processor_Port.kicad_sch

Title:

Size: A4 Date:
KiCad E.D.A. 9.0.4

Rev:
Id: 13/16



C154 VCC
0.1u
C156
4.7u
U102
HM62256BLP
C158 VCC
0.1u
C159
4.7u
U104
HM62256BLP
C160 VCC
0.1u
C161
4.7u
U105
SST39SF010
AB0
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AB8
AB9
AB10
AB11
AB12
AB13
AB14
AB15
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
VCC
GND
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
D0
D1
D2
D3
D4
D5
D6
D7
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
CS
OE
WE
NC
PGM
CE
L
H
R/W
/OUT_DIR
U57D
74HCT04
ROM_Code.bin
VCC
R20
3.3k
R22
3.3k
C155 VCC
0.1u
C157
4.7u
U103
GAL16V8
P0
P1
P2
I1/CLK
I2
I3
I4
I5
I6
I7
I8
I9
I10/OE
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
/CS_RAML
/CS_RAMH
/CS_ROM
/CS_IO
/CS_VIC
/CS_SID
/CS_CRAM
/CS_EXT
R23
1k
RAM_ONLY
JP4
C64MemGAL.jed
U97B
74HCT139
A1
A0
E
O0
O1
O2
O3
/CS_CIA1
/CS_CIA2
/CS_IO1
/CS_IO2
J23
J24
J25
ABL
ABH
DB

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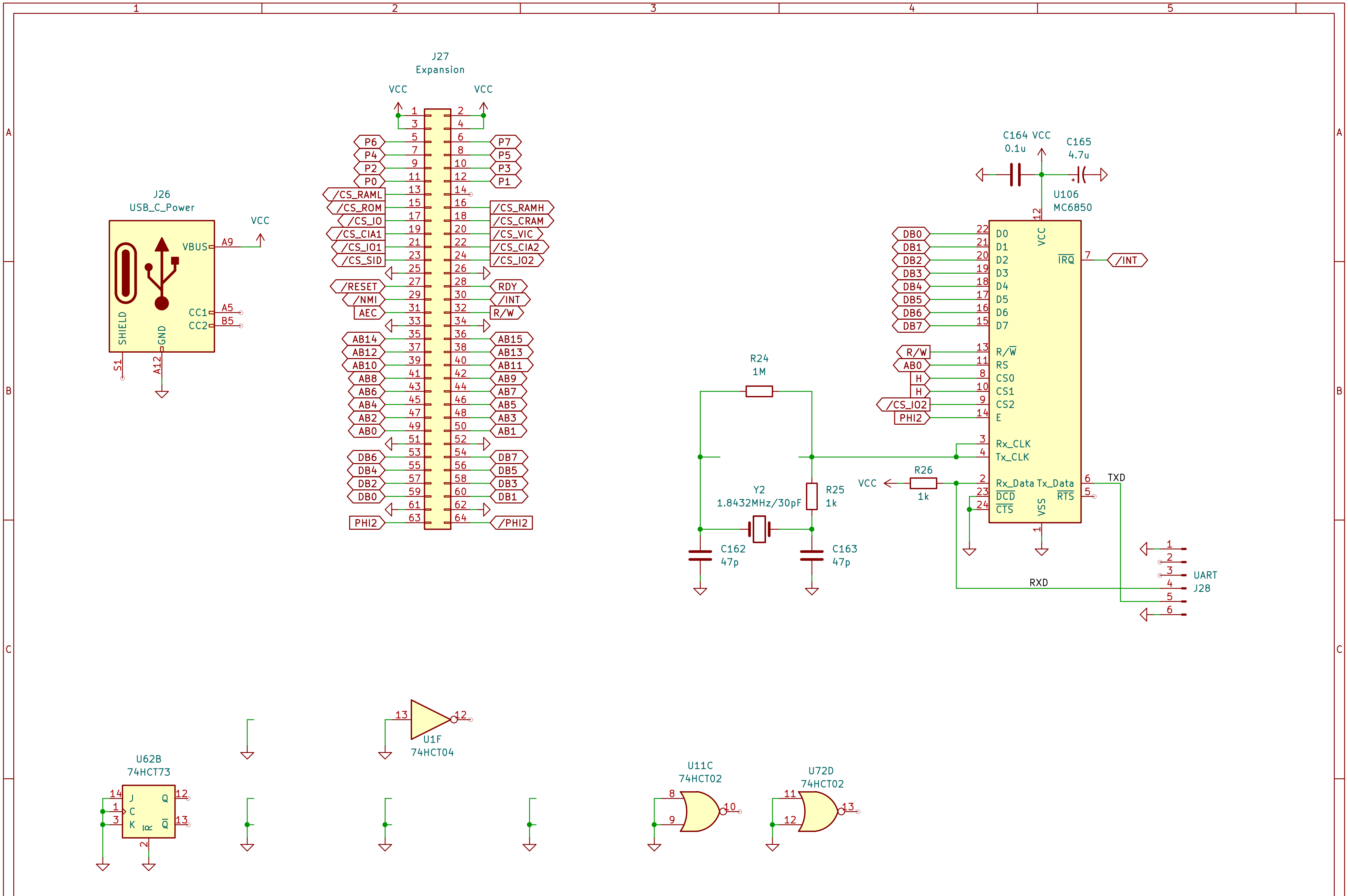
Sheet: /External Memory/
File: External_Memory.kicad_sch

Title: TTL 6510 Computer

Size: A | Date: 2025-02-04 | **Rev: A**
KiCad E.D.A. 9.0.4 | Id: 14/16


J27
Expansion
VCC
VCC
P6
P7
P4
P5
P2
P3
P0
P1
/CS_RAML
/CS_ROM
/CS_IO
/CS_CIA1
/CS_IO1
/CS_SID
/CS_RAMH
/CS_CRAM
/CS_VIC
/CS_CIA2
/CS_IO2
/RESET
/NMI
AEC
RDY
/INT
R/W
AB14
AB12
AB10
AB8
AB6
AB4
AB2
AB0
AB15
AB13
AB11
AB9
AB7
AB5
AB3
AB1
DB6
DB4
DB2
DB0
DB7
DB5
DB3
DB1
PHI2
/PHI2
J26
USB_C_Power
VBUS
A9
VCC
CC1
A5
CC2
B5
SHIELD
GND
S1
A12
C164
0.1u
VCC
C165
4.7u
U106
MC6850
D0
D1
D2
D3
D4
D5
D6
D7
R/W
RS
CS0
CS1
CS2
E
Rx_CLK
Tx_CLK
Rx_Data
DCD
CTS
Tx_Data
RTS
IRQ
VCC
VSS
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
R/W
AB0
H
H
/CS_IO2
PHI2
/INT
TXD
RXD
R24
1M
R25
1k
R26
1k
VCC
Y2
1.8432MHz/30pF
C162
47p
C163
47p
UART
J28
U1F
74HCT04
U62B
74HCT73
J
C
K
Q
R
U11C
74HCT02
U72D
74HCT02

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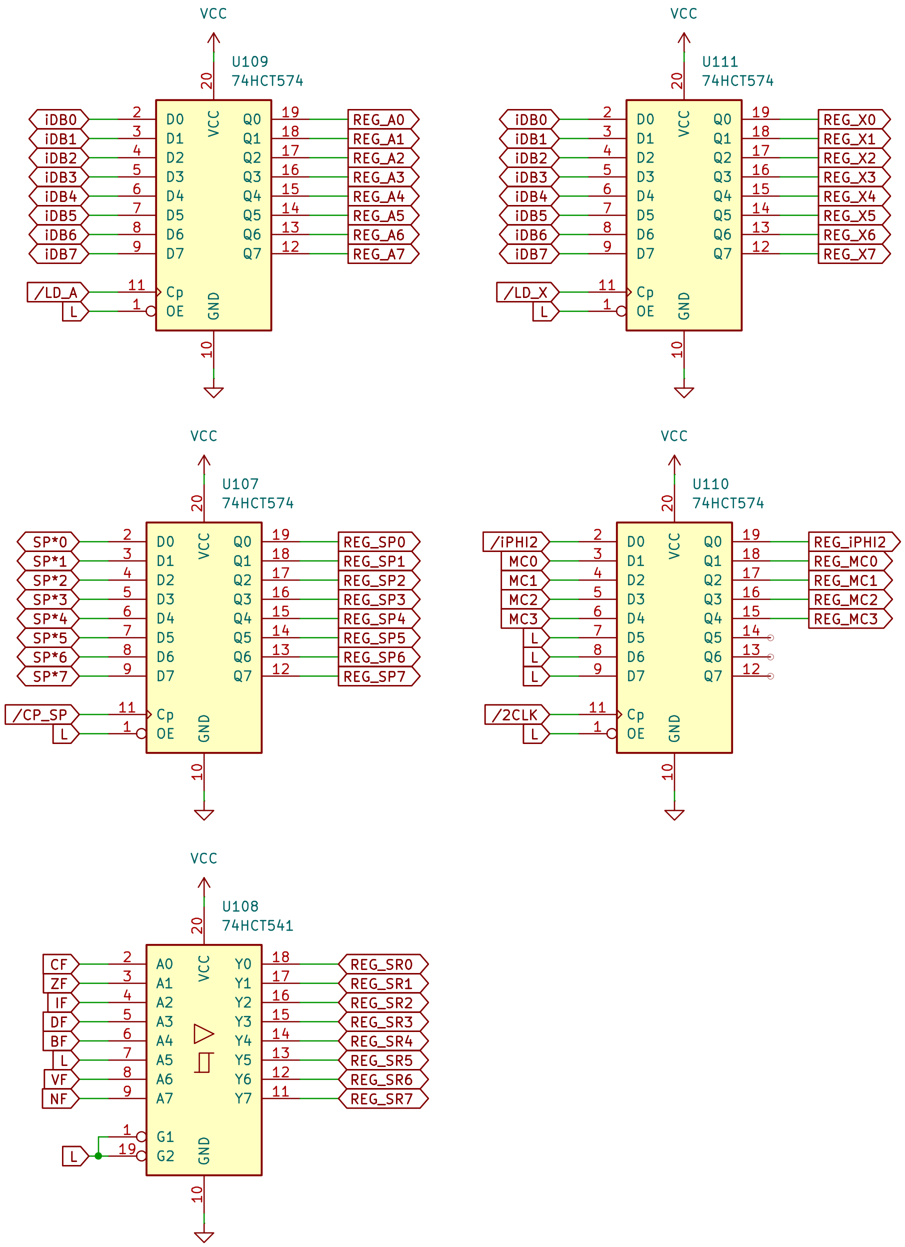
Sheet: /Miscellaneous/
File: Miscellaneous.kicad_sch

Title: TTL 6510 Computer

Size: A	Date: 2025-02-04	**Rev: A**
KiCad E.D.A. 9.0.4		Id: 15/16


VCC
U109
74HCT574
iDB0
iDB1
iDB2
iDB3
iDB4
iDB5
iDB6
iDB7
/LD_A
L
REG_A0
REG_A1
REG_A2
REG_A3
REG_A4
REG_A5
REG_A6
REG_A7
U111
74HCT574
/LD_X
REG_X0
REG_X1
REG_X2
REG_X3
REG_X4
REG_X5
REG_X6
REG_X7
U112
74HCT574
/LD_Y
REG_Y0
REG_Y1
REG_Y2
REG_Y3
REG_Y4
REG_Y5
REG_Y6
REG_Y7
U107
74HCT574
SP*0
SP*1
SP*2
SP*3
SP*4
SP*5
SP*6
SP*7
/CP_SP
REG_SP0
REG_SP1
REG_SP2
REG_SP3
REG_SP4
REG_SP5
REG_SP6
REG_SP7
U110
74HCT574
/iPHI2
MC0
MC1
MC2
MC3
/2CLK
REG_iPHI2
REG_MC0
REG_MC1
REG_MC2
REG_MC3
U113
74HCT574
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
REG_IR0
REG_IR1
REG_IR2
REG_IR3
REG_IR4
REG_IR5
REG_IR6
REG_IR7
U108
74HCT541
CF
ZF
IF
DF
BF
VF
NF
REG_SR0
REG_SR1
REG_SR2
REG_SR3
REG_SR4
REG_SR5
REG_SR6
REG_SR7
D0 D1 D2 D3 D4 D5 D6 D7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
Cp
OE
GND
A0 A1 A2 A3 A4 A5 A6 A7
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
G1
G2

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Sheet: /DigiSim_Regs/
File: DigiSim_Regs.kicad_sch

Title: TTL 6510 Computer

Size: A	Date: 2025-02-04	**Rev: A**
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