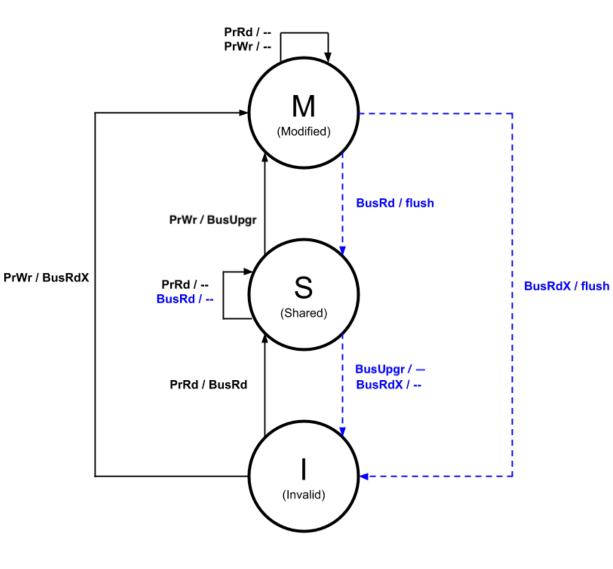
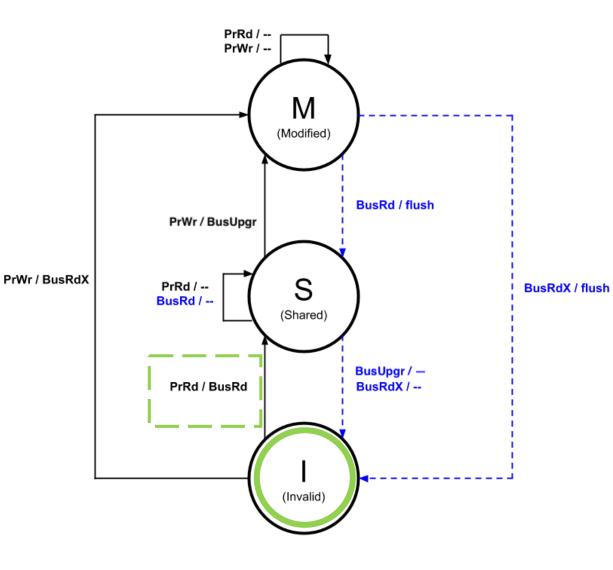
1. Given an SMP system with 3 CPUs, each with its own cache memory initially empty. To keep caches coherent the system uses a Snoopy-based write-invalidate MSI coherence protocol. Assuming the following sequence of memory instructions all accessing the same memory direction: r1, w1, r2, w3, r2, w1, w2, r3, r2, r1 (where rx indicates read by processor x and wy write by processor y), fill in the table indicating including the CPU event (PrRd, PrWr), Bus transactions (BusRd, BusRdX, BusUpgr, Flush) and state of the cache line (M, S, I) in each cache memory after each access to memory. In the observations column indicate who is providing the line when a cache requires it and when main memory is updated.

Memory	CPU		Bus	Cac	he Line S	tate	
Access	event	hit/miss	transaction(s)	Cache1	Cache2	Cache3	Observations
r1							
w1							
r2							
w3							
r2							
w1							
w2							
r3							
r2							
r1							

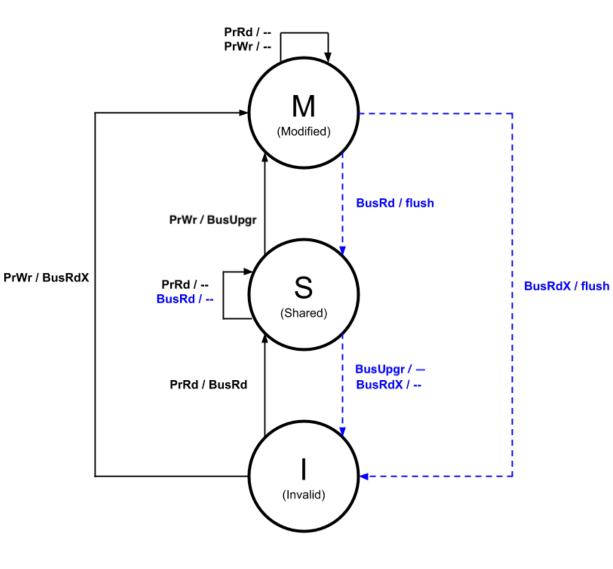
What would change in the table if a *MESI* protocol is used instead of the original *MSI*?



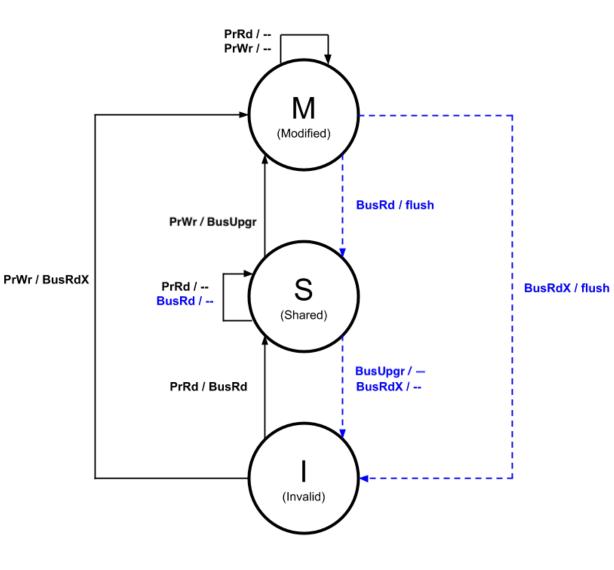
	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1					
w1					
r2					
w3					
r2					
w1					
w2					
r3					
r2					
<b>r1</b>					



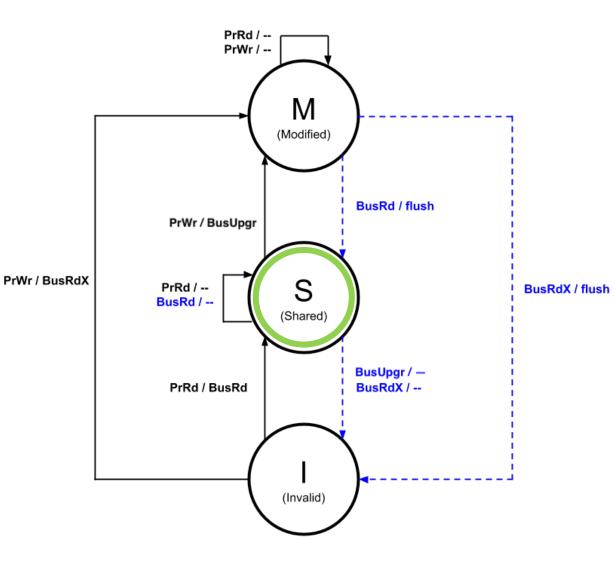
		Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd			
w1						
r2						
w3						
r2						
w1						
w2						
r3						
r2						
r1						



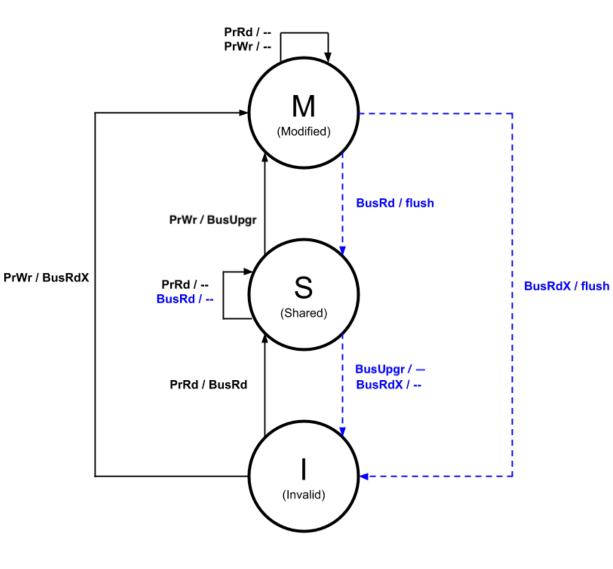
	CPU event	1 -	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	l	I
w1						
r2						
w3						
r2						
w1						
w2						
r3						
r2						
r1						



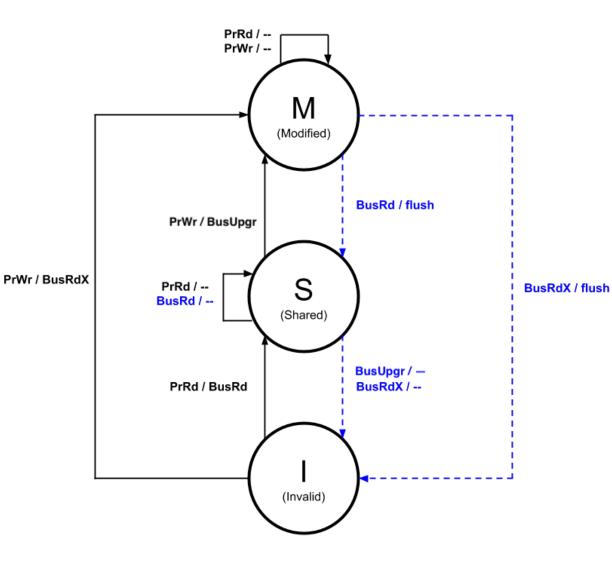
		1 -	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	l	I
w1						
r2						
w3						
r2						
w1						
w2						
r3						
r2						
r1						



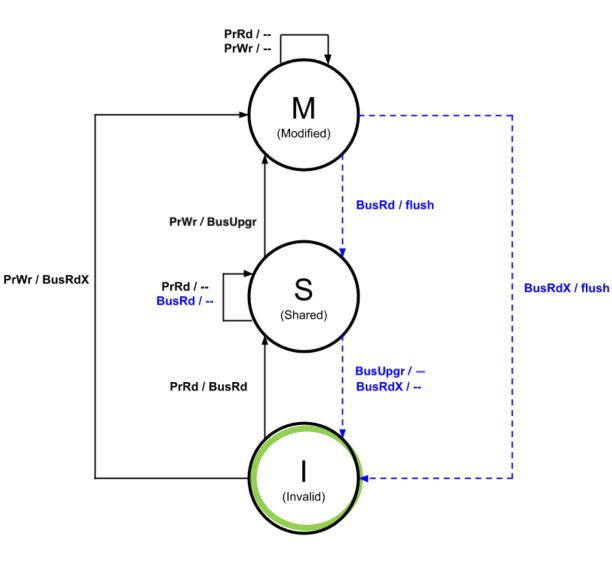
	CPU event		Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	
w1	PrWr	Hit	BusUpgr			
r2						
w3						
r2						
w1						
w2						
r3						
r2						
r1						



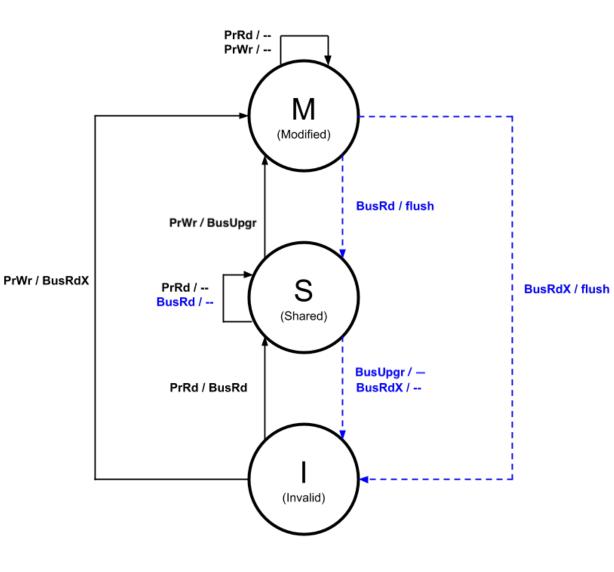
		1 -	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	l	l
w1	PrWr	Hit	BusUpgr	M	<b>I</b>	l I
r2						
w3						
r2						
w1						
w2						
r3						
r2						
<b>r1</b>						



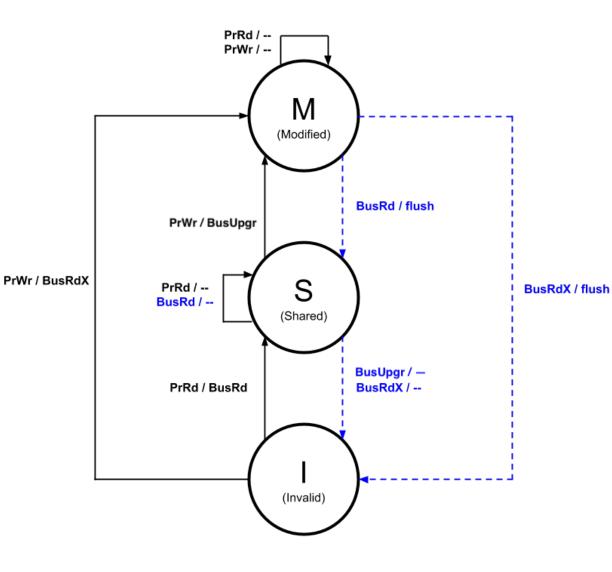
	CPU event	1 *	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	1	I
w1	PrWr	Hit	BusUpgr	М	I	I
r2						
w3						
r2						
w1						
w2						
r3						
r2						
r1						



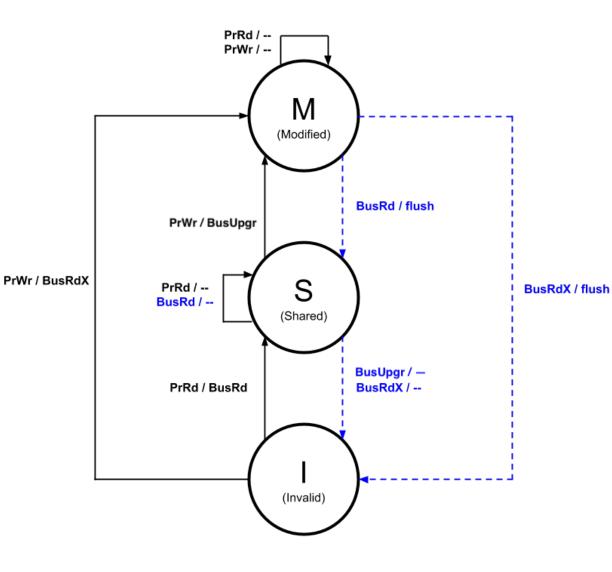
	CPU event	I *	Bus transaction(s)	mem1	mem2	mem3
<b>r1</b>	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	1
r2	PrRd	Miss				
w3						
r2						
w1						
w2						
r3						
r2						
<b>r1</b>						



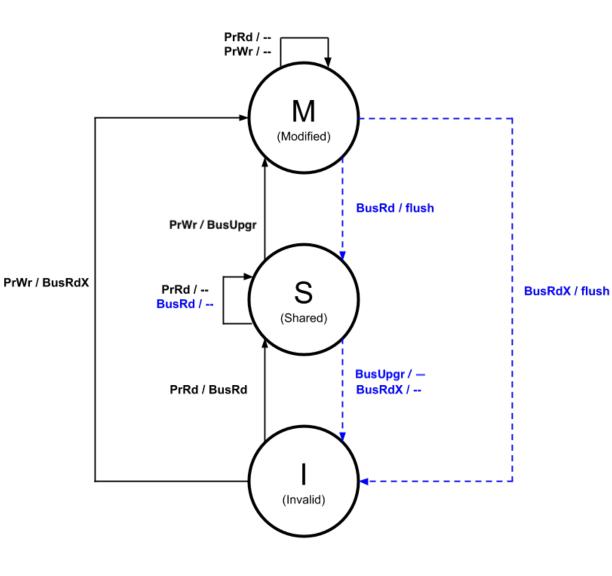
	1	<b>"</b>	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	1	l
w1	PrWr	Hit	BusUpgr	M	I	l
r2	PrRd	Miss	BusRd/flush	S	S	I
w3						
r2						
w1						
w2						
r3						
r2						
r1						



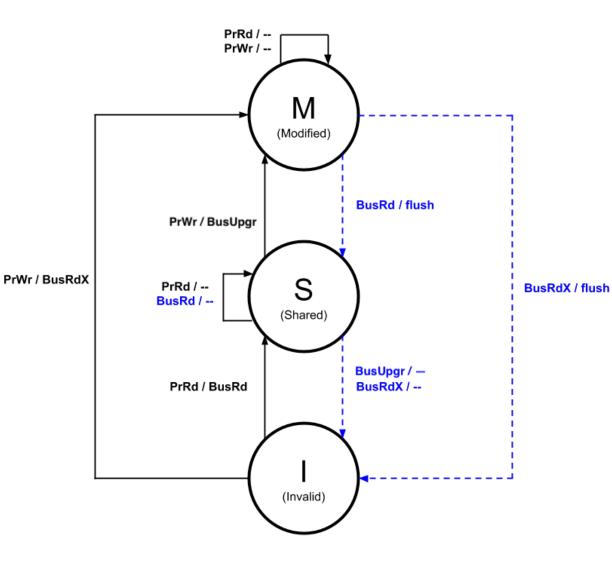
	CPU event	•	Bus transaction(s)	mem1	mem2	mem3
<b>r1</b>	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	М	ı	ı
r2	PrRd	Miss	BusRd/flush	S	S	ı
w3						
r2						
w1						
w2						
r3						
r2						
<b>r1</b>						



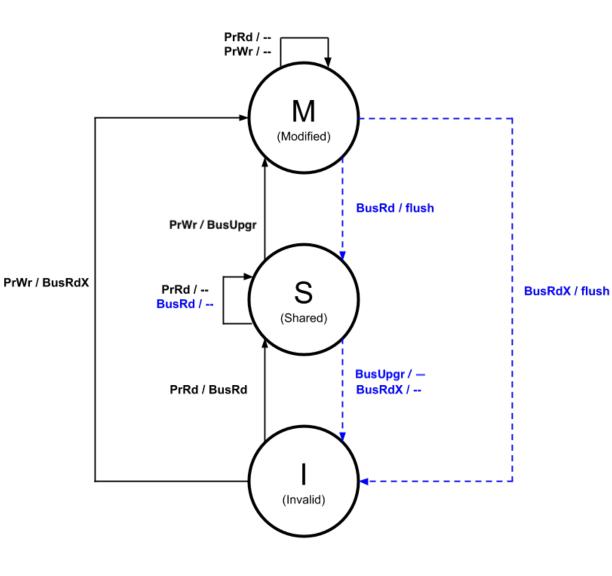
	CPU event	•	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	<b>I</b>	I
w1	PrWr	Hit	BusUpgr	M		I
r2	PrRd	Miss	BusRd/flush	S	S	ı
w3	PrWr	Miss	BusRdX			
r2						
w1						
w2						
r3						
r2						
r1						



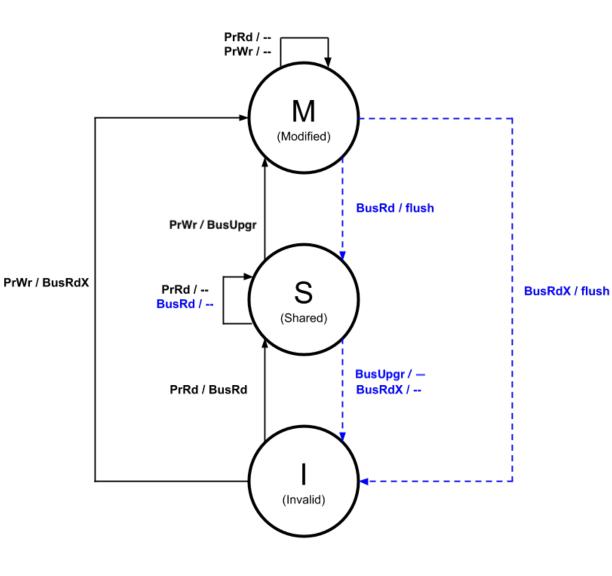
	CPU event	1 7	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd			S		I
w1	PrWr	Hit	BusUpgr	М	I	ı
r2	PrRd	Miss	BusRd/flush	S	S	l
w3	PrWr	Miss	BusRdX	I	I	M
r2						
w1						
w2						
r3						
r2						
r1						



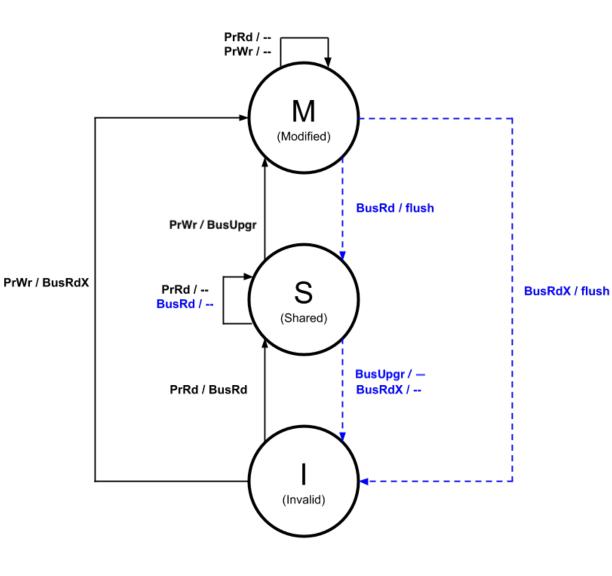
	CPU event	•	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S		I
w1	PrWr	Hit	BusUpgr	М		ı
r2	PrRd	Miss	BusRd/flush	S	S	ı
w3	PrWr	Miss	BusRdX	ı	l	M
r2						
w1						
w2						
r3						
r2						
r1						



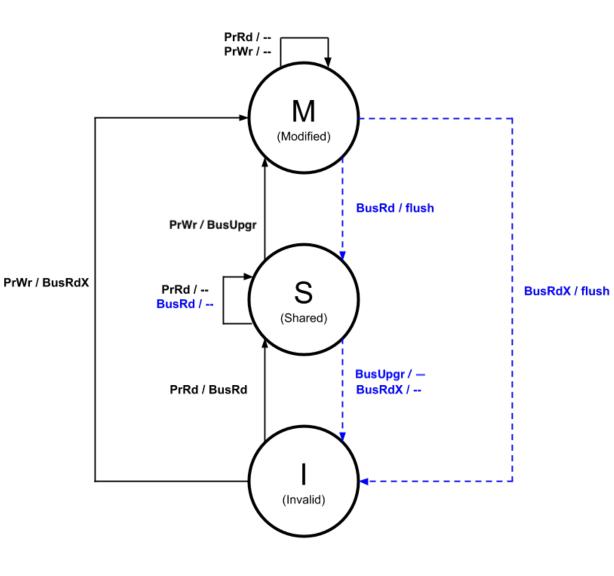
	CPU	<b>'</b>	Bus			
	event	Miss	transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	ı
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	l	I	M
r2	PrRd	Miss	BusRd/flush			
w1						
w2						
r3						
r2						
r1						



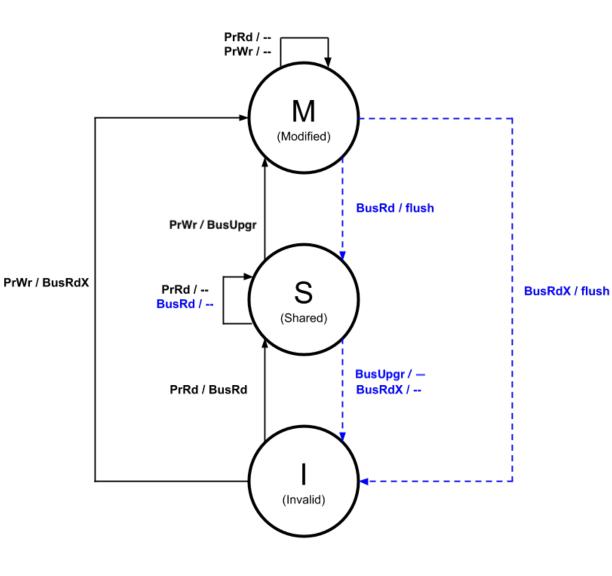
	CPU	<b>'</b>	Bus			
	event	Miss	transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	М	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	ı	I	M
r2	PrRd	Miss	BusRd/flush	ı	S	S
w1						
w2						
r3						
r2						
r1						



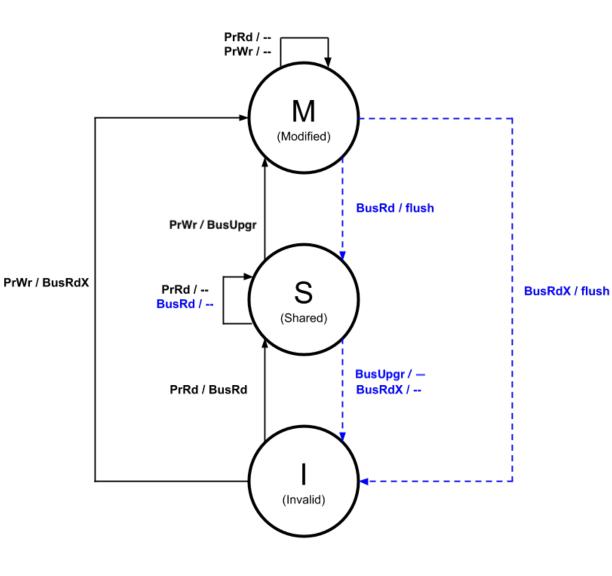
	CPU event	<b>'</b>	Bus transaction(s)	mem1	mem2	mem3
<b>r1</b>	PrRd	Miss	BusRd	S	<b>I</b>	I
w1	PrWr	Hit	BusUpgr	M		ı
r2	PrRd	Miss	BusRd/flush	S	S	ı
w3	PrWr	Miss	BusRdX	ı	I	M
r2	PrRd	Miss	BusRd/flush	ı	S	S
w1						
w2						
r3						
r2						
<b>r1</b>						



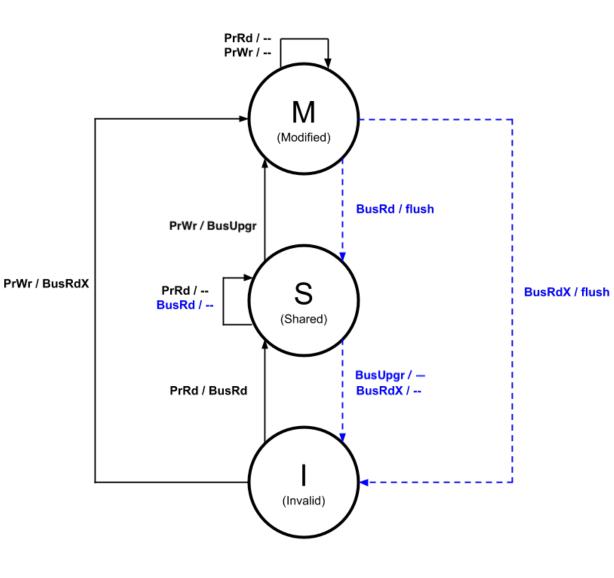
		•	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	М	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX		Ī	M
r2	PrRd	Miss	BusRd/flush	l	S	S
w1	PrWr	Miss	BusRdX			
w2						
r3						
r2						
r1						



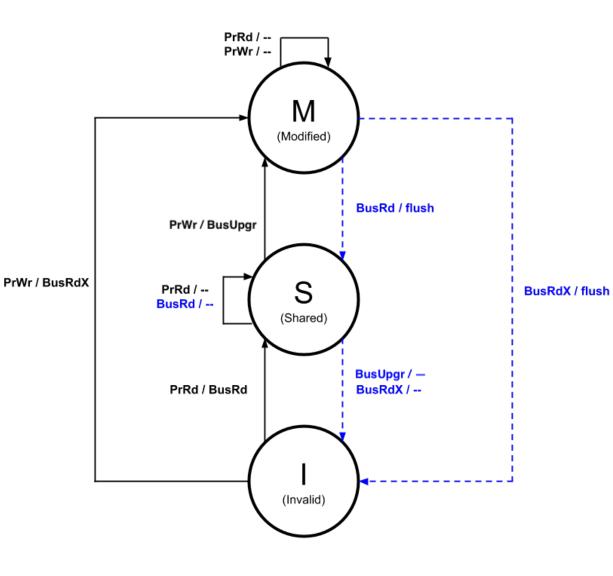
	CPU	Hit/	Bus			
	event	Miss	transaction(s)	mem1	mem2	mem3
<b>r1</b>	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	М	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	[	I
w2						
r3						
r2						
<b>r1</b>						



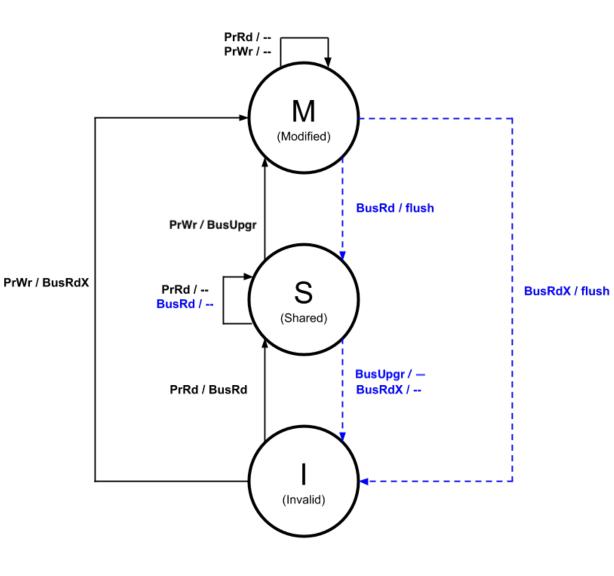
	CPU event	<b>'</b>	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	1	ı
r2	PrRd	Miss	BusRd/flush	S	S	ı
w3	PrWr	Miss	BusRdX	ı	I	M
r2	PrRd	Miss	BusRd/flush	ı	S	S
w1	PrWr	Miss	BusRdX	М	I	ı
w2						
r3						
r2						
<b>r1</b>						



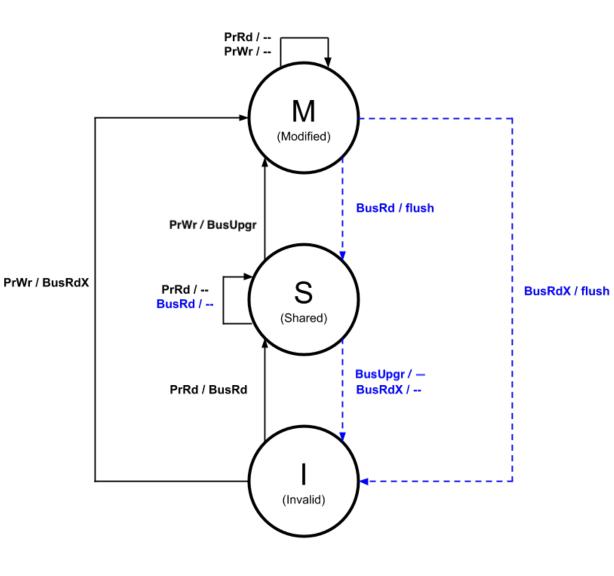
	CPU event	•	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	1
w3	PrWr	Miss	BusRdX	ı	ı	М
r2	PrRd	Miss	BusRd/flush	1	S	S
w1	PrWr	Miss	BusRdX	М	1	I
w2	PrWr	Miss	BusRdX/flush			
r3						
r2						
<b>r1</b>						



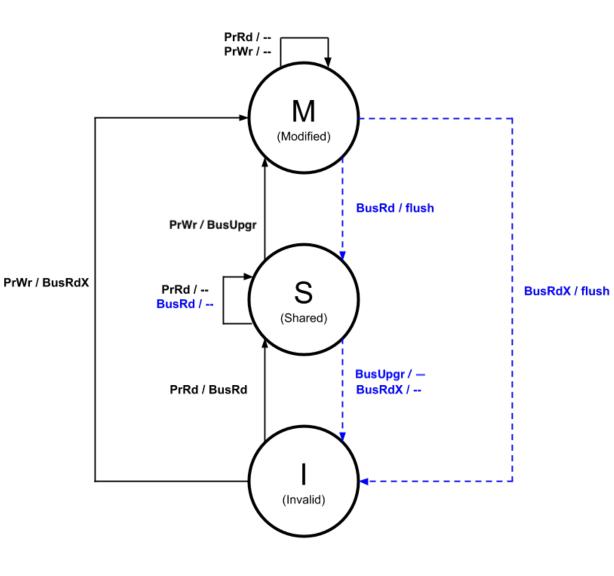
	CPU event	<b>'</b>	Bus transaction(s)	mem1	mem2	mem3
<b>r1</b>	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	l
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	ı	ı	M
r2	PrRd	Miss	BusRd/flush	ı	S	S
w1	PrWr	Miss	BusRdX	М	I	ı
w2	PrWr	Miss	BusRdX/flush	ı	M	ı
r3						
r2						
<b>r1</b>						



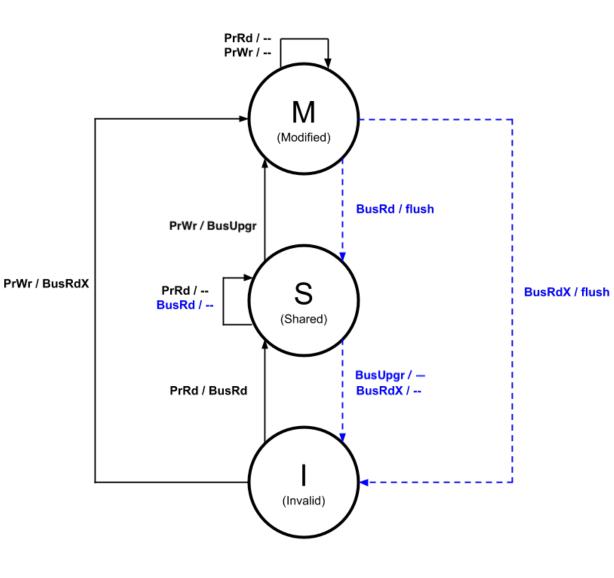
	CPU event	_	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	l
w1	PrWr	Hit	BusUpgr	M		I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX		1	M
r2	PrRd	Miss	BusRd/flush	l	S	S
w1	PrWr	Miss	BusRdX	М	1	l
w2	PrWr	Miss	BusRdX/flush		M	I
r3						
r2						
r1						



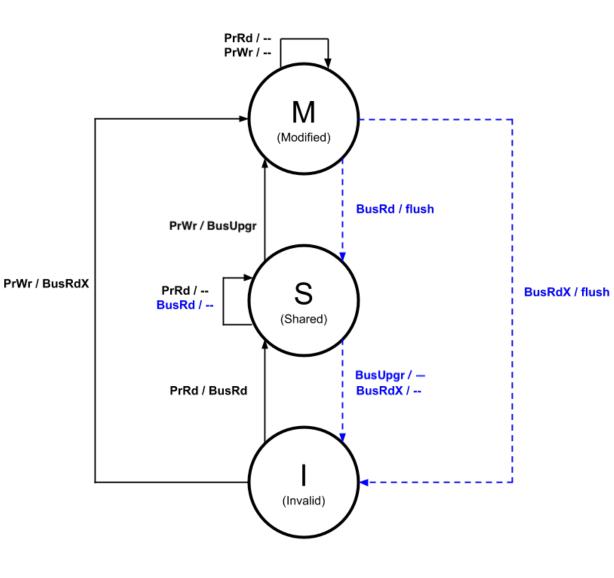
	CPU event	_	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	1	I
w1	PrWr	Hit	BusUpgr	M	1	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX		1	M
r2	PrRd	Miss	BusRd/flush	1	S	S
w1	PrWr	Miss	BusRdX	M	1	l
w2	PrWr	Miss	BusRdX/flush	1	M	I
r3	PrRd	Miss				
r2						
r1						



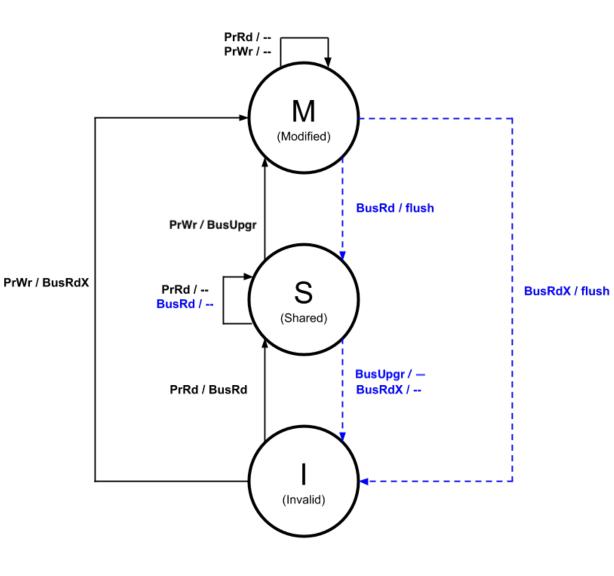
	CPU event		Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	l
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	l
w3	PrWr	Miss	BusRdX		1	M
r2	PrRd	Miss	BusRd/flush	1	S	S
w1	PrWr	Miss	BusRdX	М	1	I
w2	PrWr	Miss	BusRdX/flush	l	M	ı
r3	PrRd	Miss	BusRd/flush	ı	S	S
r2						
r1						



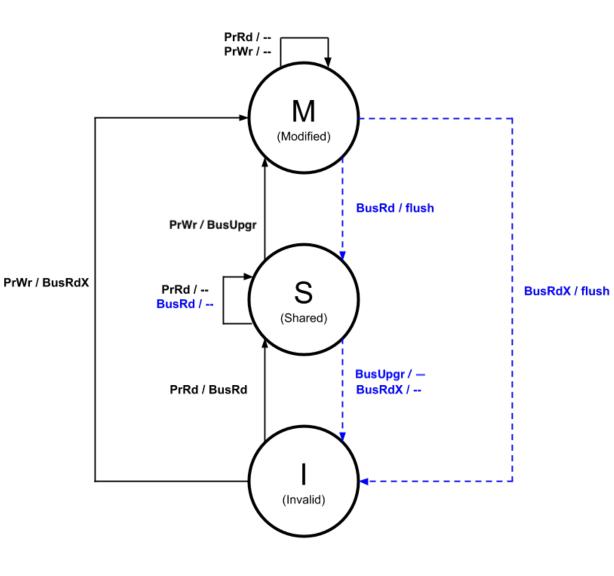
	CPU event		Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	1	l
w1	PrWr	Hit	BusUpgr	M	1	I
r2	PrRd	Miss	BusRd/flush	S	S	l
w3	PrWr	Miss	BusRdX		I	M
r2	PrRd	Miss	BusRd/flush	ı	S	S
w1	PrWr	Miss	BusRdX	М	ı	ı
w2	PrWr	Miss	BusRdX/flush	ı	M	ı
r3	PrRd	Miss	BusRd/flush	ı	S	S
r2						
r1						



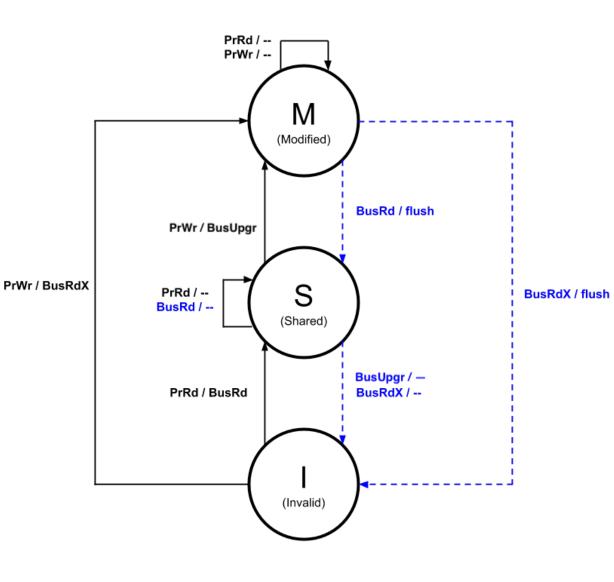
	CPU event		Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S		I
w1	PrWr	Hit	BusUpgr	M	<b>I</b>	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	l		M
r2	PrRd	Miss	BusRd/flush	ı	S	S
w1	PrWr	Miss	BusRdX	M		ı
w2	PrWr	Miss	BusRdX/flush	ı	M	ı
r3	PrRd	Miss	BusRd/flush	ı	S	S
r2	PrRd	Hit	-			
r1						



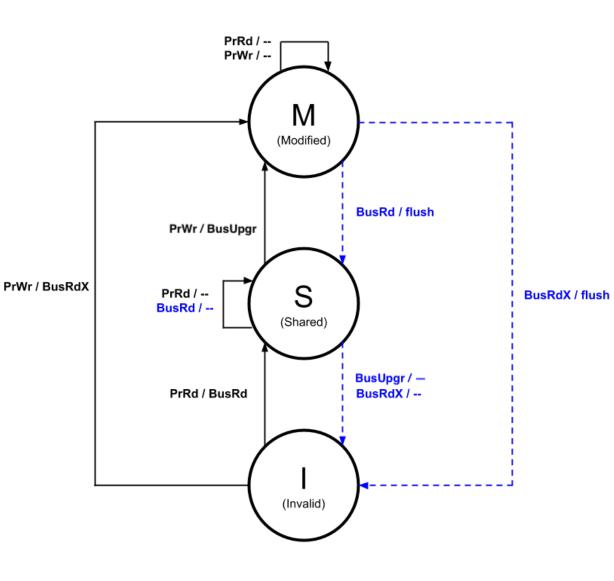
	CPU event		Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	l
w1	PrWr	Hit	BusUpgr	M	1	I
r2	PrRd	Miss	BusRd/flush	S	S	1
w3	PrWr	Miss	BusRdX	ı	I	М
r2	PrRd	Miss	BusRd/flush	ı	S	S
w1	PrWr	Miss	BusRdX	М	I	ı
w2	PrWr	Miss	BusRdX/flush	ı	M	ı
r3	PrRd	Miss	BusRd/flush	ı	S	S
r2	PrRd	Hit	-	ı	S	S
r1						



	CPU event		Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	l
w1	PrWr	Hit	BusUpgr	M	1	l
r2	PrRd	Miss	BusRd/flush	S	S	1
w3	PrWr	Miss	BusRdX	ı	I	М
r2	PrRd	Miss	BusRd/flush	ı	S	S
w1	PrWr	Miss	BusRdX	М	I	ı
w2	PrWr	Miss	BusRdX/flush	ı	M	ı
r3	PrRd	Miss	BusRd/flush	ı	S	S
r2	PrRd	Hit	-	ı	S	S
r1						



	CPU event	_	Bus transaction(s)	mem1	mem2	mem3
<b>r1</b>	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	ı	1
r2	PrRd	Miss	BusRd/flush	S	S	ı
w3	PrWr	Miss	BusRdX	ı	I	M
r2	PrRd	Miss	BusRd/flush	ı	S	S
w1	PrWr	Miss	BusRdX	М	ı	ı
w2	PrWr	Miss	BusRdX/flush	ı	M	ı
r3			BusRd/flush		S	S
r2	PrRd	Hit	_		S	S
<b>r1</b>	PrRd	Miss	BusRd			



	CPU event	· •	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	М	I	I
r2	PrRd	Miss	BusRd/flush	S	S	
w3	PrWr	Miss	BusRdX	1	1	M
r2	PrRd	Miss	BusRd/flush	ı	S	S
w1	PrWr	Miss	BusRdX	М	ı	ı
w2	PrWr	Miss	BusRdX/flush	ı	M	ı
r3	PrRd	Miss	BusRd/flush	ı	S	S
r2	PrRd	Hit	-	ı	S	S
r1	PrRd	Miss	BusRd	S	S	S