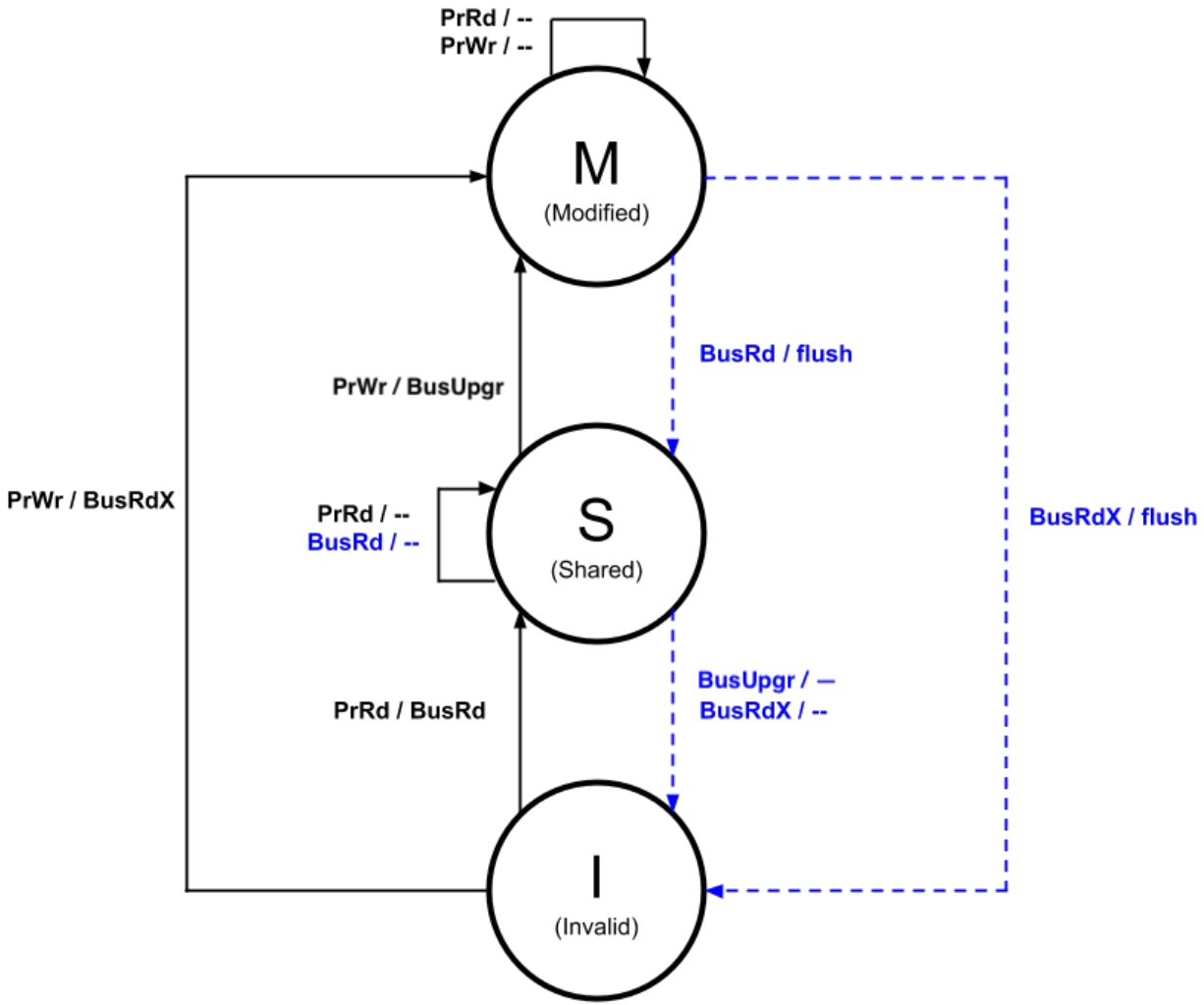
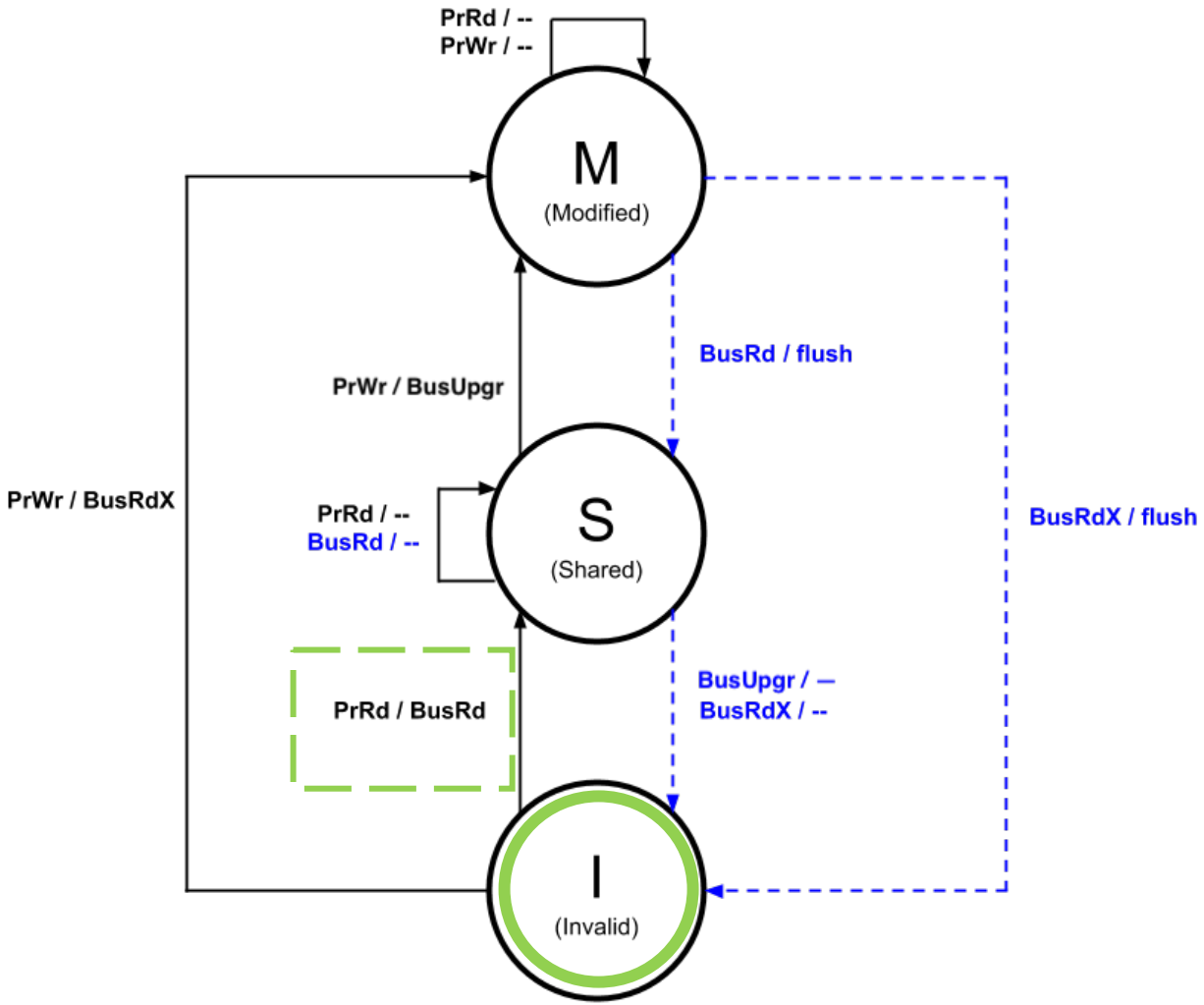
1. Given an SMP system with 3 CPUs, each with its own cache memory initially empty. To keep caches coherent the system uses a Snoopy–based write-invalidate *MSI* coherence protocol. Assuming the following sequence of memory instructions all accessing the same memory direction: `r1, w1, r2, w3, r2, w1, w2, r3, r2, r1` (where `rx` indicates read by processor `x` and `wy` write by processor `y`), fill in the table indicating including the CPU event (PrRd, PrWr), Bus transactions (BusRd, BusRdX, BusUpgr, Flush) and state of the cache line (M, S, I) in each cache memory after each access to memory. In the observations column indicate who is providing the line when a cache requires it and when main memory is updated.

Memory Access	CPU event	hit/miss	Bus transaction(s)	Cache Line State			Observations
				Cache1	Cache2	Cache3	
r1							
w1							
r2							
w3							
r2							
w1							
w2							
r3							
r2							
r1							

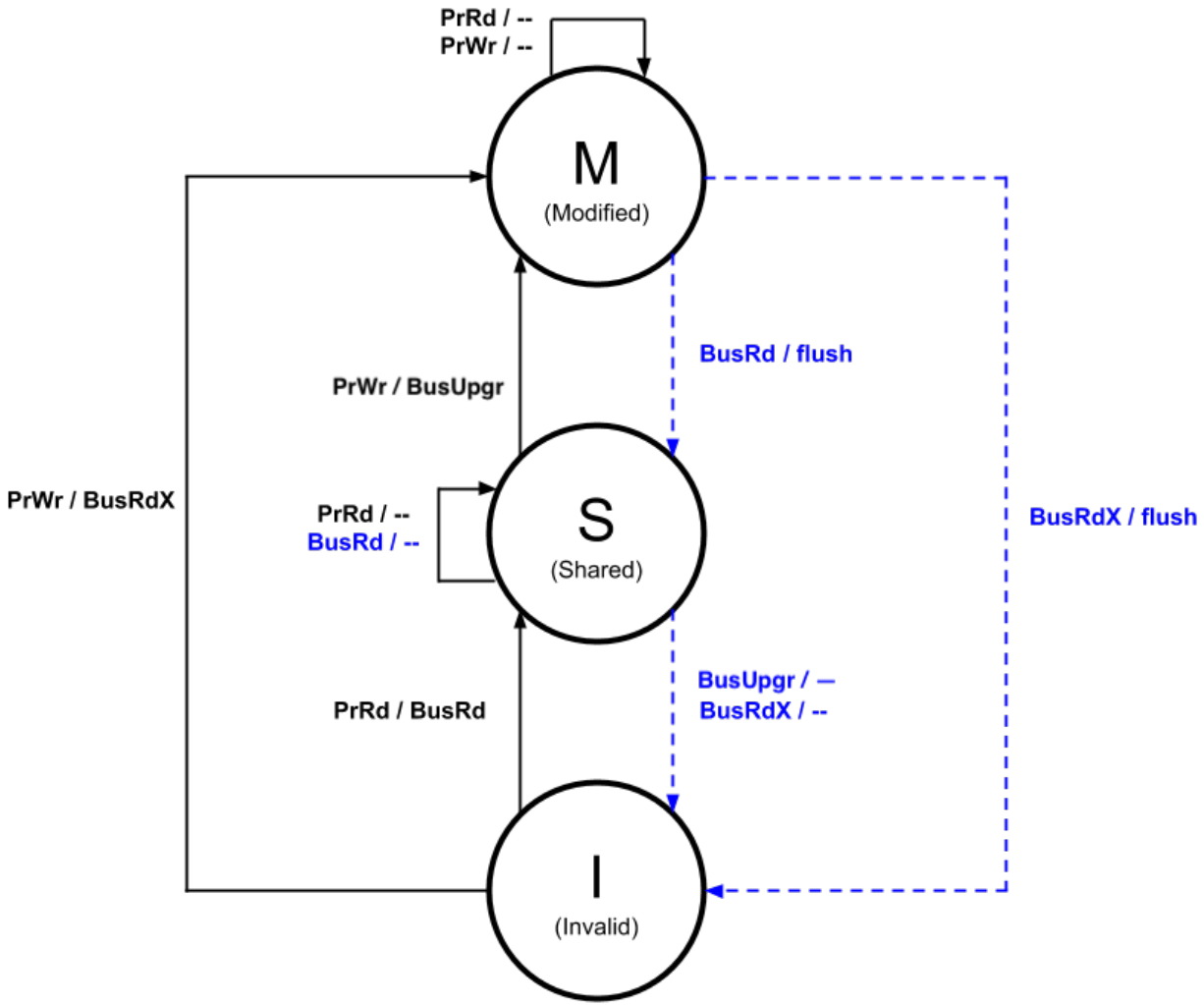
What would change in the table if a *MESI* protocol is used instead of the original *MSI*?



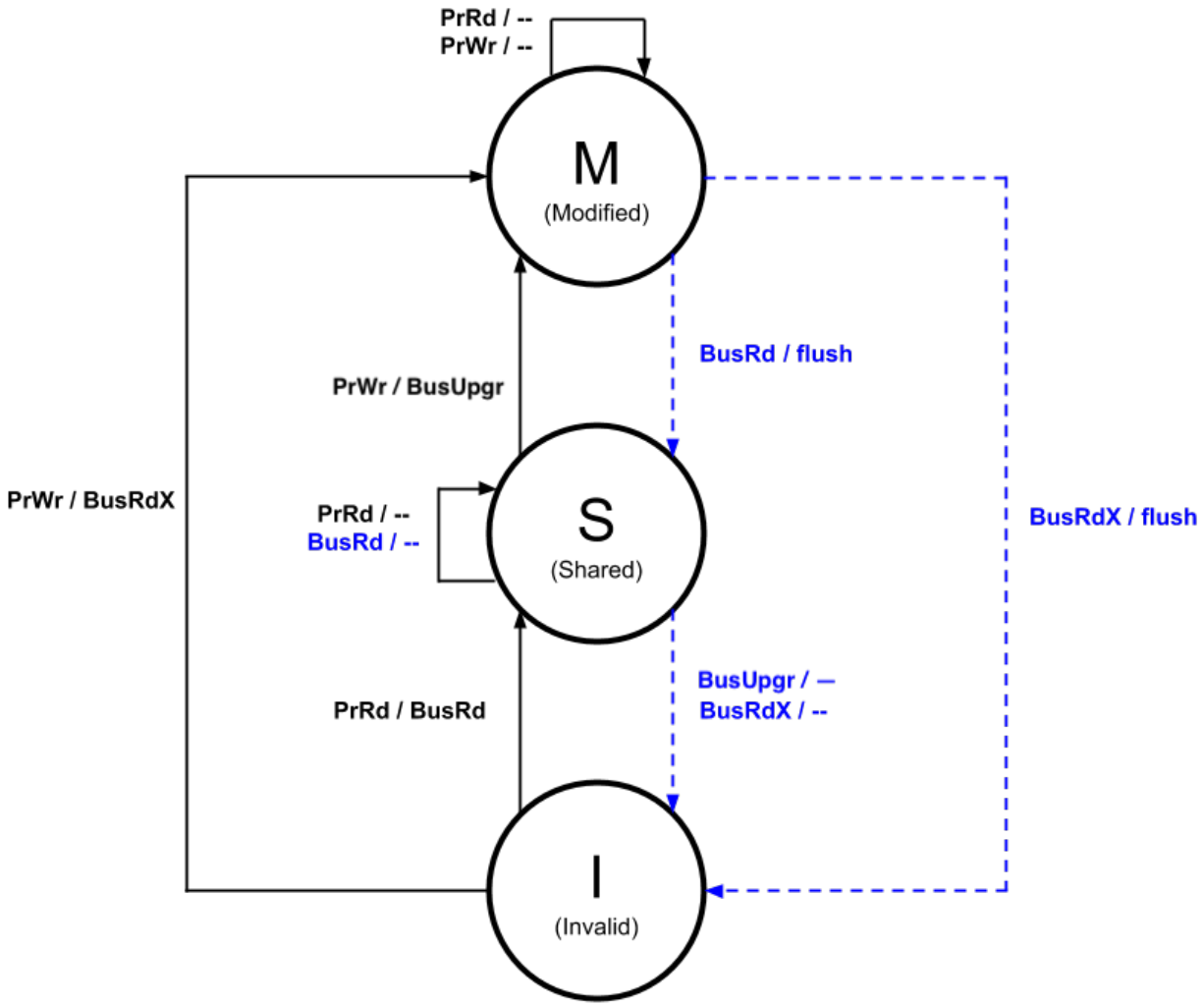
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1						
w1						
r2						
w3						
r2						
w1						
w2						
r3						
r2						
r1						



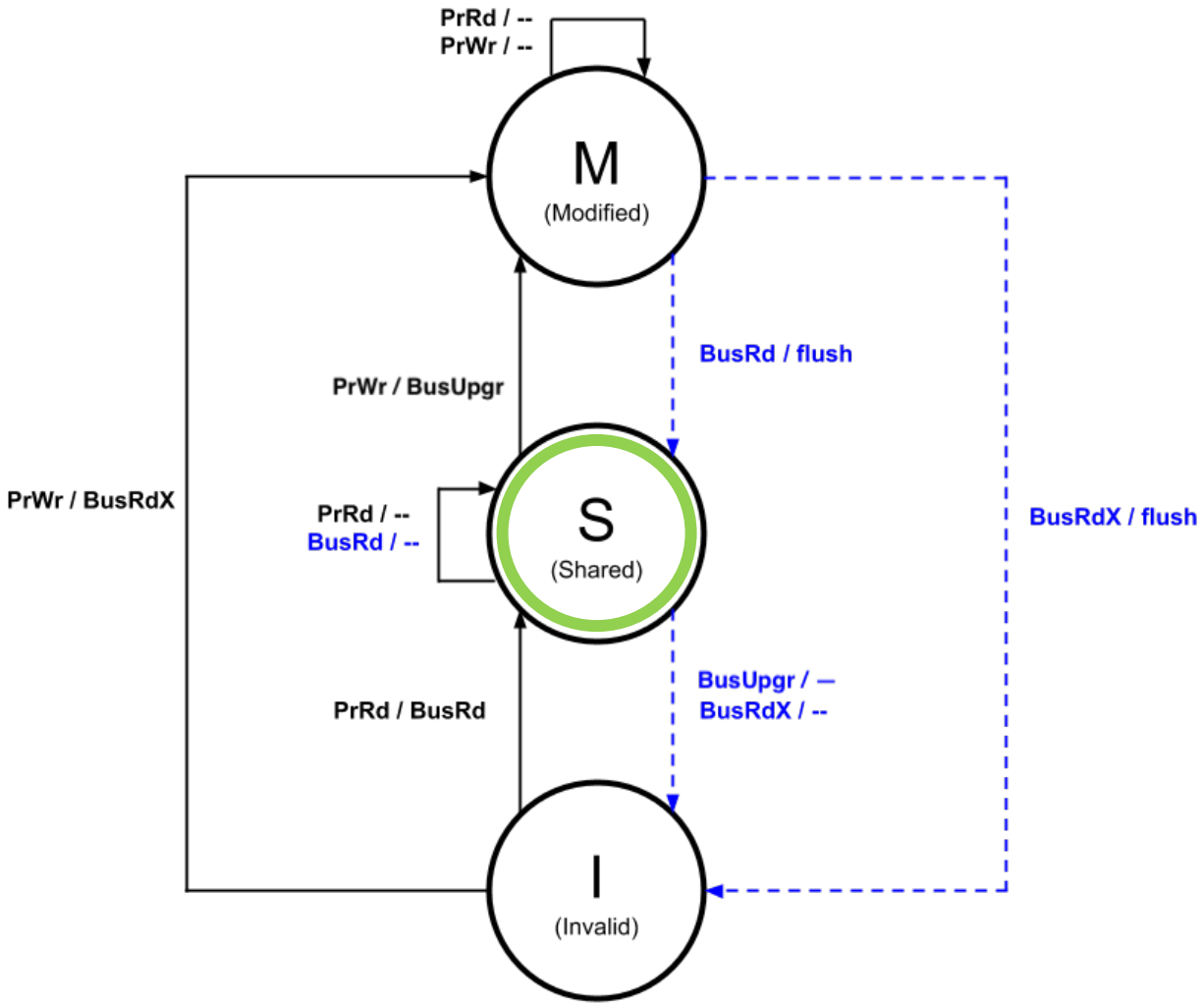
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd			
w1						
r2						
w3						
r2						
w1						
w2						
r3						
r2						
r1						



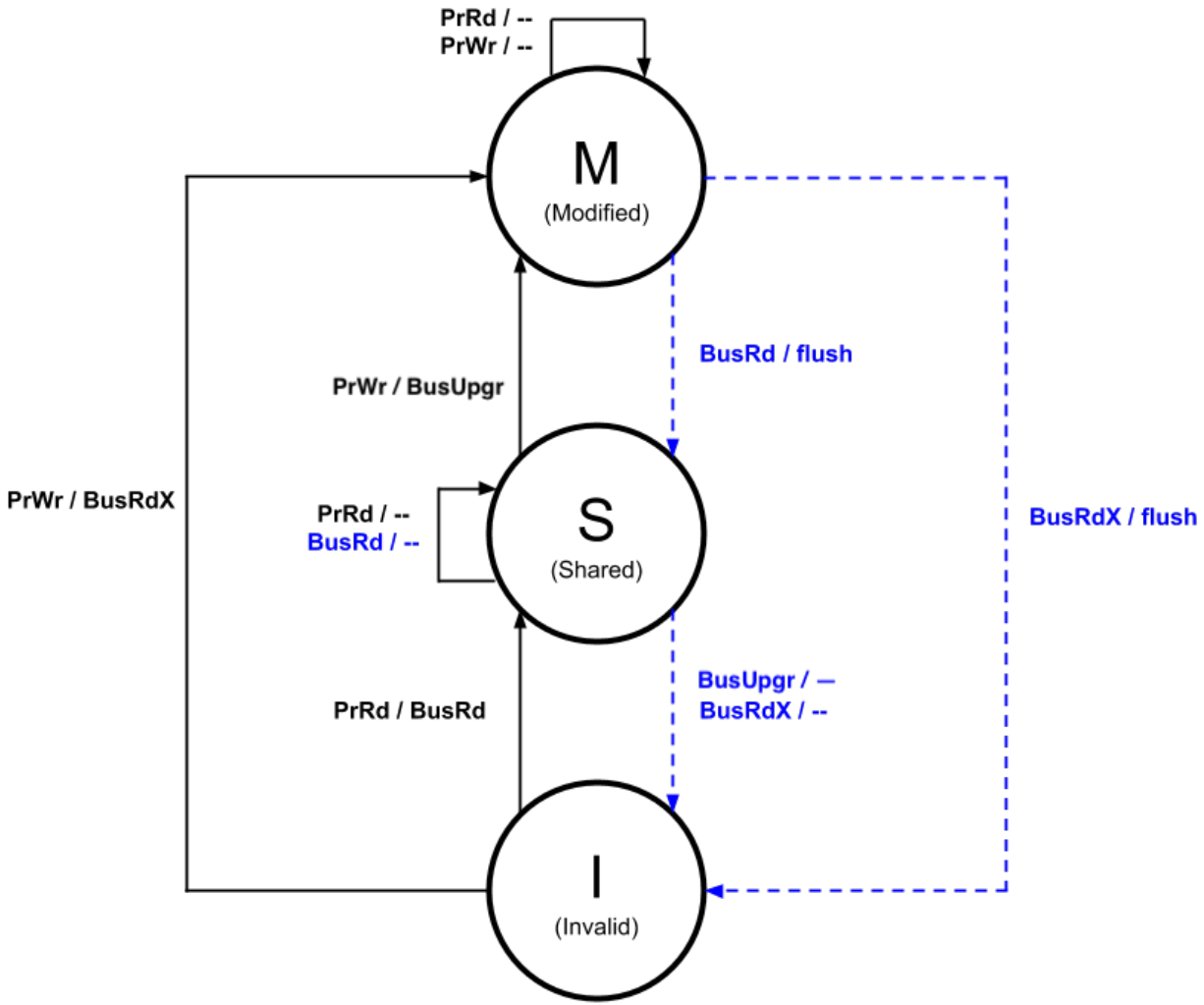
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1						
r2						
w3						
r2						
w1						
w2						
r3						
r2						
r1						



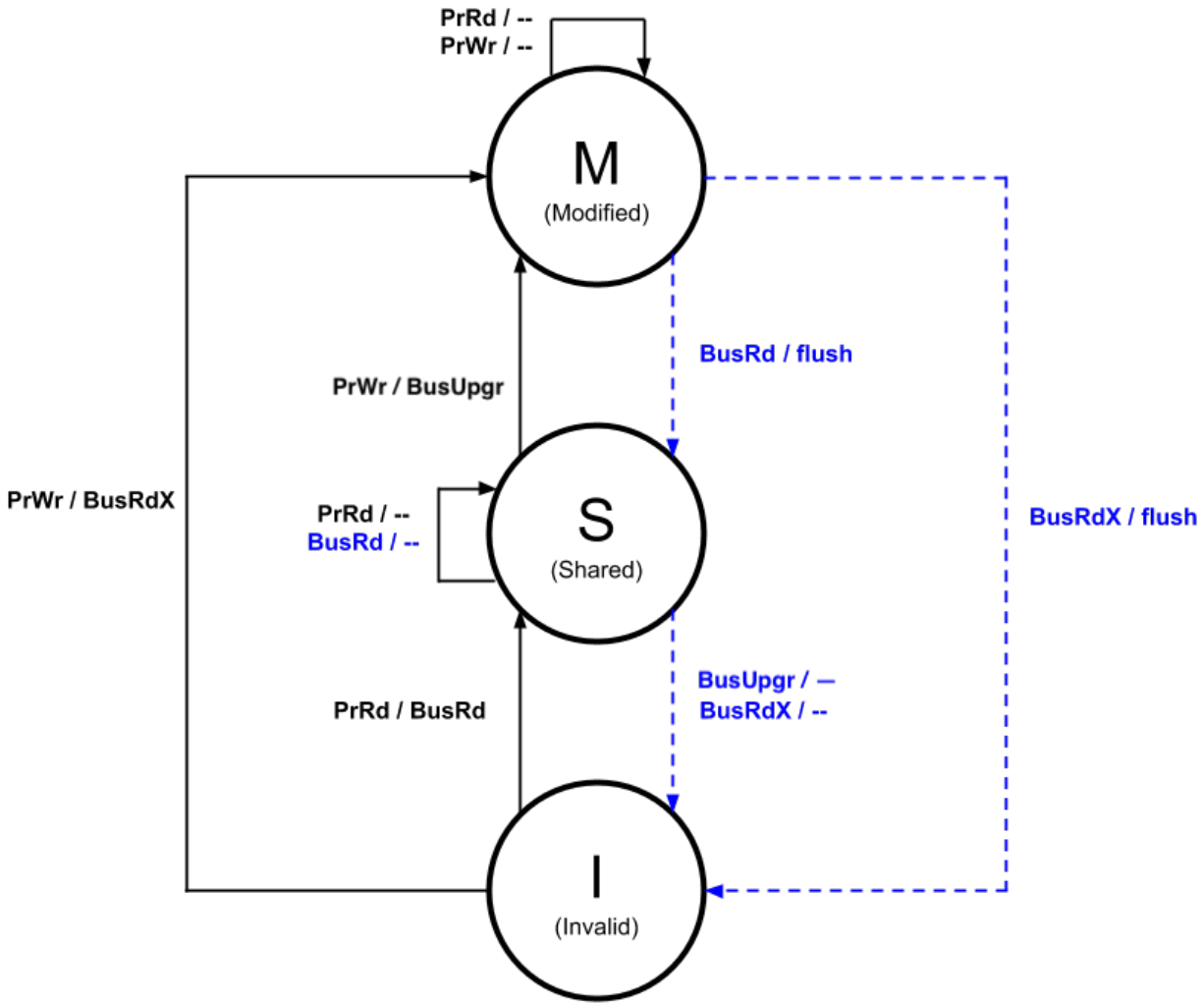
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1						
r2						
w3						
r2						
w1						
w2						
r3						
r2						
r1						



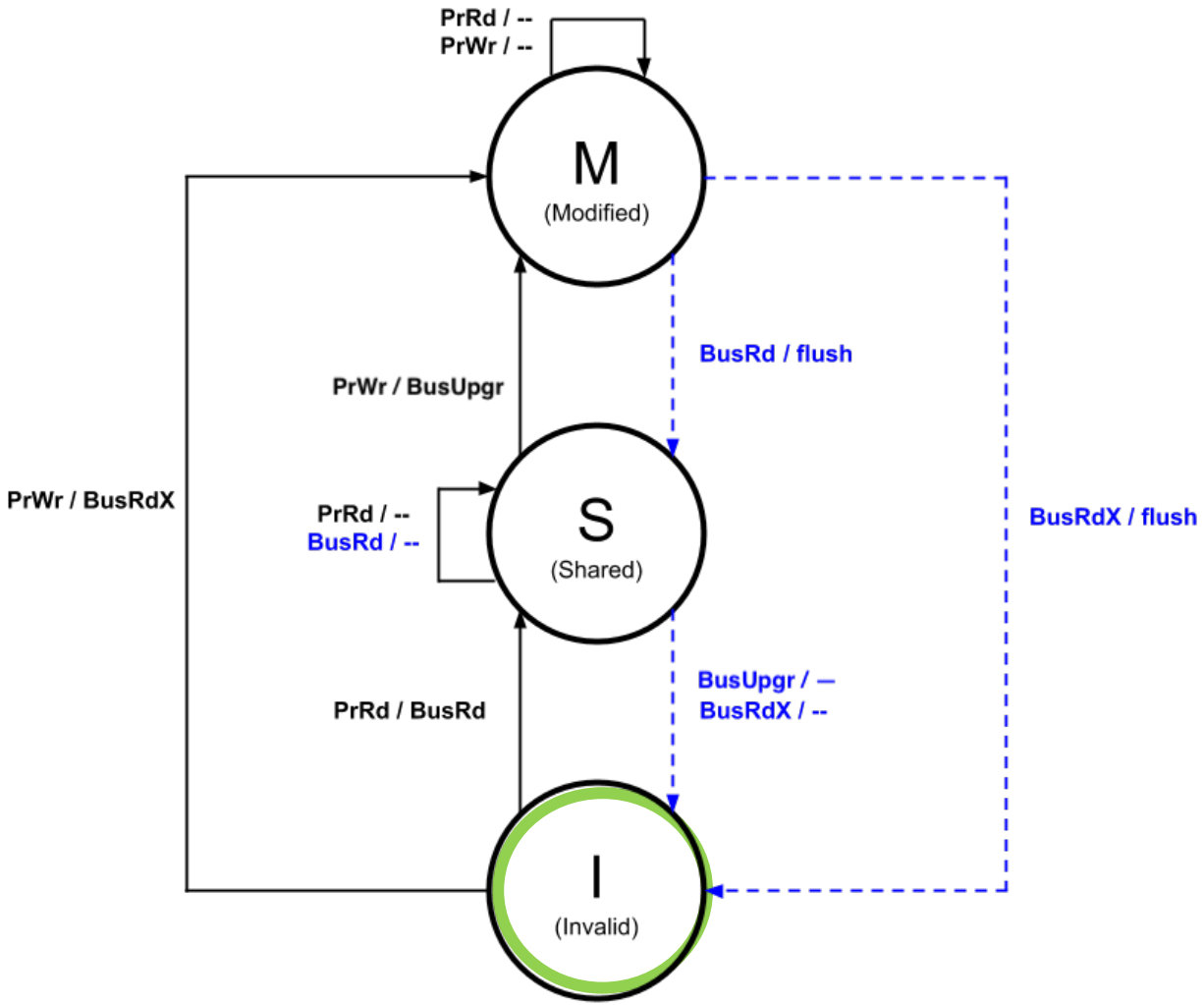
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr			
r2						
w3						
r2						
w1						
w2						
r3						
r2						
r1						



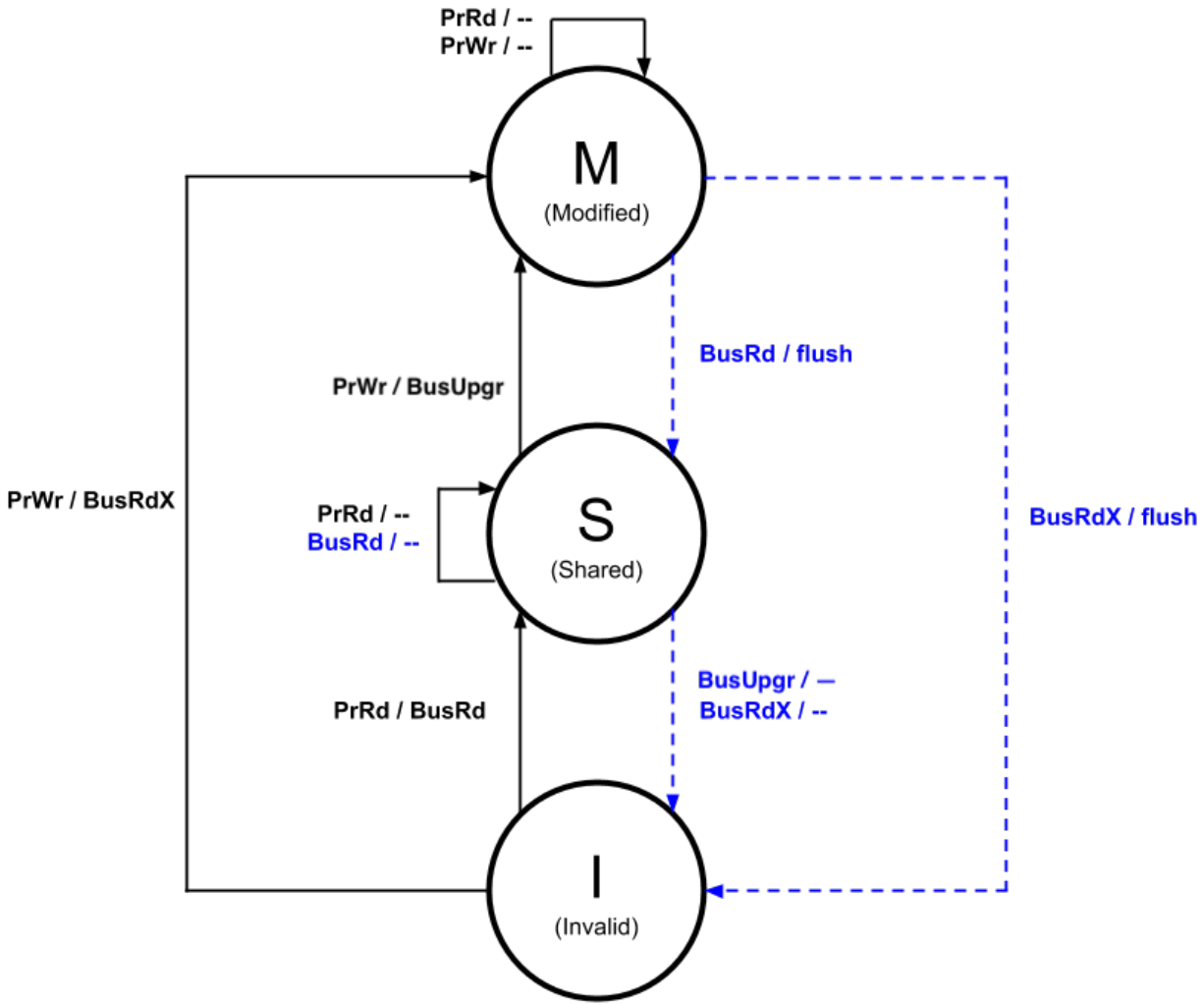
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2						
w3						
r2						
w1						
w2						
r3						
r2						
r1						



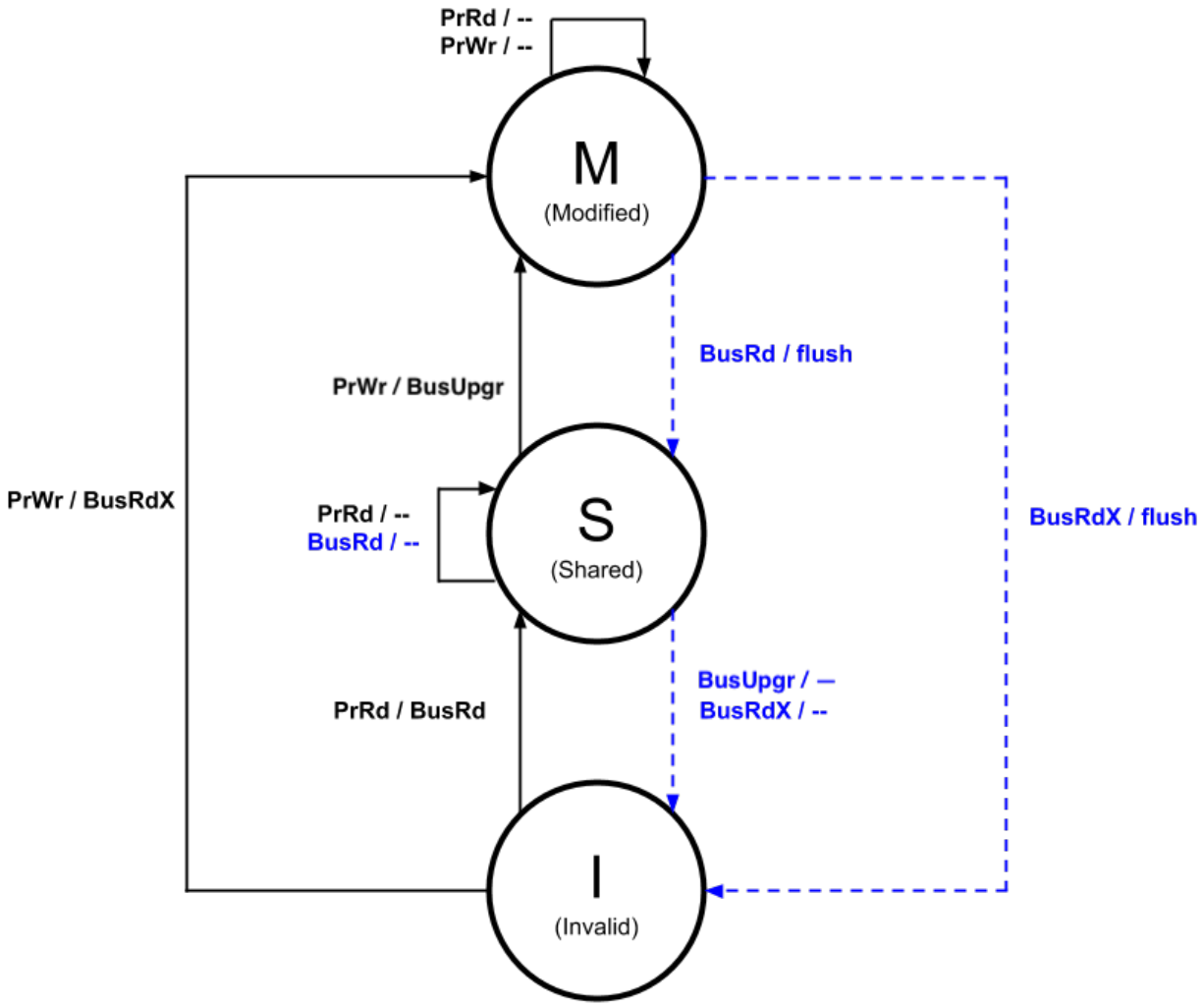
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2						
w3						
r2						
w1						
w2						
r3						
r2						
r1						



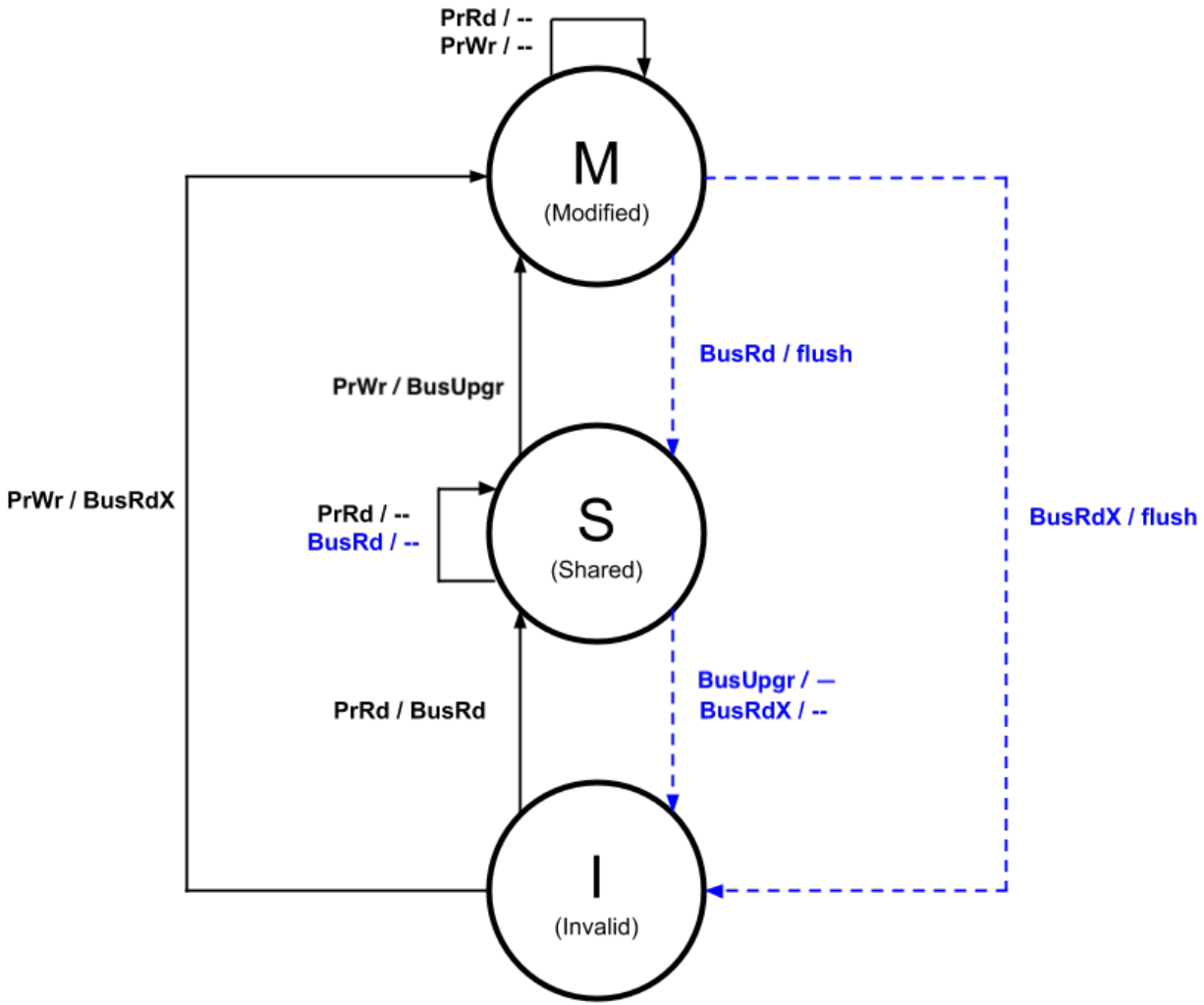
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss				
w3						
r2						
w1						
w2						
r3						
r2						
r1						



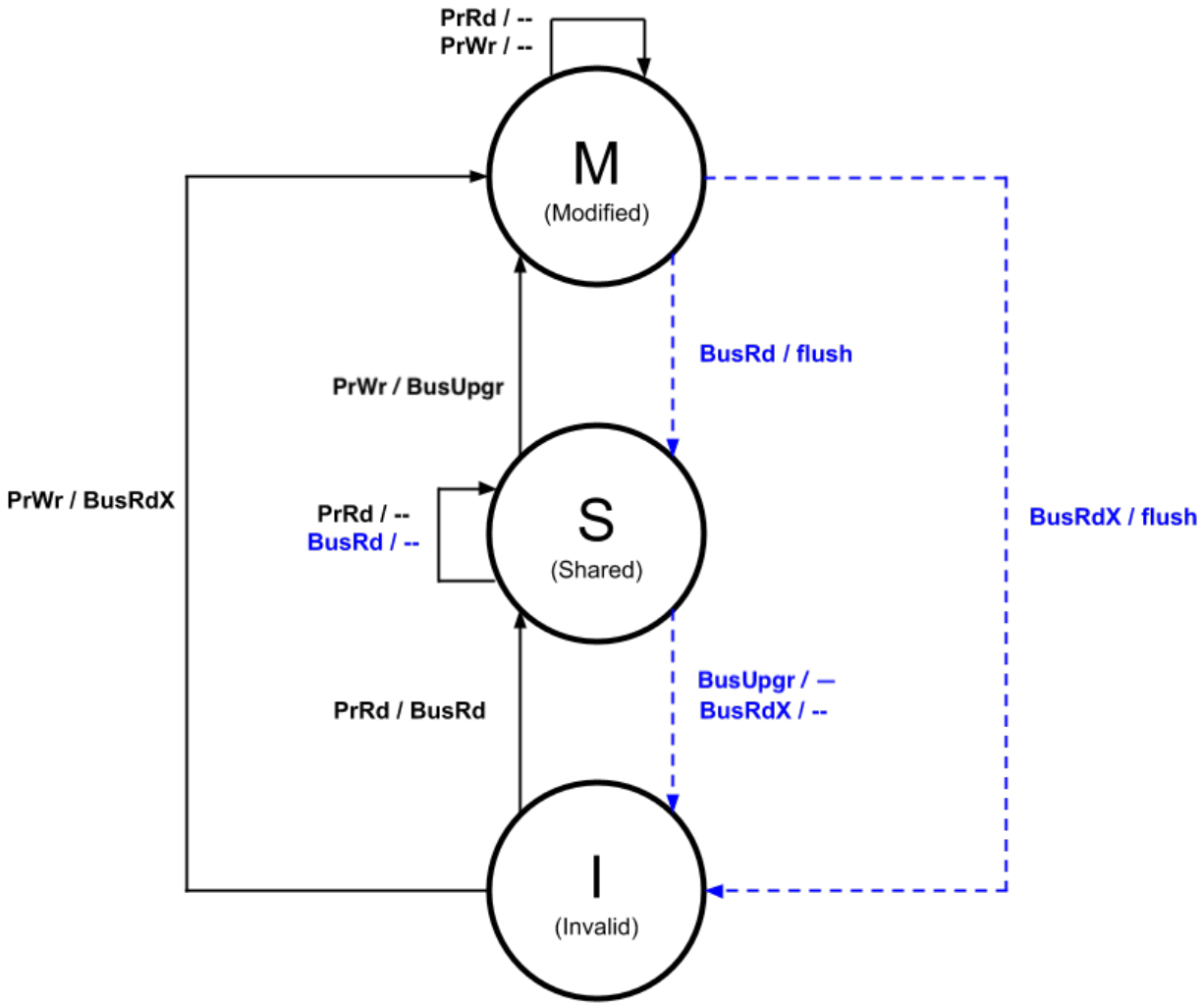
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3						
r2						
w1						
w2						
r3						
r2						
r1						



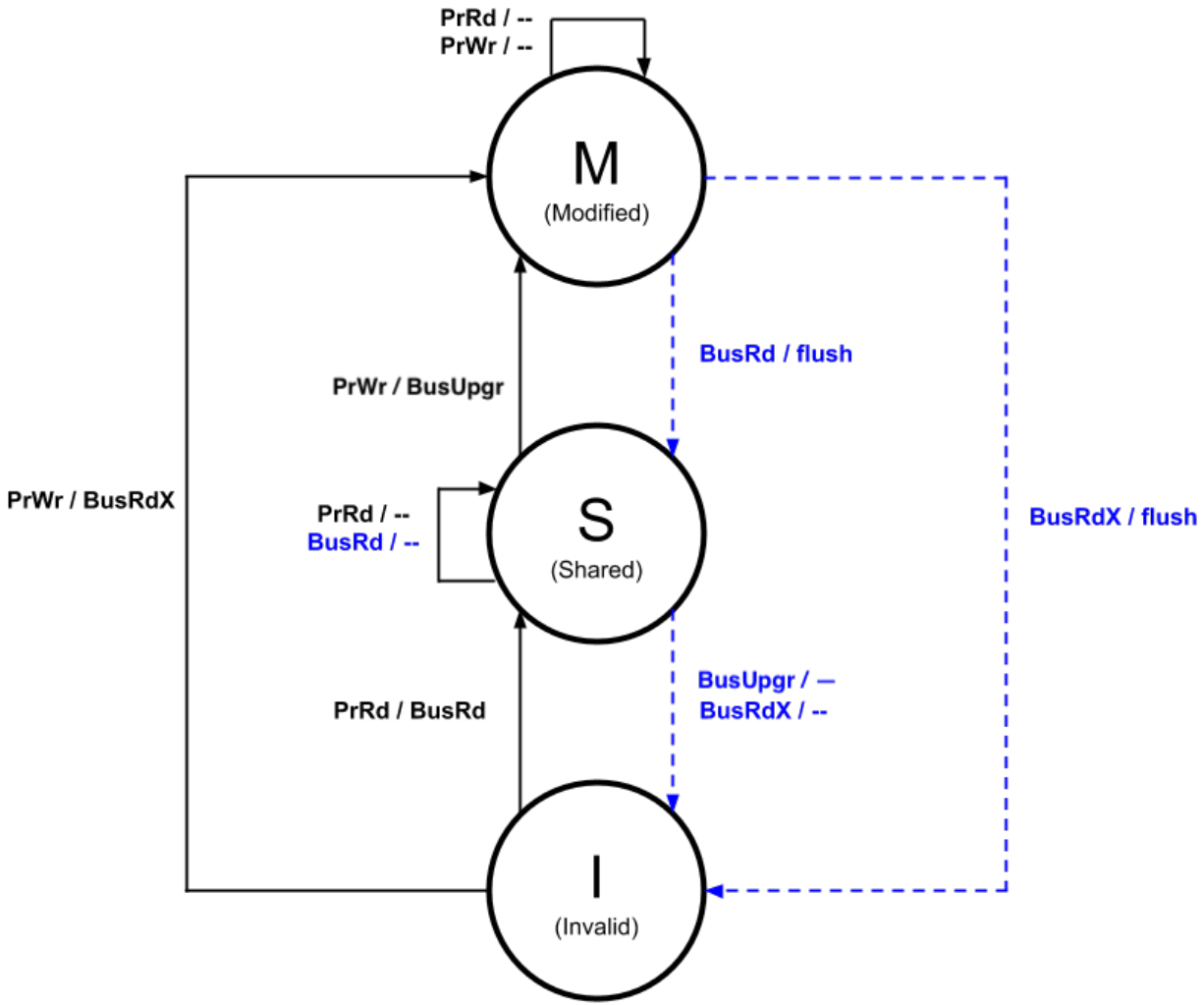
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3						
r2						
w1						
w2						
r3						
r2						
r1						



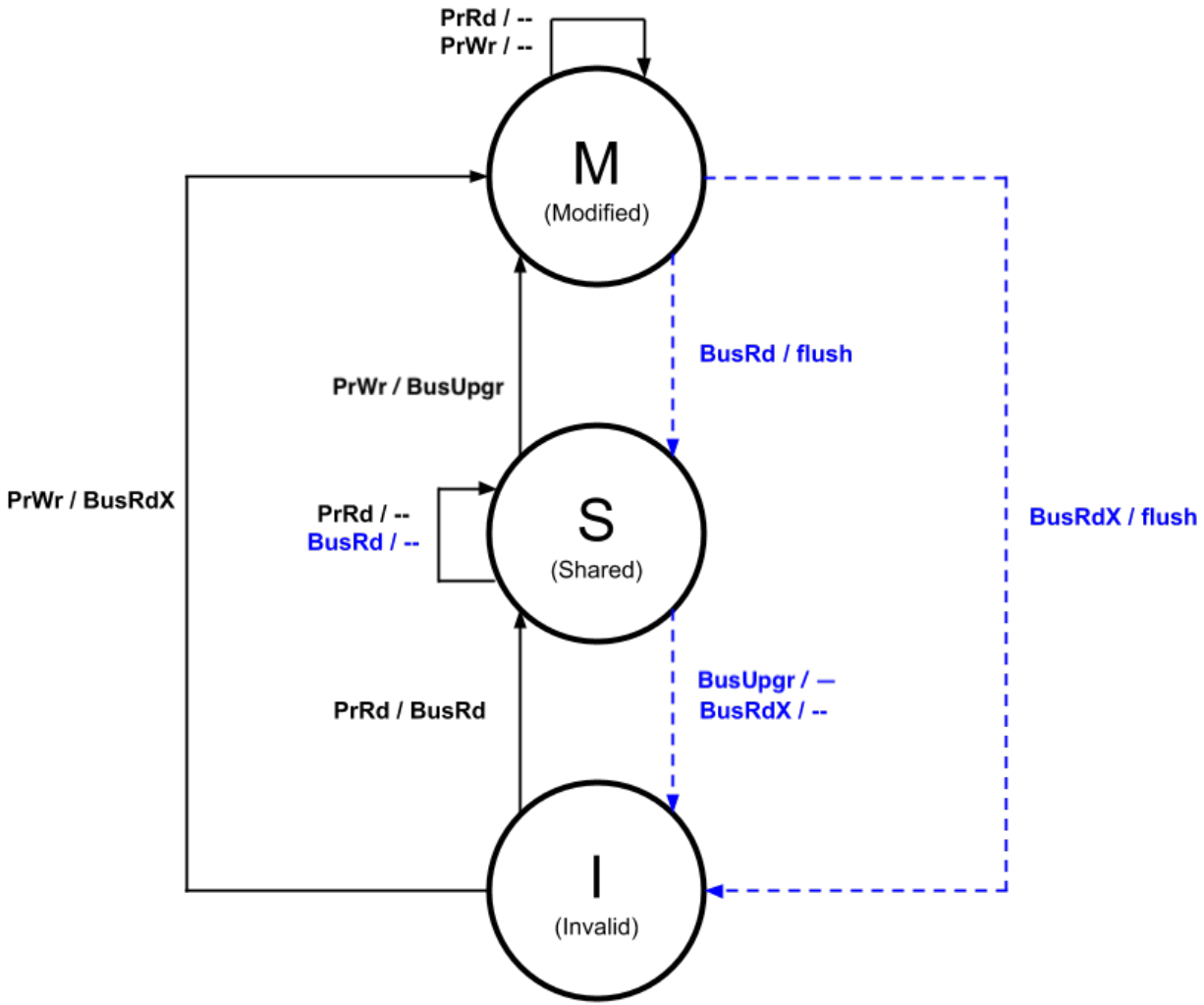
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX			
r2						
w1						
w2						
r3						
r2						
r1						



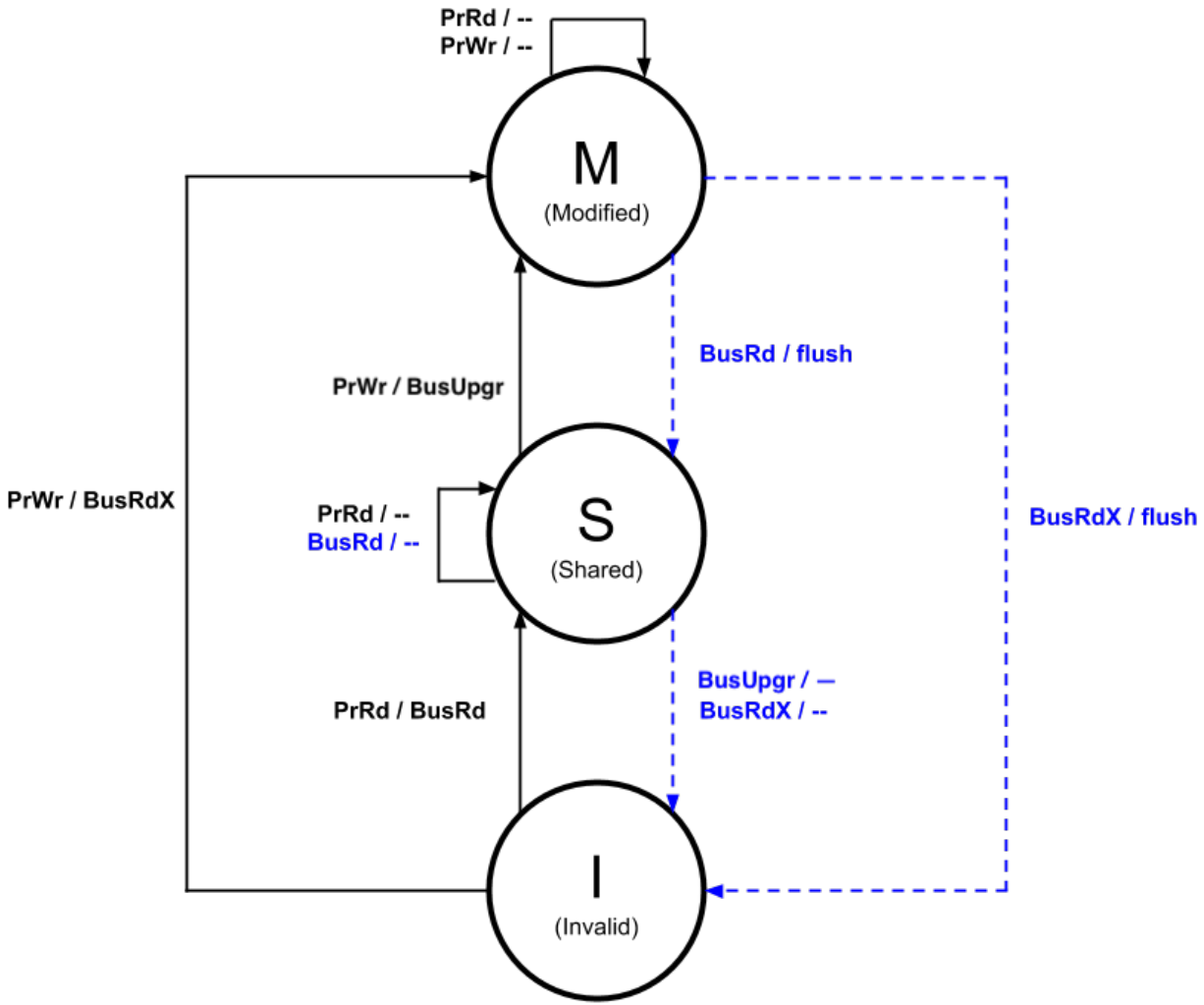
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2						
w1						
w2						
r3						
r2						
r1						



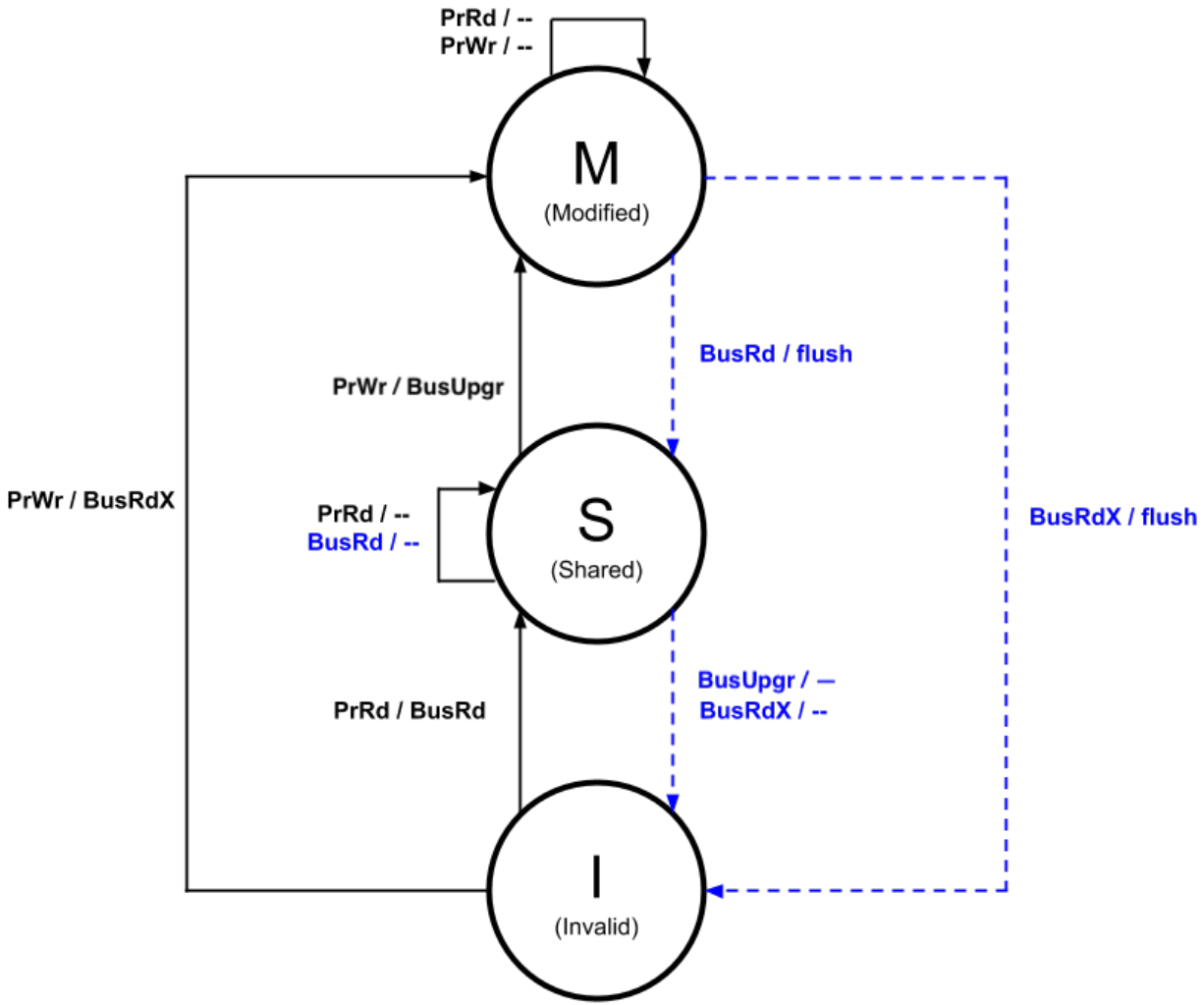
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2						
w1						
w2						
r3						
r2						
r1						



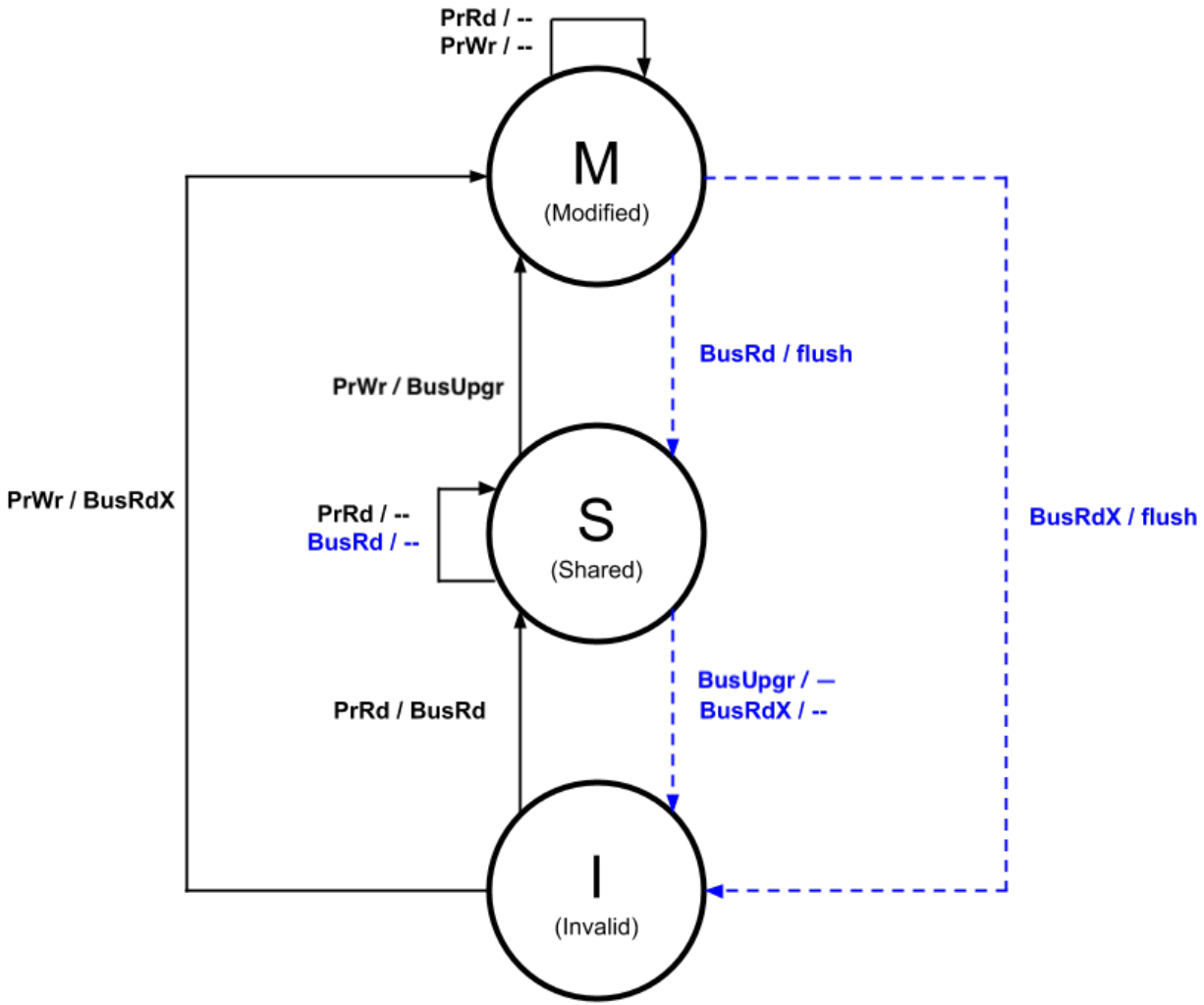
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush			
w1						
w2						
r3						
r2						
r1						



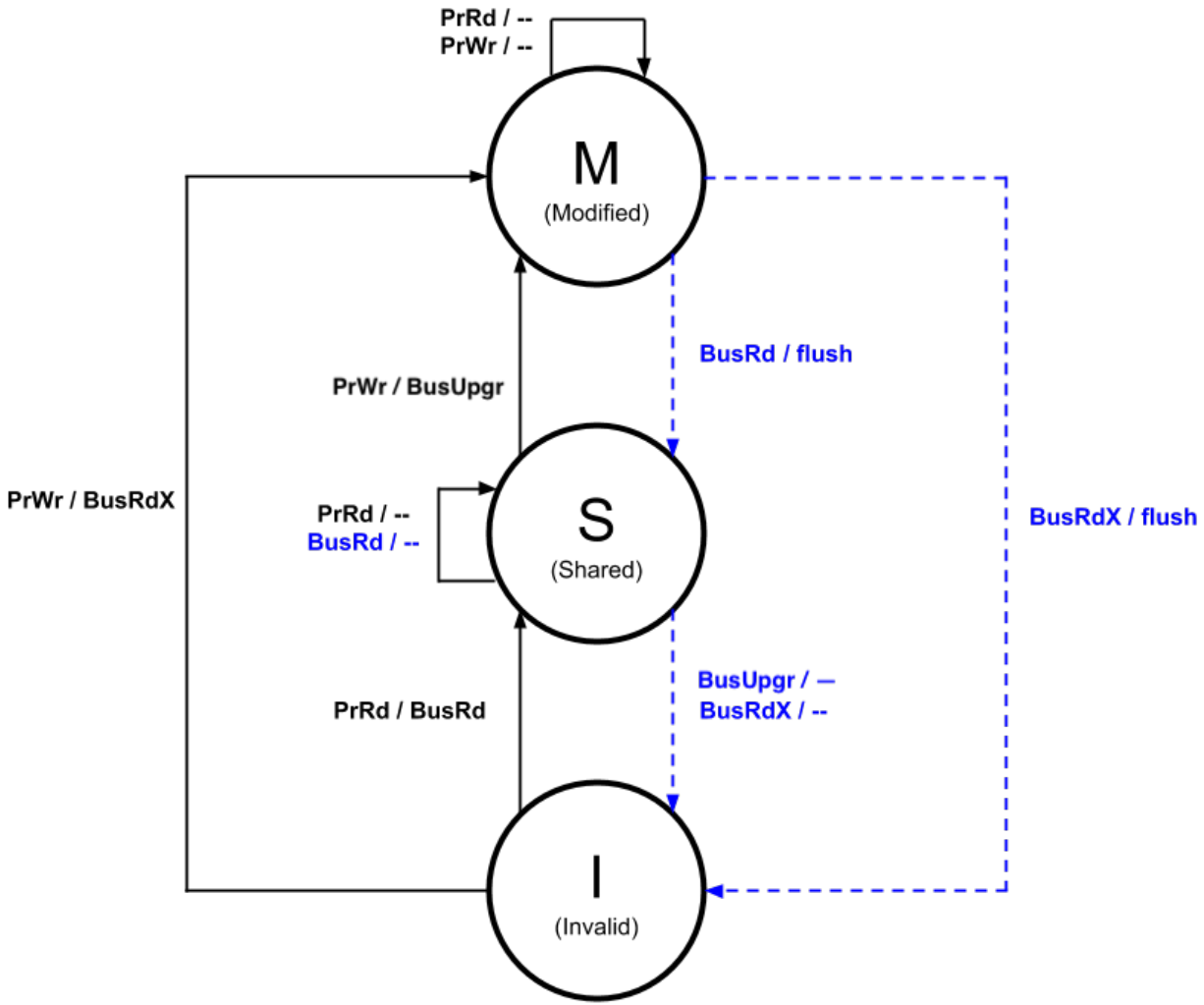
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1						
w2						
r3						
r2						
r1						



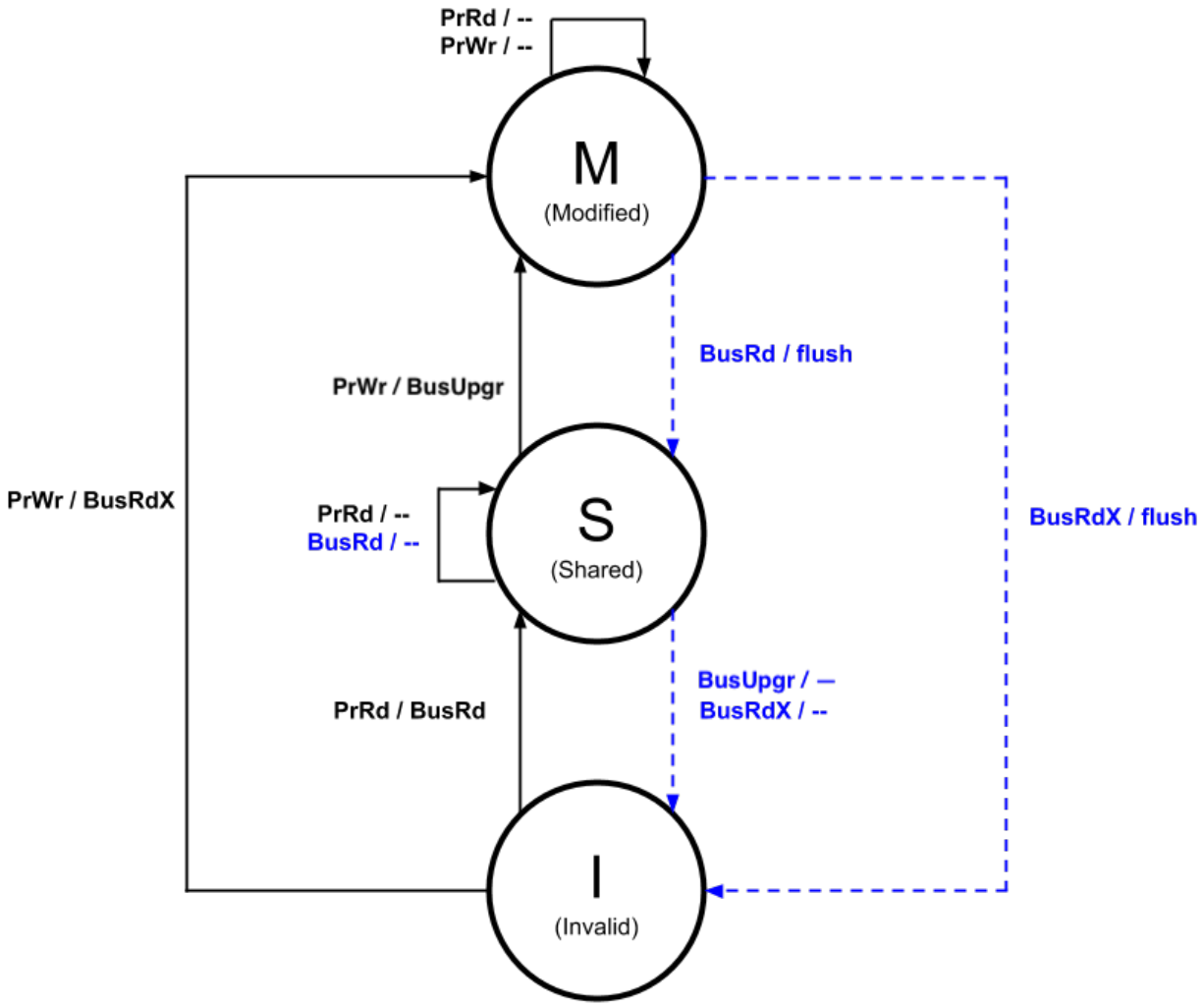
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1						
w2						
r3						
r2						
r1						



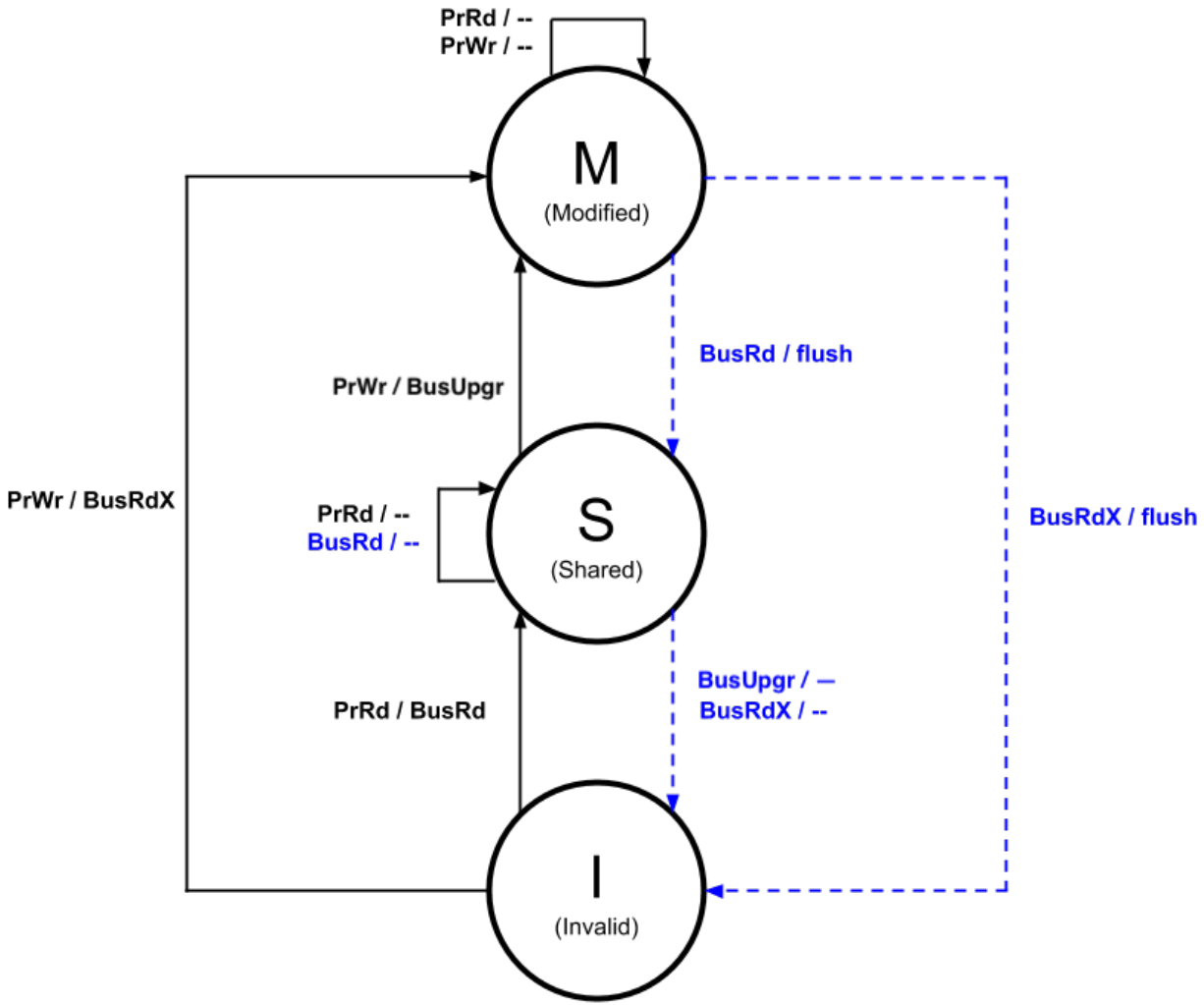
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX			
w2						
r3						
r2						
r1						



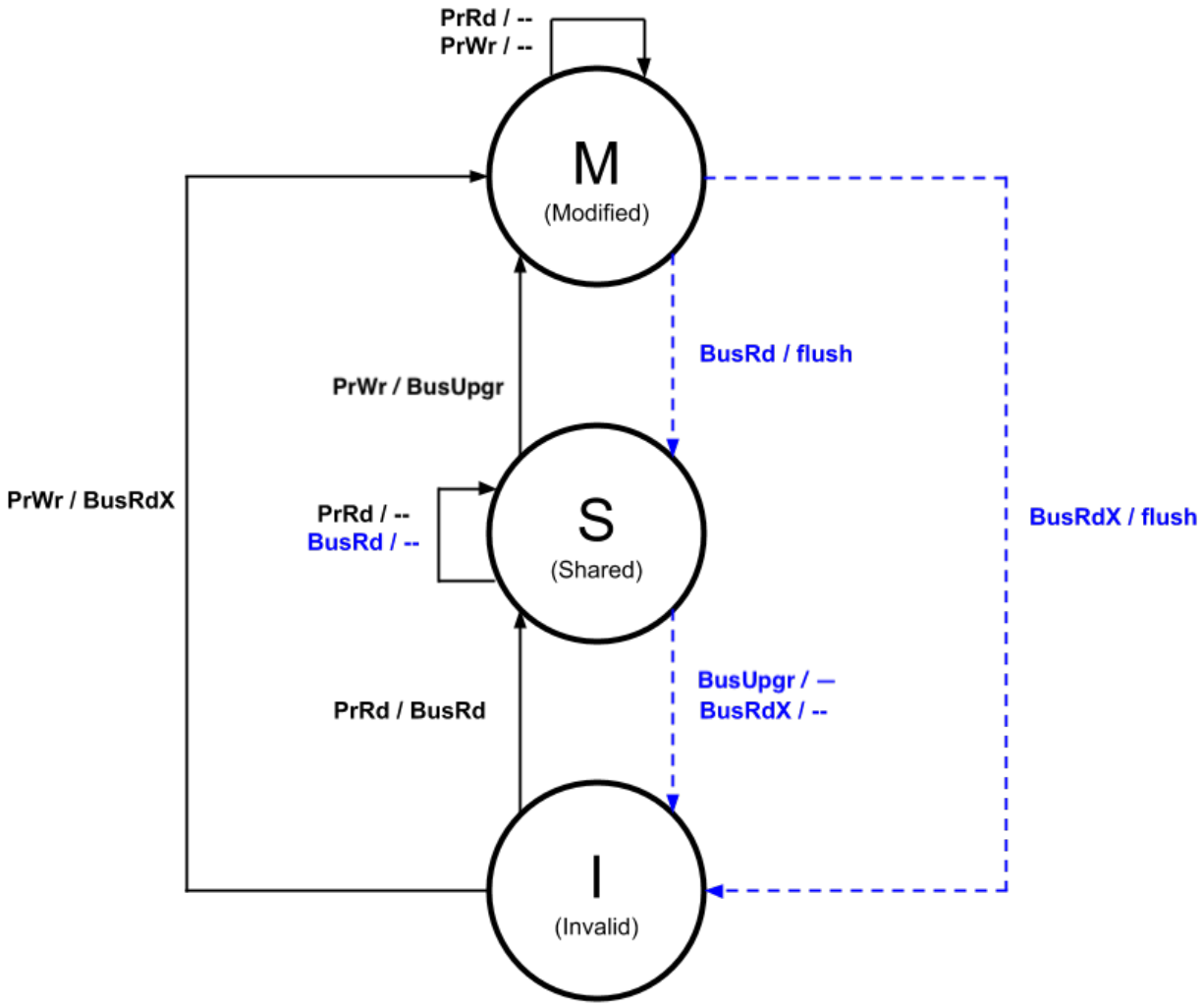
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	I	I
w2						
r3						
r2						
r1						



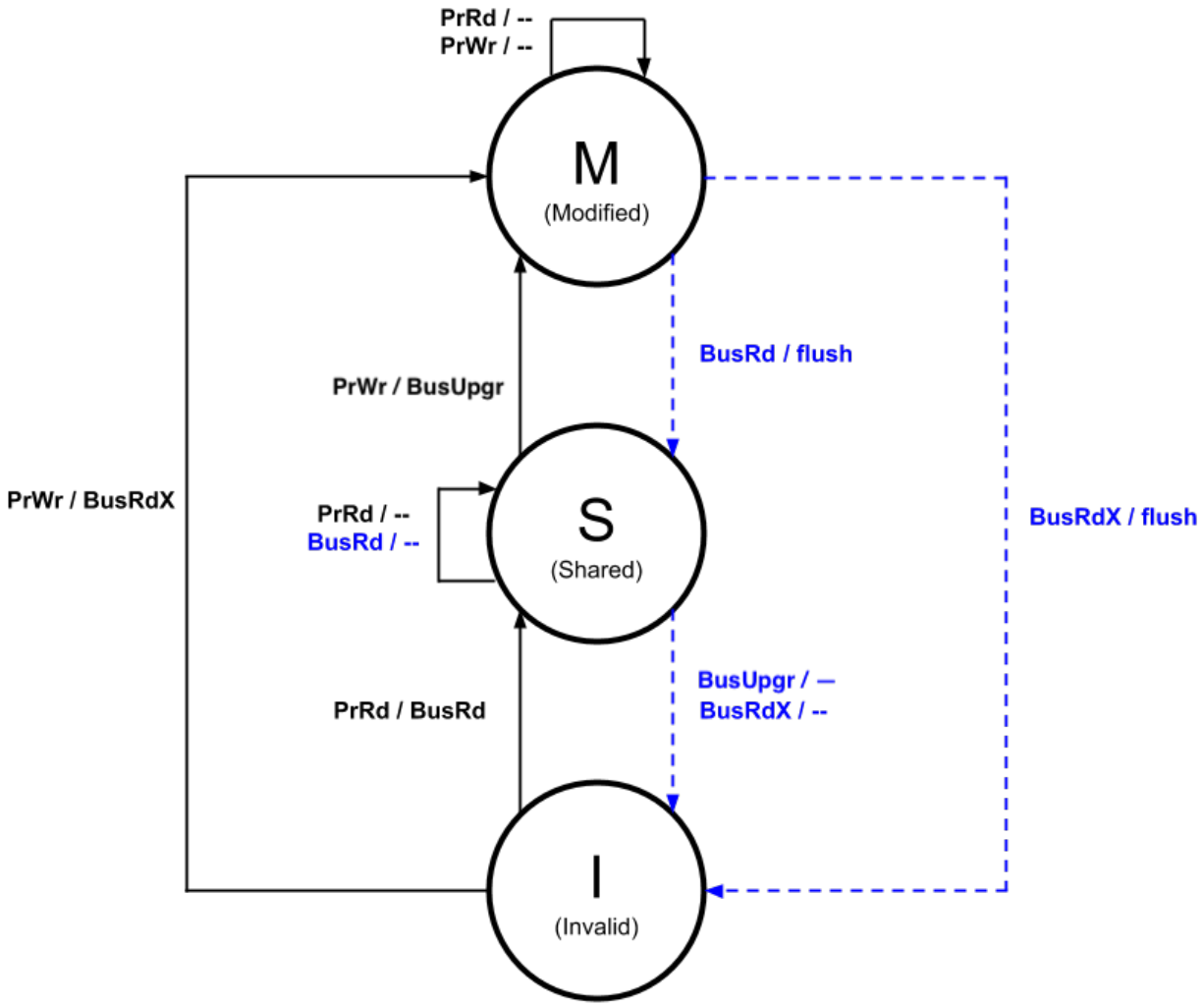
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	I	I
w2						
r3						
r2						
r1						



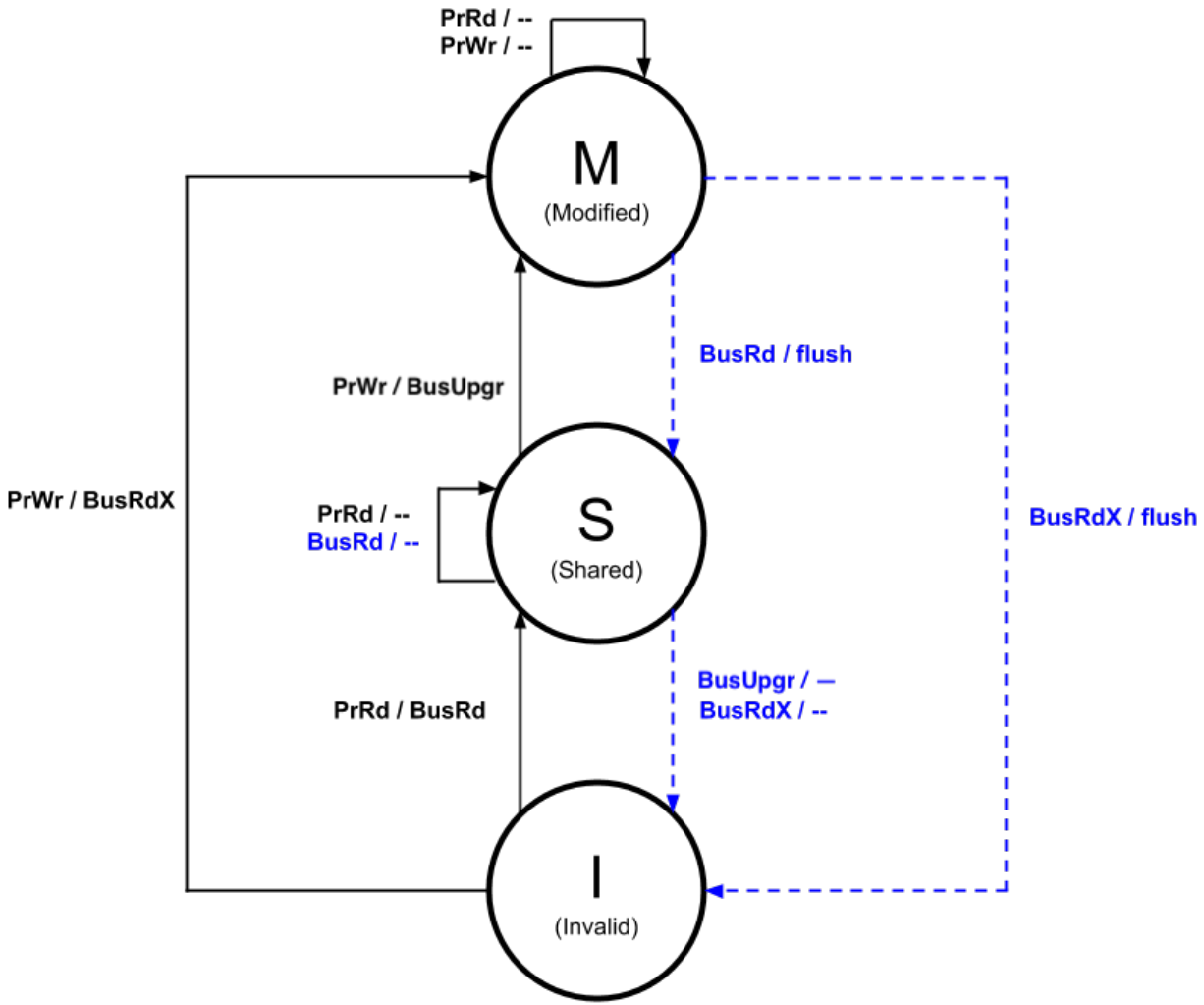
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	I	I
w2	PrWr	Miss	BusRdX/flush			
r3						
r2						
r1						



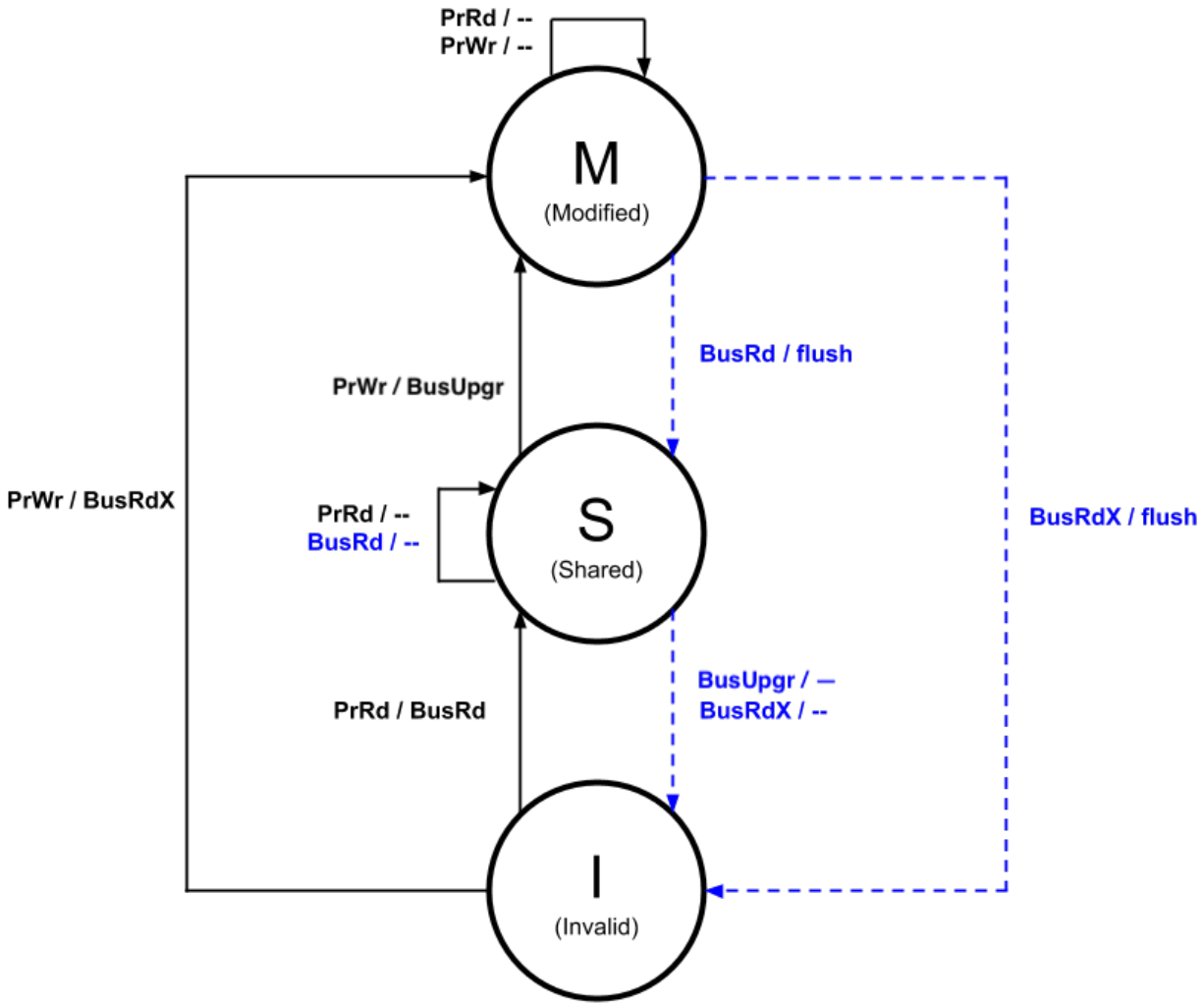
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	I	I
w2	PrWr	Miss	BusRdX/flush	I	M	I
r3						
r2						
r1						



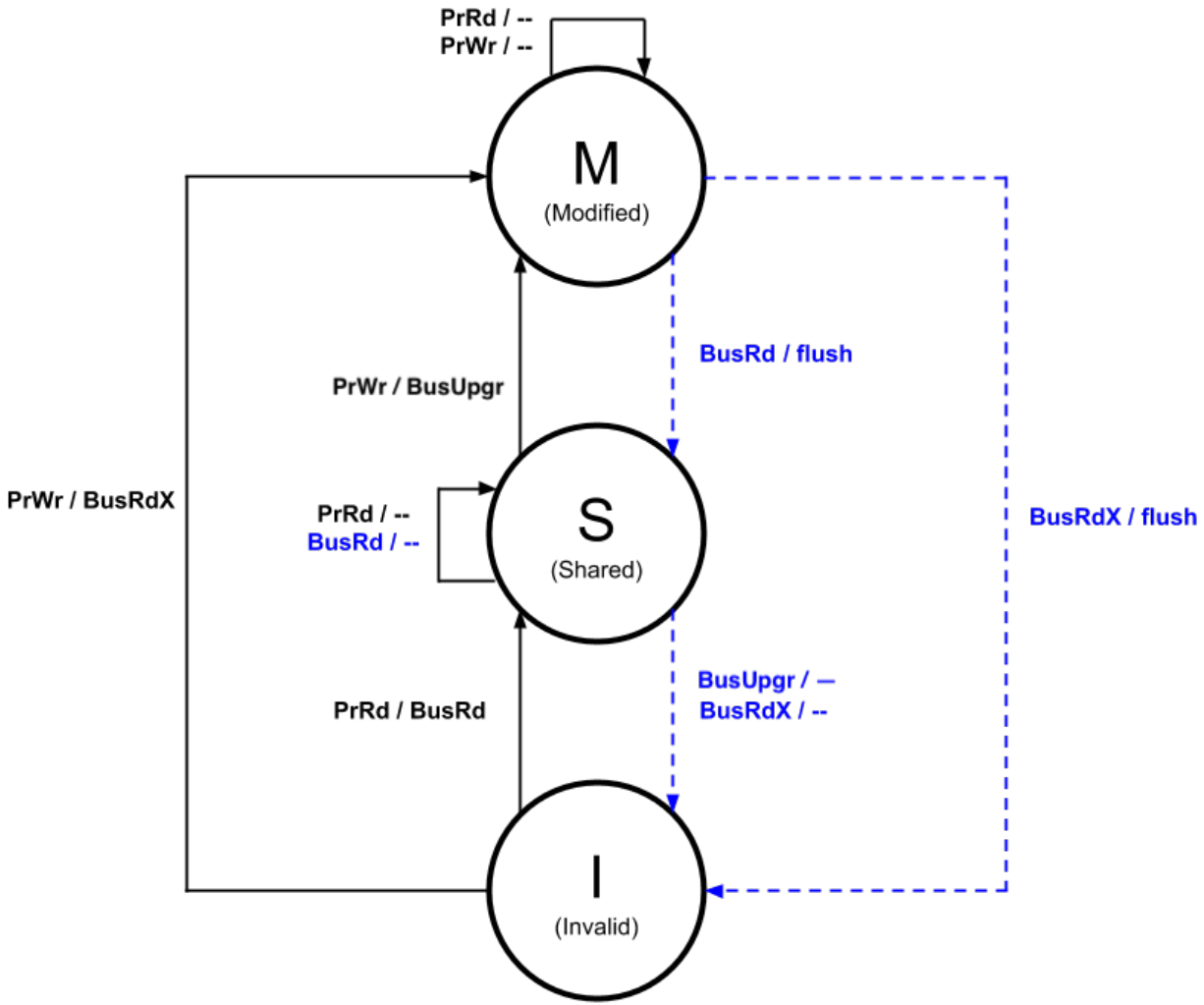
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	I	I
w2	PrWr	Miss	BusRdX/flush	I	M	I
r3						
r2						
r1						



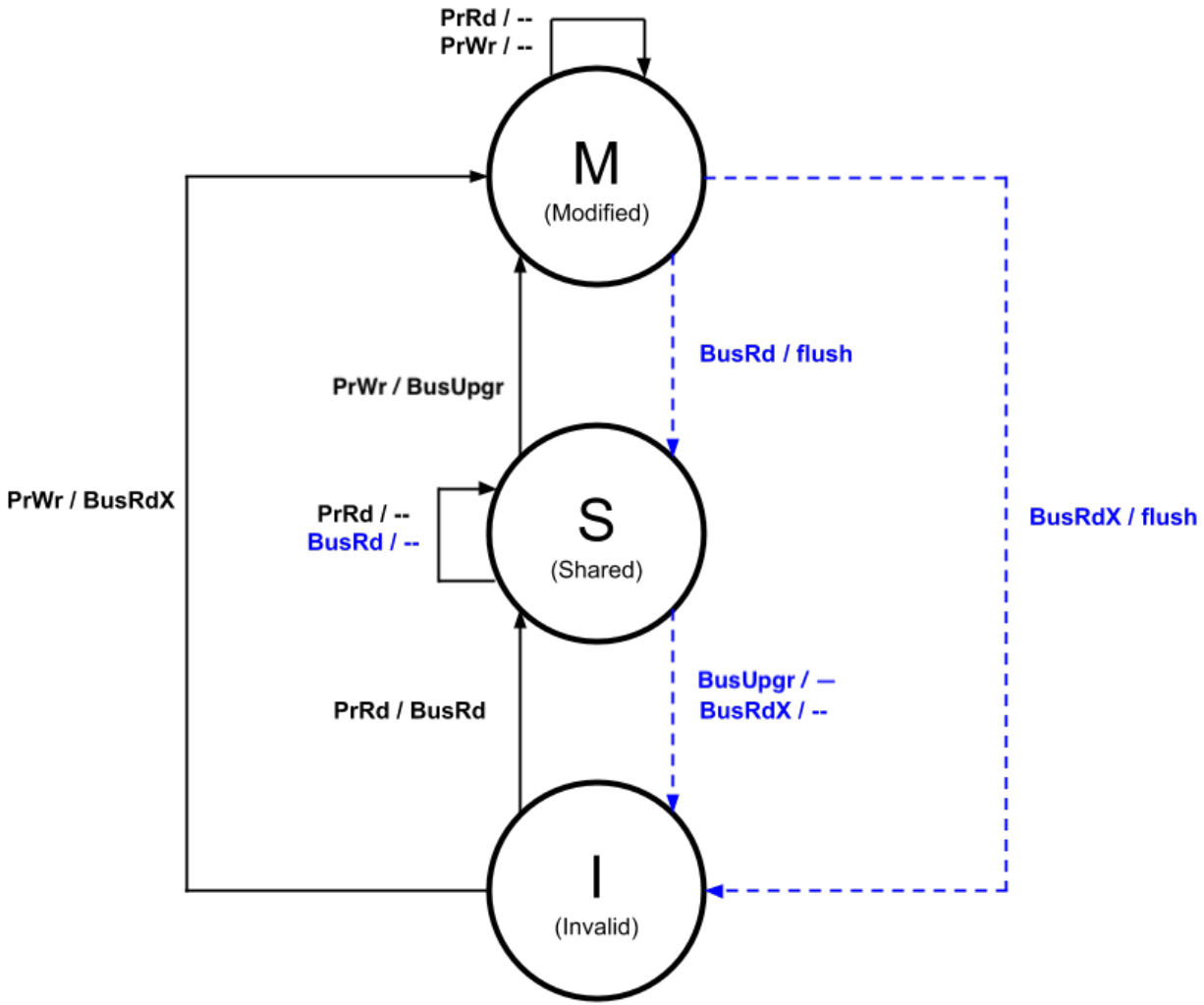
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	I	I
w2	PrWr	Miss	BusRdX/flush	I	M	I
r3	PrRd	Miss				
r2						
r1						



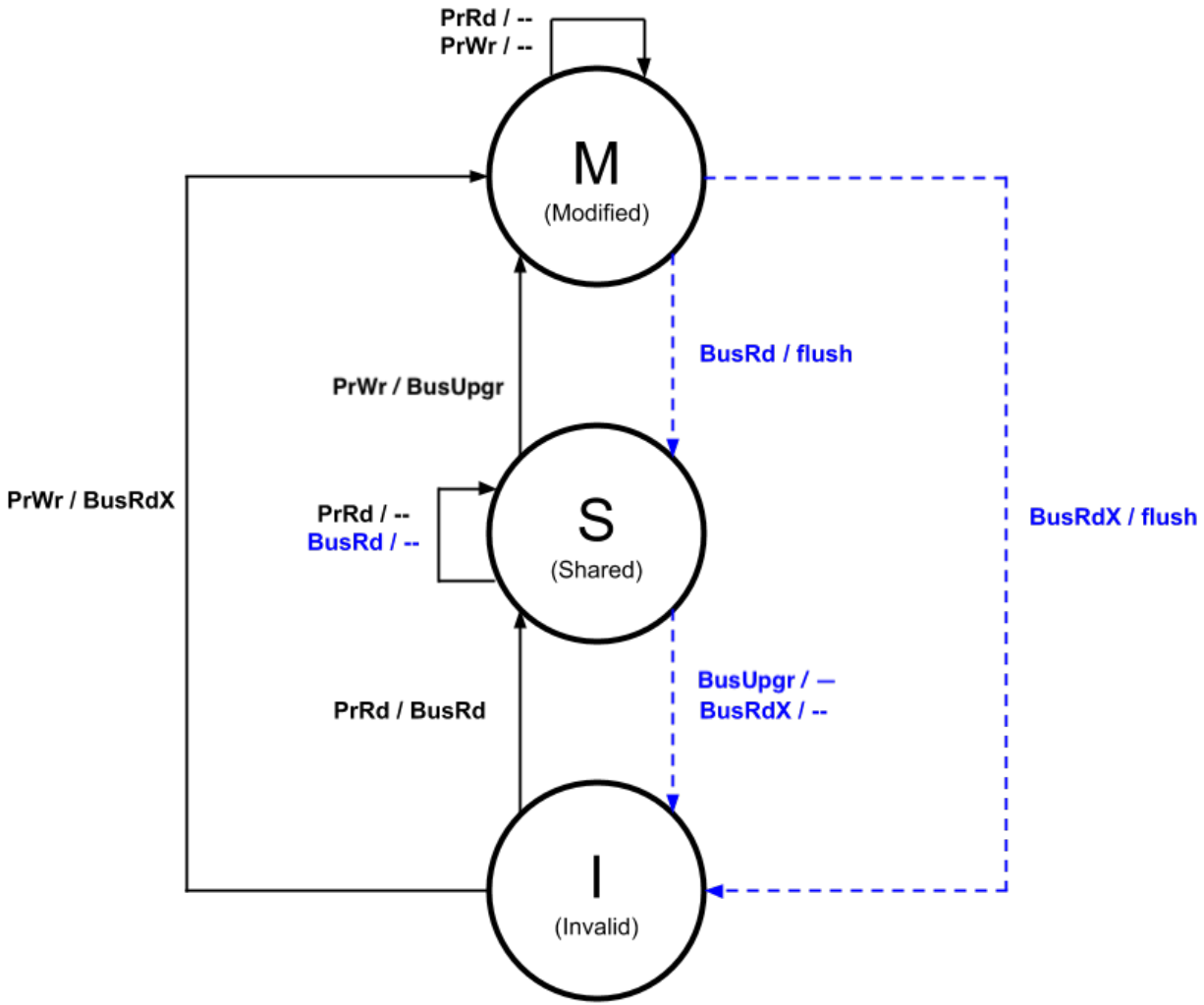
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	I	I
w2	PrWr	Miss	BusRdX/flush	I	M	I
r3	PrRd	Miss	BusRd/flush	I	S	S
r2						
r1						



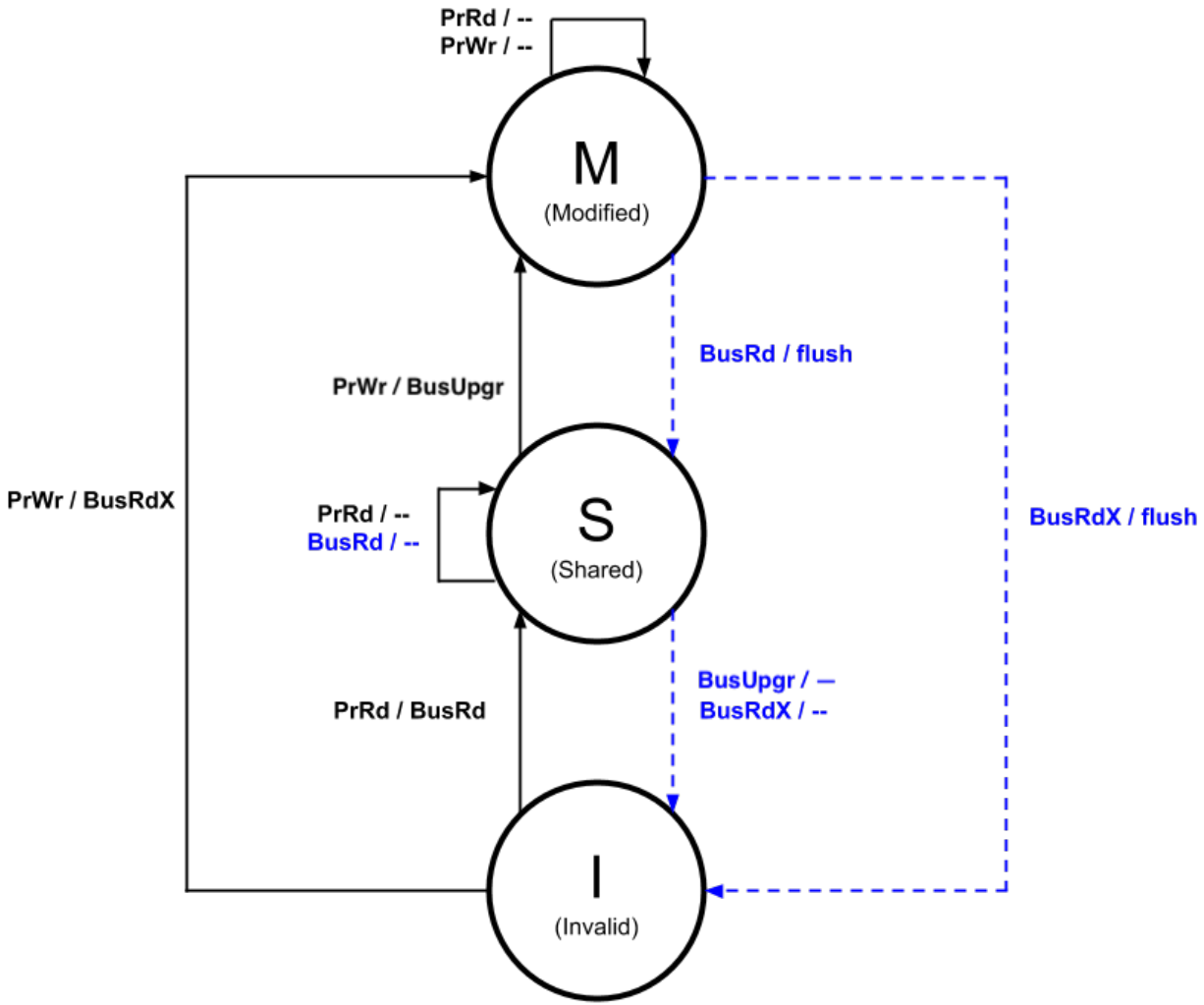
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	I	I
w2	PrWr	Miss	BusRdX/flush	I	M	I
r3	PrRd	Miss	BusRd/flush	I	S	S
r2						
r1						



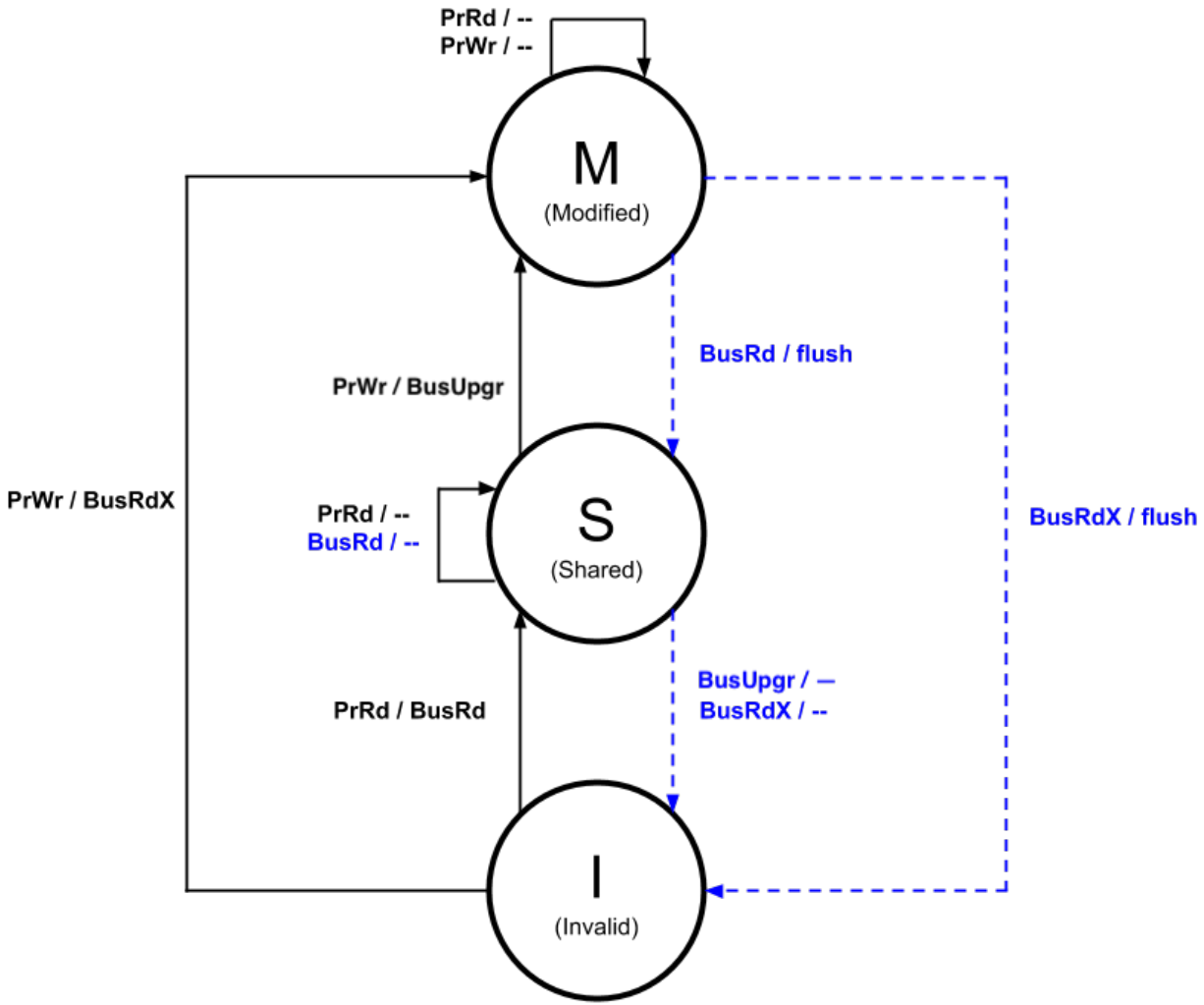
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	I	I
w2	PrWr	Miss	BusRdX/flush	I	M	I
r3	PrRd	Miss	BusRd/flush	I	S	S
r2	PrRd	Hit	-			
r1						



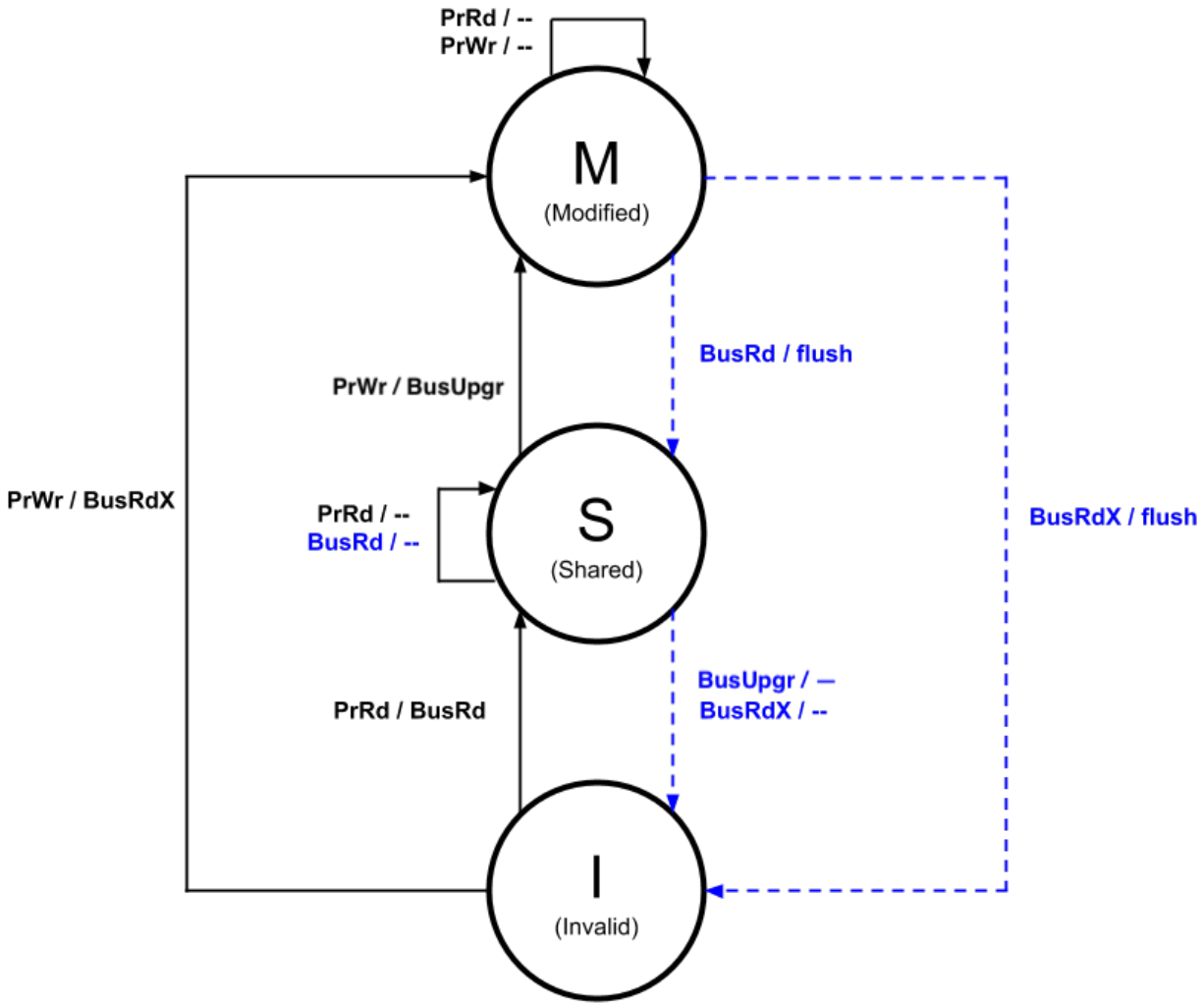
	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	I	I
w2	PrWr	Miss	BusRdX/flush	I	M	I
r3	PrRd	Miss	BusRd/flush	I	S	S
r2	PrRd	Hit	-	I	S	S
r1						



	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	I	I
w2	PrWr	Miss	BusRdX/flush	I	M	I
r3	PrRd	Miss	BusRd/flush	I	S	S
r2	PrRd	Hit	-	I	S	S
r1						



	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	I	I
w2	PrWr	Miss	BusRdX/flush	I	M	I
r3	PrRd	Miss	BusRd/flush	I	S	S
r2	PrRd	Hit	-	I	S	S
r1	PrRd	Miss	BusRd			



	CPU event	Hit/ Miss	Bus transaction(s)	mem1	mem2	mem3
r1	PrRd	Miss	BusRd	S	I	I
w1	PrWr	Hit	BusUpgr	M	I	I
r2	PrRd	Miss	BusRd/flush	S	S	I
w3	PrWr	Miss	BusRdX	I	I	M
r2	PrRd	Miss	BusRd/flush	I	S	S
w1	PrWr	Miss	BusRdX	M	I	I
w2	PrWr	Miss	BusRdX/flush	I	M	I
r3	PrRd	Miss	BusRd/flush	I	S	S
r2	PrRd	Hit	-	I	S	S
r1	PrRd	Miss	BusRd	S	S	S