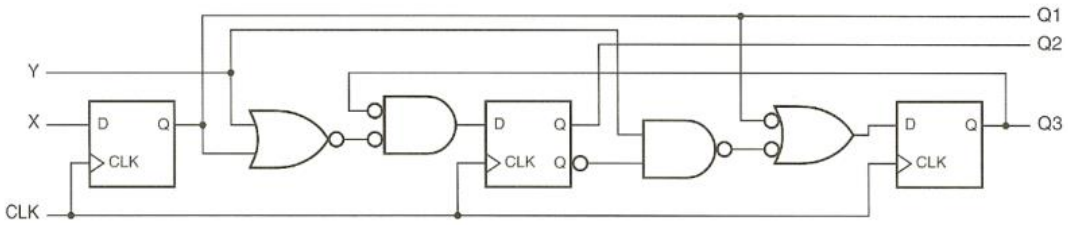
Botond Sebestyén

EMB2 ASSIGNMENT 2

1. Analyze the clocked synchronous state machine in Fig 1. Write excitation equations, transition table, and state/output table.



1a: Excitation equations:

D1 = X

D2 = Q3'*(Q1+Y)

D3 = Q1'+(Q2'*Y)

1b: Transition equations:

Q1* = X

Q2* = Q3'*(Q1+Y)

Q3* = Q1'+(Q2'*Y)

Q3 Q2 Q1	State name
0 0 0	A
0 0 1	B
0 1 0	C
0 1 1	D
1 0 0	E
1 0 1	F
1 1 0	G
1 1 1	H

1c: Transition table:

Current state	X and Y input values (XY)			
Q3Q2Q1	**00**	**01**	**10**	**11**
000	100	110	101	111
001	010	110	011	111
010	100	110	101	111
011	010	010	011	011
100	100	100	101	101
101	000	100	001	101
110	100	100	101	101
111	000	000	001	001

Q3* Q2* Q1*

1d: State table

	X and y input values			
Current state	00	01	10	11
A	E	G	F	H
B	C	G	D	H
C	E	G	F	H
D	C	C	D	D
E	E	E	F	F
F	A	E	B	F
G	E	E	F	F
H	A	A	B	B

S*

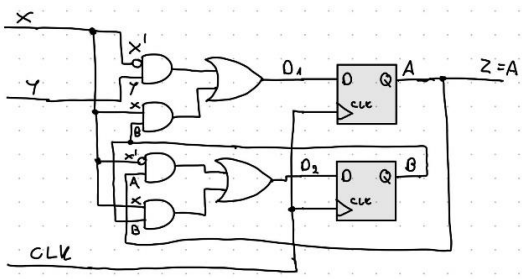
Botond Sebestyén

A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following excitation and output equations:

$$A^* = X'Y + XB$$
$$B^* = X'A + XB$$
$$Z = A$$

a. Draw the logic diagram for the circuit
b. List the state table for the sequential circuit (*Hint: headers of the state table should be: B, A, XY*)
c. Draw the corresponding state diagram

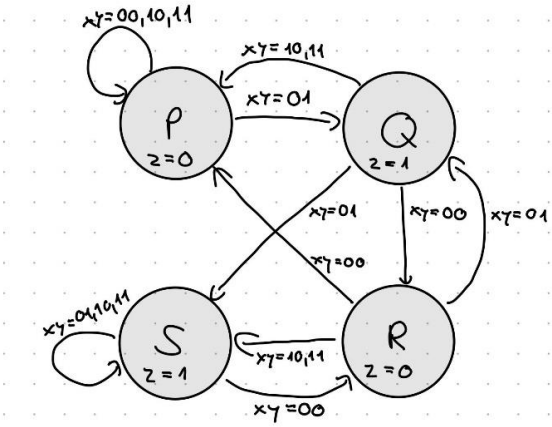
2a: Logic diagram



Transition table:

		XY			
B	A	00	01	10	11
0	0	00	01	00	00
0	1	10	11	00	00
1	0	00	01	11	11
1	1	10	11	11	11

B* A*



2b: State table

First the state names:

BA	State name
00	P
01	Q
10	R
11	S

And the table:

	XY				output
BA	00	01	10	11	Z
P	P	Q	P	P	0
Q	R	S	P	P	1
R	P	Q	S	S	0
S	R	S	S	S	1

S*

Botond Sebestyén

Design a sequential circuit with two D flip-flops Q1 and Q0 and one input X.

When X=0, the state of the circuit remains the same.
When X=1, the circuit goes through the state transition 00 - 01 - 11 - 10 and back to 00 and then repeats.
(*Hint: Headers of the state table should be Q1, Q0, X*).

Excitation equations:

Q1* = Q1*X' + Q0*X

Q0* = Q0*X' + Q1'*X

State names:

Q1Q0	Name
00	A
01	B
10	C
11	D

(Technically it is just two XOR gates, for both Q1 and Q0)

Transition table:

		X input	
Q1	Q0	0	1
0	0	00	01
0	1	01	11
1	0	10	00
1	1	11	10

Q1* Q0*

State table:

		X input	
Q1Q0		0	1
A		A	B
B		B	D
C		C	A
D		D	C

S*