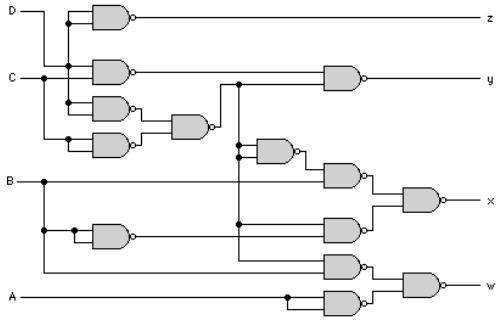
Embedded Systems Design, Spring 2025

Lecture 4



State machines and counters

Review from last time

- ?

State machine analysis

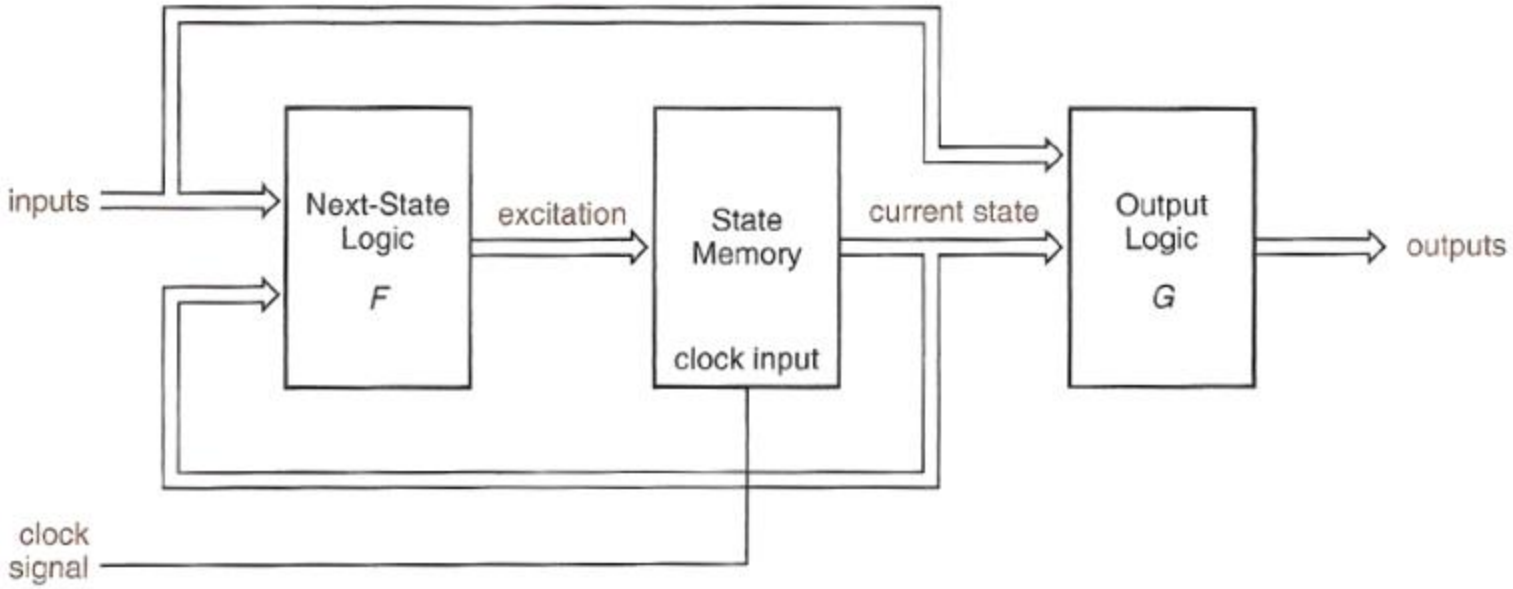
- States
- State machines
- Clocked synchronous state machines

- Next state logic
- Output logic

Mealy machine

- Next state = F(current state, input)
- Output = G(currrent state, input)

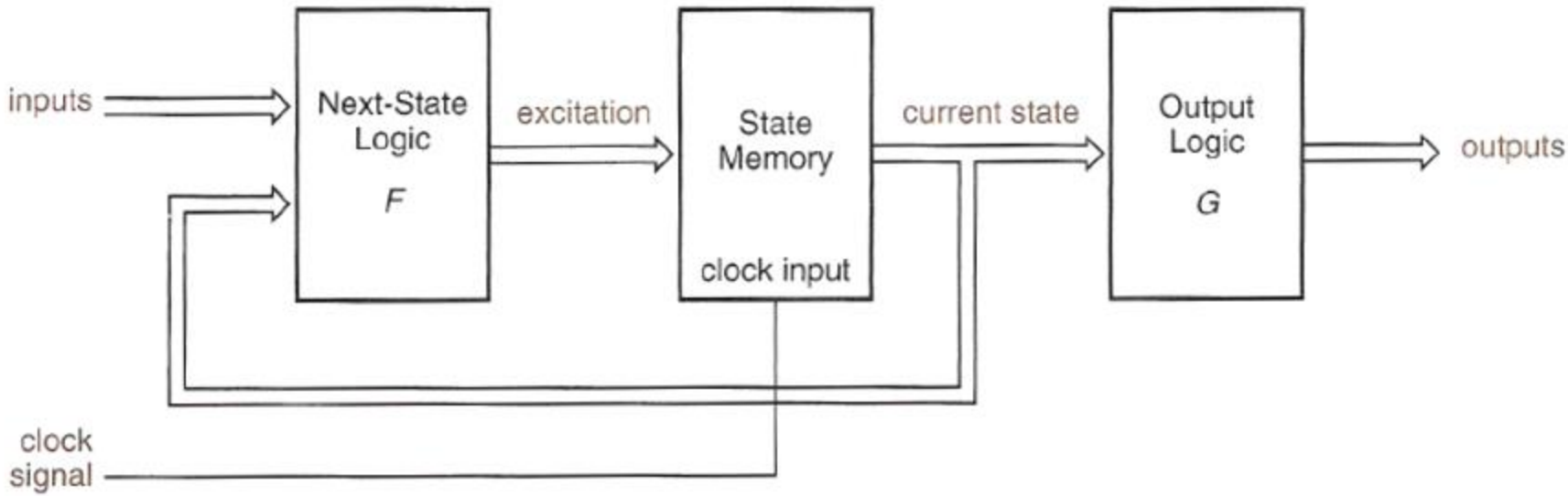
Figure 7-35 Clocked synchronous state-machine structure (Mealy machine).



Moore Machine

- Next state = F(current state, input)
- Output = G(current state)

Figure 7-36 Clocked synchronous state-machine structure (Moore machine).



Characteristic equations

Device Type	*Characteristic Equation*
S-R latch	$Q^* = S + R' \cdot Q$
D latch	$Q^* = D$
Edge-triggered D flip-flop	$Q^* = D$
D flip-flop with enable	$Q^* = EN \cdot D + EN' \cdot Q$
Master/slave S-R flip-flop	$Q^* = S + R' \cdot Q$
Master/slave J-K flip-flop	$Q^* = J \cdot Q' + K' \cdot Q$
Edge-triggered J-K flip-flop	$Q^* = J \cdot Q' + K' \cdot Q$
T flip-flop	$Q^* = Q'$
T flip-flop with enable	$Q^* = EN \cdot Q' + EN' \cdot Q$

Table 7-1
Latch and flip-flop characteristic equations.

Example

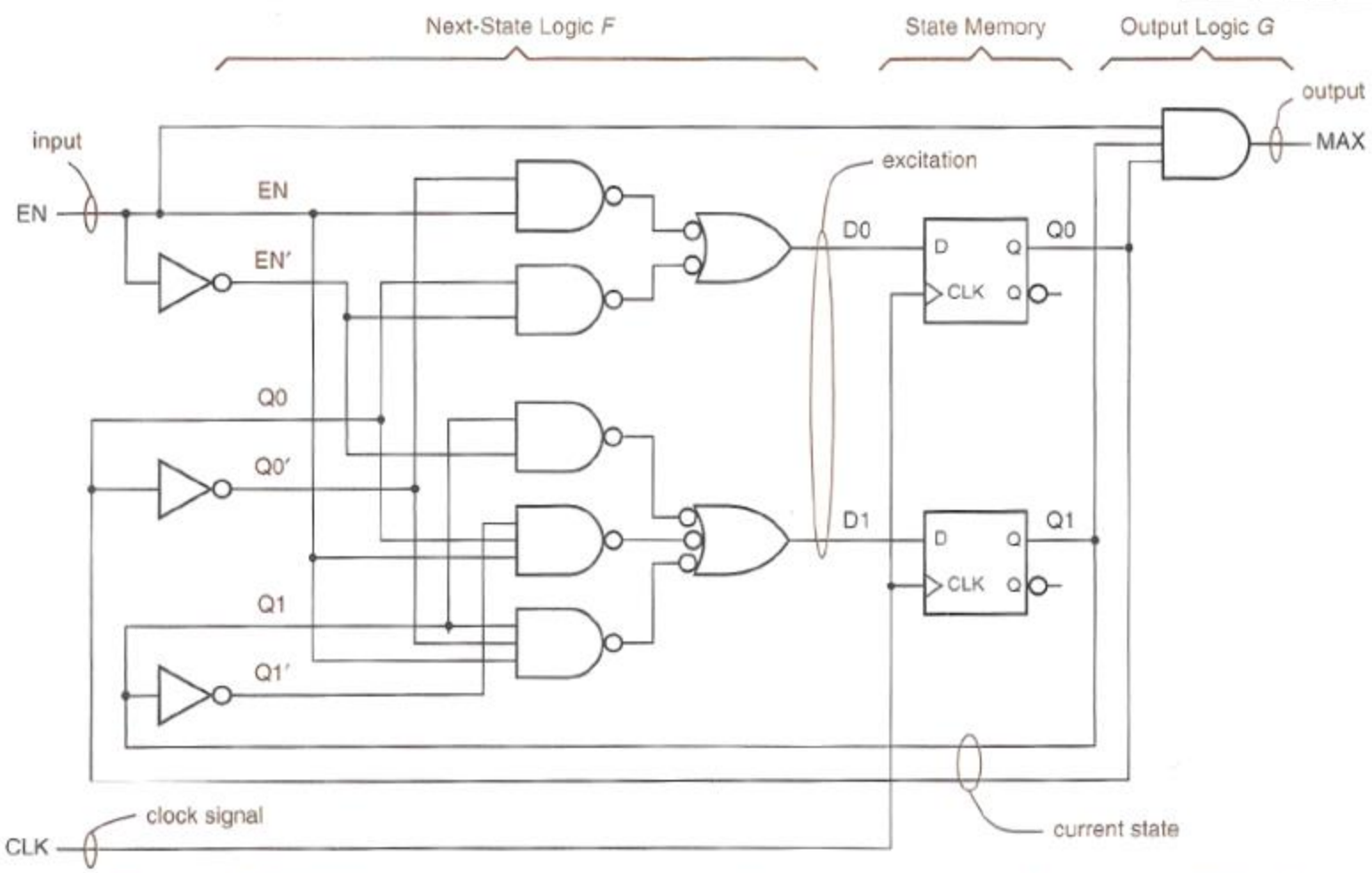


Figure 7-38 Clocked synchronous state machine using positive-edge-triggered D flip-flops.

Steps

- 1. Write the excitation equations for the FF inputs
- 2. Obtain transition equations
- 3. Determine output equations
- 4. Make transition table
- 5. Add the outputs into the transition table
- 6. Name the states and make substitutions, show the output with respect to inputs and current states
- 7. Draw state diagram

Example

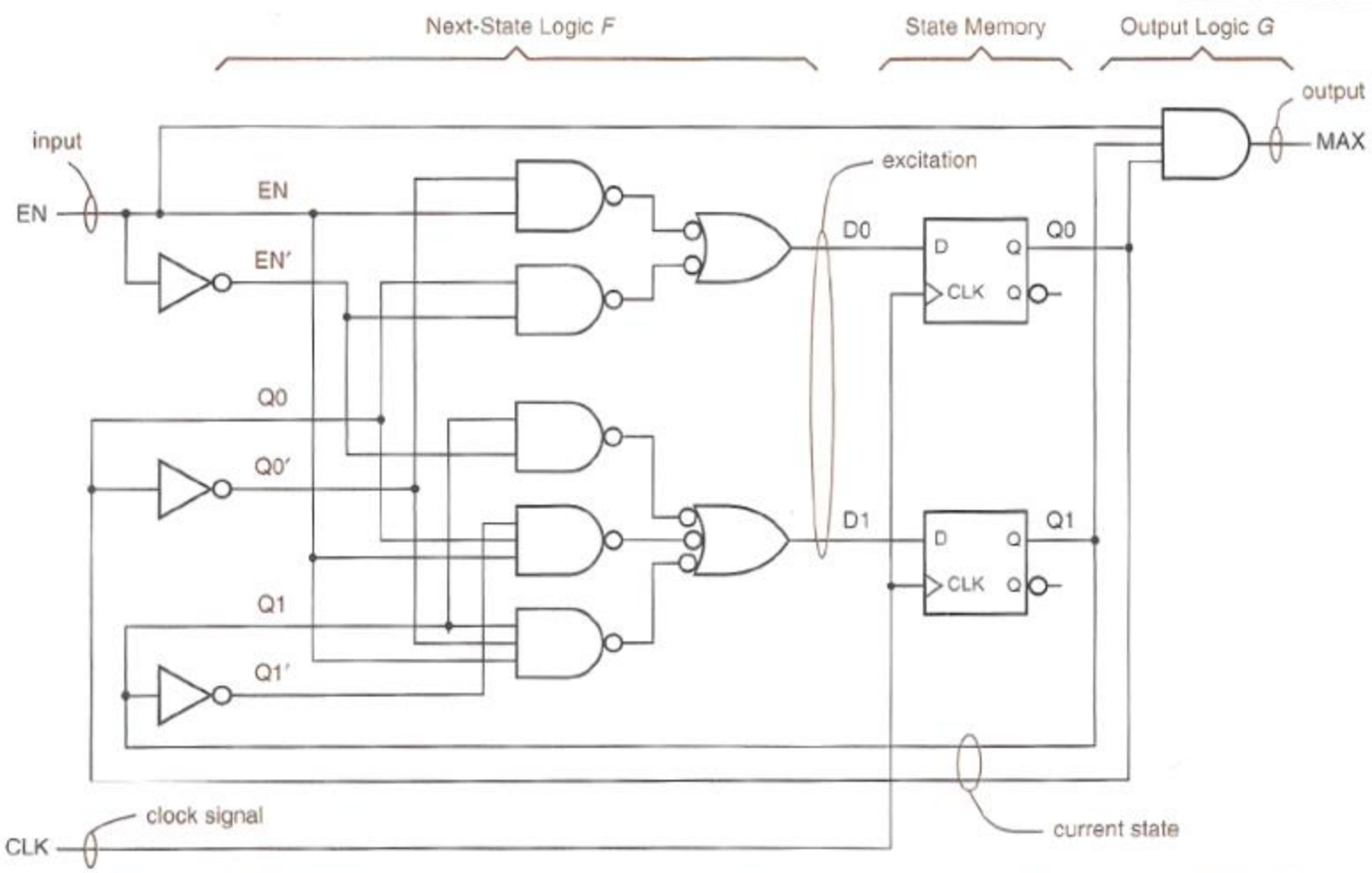


Figure 7-38 Clocked synchronous state machine using positive-edge-triggered D flip-flops.

Steps :1, 2, 3

$$D0 = Q0 \cdot EN' + Q0' \cdot EN$$
$$D1 = Q1 \cdot EN' + Q1' \cdot Q0 \cdot EN + Q1 \cdot Q0' \cdot EN$$

$$Q0* = D0$$
$$Q1* = D1$$

$$Q0* = Q0 \cdot EN' + Q0' \cdot EN$$
$$Q1* = Q1 \cdot EN' + Q1' \cdot Q0 \cdot EN + Q1 \cdot Q0' \cdot EN$$

$$MAX = Q1 \cdot Q0 \cdot EN$$

Steps 4, 5, 6

(a)

	EN	
Q1 Q0	0	1
00	00	01
01	01	10
10	10	11
11	11	00
	Q1* Q0*	

(b)

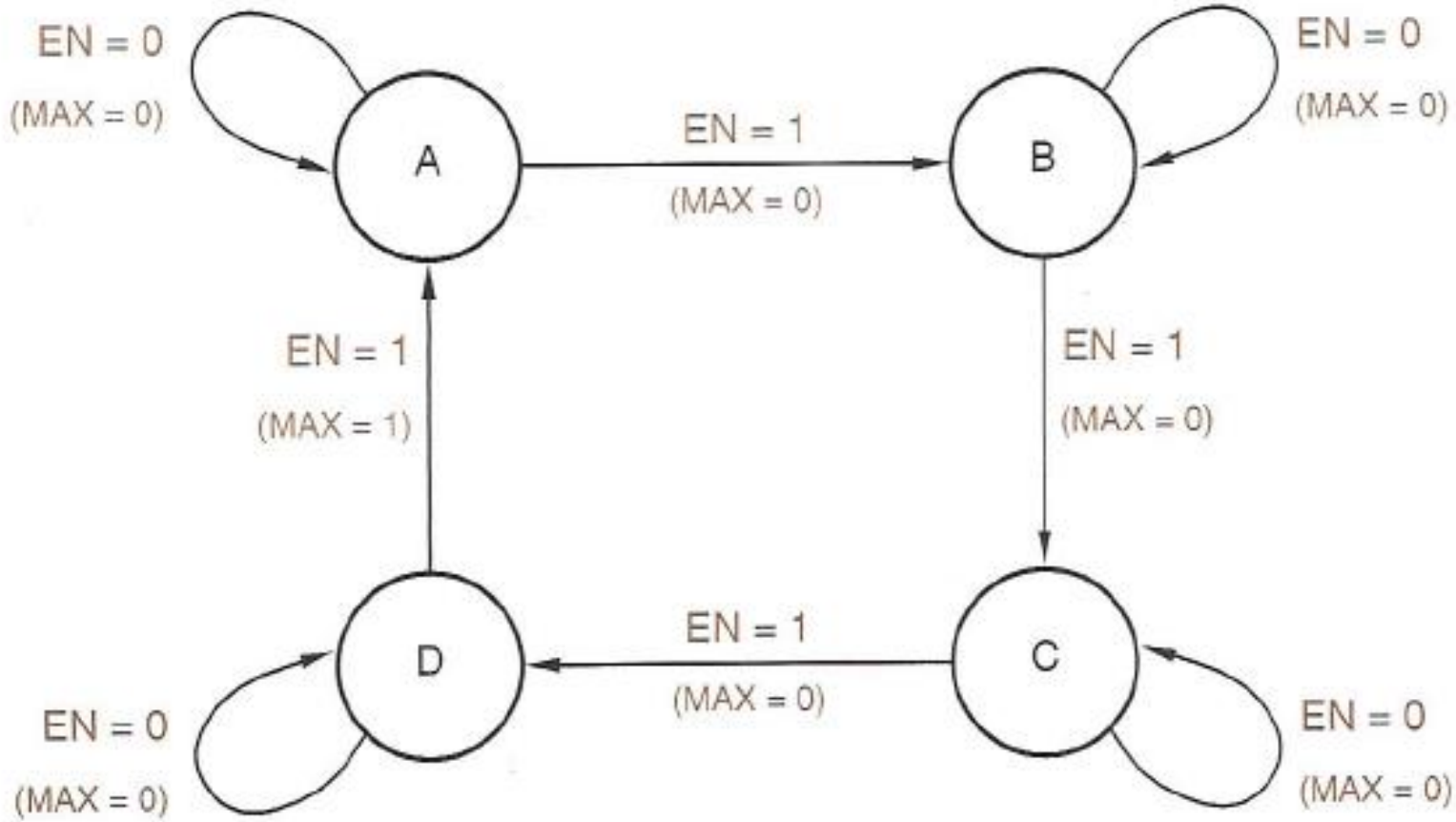
	EN	
S	0	1
A	A	B
B	B	C
C	C	D
D	D	A
	S*	

(c)

	EN	
S	0	1
A	A, 0	B, 0
B	B, 0	C, 0
C	C, 0	D, 0
D	D, 0	A, 1
	S*, MAX	

Table 7-2
Transition, state, and state/output tables for the state machine in Figure 7-38.

Step 7


EN = 0
(MAX = 0)
A
EN = 1
(MAX = 0)
B
EN = 0
(MAX = 0)
EN = 1
(MAX = 1)
EN = 1
(MAX = 0)
D
EN = 1
(MAX = 0)
C
EN = 0
(MAX = 0)
EN = 0
(MAX = 0)

Timing diagram

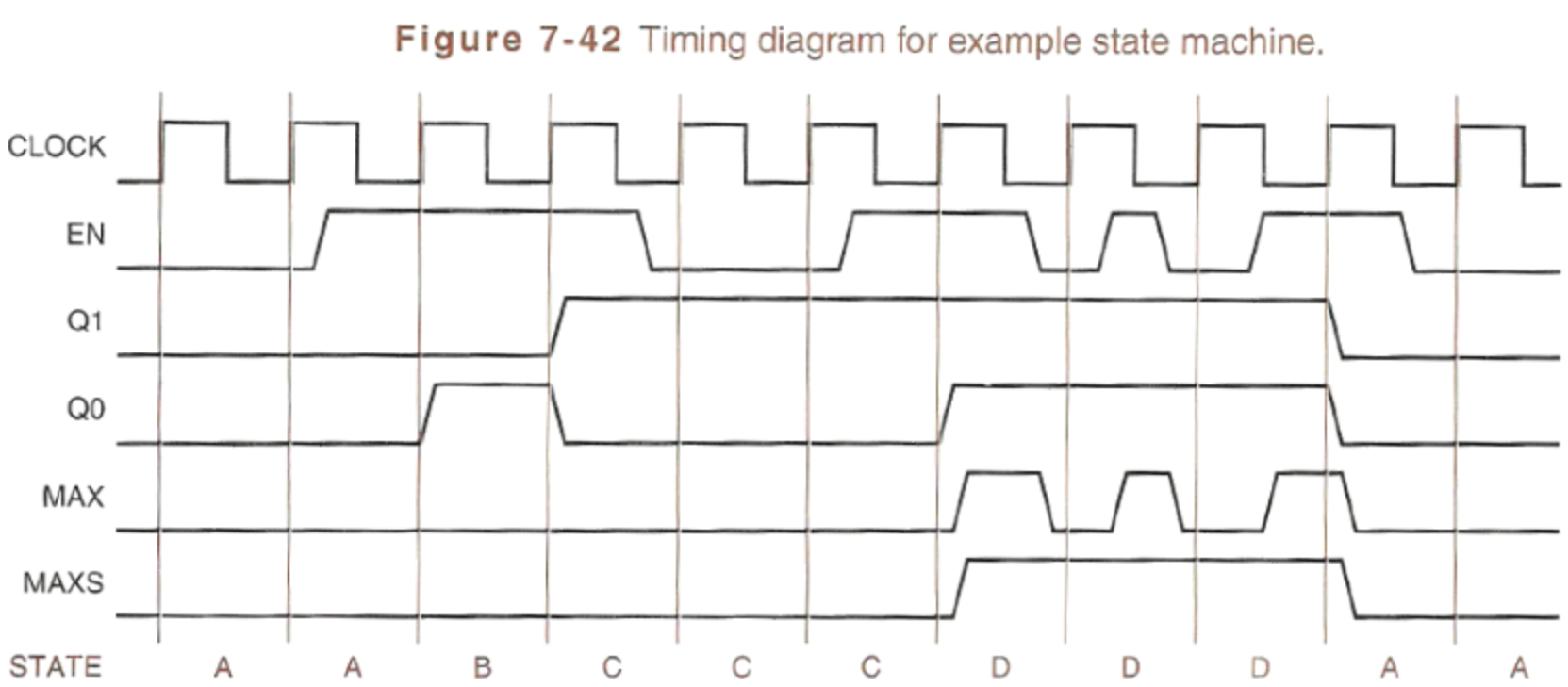
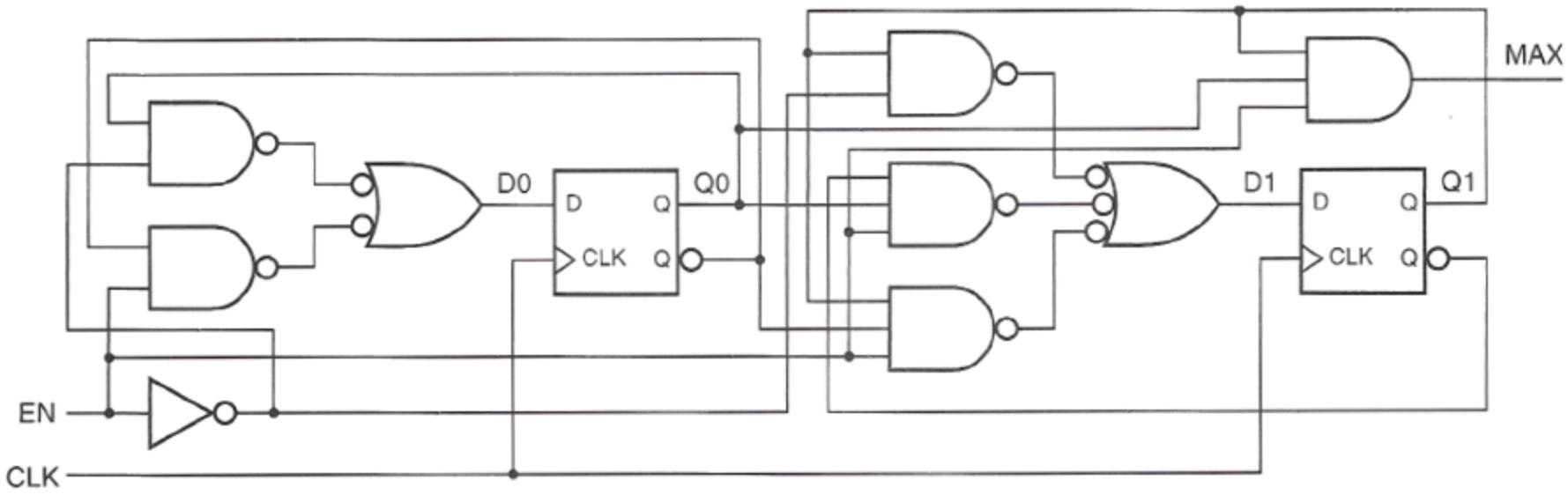


Figure 7-42 Timing diagram for example state machine.

Same example, different circuit

Figure 7-41 Redrawn logic diagram for a clocked synchronous state machine.



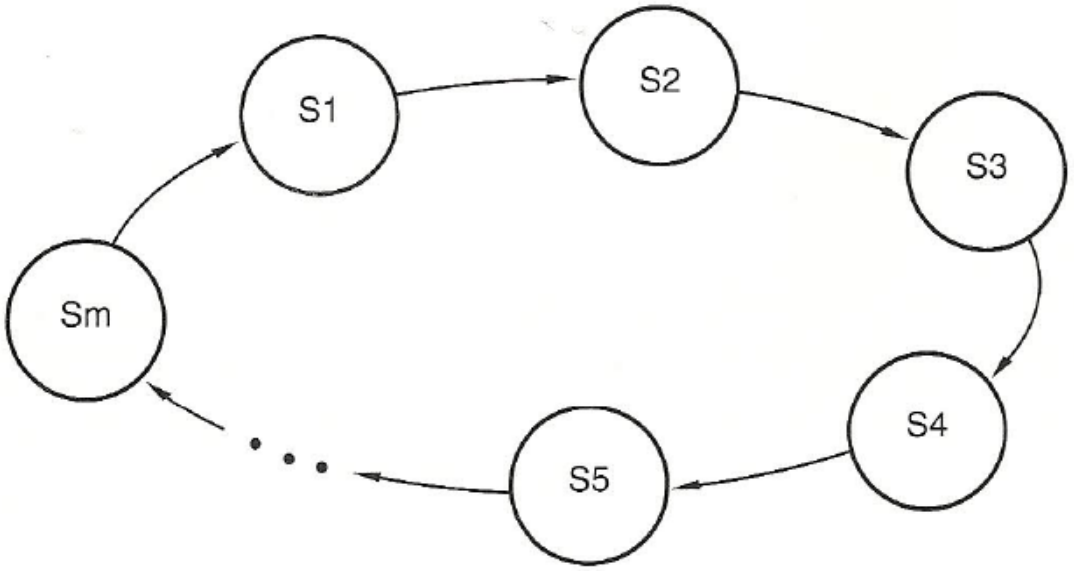
Drill state machine problem

- About 15 minutes

- Remember the steps
  - 1. Write the excitation equations for the FF inputs
  - 2. Obtain transition equations
  - 3. Determine output equations
  - 4. Make transition table
  - 5. Add the outputs into the transition table
  - 6. Name the states and make substitutions, show the output with respect to inputs and current states
  - 7. Draw state diagram

Counters

Figure 8-23
General structure of a counter's state diagram—a single cycle.



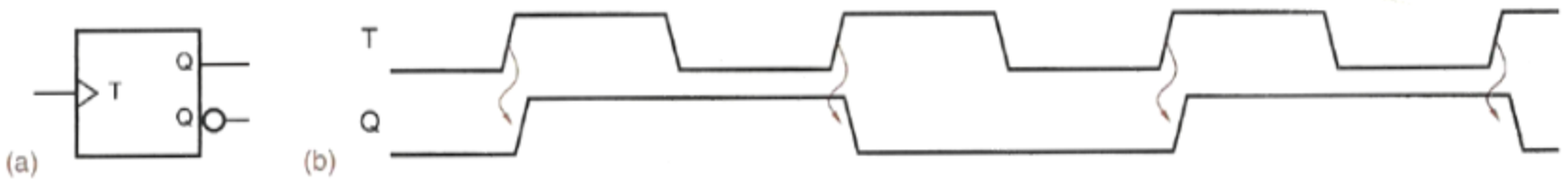


Figure 7-31 Positive-edge-triggered T flip-flop: (a) logic symbol; (b) functional behavior.

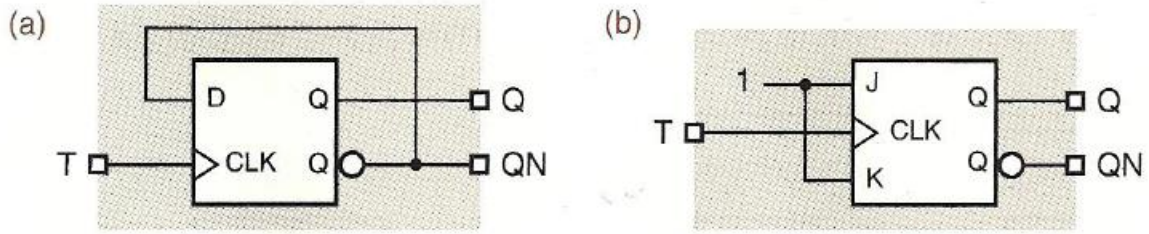
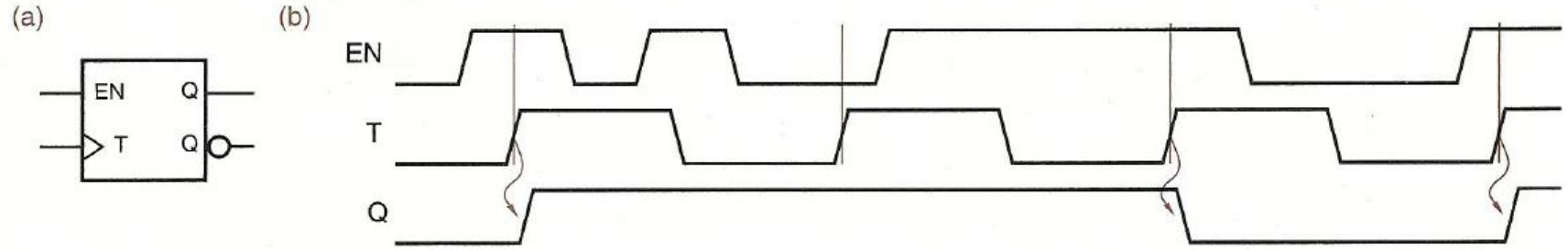


Figure 7-32
Possible circuit designs for a T flip-flop: (a) using a D flip-flop; (b) using a J-K flip-flop.

Figure 7-33 Positive-edge-triggered T flip-flop with enable: (a) logic symbol; (b) functional behavior.



Ripple counter

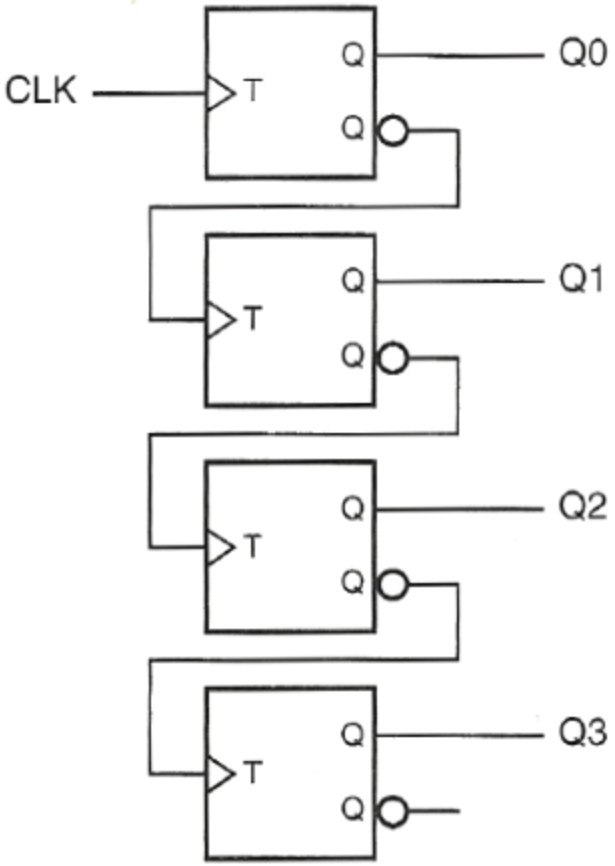


Figure 8-24
A 4-bit binary ripple counter.

Serial enable logic

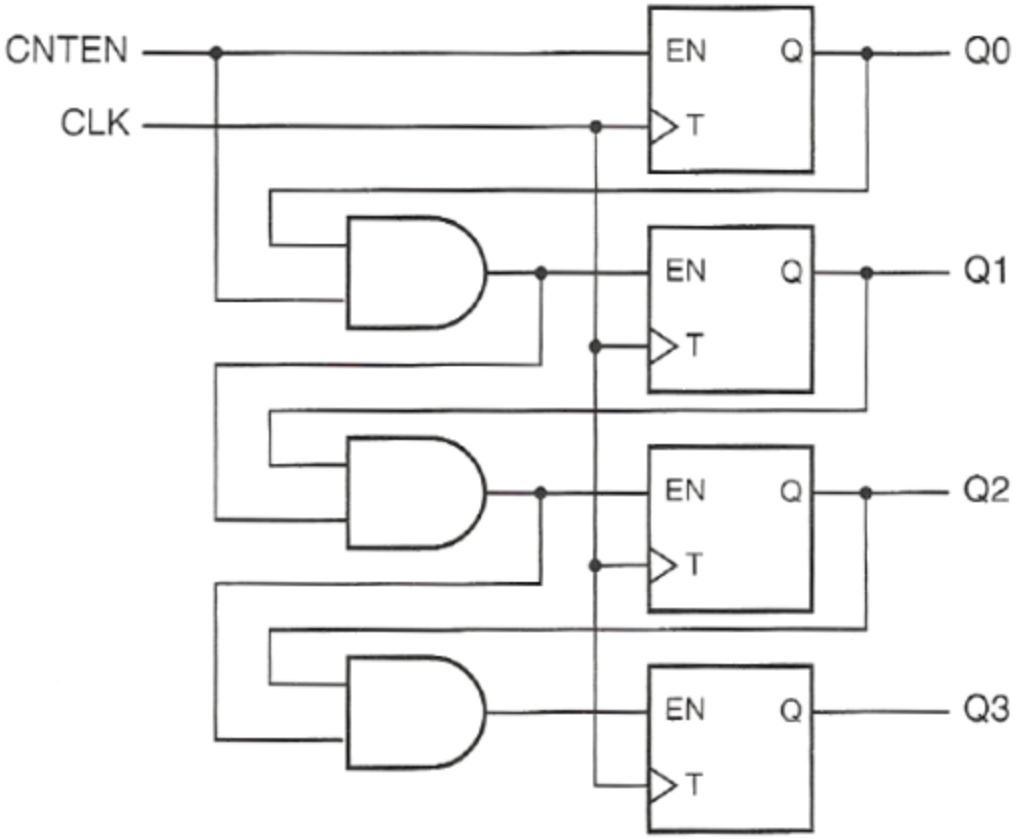
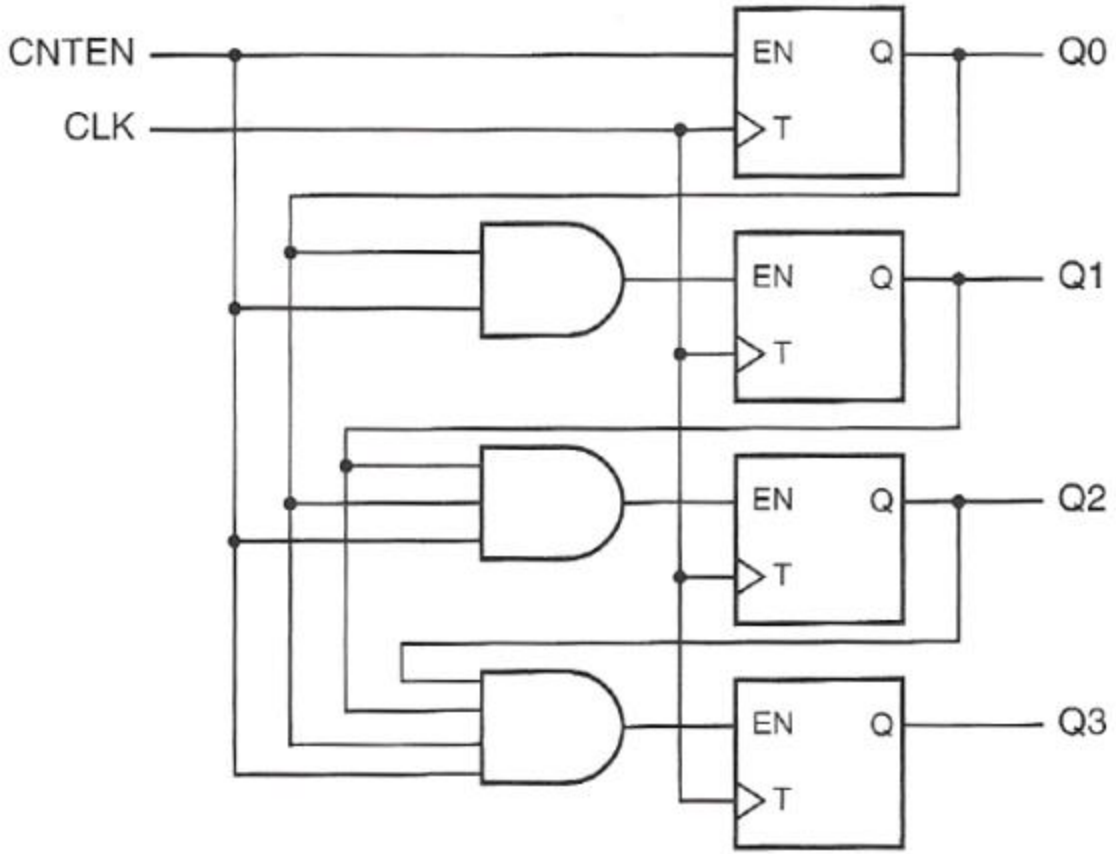


Figure 8-25
A synchronous 4-bit binary counter with serial enable logic.

Parallel enable logic

Figure 8-26
A synchronous 4-bit binary counter with parallel enable logic.



Logic symbol for the 74x163 timer

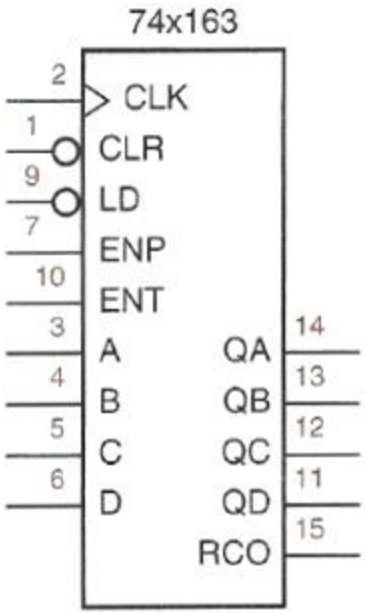


Figure 8-27
Traditional logic symbol for the 74x163.

Table 8-13 State table for a 74x163 4-bit binary counter.

Inputs				*Current State*				*Next State*			
CLR_L	*LD_L*	*ENT*	*ENP*	*QD*	*QC*	*QB*	*QA*	*QD**	*QC**	*QB**	*QA**
0	x	x	x	x	x	x	x	0	0	0	0
1	0	x	x	x	x	x	x	D	C	B	A
1	1	0	x	x	x	x	x	QD	QC	QB	QA
1	1	x	0	x	x	x	x	QD	QC	QB	QA
1	1	1	1	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	1	0	0	1	0
1	1	1	1	0	0	1	0	0	0	1	1
1	1	1	1	0	0	1	1	0	1	0	0
1	1	1	1	0	1	0	0	0	1	0	1
1	1	1	1	0	1	0	1	0	1	1	0
1	1	1	1	0	1	1	0	0	1	1	1
1	1	1	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0	1	0	0	1
1	1	1	1	1	0	0	1	1	0	1	0
1	1	1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	1	1	1	1	0	0
1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0

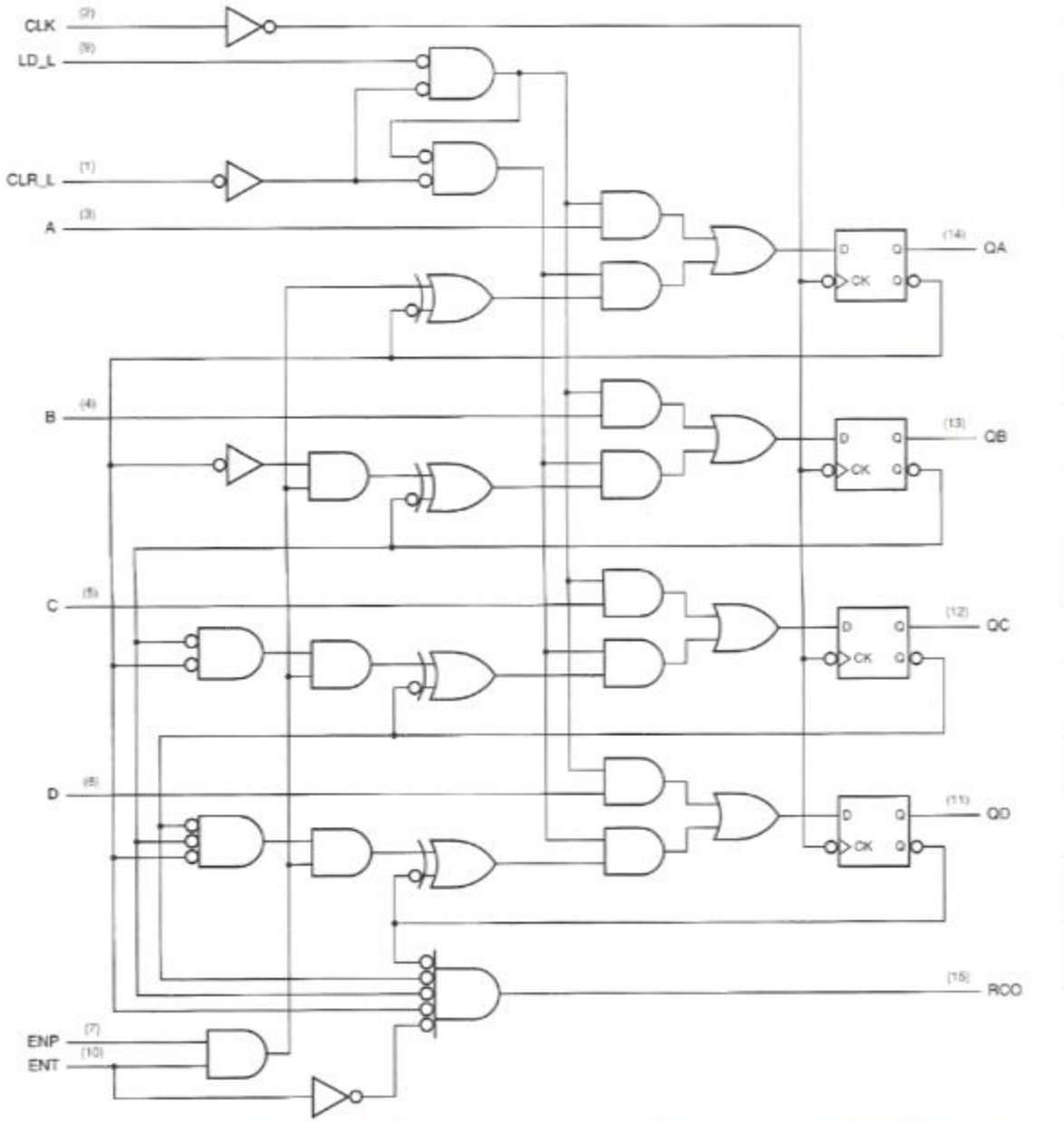
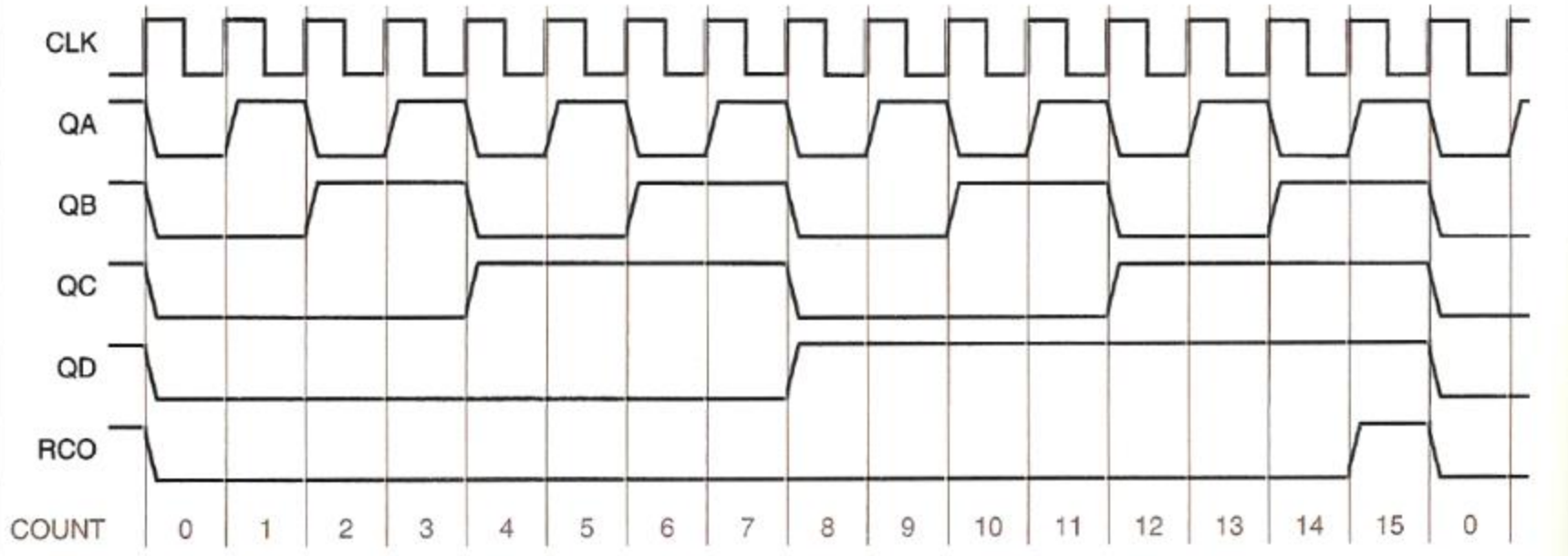


Figure 8-28 Logic diagram for the 74x163 synchronous 4-bit binary counter, including pin numbers for a standard 16-pin DIP package.

Divide by 16 counter

Figure 8-30 Clock and output waveforms for a free-running divide-by-16 counter.



Example of binary counter

- https://www.youtube.com/watch?v=U7ARbuAPPs4

- **Task:** simulate a 4 bit counter using the following template
- https://simulator.io/board/lrBpIXomS7/229

Assignment 2

- …discussion