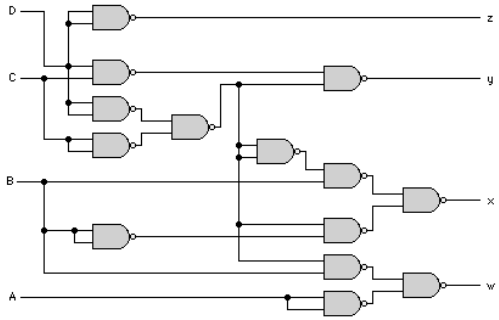
Embedded Systems Design, Spring 2025

Lecture 3



Sequential Logic: Latches and flip-flops

Review from last time

- ?

Bistability

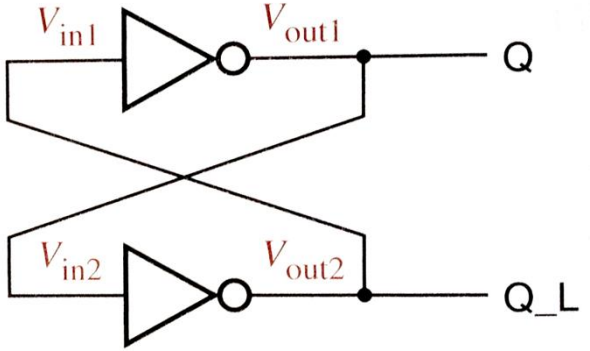
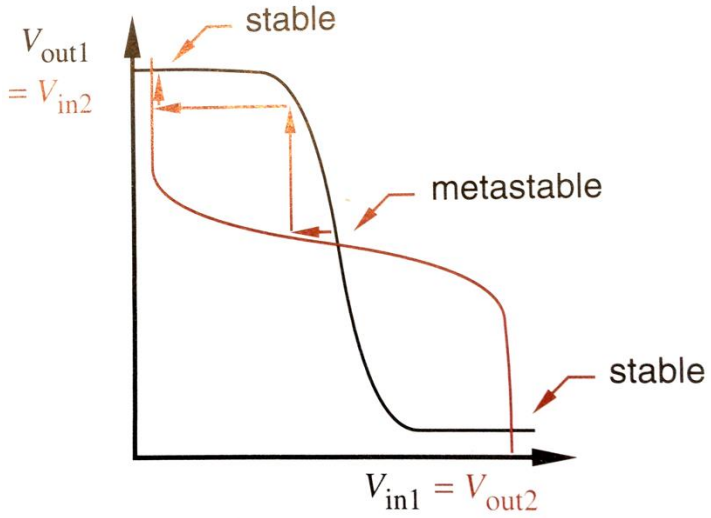


Figure 7-2
A pair of inverters forming a bistable element.



Flip flops (latches)

- 1918 – Eccles - Jordan triggered circuit

- Latches can change their state at any time
- Flip-flops can change their state only when a clocking signal is changing

Clock types

- Clock types

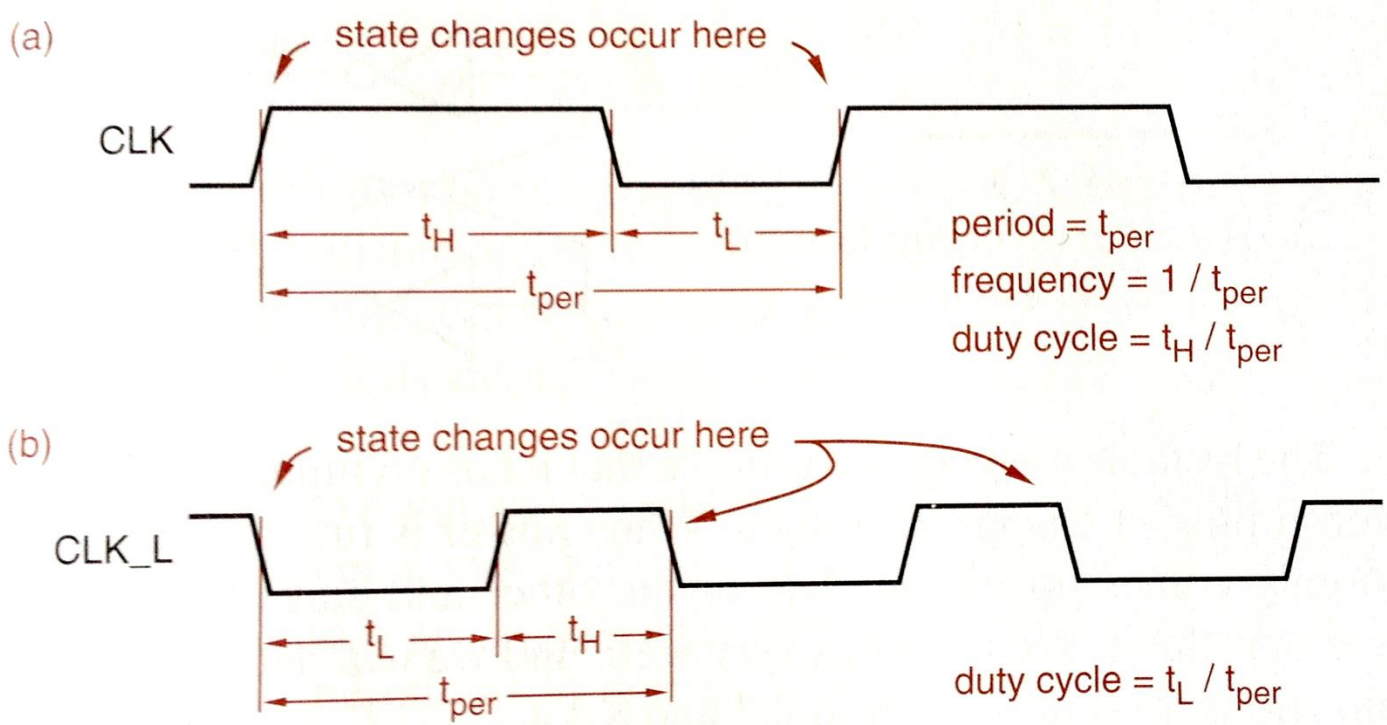
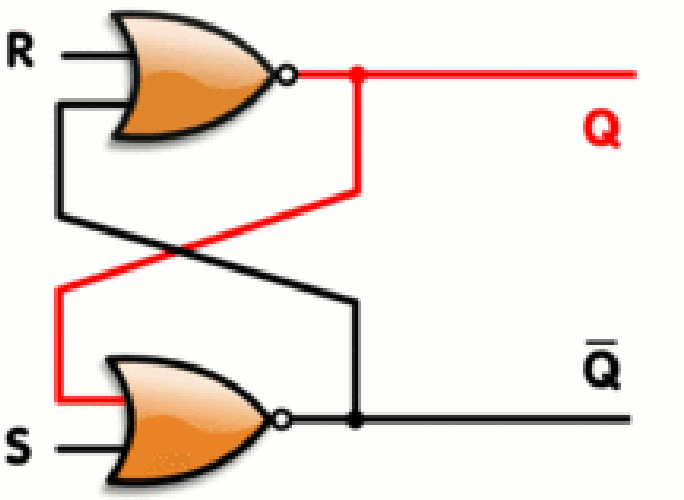
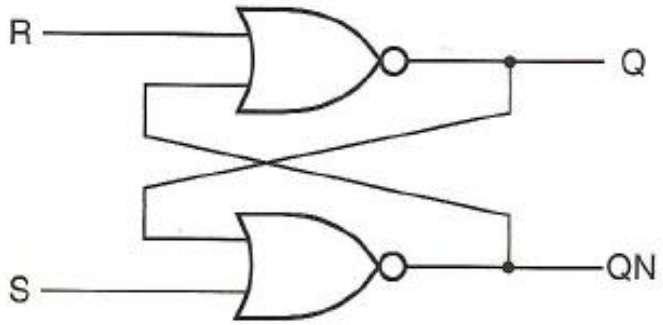


Figure 7-1
Clock signals:
(a) active high;
(b) active low.

S-R latch

- S-R latch:





(a)

(b)

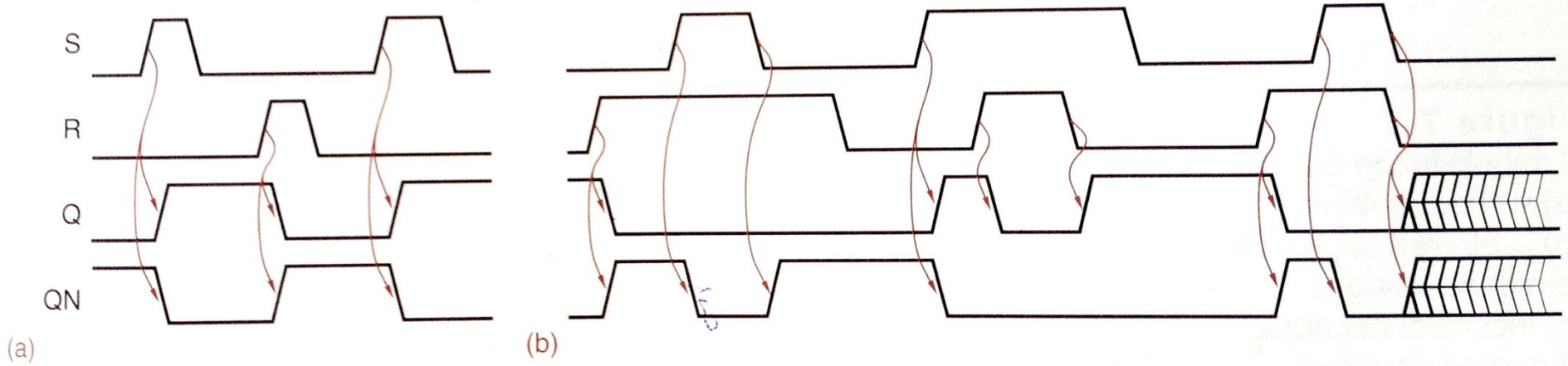
S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

Figure 7-5
S-R latch: (a) circuit design using NOR gates; (b) function table.

Typical operation

- *Metastable region*: when the output is unpredictable

Figure 7-6 Typical operation of an S-R latch: (a) "normal" inputs; (b) S and R asserted simultaneously.



- *Propagation delay*: time need for an input signal change to generate an output signal change
- *Recovery time*: giving the minimum separation between S and R as to be not simultaneous

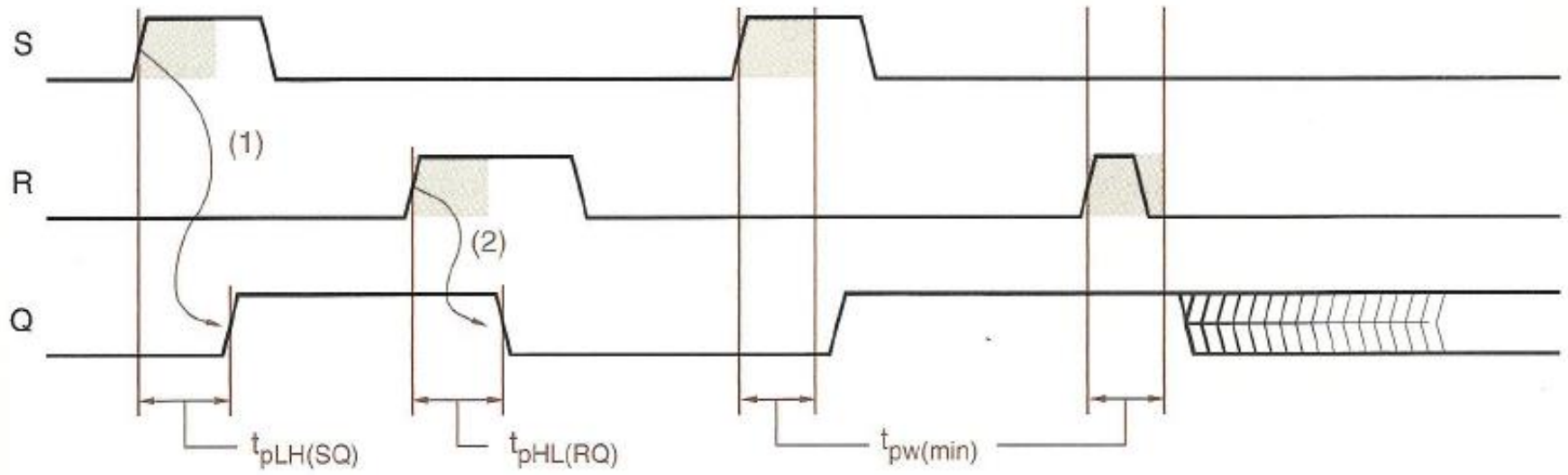


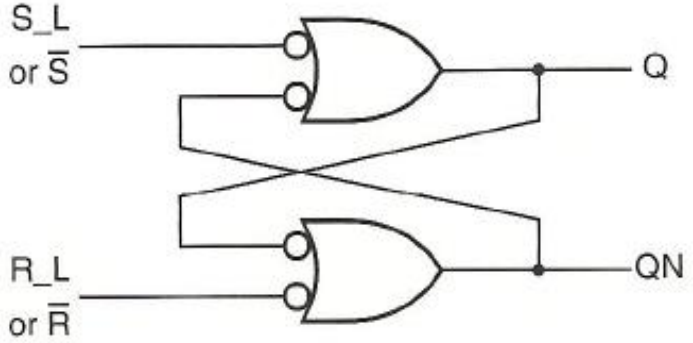
Figure 7-8 Timing parameters for an S-R latch.

$\overline{S}$-$\overline{R}$ latches

- S' and R' are active low, therefore opposite operation

Figure 7-9 $\overline{S}$-$\overline{R}$ latch: (a) circuit design using NAND gates; (b) function table; (c) logic symbol.

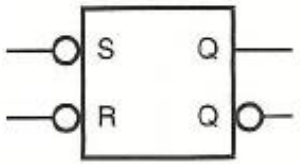
(a)



(b)

S_L	R_L	Q	QN
0	0	1	1
0	1	1	0
1	0	0	1
1	1	last Q	last QN

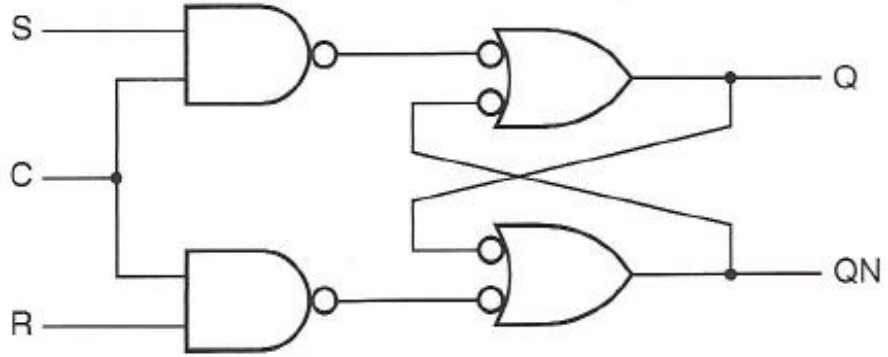
(c)



$\overline{S}$-$\overline{R}$ latch with enable

- Why? To control when the inputs are active

(a)



(b)

S	R	C	Q	QN
0	0	1	last Q	last QN
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
x	x	0	last Q	last QN

(c)

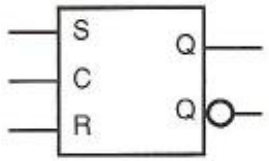
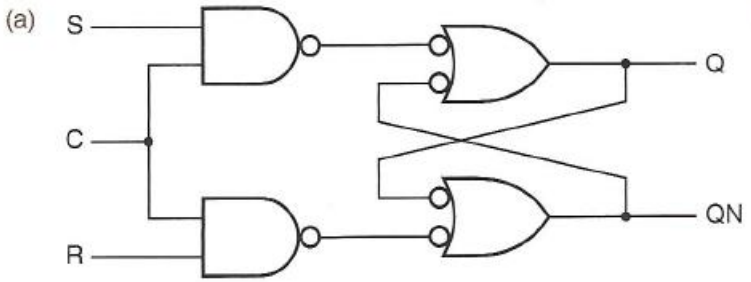


Figure 7-10 S-R latch with enable: (a) circuit using NAND gates; (b) function table; (c) logic symbol.

Typical operation



(b)

S	R	C	Q	QN
0	0	1	last Q	last QN
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
x	x	0	last Q	last QN

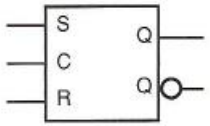
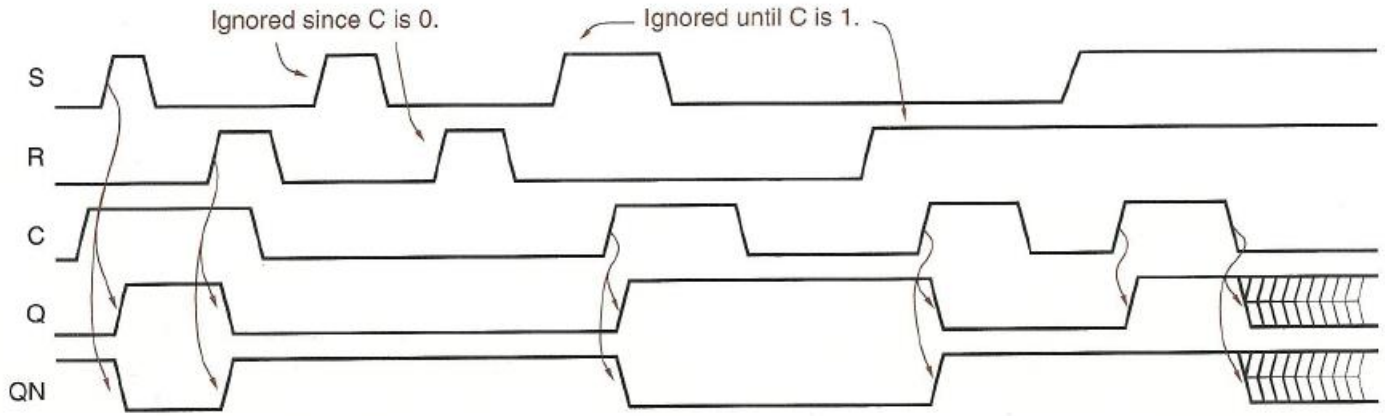
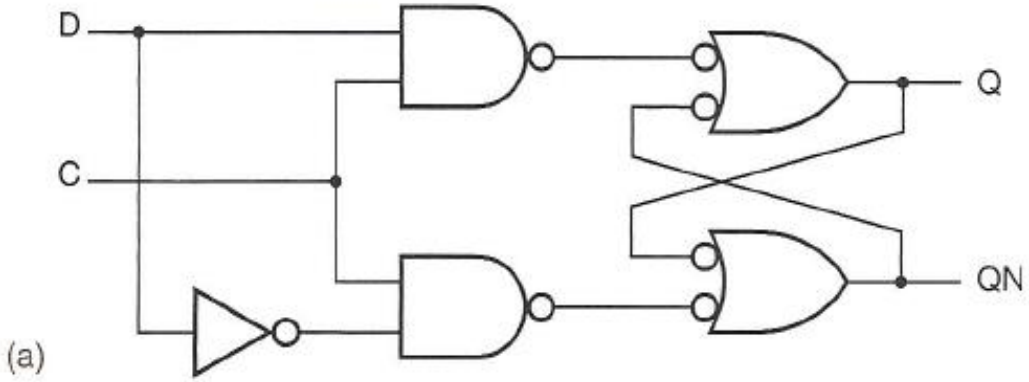


Figure 7-10 S-R latch with enable: (a) circuit using NAND gates; (b) function table; (c) logic symbol.

Figure 7-11 Typical operation of an S-R latch with enable.

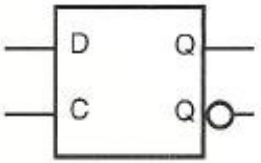


D-latches



C	D	Q	QN
1	0	0	1
1	1	1	0
0	x	last Q	last QN

(b)



(c)

Figure 7-12 D latch: (a) circuit design using NAND gates; (b) function table; (c) logic symbol.

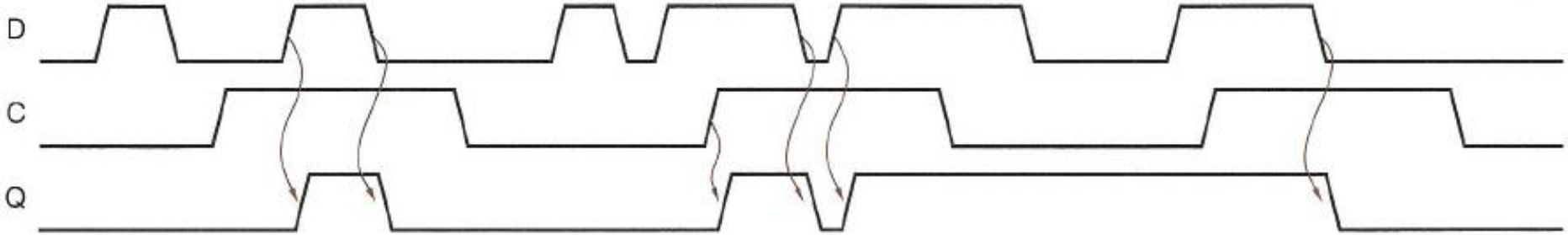
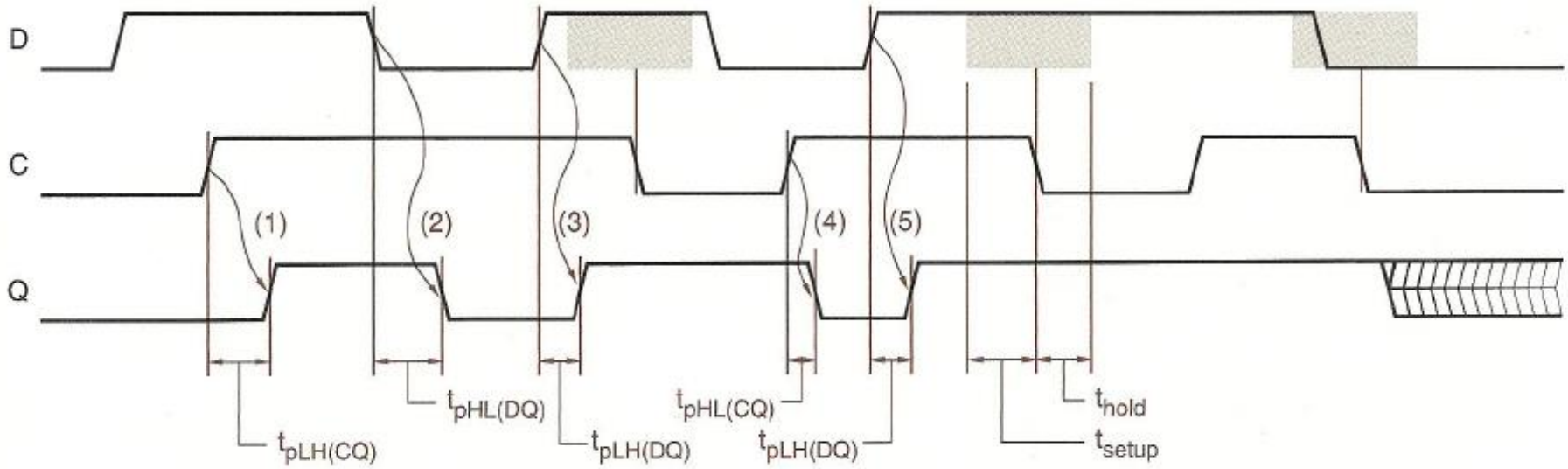


Figure 7-13 Functional behavior of a D latch for various inputs.

Timing parameters

Figure 7-14 Timing parameters for a D latch.

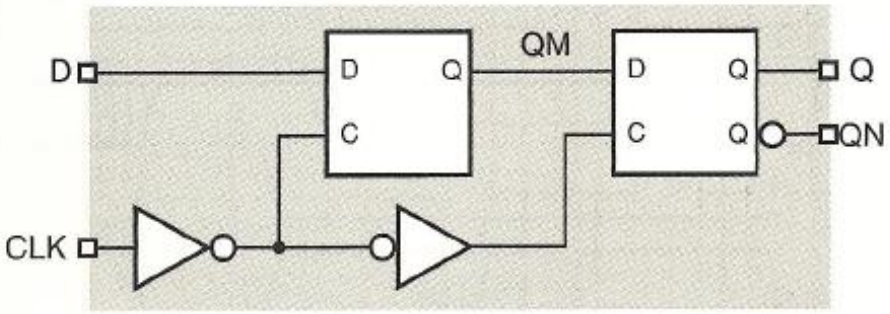


Edge triggered D Flip Flop

- **Clk**: dynamic input indicator – edge triggered behavior

Figure 7-15 Positive-edge-triggered D flip-flop: (a) circuit design using D latches; (b) function table; (c) logic symbol.

(a)



(b)

D	CLK	Q	QN
0	↑	0	1
1	↑	1	0
x	0	last Q	last QN
x	1	last Q	last QN

(c)

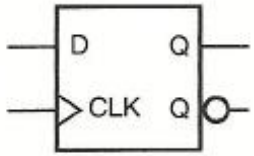
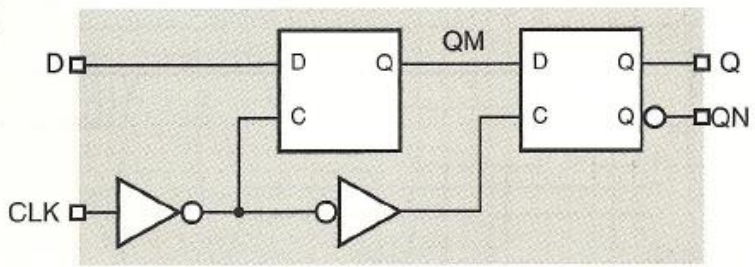


Figure 7-15 Positive-edge-triggered D flip-flop: (a) circuit design using D latches; (b) function table; (c) logic symbol.

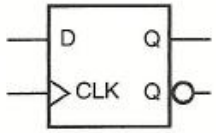
(a)



(b)

D	CLK	Q	QN
0	↑	0	1
1	↑	1	0
x	0	last Q	last QN
x	1	last Q	last QN

(c)



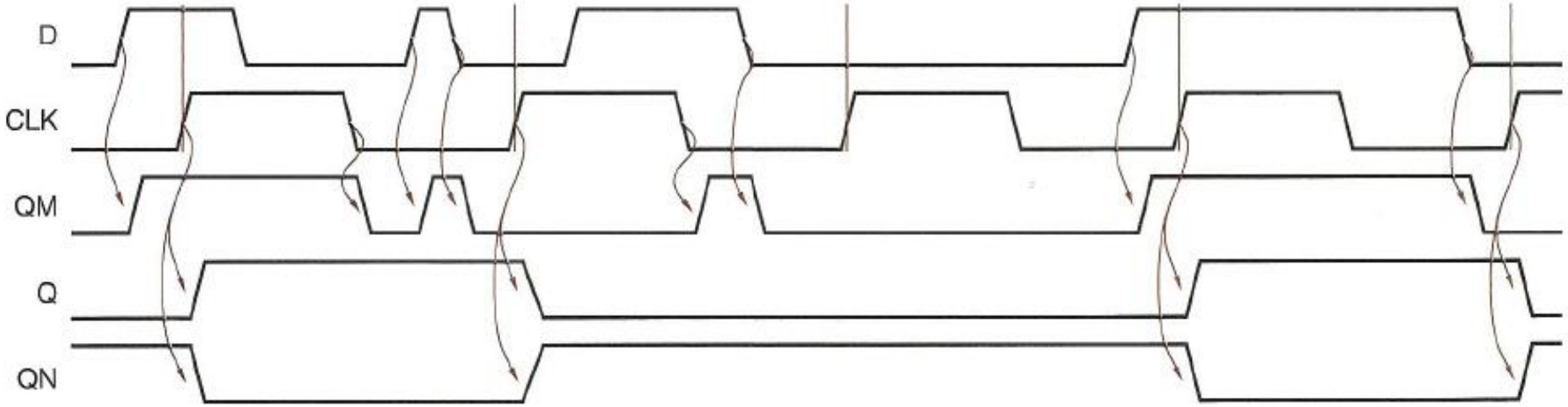
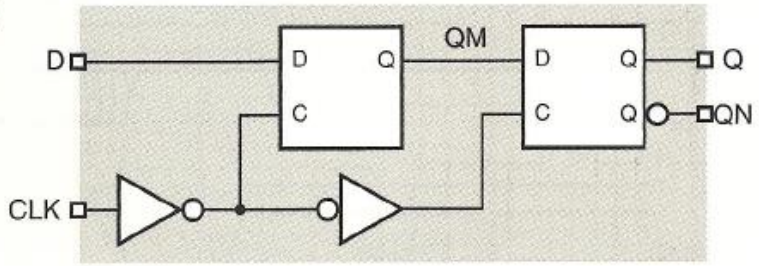


Figure 7-16 Functional behavior of a positive-edge-triggered D flip-flop.

Figure 7-15 Positive-edge-triggered D flip-flop: (a) circuit design using D latches; (b) function table; (c) logic symbol.

(a)



(b)

D	CLK	Q	QN
0	↑	0	1
1	↑	1	0
x	0	last Q	last QN
x	1	last Q	last QN

(c)

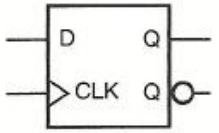
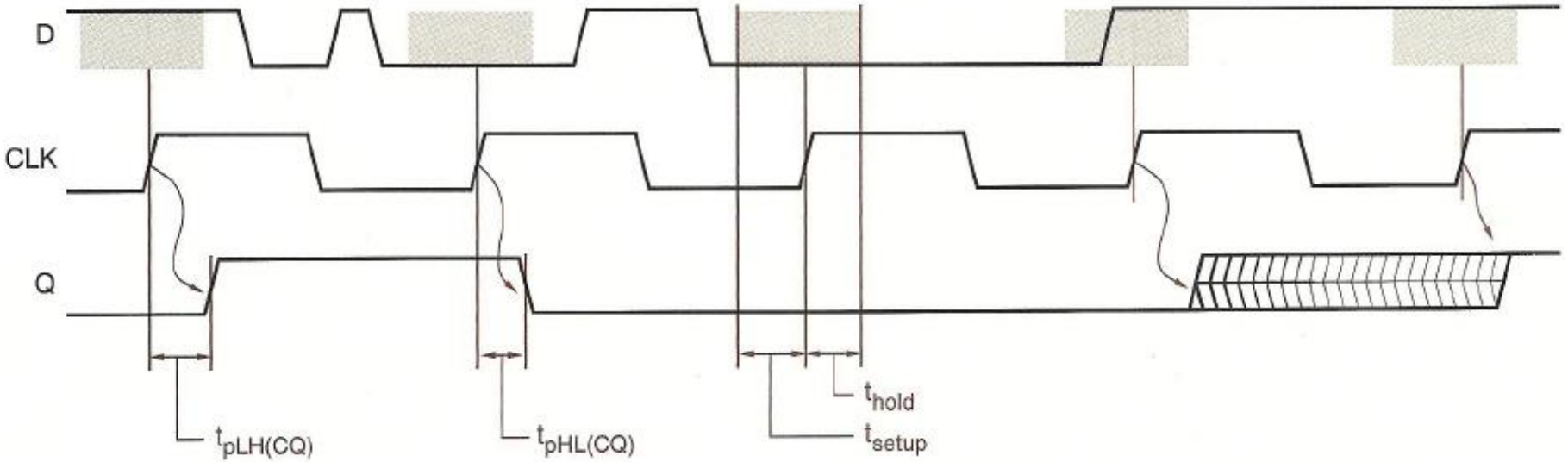
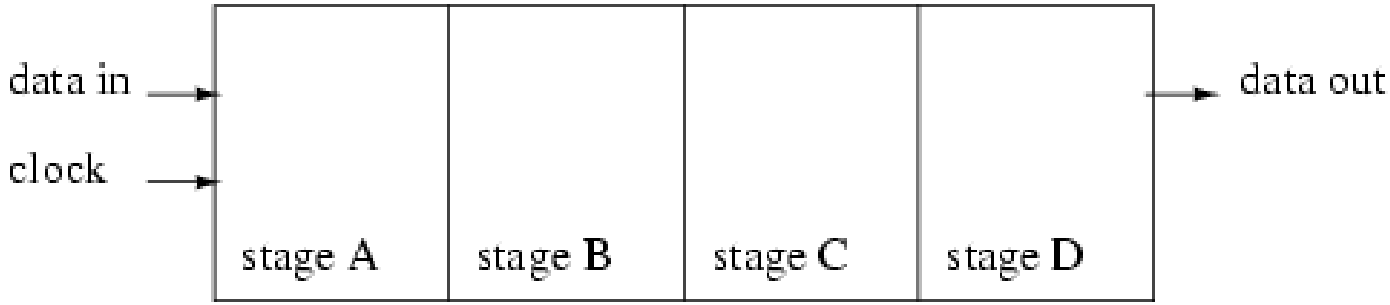


Figure 7-17 Timing behavior of a positive-edge-triggered D flip-flop.



Shift registers

- They produce a discrete delay for a specific digital signal. The delay is given by “n” stages.
- Conveyor belt similarity



Serial-in, serial-out shift register with 4-stages

Shift registers

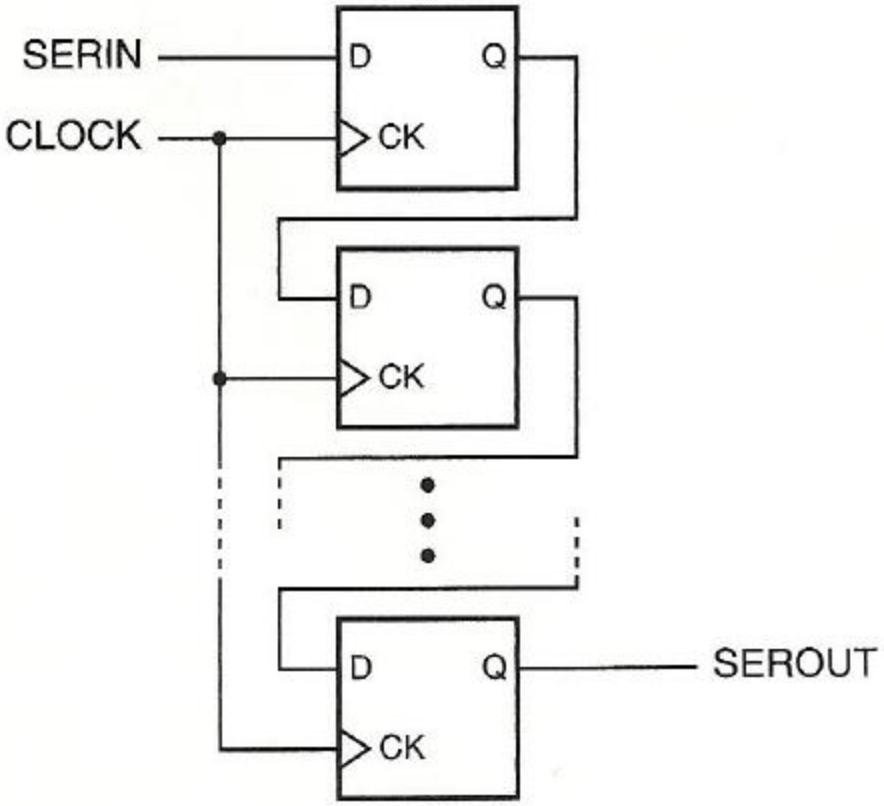
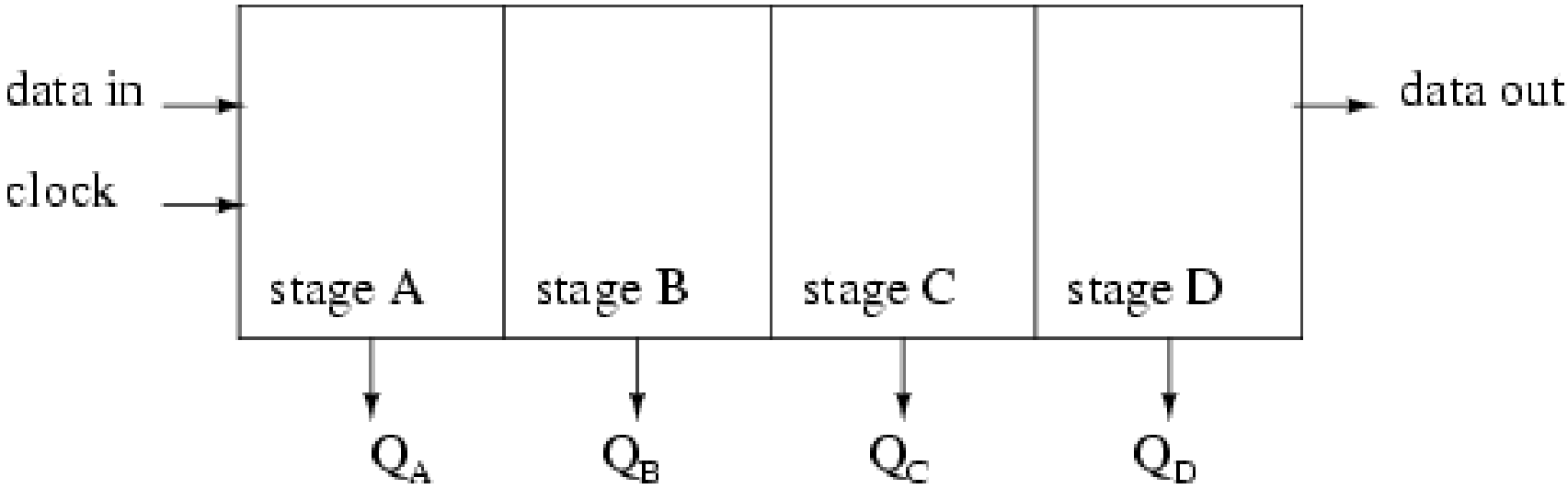


Figure 8-37
Structure of a serial-in, serial-out shift register.

Serial – in, parallel - out



Serial-in, parallel-out shift register with 4-stages

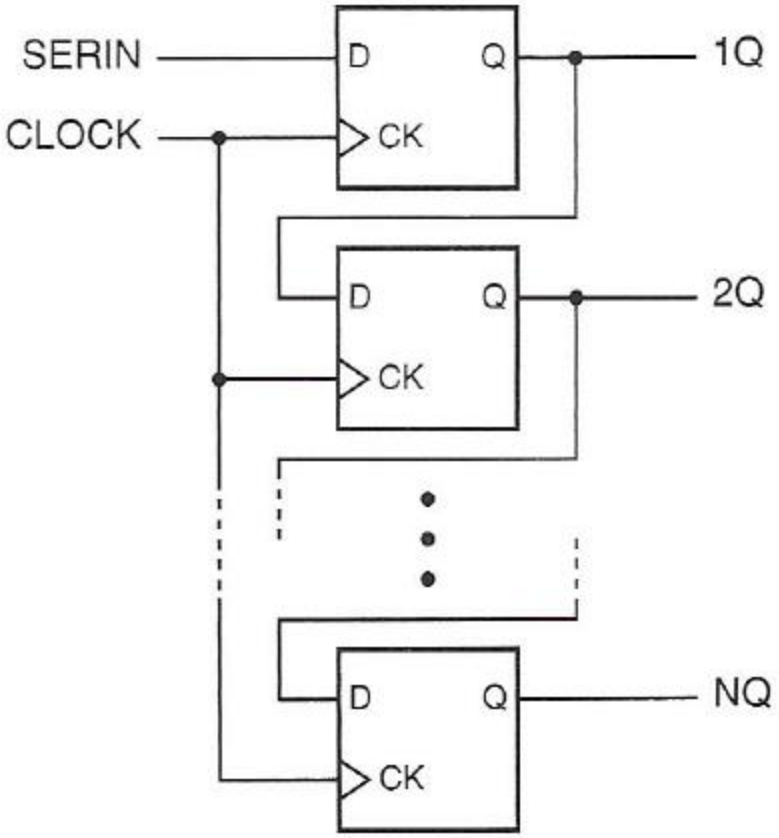
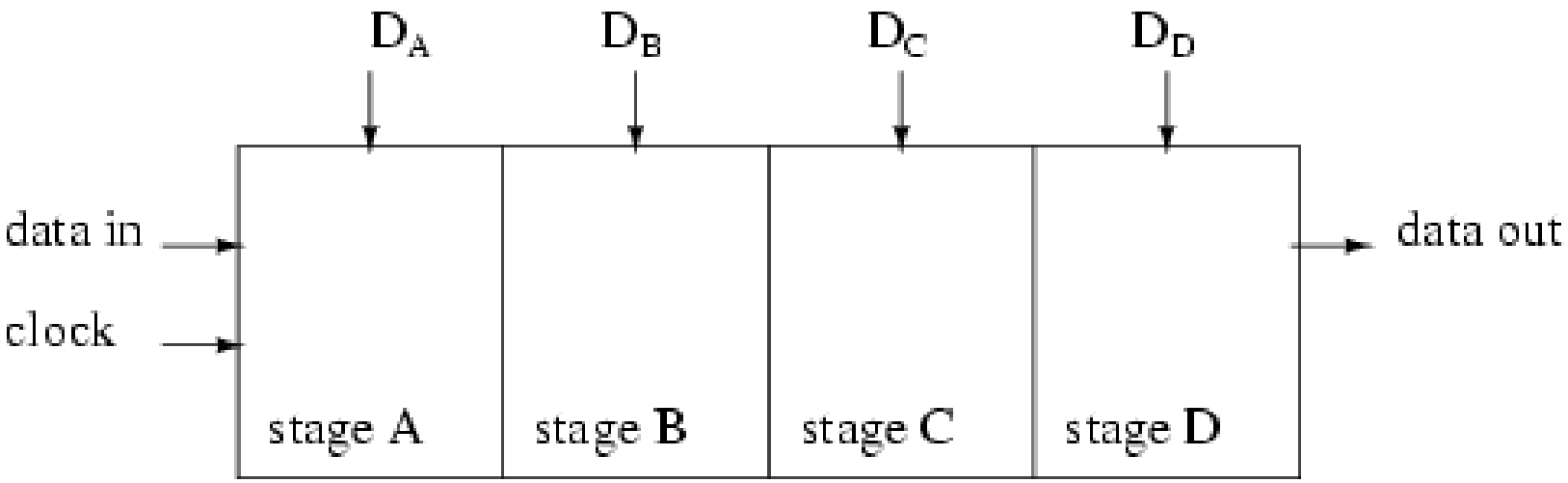


Figure 8-38
Structure of a serial-in, parallel-out shift register.

Parallel - in, serial - out



Parallel-in, serial-out shift register with 4-stages

Parallel - in, serial - out

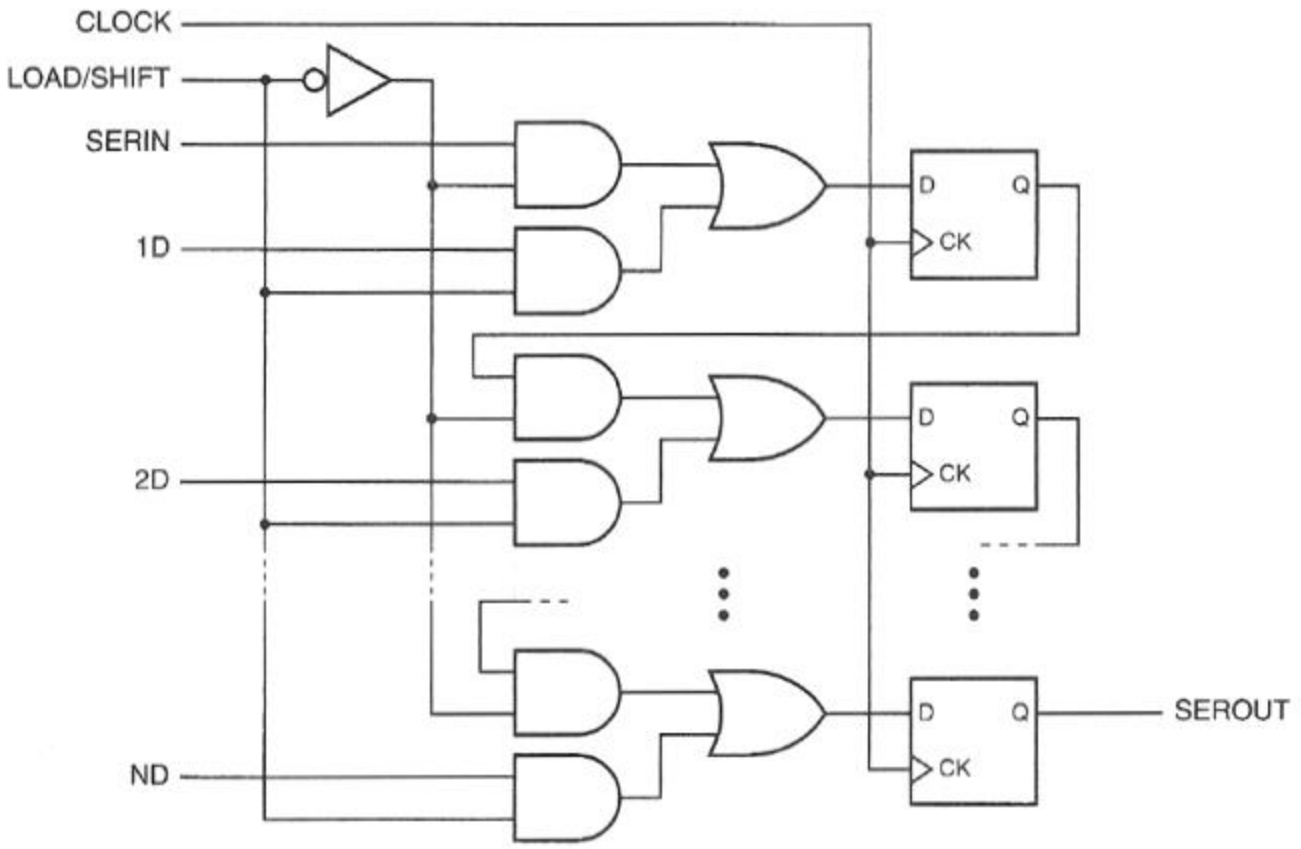
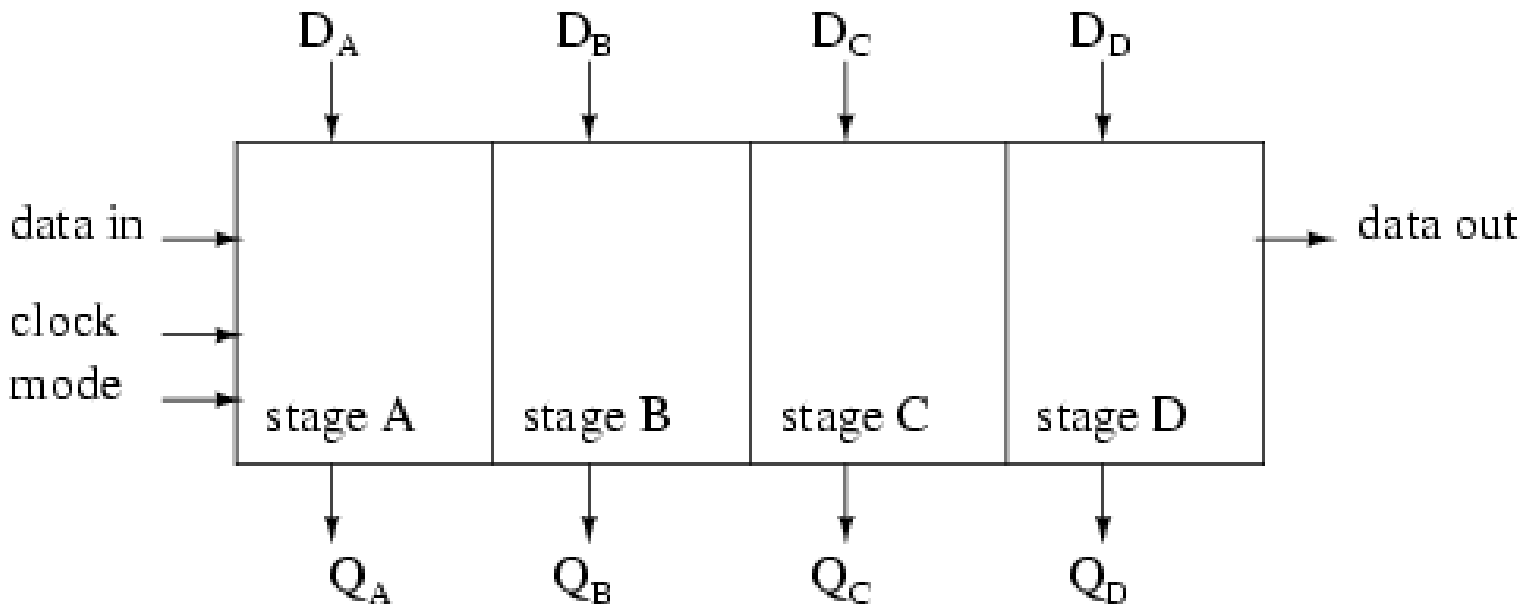


Figure 8-39 Structure of a parallel-in, serial-out shift register.

Parallel – in, parallel - out



Parallel-in, parallel-out shift register with 4-stages

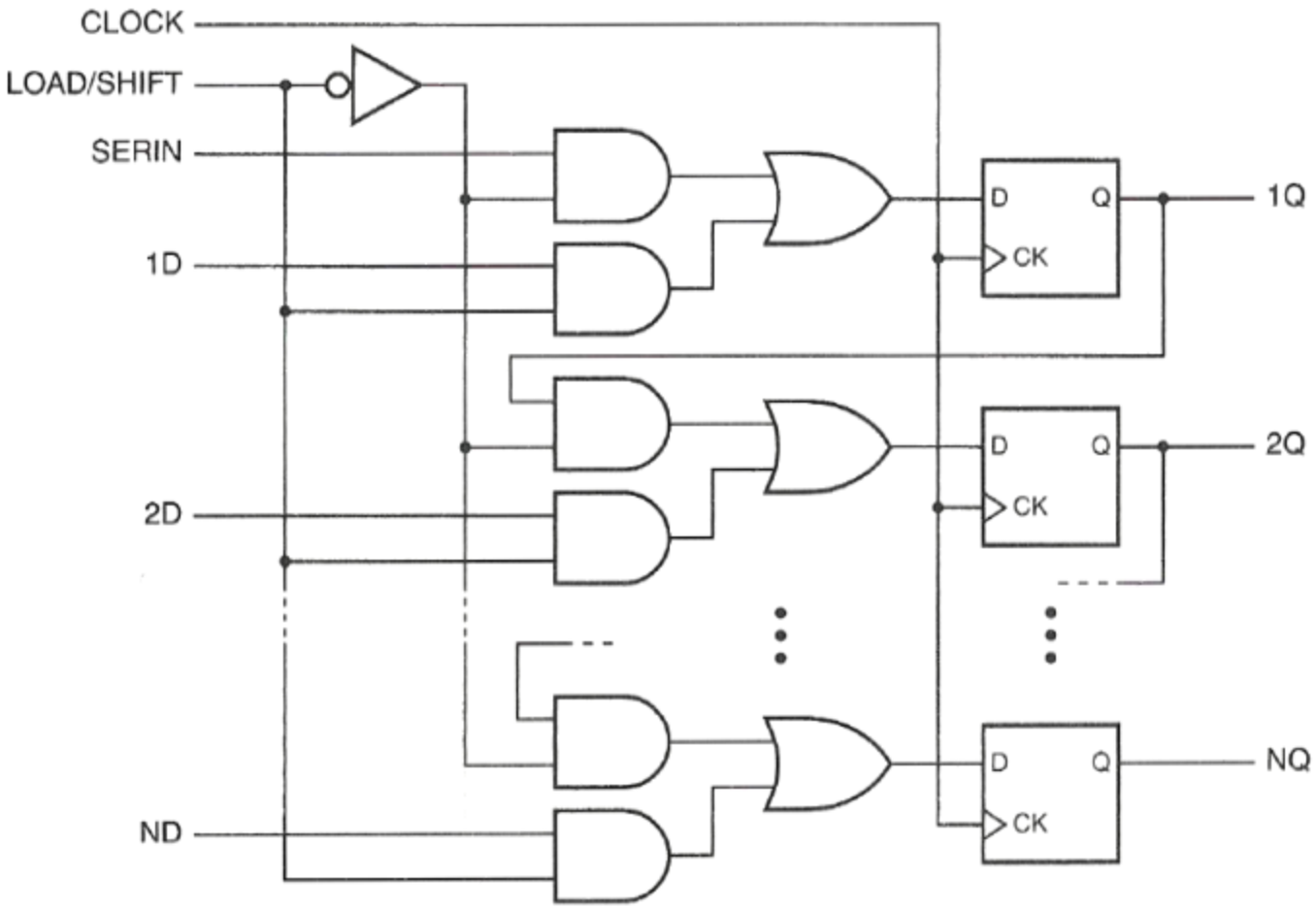


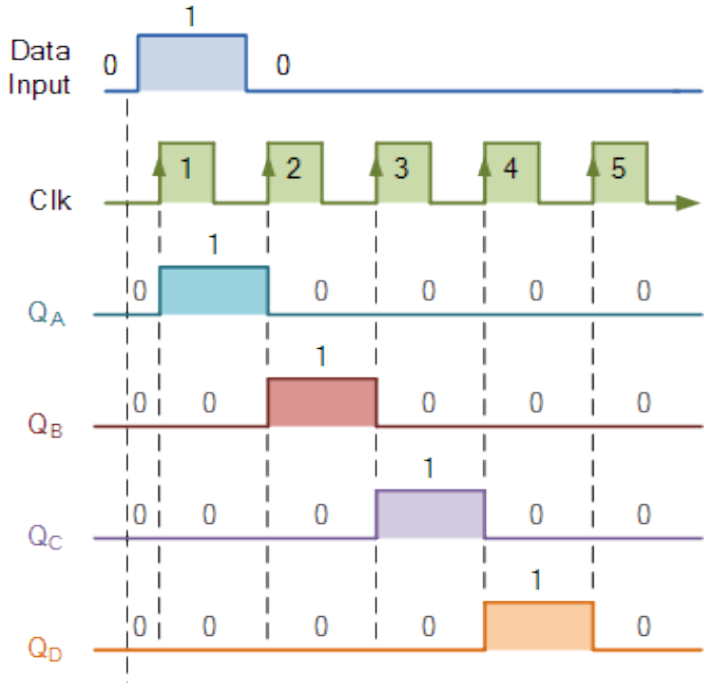
Figure 8-40 Structure of a parallel-in, parallel-out shift register.

Example: 74x194, 4 bit shift register

Table 8-24
Function table for the 74x194 4-bit universal shift register.

Function	Inputs S1	Inputs S0	Next state QA*	Next state QB*	Next state QC*	Next state QD*
Hold	0	0	QA	QB	QC	QD
Shift right	0	1	RIN	QA	QB	QC
Shift left	1	0	QB	QC	QD	LIN
Load	1	1	A	B	C	D

Example:
S1:0
S0:1



- Example

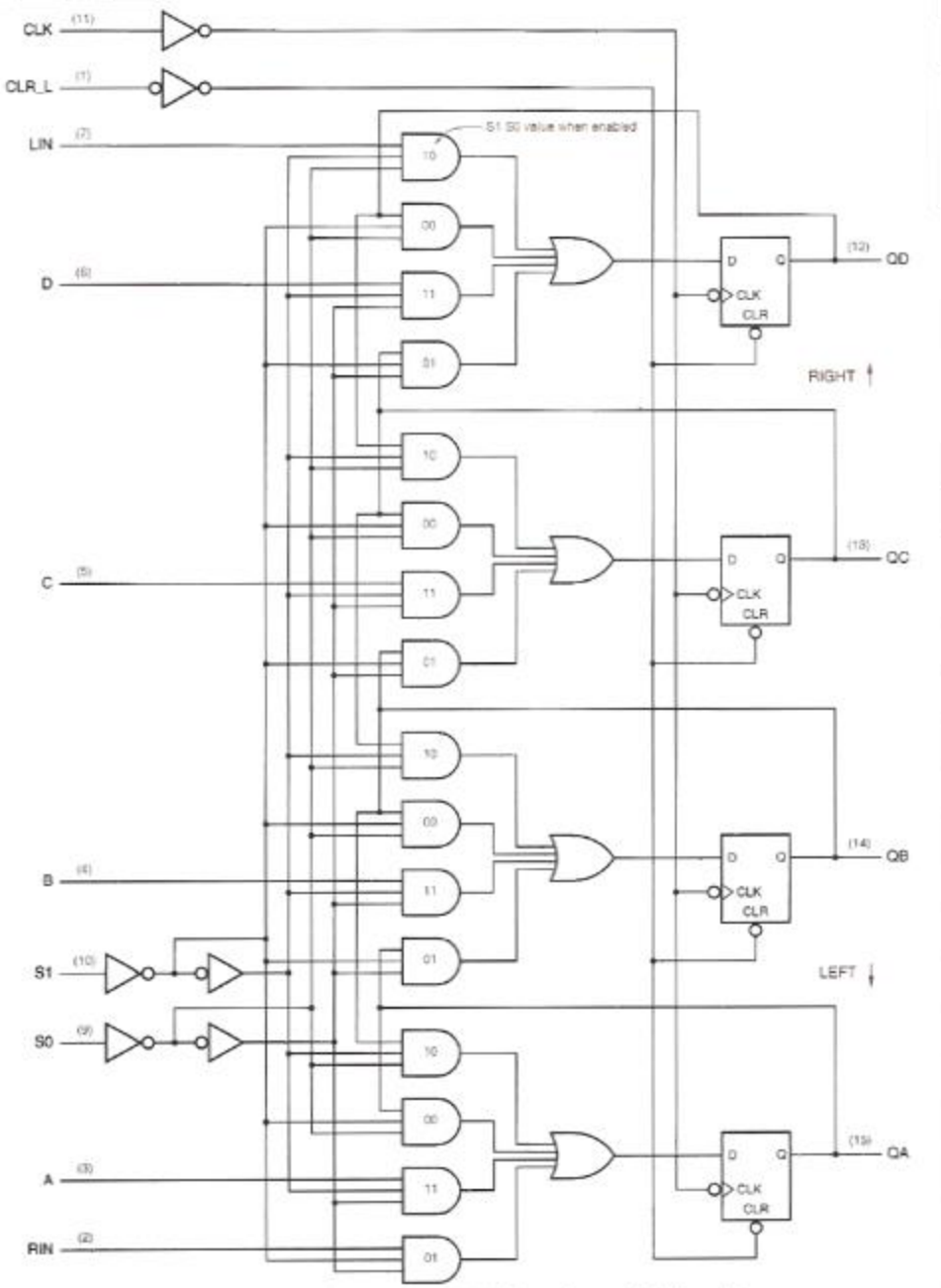


Figure 8-41 Logic diagram for the 74x194 4-bit universal shift register, including pin numbers for a standard 16-pin dual in-line package.