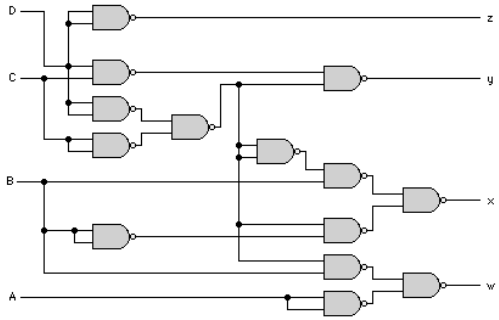
Embedded Systems Design, Spring 2025

Lecture 1



Combinational Logic Design Principles

About this course

- EMB2 – continuation of EMB1, stand alone course, 5 ECTS
- 8 Practice Assignments (not compulsory)
  - 8 during the semester (individual/groups of two) + 1 which is optional
  - You will get feedback on the 8 assignments: correct solutions (from your hand-ins)
- End of teaching period: A theory test for extra bonus points (10%)
- In June: written exam, 3 hours (theory + practical part)
- Structure of the course/topics may be adjusted during the semester, please follow itslearning for changes in schedule

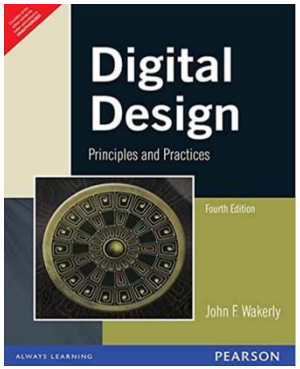
Course schedule

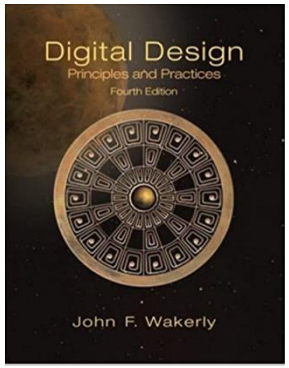
- Theory + labs (check schedule in itslearning)
- Theory sessions will be on :
  - Friday (MC) /
  - Thursday noon (EL + EIB)
- Support videos and tutorials in itslearning
- Labs will either be exercises or practical implementation
  - Designated rooms + use of the e-labs (Alsion e-lab, CIE e-lab)

- The first part of the semester will focus more on theory
- The second part of the semester will focus more on practice

Contents

- Logic components
- Boolean algebra
- Latches and flip-flops
- State machines





Book: Digital Design: Principles and Practices 4th Edition,
by John F. Wakerly (Author)

- Microcontroller hardware
- Peripherals / Serial communication
- Interrupts
- AD/DA conversion

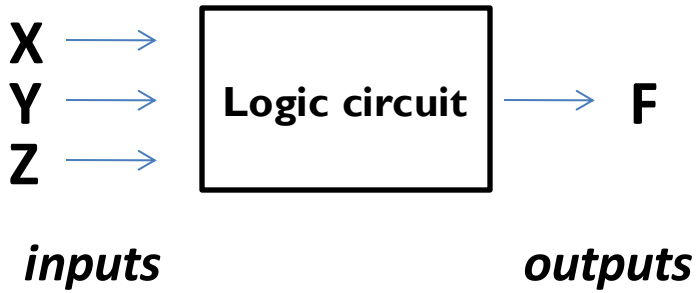
Entering the digital world

- We live in an analog world
- Digital logic – mapping the infinite set of real values to 0 and 1
- When talking about real circuits: 0 – **low**, 1 – **high**
- Noise immunity
- Buffer circuits

Physical states in various cases

Technology	0	1
Pneumatic logic	Low pressure	High pressure
Relay logic	Circuit open	Circuit closed
CMOS logic	0 - 1.5 V	3.5 - 5.0 V
TTL	0 – 0.8 V	2.0 – 5.0 V
Dynamic memory	Capacitor discharged	Capacitor charged
Erasable memory	Electrons trapped	Electrons released
Microprocessor on-chip	Fuse blown	Fuse intact
Fiber optics	Light off	Light on
Magnetic tape	Flux direction north	Flux direction south
CD	No pit	Pit
CD – R	Dye in crystalline state	Dye in noncrystalline state

Types of logic circuits

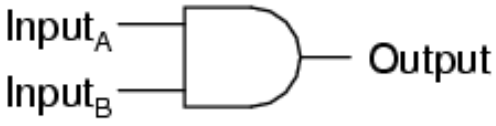


Combinational circuit: output depends on the input,
operation described by a truth table.

Sequential circuit: output depends on input and previous inputs,
operation described by a state table.

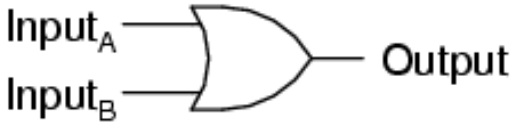
Basic logic functions

2-input AND gate



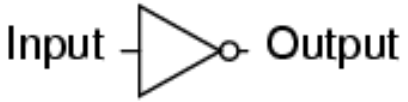
A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

2-input OR gate



A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

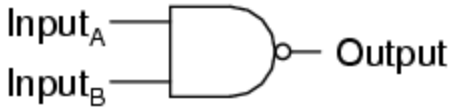
NOT gate truth table



Input	Output
0	1
1	0

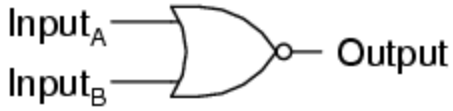
NAND, NOR

2-input NAND gate



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

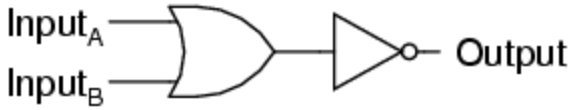
2-input NOR gate



A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Equivalent gate circuit

Equivalent gate circuit



Logic families

- 1930: Bell Labs – relays
- 1940: Eniac – 18 000 vacuum tubes
- 1950 – 1960 – invention of the IC
- 1960 – Transistor - Transistor Logic (TTL, based bipolar transistors)
- 1960 – Metal-oxide semiconductor field effect (lower power consumption, slower)
- 1980 – Complementary MOS (CMOS) – increase in performance

CMOS Logic

Logic levels

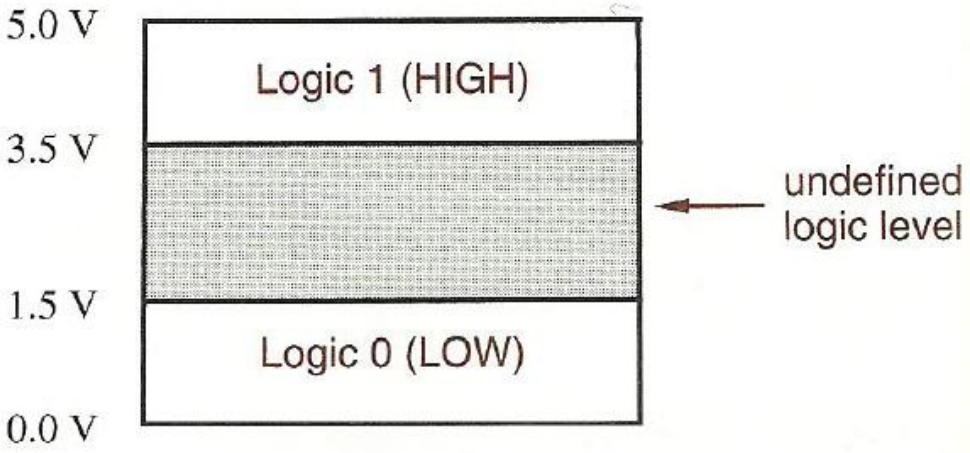
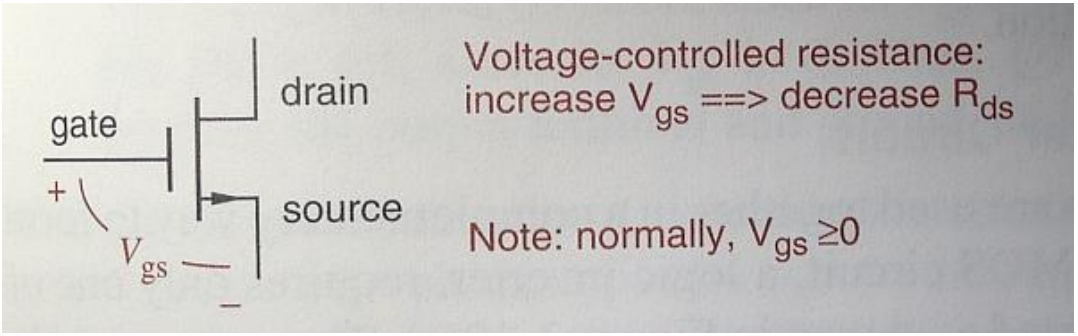


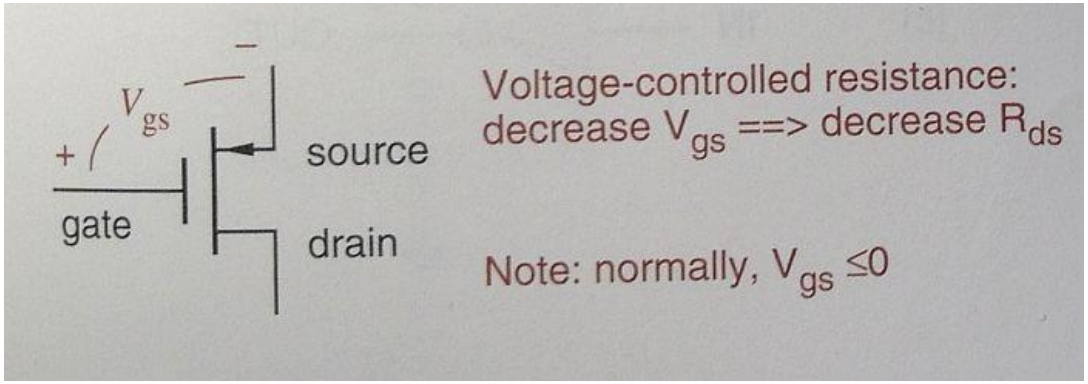
Figure 3-6
Logic levels for typical CMOS logic circuits.

pMOS, nMOS

nMOS



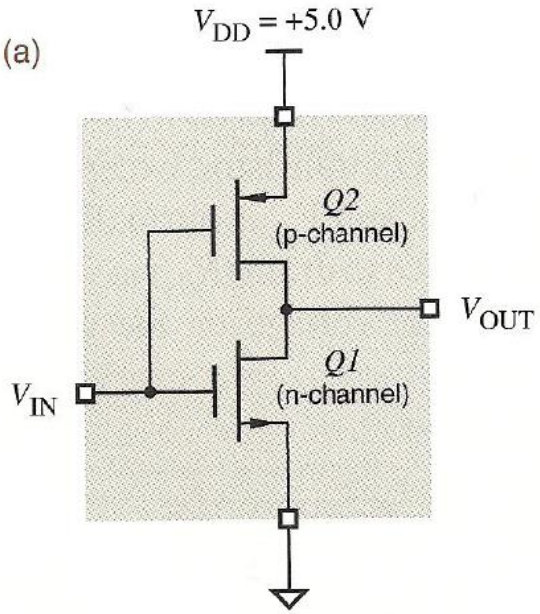
pMOS



CMOS Inverter

Figure 3-10
CMOS inverter:
(a) circuit diagram;
(b) functional behavior;
(c) logic symbol.

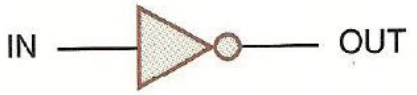
(a)



(b)

V_{IN}	Q1	Q2	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

(c)



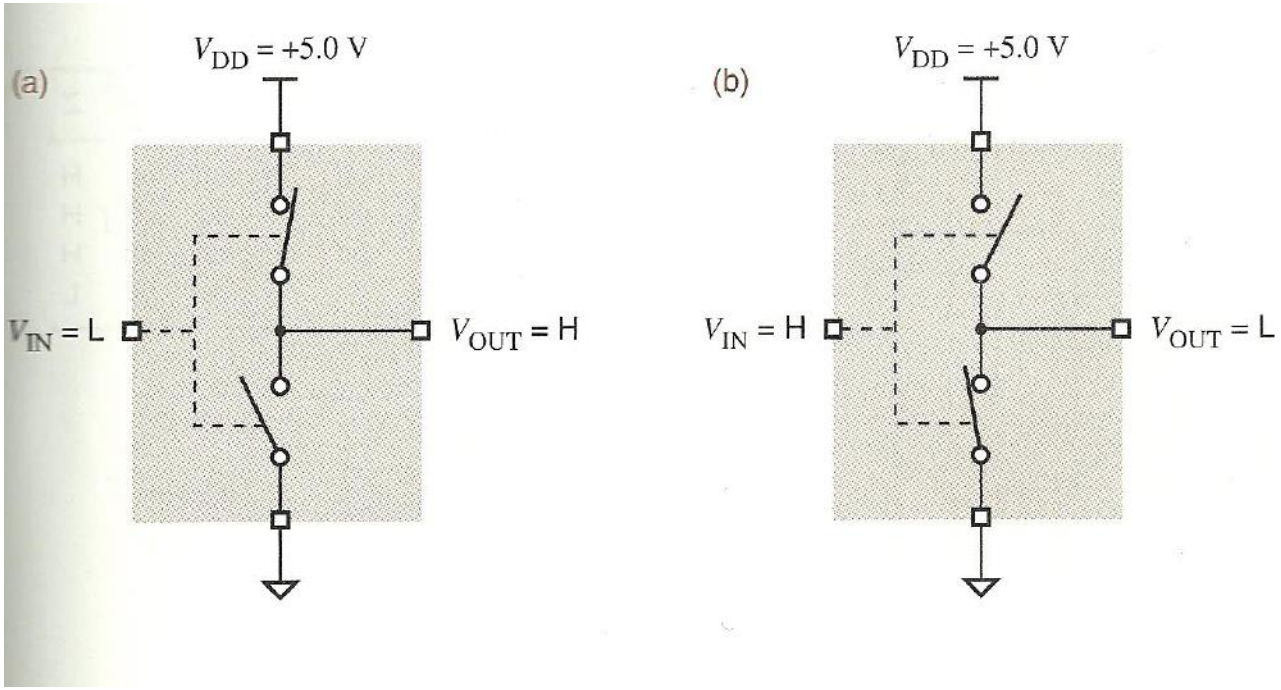


Figure 3-11
Switch model for CMOS inverter: (a) LOW input; (b) HIGH input.

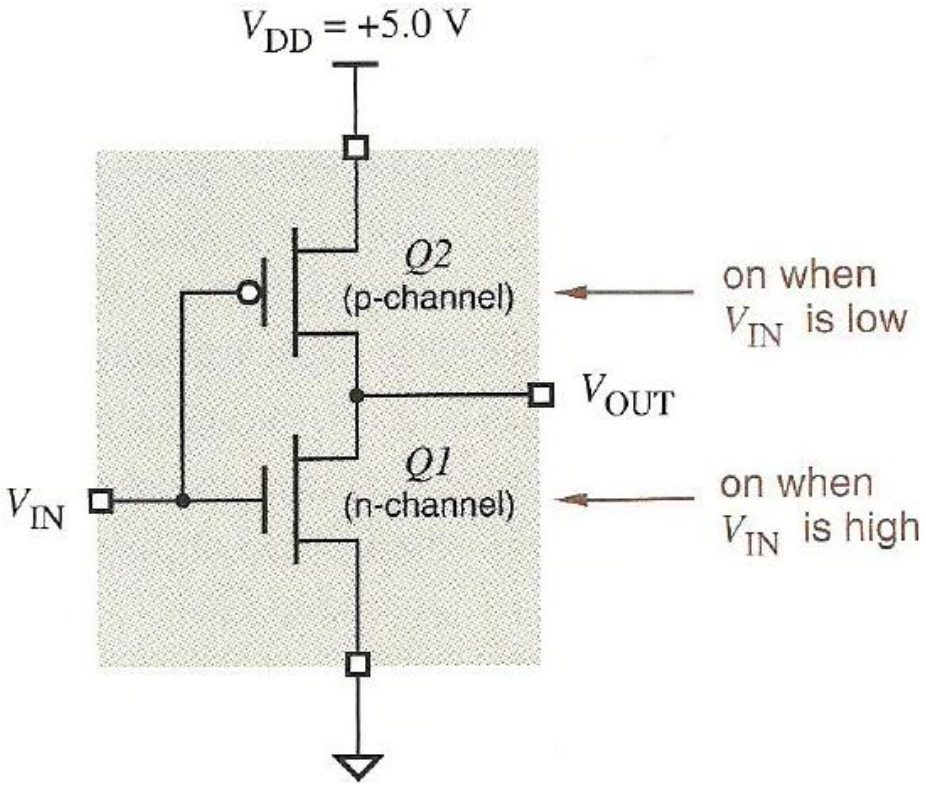
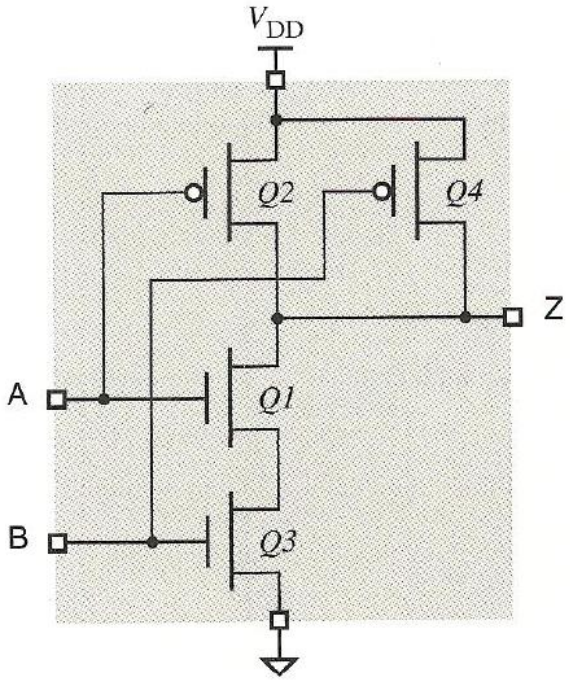


Figure 3-12
CMOS inverter logical operation.

Figure 3-13
CMOS 2-input NAND gate:
(a) circuit diagram;
(b) function table;
(c) logic symbol.

(a)



(b)

A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L

(c)

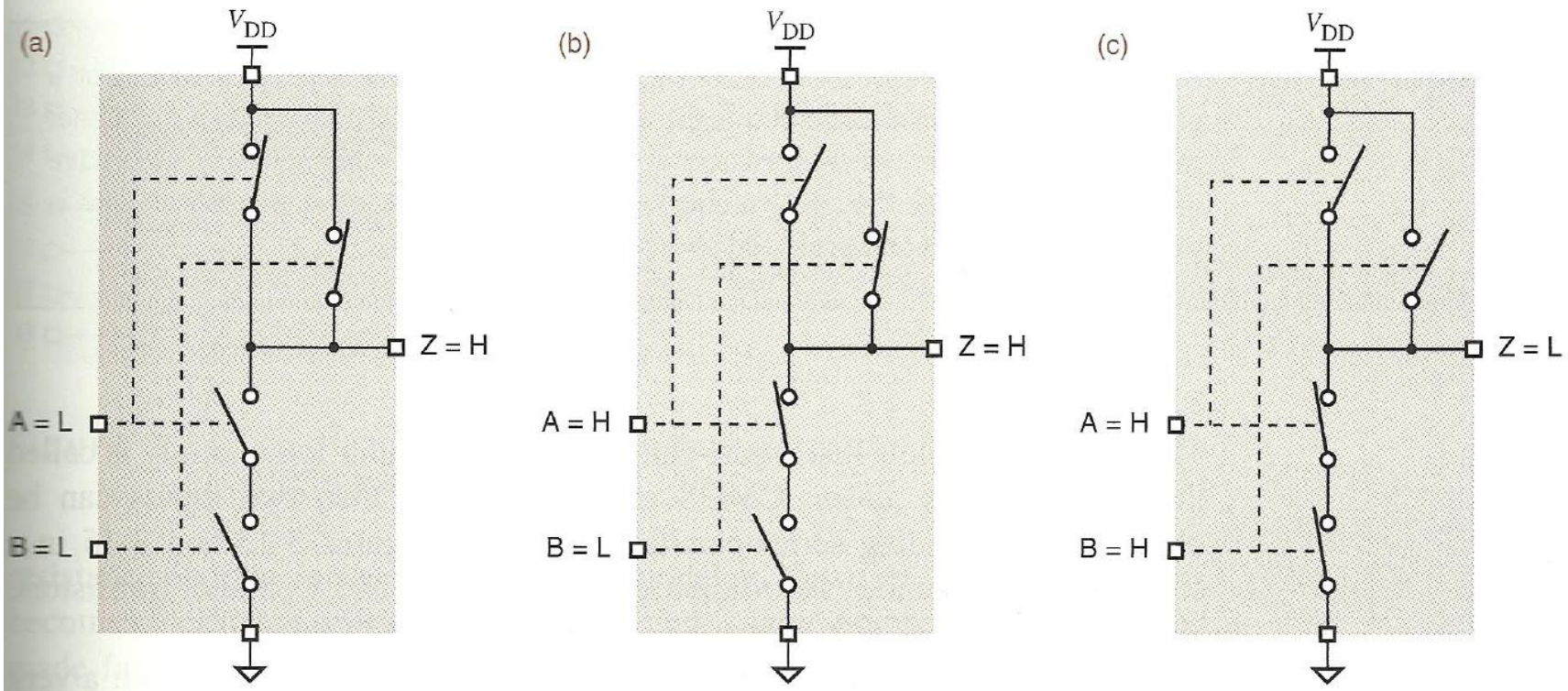
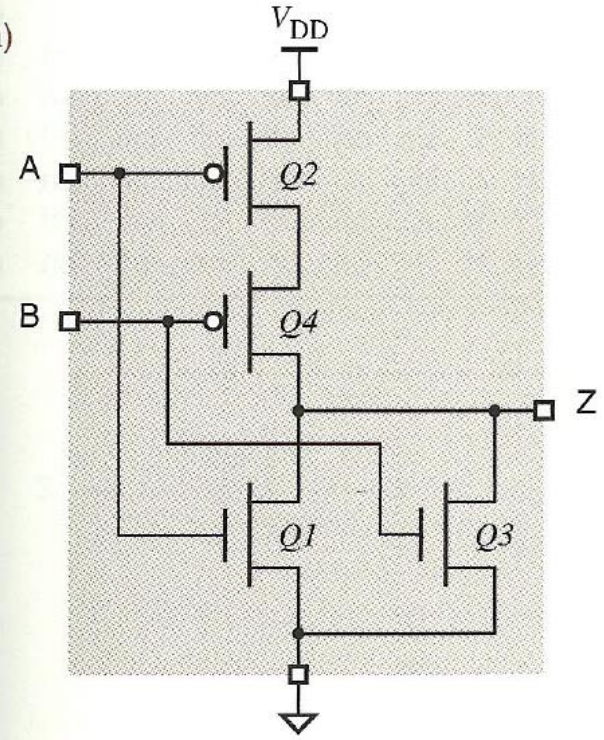


Figure 3-14 Switch model for CMOS 2-input NAND gate: (a) both inputs LOW; (b) one input HIGH; (c) both inputs HIGH.

(a)



(b)

A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

(c)

Figure 3-15
CMOS 2-input NOR gate:
(a) circuit diagram;
(b) function table;
(c) logic symbol.

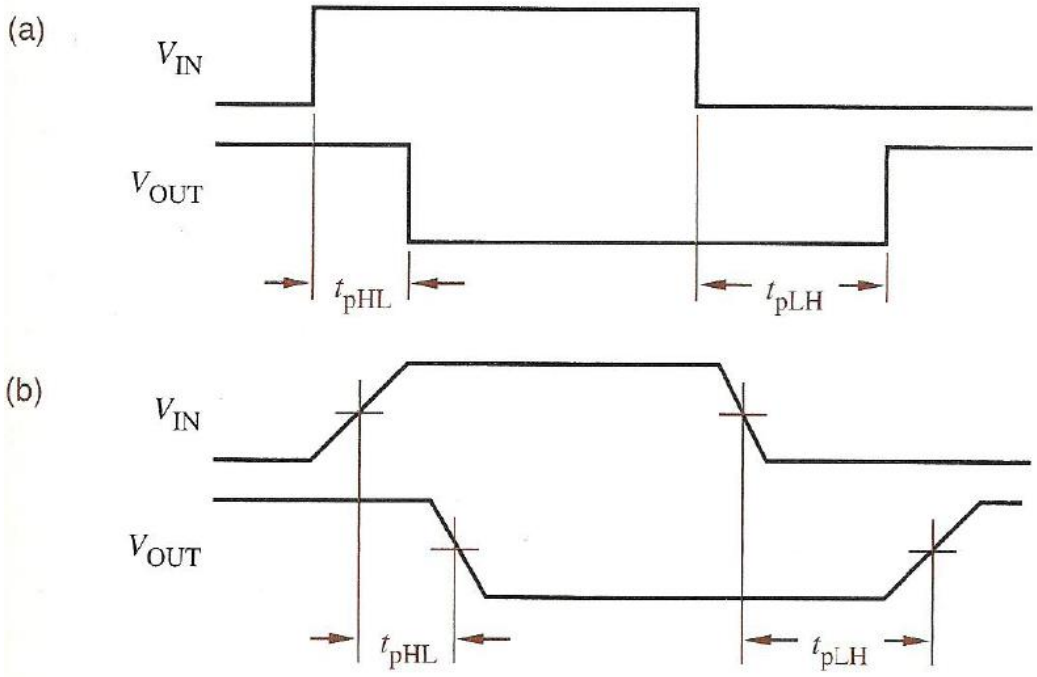


Figure 3-42
Propagation delays for a CMOS inverter: (a) ignoring rise and fall times; (b) measured at midpoints of transitions.

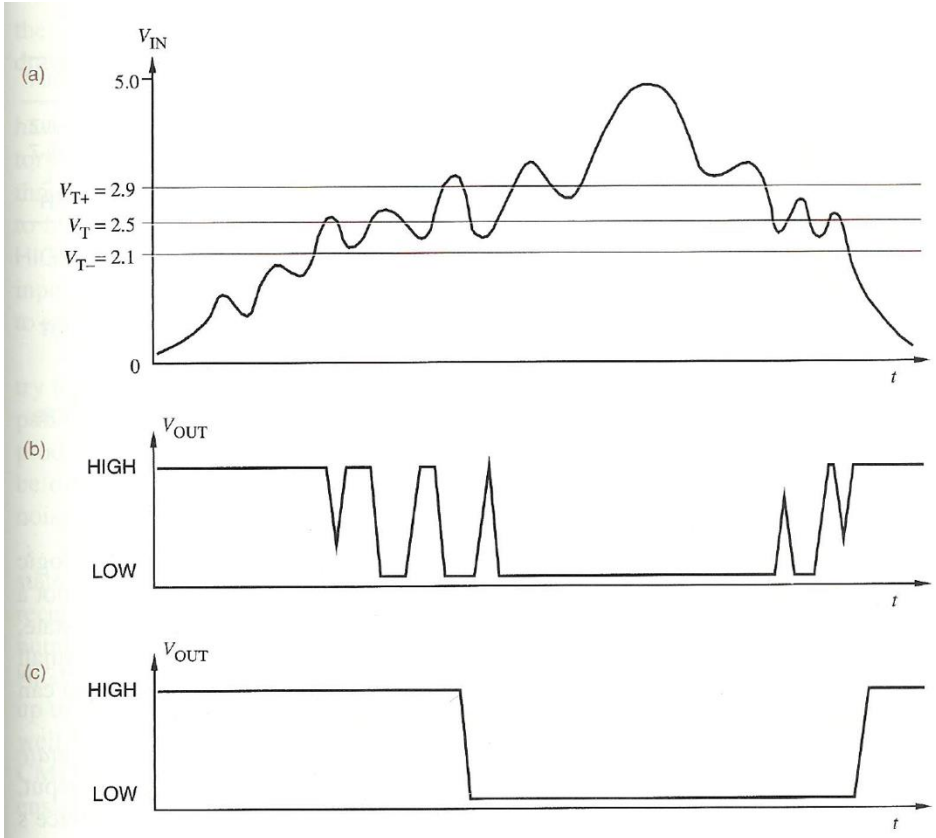
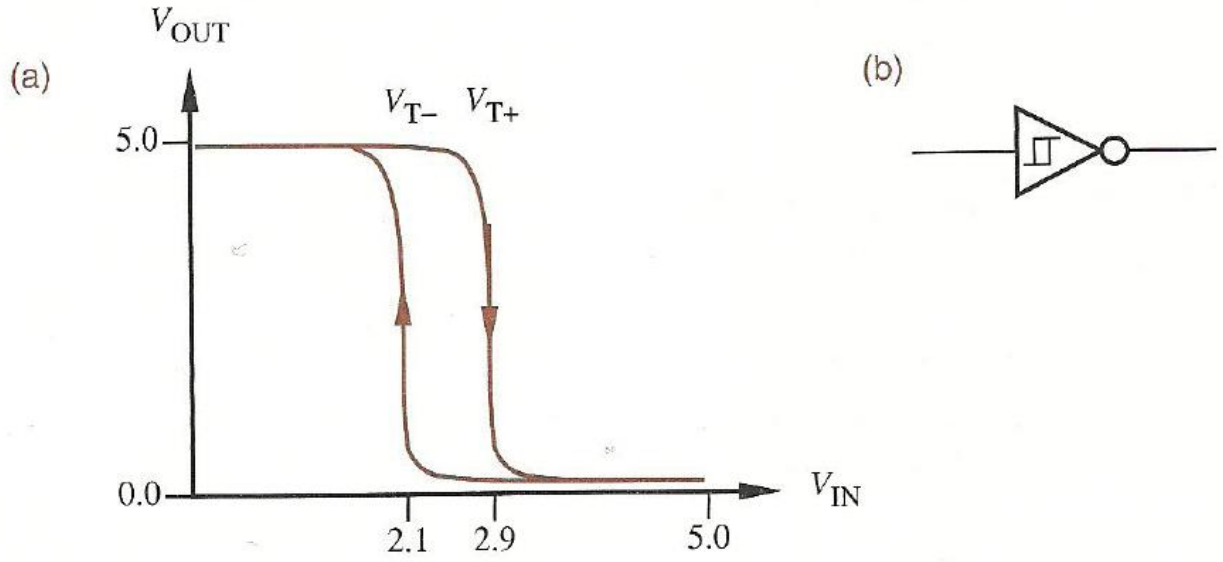


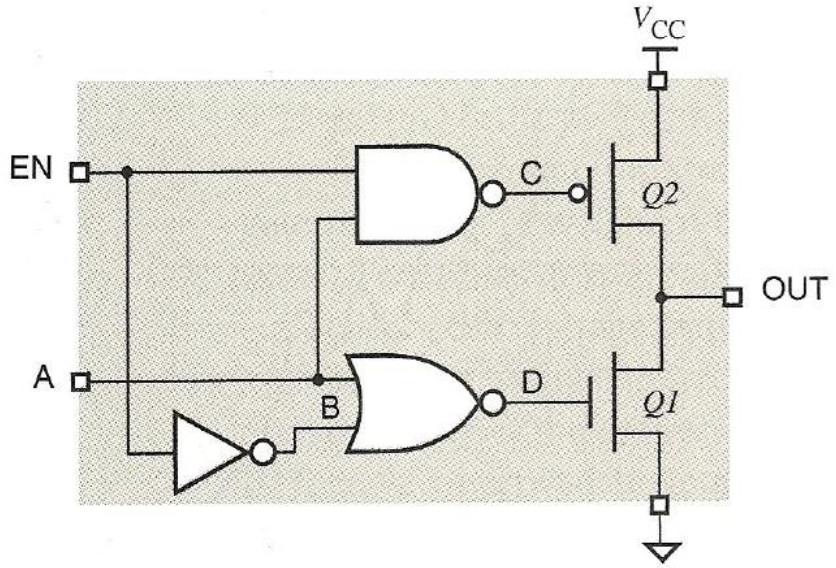
Figure 3-48 Device operation with slowly changing inputs: (a) a noisy, slowly changing input; (b) output produced by an ordinary inverter; (c) output produced by an inverter with 0.8 V of hysteresis.

Figure 3-47
A Schmitt-trigger inverter: (a) input-output transfer characteristic; (b) logic symbol.



Three state outputs

(a)



(b)

EN	A	B	C	D	*Q1*	*Q2*	OUT
L	L	H	H	L	off	off	Hi-Z
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H

(c)

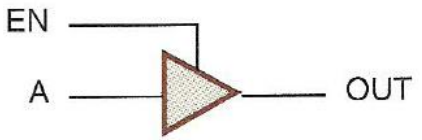
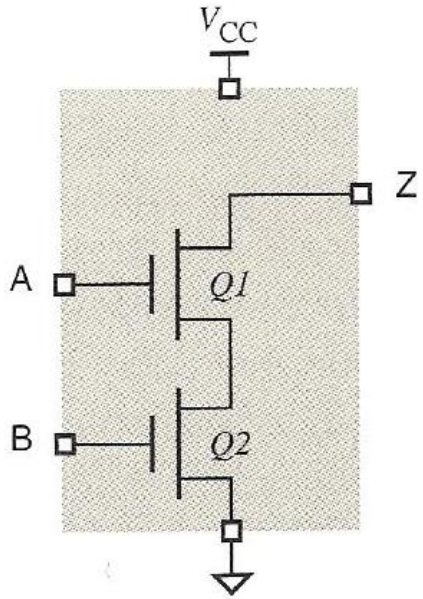


Figure 3-49 CMOS three-state buffer: (a) circuit diagram; (b) function table; (c) logic symbol.

Figure 3-50
Open-drain CMOS NAND gate: (a) circuit diagram; (b) function table; (c) logic symbol.

(a)



(b)

A	B	*Q1*	*Q2*	Z
L	L	off	off	open
L	H	off	on	open
H	L	on	off	open
H	H	on	on	L

(c)

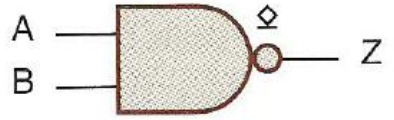
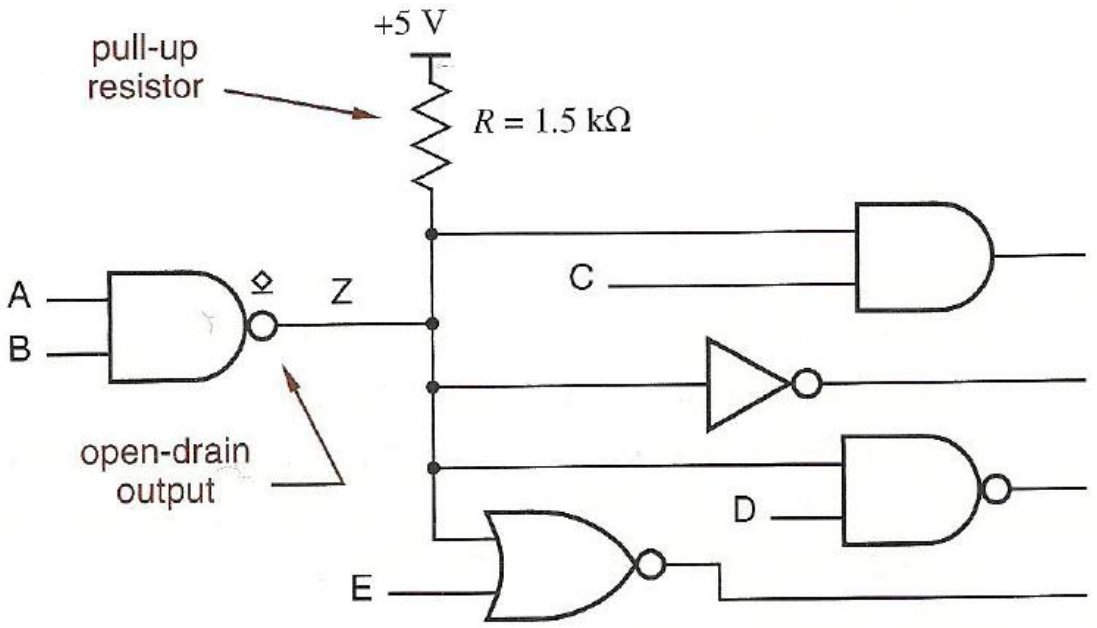


Figure 3-51
Open-drain CMOS NAND gate driving a load.



Exercises

- F = XY + X'Y'Z
- F = X + Y' + XYZ
- F = X'Y' + XY + Z'
- F = (X + Y'Z)' + X'YZ'