University of Cape Coast

College of Agriculture & Natural Sciences

School of Physical Sciences

Department of Computer Science & Information Technology

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CSC211: Computer Architecture

Duration: 2 hour

Answer all questions on the question paper.
Circle the most appropriate answer.
Only ONE attempt per question.

Registration Number:.....

1. A data type is:
   (a) a memory location containing an integer value.
   (b) the sign bit of a floating point representation.
   (c) a memory location containing a floating point value.
   (d) a representation of information for which an op-code exists that can operate on that representation.
2. Using DeMorgan's Theorem we can convert any AND-OR structure into
   (a) NOR-NAN
   (b) NAND-NOR
   (c) NAND-NAND
   (d) OR-NAND
3. In the FETCH phase, an instruction is transferred from ..... to the Instruction Register.
   (a) Processing Unit
   (b) Output device
   (c) Input device
   (d) Memory.
4. For the value of A OR B to be true,
   (a) neither of the two values A, B is true.
   (b) both of the values A,B must be true.
   (c) at least one of the two values A, B is true.
   (d) exactly one of tbe two values A, B is true.
5. If the condition codes have values N = 0, Z = 0, P = 1 at the beginning of the execution of the following sequence of instructions, what will their value be at the end of the execution of the following sequence?

Address	Instruction
0x3050	0000001000000001
0x3051	0101000000100000
0x3052	0001000000100001

   (a) $N = 0$, $Z = 0$, $P = 1$
   (b) Cannot be determined with the information given in the question.
   (c) $N = 0$, $Z = 1$, $P = 0$
   (d) $N = 1$, $Z = 0$, $P = 0$
6. We say that a set of gates is logically complete if we can build any circuit without using any other kind of gates. Which of the following sets are logically complete
   (a) None of the options
   (b) set of {AND,OR}
   (c) set of {EXOR, NOT}
   (d) set of {AND,OR,NOT}
7. The minimum number of transistors required to implement a two input AND gate is
   (a) 8
   (b) 6
   (c) 2
   (d) 4
8. Which of the following conditions is not allowed in an RS latch?
   (a) R is asserted, S is asserted
   (b) R is negated, S is negated
   (c) R is asserted, S is negated
   (d) R is negated, S is asserted
9. Which of the following instructions move the value in R5 into R6?
   i 0001110101100000
   ii 0101110101111111
   iii 1001110101111111
   (a) *i* and *iii*
   (b) *i* and *ii*
   (c) Only *i*
   (d) Only *ii*
10. With 12 bits, we can represent uniquely:
    (a) exactly 12 distinct items
    (b) exactly 4096 distinct items.
    (c) exactly 2 times 12, or 24 distinct items
    (d) as many distinct items as we wish to.
11. The addressability of LC-3 memory is
    (a) 2^{16} bits
    (b) 2^9 locations
    (c) 16 bits
    (d) 2^{16} locations
12. If the control is redirected to location 0x4444 after the execution of the following instructions, what should have been the relationship between R1 and R2 before these instructions were executed?

Address	Instruction
0x4400	1001100010111111
0x4401	0001100100100001
0x4402	0001100001000100
0x4403	0000100001000000

    (a) $R1 = R2$ (R1 and R2 were equal)
    (b) Cannot be determined with the given information.
    (c) $R1 < R2$ (R2 was greater than R1)
    (d) $R1 > R2$ (R1 was greater than R2)
13. A structure that stores a number of bits taken "together as a unit" is a
    (a) gate
    (b) register
    (c) decoder
    (d) mux

14. Which of the following LC-3 instructions does not access memory to fetch its operand?

    (a) LEA
    (b) LDI
    (c) LDR
    (d) All of the options instructions access memory to fetch their operands.

15. Two values A = 11111111111111111111111010101 and B = 1111010101 are representations of 2's complement integers.

    (a) B is larger
    (b) A and B are equal
    (c) You can not tell from the information provided.
    (d) A is larger

16. If m is a power of 2, the number of select lines required for an $m - input$ mux is:

    (a) 2^m
    (b) m
    (c) $2 * m$
    (d) $\log_2(m)$

17. For the number $A[15:0]$ = 0110110010001111, $A[14:13]$ is ..... $A[3:2]$.

    (a) less than
    (b) the same as
    (c) cannot be determined
    (d) greater than

18. ADD is an example of a/an

    (a) Control instruction
    (b) operate instruction
    (c) all of the options
    (d) data movement instruction

19. If a floating point number is represented in normalized form,

    (a) the most significant digit is non-zero.
    (b) it must be a positive number.
    (c) the most significant digit is 1.
    (d) it must be a negative number.

20. Each phase of an instruction cycle requires

    (a) between 0 and some finite number of cycles to do its job.
    (b) at least one clock cycle to do its job.
    (c) exactly one clock cycle to do its job.
    (d) no more than one clock cycle to do its job.

21. Typically the size of each register is ..... the size of values processed by the ALU.

    (a) greater than
    (b) unrelated to
    (c) identical to
    (d) less than

22. Using 8 bits, the unsigned integer representation of -13 is:

    (a) 00001101
    (b) not possible to represent.
    (c) 11110101
    (d) 10001101

23. The largest positive offset that can be used by an LC-3 instruction that utilizes the base+offset addressing mode is

    (a) 63
    (b) 31
    (c) 32
    (d) 64

24. The Von Neumann model consists of ..... parts

    (a) 3
    (b) 6
    (c) 4
    (d) 5

25. If the value stored in R0 is 1 at the end of the execution of the following instructions, what can be inferred about R5?

Address	Instruction
0x3000	0101000000100000
0x3001	0101100101100001
0x3002	0000010000000001
0x3003	0001000000100001

    (a) R5 is equal to 0
    (b) R5 is equal to 1
    (c) R5 is even
    (d) R5 is odd

26. In hex notation, each digit can have a value in the range:

    (a) 1 to 16
    (b) 0 to 9
    (c) 1 to 15
    (d) 0 to 15

27. The sequence of an Instruction cycle is:

    (a) FETCH → DECODE → EVALUATE ADDRESS → FETCH OPERANDS → EXECUTE → STORE RESULT
    (b) FETCH → DECODE → FETCH OPERANDS → EXECUTE → EVALUATE ADDRESS → STORE RESULT
    (c) FETCH → FETCH OPERANDS → DECODE → EVALUATE ADDRESS → EXECUTE → STORE RESULT
    (d) FETCH → DECODE → FETCH OPERANDS → EVALUATE ADDRESS → EXECUTE → STORE RESULT

28. For which of the following LC-3 instructions must all operands be in registers?

    (a) ADD
    (b) AND
    (c) LD
    (d) NOT

29. Which of the following circuits involves storage

    (a) RS Latch
    (b) mux
    (c) nand
    (d) decoder

30. LD is an example of a/an

    (a) Control Instruction
    (b) operate Instruction
    (c) data movement Instruction.
    (d) all of the options

31. An Instruction cycle consists of

    (a) more than 1 machine cycle
    (b) all of the options
    (c) fewer than 1 machine cycle
    (d) Exactly 1 machine cycle.

32. The Decode phase of the Instruction Cycle examines the part of the instruction.

    (a) Register
    (b) Immediate (literal) value
    (c) Offset
    (d) Opcode

33. For which of the following LC-3 instructions is no memory access performed during the instruction cycle?

    (a) LEA
    (b) STI
    (c) For all of the options, instructions memory is accessed during the instruction cycle.
    (d) LDR

34. The PC is incremented so that during the next instruction cycle, the next instruction will be processed. This happens during the

    (a) DECODE phase
    (b) EXEC phase
    (c) EVAL ADDRESS phase
    (d) FETCH phase

35. The following LC-3 instruction is located at memory address $0x5F55$. Which of the following describes the operation of this instruction?

    0000101100000000

    (a) If either N or P condition code is set, the instruction will load $0x5F56$ into the PC.
    (b) If both the N and P condition codes are set, the instruction will load $0x5E56$ into the PC.
    (c) If either N or P condition code is set, the instruction will load $0x5E56$ into the PC.
    (d) If both the N and P condition codes are set, the instruction will load $0x5F56$ into the PC.

36. If the LC-3 ISA was modified to specify 32 general purpose registers and every other specification remained unchanged, how many bits would be required to encode an LC-3 ADD instruction?

    (a) 25
    (b) 20
    (c) 24
    (d) 16

37. After the execution of which of the following instructions will the value in the Program Counter (PC) be $0x306e$?

    i 0000111001011100 at location $0x3011$
    ii 0000000001101110 at location $0x306d$
    iii 1010011001101110 at location $0x306d$

    (a) *i* and *iii*
    (b) *ii* and *iii*
    (c) *i*, *ii*, and *iii*
    (d) *i* and *ii*

38. A computer memory contains:

    (a) data only
    (b) Neither instructionn nor data.
    (c) Intructions only.
    (d) both instructions and data.

39. If we add two negative integers, represented in 2's complement notation, and the result is positive, we know:

    (a) nothing about the result.
    (b) that the result is also a negative integer
    (c) that we must have caused an overflow condition.
    (d) that the result is also a non-positive intege

40. The LC-3 ADD instruction:

    (a) can add a 16-bit value to a zero-extended 5-bit value
    (b) can only add two 16-bit values found in registers
    (c) can add a 16-bit value to a sign-extended 5-bit value
    (d) can add a 16-bit value to a sign-extended 10-bit value

41. In 2's complement arithmetic, an overflow occurs if:

    i two positive numbers produce a negative result

    ii two negative numbers produce a positive result

    (a) both i and ii
    (b) ii
    (c) neither i nor ii
    (d) i

42. Which of the following is not specified by the ISA of LC-3?

    (a) Number of general purpose registers
    (b) Data types
    (c) Number of adders in an LC-3 processor
    (d) Encodings of opcodes

43. JMP is an example of a/an

    (a) data movement Instruction.
    (b) operate Instruction
    (c) control and operate Instruction
    (d) control Instruction

44. Which of the following instructions can reference a memory location that is #1000 locations from the instruction?

    (a) LEA
    (b) STR
    (c) LD
    (d) ADD

45. Control Instructions change the value of PC in the

    (a) EXECUTE phase.
    (b) DECODE phase.
    (c) FETCH phase
    (d) EVALUATE ADDRESS phase.

46. Which of the following instructions at address 0x0200 clear register R5?

    i 0001101101100000

    ii 0101101101100000

    iii 1110101000000000

    iv 0010101000000000

    (a) *i* and *ii*
    (b) *i*, *ii*, and *iii*
    (c) *ii*
    (d) *ii* and *iv*

47. During the processing of which of the following instructions is the use of an adder not required? (Processing of an instruction spans the whole instruction cycle.) Neglect the requirement of incrementing PC in the FETCH phase of the instruction cycle, which can be accomplished with a simpler increment circuit and does not require a full blown adder.

    (a) LDR
    (b) ADD
    (c) AND
    (d) STR

48. Circuit A is a 1-bit adder; circuit B is a 1 bit multiplier.

    (a) Circuit A has the same number of gates as circuit B
    (b) non of the options
    (c) Circuit A has more gates than circuit B
    (d) Circuit B has more gates than circuit A

49. Which of the following instructions needs an EVALUATE ADDRESS phase:

    (a) JMP
    (b) ADD
    (c) NOT
    (d) LD

50. ..... Instructions are used to change the sequence of instruction execution.

    (a) Control
    (b) operate
    (c) data movement .

51. [16 Marks]Consider the given algorithm, which sets R1 to 1 if a given number is a power of 2 less than 2048; else sets R1 to 0. The number is stored in the memory location "0x4000".

This is the algorithm you will use:

Step1: Load the given number from the memory location "0x4000" to the Register R2.

Step2: Check if the number is 1. If it is, the number is a power of 2. Set R1 to 1. Go to step 8.

Step3: Put the integer "2" in register R4.

Step4: If R4 is equal to R2, set R1 as 1. Go to step 8.

Step5: If R4 is not equal to R2, multiply R4 by 2 and put the result in register R4.

Step6: If R4 < 2048, go to step 4.

Step7: If R4 >= 2048, clear R1.

Step8: Halt

Convert the above algorithm to an LC-3 program.

52. [8 Marks] Fill in the table for the following equations given the starting values A, B, and C.
$Q1 = (A\ AND\ B)\ OR\ NOT\ C$ $Q2 = B\ OR\ NOT(C\ AND\ B)$

A	B	C	Q1	Q2
1001	1110	0011		
0110	0011	1011		

53. [8 Marks]The truth table below has two inputs, A and B, and two outputs, S and C.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Draw the gate-level circuit for the outputs S and C. Use ONLY NOT and 2-input AND gates.

54. [12 Marks] Draw a finite state machine (FSM) with four states (00, 01, 10, and 11) and a 1-bit input. It should have the following transitions:

i. The input of 0 changes the state from 00 to 01.

ii. The input of 1 at state 00 does not change the state.

iii. The input of 1 changes states from 01 to 10.

iv. The input of 0 at state 01 does not change the state.

v. The input of 1 changes states from 10 to 11.

vi. The input of 0 changes states from 11 to 10.

55. [8 Marks]The following pseudo-code presents an algorithm to check if the data present in R1 is greater than 4. The table below shows an incomplete LC-3 binary program that implements this logic. **Assume that R1 has been initialised to the data value being checked.**

$R1 = R1 - 4$
$R2 = 0$
If $R1 > 0$ *then*:
    $R2 = 1$
end if
HALT
Assume PC is x3000 when execution of the program starts.

Address	Instruction	Comment
0x3000	0101 010 010 1 00000	R2 = 0
0x3001		
0x3002		
0x3003	0001 010 010 1 00001	ADD R2, R2, #1
0x3004	1111 0000 00100101	HALT

56. [2 Marks]In LC3, what is the difference between a jump and a branch instruction? Describe at least one way they are the same and one way they are different.

57. [8 Marks] You are given a 8-bit binary number A = 11111111.

    a. Write the decimal equivalent of A, assuming A is represented in 1's complement form.

    b. Write the decimal equivalent of A, assuming A is represented in 2's complement form.

    c. What is the smallest decimal number that can be represented with an **8-bit 1's complement** number?

    d. How many unique numbers can be represented using 8-bit **1's complement**? Show your answer in decimal value.

58. [8 Marks] Figure 1 shows the output of a transistor-level circuit connected to the select line of a 2-input multiplexer.

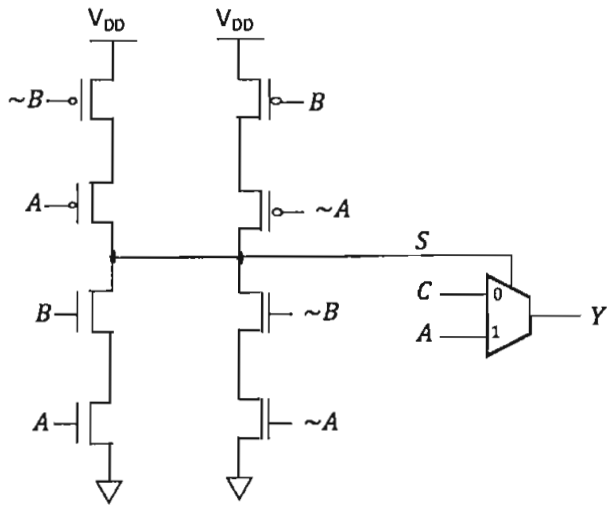

Figure 1:

Fill out the following truth table for the overall circuit. (Note: $\sim A$ means NOT(A)).

A	B	C	S	Y
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		