

# Port-Level I/O Protocols Demo Script

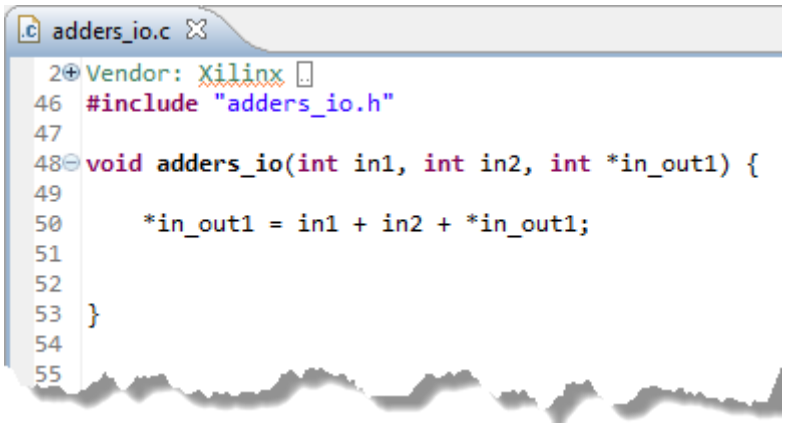
## Introduction

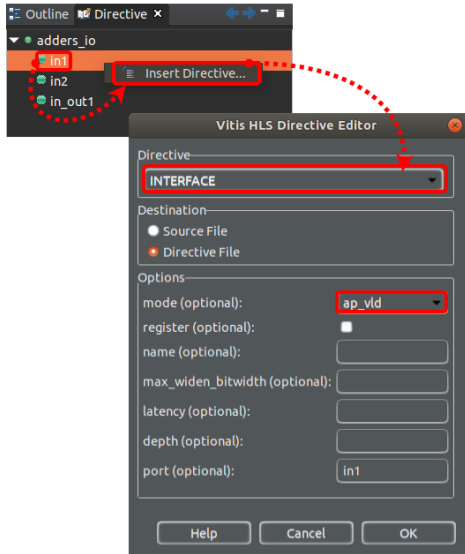
This demonstration script provides high-level instructions on how to specify port I/O protocols.

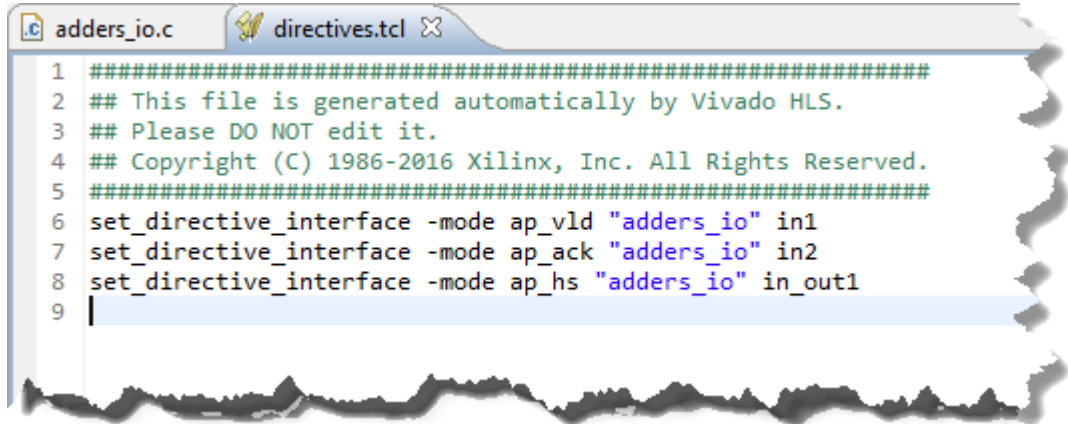
## Port-Level I/O Protocols

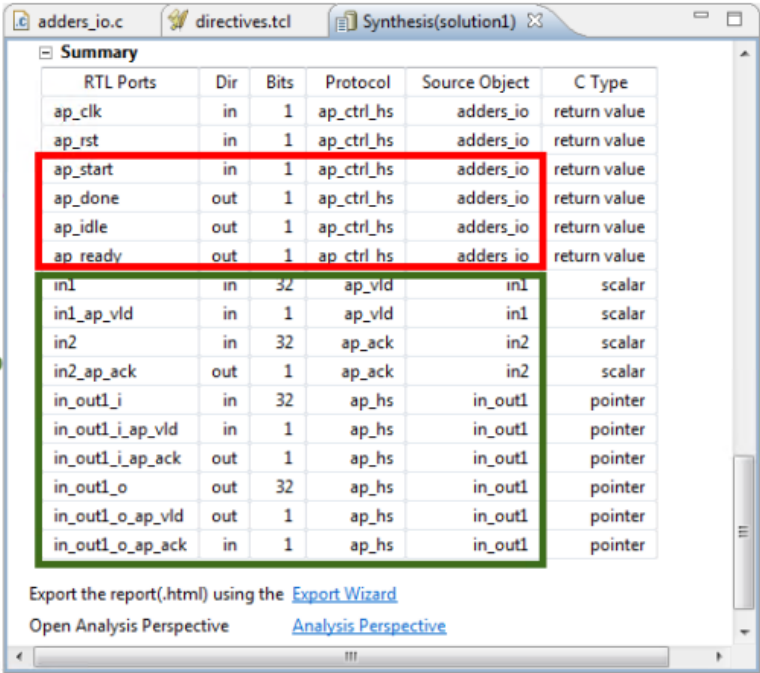
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| Action with Description  | Point of Emphasis and Key Takeaway  |
|--|---|
| <ul style="list-style-type: none"><li>Launch the Vitis™ HLS tool.</li><li>Open the provided <b>adders_io_prj</b> Vitis HLS project located in the following location:<ul style="list-style-type: none"><li>C:\Xilinx_trn\HLS2023\lab3_z0</li></ul></li></ul> | <p>You can open existing Vitis HLS tool projects from the Vitis HLS tool Welcome page. To open project <b><i>adders_io_prj</i></b> – select <i>folder adders_io_prj</i></p> |

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|---|---|
| <ul style="list-style-type: none"> <li>Access and review the source file <b>adders_io.c</b> from the Explorer pane.</li> </ul>  | <p>The source code is a very simple code, which helps to focus on the interface behavior and not the core logic.</p> <p>The code does not have a function return, but instead passes the output of the function through the pointer argument <code>*in_out1</code>.</p> <p>This also provides the opportunity to explore the interface options for bidirectional (input and output) ports.</p> <p>The pointer argument in this example is both an input and output to the function. In the RTL design, this argument is implemented as separate input and output ports.</p> |
|  <pre> 2 Vendor: Xilinx 46 #include "adders_io.h" 47 48 void adders_io(int in1, int in2, int *in_out1) { 49 50     *in_out1 = in1 + in2 + *in_out1; 51 52 53 } 54 55 </pre> |   |

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|---|---|
| <ul style="list-style-type: none"> <li>Apply the directive using the GUI and see that the directives have been added to the <i>directives.tcl</i> file.</li> </ul> <pre> set_directive_interface -mode ap_vld "adders_io" in1 set_directive_interface -mode ap_ack "adders_io" in2 set_directive_interface -mode ap_hs "adders_io" in_out1 </pre> | <p>You can apply the directives through the directives.tcl file located under the solutions1 &gt; constraints folder or through the GUI mode.</p> <p>Right-click argument <b>in1</b> and select <b>Insert Directive</b> to choose the <b>INTERFACE</b> directive as <b>ap_vld</b>.</p> <p>Right-click argument <b>in2</b> and select <b>Insert Directive</b> to choose the <b>INTERFACE</b> directive as <b>ap_ack</b>.</p> <p>Right-click argument <b>in_out1</b> and select <b>Insert Directive</b> to choose the <b>INTERFACE</b> directive as <b>ap_hs</b>.</p>  |

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|--|--|
| <ul style="list-style-type: none"> <li>Your directives.tcl file should look like the below one:</li> </ul>  <pre> 1 ##### 2 ## This file is generated automatically by Vivado HLS. 3 ## Please DO NOT edit it. 4 ## Copyright (C) 1986-2016 Xilinx, Inc. All Rights Reserved. 5 ##### 6 set_directive_interface -mode ap_vld "adders_io" in1 7 set_directive_interface -mode ap_ack "adders_io" in2 8 set_directive_interface -mode ap_hs "adders_io" in_out1 9 </pre> |  |
| <ul style="list-style-type: none"> <li>Run C synthesis.</li> <li>Expand the <b>adders_io_prj</b> &gt; <b>solution1</b> &gt; <b>syn</b> &gt; <b>report</b> folder in the Explorer pane.</li> <li>Double-click the <b>adders_io_csynth.rpt</b> file to view the Synthesis report.</li> <li>Review the <b>Interface Summary</b> in the Synthesis report.</li> </ul>   | <p>Note the port-level I/O protocols that are implemented.</p> |

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|---|--|
| <p>Block-Level Protocol</p> <p>Port-Level I/O Protocol</p>  | <ul style="list-style-type: none"> <li>Explain the Interface summary report: <ul style="list-style-type: none"> <li>The design has a clock and reset.</li> <li>The default block-level I/O protocol signals are present.</li> <li>Port <b>in1</b> is implemented with a data port and an associated input valid signal.</li> <li>The data on port <b>in1</b> is only read when port <code>in1_ap_vld</code> is active-High.</li> <li>Port <b>in2</b> is implemented with a data port and an associated output acknowledge signal.</li> <li>Port <code>in2_ap_ack</code> will be active-High when data port <code>in2</code> is read.</li> <li>The <code>inout_i</code> identifies the input part of argument <b>inout1</b>. This has associated input valid port <code>inout1_i_ap_vld</code> and output acknowledge port <code>inout1_i_ap_ack</code>.</li> <li>The output part of argument <b>inout1</b> is identified as <code>inout_o</code>. This has associated output valid port <code>inout1_o_ap_vld</code> and input acknowledge port <code>inout1_o_ap_ack</code>.</li> </ul> </li> <li>Exit the Vitis HLS tool GUI.</li> </ul> |

## Summary

In this demo, you learned to apply directives for port-level protocols.

References:

- Supporting materials
  - *Vitis High-Level Synthesis User Guide* (UG1399)