# Введение в Vitis HLS Tool CLI Flow

2021.2

## Abstract

This lab introduces how to perform basic actions in the Vitis® HLS command prompt.

## Objectives

After completing this lab, you will be able to:

* Create a new project in the Vitis HLS tool CLI
* Simulate a C design by using a self-checking test bench
* Synthesize the design
* Simulate an RTL design by using a C test bench
* Implement the design

## Introduction

This lab introduces the major features of the Vitis® High-Level Synthesis (HLS) tool Command Line Interface (CLI) flow. You will use the Vitis HLS tool in CLI mode to create a project. You will also simulate, synthesize, and implement the design provided.

## General Flow

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| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Step 1:  Creating a Vitis HLS Project |  | Step 2:  Running C Simulation & Synthesizing |  | Step 3:  Co- simulating  & Exporting |  | Step 4:  Building the full TCL script |  | Step 5:  Building TCL script and explore solutions |

Before starting the lab Step 0

Create the folders using Windows Explorer

C:\Xilinx\_trn\HLS2023\lab2\_z0\doc

Explore the C codes to understand algorithm and data dependencies.: lab2\_z0.h and lab2\_z0.c (C:\Xilinx\_trn\HLS2023\lab2\_z0\source folder).

Explore the C codes to understand algorithm and data dependencies.: lab2\_z0\_test.c file(C:\Xilinx\_trn\HLS2023\lab2\_z0\source folder).

Creating a Vitis HLS Tool Project Step 1

In this step, you will create a new Vitis HLS tool project, add source files, and provide solution settings for the default solution using the Vitis HLS tool command prompt. Later, you will open the created project in the Vitis HLS tool GUI to have a quick review of the settings were applied.

1-1. Write the commands to create a new project, associate source files, and configure solution settings.

1-1-1. Browse to the C:\Xilinx\_trn\HLS2023\lab2\_z0 directory using Windows Explorer and create and open lab2\_z0.tcl with your preferred text editor. Enter the commands pointed in the figure.

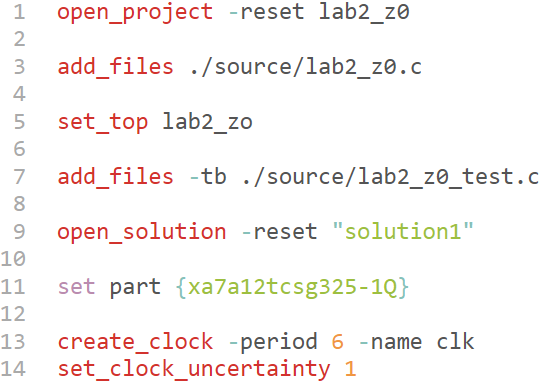


Figure 1: lab2\_z0.tcl with Project Information

Question 1

What does the **open\_project -reset lab2\_z0** do?

Question 2

What do the **add\_files ./source/lab2\_z0** and **set\_top lab2\_zo** do?

Question 3

What does the **add\_files -tb ./source/lab2\_z0\_test.c** do?

Question 4

What does the **open\_solution -reset "solution1"** do?

Question 5

What does the **set part {xa7a12tcsg325-1Q}** do?

Question 6

What do the **create\_clock -period 6 -name clk** and **set\_clock\_uncertainty 1** do?

1-1-2. Save the lab2\_z0.tcl file.

1-1-3. Exit the text editor to close the Tcl file.

1-2. Launch the Vitis HLS tool command prompt and change the directory to the C:\Xilinx\_trn\HLS2023\lab2\_z0 working directory.

1-2-1. For Windows 10: Start > Xilinx Design Tools > Vitis HLS 2021.2 Command Prompt.

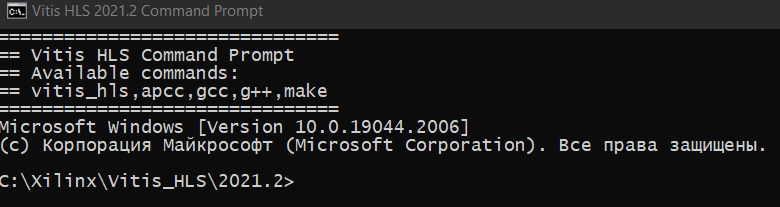


Figure 2: Vitis HLS Command Prompt

1-2-2. Enter the following command to change the directory to the current working directory:

**cd C:\Xilinx\_trn\HLS2023\lab2\_z0**

Run the lab2\_z0.tcl file to create the project and open the created project in the Vitis HLS tool GUI.

1-2-1. Enter the following command in the Vitis HLS tool command prompt to run the lab2.tcl file:

**Vitis\_hls -f lab2\_z0.tcl**

1-2-2. Enter the following command to launch the GUI with the recently created project:

**Vitis\_hls -p lab2\_z0**

You should see the created project in the Explorer view.

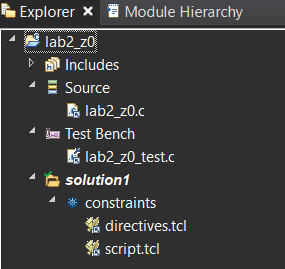


Figure 3: Vitis HLS GUI with Recently Created Project

1-2-3. Select Project > Project Settings in the Vitis HLS tool GUI.

The Project Settings dialog box opens.

1-2-3-1. Click Synthesis to ensure that the design source was added to the project as entered in the Tcl file.

1-2-3-2. Click Simulation to ensure that the test bench source was added to the project as entered in the Tcl file

1-2-4. Close the Project Settings dialog box once the source files are verified.

1-2-5. Select Solution > Solution Settings in the Vitis HLS tool GUI.

The Solution Settings dialog box for the active solution, i.e., Solution1, the only solution that exists in this current project, opens.

1-2-6. Select Synthesis to ensure that the clock frequency and part number are the ones described in the Tcl file.

1-2-7. Close the Solution Settings dialog box once the clock frequency and device settings are verified.

1-2-8. Select File > Exit in the Vitis HLS tool GUI to exit the GUI.

Running C Simulation and Synthesizing the Design Step 2

In this step, you will run C simulation and synthesize the design from the Vitis HLS tool command prompt and then open the Vitis HLS tool GUI to review the project status and Synthesis report.

2-1. Simulate the design.

2-1-1. Enter the following command in the Vitis HLS tool command prompt to run C simulation:

csim\_design -clean

This command compiles and runs pre-synthesis C simulation of the design using the provided C test bench.



Figure 4: Running C Simulation from the Command Prompt

2-2. Synthesize the design.

2-2-1. Enter following command in the Vitis HLS tool command prompt to synthesize the design:

**csynth\_design**

This will elaborate and perform high-level synthesis on the source files added to the project. This also analyzes the sources files, validates the directives if they are present, and performs some initial code transformations.

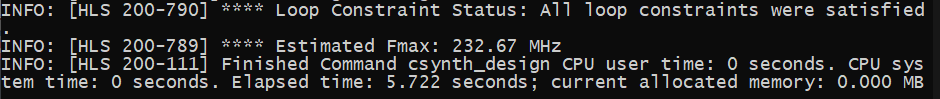


Figure 5: Performing Synthesis from the Command Prompt

2-3. Verify the Synthesis report in the Vitis HLS tool GUI.

2-3-1. Enter the following command to launch the GUI:

Vitis\_hls -p lab2\_z0

2-3-2. Select Solution > Open Report > Synthesis in the Vitis HLS tool GUI if the Synthesis report does not open automatically.

2-3-3. Analyze the report file.

Question 7

Write down the following details from the Synthesis report and Performance profile:

* Estimated clock period:
* latency (cycles):
* Loop trip count:
* Loop Iteration Latency (cycles):
* Loop Latency (cycles):
* Iteration Interval (cycles):
* Iteration Interval (time): Iteration Interval (cycles) \* Estimatedё clock period =
* Number of BRAM\_18K:
* Number of DSP48E used:
* Number of FFs used:
* Number of LUTs used:
* Number of URAM used:

Question 8

Explain why the Latency(cycles) is one cycle more than Loop latency (cycles).

Explain why the Iteration Interval(cycles) is one cycle more than Latency(cycles).

2-3-4. Select File > Exit in the Vitis HLS tool GUI to exit the GUI.

Co-simulating and Exporting the RTL Step 3

In this step, you will perform C/RTL co-simulation on the generated RTL files by using the C test bench from the Vitis HLS tool command prompt.

3-1. Perform C/RTL co-simulation.

3-1-1. Enter the following command in the Vitis HLS tool command prompt to execute post-synthesis co-simulation:

cosim\_design -trace\_level all -tool xsim

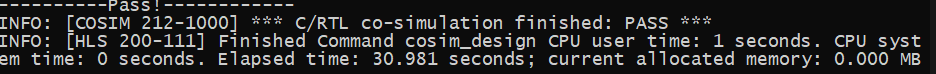


Figure 6: C/RTL Co-simulation

Notice that the message \*\*\* C/RTL co-simulation finished: PASS \*\*\* is displayed.

3-2. Verify the results in the Vitis HLS tool GUI.

3-2-1. Enter the following command to launch the GUI:

Vitis\_hls -p lab2\_z0

3-2-2. Select Solution > Open Report > Cosimulation in the Vitis HLS tool GUI to open the RTL Simulation report.

Question 9

Compare Iteration Interval (Avg, Max, Min), latency (Avg, Max, Min) achieved after cosimulation with the results achieved after synthesis.

3-2-3. Close the Vitis HLS tool GUI.

3-2-4. Enter the following command to close the Vitis HLS tool command prompt:

exit

Building the full lab2\_z0.tcl file Step 4

4-1. Complete the lab2\_z0.tcl file.

4-1-1. Browse to the C:\Xilinx\_trn\HLS\_2023\lab2\_z0 directory using Windows Explorer and open lab2\_z0.tcl with your preferred text editor.

4-1-2. Insert the following, highlighted commands, into lab2\_z0.tcl to complete the script:

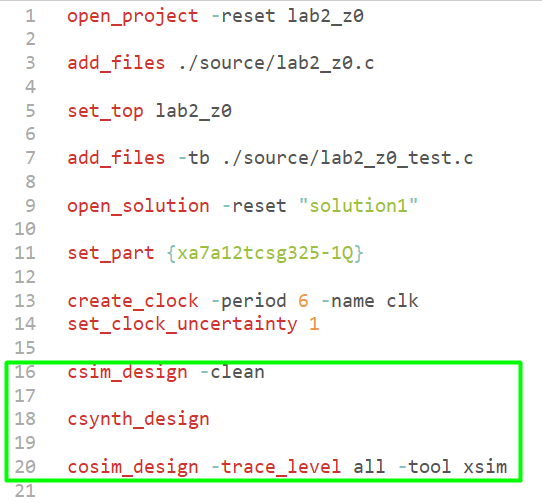


Figure 7: Full lab2\_z0.tcl script

4-1-3. Save the lab2\_z0.tcl file.

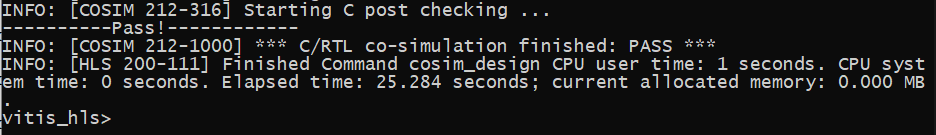
4-1-4. Exit the text editor to close the Tcl file.

4-2. Run complete script.

4-2-1. Enter the following command in the Vitis HLS tool command prompt to run the lab2\_z0.tcl file:

Vitis\_hls -f lab2\_z0.tcl

Full procedure from creating the project up to cosimulation will be implemented.



4-2-2. Enter the following command to close the Vitis HLS tool command prompt:

exit

Building the lab2\_z0\_ex.tcl file and conduct an exploration Step 5

5-1. Complete the lab2\_z0\_ex.tcl file.

5-1-1. Browse to the C:\Xilinx\_trn\HLS\_2023\lab2\_z0 directory using Windows Explorer create and open lab2\_z0\_ex.tcl with your preferred text editor.

5-1-2. Insert the commands into lab2\_z0\_ex.tcl to complete the script for exploration procedure:

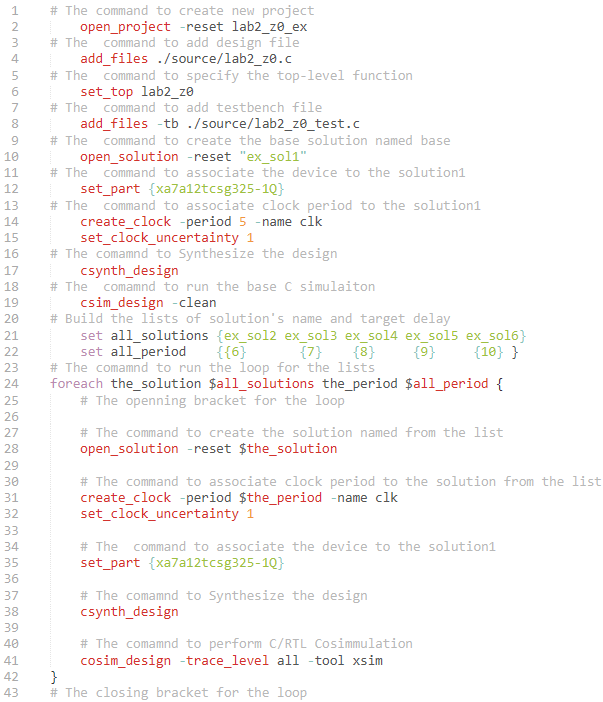


Figure 8: lab2\_ex.tcl script

5-1-3. Save the lab2\_z0\_ex.tcl file.

5-1-4. Exit the text editor to close the Tcl file.

5-2. Run complete script.

5-2-1. Enter the following command in the Vitis HLS tool command prompt to run the lab2\_z0\_ex.tcl file:

Vitis\_hls -f lab2\_z0\_ex.tcl

Full procedure from creating the project up to co-simulation for each delay in the list will be implemented.

5-2-2. Enter the following command to close the Vitis HLS tool command prompt:

exit

5-3. Verify and compare the Synthesis reports in the Vitis HLS tool GUI.

5-3-1. Enter the following command to launch the GUI:

Vitis\_hls -p lab2\_z0\_ex

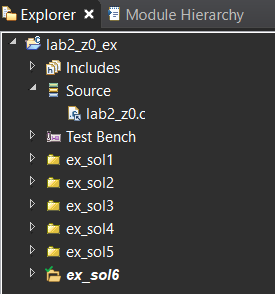


Figure 9: Vitis HLS tool GUI for lab2\_explore\_prj project

5-3-2. Verify that there are six solutions: *ex\_sol[6:1]*.

5-3-3. Verify that *ex\_sol6* is active and the target clock period is equal 10ns.

5-3-4. Select Project > Compare Reports in the Vitis HLS tool GUI.

5-3-5. In the window appeared select all solutions for comparing.

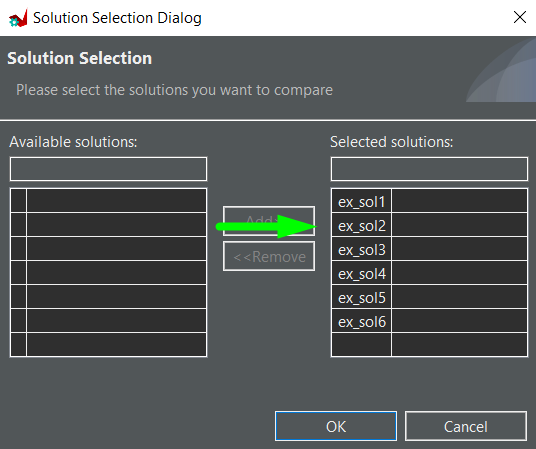


Figure 10: Solutions to compare - report

5-3-6. Use data from the *compare\_report* tab to complete the spreadsheet as it done on the following figure (An example of the spreadsheet is in file ./source/lab2\_z0\_ex.xlsx).

Pay attention that Latency (ns) is calculated by multiplying **Clock estimated (ns)** on Iteration interval (cycles).

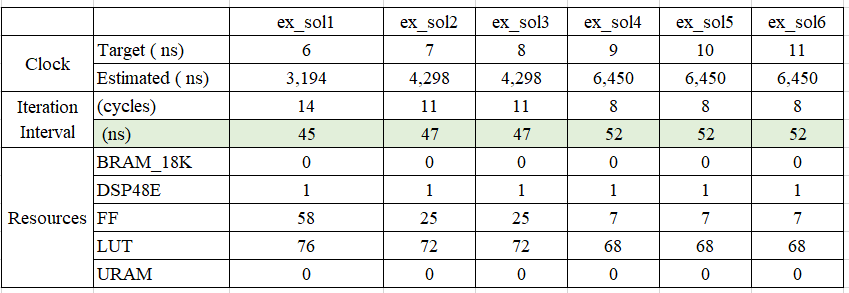


Figure 11: Solutions to compare - spreadsheet

5-3-7. Construct the diagram by using Iteration Interval (ns) and FF, LUT resources (DSP, BRAM18, URAM have constant values and can be omitted). (An example of the spreadsheet with the diagram is in file ./source/lab2\_z0\_ex.xlsx).

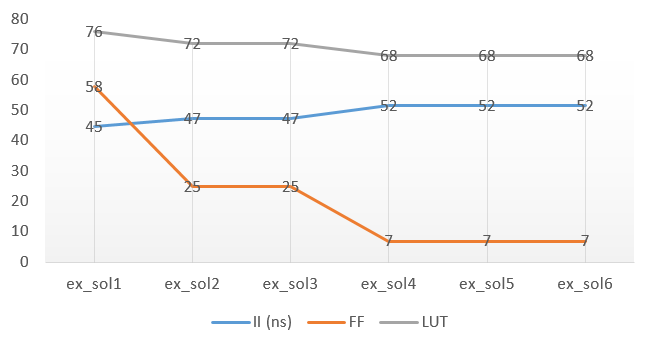


Figure 12: Solutions to compare - diagram

Question 10

Explain which solution, in your opinion, is the best (criteria are max performance and min resources) and why do you think so.

## Summary

In this lab, you learned how to use the Vitis HLS tool command prompt to:

* Create the Vitis HLS tool project
* Create a solution with the desired settings
* Execute major actions in the Vitis HLS (simulate, synthesize, cosimulate and export the RTL of the design) design flow

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