

Understanding the transient detector

Its functionalities and effects

About this document

Scope and purpose

This document describes the functionality of the transient detector intellectual property block and its effects on MOSFET driver on-off transitions. It also provides suggestions for selecting minimum pulse width according to oscillation in the application.

Intended audience

Power supply designers, component engineers, hardware engineers, etc.

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Transient detector description

1 Transient detector description

Looking into the implementation of 2EDL8x2x driver and DHPxxxxNxxx5 power-stage product families, one can find the inclusion of an IP block called “transient detector” in the block diagram shown below. The transient detector block is placed close to the High-side Output (HO) driver in order to ensure the stability of the driver output signal in case of potential instability of the level shifter caused by phase node movement. (Explicitly, the transient detector does not affect the low-side output.)

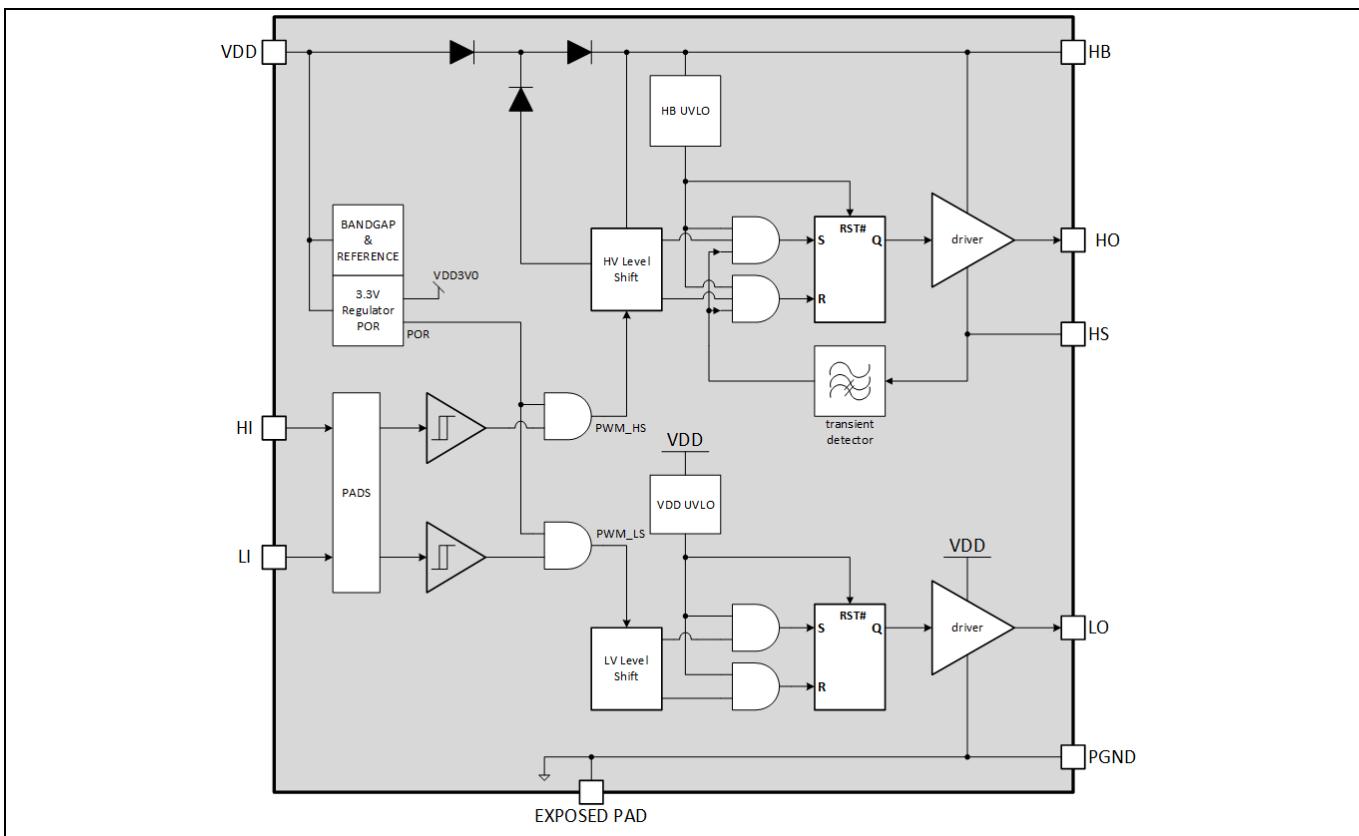


Figure 1 Detailed driver block diagram

The following describes the basic operation of the block.

- The transient detector monitors the phase node and tracks its movement, and the rate of change over time for both rising and falling edge.
- Whenever the rate of change is larger than a certain dv/dt threshold, the transient detector is active and blocks the HO output from changing state.
- A High-side Input (HI) toggle triggers a decision to change the state, but HO waits until the transient detector's active state is removed, then the decision is propagated through.

This block is designed to prevent re-toggling of HO due to the instability of the level shifter caused by phase node movement. For example, a fast-rising phase node voltage could pull the power ground (PGND) down. This could result in potential between HI and PGND higher than the rising threshold of the high-side signal. Such a glitch or noise can be picked up by the driver and propagate through. This results in incorrect logic that could lead to a shoot-through event, transformer volt-second imbalance, and potential device destruction.

While the transient detector works well to prevent re-toggling, it could falsely trigger under certain circumstances. The following describes different scenarios that have been observed and taken into account so far.

Transient detector description

First, the transient detector is activated within a given dv/dt range. A common phase node switching waveform has an overshoot and oscillates with a certain damping factor. The transient detector toggles between active and inactive states while there is movement detected on the phase node, as shown below. Switching HI before and after the switching event and its oscillation yields correct logic operation.

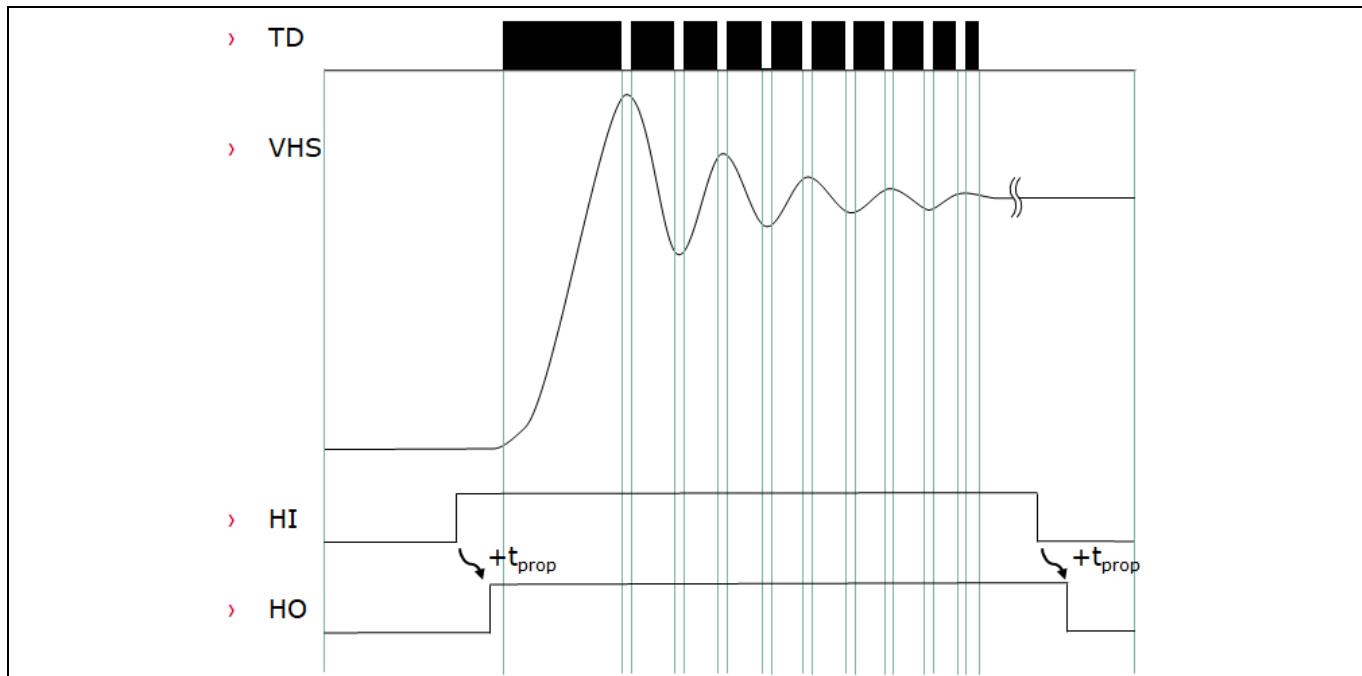


Figure 2 Hard switching before and after oscillation, e.g. hard-switching buck

1.1 Transient detector affecting turning off

If the turning off event is initiated before the oscillation settles down, the activated transient detector would block and delay the toggling decision until the next time the transient detector is deactivated. The waveform example below shows the switching off behavior while the transient detector is still activated. The shaded region in red indicates the additional delay introduced by the activation of the transient detector before the next deactivation. This illustration is applicable to a buck with short duty cycle and a full-bridge converter in burst mode (also short pulses).

Transient detector description

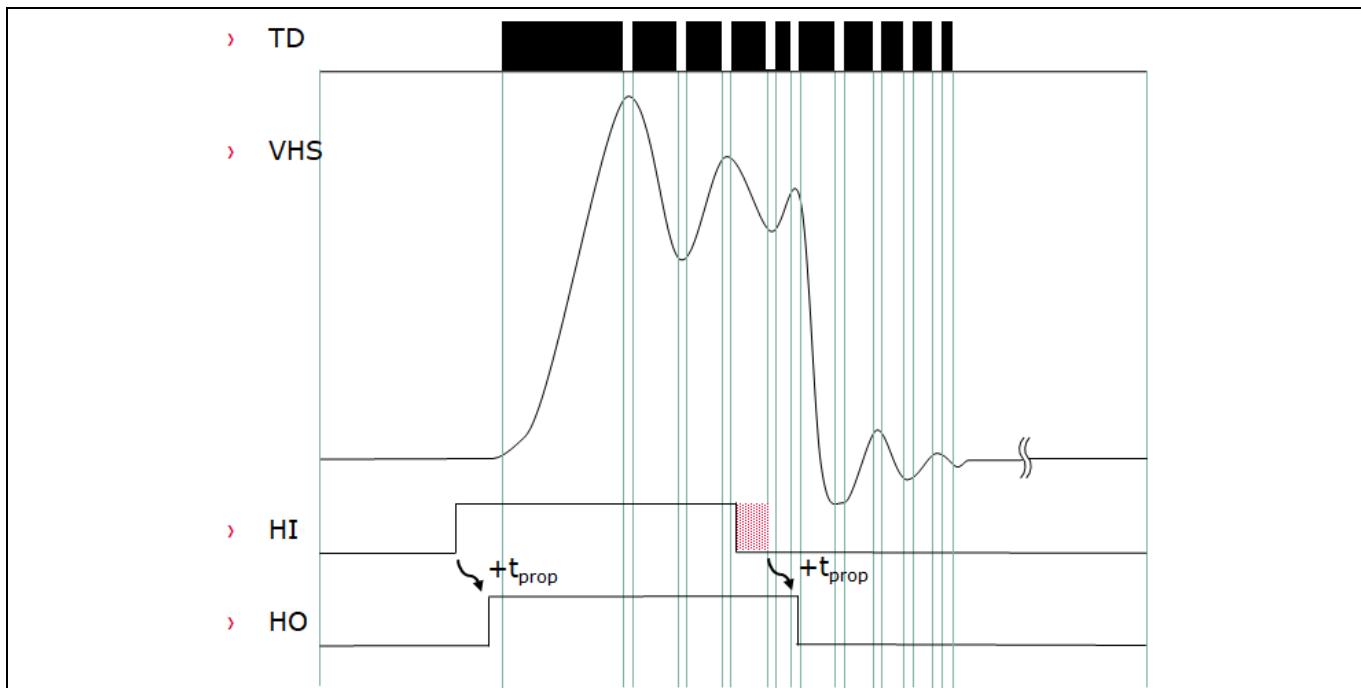


Figure 3 Switching off before oscillation completes, e.g. short duty cycle and burst mode

1.2 Transient detector affecting turning on

Another scenario of a delayed decision reacting to HI toggle can happen when HI is turned on before low-level oscillation finishes. This oscillation could be part of the unfinished undershoot oscillation in buck converters or the primary-side mid-level oscillation in full-bridge converters. Again, the shaded region in red indicates the additional delay introduced by the activation of the transient detector before the next deactivation.

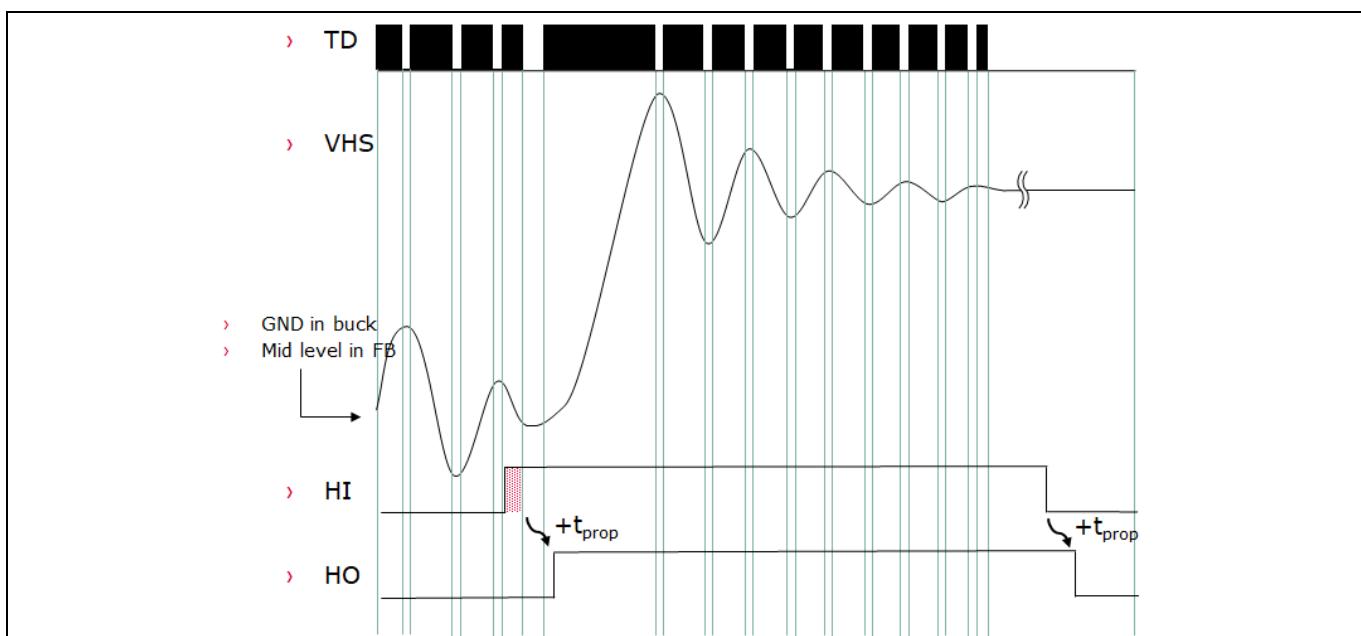


Figure 4 Switching on before oscillation completes, e.g. buck and feedback with short dead-time

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Transient detector description

Additional delay caused by the transient detector is limited to one-half of the oscillation period, as the signal always propagates through whenever the transient detector sees a peak or valley where dv/dt approaches zero.

The examples given above are applicable for hard-switching topologies, such as buck and full-bridge converters, where the effect is generally small and can be avoided as shown in the next section. For soft-switching topologies, the transient detector will have a more significant effect if used in the primary side simply because the phase node takes longer to settle after a transition. This results in longer propagation delay and therefore, drivers with a transient detector are not recommended for soft-switching primary-side application. For soft-switching secondary-side application, the delayed turn-on of synchronous rectification FETs is safe but results in extended body diode conduction, potentially causing efficiency drop.

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Choosing minimum pulse width for the application

2 Choosing minimum pulse width for the application

How to work with the transient detector in an application? Use the following methodology to select the minimum pulse width in the application.

1. Start with a short pulse width of 50 ns.
2. Increase and ramp up the width by 10 ns.
3. Monitor the output pulse and record pulse extension. Please note, pulse width distortion is below 5 percent. If oscillation is detected, the high-side output pulse will extend slightly.

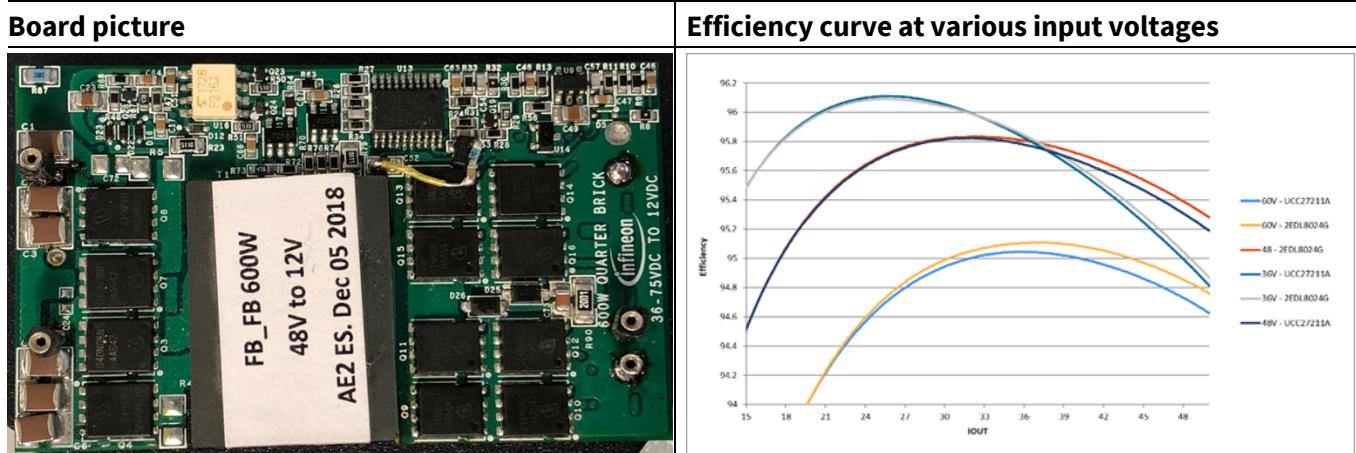
The short pulse distortion (extension) depends on the oscillation settling time in the application. An example, in our isolated DC-DC converter demo, is shown below.

Table 1 Example showing pulse extension with short pulse width

HI pulse width [ns]	HO pulse width [ns]
50	65
60	70
70	80
80	85
90	90

As a result, the minimum pulse width was chosen to be 100 ns and the device operates according to intended functionality under all operating conditions in this application. The following showcases the efficiency of such an application.

Table 2 Driver outperforms competition in isolated DC-DC converter despite transient detector



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Datasheet information related to transient detector



3 Datasheet information related to transient detector

The following shows three sections with transient detector related information in the datasheet. This clearly explains its relevance to the propagation delay and illustrates the slew rate threshold and its temperature dependency.

Table 3 Datasheet information related to the transient detector

Section	Information														
1) 4.4 Dynamic Electrical Characteristics	<table border="1"><tr><td>T_{DR}</td><td>Rising Propagation Delay^{2,3}</td><td>---</td><td>45</td><td>50</td><td>ns</td><td>$C_{LOAD} = 0$</td></tr><tr><td>T_{DF}</td><td>Falling Propagation Delay⁷</td><td>---</td><td>45</td><td>54</td><td>ns</td><td>$C_{LOAD} = 0$</td></tr></table> <p>² A transient detector blocks the toggling of the high side output when it detects moving phase node (due to transition and/or oscillation). It prevents unwanted retoggling but may increase propagation delay. See transient detector activation in Figure 6.</p>	T_{DR}	Rising Propagation Delay ^{2,3}	---	45	50	ns	$C_{LOAD} = 0$	T_{DF}	Falling Propagation Delay ⁷	---	45	54	ns	$C_{LOAD} = 0$
T_{DR}	Rising Propagation Delay ^{2,3}	---	45	50	ns	$C_{LOAD} = 0$									
T_{DF}	Falling Propagation Delay ⁷	---	45	54	ns	$C_{LOAD} = 0$									
2) 5 Descriptive Illustration	<p>Figure 6 Transient Detector Response¹</p> <p>¹ Reference slew rate threshold versus temperature under Section 6 Typical Characteristics.</p>														
3) 6 Typical Characteristics	<p>Transient Detector Threshold vs. Temperature</p> <table border="1"><caption>Data points estimated from Figure 6</caption><thead><tr><th>Junction Temperature [°C]</th><th>Slew Rate Threshold [V/ns]</th></tr></thead><tbody><tr><td>-50</td><td>0.24</td></tr><tr><td>0</td><td>0.20</td></tr><tr><td>50</td><td>0.16</td></tr><tr><td>100</td><td>0.12</td></tr><tr><td>150</td><td>0.09</td></tr></tbody></table> <p>$V_{DD} = 12 \text{ V}$</p>	Junction Temperature [°C]	Slew Rate Threshold [V/ns]	-50	0.24	0	0.20	50	0.16	100	0.12	150	0.09		
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Revision history

Document version	Date of release	Description of changes

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