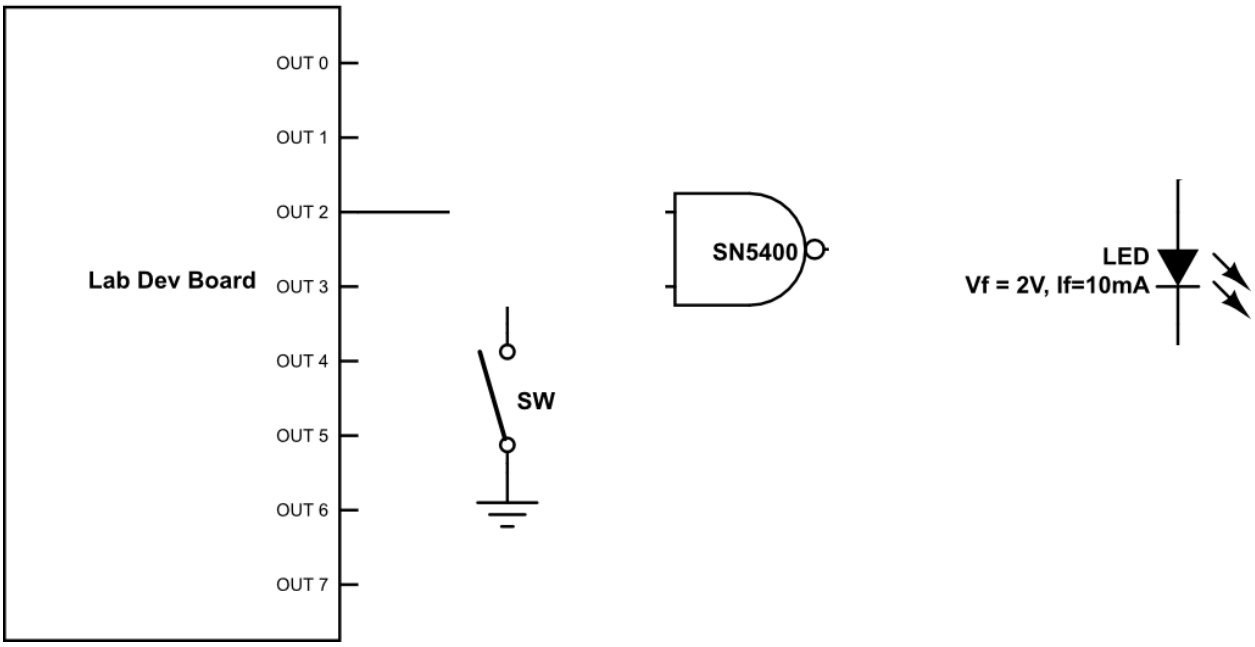
ECE3221 – Quiz # 1 **May 13, 2019** **Adam Wilson**

Name: **Student #: _____ Signature: _____**

Time limit: 30 minutes. Calculators not allowed.

1. (3 marks) Using the attached data sheet for the SN5400 NAND gate, determine what the worst-case noise margin is when these NAND gates are interfaced together in a circuit.

2. (4 marks) Interface the switch to the input of the NAND gate and the LED to the output of the NAND gate such that the switch controls the LED. Assume that OUT 2 from the Lab Dev Board is currently a logic high. Make use of the provided data sheet for the SN5400 and use any necessary resistors. Note the forward voltage drop of the LED and the current required by the LED.



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3. The following 3 assembly language instructions have been used to set **OUT 2** to a logic high. Where register 2 holds the address of the output port (OUT 0 to OUT 7) and register 5 holds the value to be written to the outputs (ie: the 3rd bit from the right corresponds to OUT 2). Register 0 = 0x0000.

```
ori    r2, r0, 0x8880

ori    r5, r0, 0x0027 #set outputs 0, 1, 2, and 5 high, while outputs 3, 4, 6, and 7 are low

sthio  r5, 0(r2) # this will update the outputs with the value stored in register 5.
```

(4 marks) Write out the binary machine language for the second assembly language instruction:

(2 marks) Convert the binary machine language instruction to HEX:

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4. (2 marks) We must disable the switch from being able to activate the LED by setting OUT 2 low. Fill in the assembly language instruction below to update register 5 with the instruction and immediate value. The outputs must be updated so that only OUT 2 is changed (to low) while the other outputs are not affected.

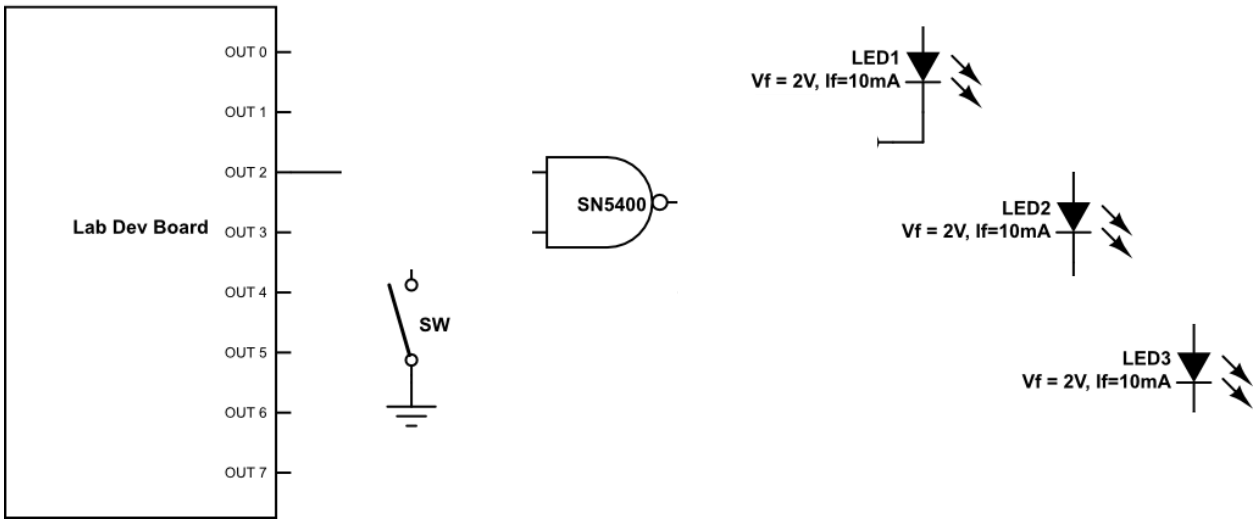
   _____ r5, r5, _____ # set output 2 low while not changing outputs 0, 1, 3, 4, 5, 6, and 7

   sthio r5, 0(r2) # this will update the outputs with the value stored in register 5.

BONUS mark: Using the remaining NAND gates in the SN5400 package, show how the circuit can be updated to allow the switch to control all 3 LEDs shown below.

NOTES:

- the switch must still be interfaced to the input of the SN5400 NAND gate and the LEDs must still be controlled by the output of the SN5400 NAND gate.
- OUT 2 is once again set to a logic high
- Additional resistors may be used if necessary.



ECE3221 – Quiz # 2 **May 21, 2019** **Adam Wilson**

Name: _ _ Student #: _____ Signature: _____

Time limit: 30 min. Calculators not allowed. All programming questions relate to the NIOS II processor.

1. (1 mark) Use an assembler directive to tell the assembler to begin placing binary values at memory address 0x00001200.

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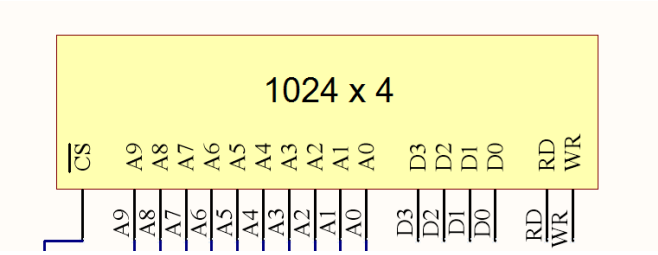
2. (2 marks) Explain why switch debouncing is necessary when interfacing real switches to digital circuits:

3. (3 marks) List the 3 pieces of information that must be provided to the CPU of a computer when giving an instruction in machine language or assembly language:

4. (5 marks) Draw and label a block diagram of a single port **1024x4** read write memory chip. Ensure that the memory chip includes **an active low chip select line, all address lines, all data lines, a read line, and a write line**. What is the storage capacity of this memory chip in bytes?



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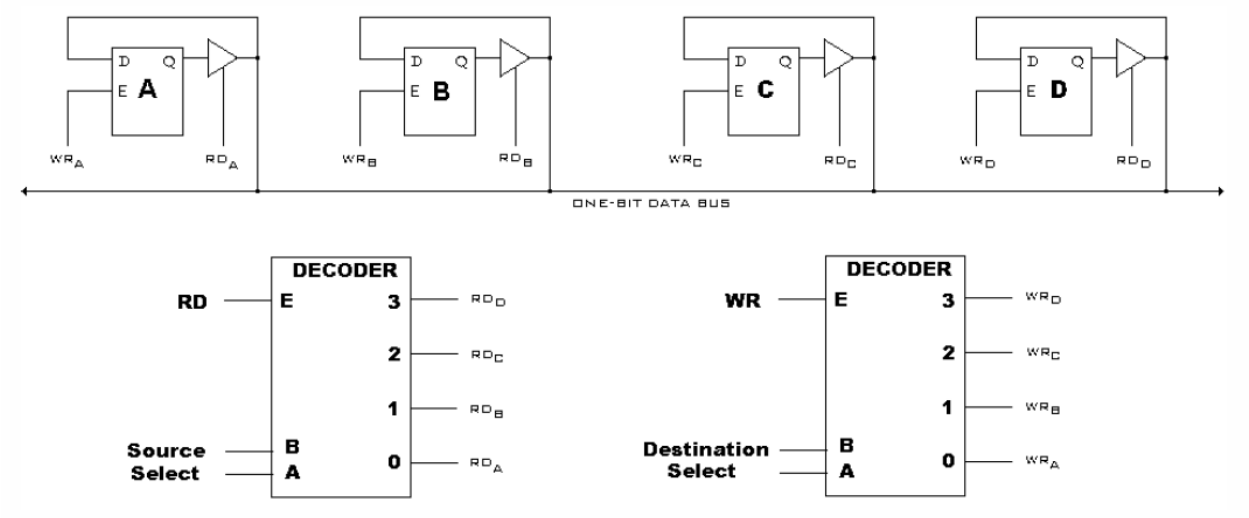
5. (7 marks) Given the circuit below, the value in the source register (B) is to be copied into a destination register (C) by specifying a two-bit address for each. Single read and write signals are directed to the appropriate one-bit registers. Label completely the timing diagram to perform the register transfer. Assume output Q_B is initially 0 and output Q_C is initially 1.



Source Address

Dest. Address

Q_B	1
	0
WR	1
	0
RD	1
	0
Q_C	1
	0
$DATA\ BUS$	1
	0

ECE3221 – Quiz # 3 **May 27, 2019** **Adam Wilson**

Name: _ Student #: _____ Signature: _____

Time limit: 30 min. Calculators not allowed. All programming questions relate to the NIOS II processor.

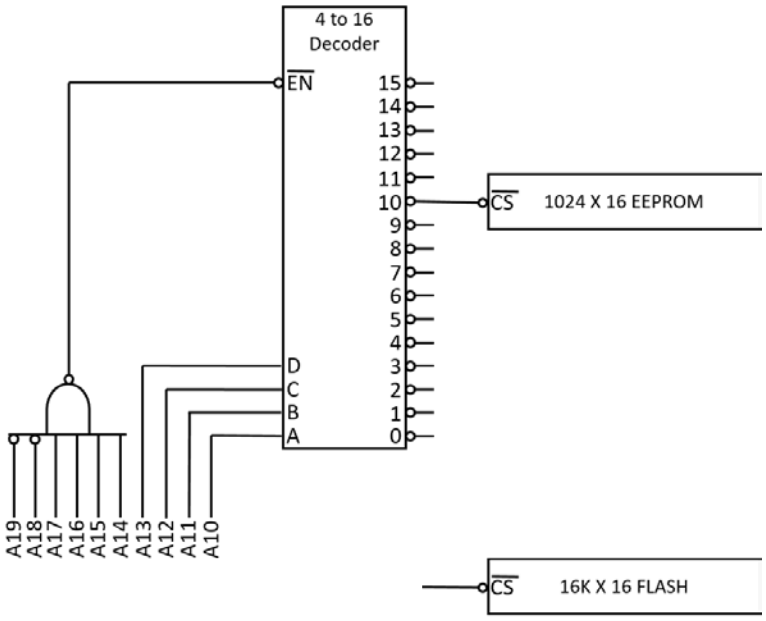
A computer system has a 20-bit address bus and a 16-bit data bus. Answer the next 4 questions related to the computer system:

1. (1 mark) What is the maximum number of memory locations that can be addressed by this system?

2. (1 mark) If the system addresses 2 bytes at a time (the width of the data bus), what is the maximum amount of memory storage, in bytes, that can be addressed by this system?

3. (5 marks) The following decoder circuit is used to decode 16 sub-sections of memory within the 20-bit memory space. Fill in the addresses in the memory map (shown on the next page) of the system with the starting and ending addresses of the total 20-bit memory space, the starting and ending addresses of the EEPROM and ending address of FLASH.

4. (2 marks) Draw another decoding circuit, on the figure below, to locate the FLASH at the location shown in the memory map (starting at 0x08000).



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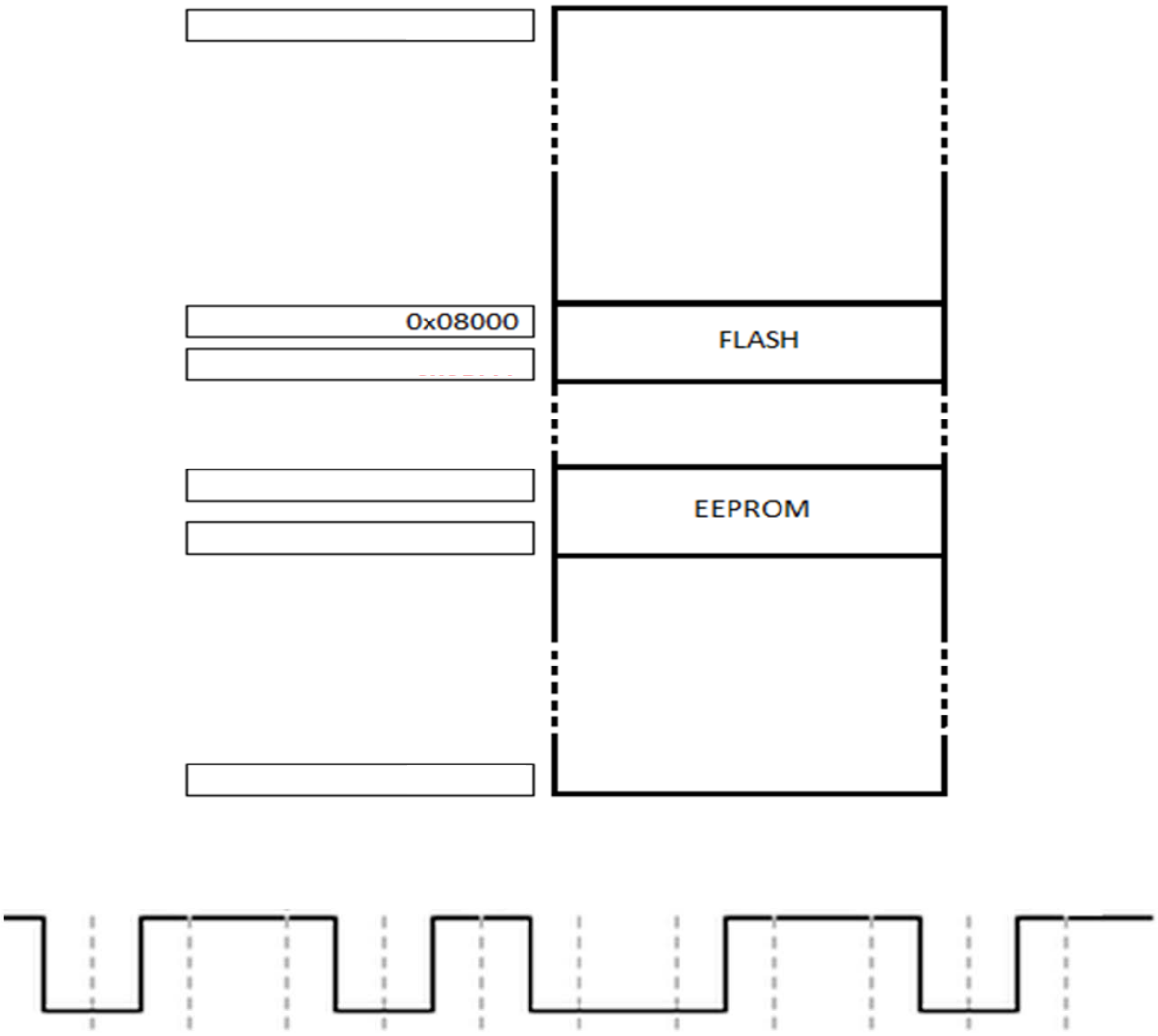

Figure 1 - Asynchronous transmission of 8 data bits

5. (2 marks) Figure 1 shows the timing diagram for an asynchronous RS232 data transmission with a data size of 8 bits. What is the value of the data byte being transmitted in **hex**?

6. (1 mark) What type of parity is being used in the data transmission in Figure 1 (assume no errors in the data)?

7. (1 mark) If the duration of each bit is 10µs in Figure 1, what is the data rate of the transmission in **bit/s**?

ECE3221 – Quiz # 4 **June 3, 2019** **Adam Wilson**

Name: Student #: _____ Signature: _____

Time limit: 30 min. Calculators not allowed. All programming questions relate to the NIOS II processor.

1. (4 marks) Complete the table below with the signed 8-bit binary values indicated.

Signed Decimal Value	Sign and Magnitude (8-bit)	2's Complement (8-bit)
+31		
-31		
+65		
-65		

2. (1 mark) A technique used to improve the efficiency of input (or output) operations of computer system by allowing writes (or reads) to (or from) memory directly without continual CPU interaction is called:

3. (1 mark) This unit serves as the interface between the processor and the computer buses of a computer. It initiates read and write operations by manipulating the address and control lines. What is this unit called?

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4. (2 marks) Show the assembly language instruction(s) required to convert an ASCII character that is stored in r8 to uppercase.

5. (3 marks) When a subroutine is called from the main program code using the **call** instruction, the processor branches to the area of memory where the subroutine is stored by updating the program counter with the address of the subroutine. Explain how the processor is redirected to continue to execute the instructions that follow the call instruction in the main program code following completion of the subroutine. Discuss the instruction(s) required and the registers involved:

6. (4 marks) Describe what the stack is in a computer program and how it may be used. List 2 common operations that are used to access the stack and describe the purpose of these operations.

ECE3221 – Quiz # 5 **June 10, 2019** **Adam Wilson**

Name: _____ Student #: _____ Signature: _____

Time limit: 60 min. Calculators not allowed. All programming questions relate to the NIOS II processor.

1. (2 marks) Explain the difference between interrupts and polling.

2. (2 mark) What is an interrupt vector table and does the NIOS II processor have one?

3. (5 marks) List (in sequence) the 5 events that occur when an interrupt is generated and acknowledged on the NIOS II processor:

4. (1 mark) What is the name of the subroutine that is executed when an interrupt occurs?

5. (1 mark) The **eret** instruction is used to return from the interrupt "subroutine". What must first be done to ensure that the NIOS II processor returns to the proper instruction?

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6. (1 mark) What does the term **interrupt latency** refer to?

7. (4 marks) Using a conditional branch instruction, write the assembly code to repeat a block of code 5 times. The code needs to initially store a value in register r6 and then loop through decrementing that value and repeating the loop until the value in r6 is zero (include comments):

8. (4 marks) Write assembly language code to accomplish each of the following *separate* tasks described in C-Language. Maximum 3 lines of code for each part.

unsigned char mycode [4] = {3,2,0,1};

d = d * 0.75; // assume r7 is the value of unsigned integer d
Do not use the multiply or divide instruction in this answer. No loops allowed.

ECE3221 – Quiz # 6 **June 17, 2019** **Adam Wilson**

Name: _____ Student #: _____ Signature: _____

Time limit: 60 min. Calculators not allowed. All programming questions relate to the NIOS II processor.

1. (2 marks) Use logic gates to design a 2 to 1 multiplexer. Label inputs: ***A***, ***B***, and ***SELECT*** and output:
   Y?

2. (5 marks) Draw and label the diagram of a single port **256x8** read write memory chip. Ensure that the memory chip includes **an active low chip select line, all address lines, all data lines, a read line and a write line**. The memory is to be interfaced to a system with a **16-bit address space (use a NAND gate to perform the address decoding)** and this block of memory is to span the address range **0x1F00 to 0x1FFF**.

ECE3221 – Quiz # 6 **June 17, 2019** **Adam Wilson**

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3. (1 mark) A faster clock speed translates into a faster computer. Give one example of a limitation that may prevent the clock speed of a computer from being increased to 10x the normal clock rate.

4. (1 mark) Write a single line of assembly code to divide the **signed** value stored in register r4 by 16 and store the result in register r5 using a shift instruction:

5. (1 mark) Convert the following decimal value to BCD (show result in binary):

   94058390_{10} =

6. (5 marks) In the lab you see the following program listing. Carefully examine this listing and answer the questions that follow. *Each question refers to a specific line in the listing*

```
.EQU STORAGE, 0x00001000
# ===== start of code =====
        movia   r6, Y           #line 1
        stw     r6, 0(r6)       #line 2
        or      r6, r0, r0      #line 3
# ===== more code here=====
.ORG STORAGE
W:    .word  9, 8, 7
X:    .half 6, 5
Y:    .skip 4
```

   a) The instruction at line 1 (movia) is an alias for what instruction(s)?

   b) What binary instruction is generated by the assembler for the instruction at line 3?

   c) What value is stored by the instruction at line 2 (assuming line 1 has already executed)?

   d) What is the purpose of the instruction at line 3?

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7. (5 marks) In each of the separate C-language code segments below, give the final value of a.

unsigned int a=1, b=2; if(!b) a++;	a =

unsigned int a=4, b=2;
while(b) b = 3;
a = 0;
	a =

unsigned int a=3, *b;
b = &a;
*b = 0;
	a =

unsigned int a;
a = 5;
a = a | 0x0010;
	a =

unsigned int a=3, b=8; while(b){b = b>>1; a++;}	a =

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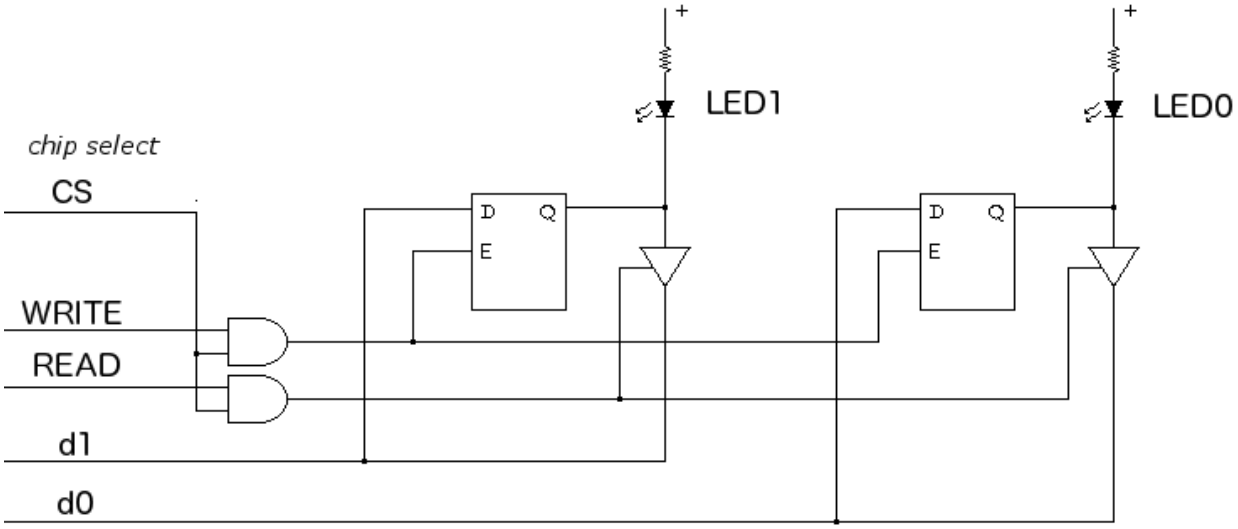
8. (5 marks) Draw a timing diagram showing the signals (CS, WRITE, READ, d1, and d0) as the following sequence of events occurs:

   - Assume both LEDs are off to start and all five signals are zero
   - LED1 is turned on while LED0 is turned off
   - The data bus (d1 and d0) is used to communicate data to other components not shown
   - LED0 is turned on while LED1 is turned off
   - Both LEDs are turned off
   - At end of timing diagram the state of both LEDs is put onto the data bus



CS

WRITE

READ

d1

d0