ECE3221 – Quiz # 6 **June 14, 2018** **Adam Wilson**

Name: __SOLUTIONS_____ Student #: _____ Signature: _____

Calculators not allowed. All programming questions refer to the NIOS II processor.

1. (4 marks)

Complete the bitwise logical XOR of the two 16 bit values shown below and fill in the right hand columns with the equivalent hex value																	hex			
1	1	0	1	0	1	1	1	0	0	1	1	1	0	1	0	=	D	7	3	A
0	1	1	0	1	0	1	0	1	1	1	0	0	0	1	1	=	6	A	E	3
1	0	1	1	1	1	0	1	1	1	0	1	1	0	0	1	=	B	D	D	9

Complete the bitwise logical NAND of the two 15 bit values shown below and fill in the right hand columns with the equivalent octal value																octal				
0	0	1	0	1	1	1	0	1	0	0	1	1	1	0	=	1	3	5	1	6
1	0	1	0	1	1	1	1	1	0	0	1	0	1	0	=	5	3	7	1	2
1	1	0	1	0	0	0	1	0	1	1	0	1	0	1	=	6	4	2	6	5

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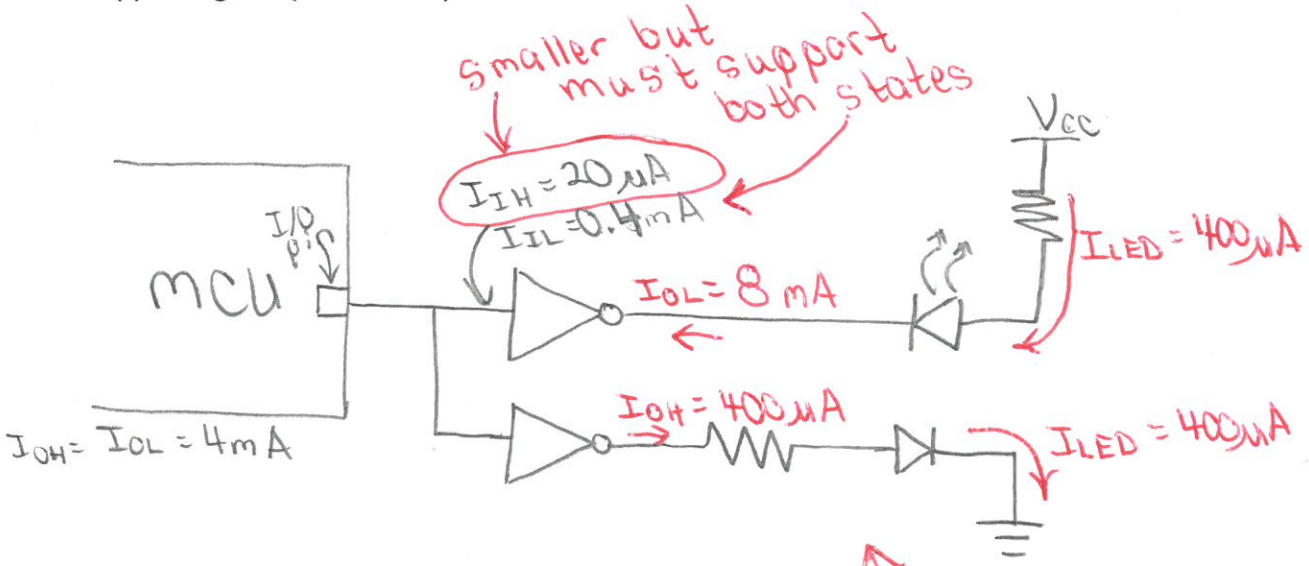
2. (6 marks) Assume a single standard I/O pin of a dsPIC33FH128GP802 microcontroller is used to control a large number of LEDs through an SN74LS04 logic inverter (one LED is connected to the output of each logic inverter and the inputs of all logic inverters are connected together and to a single I/O pin of the microcontroller). What is the maximum number of LEDs that can be controlled (the LEDs require 400µA each when on to be sufficient bright)?

See below.

Draw a subset of the circuit showing the I/O port, 2 logic inverters, 2 LEDs and any supporting components required.



$$Fanout = \frac{I_{OL}}{I_{IL}} = \frac{4mA}{0.4mA} = 10$$

$$Fanout = \frac{I_{OH}}{I_{IH}} = \frac{4mA}{20\mu A} = 200$$

must select smaller of the two

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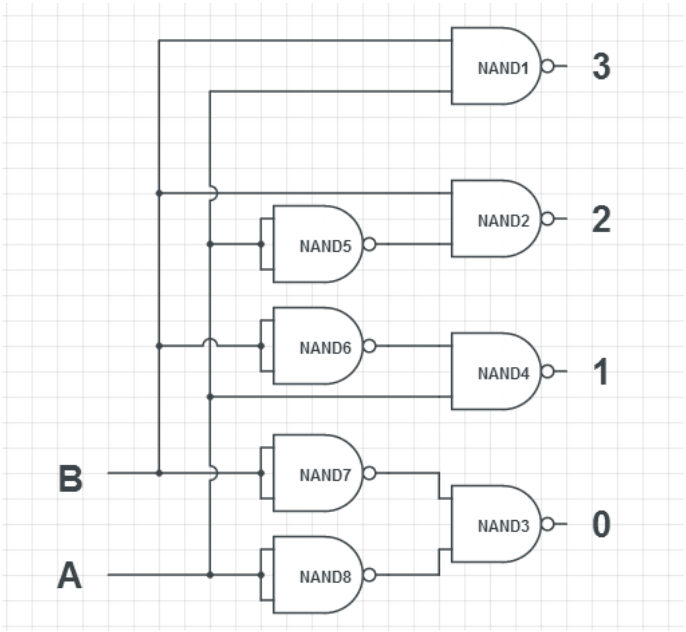
3. (1 mark) Using any number of 2-input NAND gates (and only 2-input NAND gates), show the connections to create a 2 to 4 decoder with active low outputs.

Input		Outputs			
A	**B**	**3**	**2**	**1**	**0**
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1



4. (1 mark) What must be done to ensure that nested calls and recursive subroutines are able to return to the main program properly?

Push the **ra** register to the stack at the beginning of the subroutine and **pop** it before the ret statement

5. (3 marks) How many address lines and how many data lines does a 1M x 4 memory chip have? What is the storage capacity of this memory chip in **bytes**?

# of Address Lines: ___20_____

# of Data Lines: _____4_____

Storage capacity: _____0.5 Mbytes or 512 kBytes or 524288 bytes_____

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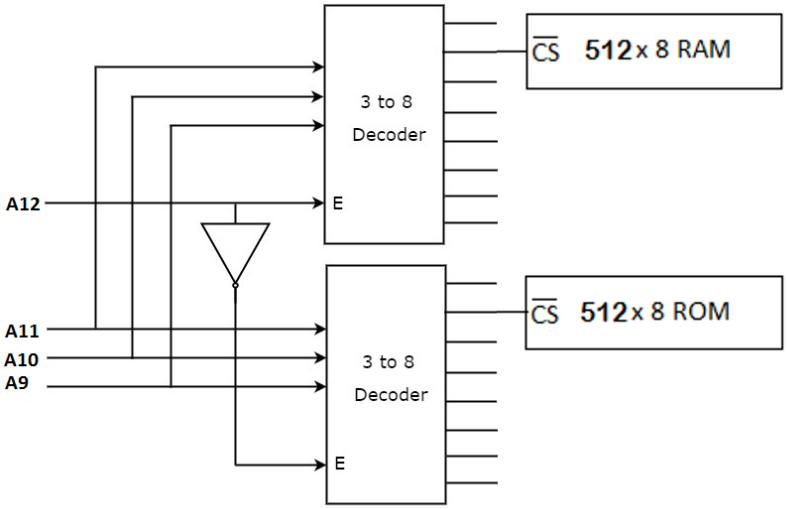
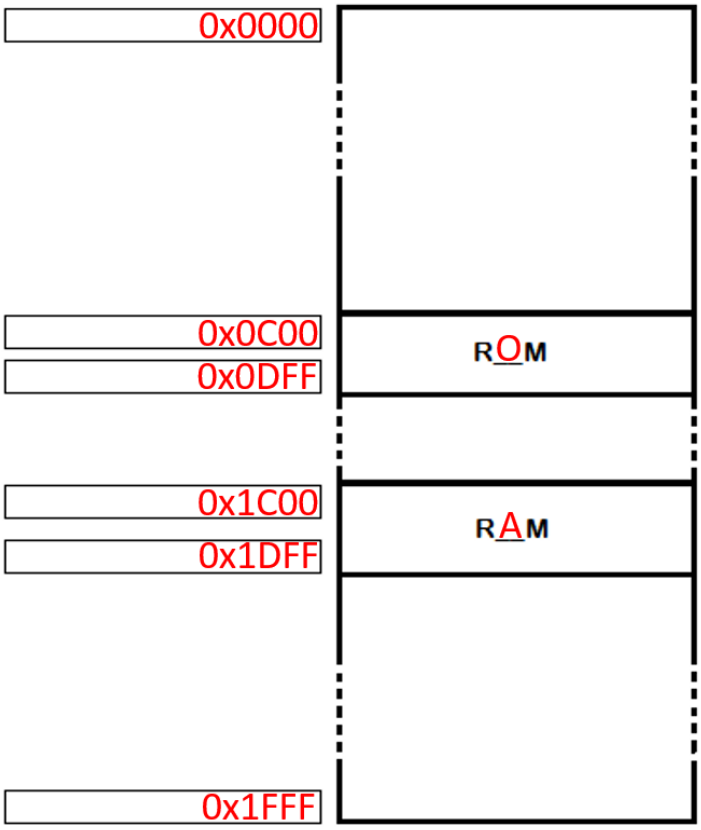
6. (7 marks) The following decoder circuit is used to decode 16 sections of memory within a 13-bit memory space. Fill in the addresses in the memory map of the system shown below with the starting and ending addresses of the total 13-bit memory space and starting and ending addresses of the RAM and ROM. Also fill in the blank to label which block is RAM and which is ROM.





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7. (5 marks) In each of the separate C-language code segments below, give the final value of a.

unsigned int a=1, b=2; if(!b) a++;	a = 1

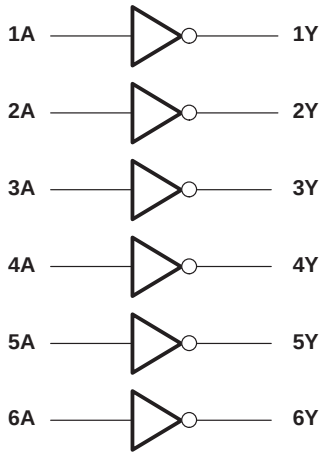
unsigned int a=4, b=2;
while(b) b = 3;
a = 0;
	a = 4

unsigned int a=3, *b;
b = &a;
*b = 0;
	a = 0

unsigned int a;
a = 5;
a = a | 0x0010;
	a = 0x15 = 21

unsigned int a=3, b=8; while(b){b = b>>1; a++;}	a = 7

logic diagram (positive logic)



$Y = \overline{A}$

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN5404 SN7404			UNIT
				MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 400 Ω, C_L = 15 pF		12	22	ns
t_{PHL}					8	15	

recommended operating conditions (see Note 3)

		SN54LS04			SN74LS04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS04			SN74LS04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4			0.4	V
			I_{OL} = 8 mA					0.25	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			1.2	2.4		1.2	2.4	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			3.6	6.6		3.6	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS04 SN74LS04			UNIT
				MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 electrical characteristics. Additional information is provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 family are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings(1)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +160°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to V_{SS}(4) ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 3.0V$(4) ..... -0.3V to +5.6V
Voltage on any 5V tolerant pin with respect to Vss when $V_{DD} < 3.0V$(4) ..... -0.3V to 3.6V
Voltage on V_{CAP} with respect to V_{SS} ..... 2.25V to 2.75V
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin(2) ..... 250 mA
Maximum output current sunk by any I/O pin(3) ..... 4 mA
Maximum output current sourced by any I/O pin(3) ..... 4 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports(2) ..... 200 mA

Note 1: Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

3: Exceptions are CLKOUT, which is able to sink/source 25 mA, and the V_{REF+}, V_{REF-}, SCLx, SDAx, PGECx and PGEDx pins, which are able to sink/source 12 mA.

4: See the **"Pin Diagrams"** section for 5V tolerant pins.