ECE3221 – Quiz # 1 **May 13, 2019** **Adam Wilson**

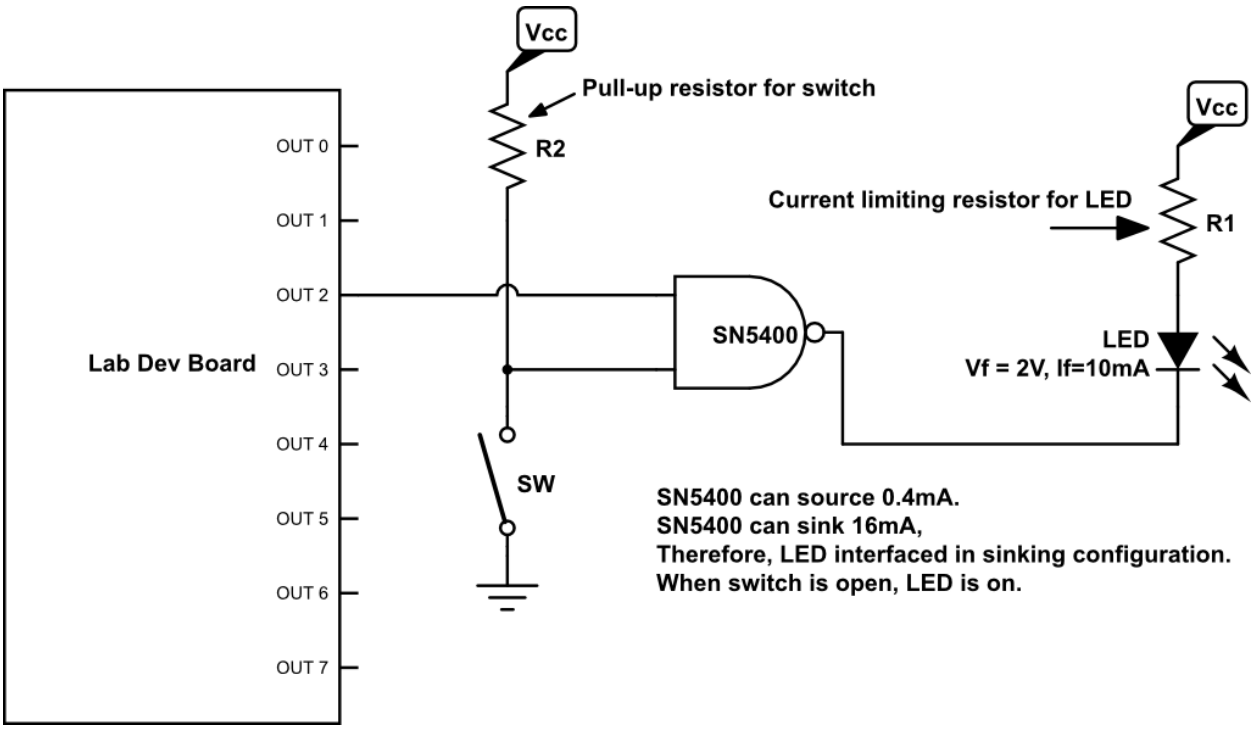
Name: SOLUTIONS Student #: _____ Signature: _____

Time limit: 30 minutes. Calculators not allowed.

1. (3 marks) Using the attached data sheet for the SN5400 NAND gate, determine what the worst-case noise margin is when these NAND gates are interfaced together in a circuit.

$V_{OH} - V_{IH} = 2.4V - 2V = 0.4V$ and $V_{IL} - V_{OL} = 0.8V - 0.4V = 0.4V$, therefore worst- case noise margin is 0.4V

2. (4 marks) Interface the switch to the input of the NAND gate and the LED to the output of the NAND gate such that the switch controls the LED. Assume that OUT 2 from the Lab Dev Board is currently a logic high. Make use of the provided data sheet for the SN5400 and use any necessary resistors. Note the forward voltage drop of the LED and the current required by the LED.



Name: SOLUTIONS Student #: _____ Signature: _____

3. The following 3 assembly language instructions have been used to set **OUT 2** to a logic high. Where register 2 holds the address of the output port (OUT 0 to OUT 7) and register 5 holds the value to be written to the outputs (ie: the 3rd bit from the right corresponds to OUT 2). Register 0 = 0x0000.

   ori r2, r0, 0x8880

   ori r5, r0, 0x0027 #set outputs 0, 1, 2, and 5 high, while outputs 3, 4, 6, and 7 are low

   sthio r5, 0(r2) # this will update the outputs with the value stored in register 5.

(4 marks) Write out the binary machine language for the second assembly language instruction:

Referring to the provided Table 8-1:

OP of ori = 0x14, rA = r0, rB = r5, and IMM16 = 0x0027, therefore the binary machine language instruction is:

5 bits	5bits	16 bits	6 bits
rA	rB	IMM16	OP
00000	00101	0000000000100111	010100

(2 marks) Convert the binary machine language instruction to HEX:

Binary Machine Language Instruction: 0000 0001 0100 0000 0000 1001 1101 0100

Machine langue instruction in HEX: 0x014009D4

Name: SOLUTIONS Student #: _____ Signature: _____

4. (2 marks) We must disable the switch from being able to activate the LED by setting OUT 2 low. Fill in the assembly language instruction below to update register 5 with the instruction and immediate value. The outputs must be updated so that only OUT 2 is changed (to low) while the other outputs are not affected.

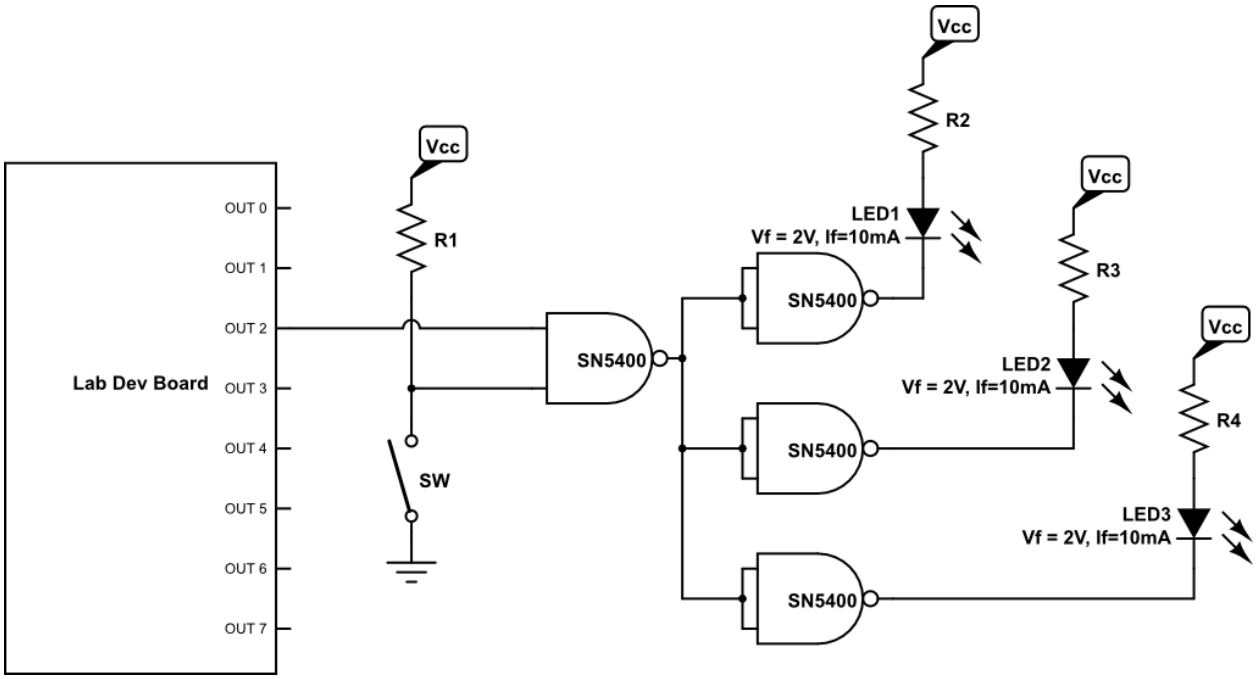
   andi r5, r5, 0xFFFB # set output 2 low while not changing outputs 0, 1, 3, 4, 5, 6, and 7

   sthio r5, 0(r2) # this will update the outputs with the value stored in register 5.

BONUS mark: Using the remaining NAND gates in the SN5400 package, show how the circuit can be updated to allow the switch to control all 3 LEDs shown below.

NOTES:

- the switch must still be interfaced to the input of the SN5400 NAND gate and the LEDs must still be controlled by the output of the SN5400 NAND gate.
- OUT 2 is once again set to a logic high
- Additional resistors may be used if necessary.
- There are a total of 4 NAND gates in an SN5400.



TEXAS INSTRUMENTS

SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00

SDLS025D – DECEMBER 1983 – REVISED MAY 2017

SNx400, SNx4LS00, and SNx4S00 Quadruple 2-Input Positive-NAND Gates

1 Features

- Package Options Include:
  - Plastic Small-Outline (D, NS, PS)
  - Shrink Small-Outline (DB)
  - Ceramic Flat (W)
  - Ceramic Chip Carriers (FK)
  - Standard Plastic (N)
  - Ceramic (J)
- Also Available as Dual 2-Input Positive-NAND Gate in Small-Outline (PS) Package
- Inputs Are TTL Compliant; V_{IH} = 2 V and V_{IL} = 0.8 V
- Inputs Can Accept 3.3-V or 2.5-V Logic Inputs
- SN5400, SN54LS00, and SN54S00 are Characterized For Operation Over the Full Military Temperature Range of –55ºC to 125ºC

2 Applications

- AV Receivers
- Portable Audio Docks
- Blu-Ray Players
- Home Theater
- MP3 Players or Recorders
- Personal Digital Assistants (PDAs)

3 Description

The SNx4xx00 devices contain four independent, 2-input NAND gates. The devices perform the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LS00DB	SSOP (14)	6.20 mm × 5.30 mm
SN7400D, SN74LS00D, SN74S00D	SOIC (14)	8.65 mm × 3.91 mm
SN74LS00NSR	PDIP (14)	19.30 × 6.35 mm
SNJ5400J, SNJ54LS00J, SNJ54S00J	CDIP (14)	19.56 mm × 6.67 mm
SNJ5400W, SNJ54LS00W, SNJ54S00W	CFP (14)	9.21 mm × 5.97 mm
SN54LS00FK, SN54S00FK	LCCC (20)	8.89 mm × 8.89 mm
SN7400NS, SN74LS00NS, SN74S00NS	SO (14)	10.30 mm × 5.30 mm
SN7400PS, SN74LS00PS	SO (8)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram, Each Gate (Positive Logic)

Pin Functions (continued)

PIN					I/O	DESCRIPTION
NAME	CDIP, CFP, SOIC, PDIP, SO, SSOP	SO (SN74xx00)	CFP (SN5400)	LCCC		
3Y	8	—	8	12	O	Gate 3 output
4A	13	—	12	18	I	Gate 4 input
4B	12	—	13	19	I	Gate 4 input
4Y	11	—	14	16	O	Gate 4 output
GND	7	4	11	10	—	Ground
NC	—	—	—	1, 5, 7, 11, 15, 17	—	No connect
V_{CC}	14	8	4	20	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}(2)			7	V
Input voltage	SNx400 and SNxS400		5.5	V
	SNx4LS00		7	
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to network ground terminal.

6.2 ESD Ratings: SN74LS00

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance. ESD Tested on SN74LS00N package.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	SN54xx00	4.5	5	5.5	V
		SN74xx00	4.75	5	5.25	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage	SNx400, SN7LS400, and SNx4S00			0.8	V
		SN54LS00			0.7	
I_{OH}	High-level output current	SN5400, SN54LS00, and SN74LS00			–0.4	mA
		SNx4S00			–1	
I_{OL}	Low-level output current	SNx400			16	mA
		SN5LS400			4	
		SN7LS400			8	
		SNx4S00			20	

6.4 Thermal Information

THERMAL METRIC[1][2]		SN74LS00				UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.9	102.8	54.8	89.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	53.3	42.1	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48	53.4	34.8	50.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.6	16.5	26.9	16.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.8	52.9	34.7	49.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics: SNx400

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = MIN and I_I = –12 mA				–1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, and I_{OH} = –0.4 mA		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, and I_{OL} = 16 mA			0.2	0.4	V
I_I	V_{CC} = MAX and V_I = 5.5 V				1	mA
I_{IH}	V_{CC} = MAX and V_I = 2.4 V				40	µA
I_{IL}	V_{CC} = MAX and V_I = 0.4 V				–1.6	mA
I_{OS}	V_{CC} = MAX	SN5400	–20		–55	mA
		SN7400	–18		–55	
I_{CCH}	V_{CC} = MAX and V_I = 0 V			4	8	mA
I_{CCL}	V_{CC} = MAX and V_I = 4.5 V			12	22	mA

6.6 Electrical Characteristics: SNx4LS00

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = MIN and I_I = –18 mA				–1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = MAX, and I_{OH} = –0.4 mA		2.5	3.4		V
V_{OL}	V_{CC} = MIN and V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4	V
		I_{OL} = 8 mA (SN74LS00)		0.35	0.5	
I_I	V_{CC} = MAX and V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = MAX and V_I = 2.7 V				20	µA
I_{IL}	V_{CC} = MAX and V_I = 0.4 V				–0.4	mA
I_{OS}	V_{CC} = MAX		–20		–100	mA
I_{CCH}	V_{CC} = MAX and V_I = 0 V			0.8	1.6	mA
I_{CCL}	V_{CC} = MAX and V_I = 4.5 V			2.4	4.4	mA

6.7 Electrical Characteristics: SNx4S00

over operating free-air temperature range (unless otherwise noted)

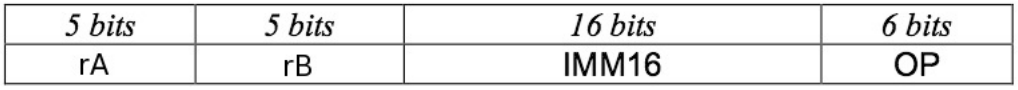
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = MIN and I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, and I_{OH} = –1 mA	2.5	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, and I_{OL} = 20 mA			0.5	V
I_I	V_{CC} = MAX and V_I = 5.5 V			1	mA
I_{IH}	V_{CC} = MAX and V_I = 2.7 V			50	µA
I_{IL}	V_{CC} = MAX and V_I = 0.5 V			–2	mA

Category	Instruction		Meaning
Arithmetic	**addi**	rB, rA, imm	rB ← rA + imm_s
	add	rC, rA, rB	rC ← rA + rB
	sub	rC, rA, rB	rC ← rA − rB
Logical	**and**	rC, rA, rB	rC ← rA *and* rB
	andi	rB, rA, imm	rB ← rA *and* imm_u
	or	rC, rA, rB	rC ← rA *or* rB
	ori	rB, rA, imm	rB ← rA *or* imm_u
	xor	rC, rA, rB	rC ← rA *xor* rB
	xori	rB, rA, imm	rB ← rA *xor* imm_u
	nor	rC, rA, rB	rC ← rA *nor* rB
Comparator	**cmpgei**	rB, rA, imm	rB ← (rA ≥ imm_s)? 1 : 0
	cmplti	rB, rA, imm	rB ← (rA < imm_s)? 1 : 0
	cmpnei	rB, rA, imm	rB ← (rA ≠ imm_s)? 1 : 0
	cmpeqi	rB, rA, imm	rB ← (rA = imm_s)? 1 : 0
	cmpgeui	rB, rA, imm	rB ← (rA_u ≥ imm_u)? 1 : 0
	cmpltui	rB, rA, imm	rB ← (rA_u < imm_u)? 1 : 0
	cmpge	rC, rA, rB	rC ← (rA ≥ rB)? 1 : 0
	cmplt	rC, rA, rB	rC ← (rA < rB)? 1 : 0
	cmpne	rC, rA, rB	rC ← (rA ≠ rB)? 1 : 0
	cmpeq	rC, rA, rB	rC ← (rA = rB)? 1 : 0
	cmpgeu	rC, rA, rB	rC ← (rA_u ≥ rB_u)? 1 : 0
	cmpltu	rC, rA, rB	rC ← (rA_u < rB_u)? 1 : 0
Shift	**sll**	rC, rA, rB	rC ← rA ≪ $\text{rB}_{4..0}$
	slli	rC, rA, imm	rC ← rA ≪ $\text{imm}_{4..0}$
	srl	rC, rA, rB	rC ← rA_u ≫ $\text{rB}_{4..0}$
	srli	rC, rA, imm	rC ← rA_u ≫ $\text{imm}_{4..0}$
	sra	rC, rA, rB	rC ← rA_s ≫ $\text{rB}_{4..0}$
	srai	rC, rA, imm	rC ← rA_s ≫ $\text{imm}_{4..0}$
	rol	rC, rA, rB	rC ← rA *rol* $\text{rB}_{4..0}$
	ror	rC, rA, rB	rC ← rA *ror* $\text{rB}_{4..0}$
	roli	rC, rA, imm	rC ← rA *rol* $\text{imm}_{4..0}$
Memory	**ldw**	rB, imm (rA)	rB ← MEM[imm_s+rA]
	stw	rB, imm (rA)	MEM[imm_s+rA] ← rB
Branch	**br**	imm	goto PC+4+imm_s
	bge	rA, rB, imm	if (rA ≥ rB) goto PC+4+imm_s
	blt	rA, rB, imm	if (rA < rB) goto PC+4+imm_s
	bne	rA, rB, imm	if (rA ≠ rB) goto PC+4+imm_s
	beq	rA, rB, imm	if (rA = rB) goto PC+4+imm_s
	bgeu	rA, rB, imm	if (rA_u ≥ rB_u) goto PC+4+imm_s
	bltu	rA, rB, imm	if (rA_u < rB_u) goto PC+4+imm_s
Jump	**call**	imm	goto imm ≪ 2; ra ← PC+4
	callr	rA	goto rA; ra ← PC+4
	ret		goto ra
	jmp	rA	goto rA
	jmpi	imm	goto imm ≪ 2
Misc	**break**		stops the processor[2]

[2]This is not the official function of the instruction.

Table 8–1. OP Encodings

OP	Instruction	OP	Instruction	OP	Instruction	OP	Instruction
0x00	call	0x10	cmplti	0x20	cmpeqi	0x30	cmpltui
0x01		0x11		0x21		0x31	
0x02		0x12		0x22		0x32	custom
0x03	ldbu	0x13		0x23	ldbuio	0x33	initd
0x04	addi	0x14	ori	0x24	muli	0x34	orhi
0x05	stb	0x15	stw	0x25	stbio	0x35	stwio
0x06	br	0x16	blt	0x26	beq	0x36	bltu
0x07	ldb	0x17	ldw	0x27	ldbio	0x37	ldwio
0x08	cmpgei	0x18	cmpnei	0x28	cmpgeui	0x38	
0x09		0x19		0x29		0x39	
0x0A		0x1A		0x2A		0x3A	R-Type
0x0B	ldhu	0x1B	flushda	0x2B	ldhuio	0x3B	flushd
0x0C	andi	0x1C	xori	0x2C	andhi	0x3C	xorhi
0x0D	sth	0x1D		0x2D	sthio	0x3D	
0x0E	bge	0x1E	bne	0x2E	bgeu	0x3E	
0x0F	ldh	0x1F		0x2F	ldhio	0x3F	



ori

bitwise logical or immediate

Operation: rB ← rA | (0x0000 : IMM16)

Assembler Syntax: `ori rB, rA, IMM16`

Example: `ori r6, r7, 100`

Description: Calculates the bitwise logical OR of rA and (0x0000 : IMM16) and stores the result in rB.

Table 8–2. OPX Encodings for R-Type Instructions

OPX	Instruction	OPX	Instruction	OPX	Instruction	OPX	Instruction
0x00		0x10	cmplt	0x20	cmpeq	0x30	cmpltu
0x01	eret	0x11		0x21		0x31	add
0x02	roli	0x12	slli	0x22		0x32	
0x03	rol	0x13	sll	0x23		0x33	
0x04	flushp	0x14		0x24	divu	0x34	break
0x05	ret	0x15		0x25	div	0x35	
0x06	nor	0x16	or	0x26	rdctl	0x36	sync
0x07	mulxuu	0x17	mulxsu	0x27	mul	0x37	
0x08	cmpge	0x18	cmpne	0x28	cmpgeu	0x38	
0x09	bret	0x19		0x29	initi	0x39	sub
0x0A		0x1A	srli	0x2A		0x3A	srai
0x0B	ror	0x1B	srl	0x2B		0x3B	sra
0x0C	flushi	0x1C	nextpc	0x2C		0x3C	
0x0D	jmp	0x1D	callr	0x2D	trap	0x3D	
0x0E	and	0x1E	xor	0x2E	wrctl	0x3E	
0x0F		0x1F	mulxss	0x2F		0x3F	

5 bits	*5 bits*	*5 bits*	*6 bits*	*5 bits*	*6 bits*
rA	rB	rC	OPX	IMM5	0x3A

or

bitwise logical or

Operation: rC ← rA | rB

Assembler Syntax: `or rC, rA, rB`

Example: `or r6, r7, r8`

Description: Calculates the bitwise logical OR of rA and rB and stores the result in rC.