Name: **Student #:** _____ **Signature:** _____

Time limit: 30 minutes. Calculators not allowed.

1. (3 marks) Using the attached data sheet for the SN5400 NAND gate, determine what the worst-case noise margin is when these NAND gates are interfaced together in a circuit.

2. (4 marks) Interface the switch to the input of the NAND gate and the LED to the output of the NAND gate such that the switch controls the LED. Assume that OUT 2 from the Lab Dev Board is currently a logic high. Make use of the provided data sheet for the SN5400 and use any necessary resistors. Note the forward voltage drop of the LED and the current required by the LED.
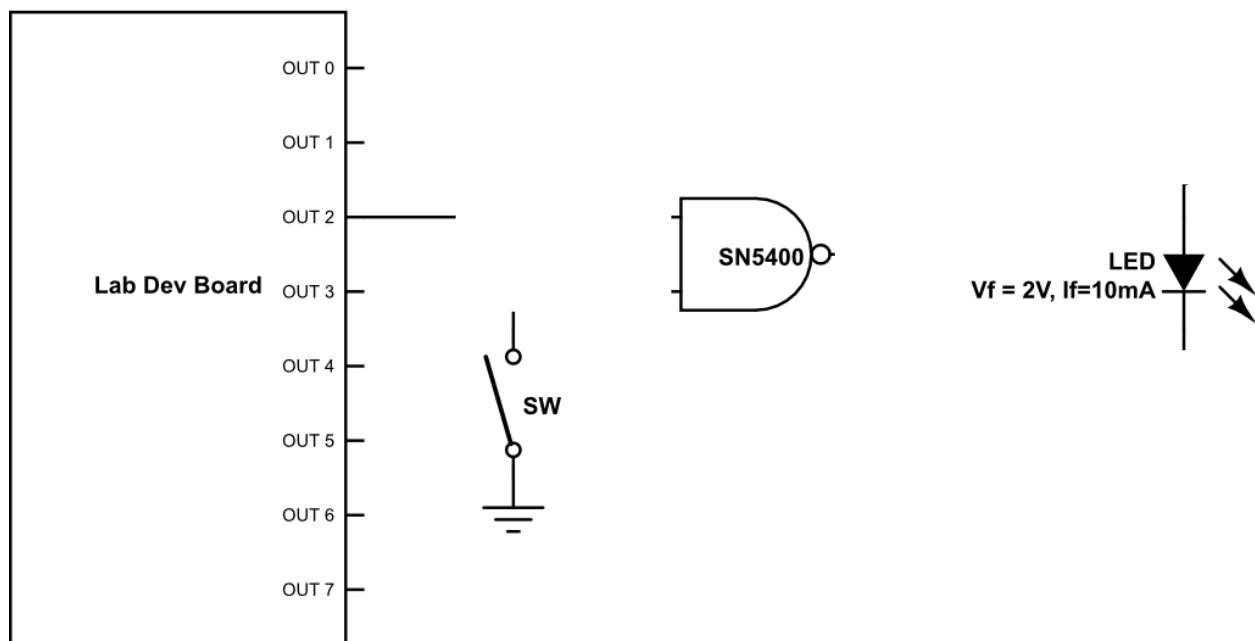
Name: Student #: _____ Signature: _____

3. The following 3 assembly language instructions have been used to set **OUT 2** to a logic high. Where register 2 holds the address of the output port (OUT 0 to OUT 7) and register 5 holds the value to be written to the outputs (ie: the 3rd bit from the right corresponds to OUT 2). Register 0 = 0x0000.

    ori   r2, r0, 0x8880

    ori   r5, r0, 0x0027 #set outputs 0, 1, 2, and 5 high, while outputs 3, 4, 6, and 7 are low

    sthio r5, 0(r2) # this will update the outputs with the value stored in register 5.

(4 marks) Write out the binary machine language for the second assembly language instruction:

 (2 marks) Convert the binary machine language instruction to HEX:

Name: **Student #:** _____ **Signature:** _____

4. (2 marks) We must disable the switch from being able to activate the LED by setting OUT 2 low. Fill in the assembly language instruction below to update register 5 with the instruction and immediate value. The outputs must be updated so that only OUT 2 is changed (to low) while the other outputs are not affected.

    _____ r5, r5, _____ # set output 2 low while not changing outputs 0, 1, 3, 4, 5, 6, and 7

    sthio r5, 0(r2) # this will update the outputs with the value stored in register 5.

BONUS mark: Using the remaining NAND gates in the SN5400 package, show how the circuit can be updated to allow the switch to control all 3 LEDs shown below.

NOTES:

- the switch must still be interfaced to the input of the SN5400 NAND gate and the LEDs must still be controlled by the output of the SN5400 NAND gate.

- OUT 2 is once again set to a logic high

- Additional resistors may be used if necessary.