ECE3221 – Quiz # 1 **May 10, 2017** **Adam Wilson**

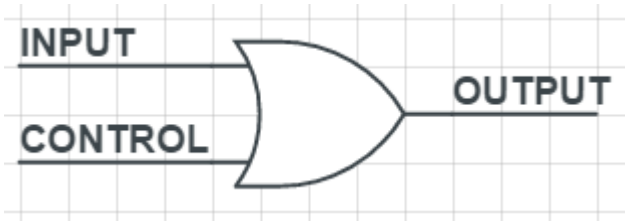
Name: ____Solutions_____ Student #: _____ Signature: _____

Calculators not allowed

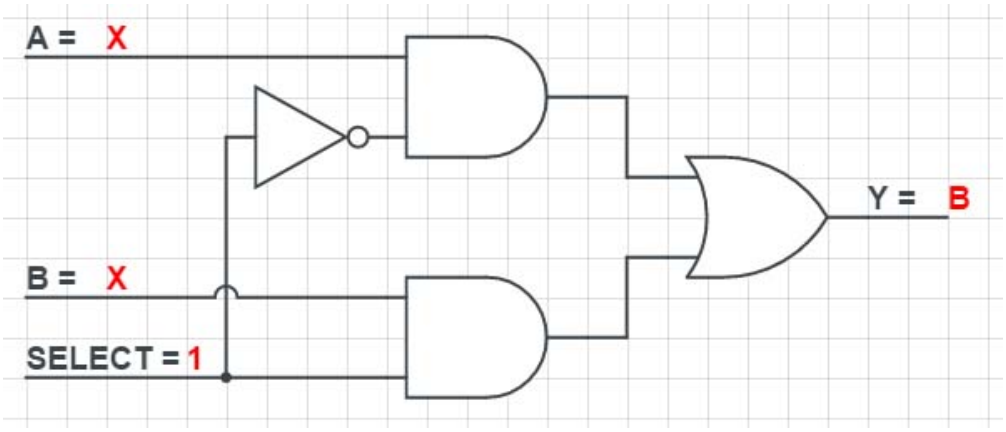
1. (4 marks) Complete the table below by converting each of the supplied 8-bit numbers to the base shown.

Value	Binary	Octal	Decimal	Hexadecimal
10011011_2	10011011_2	233_8	155_{10}	$9B_{16}$
357_8	11101111_2	357_8	239_{10}	EF_{16}
255_{10}	11111111_2	377_8	255_{10}	FF_{16}
$8F_{16}$	10001111_2	217_8	143_{10}	$8F_{16}$

2. (1 mark) Draw a logic gate that uses the input signal: ***CONTROL*** to determine if the input signal: ***INPUT*** is allowed to pass to the output signal: ***OUTPUT***. When ***CONTROL*** is low ***OUTPUT = INPUT***, when ***CONTROL*** is high ***OUTPUT = 1***. Label all inputs and outputs.



3. (2 marks) Use logic gates to design a 2 to 1 multiplexer. Label inputs: ***A***, ***B***, and ***SELECT*** and output: ***Y***?



4. (1 mark) Label the logic levels (**1 or 0**) on the inputs of the multiplexer in question 3, such that the output ***Y = B***. SOLUTION SHOWN IN RED ABOVE.

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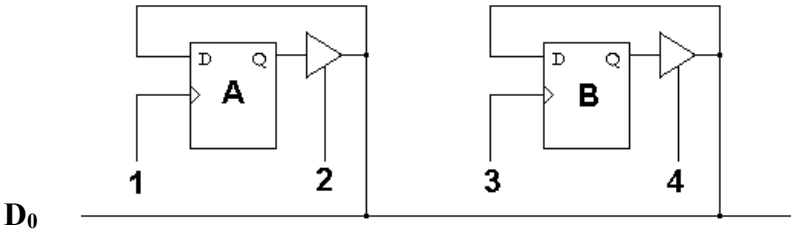
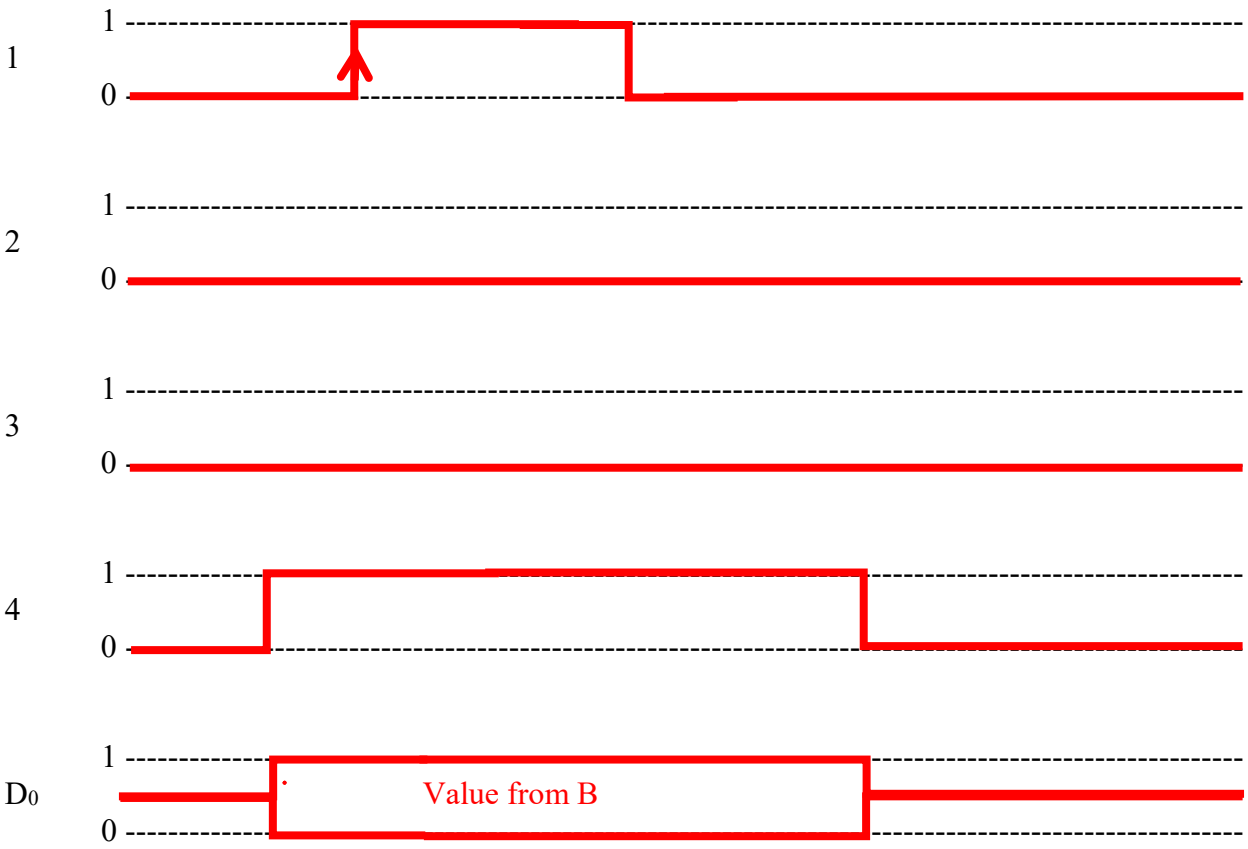
5. (5 marks) Draw a timing diagram showing the signals (1,2,3,4) as the value in **B** is copied to **A**. Assume all four signals levels are zero before and after the above operation.





A high on signal 4 places the value from B onto the data bus (READ). While the data is still on the data bus, a rising edge on signal 1 clocks the data from the data bus into A (WRITE). After the rising edge has occurred and the data from B is successfully copied to A, signal 1 can return to low to get ready for the next register A write signal. Signal 4 can also return to low thus returning the data bus to a high impedance state and allowing other devices to use the data bus.