microComponents

Operating Manual

for the

Micropump Driver

mp6-QuadOEM

Sold in North America by:
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Bartels mikrotechnik

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Content

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1 General Description

The mp6-QuadOEM is a quad-output high-voltage DC-AC converter that drives four mp6 pumps. The device features a 2.7 V to 5.5 V input range that allows the device to accept a variety of voltage sources such as single-cell lithium-ion (Li+) batteries. The outputs of the device generate up to 250 V_{PP} for maximum performance. The high-voltage outputs are ESD protected up to ±15 kV Human Body Model (HBM), ±6kV Contact Discharge, and ±8 kV Air Gap discharge, as specified in IEC 61000-4-2. The mp6-QuadOEM uses a high-voltage full-bridge output stage to convert the high voltage generated by the boost converter to a sinusoidal output waveform. The mp6-QuadOEM utilizes a high-frequency spread-spectrum oscillator to reduce the amount of EMI/EFI generated by the boost-converter circuit. The mp6-QuadOEM provides an I^2C interface to set the boost converter and output switching frequencies through an 8-bit register and the peak output voltages with 5 bits of resolution. The mp6-QuadOEM also provides an adjustable automatic ramping feature that slowly increases or decreases the peak output voltage when a change is made to the output amplitude. The slew rate of the automatic ramp is set with 3 bits of resolution through the I^2C interface and it is independent for each channel. The mp6-QuadOEM comes in a 38.1 mm x 17.78 mm, 28-pin DIL package[1].

2 Proper Use

2.1 Intended Purpose

The mp6-QuadOEM was designed as a next step from the mp6-QuadEVA board to control up to four micropumps for gas pumping, i.e. four pieces of mp6-AIR micropumps.
Nevertheless, it is also possible to pump liquids, with either the mp6-AIR, mp6-pp or the standard mp6 pump; though the higher frequencies will not result in a performance boost.

If liquids should be pumped, please regard the following:
The micropump is intended for pumping liquids or gases with varying flow rates controlled by the electronics. The mp6-QuadOEM is intended as a pump driver for mp6-AIR/mp6/mp6-pp.
Any other use of the micropump or controller unit is deemed improper.
Do not make any modifications or extensions to the pump or controller without the prior written consent of the manufacturer. Such modifications may impair the safety of the unit and are prohibited! Bartels Mikrotechnik GmbH rejects any responsibility for damage to the unit caused by unauthorized modifications to the pump and risk and liability are automatically transferred to the operator.

2.2 Misuse

The use of gases or liquids, which may alone or in combination create explosive or otherwise health-endangering conditions (including vapors) is not permitted.

2.3 Staff Selection and Qualification

All work in connection with the installation, assembly, commissioning/decommissioning, disassembly, operation, servicing, cleaning and repairing of the pump and the controller must be carried out by qualified, suitably trained and

[1] Connection pins do not fit into standard IC sockets as the pins have a square cross section.

instructed personnel. Work on electrical components and assemblies must be carried out by personnel with the necessary qualifications and skills.

2.4 Safety Notice

The mp6-QuadOEM generates voltages of up to 250 Vpp. All parts of the controller can carry voltages in this range. Therefore, the board should only be used by qualified personnel. Although the output power of the module is very low, **proper insulation according to the application conditions needs to be considered by the customer.** This especially applies to the bottom side of the PCB. Contact with water or other liquids needs to be prevented. The pump must not be unplugged while the board is active.

DANGER
THE DEVICE CAN CARRY HIGH VOLTAGE! BE CAREFUL, WHILE CONNECTING AND HANDLING THE BOARD!

3 Pin Configuration

GND	1	28	VDD
VDD	2	27	GND
A0	3	26	NC
A1	4	25	NC
SDA	5	24	NC
SCL	6	23	NC
PIEZO11-	7	22	PIEZO42-
PIEZO11+	8	21	PIEZO42+
PIEZO12+	9	20	PIEZO41+
PIEZO12-	10	19	PIEZO41-
PIEZO21-	11	18	PIEZO32-
PIEZO21+	12	17	PIEZO32+
PIEZO22+	13	16	PIEZO31+
PIEZO22-	14	15	PIEZO31-

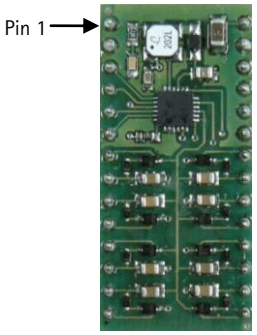

Figure 1: Pin Configuration

4 Typical Operating Circuit

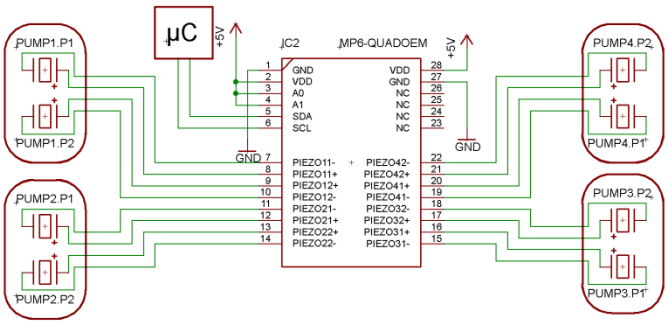

Figure 2: Typical Operating Circuit

5 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings
(All voltages referenced to GND, unless otherwise noted.)

VDD	-0.3V to +6.0V		A0, A1	-0.3V to +6.0V
PIEZOXX, COM	-0.3V to +160V		SCL, SDA	-0.3V to (VDD + 0.3V)

6 Electrical Characteristics

Table 2: Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{DD}		2.7		5.5	V
Input Supply Current	I_{DD}	All channels on, 300V_{PP}, f = 100Hz, sinewave output shape		75		mA
Shutdown Supply Current	I_{SHDN}	A0, A1 = 0V or V_{DD}; SCL = SDA = GND or V_{DD}; not toggling		25	100	nA
Undervoltage Lockout	VUV	V_{DD} rising	1.6	2.0	2.5	V
PIEZO OUTPUTS						
Peak-to-Peak Output Voltage	V_{PP}	PIEZO_ _+ - PIEZO_ _-; VO_ _[4:0]=01000; V_{DD}=5.0V		75		V
		PIEZO_ _+ - PIEZO_ _-; VO_ _[4:0]=10000; V_{DD}=5.0V		150		
		PIEZO_ _+ - PIEZO_ _-; VO_ _[4:0]=11111; V_{DD}=5.0V		250		
Switching Frequency	f_{LR}	FO[7:0]=10000000; V_{DD}=5.0V	194	200	206	Hz
	f_{HR}	FO[7:0]=10111111; V_{DD}=5.0V	388	400	412	
BOOST CONVERTER						
Peak Output Voltage	V_{CS}	VO_ _[4:0] = 01000; V_{DD} = 5.0V		40		V
		VO_ _[4:0] = 10000; V_{DD} = 5.0V		75		
		VO_ _[4:0] = 11111; V_{DD} = 5.0V		150		
Tapped-Inductor Center Switching Frequency	f_{SW}	FSW[4:0] = 10000		400		kHz
		FSW[4:0] = 11111		800		
		FSW[4:0] = 00000 (default)		800		
		FSW[4:0] = 01111		1600		
Tapped-Inductor Switching Frequency Spreading Factor	S_F	SS[1:0] = 01, 10, or 11		8		%
I^2C INTERFACE LOGIC (SDA, SCL, A1, AND A0)						
Input Logic-Low Voltage	V_{IL}				0.5	V
Input Logic-High Voltage	V_{IH}		1.5			V
Input Hysteresis	I_{HYS}			130		mV
Input Leakage Current	I_{LKG}		-1		+1	µA
Output Low Voltage	V_{OL}	ISINK = 3mA			0.4	V
Input/Output Capacitance	$C_{I/O}$			10		pF
Serial-Clock Frequency	f_{SCL}				400	kHz
Clock Low Period	t_{LOW}		1.3			µs

Clock High Period	t_{HIGH}		0.6			µs
Bus Free Time	t_{BUF}		1.3			µs
START Setup Time	$t_{SU,STA}$		0.6			µs
START Hold Time	$t_{HD,STA}$		0.6			µs
STOP Setup Time	$t_{SU,STO}$		0.6			µs
Data In Setup Time	$t_{SU,DAT}$		100			ns
Data In Hold Time	$t_{HD,DAT}$		0		900	ns
Receive SCL/SDA Minimum Rise Time	t_R			$20 + 0.1C_B$		ns
Receive SCL/SDA Maximum Rise Time	t_R			300		ns
Receive SCL/SDA Minimum Fall Time	t_F			$20 + 0.1C_B$		ns
Receive SCL/SDA Maximum Fall Time	t_F			300		Ns
Transmit SDA Fall Time	t_F	C_B = 400pF	$20 + 0.1C_B$		300	ns
SCL/SDA Noise Suppression Time	t_I			50		ns
ESD PROTECTION						
PIEZO_ _+ to PIEZO_ _-		Human Body Model	±15			kV
		IEC 61000-4-2 Contact Discharge	±6			
		IEC 61000-4-2 Air Gap Discharge	±8			
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}		160			°C
Thermal Shutdown Hysteresis	T_{HYST}		12			°C

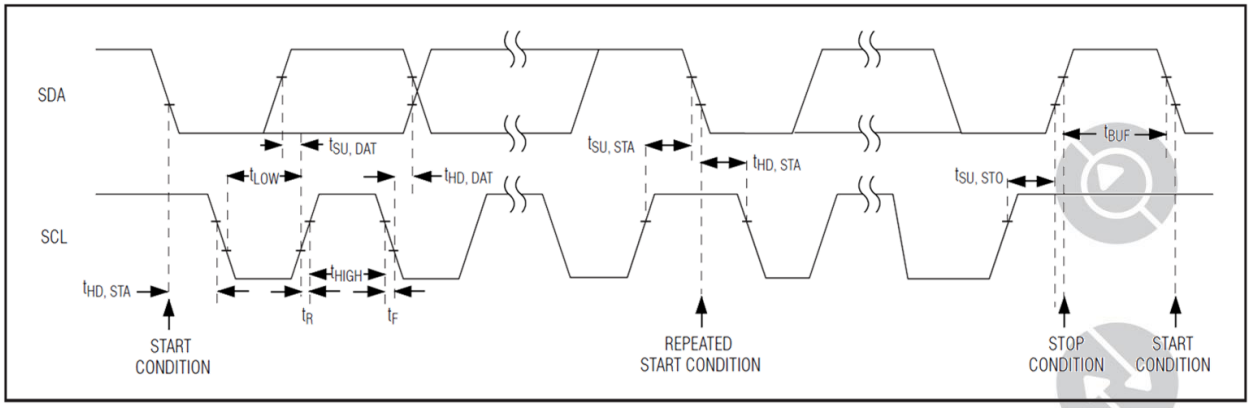

Figure 3: I²C Timing Specifications

7 Signal Shapes

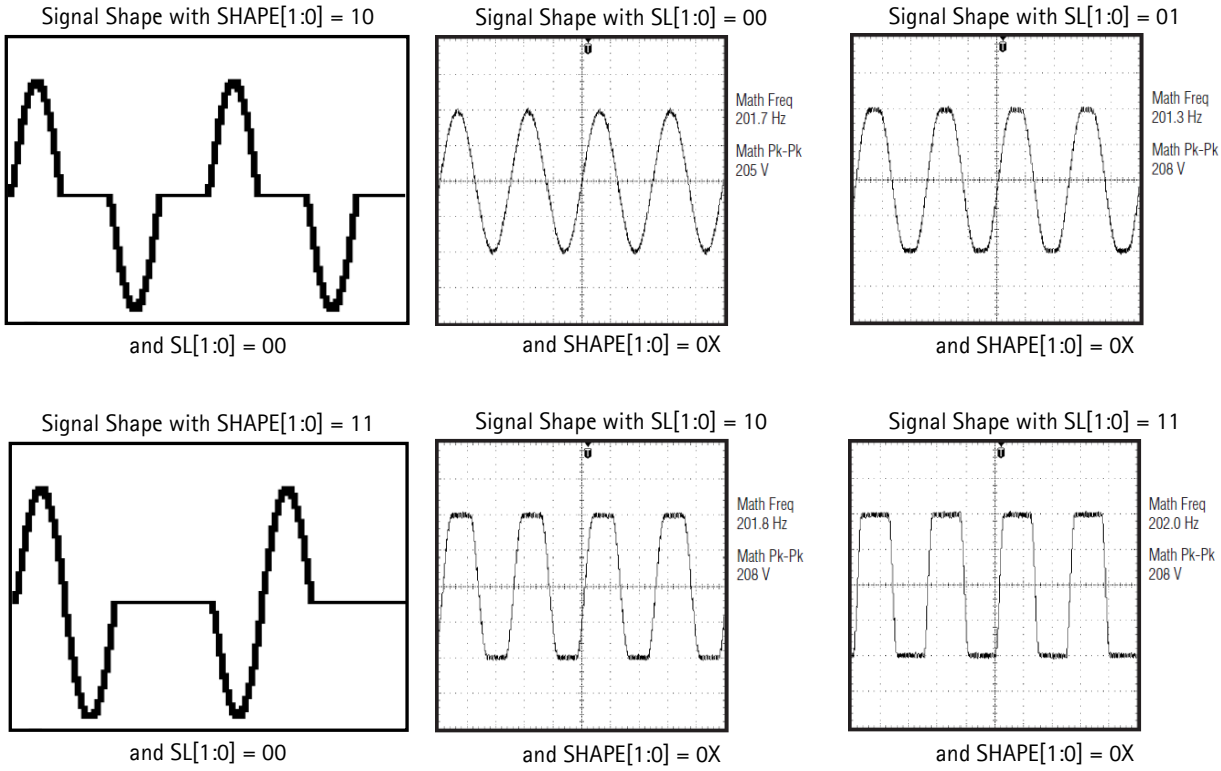

Figure 4: Signal shapes

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8 Pin Description

Table 3: Pin Descriptions

PIN	NAME	FUNCTION
1	GND	Ground
2	VDD	Input Supply Voltage
3	A0	Address Input 0. Address inputs allow up to four connections on one common bus. Connect A0 to GND or VDD.
4	A1	Address Input 1. Address inputs allow up to four connections on one common bus. Connect A1 to GND or VDD.
5	SDA	Open-Drain, Serial Data Input/Output. SDA requires an external pull-up resistor
6	SCL	Serial-Clock Input. SCL requires an external pull-up resistor.
7	COM[1] PIEZO11-	High-Voltage common Output. Connect to negative input of piezo 1 of pump 1
8	PIEZO11+	High-Voltage Output 11+. Connect to positive input of piezo 1 of pump 1
9	PIEZO12+	High-Voltage Output 12+. Connect to positive input of piezo 2 of pump 1
10	PIEZO12-	High-Voltage Output 12-. Connect to negative input of piezo 2 of pump 1
11	COM[1] PIEZO21-	High-Voltage common Output. Connect to negative input of piezo 1 of pump 2
12	PIEZO21+	High-Voltage Output 21+. Connect to positive input of piezo 1 of pump 2
13	PIEZO22+	High-Voltage Output 22+. Connect to positive input of piezo 2 of pump 2
14	PIEZO22-	High-Voltage Output 22-. Connect to negative input of piezo 2 of pump 2
15	COM[1] PIEZO31-	High-Voltage common Output. Connect to negative input of piezo 1 of pump 3
16	PIEZO31+	High-Voltage Output 31+. Connect to positive input of piezo 1 of pump 3
17	PIEZO32+	High-Voltage Output 32+. Connect to positive input of piezo 2 of pump 3
18	PIEZO32-	High-Voltage Output 32-. Connect to negative input of piezo 2 of pump 3
19	COM[1] PIEZO41-	High-Voltage common Output. Connect to negative input of piezo 1 of pump 4
20	PIEZO41+	High-Voltage Output 41+. Connect to positive input of piezo 1 of pump 4
21	PIEZO42+	High-Voltage Output 42+. Connect to positive input of piezo 2 of pump 4
22	PIEZO42-	High-Voltage Output 42-. Connect to negative input of piezo 2 of pump 4
23	NC	Not connected (do not connect)
24	NC	Not connected (do not connect)
25	NC	Not connected (do not connect)
26	NC	Not connected (do not connect)
27	GND	Ground
28	VDD	Input Supply Voltage

[1] *The COM pin is connected to all of the pumps.*

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9 Detailed Description

The mp6-QuadOEM is a quad-output high-voltage DC-AC converter that drives four mp6 pumps. The device features a 2.7 V to 5.5 V input range that allows the device to accept a variety of sources such as single-cell Li+ batteries. The outputs of the device generate up to 250 V_{PP} for maximum pump performance. The mp6-QuadOEM utilizes a high-frequency spread-spectrum boost converter that reduces the amount of EMI/EFI generated by the circuit. The boost-converter switching frequency is set with an 8-bit register through the I^2C interface. The mp6-QuadOEM uses a high-voltage full-bridge output stage to convert the high voltage generated by the boost converter to an AC waveform suitable for driving a piezo membrane pump. An internal register controlled through the I^2C interface sets the shape of the output waveform. The output switching frequency for all outputs is set with an 8-bit register through the I^2C interface. The mp6-QuadOEM provides a serial digital interface that allows the user to set the peak voltage of each output independently with 5 bits of resolution. The mp6-QuadOEM also provides an adjustable automatic ramping feature that slowly increases or decreases the peak output voltage when the set value is changed. The slew rate of the ramp is set with 3 bits of resolution through the I^2C interface and it is independent for each channel. The high-voltage outputs are ESD protected up to ±15 kV Human Body Model, ±8 kV Air Gap Discharge, and ±6 kV Contact Discharge, as specified in IEC 61000-4-2.

9.1 Output Voltage

The shape, slope, frequency, ramp-on/-off times, and peak-to-peak voltage of the mp6-QuadOEM lamp outputs are programmed using internal registers. The mp6-QuadOEM is capable of producing output waveforms with varying shapes and slew rates. The user sets the shape and slew rate of the output using bits in the shape registers. The mp6-QuadOEM output frequency uses an internal oscillator to set the desired frequency. The output frequency is adjusted by the FO[7:0] bits of the output frequency register. The frequency increases and decreases linearly with FO[7:0]. The peak-to-peak voltage of the output is varied from zero to 250 V_{PP} by programming the VO_ _[4:0] bits of the ramping time and output peak voltage registers. The peak-to-peak voltage increases and decreases linearly with VO_ _[4:0]. The mp6-QuadOEM also features a slow fade-on and slow fade-off time feature, it is programmed by the RT_ _ [2:0] bits of the ramping time and output peak voltage registers. This slow fade-on/-off feature causes the peak-to-peak voltage of the outputs to rise slowly from the previously set value to the maximum set value. This feature also causes the peak-to-peak voltage of the outputs to fall from the maximum set value to zero when the device is placed into shutdown. The slow rise and fall of the peak-to-peak output voltage creates a soft fade-on and fade-off of the mp6 pumps.

9.2 Boost Converter

The mp6-QuadOEM boost converter consists of an external-tapped inductor from VDD to the LX input, an internal DMOS switch, an external diode from the secondary of the tapped inductor to the CS output, an external capacitor from the CS output to GND, and a mp6 pump connected to each output. When the DMOS switch is turned on, LX is connected to GND, and the inductor is charged. When the DMOS switch is turned off, the energy stored in the inductor is transferred to the capacitor CCS and the mp6. Note: The mp6-QuadOEM exhibits high-voltage spikes on the LX node. The addition of a snubber circuit to the LX node protects the device by suppressing the high voltage spikes. The values of RSN and CSN should be optimized for the specific tapped inductor used. Typical values are RSN = 20Ω and CSN = 330pF. The mp6-QuadOEM boost-converter frequency uses an internal oscillator to set the frequency of the boost converter. The oscillator frequency is adjusted by the FSW[4:0] bits of the boost-converter frequency register. The boost converter increases and decreases linearly with FSW[3:0]. To further reduce the amount of EMI/EFI generated by the circuit, the boost-converter frequency can be modulated (see the SS[1:0] bits of the boost-converter

frequency register). Enabling modulation spreads the switching energy of the oscillator in the frequency domain, thus decreasing EMI.

9.3 Independent Dimming Control

The performance of the mp6 pump is proportional to the peak-to-peak voltage applied. The mp6-QuadOEM provides four registers to control the peak-to-peak voltage of each output using the VO_ _[4:0] bits of the ramping time and output peak voltage registers.

9.4 Signal Output Waveshape

The mp6-QuadOEM can produce sine-wave to square-wave waveshapes on the outputs by varying the slope of the outputs. This is achieved by using bits SL[1:0] of the shape register. If the shape configuration is set to sine and if all outputs have the same amplitude settings, then each output has a sinusoidal waveshape. If the outputs have different amplitude settings, then the output with the highest setting has a sine waveshape while the remaining outputs have a clamped sine waveshape.

9.5 Shutdown

The mp6-QuadOEM can be placed in shutdown by writing a '0' to the EN bit of the system register. When activating shutdown, the pump outputs are shut down; however, the register contents remain unchanged.

9.6 Undervoltage Lockout (UVLO)

The mp6-QuadOEM has a UVLO threshold of +2.0V (typ). When VDD falls below +2.0V (typ), the device enters a non-operative mode. The contents of the I^2C registers are not guaranteed to remain unchanged below UVLO.

9.7 Thermal Protection

The mp6-QuadOEM enters a non-operative mode if the internal die temperature of the device reaches or exceeds +160°C (typ). The mp6-QuadOEM is latched, and only cycling the power supply of the mp6-QuadOEM resets the thermal protection bit as well as all registers.

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10 I²C Registers and Bit Descriptions

Ten internal registers program the mp6-QuadOEM. Table 4 lists all the registers, their addresses, and power-on reset states. All registers are read/write. Register 0x0A is reserved as a command to update all signal peak voltage output registers. Register 0x0B is reserved and should not be used.

Table 4: Register Map

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS	POWER-ON RESET STATE
SYSTEM										
Device Id	DEVID3	DEVID2	DEVID1	DEVID0	REV3	REV2	REV1	REV0	0x00	0xB2
Power Mode	OVR TEMP[1]	X	X	X	X	X	X	EN	0x01	0x00
OUTPUT FREQUENCY										
Output Frequency	FO7	FO6	FO5	FO4	FO3	FO2	FO1	FO0	0x02	0x00
Signal Shape										
Slope/Shape	X	ENDAMP	X	X	SHAPE1	SHAPE0	SL1	SL0	0x03	0x00
BOOST-CONVERTER FREQUENCY										
Boost-Converter Frequency	SS1	SS0	X	FSW4	FSW3	FSW2	FSW1	FSW0	0x04	0x00
AUDIO[2]										
Audio Effects	FR_AM	NO_SAMPLE	AUXDIV1	AUXDIV0	AU4	AU3	AU2	AU1	0x05	0x00
SIGNAL RAMPING TIME AND PEAK VOLTAGE										
Ramping Time and Peak Output Voltage CH1[3]	RT1_2	RT1_1	RT1_1	VO1_4	VO1_3	VO1_2	VO1_1	VO1_0	0x06	0x00
Ramping Time and Peak Output Voltage CH2[3]	RT2_2	RT2_1	RT2_1	VO2_4	VO2_3	VO2_2	VO2_1	VO2_0	0x07	0x00
Ramping Time and Peak Output Voltage CH3[3]	RT3_2	RT3_1	RT3_1	VO3_4	VO3_3	VO3_2	VO3_1	VO3_0	0x08	0x00
Ramping Time and Peak Output Voltage CH4[3]	RT4_2	RT4_1	RT4_1	VO4_4	VO4_3	VO4_2	VO4_1	VO4_0	0x09	0x00

X = Don't Care
[1]Read back only
[2]Audio functions are not supported, as the audio input pin is not available. Keep the register value at the default (0x00)
[3]Send command 0Ah (update all signal ramping time and peak voltage registers) to have the programmed voltage effectively applied to the pumps

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10.1 Slave Address

The mp6-QuadOEM device address is set through external inputs. The slave address consists of five fixed bits (B7–B3, set to 11110) followed by two input programmable bits (A1 and A0). For example: If A1 and A0 are hardwired to ground, then the complete address is 1111000. The full address is defined as the seven most significant bits followed by the read/write bit. Set the read/write bit to 1 to configure the mp6-QuadOEM to read mode. Set the read/write bit to 0 to configure the mp6-QuadOEM to write mode. The address is the first byte of information sent to the mp6-QuadOEM after the START condition.

10.2 System Registers (0x00, 0x01)

Table 5

Device ID (DEVID3/DEVID2/DEVID1/DEVID0)	DEVID[3:0] is preprogrammed to 1011 to identify the mp6-QuadOEM; see Table 6.
Revision (REV3/REV2/REV1/REV0)	REV[3:0] is preprogrammed to the current revision of the mp6-QuadOEM and is REV[3:0] = 0010.
System Over temperature (OVRTEMP)	1 = Thermal shutdown temperature exceeded. 0 = Analog circuitry operating properly. OVRTEMP = 1 turns the outputs off. To set OVRTEMP to 0 and restart in default condition (all register reset), cycle the power supply of the mp6-QuadOEM.

Table 6: Device Identification, Status, and Enable

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x00	DEVID3	DEVID2	DEVID1	DEVID0	REV3	REV2	REV1	REV0
0x01	OVRTEMP	X	X	X	X	X	X	EN

X = Don't Care

Table 7: Signal Output Frequency

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x02	FO7	FO6	FO5	FO4	FO3	FO2	FO1	FO0

Table 8: Signal Frequency Range

FO[7:6]	FREQUENCY RANGE (Hz)
00	50-100
01	100-200
10	200-400
11	400-800

10.3 Output Shape Register (0x03)

Table 9

Damping Enable (ENDAMP)	1 = Active damping on LX node enabled. 0 = Active damping on LX node disabled. ENDAMP = 1 actively damps the oscillation on the LX pin and could reduce EMI.
Shape (SHAPE1/SHAPE0)	SHAPE[1:0] sets the desired output waveform; see Table 10 and Table 11.
Slew Rate (SL1/SL0)	SL[1:0] sets the slope of the output; see Table 12.

Table 10: Signal Shape Configuration

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x03	X	ENDAMP	X	X	SHAPE1	SHAPE0	SL1	SL0

X = Don't Care

Table 11: Signal Output Shape Configuration

SHAPE[1:0]	OUTPUT SHAPE
0X	Full Wave
10	Half Wave
11	Half Wave

X = Don't Care

Table 12: Signal Slope Configuration

SL[1:0]	OUTPUT SLOPE
00	Sine
01	Fast Slope
10	Faster Slope
11	Fastest Slope (Square Wave)

10.4 Boost-Converter Frequency Register (0x04)

Table 13

Spread Spectrum (SS1/SS0)	SS[1:0] sets the spread-spectrum modulation frequency to a fraction of the boost-converter frequency; see Table 14 and Table 15.
Boost-Converter Switching Frequency (FSW[4:0])	FSW4 sets the switching frequency range of the boost converter and FSW[3:0] sets the switching frequency within the frequency range; see Table 16. The frequency range for FSW4 = 0 is 800 kHz – 1600 kHz. The frequency range for FSW4 = 1 is 400 kHz–800kHz. FSW[3:0] = 0000 sets the frequency to the minimum value of the frequency range. FSW[3:0] = 1111 sets the frequency to the maximum value of the frequency range. Boost-converter switching frequency increases linearly with FSW[3:0].

Table 14: Boost-Converter Configurations

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x04	SS1	SS0	X	FSW4	FSW3	FSW2	FSW1	FSW0

X = Don't Care

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Table 15: Spread-Spectrum Configuration

SS[1:0]	SPREAD-SPECTRUM
00	Disabled
01	1/8
10	1/32
11	1/128

Table 16: Boost-Converter Frequency Range

FSW3	FSW2	FSW1	FSW0	BOOST-CONVERTER SWITCHING FREQUENCY (kHz)	
				FSW4 = 0	FSW4 = 1
0	0	0	0	800	400
0	0	0	1	853	427
0	0	1	0	907	453
0	0	1	1	960	480
0	1	0	0	1013	507
0	1	0	1	1067	533
0	1	1	0	1120	560
0	1	1	1	1173	587
1	0	0	0	1227	613
1	0	0	1	1280	640
1	0	1	0	1333	667
1	0	1	1	1387	693
1	1	0	0	1440	720
1	1	0	1	1493	747
1	1	1	0	1547	773
1	1	1	1	1600	800

10.5 Ramping Time and Peak Output Voltage Register (0x06, 0x07, 0x08, 0x09)

Table 17

Ramping Time (RT4_ _/RT3_ _/RT2_ _/RT1_ _)	RT_ _[2:0] sets the ramp time of each output; see Table 19.
Output Peak-to-Peak Voltage (VO1_ _/VO2_ _/VO3_ _/VO4_ _)	VO_ _[4:0] controls the peak-to-peak voltage of each output. When VO_ _[4:0] = 00000, the output follows COM. When VO_ _[4:0] = 11111, the output has a 150V peak with respect to COM. The output voltage rises linearly with VO_ _[4:0].

Table 18: Output Configuration

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x06	RT1_2	RT1_1	RT1_1	VO1_4	VO1_3	VO1_2	VO1_1	VO1_0
0x07	RT2_2	RT2_1	RT2_1	VO2_4	VO2_3	VO2_2	VO2_1	VO2_0
0x08	RT3_2	RT3_1	RT3_1	VO3_4	VO3_3	VO3_2	VO3_1	VO3_0
0x09	RT4_2	RT4_1	RT4_1	VO4_4	VO4_3	VO4_2	VO4_1	VO4_0

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Table 19: Ramping Time Configuration

RT_ _[2:0]	Ramping Time (ms)
000	<0.1
001	62.5
010	125
011	250
100	500
101	750
110	1000
111	2000

10.6 I²C Interface

The mp6-QuadOEM features an I²C-compatible as a slave device, 2-wire serial interface consisting of a serial data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication to the device at clock rates up to 400 kHz. Figure 3 shows the 2-wire interface-timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the mp6-QuadOEM by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the mp6-QuadOEM is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the mp6-QuadOEM transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pull-up resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the mp6-QuadOEM from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

10.7 Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the START and STOP Conditions section). SDA and SCL idle high when the I2C bus is not busy.

10.8 START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 5). A START condition from the master signals the beginning of a transmission to the mp6-QuadOEM. The master terminates transmission and frees the bus by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

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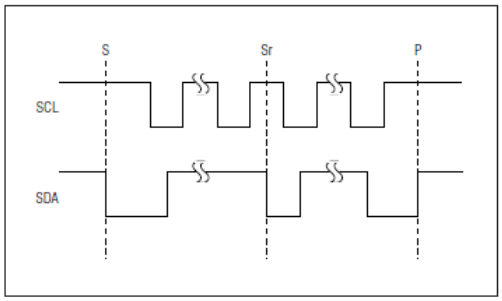

Figure 5: START, STOP and REPEATED START Conditions

10.9 Early STOP Conditions

The mp6-QuadOEM recognizes a STOP condition at any point during data transmission, except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

10.10 Slave Address

The mp6-QuadOEM has selectable device addresses through external inputs. The slave address consists of five fixed bits (B7–B3, set to 11110) followed by two pin programmable bits (A1 and A0). For example: If A1 and A0 are hardwired to ground, the complete address is 1111000. The full address is defined as the seven most significant bits followed by the read/write bit. Set the read/write bit to 1 to configure the mp6-QuadOEM to read mode. Set the read/write bit to 0 to configure the mp6-QuadOEM to write mode. The address is the first byte of information sent to the mp6-QuadOEM after the START condition.

10.11 Acknowledge

The acknowledge bit (ACK) is a clocked 9.th bit that the mp6-QuadOEM uses to handshake receipt each byte of data when in write mode (see Figure 6). The mp6-QuadOEM pulls down SDA during the entire master generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault had occurred. In the event of an unsuccessful data transfer, the bus master may retry communication. The master pulls down SDA during the 9.th clock cycle to acknowledge receipt of data when the mp6-QuadOEM is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the mp6-QuadOEM followed by a STOP condition.

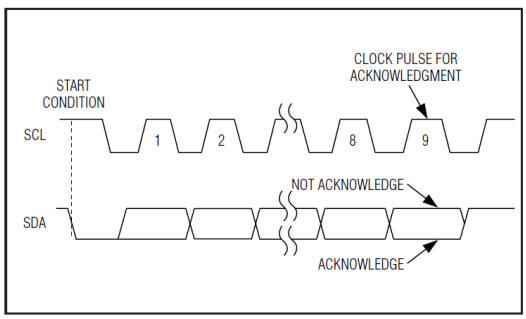

Figure 6: Acknowledge

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10.12 Write Data Format

A write to the mp6-QuadOEM includes transmission of a START condition, the slave address with the R/W bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 7 illustrates the proper frame format for writing one byte of data to the mp6-QuadOEM. Figure 8 illustrates the frame format for writing n-bytes of data to the mp6-QuadOEM. The slave address with the R/W bit set to 0 indicates that the master intends to write data to the mp6-QuadOEM. The mp6-QuadOEM acknowledges receipt of the address byte during the master-generated 9.th SCL pulse. The second byte transmitted from the master configures the mp6-QuadOEM internal register address pointer. The pointer tells the mp6-QuadOEM where to write the next byte of data. An acknowledge pulse is sent by the mp6-QuadOEM upon receipt of the address pointer data. The third byte sent to the mp6-QuadOEM contains the data that will be written to the chosen register. An acknowledge pulse from the mp6-QuadOEM signals receipt of the data byte. The address pointer automatically increments to the next register address after each received data byte. This auto increment feature allows a master to write to sequential registers within one continuous frame. Attempting to write to register addresses higher than 0x0B results in repeated writes of 0x0B. Figure 8 illustrates how to write to multiple registers with one frame. The master signals the end of transmission by issuing a STOP condition.

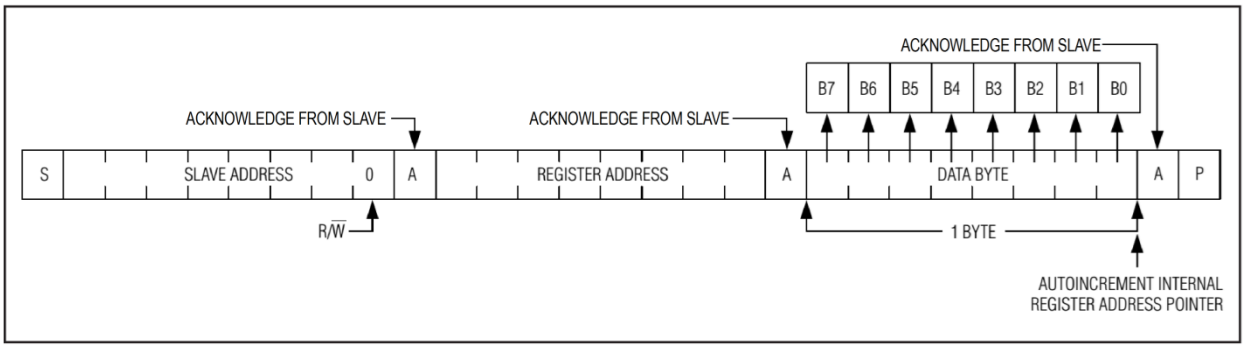

Figure 7: Writing One Byte of Data to the mp6-QuadOEM

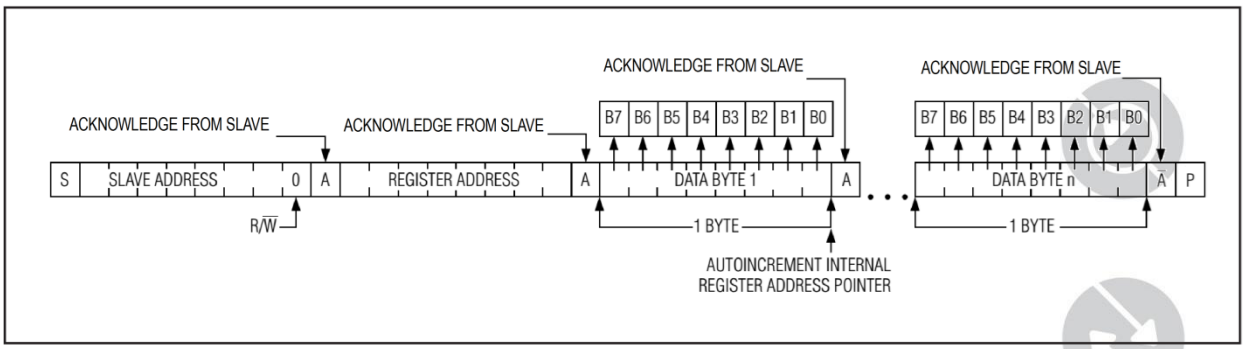

Figure 8: Writing n-Bytes of Data to the mp6-QuadOEM

10.13 Read Data Format

Send the slave address with the R/W set to 1 to initiate a read operation. The mp6-QuadOEM acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00. The first byte transmitted from the mp6-QuadOEM will be the contents of register 0x00. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). The address pointer automatically increments after each read data byte. This auto increment feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read will be from register 0x00 and subsequent reads will auto increment the address pointer until the next STOP condition. The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the mp6-QuadOEM's slave address with the R/W bit set to 0 followed by the register address. A REPEATED START condition is then sent, followed by the slave address with the R/W set to 1. The mp6-QuadOEM transmits the contents of the specified register. The address pointer automatically increments after transmitting the first byte. Attempting to read from register addresses higher than 0x0B results in repeated reads of 0x0B. The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 9 illustrates the frame format for reading one byte from the mp6-QuadOEM. Figure 10 illustrates the frame format for reading multiple bytes from the mp6-QuadOEM.

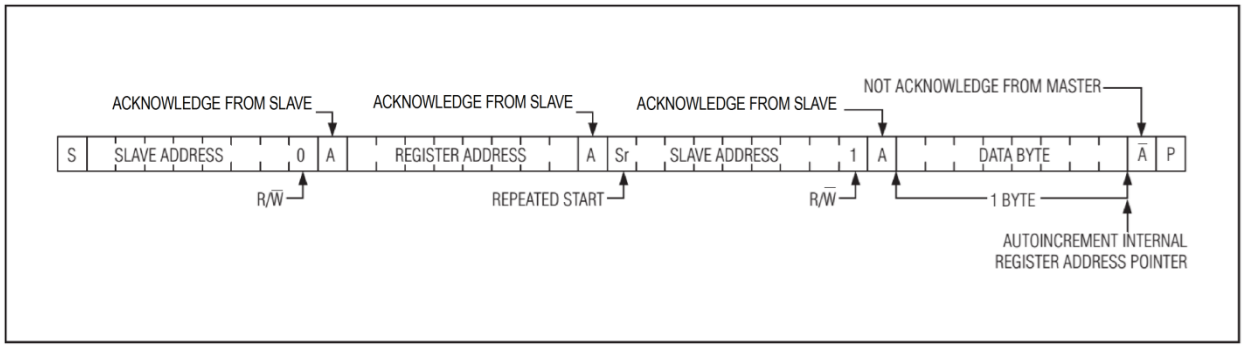

Figure 9: Reading One Indexed Byte of Data from the mp6-QuadOEM

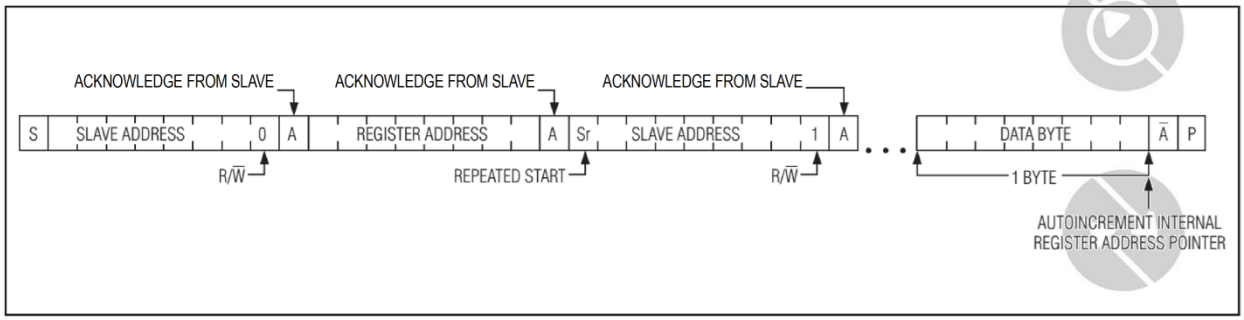

Figure 10: Reading n-Bytes of Indexed Data from the mp6-QuadOEM

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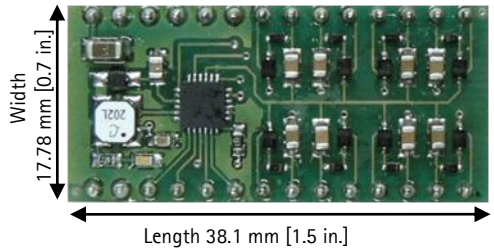
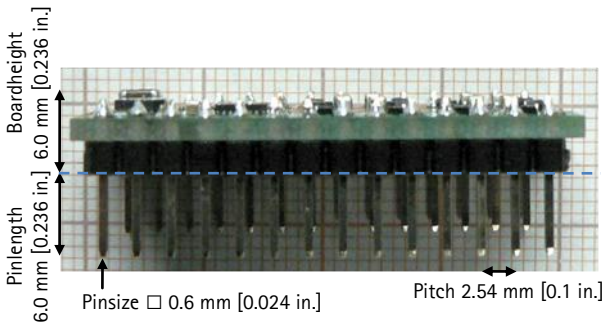
11 Package Dimensions

Table 20: Package Dimensions





All pins have a square cross section of 0.6 mm (0.024 in.)

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