ECE 423 Final Project

Stephen More

1) Project Overview:

DRC: PASSED
LVS: PASSED

I unfortunately ran out of time and was not able to connect all the parts of the full op amp with common mode feedback in layout. I created the layouts for the bias circuit, the differential folded cascode op amp, and the common mode feedback circuit, all individual circuits passed LVS and DRC.

Specifications and Results:

Name	Spec	SS	TT	FF
Power Supplies (V)	VDD VCM	1.7 1	1.8 1	1.9 1
External Capacitors (pF)	Cload	3.44	3	2.55
Diff Loop Gain (dB)	>65	65**	68.67	71.65
Diff Loop UGBW (MHz)	>65	83.39	120.7	109.5
Diff Loop PM (deg)	>60	63.6	59.6*	65.4
CMFB Phase Margin	>60	76	75.6	74.7
Vout DC (V) CM Accuracy	< ±0.05V	658.9m -0.341	628.2m -0.372	552.9m -447
Output Swing (Vpp)	> 1	1.13	1.079	0.958
Power Consumption (mW)	< 8	3.421	3.307	3.117

*Orange Boxes Indicate not meeting a requirement.
** Measured value was 64.97dB

For CMFB Phase margin, I was able to find a length value for all transistors other than the cascode outputs which allowed for PM requirement to be met, however, it was unmanufacturable so during the layout phase I conformed to a length that did not quite make it.

For Vout DC Accuracy, my guess would be that the CMFB circuit isn't providing the desired feedback, causing the output voltage to be lower than VCM. I went with the design I did so that I could meet as many requirements as possible, and I wasn't able to figure out the issue.

2) Schematics:

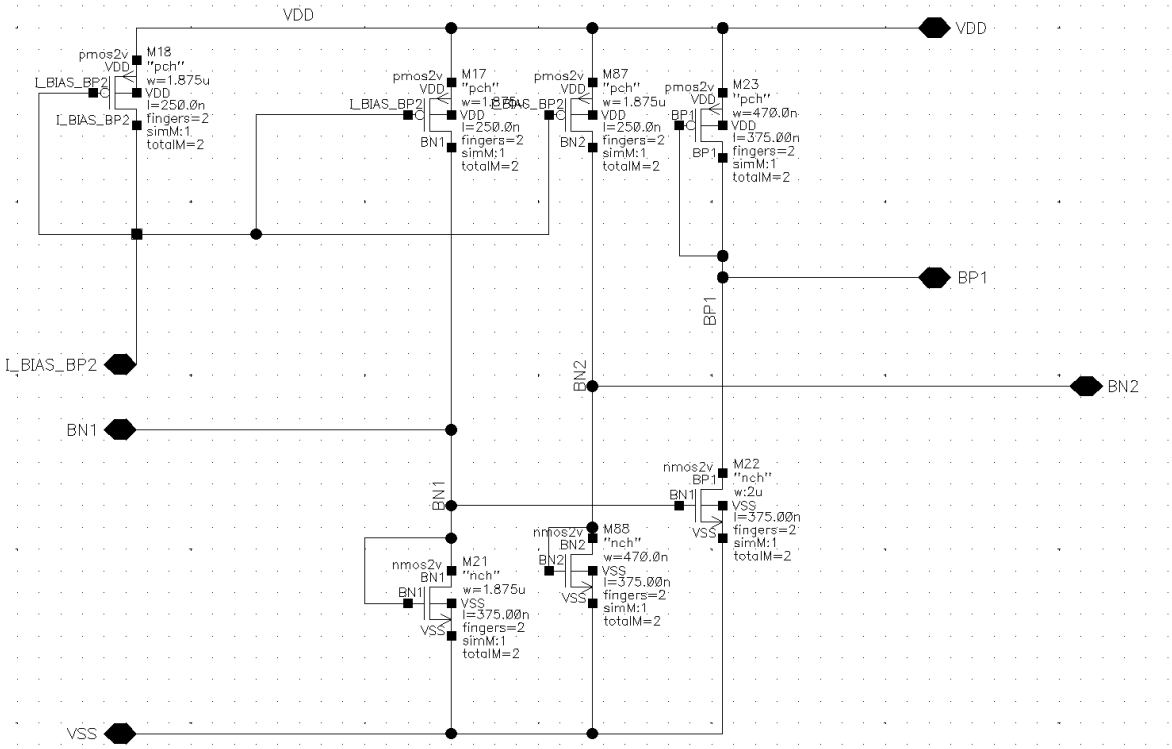

Figure I: Bias Circuit

Widths and Lengths Top to Bottom:
M18: w=1.875u, l=250n
M17: w=1.875u, l=250n
M87: w=1.875u, l=250n
M23: w=470n, l=375n
M21: w=1.875u, l=375n
M88: w=470n, l=375n
M22: w=2u, l =375n

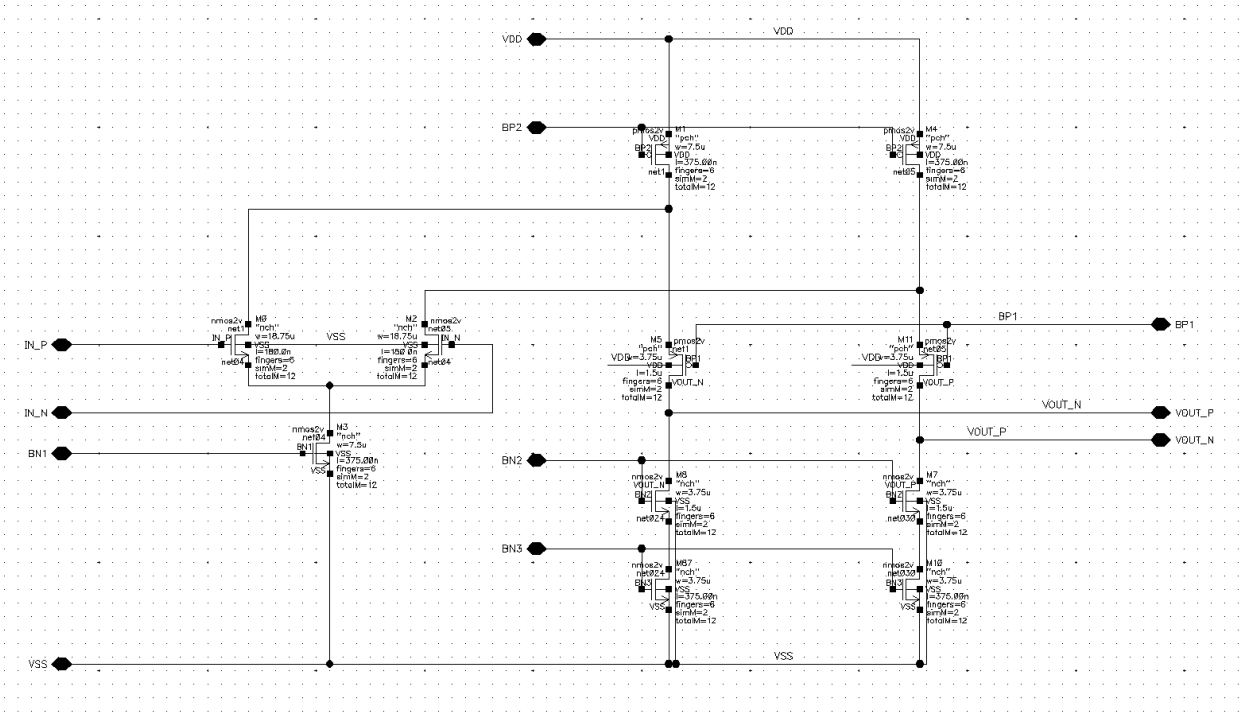

Figure II: Folded Cascode Amplifier Circuit

Widths and Lengths Top to Bottom:
M1: w=7.5u, l=375n
M4: w=7.5u, l=375n
M0: w=18.75u, l=180n
M2: w=18.75u, l=180n
M5: w=3.75u, l=1.5u
M11: w=3.75u, l=1.5u
M3: w=7.5u, l=375n
M8: w=3.75u, l =1.5u
M7: w=3.75u, l =1.5u
M67: w=3.75u, l=375n
M10: w=3.75u, l=375n

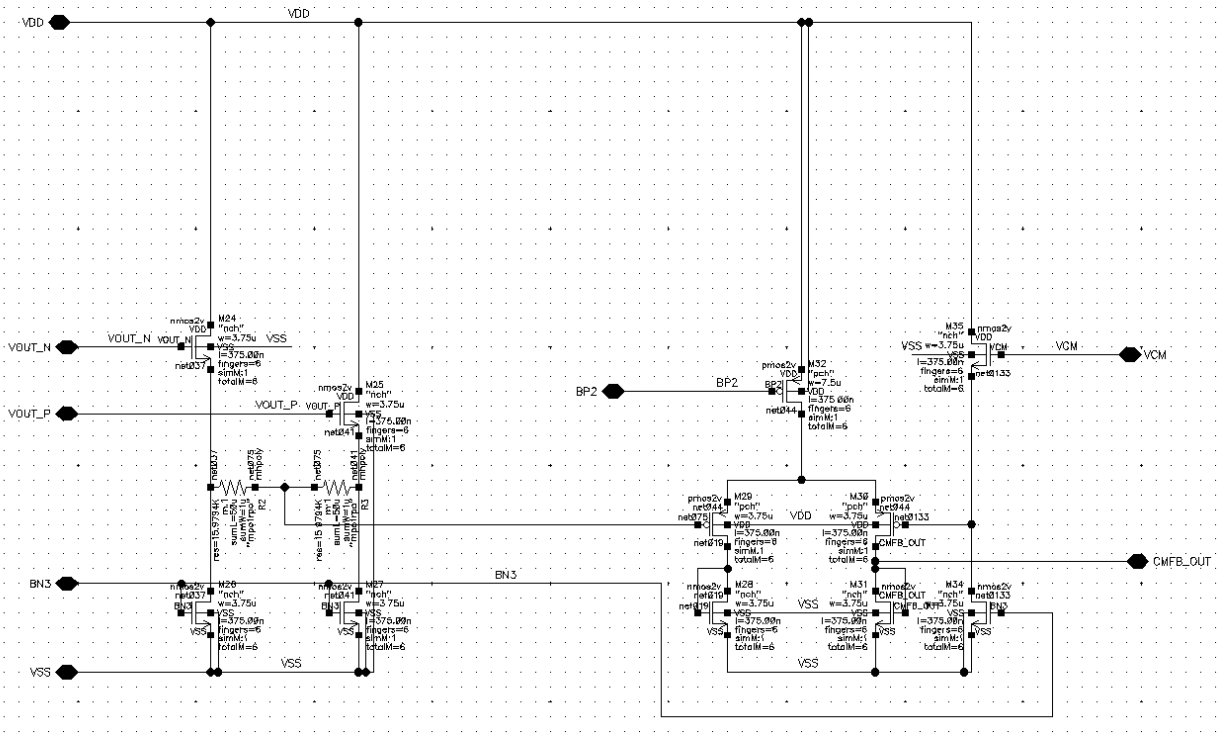

Figure III: Common Mode Feedback Amplifier Circuit

Widths and Lengths Top to Bottom:
Rnhpoly resistors: 15.97k
M24: w=3.75u, l=375n
M25 w=3.75u, l=375n
M67: w=3.75u, l=375n
M10: w=3.75u, l=375n
M32: w=7.5u, l=375n
M35: w=3.75u, l=375n
M29: w=3.75u, l=375n
M30: w=3.75u, l=375n
M20: w=3.75u, l=375n
M27: w=3.75u, l=375n
M28: w=3.75u, l=375n
M31: w=3.75u, l=375n

Testbench Schematics:

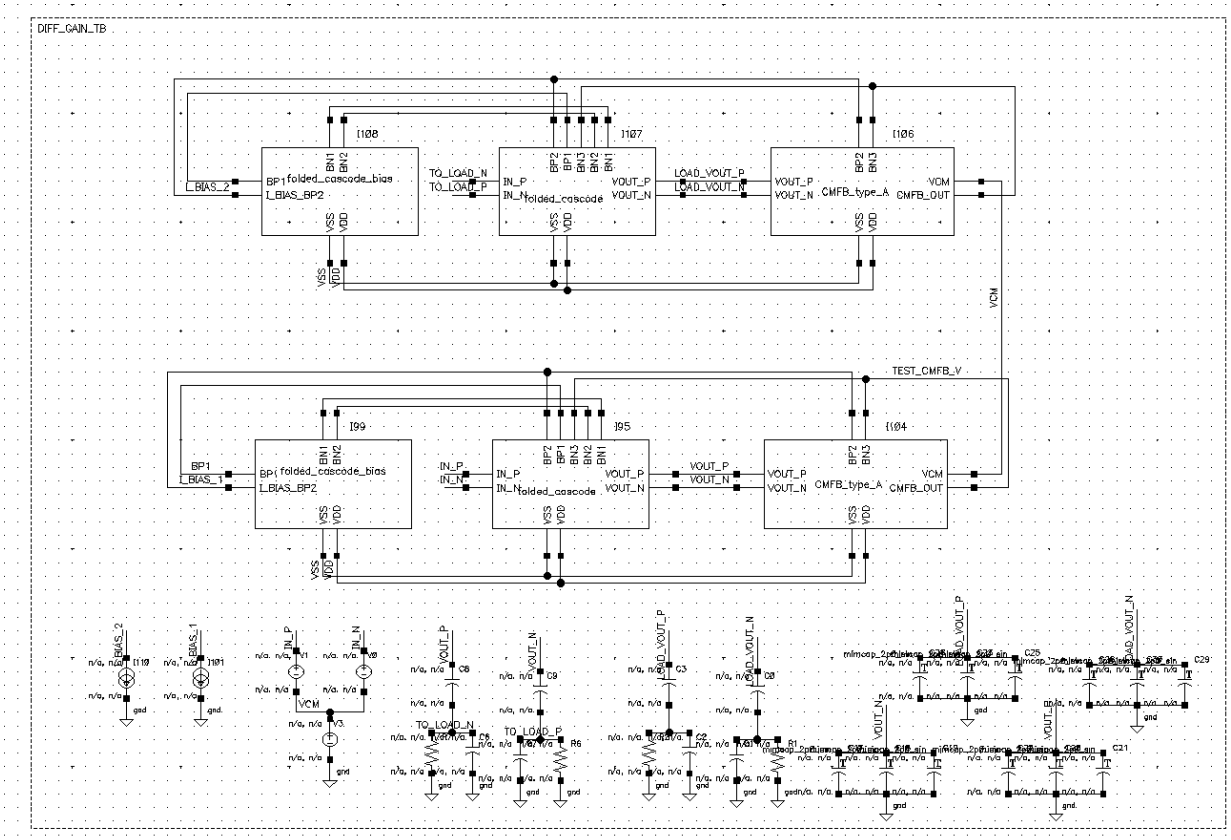

Figure IV: Differential Testbench

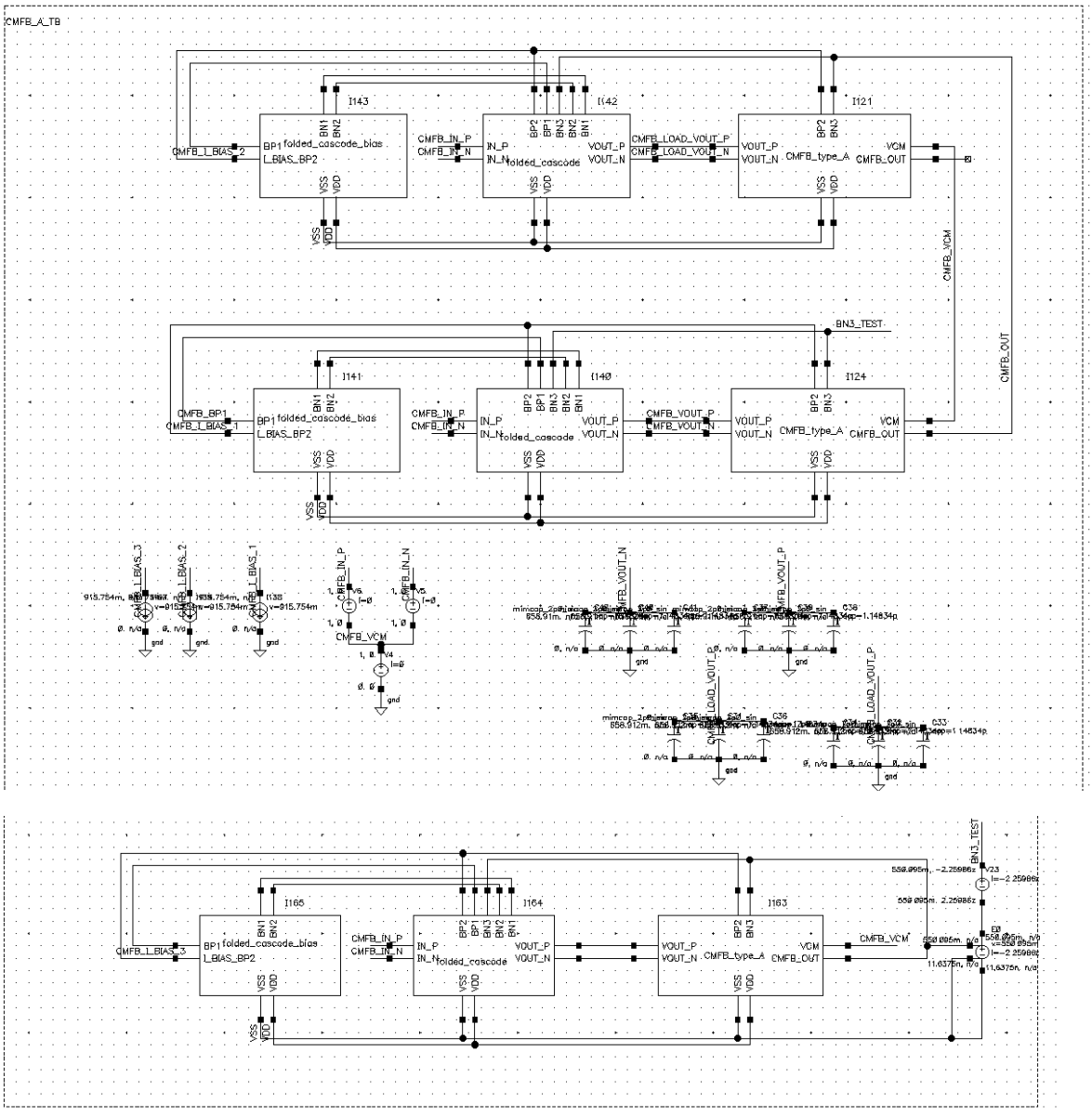

Figure V: CMFB Testbench

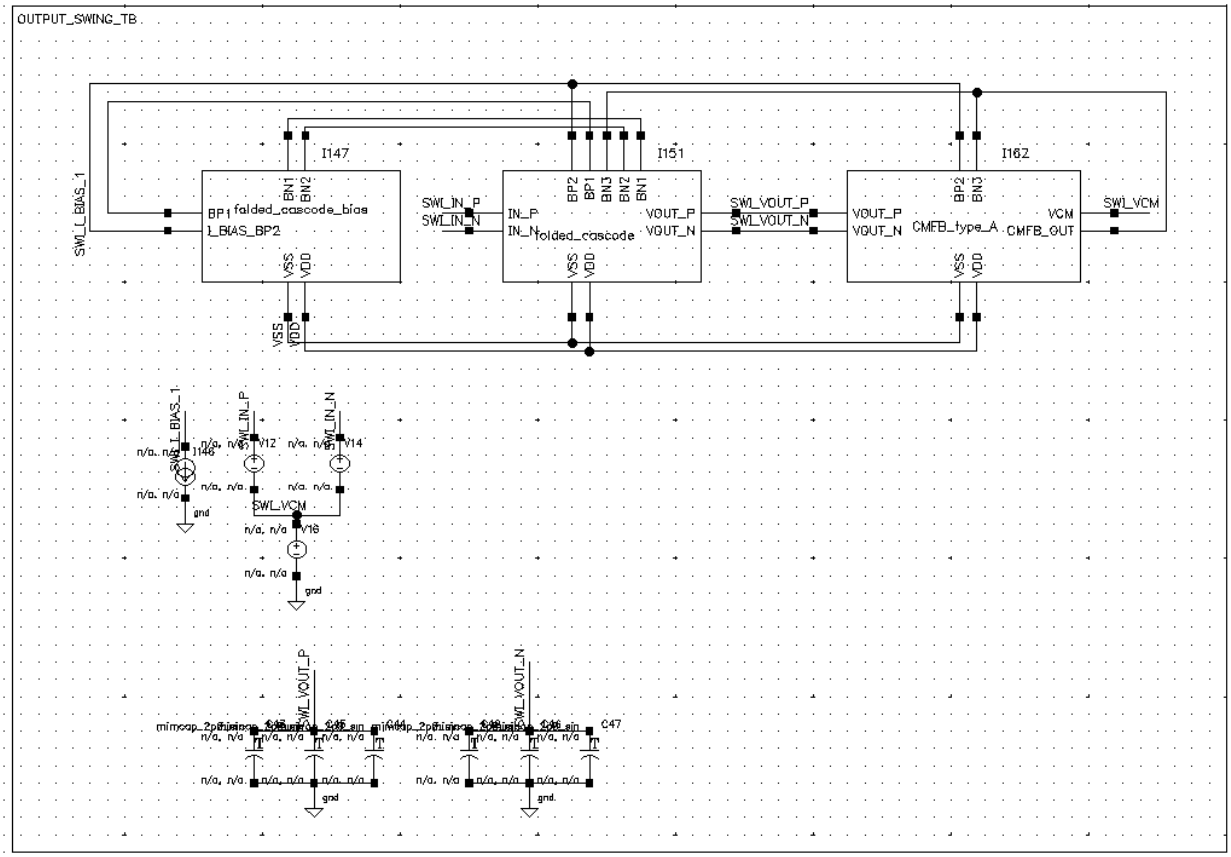

Figure VI: Output Swing Testbench

3) Simulation Results:

Differential Gain & UGBW across corners:

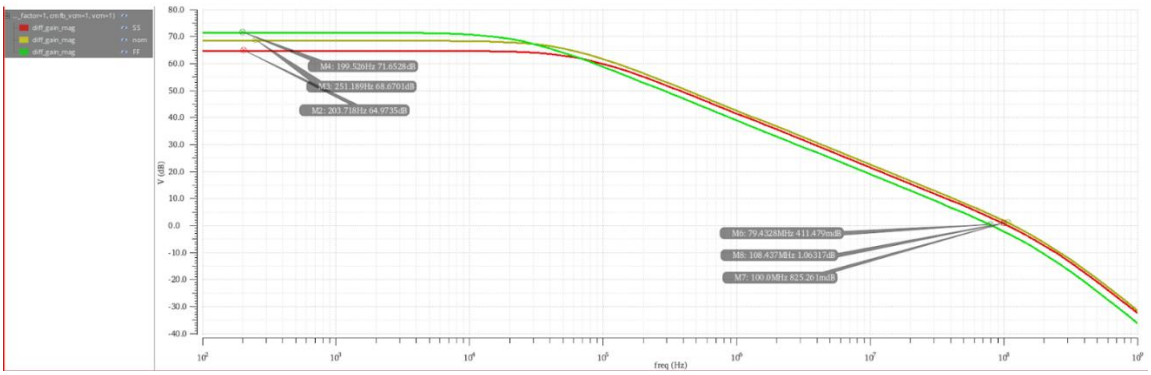

Figure VII: Magnitude (dB) of differential gain across corners

Differential Phase:

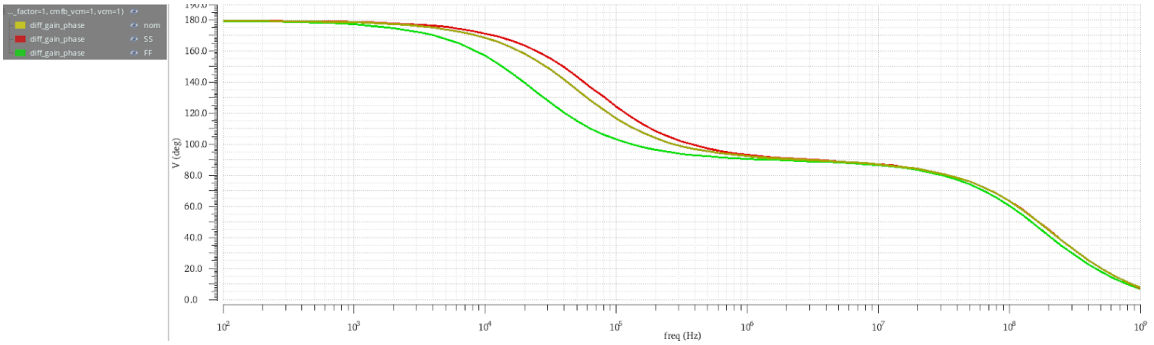

Figure VIII: Phase (deg) of differential across corners

Differential UGBW and Phase for each corner:

SS:

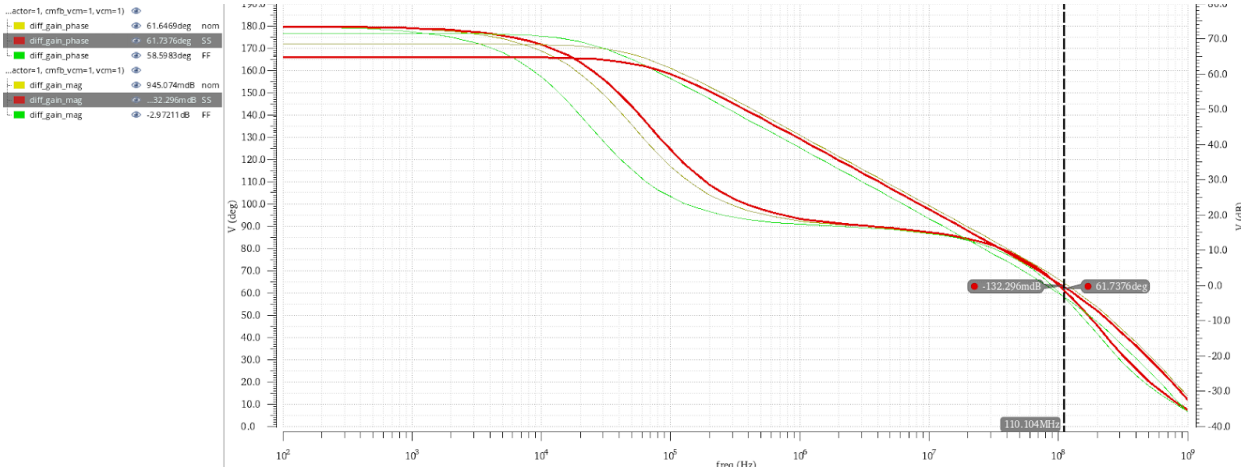

Figure IX: Differential Gain and Phase on SS corner

FF:

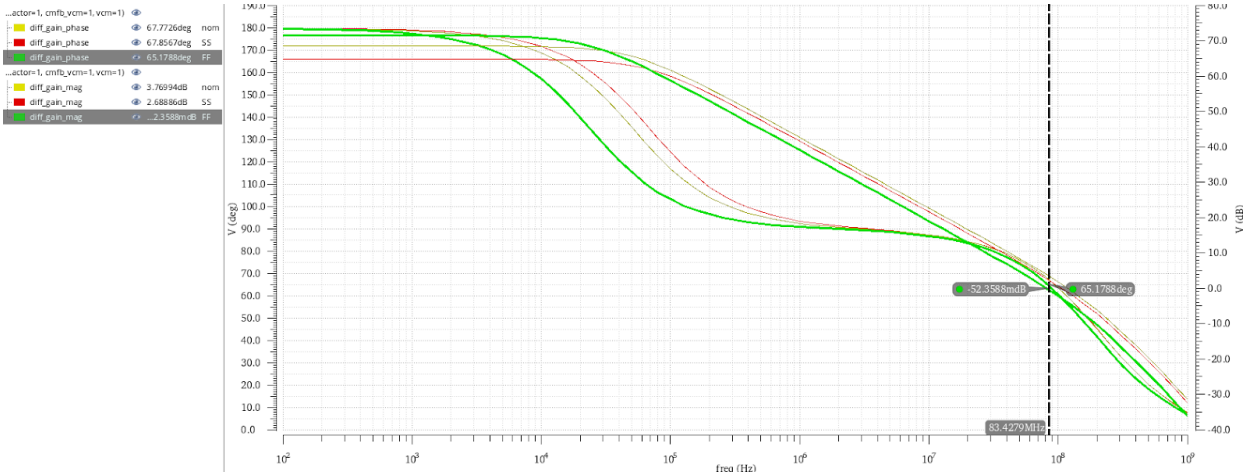

Figure X: Differential Gain and Phase on FF corner

TT:

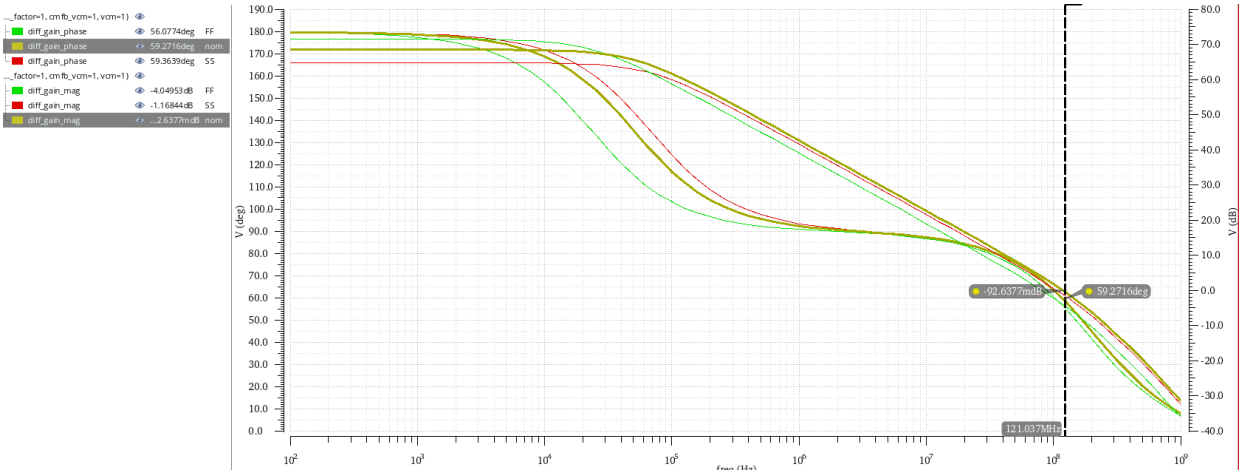

Figure XI: Differential Gain and Phase on TT corner

CMFB Gain:

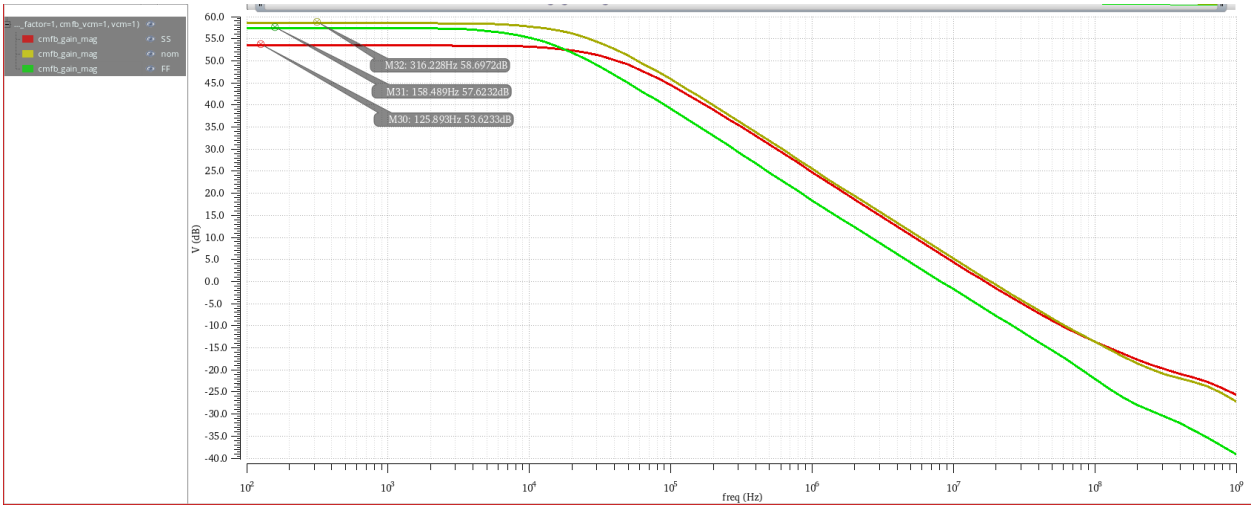

Figure XII: Magnitude (dB) of CMFB gain across corners

CMFB Phase:

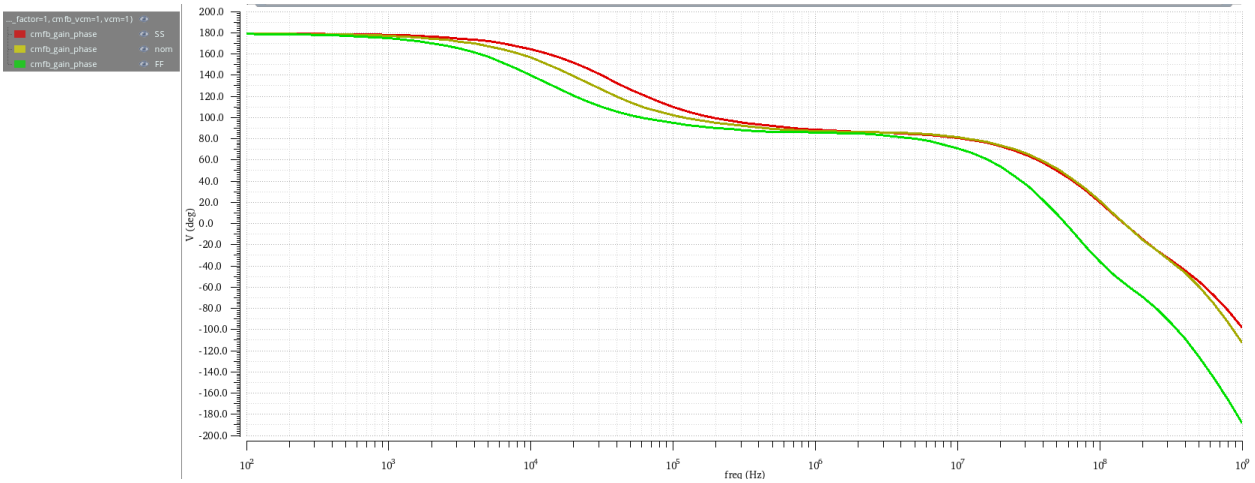

Figure XIII: Phase (deg) of CMFB across corners

CMFB UGBW and Phase across Corners:

SS:

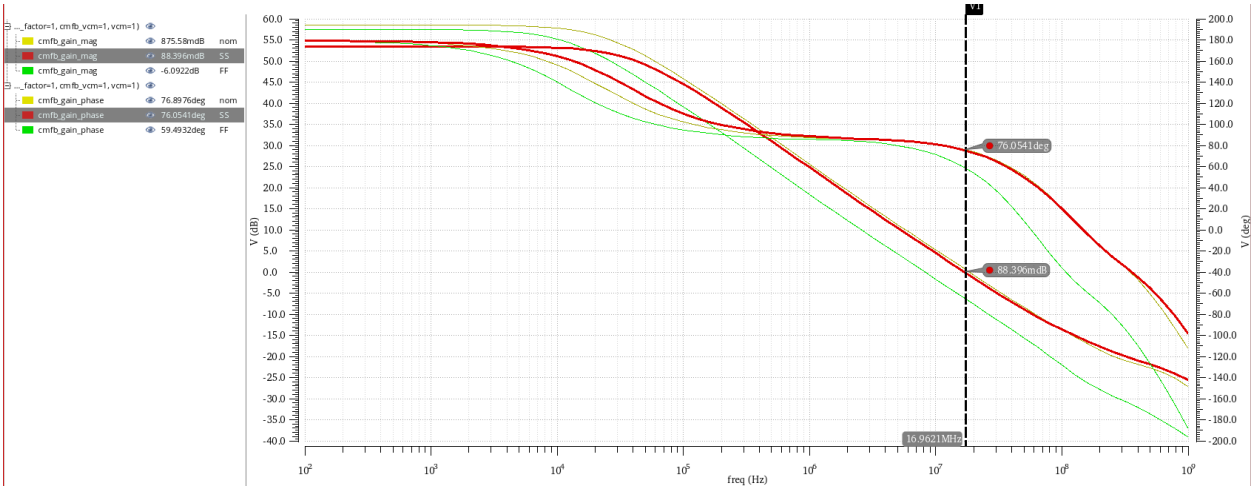

Figure XIV: CMFB Gain and Phase on SS corner

FF:

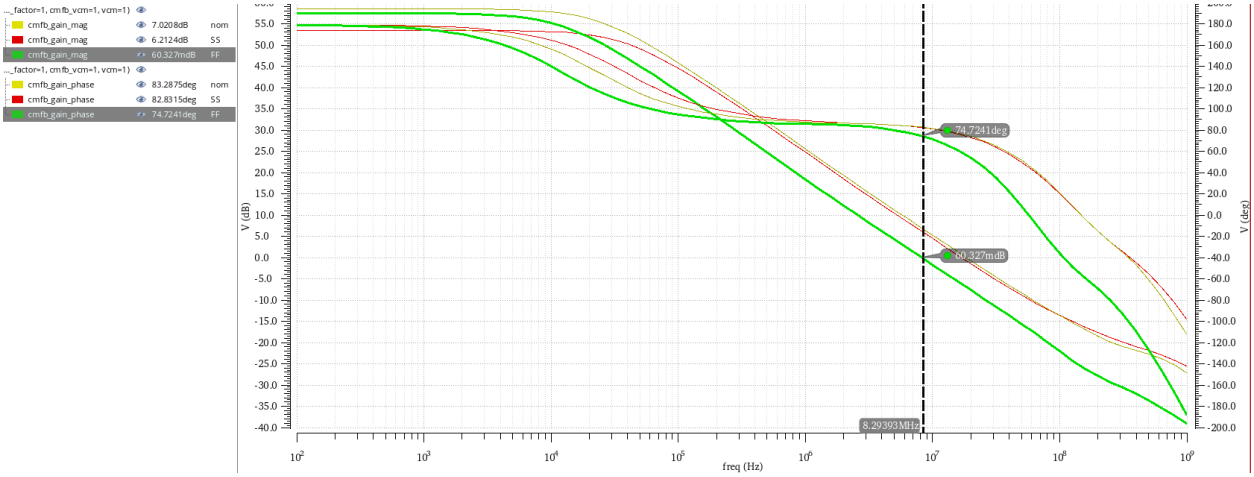

Figure XV: CMFB Gain and Phase on FF corner

TT:

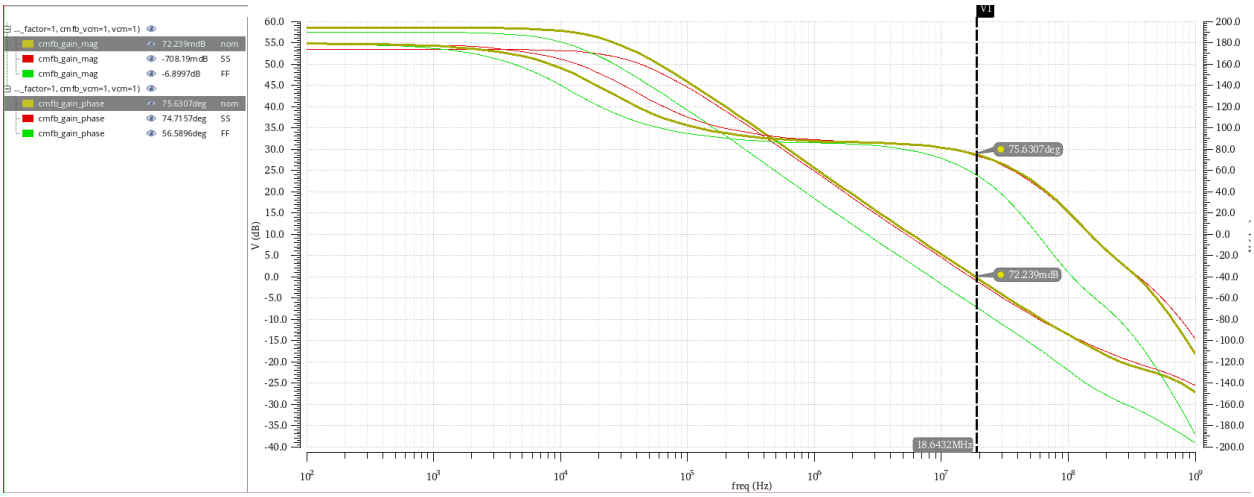

Figure XVI: CMFB Gain and Phase on TT corner

Output Swing Across Corners:

TT:

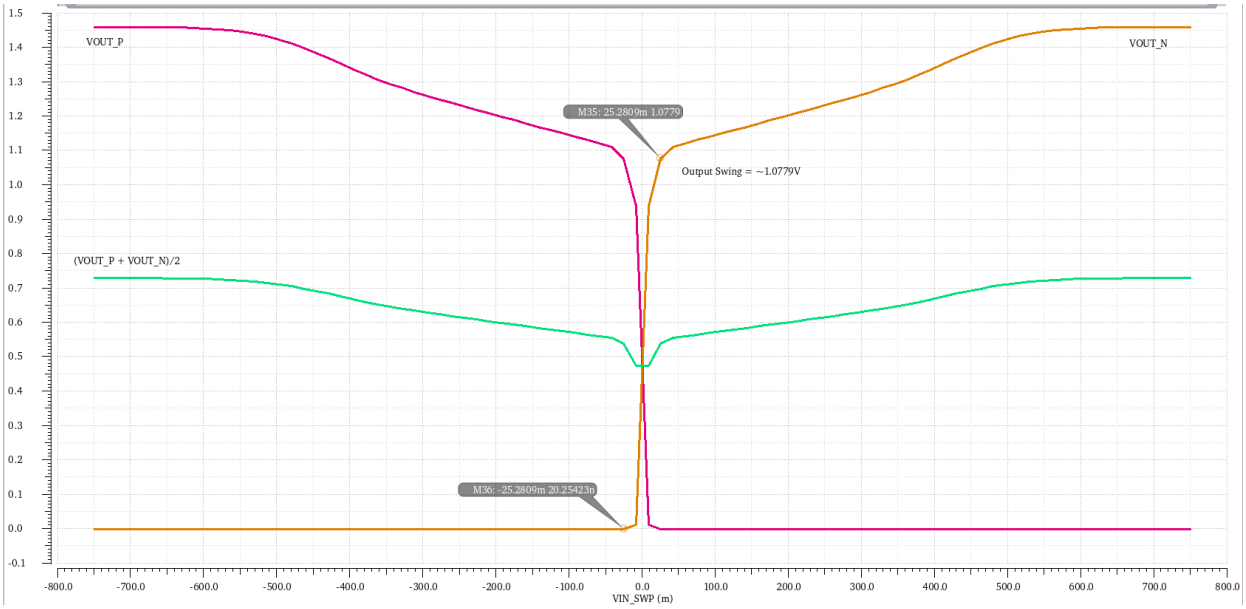

Figure XVII: Output Swing on TT Corner

SS:

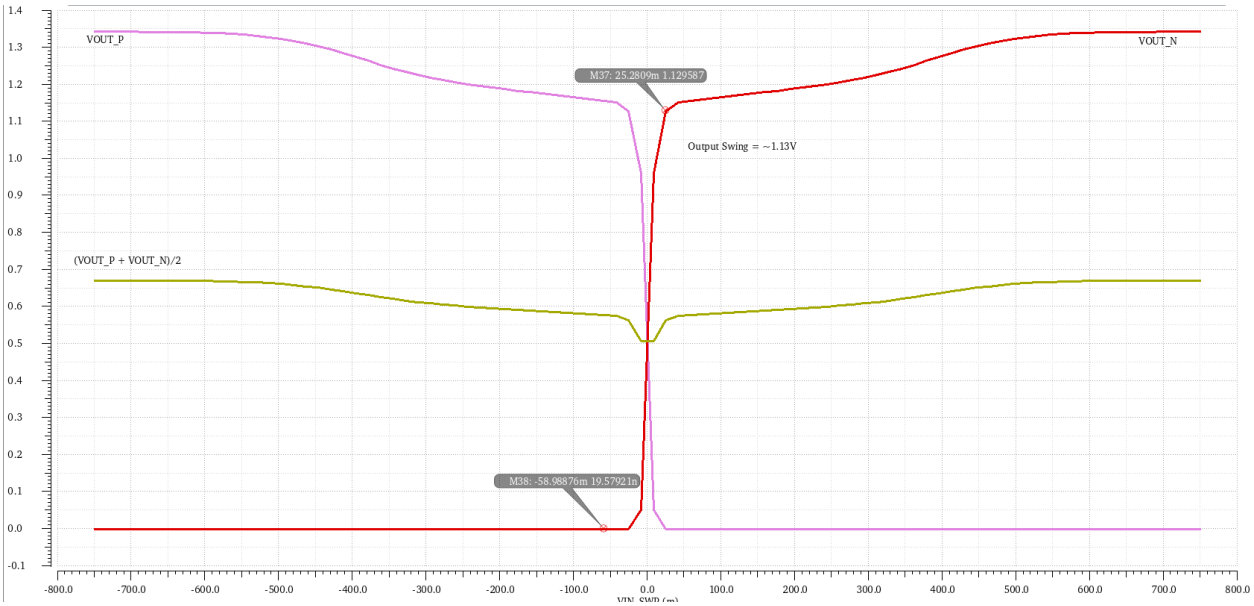

Figure XVIII: Output Swing on SS Corner

FF:

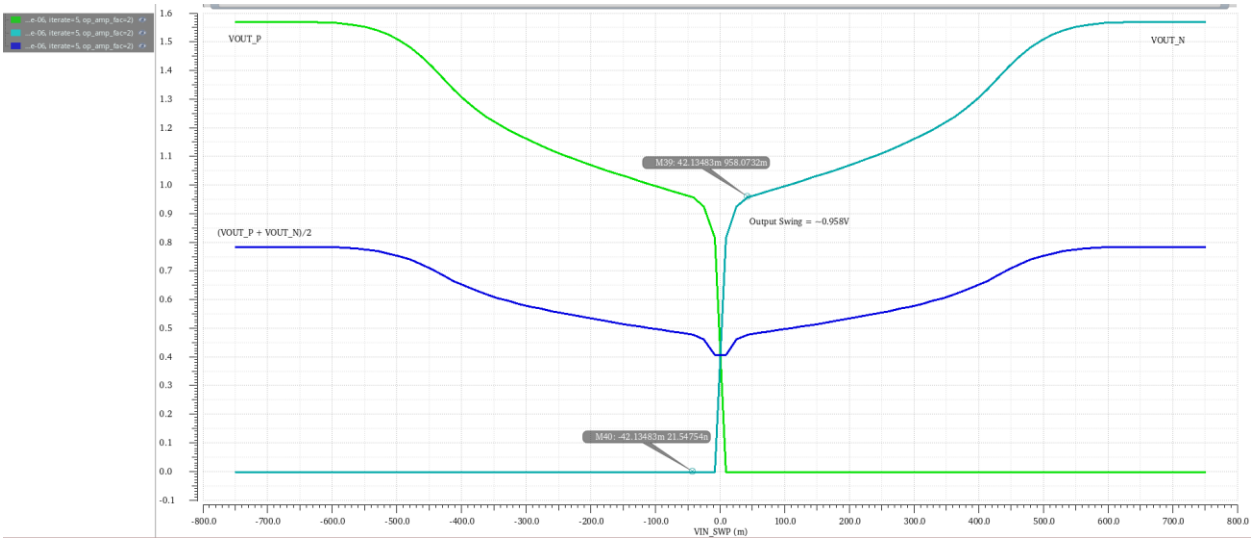

Figure XIX: Output Swing on FF Corner

Results from testbench:

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	SS	FF
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
Final_Project:folded_cascode_CMFB_TEST:1	diff_pm	-120.4				-120.4	-114.6	-117.8	-114.6
Final_Project:folded_cascode_CMFB_TEST:1	diff_ugbw	120.7M				83.39M	120.7M	109.5M	83.39M
Final_Project:folded_cascode_CMFB_TEST:1	cmfb_ugbw	18.89M				8.395M	18.89M	17.25M	8.395M
Final_Project:folded_cascode_CMFB_TEST:1	cmfb_pm	-104.4				-105.3	-104	-104	-105.3
Final_Project:folded_cascode_CMFB_TEST:1	full_pwr	3.307m				3.117m	3.421m	3.421m	3.117m
Final_Project:folded_cascode_CMFB_TEST:1	unit_load_cap	1p				851.9f	1.148p	1.148p	851.9f

Figure XX: Calculator results for power and capacitance

Equation used by calculator for current calculation is the following:

(mag(VDC("/VDD")) * (abs(OP("/I99/M18" "id")) + abs(OP("/I99/M17" "id")) + abs(OP("/I99/M87" "id")) + abs(OP("/I99/M23" "id")) + abs(OP("/I95/M1" "id")) + abs(OP("/I95/M4" "id")) + (abs(OP("/I104/M24" "id")) + abs(OP("/I104/M25" "id")) + abs(OP("/I104/M32" "id")) + abs(OP("/I104/M35" "id")))))

4) Layout

I think I deserve the points for completing layout because even though I wasn't able to lay out the entire circuit in one piece, I was able to pass DRC and LVS on the bias circuit, the diff amp, and the CMFB amp.

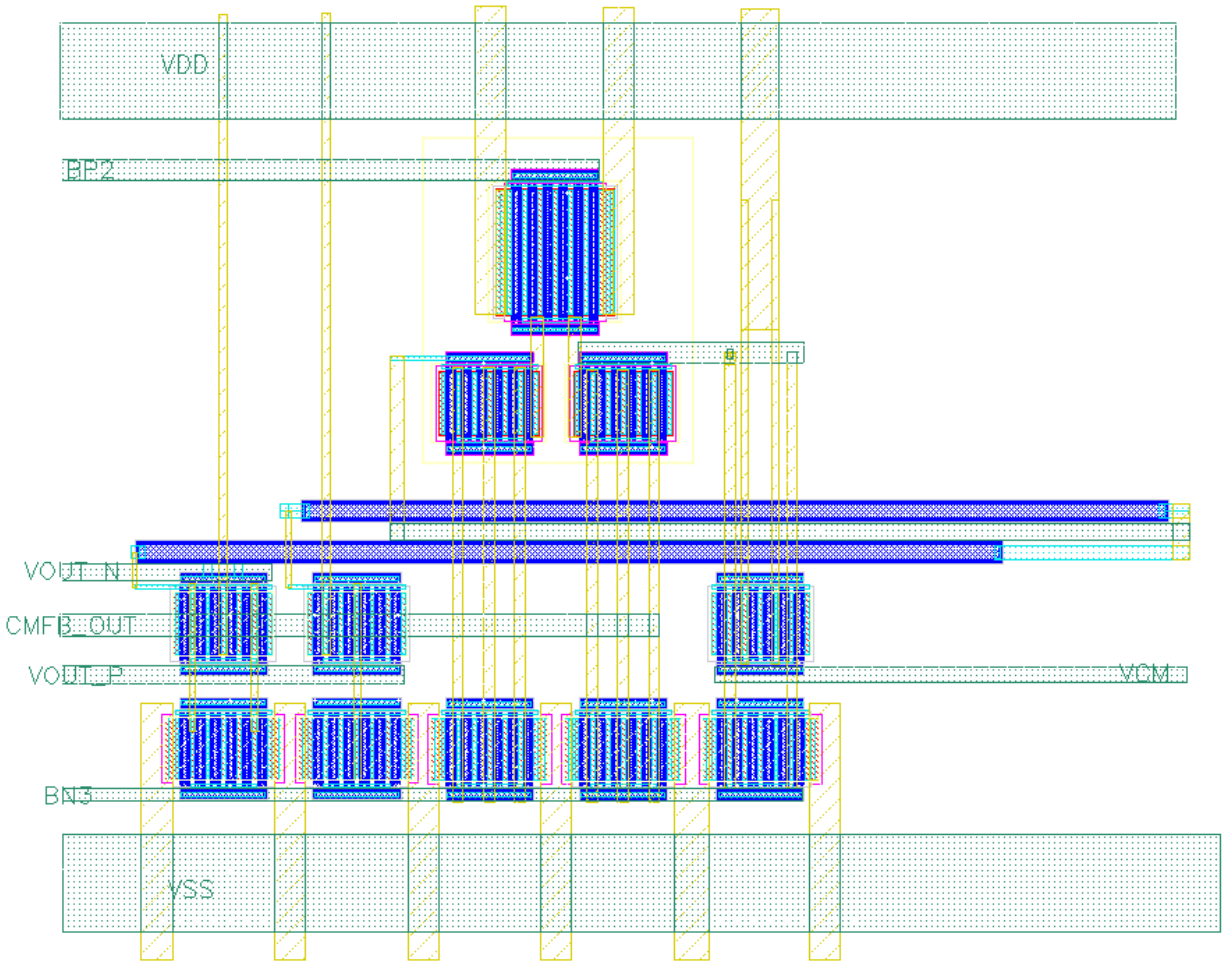

Figure XXI: CMFB Layout

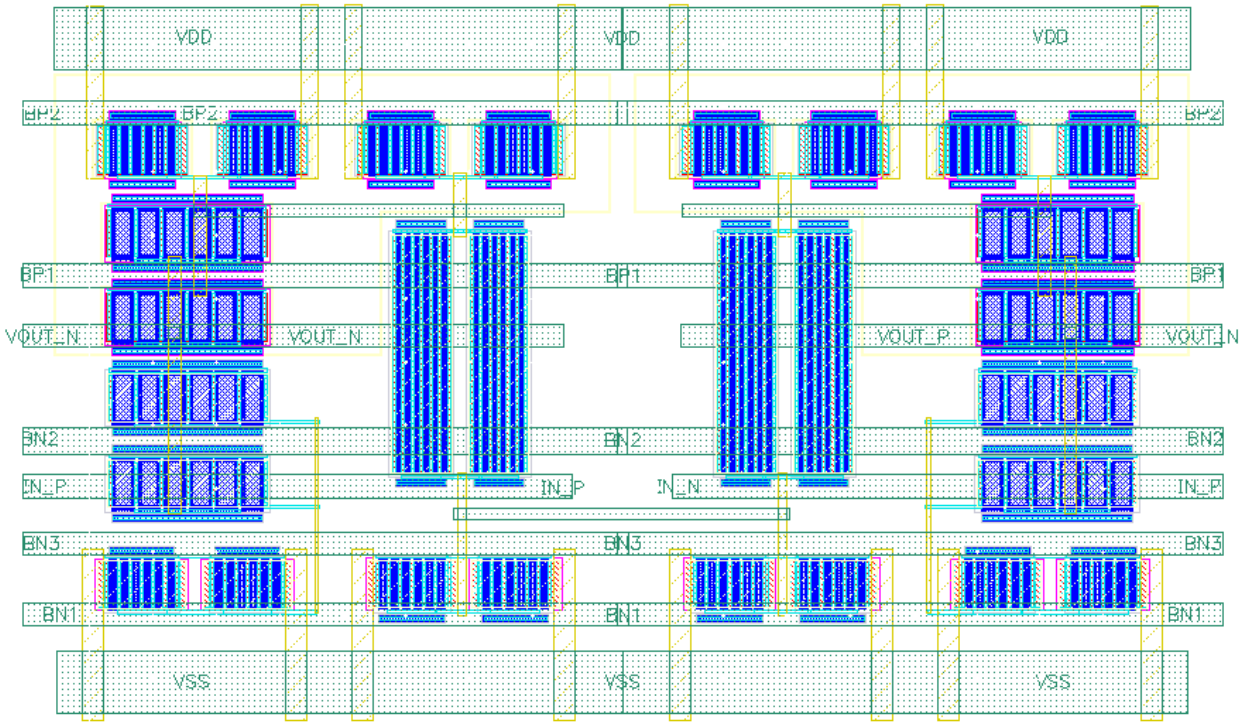

Figure XXII: Cascode Amplifier Layout

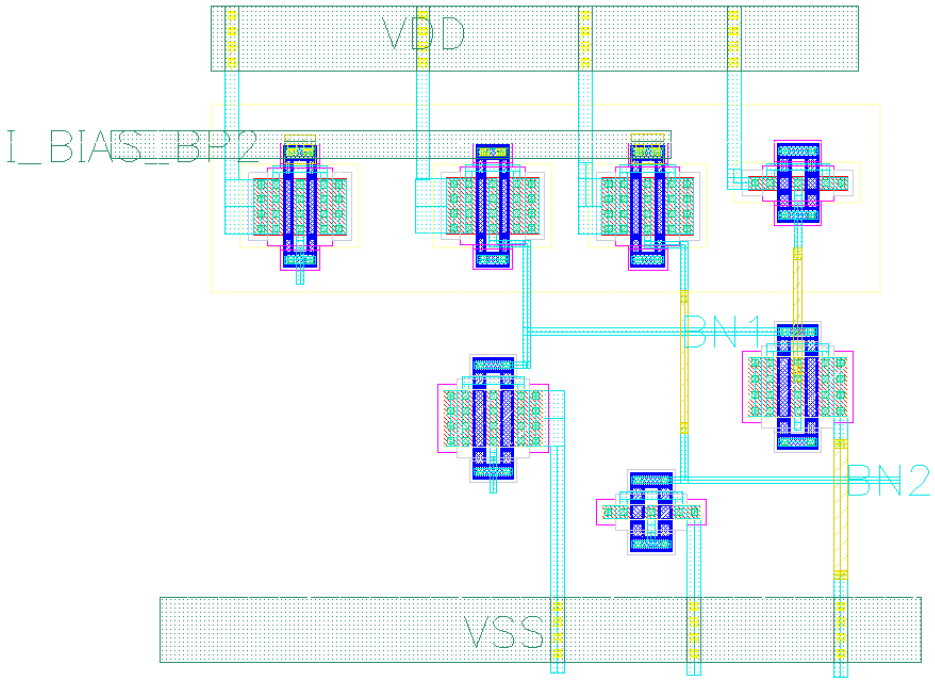

Figure XXIII: Cascode Amplifier Bias Layout