UNIVERSITY OF TORONTO
FACULTY OF APPLIED SCIENCE AND ENGINEERING

ECE241F – Digital Systems
Midterm 1 Assessment

Open October 15, 6:00pm to October 16, 6:00am Toronto time
Duration: 120 minutes (includes the time to upload your solutions)

Examiners: Paul Chow and Belinda Wang

Exam Type X: Open Book. You may use your own notes and books. No design tools, such as *logisim* and *Quartus* are permitted. You may use apps for writing, such as those for note taking or writing on PDFs. No online resources, other than the Quercus notes, are permitted. No external help from others is permitted.

Calculator Type 1: Any type allowed

The number of marks for each question are indicated.

The examination has **14 pages**, including this one.

You do not have to submit your solutions on these pages. You may write your solutions on any media, such as blank paper, or a note-taking app, as long as the background is white. It is only important that you submit your answers clearly.

Revision : 1.4

Question 1 [1 Marks]

If you are unable to print this page for signing, or sign this page through some other means, you may do the following:

(a) On a separate page write, "I have read the First Statement of Academic Integrity and agree to abide by it."

(b) Sign below the sentence you wrote.

(c) You can scan the sheet and upload it.

First Statement of Academic Integrity

To have this assessment graded please read and sign the following:

> I, _____, pledge upon my honour that I will not violate our Faculty's Code of Behaviour on Academic Matters during this assessment by acting in any way that would constitute cheating, misrepresentation, or unfairness, including but not limited to, using unauthorized aids and assistance, impersonating another person, and committing plagiarism. I acknowledge that providing unauthorized assistance to someone else is also considered a serious academic offence.

Question 2 [6 Marks]

Assuming all numbers are unsigned integers, do the requested number conversions. You must show your work so that we can understand how you arrived at your solution.

hexadecimal A9 to

12-bit binary

decimal

decimal 241 to

12-bit binary

hexadecimal

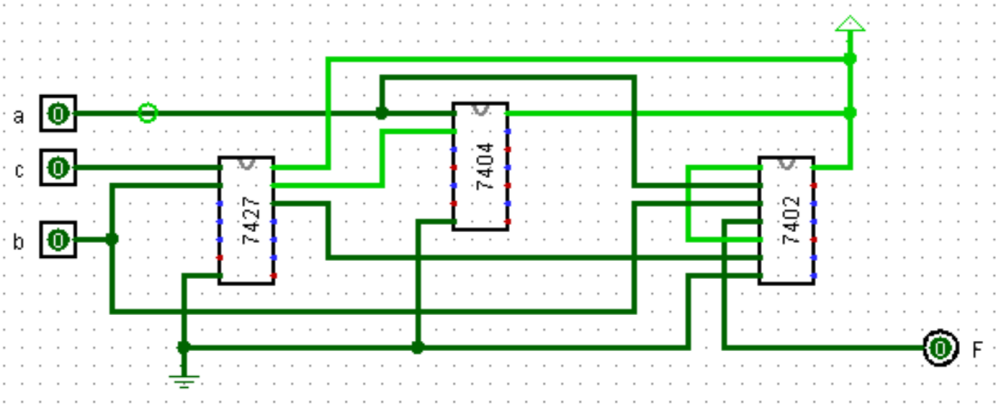
binary 0011 1011 0100 to

hexadecimal

decimal

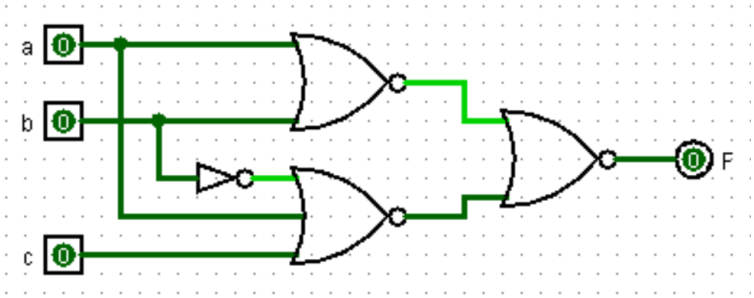
Question 3: **[12 marks]**

a) **[4 marks]** The following circuit diagram is created using Logisim. Draw the corresponding circuit using logic gates. Note: see the Lab1 document for the chip information.



b) **[2 marks]** After you have built the circuit, you find that the output is incorrect. Remember that, in reality, these are physical chips, so you cannot look inside them. You only have access to the inputs and outputs of the circuit, and the pins of the chips to check the values of each signal. Also, each connection is made with a physical wire that may or may not be broken. You have a Logic Probe, which is a device that you can use to touch a wire or pin and determine whether it is a 1 or 0. Describe how you would find the problem.

c) For the logic circuit given below,



i) **[2 marks]** write the logic expression for the output function, *F* in Product-of-Sums (PoS) form.

ii) **[4 marks]** Derive the simplest logic expression using Boolean algebraic properties, for *F* in Sum-of-Products (SoP) form. Show your work. State the rules that you have used.

Question 4: **[10 marks]**

a) **[2 marks]** For the given logic function, $f(a,b,c,d) = \sum m\,(0,2,4,8,10,12) + \sum D\,(5,7,15)$ where D represents "don't care". Note: To be clear about ordering, the term m_5 would be represented by the product term, $\bar{a}b\bar{c}d$. Fill in the Karnaugh map (K-map) below.

c d \ a b	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

b) **[4 marks]** For the K-map shown below, determine the minimum-cost SoP expression for function *f* and find the cost of implementing the function using AND-OR-NOT gates. All inputs are only available in their true form. If an inversion is required, then you will need to add that to your circuit and count it in your cost. The AND and OR gates can have any number of inputs.

c d \ a b	0 0	0 1	1 1	1 0
0 0	1	1	1	0
0 1	0	x	x	0
1 1	0	x	x	0
1 0	1	1	0	1

c) **[4 marks]** For the K-map shown below, determine the minimum-cost PoS expression for function *f* and find the cost of implementing the function using only NOR gates. All inputs are only available in their true form. If an inversion is required, then you will need to add that to your circuit and count it in your cost. The NOR gates can have any number of inputs.

c d \ a b	0 0	0 1	1 1	1 0
0 0	1	1	1	0
0 1	0	x	x	0
1 1	0	x	x	0
1 0	1	1	0	1

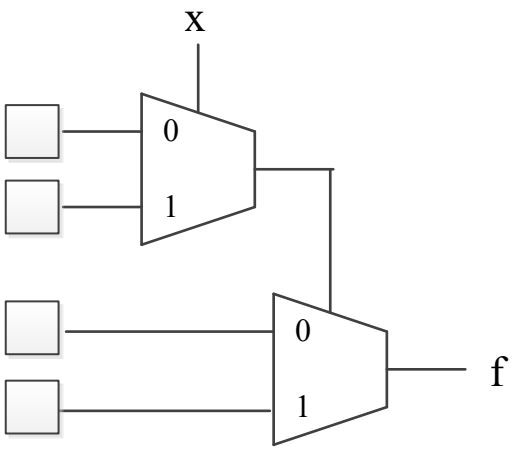
Question 5: **[8 marks]**

a) **[3 marks]** Prove or disprove $\bar{x}y + x\bar{y} = xy + \bar{x}\bar{y}$ using Venn diagrams.

b) **[5 marks]** Prove or disprove $x \oplus y \oplus (xy) = x + y$ using Boolean algebra manipulations. Show your work and state the rules that you have used.

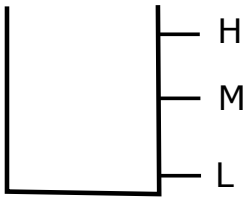
Question 6: **[4 marks]**

Fill in the boxes on the left side of the diagram shown below with the choices of 0, 1, Y, Z, to implement the logic function, $f = Z + \bar{X}Y$. If you are answering on another piece of paper, just draw the four boxes in the same orientation and fill them in. You do not have to draw the whole circuit.



Question 7 [10 Marks]

There are four water tanks, each with three sensors (H,M,L) as shown in the figure below. If a sensor is touching water, then it will output a 1. For example, if the water is just above the M sensor, then the sensors will read (0,1,1), i.e., H is off, but M and L are on.



You are asked to design a circuit that can be used to show the level of the water as 2, 1, or 0 on a seven-segment display according to the following table:

2	Water is above H
1	Water is between M and H
0	Water is between L and M

Since there are four tanks, there will be two switches (S1,S0) to select which tank level to display.

Hint: To get started, you will need to design a circuit that takes the inputs from H, M and L and output a two-bit value that corresponds to the current level, i.e., if (H,M,L) are (0,1,1), then the output of the circuit will be (B1,B0) = (01), where B1 and B0 are the signal names for the two bits.

Full marks for this question is a solution that shows you know what to do, and given time, you could get all the details filled in. Here, just convince us you know what needs to be done.

[8 Marks] Your grade will be mostly based on how you approach the problem, rather than achieving a fully working solution. For example, if you need to minimize an equation, you can just say, using technique X, we can simplify the equation and then go on to describing the next step. Your solution should describe clearly the steps you are taking.

[2 Marks] Your final solution should be written in Verilog. Minor syntax errors will not be penalized. Again, details are not as important as showing what modules you require and how they are instantiated and connected. If there is a module from the Quercus notes that you can use, you do not need to write it out here. You can just refer to the module by name in the following manner:

```
module mytop(input x, y, z, output a, b);

   mux2to1 U1 (x, y, z, a);
   mux2to1 U2 (x, y, z, b);
   ...

endmodule

declare mux2to1 from Quercus Module 6.2
```

Question 8 [1 Marks]

As with Q1, if you are unable to print the next page for signing, or sign the next page through some other means, you may do the following:

(a) On a separate page write, "I have read the Final Statement of Academic Integrity and agree to abide by it."

(b) For Part (d) of the statement, write down "Part (d), the statement number (i, ii, or iii) and any required information, if needed."

(c) Below what you have written, sign your name and print your name, the date, and your city.

(d) You can scan the sheet and upload it.

Final Statement of Academic Integrity

In submitting this ECE241 Digital Systems assessment, I confirm the following:

(a) My conduct during this assessment adheres to the Code of Behaviour on Academic Matters of the Faculty of Applied Science and Engineering of the University of Toronto. I confirm that I did NOT act in such a way that would constitute cheating, misrepresentation, or unfairness, including but not limited to, using unauthorized aids, receiving assistance from another person, impersonating another person, and committing plagiarism.

(b) I acknowledge that this assessment is open book and I have only used my own notes and books. I have not used any online resources or consulted with any other person.

(c) I did not provide unauthorized assistance to anyone else writing the assessment.

Continued on next page

(d) I acknowledge one of the following statements regarding time spent on the assessment. Circle the applicable statement, and fill in the blanks where appropriate.

(i) I spent no more than 2 hours between first accessing the final assessment questions on Crowdmark, and completing the submission of all components of the assessment.

(ii) I received authorization from Professor Chow via email to spend _____ hours and _____ minutes on this assessment. I spent no more than the authorized amount of time.

(iii) I spent more than either 2 hours or the previously authorized time limit due to the reasons described below (e.g., power failure, Internet disruption).

Total time spent: _____

Explanation:

I pledge upon my honour that my conduct during this assessment is in compliance with the statements above.

I further pledge that I will not provide unauthorized aid to anyone else in the class who may be writing this assessment at a later time.

Signature _____

Name (print or type) _____

Date _____

City _____