adders_Questions

Question 1:
Design a full-adder, using AND-OR-NOT gates. Write the Verilog code for the full-adder using primitive gate instantiations instead of continuous assignment statements.

Question 2:
Design a 4-bit ripple-carry adder. Write the Verilog code for the ripple-carry adder using

a) Module instantiation by port (as shown in the video)
b) Module instantiation by name