Research Progress on Memristor: From Synapses to Computing Systems

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***Abstract*— As the limits of transistor technology are approached, feature size in integrated circuit transistors has been reduced very near to the minimum physically-realizable channel length, and it has become increasingly difficult to meet expectations outlined by Moore's law. As one of the most promising devices to replace transistors, memristors have many excellent properties that can be leveraged to develop new types of neural and non-von Neumann computing systems, which are expected to revolutionize information-processing technology. This survey provides a comparative overview of research progress on memristors. Different memristor synaptic devices are classified according to stimulation patterns and the working mechanisms of these various synaptic devices are analyzed in detail. Crossbar-based memristors have demonstrated advantages in physically executing vector-matrix multiplication and enabling highly power-efficient and area-efficient neuromorphic system designs. The extensive uses of crossbar-based memristors cover in-memory logic, vector-matrix multiplication, and many other fundamental computing operations. Furthermore, memristor-based architectures for efficient neural network training and inference have been studied. However, memristors have non-ideal properties due to programming inaccuracies and device imperfections from fabrication, which lead to error or mismatch in computed results. To build reliable memristor-based designs, circuit-level, algorithm-level, and system-level solutions to memristor reliability issues are being studied. To this end, state-of-the-art realizations of memristor crossbars, crossbar-based designs, and peripheral circuitry are presented, which show both promising full-system inference accuracy and excellent power efficiency in multiple tasks. Memristor in-situ learning benefits from high energy efficiency and biologically-imitative characteristics, which are conducive to further realizing hardware acceleration of cognitive learning. At present, the learning and training processes of brain-like networks are complex, presenting great challenges for network design and implementation.**

Manuscript received December 17, 2021; revised February 14, 2022; accepted March 9, 2022. Date of publication March 21, 2022; date of current version April 28, 2022. The work of Ailong Wu was supported in part by the Natural Science Foundation of China under Grant 61976084 and in part by the Natural Science Foundation of Hubei Province of China under Grant 2021CFA080. This article was recommended by Associate Editor M.-F. Chang. *(Xiaoxuan Yang and Brady Taylor contributed equally to this work.) (Corresponding author: Yiran Chen.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSI.2022.3159153.

Digital Object Identifier 10.1109/TCSI.2022.3159153

***Index Terms*— Memristor, memristive devices, processing-in-memory, reliability, in-situ learning, neuromorphic computing.**

I. Introduction

MEMRISTORS were originally proposed by Prof. Leon Ong Chua in 1971 as a fundamental circuit device representing the relationship between magnetic flux and charge [1]. In 2008, researchers from HP Labs created a nanoscale memristor device for the first time and provided corresponding mathematical models and circuit simulations matching Prof. Chua's descriptions [2]. Due to its high density, low access energy, and nanoscale dimensions, the memristor has been regarded as one of the most promising emerging non-volatile memory technologies. Utilizing memristors to store data is area-efficient due to their ability to store multiple bits per cell. Programming and reading data from memristors is achieved through applying voltage across the memristor above and below a threshold, respectively. Furthermore, memristor cells can be integrated into memristor arrays, crossbars, and cubes (through 3D integration [3]) for improved density.

In addition to data storage functions, memristor crossbars can realize vector-matrix multiplication (VMM). With analog voltages applied to each row, the memristor crossbar can accumulate currents along each column [5]. According to Kirchhoff's law, the output current for each column is the sum of products of voltage applied at each row multiplied by memristor conductance at each row. Therefore, the crossbar can compute using the memory itself, which significantly mitigates the communication burden of data for each operation. Fig. 1 gives an example of memristor-based vector-matrix multiplication. Memristor crossbar-based designs have been popular in many recent neural network architectures [6]–[8] due to their ability to implement VMM operations with high energy efficiency.

However, the non-idealities of memristor devices are of great concern for developing reliable memristor-based architectures. Errors in conductance stored by memristor cells, for example, cause errors in vector-matrix multiplication results. Memristor reliability issues include device faults, device endurance, IR-drop, variation, and noise. Therefore, effective circuit-level, algorithm-level, and system-level solutions are necessary to mitigate reliability issues and enable the reliable design of memristor-based neuromorphic computing systems.

Based on the discussion of memristor crossbar-based designs, this survey also presents state-of-the-art realizations

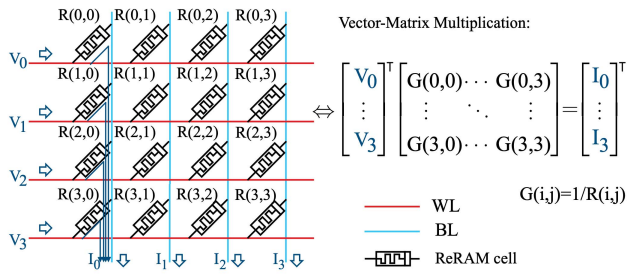

Fig. 1. Memristor-based vector-matrix multiplication [4].

of memristor crossbars and peripheral circuit designs, demonstrating both promising full-system inference accuracy and high power efficiency for many workloads.

Memristor-based in-situ learning networks feature outstanding energy efficiency and biologically-imitative qualities, making them ideal for furthering the hardware acceleration of cognitive learning. However, the training processes and learning of brain-like networks are highly sophisticated. Therefore, there are significant obstacles to the design and implementation of memristor-based in-situ learning networks.

In this survey, perspectives on the state-of-the-art research progress surrounding the memristor are provided, from synapses to computing systems. The organization of this paper is as follows: In Section II, the benefits of memristor synapses and specific synaptic structures are introduced. In Section III, the details of memristor crossbar-based designs are analyzed, particularly for in-memory logic, vector-matrix multiplication, and neural network architectures. The causes and potential solutions for memristor reliability issues are explained in Section IV. In Section V, the state-of-the-art of memristor crossbar realizations and performance are presented. In Section VI, the hardware and software considerations of memristor-based in-situ learning networks are discussed. Finally, Sections VII and VIII discuss challenges and possible future work in the study of memristors.

II. Memristor Synapses and Neurons

The synapse is the unit where biological neurons connect with each other and transmit information. The human brain contains more than 10 million neurons, each of which is connected to more than 2,000 synapses. Hence, the design and implementation of synaptic circuits are very important in the construction of artificial neural network hardware. However, traditional synaptic simulations use transistor circuits, which have two main disadvantages: state volatility and the difficulty of repetitive programming, which limit applications of transistor synapses in large-scale artificial neural networks.

The emergence of physical memristor devices opens up new possibilities for synaptic hardware simulation. Many neural circuits consist of three basic processing modules: Multiplication, accumulation, and activation. Synthesizing the weighted signals and activating the outputs of multiple synapses are key to neural circuit design. Memristors are especially suitable for realizing synapses in artificial neural circuits for the following reasons [9]: Firstly, the conductance of a memristor can represent synaptic weight and can be changed by different applied voltages. Secondly, memristors are simple two-terminal devices, which can realize high-density, integrated crossbar-array structures. In addition, their nanoscale size, low power-consumption, and non-volatile memory properties make the structure of the memristor synapse smaller and more efficient than conventional transistor synapses.

Expanding on the fundamentals of memristor synapses, researchers have proposed different types of synapse structures, including five-memristor synapses [10], one-transistor and one-memristor (1T1M) synapses [11], and two-transistor and one-memristor (2T1M) synapses [12]. In order to achieve efficient synaptic operation, many different memristor synapses have differing topologies, such as memristor bridge circuits and memristor/double-memristor synaptic arrays. The former has a complex structure, which is not convenient for large-scale integration. In the latter, because the structure of memristors in the array is intersect-linked and fixed, the corresponding row or column of the array must be selected in advance when programming a memristor weight. This makes the relevant circuitry unable to achieve full parallel weight programming. Therefore, further work to construct new circuits to achieve large-scale parallel weight adjustment is required. Chen *et al.* [10] proposed a synaptic circuit composed of five memristors. This circuit can execute positive and negative synaptic weights, in which only one memristor is used for weight calculation, and the other four memristors are used for symbol-setting. In order to realize bidirectional control of a single memristor, Dubey *et al.* [12] proposed a 2T1M synaptic structure, which uses two CMOS switches to control the input of positive and negative signals. Furthermore, some memristor synaptic structures have been proposed to simulate spike-timing-dependent plasticity (STDP) in spiking neural circuits, which further verifies the advantage of memristors in simulating synaptic learning for brain-inspired computing [13].

Another widely used memristor synaptic structure is the memristor crossbar array, in which a synaptic weight is expressed by the conductance of memristors connecting each crossing of a word-line and orthogonal bit-line. Through the electrical characteristics of the memristor, the array can easily execute large-scale matrix multiplication, which can be used to speed up the operation of neural networks. In order to independently control the write/read operation of each memristor in the crossbar array, many 1T1M array structures have been proposed. Given that a single memristor can represent positive synaptic weights only, Ai *et al.* [14] proposed double-memristor synaptic crossbar arrays to represent positive and negative synaptic weights, and kernel weights are defined as the element-wise difference in conductance between the two memristor arrays. CMOS-memristor hybrid technology can achieve fully-parallel programming operations that classical crossbar arrays cannot. These crossbar circuits combined with the inherent computing characteristics of memristor arrays can achieve large-scale feedforward parallel computing that significantly improves computing speed compared to serial computing techniques.

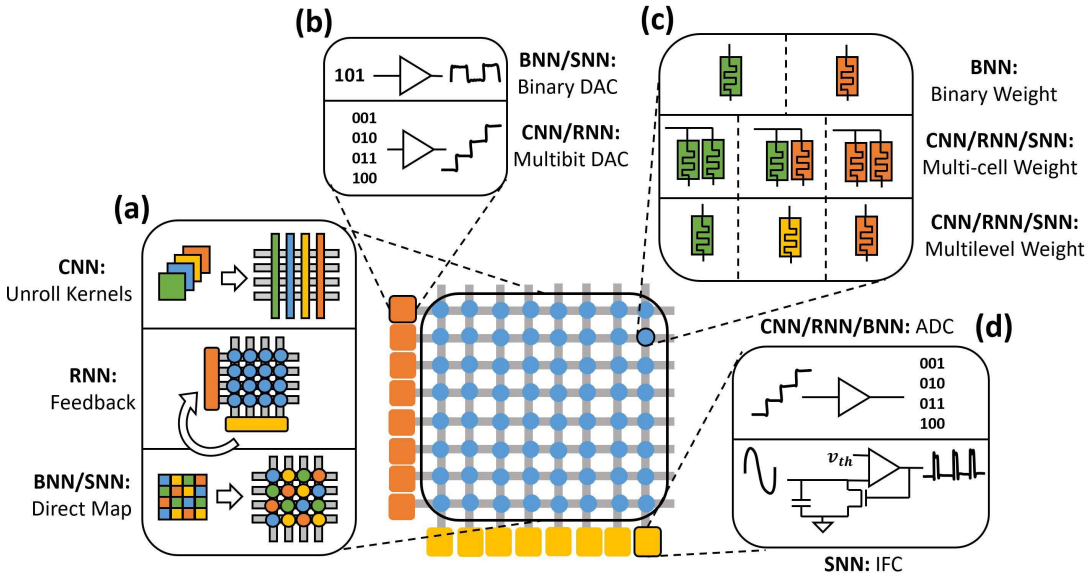

Fig. 2. Breakdown of major components in memristor crossbar-based applications: (a) Data is mapped in many ways to facilitate different applications. In the top section, CNN weight kernels are unrolled and mapped to crossbar columns as conveyed by the colored bars. In the middle section, output data is fed back to input drivers in RNN architectures. In the bottom section, weights are directly mapped to each cell of the crossbar as conveyed by the colored boxes. (b) Input drivers can include simple buffers for generating binary pulses for BNNs/SNNs, and DACs for converting digital inputs to analog voltages. (c) Memristors can represent a binary weight when in either low- or high-resistance states (LRS/HRS). They can also be tuned to specific resistances in multilevel weights, or multiple memristors across several columns can represent a single, high-precision multicell weight. (d) In the output stage, ADCs can convert current or voltage outputs into digital signals, or IFCs can be used in SNNs to convert current to spiking voltage outputs.

III. Crossbar-Based Memristor Designs

Memristors can be naturally used for vector-matrix multiplication (VMMs). A memristor-based crossbar array has word-lines (WLs) and bit-lines (BLs) that are orthogonal to each other. An input vector is encoded as analog voltages and applied to the crossbar, while the matrix is represented as conductances of the memristors and stored at each cross-point. According to Kirchhoff's current law, the VMM result is equal to the current through each crossbar column [15]. With the help of peripheral circuitry, memristor crossbar arrays support processing-in-memory (PIM) operations, including in-memory logic and memristor-based VMM. In this section, different types of memristors are examined. Then, the use of crossbars in various computing tasks is discussed. Fig. 2 provides a summary of memristor crossbar applications, including the cell design and peripheral circuits used for different neural networks.

A. Types of Memristor

Basic and common cells for memristor crossbars are categorized into one-memristor (1M) [16]–[18], 1T1M [11], [19], [20], one-selector and one-memristor (1S1M) [21]–[23], and one-diode and one-memristor (1D1M) [24], [25]. Besides these, there are one-transistor and multiple-memristor (1TnM) [26] as well as 2T1M [27] designs.

Utilizing 1M for each cell to construct the memristor crossbar demonstrates high area density and high power efficiency [17]. However, sneak path (i.e., the undesired current flowing through unselected cells) can disturb the accurate programming and reading of cells in the crossbar [28]. To suppress the sneak path problem, sensing methods with precise voltage control [29] and reading schemes with reference to the sneak current [30] have been proposed. Outside of these algorithmic approaches, the memristor can be integrated with other components to avoid sneak path problems. For instance, 1T1M, 1S1M, and 1D1M can be viewed as potential candidates for reliable memristor computing. Self-selective and self-rectifying memristors also show great potential for solving the sneak path current issue with a simple structure [31].

1T1M cells integrate a transistor with a memristor and are thus highly compatible with the CMOS process. Furthermore, 1T1M arrays can support the parallel programming of memristor cells in a row or column. More importantly, the gate in the transistor can precisely control linearity and symmetry in weight programming. However, the larger cell area compared to 1M designs constrains area efficiency. Moreover, when considering high-dimension integration, the 1T1M design also has sneak and leakage current issues [32].

1S1M designs, with the same area consumption as 1M designs, have high area efficiency and are potentially scalable to 3D. Selectors with high non-linearity are preferable for achieving high power efficiency and programming accuracy.

1D1M designs integrate a diode with each memristor. However, this design cannot program bipolar memristors since the reverse current of a diode is very small.

B. Crossbars for In-Memory Logic

Binary memristor crossbars can be used to implement in-memory logic [33], [34]. Memristor-aided logic (MAGIC) [33] is the first work of its kind to support in-memory logic with memristor devices, and it analyzes the range of the voltage needed to guarantee successful switching behavior for each logic operation. Here, an example of the operation of

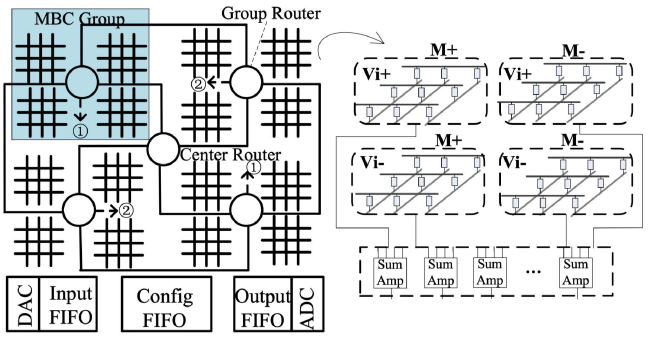

Fig. 3. Memristor-based reconfigurable neuromorphic computing accelerator architecture [38].

implementing NOR logic with memristors is given. Firstly, the input cells, as well as the output memristor cell, are all placed in the same row. Input cells starting with unknown status will be programmed to store the input values as conductance states. In the NOR implementation, the output cell is initialized to high resistance first. In the first cycle, the p terminals of the input cells are set to an execution voltage, while the p terminal of the output cell is grounded. As a result, the output cell will switch to a low resistance if there exists at least one high resistance cell among input cells. This NOR operation only takes a single cycle. Following the FELIX design [34], memristor-based logic for INV, OR, and XOR operations can be executed within one, two, and two cycles, respectively.

Single memristor-based logic gates (such as NOR) can be further utilized to fulfill more complex functionalities, such as addition [35] or multiplication [36]. Similarly, digital processing-in-memory designs can be built with memristors. For instance, Imani *et al.* [37] proposed a digital memristor-based computing system named FloatPIM, which enables floating-point representation and calculations with single-bit memristors. Moreover, Yang *et al.* [4] exploited memristor-based in-memory logic techniques to implement a memristor-based hybrid softmax design. While memristor-based in-memory logic benefits from substantial parallelism by executing the same operation on many rows simultaneously, the minimization of data transfer, and the very high density of memristor arrays, its practicality suffers from the low endurance of memristor technology to reprogramming resistive state, as well as the duration required by multiple write operations for a single logic operation. The endurance issue will be further addressed in section IV.

C. Crossbars for Vector-Matrix Multiplication

Hu *et al.* [5] first proposed the use of memristor crossbars for vector-matrix multiplication (VMM). To support VMM calculations, the network's weights and activations should be mapped to each memristor's conductance and crossbar input voltages according to the resolution of the memristor devices and digital-to-analog converters (DACs), respectively [38]. A design of memristor-based reconfigurable neuromorphic computing accelerator (RENO) architecture is shown in Fig. 3. When memristor cell resolution is lower than the weight quantization bit number, multiple cells can be used to represent a single weight parameter. Since the memristor conductance can only represent positive values, the difference of the results from two arrays is utilized to represent both positive and negative values [39]. A kernel in a convolutional layer needs to first be unrolled and mapped to a crossbar, while a kernel in a fully connected layer is mapped directly to a crossbar [6]. The memristor computation process accumulates the calculated results from crossbars and uses analog-to-digital converters (ADC) to generate outputs. Note that VMM operations in memristor crossbars do not require repeated reprogramming of memristors as for in-memory logic and therefore do not suffer from endurance issues, but repeatedly "reading" these memristors during VMM operations can slowly alter device state. This issue is further addressed in section IV.

D. Crossbars for Neural Network Architectures

Memristor-based crossbars have become indispensable for implementing neural network architectures in the analog domain. As crossbars provide an efficient and nigh-instantaneous means of physically emulating VMM operations, different neural network algorithms such as convolutional, spiking, and recurrent neural networks can be executed by architectures that process and transport data in the form of voltages or currents between memristor crossbars. In this section, architectures for convolutional, spiking, and recurrent neural networks are briefly explored, as well as the methodologies and physics that enable them.

1) Convolutional Neural Networks: Convolutional neural networks (CNNs) are by far the most readily explored derivative of neural network algorithms for memristor-based architectures due to the ability of CNNs to efficiently extract the spatial information of data. PRIME is one of the earliest crossbar-based architectures for neural networks capable of implementing either multilayer perceptrons (MLPs) or CNNs [7]. CNN kernels are trained offline and mapped to crossbars, with both positive and negative weights represented by the column-wise difference in outputs of two separate crossbars. PRIME uses multiplexers that attach the columns of the crossbar to computational logic or write/read logic, depending on whether the array is enabled for memory or computational mode. The WL drivers can drive different analog voltages in either mode. In computational mode, the column currents for the positive and negative arrays are passed through analog subtractor and sigmoid circuits. The digital output is generated by converting the column current to a voltage and comparing the voltage to the voltage sources. The sign of the output is stored as the MSB of the output, which can be used as the select signal of a ReLU activation function if desired. PRIME brings further attention to the issue of activation and parameter precision, pointing out that both are factors in the precision of output data. While activation precision depends on the circuitry driving the crossbar array, parameter precision can be achieved either through using multiple single-bit memristor cells to represent a single parameter or through multilevel memristors [40], [41].

ISAAC expands on the concept of crossbar-based CNN architectures [8] by incorporating pipelining. The architecture

uses a network of tiles in which each tile has several crossbar units along with ADCs, shift-and-add logic, and registers. As kernels in CNNs only work on portions of the feature map at a time, there is no need to wait for all outputs of a layer to be produced before beginning to process the next layer. Furthermore, resources within each tile can be pipelined so that the next slice of a feature map can be sent to a crossbar without waiting for the previous slice to finish the conversion to a digital value. Shift-and-add logic is also necessary if kernels map to more than a single crossbar.

PipeLayer [6], beyond including training of kernels into the architecture, changes up the pipeline of ISAAC and deeply explores the mapping of kernels and activations to crossbars. Kernels are reshaped into 1-D vectors and are mapped to single columns of multiple arrays (represented once again by separate positive and negative arrays, as well as being split amongst multiple arrays if the kernel is larger than the height of a single array). The feature map is split into 1-D vectors that are applied to the rows of the arrays to generate dot-products with each kernel. While fast, this method comes at the expense of replicating data in the feature map. Each vector of the feature map must be applied to the kernels one at a time, but duplicating the kernels with identically-mapped crossbars can accelerate the processing of the feature map at the expense of utilizing more arrays. Other works, such as MobiLattice [42], show the benefits of using mixed-signal processing to minimize the under-utilization of crossbar arrays, while works like 3D CNN [43] utilize 3D crossbars for an even denser realization of CNN architectures.

2) Spiking Neural Networks: Spiking neural networks (SNNs) refer to the encoding of input and output activations of a neural network as voltage spikes. Popular digital SNNs exist commercially, including IBM's TrueNorth and Intel's Loihi [44] [45]. Work in this area of crossbar-based neural networks largely involves the design of peripheral circuitry. PipeLayer is a partial implementation of an SNN [6], using an integrate-and-fire circuit (IFC) to convert an analog current into a spiking voltage signal, and then into a digital output. The IFC is a staple of crossbar-based SNN implementations [46]. In an IFC, the current from the column of a crossbar is integrated by a capacitor into a proportional voltage. When this voltage reaches the predetermined threshold voltage, a comparator's output rises, activating a transistor in parallel with the capacitor to discharge it. The comparator's output falls back down, creating a spiking signal that can be buffered as input to subsequent layers, or, in the case of PipeLayer [6], a digital counter can count the spikes produced during the compute time to estimate the IFC's spiking rate.

Several aspects of this circuit can be optimized for improved performance and efficiency. To ensure that the current from the column doesn't change as the capacitor of the IFC charges, a current amplifier can be used to hold the voltage at the column constant, thereby charging the capacitor linearly [39]. This optimization is compatible with designs where two arrays are used to represent positive and negative parameters, using the amplifier to both subtract the currents and hold the column voltage constant. The addition of a buffer between the output of the IFC's comparator and the transistor in parallel with the capacitor can introduce a nonlinear activation function akin to a hyperbolic tangent function to the output spiking signal [47]. The delay of the buffer causes the spiking rate of the IFC to saturate to a value based on the current amplifier's reference voltage and the IFC's threshold voltage, such that the output spiking rate of the IFC increases linearly with column current up until the saturation rate. As for the input circuitry of an SNN, the input activation of an SNN can also take several different forms, including a simple analog voltage as seen in PipeLayer [6], another spiking waveform (as in TrueNorth [44] and Loihi [45]), or a pulse-width modulated (PWM) signal [48]. In the latter case, the signal is represented by an input signal where the duty cycle of a pulse corresponds to the digital input value. This approach benefits from higher precision capabilities and use of efficient digital circuits instead of expensive DACs.

3) Recurrent Neural Networks: Recurrent neural networks (RNNs) differ from other models in that the output depends upon both current inputs and previous outputs. For one implementation of an RNN [49], two arrays are used. The first array is split into two sections of WLs, with the current from both sections being aggregated by the hidden layer neurons. The first section of WLs is driven by the input neurons, while the second section of WLs is driven by feedback connections from the hidden layer neurons. Finally, the second array is also driven by the hidden layer neurons, connected through the crossbar to the final output layer neurons. In the neuron circuit, an integrator converts the current to voltage and is modulated by an activation function implemented via a voltage follower circuit. However, this architecture implements a vanilla RNN only, an algorithm that can suffer from the vanishing gradient problem during training. In a newer architecture [50], long short-term memory (LSTM) and gated recurrent units (GRUs), which avoid this problem, are implemented. These algorithms require element-wise multiplication and different types of activation functions (hyperbolic tangent and sigmoid), both of which are executed digitally. This architecture pipelines the crossbar-based VMM, the activation functions, and the element-wise multiplication in three separate stages and can therefore process three separate sequences simultaneously. Note that elements of the same sequence cannot be in the pipeline simultaneously, as processing one element requires that the previous element has already been processed. In another architecture [51], the VMMs are executed by the crossbar as usual, and software is used for activation functions and element-wise multiplication of the data. Other LSTM designs [52] [53] [54] opt for a completely analog design in which an analog activation circuit is used and the element-wise multiplication is performed by a voltage multiplier circuit.

4) Binary Neural Networks and Other ML Applications: Through the various neural networks mentioned above, memristor-based processing-in-memory designs show their potential in accelerating networks with high energy efficiency. However, when implementing these complex networks, memristors with multilevel states are preferable, while multiple memristor cells may be required to represent one full-precision weight value in the network. This multilevel cell is more

vulnerable to noise, and reliability issues will be discussed in the next section. Furthermore, the integration of multiple cells will increase the energy and area overhead. Therefore, memristor-based designs can further boost their performance when executing hardware-friendly networks, such as binary neural networks (BNNs) [55]–[58]. Tang *et al.* [55] proposed using a memristor crossbar as a processing engine to implement a BNN and discussed the matrix splitting problem when supporting large weight kernels. Sun *et al.* [56] put forward a parallel XNOR-RRAM architecture with a bit-cell design and enabled parallel read-out mode to improve performance. Song *et al.* [57] proposed a complementary resistive cell design for XNOR activation, and thus enabled in-situ BNN computations in memristors. Other forms of crossbar-based machine learning and neural network algorithms have also been developed, including reinforcement learning [59], generative adversarial networks (GANs) [60] [61], natural language processing (NLP) [4], and algorithms that utilize the sparsity of feature maps (such as in deconvolution) for efficient inference [61] [62]. Other general-purpose memristor-based processing-in-memory designs provide energy-efficient solutions in genome sequence alignment [63]–[66], graph processing [67]–[69], and scientific computing [70]–[72].

A simulation framework for memristor-based crossbar systems is essential to evaluate the performance, energy, and area consumption under neural network tasks. Representative frameworks include NVSim [73], MNSim [74], NeuroSim [75], RxNN [76], Pytorx [77], and the analog in-memory computing toolkit [78]. These frameworks enable fast, accurate, and flexible designs and validate the performance considering the overall architecture.

IV. Reliability Issues in Memristors

Memristor-based designs have demonstrated their potential in enabling fast and efficient neuromorphic computing systems. However, one key challenge in building trustworthy memristor-based designs lies in the non-idealities of memristor devices. For instance, faults in memristor cells introduce errors to vector-matrix multiplication results. Worse still is that the effects of device faults can accumulate through the computing system and result in serious accuracy degradation for deep neural networks. In this section, reliability issues pertaining to memristor crossbars are discussed, including device faults, device endurance, IR-drop, variation, and noise. Based on the analysis of each cause, effective circuit-level, algorithm-level, and system-level solutions have been provided to mitigate these issues and enable the reliable design of memristor-based neuromorphic computing systems. Fig. 4 provides an overview of memristor reliability issues.

A. Device Faults

Memristor device faults caused by fabrication defects and programming processes can be classified into soft faults and hard faults [79]. Soft faults refer to the errors that happen when the memristor conductance differs from the target conductance and can be fixed by re-writing or tuning the memristor conductance. Hard faults refer to the errors in which the memristor state is stuck at a low conductance (i.e., stuck-at-0, SA0) or high conductance (i.e., stuck-at-1, SA1) and cannot be further changed. Therefore, hard faults in memristors are more detrimental to reliable computing systems since they cannot be easily fixed by writing operations [80]. Methods for tolerating hard faults in memristor devices consist of the remapping strategy [79], fault-aware retraining [79], [81], redundancy columns utilization [81], [82], error-correction codes [83], [84], profiling with error compensation [77], and circuit techniques [85]. For instance, Xia *et al.* [79] observed that a neural network has sparsity in its weights, which can be matched to the memristor cells with SA0 faults. Therefore, they suggest reordering neurons to circumvent the SA0 fault. He *et al.* [77] proposed an error correction algorithm to compensate SA0 and SA1 faults, which requires one-time profiling to achieve high inferencing accuracy.

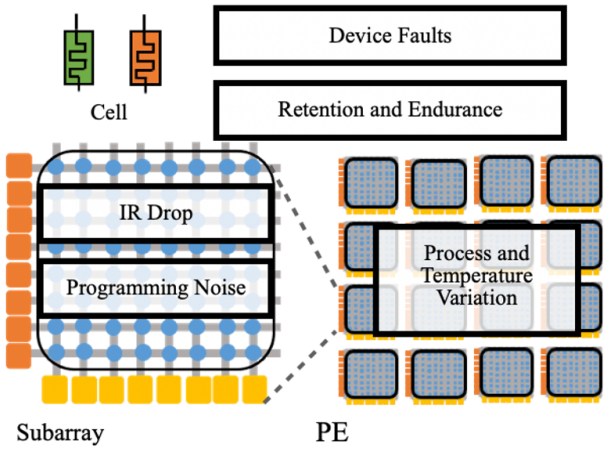

Fig. 4. Overview of memristor reliability issues. Cell level: device faults, retention and endurance issues; Subarray level: IR drop and programming noise issues; processing element (PE) level: process and temperature variation.

B. Retention and Endurance

Memristor devices have the property of high retention time for up to 10 years in some cases [86]. However, they can also experience a memristance degradation issue caused by the oxygen vacancy profile changing due to oxygen diffusion [87]. Chen *et al.* [88] proposed tuning the cycling conditions to minimize filament degradation during usage. Fukuyama *et al.* [89] investigated the optimal combination of writing techniques, including "verify", "finalize verify", and "relaxation effect". Furthermore, the retention problem is closely related to the endurance problem, as there exists a trade-off between these two issues.

Currently, the endurance of a memristor device ranges from 10^6 to 10^{12} [3], [90]–[93]. The endurance problem (also referred to as wear-out or the aging problem) sets an upper bound for reprogramming times and limits the usage of memristor devices in online training. To reconcile the endurance problem with the programming approach, Wen *et al.* [94] proposed using an optimized programming order with reset operations followed by set operations and shortening the reset operations for less significant bits. Zhang *et al.* [95] also put forward a software approach to skew trained weights toward smaller values and a hardware mapping

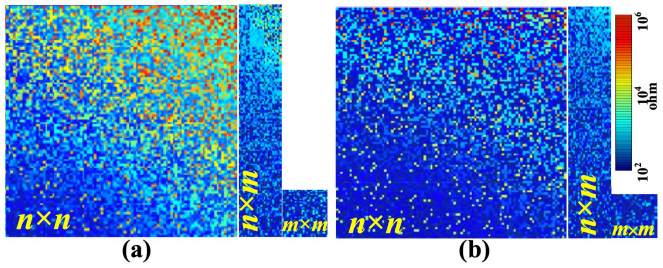

Fig. 5. Trained memristor resistance discrepancy: (a) without IR-drop compensation. (b) With IR-drop compensation [97].

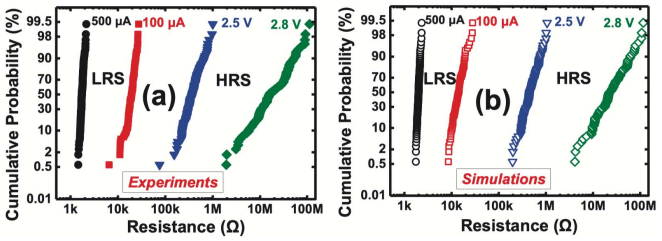

Fig. 6. (a) Measured and (b) simulated complete multilevel cell characteristics with resistance distributions due to cycle-to-cycle variations [98].

approach that considers the aging status of the memristors. Shirinzadeh *et al.* [96] utilized an endurance management framework to balance writing traffic and enhance the potential usage of a memristor-based computing architecture.

C. IR-drop

IR-drop is introduced by wire resistance. Liu *et al.* [97] analyzed the IR-drop phenomenon in various-sized memristor crossbars and put forward reduction and compensation techniques to improve the training and recall performance. As the crossbar size increases, the impact of IR-drop becomes more severe, resulting in performance variations or functional failure in the memristors. Therefore, the 1-D reduction method is put forward to utilize small crossbars for area efficiency and reliability. A large weight matrix (of size $n \times m$) can be decomposed into two smaller matrices (of size $n \times r$ and $r \times m$, where $r \ll m$). The compensation method can also update weights in the recall stage to compensate for the effect of IR-drop. Fig. 5 shows the effectiveness of IR-drop compensation, with the memristor resistance discrepancy minimized. He *et al.* [77] proposed a training method that incorporates the current shift in memristor crossbars due to IR-drop as stochastic noise in the training process.

D. Programming Noise

The programming noise in a memristor can be estimated by a Gaussian distribution or log-normal distribution [98], as shown in Fig. 6. The variation of the programming noise is related to the programmed value (i.e., memristor conductance). The programmed states can be uniformly distributed or nonuniformly distributed [99] among the available conductance range. Since the memristor noise margin is inversely proportional to the number of conductance levels, using a large-resolution memristor cell (such as an 8-bit cell) can be a challenge for the inferencing accuracy as suggested in [100]. Furthermore, multiple memristor cells can be integrated to represent a single weight if the memristor cell's resolution is smaller than the weight's resolution. In this case, programming noise will be multiplied by a scalar during integration, and the programming noise in the most significant bits is of greater concern. Therefore, a dynamic fixed-point representation [101] is utilized to remove the most significant bits which represent zero.

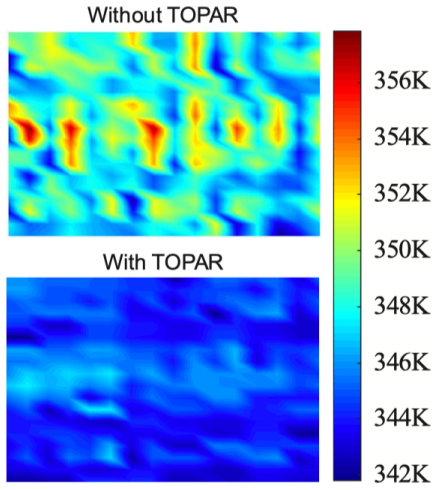

Fig. 7. Thermal distributions of memristor arrays when running the conv2_blk of ResNet50 both with and without the thermal-aware optimization framework TOPAR [107].

E. Process and Temperature Variation

In a memristor-based computing system, process variations are inevitable due to the nanoscale size of the technology [80]. To combat process variations, the sensing strategy can select and activate a limited number of rows in one cycle and provide a large sensing margin [102]. Besides, on-chip ADC reference generation is helpful for mitigating the offsets generated by the process variations [103]. Other than the circuit-level designs, training and mapping technology has been put forward to solve the process variation problem. Hu *et al.* [5] proposed a hardware training method to minimize such problems caused by process variations, where the parameter tuning strategy is based on the difference between the target value and the output value with noise. Yan *et al.* [104] observed that the memristance drift pattern is related to the conductance value and the sensing voltage direction. To mitigate the weight drift, a closed-loop circuit design is proposed that minimizes the difference between the previous recall result and the current result. Chen *et al.* [105] came up with the bipartite-matching mapping method to decrease the impact of large variations in memristors. Moreover, they design a training algorithm to leverage the inherent self-healing capability of a neural network to further prevent large weights from being mapped to a large variation memristor.

Temperature variations, also referred to as thermal noise, is generated due to the thermal agitation of the charge carriers inside the conductor [106]. Shin *et al.* [107] introduced a thermal-aware optimization framework named TOPAR, as shown in Fig. 7, to minimize the temperature variation among memristor arrays. Yang *et al.* [100] proposed a hardware-aware training method to tackle the thermal noise in a memristor-based crossbar. Even at relatively high

temperatures (such as 400 K), the inferencing accuracy of memristor-based designs can be improved.

V. Implemented Designs

In previous sections, examples of concepts and designs that illustrate the basis for memristor crossbar-based designs have been shown. In this section, state-of-the-art realizations of crossbars and accompanying designs are explored. The demonstration results show that memristor-based designs have great advantages in computing efficiency.

A. Crossbar Implementations

Memristor crossbars have made several leaps in progress in terms of speed, size, power consumption, and precision. In a recent review by Xia and Yang [28], a few notable accomplishments in memristor technology are cited that have large implications on implementing a memristor crossbar-based system. Memristor crossbars can be implemented with memristors that are 2 nm on a side and separated by about 12 nm between cells in the crossbar array [108]. Another crossbar with larger memristors (about 50 nm) is capable of switching from 0.73 to 97.83 kΩ or back in 85 ps, using only about 15 μA [109]. In terms of precision, one work reports over 500 possible conductance states [110], allowing for about 9 to 10 bits of precision for a memristor weight. Finally, the largest implemented crossbar is a 128×64 1T1M array [111] [19] [51] [112]. These performance parameters can be useful for optimizing the circuitry that interfaces a memristor crossbar with the other components of an intelligent system. As outlined in previous sections, choosing the right memristor crossbar for a system will depend upon the system's constraints and goals. If the system is meant to execute a large model with many parameters requiring high precision, a 1T1M array would be recommended, while 1S1M or memristor-only arrays can be beneficial in severely size-constrained applications [28].

B. Design Integration

As memristor technology has developed over recent years, so has our ability to integrate crossbars into powerful architectures. While crossbars are limited in size by parasitics and practicality, IBM has developed architectures comprised of up to 1 million memristive synapses [113]. Another recent work [114] demonstrates a memristor crossbar-based system for CNNs fully implemented in hardware. Eight chips (130 nm CMOS technology) were integrated on a printed circuit board (PCB), each of which includes a 128×16 1T1M array, decoding logic, drivers, and multiplexers for operating the arrays in memory or compute mode, 8-bit ADCs, and shift-and-add circuitry. Also included in the PCB were DRAM chips and an ARM microcontroller. The memristors were multicell and capable of 32 different states from 2-20μS, of which 15 states were used for the demonstration. A five-layer CNN was trained for MNIST in Python with an accuracy of 97.99 percent, or 96.92 percent after quantization. When the memristors were programmed and the system was tested, the hardware implementation achieved 95.07 percent accuracy. To account for device variation and programming noise, in-situ training of the fully-connected layer is completed for an epoch, improving the accuracy to 96.19 percent. The resulting computational efficiency of the full system is estimated to be 11,014 GOPS per W. It's worth noting that the ADCs are the largest and most power-hungry blocks of the chip by far.

Another system fully integrates a 54×108 (memristor only) crossbar with on-chip 4-bit DACs, 13-bit ADCs, interface circuits, and an OpenRISC processor in 180 nm CMOS technology [115]. The system is able to achieve an accuracy of 94.6 percent on a breast cancer screening data-set using a two-layer network: the first layer implements principal component analysis (PCA) using online learning [116] on one portion of the crossbar; the second layer performs a single-layer perceptron (SLP) on a separate portion of the crossbar. It is estimated that the system sports a computational efficiency of 187.62 GOPS per W at 180 nm technology, but the authors claim that 1.37 TOPS per W (1,370 GOPS per W) can be achieved with 40 nm technology, not including other potential improvements from reducing the ADC precision or selecting a more efficient processor core.

Slightly more recent works integrate memristor crossbar arrays with CMOS technology directly on-chip to minimize losses due to communication over PCB [102] [103]. These works provide 11.91 TOPS per W for 8-bit input, 8-bit weight, and 14-bit output MACs at 22 nm, and 36.4 TOPS per W for 1-bit input, 1-bit weight MACs at 40 nm, respectively.

VI. Memristor In-Situ Learning Networks

Memristor-based neuromorphic learning can be divided into ex-situ and in-situ learning styles. Ex-situ learning refers to the training of a neural network in software, after which the final weight is written into memristor memory [117]. In contrast, in-situ learning means that every synapse or weight updated is reflected by the updating of memristor memory throughout the entire learning process. That is to say, the conductance of the memristor synapses is updated in real-time [118]. Meanwhile, the calculation of synaptic weight updates can be accomplished through external circuits, sometimes using the memristors themselves in the process. In this way, in-situ learning can adapt to the characteristics and defects of hardware devices and has better learning stability than ex-situ learning. Nevertheless, in-situ learning needs to continually adjust or write memristor conductance throughout the learning process, which can be complicated and difficult to implement.

To avoid the influence of sneak path (i.e., the undesired current flowing through unselected cells) and quickly update the conductances of all memristors, 1T1M structure is preferred in multiple designs. For instance, Dong *et al.* [118] proposed a memristor-based multilayer perceptron (MLP) using the 1T1M synaptic structure and exploited in-situ learning by applying compact extreme learning machine to bimodal memristive synapses. Besides, Ryu and Kim [119] constructed long short-term memory (LSTM) networks via 1T1M synapses to achieve in-situ learning. In fact, for in-situ learning, accurately adjusting the memristor conductance according to the weight value is also a challenge. A naïve solution is to utilize linear models to calculate the duration of voltage pulse corresponding to the variation of conductances, whereas this approach cannot be applied to the actual nonlinear memristor. For 1T1M synaptic, the programming of conductance can be controlled by the voltage-gated amplitude of the transistor.

Here, an example of a memristor-based LSTM circuit with in-situ learning ability is presented [120]. In this example, a type of memristor-based LSTM circuit with in-situ learning ability [120] is designed, which consists of memristor-based LSTM cells, a memristor-based fully-connected layer, and a winner-take-all (WTA) module. To fulfill the LSTM functionality, memristor-based LSTM circuits are equipped with feedforward and recurrent structures and have the ability to process time-series data, and then in-situ learning is operated by updating the memductances in the memristor-based LSTM circuit in parallel.

Recently, some explorations are to design HTM spatial pooling with memristor crossbar circuits [121]. The characteristics of this HTM spatial pooling with memristor crossbar circuits are as follows: (1) It can accomplish the functions of strength and state of synaptic connections at the same time; (2) Local region suppression with fixed radius is used to replace global suppression. For the input with topological structure, local region suppression is more effective than global suppression; (3) WTA circuit is applied to perform suppression operation; (4) By developing in-situ updating strategy that can renovate the strength and state of synaptic connections in parallel, the learning process is completely realized by the designed circuit, then the training of spatial pooling is accelerated. Based on on-device training, the HTM spatial pooling with memristor crossbar circuits is trained by competitive Hebbian learning rule. Although it is not as accurate as of the back propagation algorithm, it has the advantages of fast execution, simple circuit implementation, and low power consumption. Moreover, HTM spatial pooling with memristor crossbar circuits solves the problems of full implementation and insufficient parallelism for spatial pooling synapse that previous spatial pooling circuits suffer bottleneck.

VII. Challenges in Memristor Studies

In recent years, more and more researchers have begun to study the properties of memristors and establish more realistic memristor models. In order to explore the properties of memristors, different mathematical models of memristors are compared [122]. For example, the switching properties of TiO_2 based memristors are described in more detail in [123]. Simultaneously, different SPICE models of memristors and their applications in circuit design are investigated [124], [125]. One significant challenge is designing circuit models that can meet the requirements of existing memristor devices. Therefore, new memristor models are constantly established, including magnetic flux-controlled memristor models [126], threshold adaptive memristor (TeAM) models [127], and voltage-controlled threshold adaptive memristor (VTeAM) models [128]. However, each existing memristor model still cannot fully satisfy all demands of memristor circuit simulations. For example: (1) Magnetic flux-controlled memristor models lack threshold characteristics; (2) TeAM models have a current threshold, while most real memristor devices are activated by a voltage threshold; (3) VTeAM models have a voltage threshold, but the resistance of the memristor changing with voltage cannot be well simulated. Hence, there is an urgent need to propose circuit models that reflect the intrinsic characteristics of memristors rather than ideal prototypes, which can more accurately reveal the voltage-current traits of real memristors. Thus, these models would be able to emulate a variety of real memristor devices with different materials and could be applied to memristor neural network circuits.

Using memristor synapse arrays to design cellular neural networks has been proven to accelerate neural network operations [129]. Moreover, memristors are used to construct other neural network circuits, such as RBF neural networks [130], Hopfield neural networks [131], echo state networks [132], spiking neural networks [133], convolution neural networks [134], etc. However, the learning algorithms in the above networks all need computer-aided calculations, and directly implementing these neural network algorithms in hardware is a bottleneck on performance. Implementing neural networks with memristor circuits fundamentally changes how these algorithms can be executed. Subsequently, many scholars have carried out extensive research in this direction, including backpropagation-based algorithms, WTA algorithms, random adjustment algorithms, and so forth. However, the existing research still lacks success in circuit-level implementations of memristor neural networks for realizing pattern recognition functions with low error in hardware.

Due to the rapid development of brain-inspired computing, memristor-based neural network processing-in-memory architectures are outperforming traditional von-Neumann computer architectures [135]. However, memristor-based in-memory computing hardware is plagued by oversized peripheral circuit area and excessively low functional unit utilization. Possible solutions to these issues are aggregating peripheral circuits to realize functional units and proposing data mapping strategies to further improve the utilization of functional units and reduce the data transmission between memristor cubes.

For potential applications of memristor-based neuromorphic networks, scholars have studied correlative pattern recognition implemented in hardware [136]. However, there have been few previous studies that determined how to combine memristor-based neuromorphic networks with memristor data storage to achieve more complex functional applications. In addition, it is also very important for the design of peripheral control circuits and the optimization of weight adjustment processes in memristor-based neuromorphic networks [137]. Adopting new algorithms to create a memristor-based neuromorphic network with fewer memristors and smaller errors, as well as the ability to complete the complex pattern recognition functions with faster speed and higher accuracy, is worthy of further investigation.

In order to accelerate the commercialization of memristors, it is critical to investigate how to reduce the failure rates, extend the service life and minimize interference. Firstly, memristor reliability is lower than that of traditional CMOS circuits, and the failure rate of a single memristor unit is significantly higher than that of a CMOS unit. Secondly, due to the integration of different types of chips, the fabrication of CMOS-memristor hybrid integrated circuits adds many additional steps and introduces additional defect risks. Moreover, each chip layer contains a large number of functional modules. If any one of the modules, or their interconnection, or the interconnection between each layer encounters manufacturing defects, the entire chip may fail, and the product failure

rate is high. Furthermore, in a single device, multiple read operations may alter the state of the device, and detecting and avoiding this phenomenon is very important to the reliability of data. Finally, in CMOS-memristor hybrid circuits, because multiple memristor units are connected to a single nanowire, it is easy to interfere with adjacent units when operating on a single memristor unit.

VIII. Future Work

From current research trends in memristor technology, the following issues are worth particular emphasis in future research:

(1) By analyzing memristor devices made of different materials, more stable and reliable memristor materials and preparation methods should be pursued. The key to solving the problem of low reliability in many applications based on memristors is to improve the reliability of a single memristor. Improving the manufacturing process of memristors or using new manufacturing materials to improve the reliability of single memristor units will play a decisive role in the applications of memristors.

(2) Whether digital or analog computation, the fluctuation of memristor device properties across different cycles or in different devices can have a large impact on calculation results. For example, the fluctuations of SET threshold voltages for different memristor devices will lead to discrepancies in operation. Especially for accurate scientific calculation, the conformance requirement of memristor devices is relatively higher. The use of verification methods or redundancy design can improve tolerance of these errors to a certain extent, but it will incur additional energy consumption and delay, weakening the inherent advantages of in-memory computing based on memristors. Therefore, the conformance of memristor devices is an important problem.

(3) The reconfigurable memristor system based on memristor neurons should be optimized and refined. Each memristor subarray or processing unit can be considered as a functional module. The memristor system design should consider a variety of network structures and provide adaptable adjustment according to the requirement. Besides, the information transmission and connection should also be flexible.

(4) Learning algorithms that are suitable for implementation by memristor circuits should be explored for multilayer neural networks, as well as designs for the corresponding online learning and adjustment circuits.

(5) By designing new learning algorithms which can make full use of memristor characteristics, so that network learning and training speeds are faster, errors are mitigated, and noise tolerance is improved. One path forward is to build memristor-based biological network circuits to simulate memory functions of the human brain. Another path forward is to establish memristor-based integrated network circuits to realize non-von Neumann computational paradigms so as to innovate a new generation of intelligent computer architectures.

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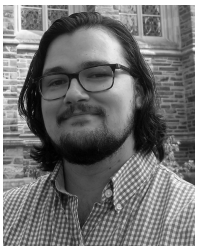

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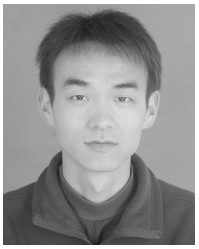

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