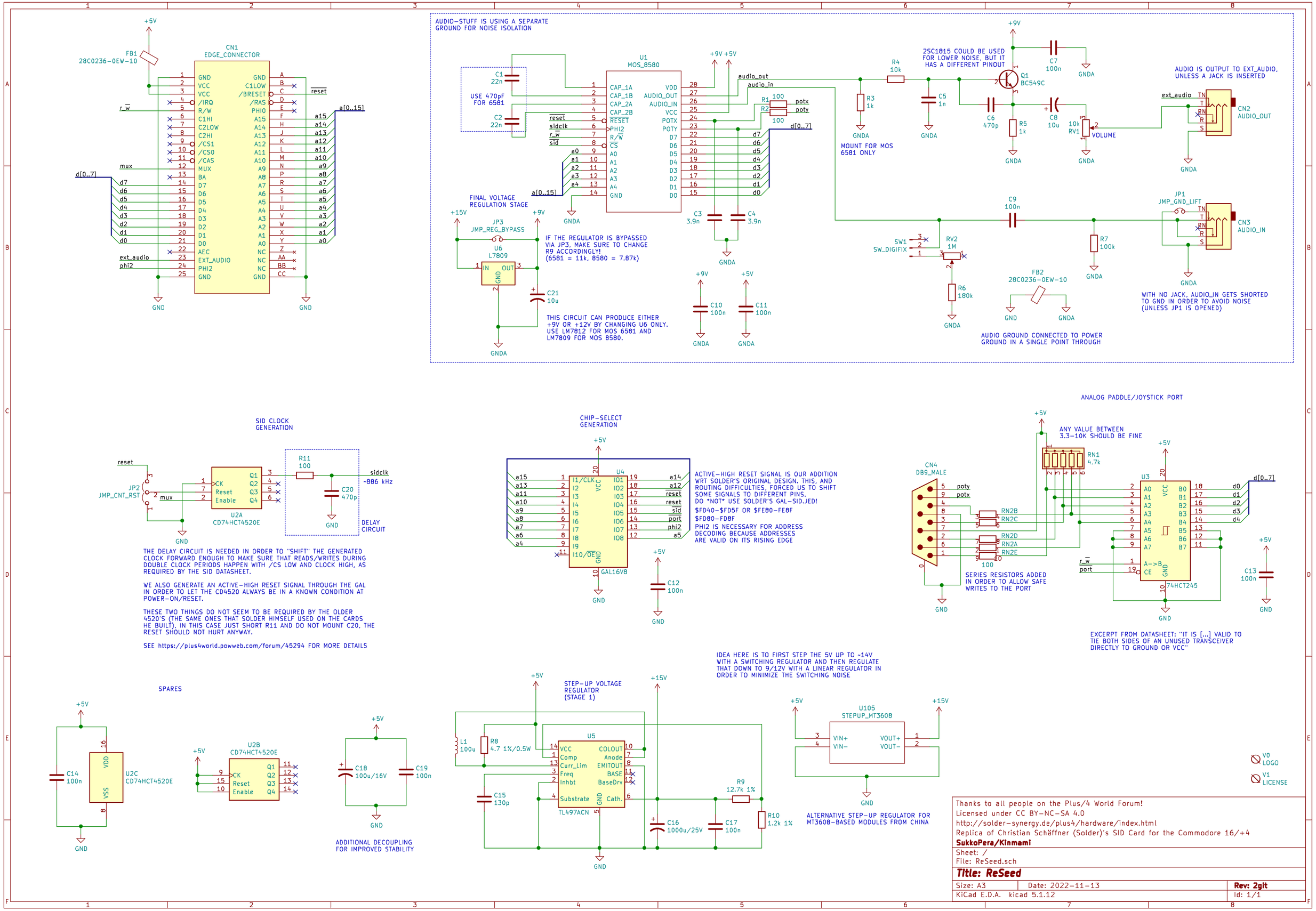
CN1
EDGE_CONNECTOR
FB1
28C0236-0EW-10
AUDIO-STUFF IS USING A SEPARATE GROUND FOR NOISE ISOLATION
U1
MOS_8580
USE 470pF FOR 6581
FINAL VOLTAGE REGULATION STAGE
JP3
JMP_REG_BYPASS
U6
L7809
IF THE REGULATOR IS BYPASSED VIA JP3, MAKE SURE TO CHANGE R9 ACCORDINGLY! (6581 = 11k, 8580 = 7.87k)
THIS CIRCUIT CAN PRODUCE EITHER +9V OR +12V BY CHANGING U6 ONLY. USE LM7812 FOR MOS 6581 AND LM7809 FOR MOS 8580.
25C1815 COULD BE USED FOR LOWER NOISE, BUT IT HAS A DIFFERENT PINOUT
Q1
BC549C
MOUNT FOR MOS 6581 ONLY
AUDIO IS OUTPUT TO EXT_AUDIO, UNLESS A JACK IS INSERTED
CN2
AUDIO_OUT
VOLUME
JP1
JMP_GND_LIFT
CN3
AUDIO_IN
WITH NO JACK, AUDIO_IN GETS SHORTED TO GND IN ORDER TO AVOID NOISE (UNLESS JP1 IS OPENED)
FB2
28C0236-0EW-10
AUDIO GROUND CONNECTED TO POWER GROUND IN A SINGLE POINT THROUGH
SID CLOCK GENERATION
JP2
JMP_CNT_RST
U2A
CD74HCT4520E
DELAY CIRCUIT
~886 kHz
THE DELAY CIRCUIT IS NEEDED IN ORDER TO "SHIFT" THE GENERATED CLOCK FORWARD ENOUGH TO MAKE SURE THAT READS/WRITES DURING DOUBLE CLOCK PERIODS HAPPEN WITH /CS LOW AND CLOCK HIGH, AS REQUIRED BY THE SID DATASHEET.
WE ALSO GENERATE AN ACTIVE-HIGH RESET SIGNAL THROUGH THE GAL IN ORDER TO LET THE CD4520 ALWAYS BE IN A KNOWN CONDITION AT POWER-ON/RESET.
THESE TWO THINGS DO NOT SEEM TO BE REQUIRED BY THE OLDER 4520'S (THE SAME ONES THAT SOLDER HIMSELF USED ON THE CARDS HE BUILT), IN THIS CASE JUST SHORT R11 AND DO NOT MOUNT C20, THE RESET SHOULD NOT HURT ANYWAY.
SEE https://plus4world.powweb.com/forum/45294 FOR MORE DETAILS
CHIP-SELECT GENERATION
U4
GAL16V8
ACTIVE-HIGH RESET SIGNAL IS OUR ADDITION WRT SOLDER'S ORIGINAL DESIGN. THIS, AND ROUTING DIFFICULTIES, FORCED US TO SHIFT SOME SIGNALS TO DIFFERENT PINS.
DO *NOT* USE SOLDER'S GAL-SID.JED!
$FD40-$FD5F OR $FE80-FE8F
$FD80-FD8F
PHI2 IS NECESSARY FOR ADDRESS DECODING BECAUSE ADDRESSES ARE VALID ON ITS RISING EDGE
ANALOG PADDLE/JOYSTICK PORT
ANY VALUE BETWEEN 3.3-10K SHOULD BE FINE
CN4
DB9_MALE
SERIES RESISTORS ADDED IN ORDER TO ALLOW SAFE WRITES TO THE PORT
U3
74HCT245
EXCERPT FROM DATASHEET: "IT IS [...] VALID TO TIE BOTH SIDES OF AN UNUSED TRANSCEIVER DIRECTLY TO GROUND OR VCC"
SPARES
U2C
CD74HCT4520E
U2B
CD74HCT4520E
ADDITIONAL DECOUPLING FOR IMPROVED STABILITY
STEP-UP VOLTAGE REGULATOR (STAGE 1)
IDEA HERE IS TO FIRST STEP THE 5V UP TO ~14V WITH A SWITCHING REGULATOR AND THEN REGULATE THAT DOWN TO 9/12V WITH A LINEAR REGULATOR IN ORDER TO MINIMIZE THE SWITCHING NOISE
U5
TL497ACN
U105
STEPUP_MT3608
ALTERNATIVE STEP-UP REGULATOR FOR MT3608-BASED MODULES FROM CHINA
V0 LOGO
V1 LICENSE
Thanks to all people on the Plus/4 World Forum!
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http://solder-synergy.de/plus4/hardware/index.html
Replica of Christian Schäffner (Solder)'s SID Card for the Commodore 16/+4
SukkoPera/Kinmami
Sheet: /
File: ReSeed.sch
Title: ReSeed
Size: A3
Date: 2022-11-13
Rev: 2git
KiCad E.D.A. kicad 5.1.12
Id: 1/1