

[Articles](#)

PIC16F628 Instruction-Set

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Table Of Contents

01 SPECIAL PURPOSE REGISTERS

02 ADDITIONAL INSTRUCTIONS

- [PIC16F628 PDF Data Sheet](#)
- [PIC16F628A.INC](#)
- [Start Here with PIC16F628](#)



SPECIAL PURPOSE REGISTERS

Although we have written Special Purpose Registers are located at 00 to 1F in the Instruction Set above (bank 0), they are also found in Bank 1. But you do not have to know their location or file number.



When writing a program, simply use the full name (from the list below) and the assembler will locate the file number during assembly.

Most assemblers have a built-in list with the names of all the registers and file numbers. For a PIC16F628, the list is: [P16F628A.inc](#) It is called a .inc file (include file).

When writing a program, place the following instructions at the top:

```
LIST P=16F628A, F=INHX8M
include "P16F628A.inc"
```

In the same folder where your program is located, place the .inc file. The assembler will find the .inc file, read the name you have given to each file, and produce a file number.

Below are the names of the files. Write them in your program in lower case thus:

```

btfss    status,z    ;test the zero bit and skip if set
    movlw    46h        ;put 46h into w
    movwf    porta      ;output 46h via port A

    bsf      portb,2    ;output a high on the third line of port B
    bsf      trisb,1    ;Make the second line of port B output
    bcf      status,rp0 ;Get back to Bank 0 where PortA and PortB is located
    movlw    88h        ; "1000 1000"
    movlw    portb

;=====
;
;   Register Definitions
;
;=====

W          EQU    H'0000'
F          EQU    H'0001'

;----- Register Files-----

INDF       EQU    H'0000'
TMR0       EQU    H'0001'
PCL        EQU    H'0002'
```

```

STATUS      EQU  H'0003'
FSR         EQU  H'0004'
PORTA       EQU  H'0005'
PORTB       EQU  H'0006'
PCLATH      EQU  H'000A'
INTCON      EQU  H'000B'
PIR1        EQU  H'000C'
TMR1L       EQU  H'000E'
TMR1H       EQU  H'000F'
T1CON       EQU  H'0010'
TMR2        EQU  H'0011'
T2CON       EQU  H'0012'
CCPR1L      EQU  H'0015'
CCPR1H      EQU  H'0016'
CCP1CON     EQU  H'0017'
RCSTA       EQU  H'0018'
TXREG       EQU  H'0019'
RCREG       EQU  H'001A'
CMCON       EQU  H'001F'

```

```

OPTION_REG  EQU  H'0081'
TRISA       EQU  H'0085'
TRISB       EQU  H'0086'
PIE1        EQU  H'008C'
PCON        EQU  H'008E'
PR2         EQU  H'0092'
TXSTA       EQU  H'0098'
SPBRG       EQU  H'0099'
EEDATA      EQU  H'009A'
EEADR       EQU  H'009B'
EECON1      EQU  H'009C'
EECON2      EQU  H'009D'
VRCON       EQU  H'009F'

```

```

;----- STATUS Bits -----

```

```

IRP         EQU  H'0007'
RP1         EQU  H'0006'
RP0         EQU  H'0005'
NOT_TO      EQU  H'0004'
NOT_PD      EQU  H'0003'
Z           EQU  H'0002'
DC          EQU  H'0001'
C           EQU  H'0000'

```

```

;----- INTCON Bits -----

```

```

GIE                EQU  H'0007'
PEIE               EQU  H'0006'
T0IE              EQU  H'0005'
INTE              EQU  H'0004'
RBIE              EQU  H'0003'
T0IF              EQU  H'0002'
INTF              EQU  H'0001'
RBIF              EQU  H'0000'

```

```

;----- PIR1 Bits -----

```

```

EEIF              EQU  H'0007'
CMIF              EQU  H'0006'
RCIF              EQU  H'0005'
TXIF              EQU  H'0004'
CCP1IF           EQU  H'0002'
TMR2IF           EQU  H'0001'
TMR1IF           EQU  H'0000'

```

```

;----- T1CON Bits -----

```

```

T1CKPS1           EQU  H'0005'
T1CKPS0           EQU  H'0004'
T1OSCEN           EQU  H'0003'
NOT_T1SYNC        EQU  H'0002'
TMR1CS            EQU  H'0001'
TMR1ON            EQU  H'0000'

```

```

;----- T2CON Bits -----

```

```

TOUTPS3           EQU  H'0006'
TOUTPS2           EQU  H'0005'
TOUTPS1           EQU  H'0004'
TOUTPS0           EQU  H'0003'
TMR2ON            EQU  H'0002'
T2CKPS1           EQU  H'0001'
T2CKPS0           EQU  H'0000'

```

```

;----- CCP1CON Bits -----

```

```

CCP1X             EQU  H'0005'
CCP1Y             EQU  H'0004'
CCP1M3            EQU  H'0003'
CCP1M2            EQU  H'0002'
CCP1M1            EQU  H'0001'
CCP1M0            EQU  H'0000'

```

```

;----- RCSTA Bits -----

```

```

SPEN              EQU  H'0007'
RX9               EQU  H'0006'

```

```

SREN          EQU  H'0005'
CREN          EQU  H'0004'
ADEN          EQU  H'0003'
FERR          EQU  H'0002'
OERR          EQU  H'0001'
RX9D          EQU  H'0000'

```

```

;----- CMCON Bits -----

```

```

C2OUT         EQU  H'0007'
C1OUT         EQU  H'0006'
C2INV         EQU  H'0005'
C1INV         EQU  H'0004'
CIS           EQU  H'0003'
CM2           EQU  H'0002'
CM1           EQU  H'0001'
CM0           EQU  H'0000'

```

```

;----- OPTION Bits -----

```

```

NOT_RBPU      EQU  H'0007'
INTEDG        EQU  H'0006'
T0CS          EQU  H'0005'
T0SE          EQU  H'0004'
PSA           EQU  H'0003'
PS2           EQU  H'0002'
PS1           EQU  H'0001'
PS0           EQU  H'0000'

```

```

;----- PIE1 Bits -----

```

```

EEIE          EQU  H'0007'
CMIE          EQU  H'0006'
RCIE          EQU  H'0005'
TXIE          EQU  H'0004'
CCP1IE        EQU  H'0002'
TMR2IE        EQU  H'0001'
TMR1IE        EQU  H'0000'

```

```

;----- PCON Bits -----

```

```

OSCF          EQU  H'0003'
NOT_POR       EQU  H'0001'
NOT_BO        EQU  H'0000'
NOT_BOR       EQU  H'0000'
NOT_BOD       EQU  H'0000' ;Backwards compatability to 16F62X

```

```

;----- TXSTA Bits -----
CSRC                EQU  H'0007'
TX9                 EQU  H'0006'
TXEN                EQU  H'0005'
SYNC                EQU  H'0004'
BRGH                EQU  H'0002'
TRMT                EQU  H'0001'
TX9D                EQU  H'0000'

;----- EECON1 Bits -----
WRERR               EQU  H'0003'
WREN                EQU  H'0002'
WR                  EQU  H'0001'
RD                  EQU  H'0000'

;----- VRCON Bits -----

VREN                EQU  H'0007'
VROE                EQU  H'0006'
VRR                 EQU  H'0005'
VR3                 EQU  H'0003'
VR2                 EQU  H'0002'
VR1                 EQU  H'0001'
VR0                 EQU  H'0000'

;=====
;
;  RAM Definition
;
;=====

__MAXRAM H'01FF'
__BADRAM H'07'-H'09', H'0D', H'13'-H'14', H'1B'-H'1E'
__BADRAM H'87'-H'89', H'8D', H'8F'-H'91', H'93'-H'97', H'9E'
__BADRAM H'105', H'107'-H'109', H'10C'-H'11F', H'150'-H'16F'
__BADRAM H'185', H'187'-H'189', H'18C'-H'1EF'

;=====
;
;  Configuration Bits
;
;=====

_BODEN_ON           EQU  H'3FFF'
_BODEN_OFF          EQU  H'3FBF'
_BOREN_ON           EQU  H'3FFF'
_BOREN_OFF          EQU  H'3FBF'

```

```

_CP_ON           EQU  H'1FFF'
_CP_OFF          EQU  H'3FFF'
_DATA_CP_ON      EQU  H'3EFF'
_DATA_CP_OFF     EQU  H'3FFF'
_PWRTE_OFF       EQU  H'3FFF'
_PWRTE_ON        EQU  H'3FF7'
_WDT_ON          EQU  H'3FFF'
_WDT_OFF         EQU  H'3FFB'
_LVP_ON          EQU  H'3FFF'
_LVP_OFF         EQU  H'3F7F'
_MCLRE_ON        EQU  H'3FFF'
_MCLRE_OFF       EQU  H'3FDF'
_RC_OSC_CLKOUT   EQU  H'3FFF'
_RC_OSC_NOCLKOUT EQU  H'3FFE'
_ER_OSC_CLKOUT   EQU  H'3FFF'
_ER_OSC_NOCLKOUT EQU  H'3FFE'
_INTOSC_OSC_CLKOUT EQU  H'3FFD'
_INTOSC_OSC_NOCLKOUT EQU  H'3FFC'
_INTRC_OSC_CLKOUT EQU  H'3FFD'
_INTRC_OSC_NOCLKOUT EQU  H'3FFC'
_EXTCLK_OSC      EQU  H'3FEF'
_HS_OSC          EQU  H'3FEE'
_XT_OSC          EQU  H'3FED'
_LP_OSC          EQU  H'3FEC'

```

ADDITIONAL INSTRUCTIONS

ADDWF PCL,1 ADDWF 02,1 Alter the program counter to create a jump

CLRF INDF,1 CLRF 00,1 Clear INDIRECT file

INCF FSR,1 INCF 04,1 Increment the File Select Register

INTCON address is either 0Bh or 8Bh - it is mapped at both locations.

BCF INTCON,RBIF Clear RB<7:4> Port-change Interrupt flag

BSF INTCON,RBIF Set RB<7:4> Port-change Interrupt flag

BCF INTCON,RBIE Disables the Port-change Interrupt

BSF INTCON,RBIE Enables the Port-change Interrupt

BCF INTCON,INTE Disables the RB0/INT Interrupt

BSF INTCON,INTE Enables the RB0/INT Interrupt

BCF INTCON,T0IE Disables the TMR0 Interrupt

BSF INTCON,T0IE Enables the TMR0 Interrupt

BCF INTCON,EEIE Disables the EE write complete Interrupt

BSF INTCON,EEIE Enables the EE write complete Interrupt

BCF INTCON,GIE Disables all Interrupts

BSF INTCON,GIE Enables all un-masked Interrupts

OPTION address is 81h - use the word OPTION

OPTION,0 OPTION,1 OPTION,2 **Prescaler Rate Select Bits**

Bit Value	TMR0 Rate	WDT Rate
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1:64	1:32
110	1:128	1:64
111	1:256	1:128

e:g:

BSF OPTION,0 BCF OPTION,1 BSF OPTION,2 TMR0 Rate = 1:64 WDT Rate = 1:32

BSF OPTION,0 BSF OPTION,1 BSF OPTION,2 TMR0 Rate = 1:256 WDT Rate = 1:128

BCF OPTION,PSA BCF OPTION,3 Prescaler assigned to TMR0

BSF OPTION,PSA BSF OPTION,3 Prescaler assigned to the WDT

BCF OPTION,T0SE BCF OPTION,4 Increment on low-to-high on RA4/T0CKI pin

BSF OPTION,T0SE BSF OPTION,4 Increment on high-to-low on RA4/T0CKI pin

BCF OPTION,T0CS BCF OPTION,5 Internal Instruction cycle clock (CLKOUT)

BSF OPTION,T0CS BSF OPTION,5 Clock source select. Transition on RA4/T0CKI Pin

BCF OPTION,INTEDG BCF OPTION,6 Interrupt on falling edge of RB0/INT Pin

BSF OPTION,INTEDG BSF OPTION,6 Interrupt on rising edge of RB0/INT Pin

BCF OPTION,RBPU BCF OPTION,7 PORT B Pull-ups are enabled

BSF OPTION,RBPU BSF OPTION,7 PORT B Pull-ups are disabled

STATUS address is either 03h or 83h - it is mapped at both locations.

BTFSS STATUS,C or BTFSC 03,0 Test the carry bit. C=1=set = carry occurred

BTFSS STATUS,C or BTFSC 03,0 Test the carry bit. C=0=reset = carry did not occur

BTFSS STATUS,DC BTFSS 03,1 Test the digit carry bit. C=1=set = carry-out from the

4th lower order bit of the result occurred.

BTFSS STATUS,DC BTFSS 03,1 Test the digit carry bit. C=0=reset = carry-out did not

occur from the 4th lower order bit of the result.

BTFSS STATUS,Z or BTFSC 03,2 Test the zero bit. Z=1=set = result of arithmetic or logic operation is zero.

BTFSS STATUS,Z or BTFSC 03,2 Test the zero bit. Z=0=reset = result of arithmetic

or logic operation is not zero.

BSF STATUS,RP0 BSF 03,5 Go to Bank1 for TRISA or TRISB register

BCF STATUS,RP0 BCF 03,5 Go to Bank0 for programming

CLRF INDF,1 CLRF 00,1 Clear INDIRECT file

RETFIE Return from Interrupt Sets INTCON,GIE

File name:	File No:	Comments:
EECON1	equ 088h	;EEPROM Control Register 1
EECON2	equ 089h	;EEPROM Control Register 2
EEADR	equ 9	;EEPROM address Register

File name:	File No:	Comments:
EEDATA	equ 8	;EEPROM Data Register
FSR	equ 4	;File Select Register
INDF	equ 0	;INDIRECT file
INTCON	equ 0Bh	;Interrupt and Timer bits
OPTION	equ 081h	;Option Register
PCL	equ 2	;Program Counter Low-bits
PORTA	equ 5	;Port A
PORTB	equ 6	;Port B
STATUS	equ 3	;Status Register
TRISA	equ 085h	;Make Port A bits input or output
TRISB	equ 086h	;Make Port B bits input or output

Bit name:	Bit No:	Comments and name of file holding the bit:
Carry	equ 0	;Carry bit in Status file C=0=no carry-out
DC	equ 1	;Digit Carry in Status DC=0=no carry out from 4th low-order digit
EEIF	equ 4	;In EECON1 EEIF=1=The write operation completed
f	equ 1	;Place the result of the operation in the file
GIE	equ 7	;Global Interrupt Enable bit. In INTCON 0=Disables all interrupts
RD	equ 0	;In EECON1 Read Control bit
RP0	equ 5	;In Status. Register Bank select RP0=clear=bank0 RP0=set=bank1
Self	equ 1	;Store the result in the file
TOIE	equ 5	;In INTCON Timer0 Overflow Interrupt Enable bit
TOIF	equ 2	;In INTCON Timer0 Overflow Interrupt Flag bit
W	equ 0	;Place the result in W
WR	equ 1	;In EECON1 Write Control bit
WREN	equ 2	;In EECON1 EEPROM Write Enable bit

Bit name:	Bit No:	Comments and name of file holding the bit:
Z	equ 2	;Z in Status file. Zero flag=set=1 when result of operation is zero!!

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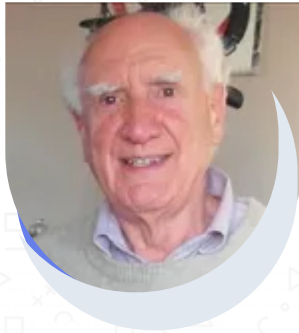
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