

Fig. 5.7. Response of a simulated tuned circuit

Apply a 2V r.m.s. 50Hz signal to OA1/Input 2, and monitor by means of a reliable 10V a.c. meter of not less than 1 kilohm/volt sensitivity. The input function should preferably come from a low impedance source to avoid serious loading errors when the voltmeter is removed. Next, connect the a.c. voltmeter to the output of OA1 and adjust CP1 so that OA1 input and output voltages are exactly equal. CP1 could alternatively be set by the reference voltage and d.c. voltmeter method mentioned earlier, for a coefficient of 0.1. If the CP2 setting is altered it will be discovered that the simulated circuit goes off resonance, and can be tuned by CP2 between approximately 5Hz and 50Hz.

UNIT "A" will now be ready for analysis of the Fig. 5.6a tuned circuit, and will also cover a useful range of other values for L , C , and R in real time.

When handling sinusoidal or step functions, an amplifier will still have a maximum output voltage swing of $\pm 10V$, but this will be the peak voltage value. To check for overloading with an a.c. meter, ensure that amplifier output voltages do not exceed 7.07V r.m.s. for a sine wave function, and 5V mean for an equal mark-space square wave.

RESCALING PROBLEM EXAMPLE 3.

To rescale the problem for larger or smaller values of L and C , beyond the coverage of CP2, and by abandoning real time operation, note that a tenfold increase in tuned circuit frequency corresponds to a hundredfold increase in $1/LC$. For most applications, where the series resistance R will lie between zero and just beyond critical damping ($R > 2\sqrt{[L/C]}$), the scaling of R/L can stay as it is for all reasonable values of L and C , but should anyway only be changed by adjustment of the gain factor at OA1/Input 1. Similarly, the $f(t)/L$ gain of 100 at OA1/Input 2 can remain fixed.

It is not necessary to use inconveniently large or small input functions when rescaling for new voltages and currents. 2V r.m.s. could equally well represent an input function of, say, 0.2V r.m.s., and from Ohm's Law the current I will automatically become 2mA, instead of the former 20mA, even though it is still represented by 2 computer volts.

If it is desired to extend the computer operating time, by adjustment of integrator and inverting amplifier closed-loop gains, refer to Table 5.2, while remembering that integrator closed-loop gains are calculated on the basis of $1/R_{in}C_f$ where R is in ohms and C is in farads.

For reasons of reduced accuracy, it is not advisable to use computer operating frequencies above 1kHz or below 0.05Hz in connection with Problem Example 3. It should be mentioned that although frequencies in the region of 0.05Hz are too low for display on an a.c. coupled oscilloscope, the behaviour of a system can be demonstrated in slow motion by the oscillating movement of a d.c. voltmeter pointer (centre-zero).

Some typical oscilloscopes are given in Fig. 5.7 to show the response of a simulated tuned circuit. If the computer oscilloscope is provided with a good graticule, and has a linear response, amplitude and time measurements which are accurate to within approximately 5 per cent may be obtained straight from the trace.

The behaviour of a real tuned circuit can be evaluated by comparison with a simulated circuit. A tracing is made of the real circuit oscilloscope display, and is then superimposed on the readout given by the simulated circuit. The computer is adjusted so that time scales are related by a known factor, and tracing and readout display are identical, then quantitative measurements are taken from the computer voltages and dial settings.

Next month: The construction and operation of UNIT "B"



ANALOGUE COMPUTER

PEAC

**By
D. BOLLEN**

THE PEAC basic equipment has now been dealt with and this month we commence a detailed description of the chief ancillary unit. Subsequent articles will cover the remaining two ancillary units.

Perhaps it should be repeated at this stage that the three ancillary units are purely optional add-on items. The additional facilities they each provide, are indicated in the PEAC Specification (January 1968, page 38).

PEAC UNIT "B"

UNIT "B" reinforces the facilities of UNIT "A", but does not introduce new computing circuit elements. A master potentiometer and a suitably scaled readout meter improve the accuracy and ease of handling of UNIT "A", while the integrator mode switching circuit opens up further possibilities in the solution of Calculus problems.

UNIT "B" FRONT PANEL

It may not be necessary to use hardboard for the front panel if a thick grade of plastic laminate is used, since the wooden surround in the box front gives plenty of support.

Prepare a $17\frac{3}{4}$ in \times $8\frac{3}{4}$ in white laminate panel and establish hole centres with a sharp spike, from the drawings Fig. 6.1 and Fig. 6.2. Next, drill only the holes for all sockets, S7, S8, the meter mounting studs, and cut out a hole for the meter body with a fretsaw.

Beginning with the master potentiometer dial, draw a 300 degree arc of radius $2\frac{1}{2}$ in with a pencil compass (refer to Fig. 6.2). Divide the arc into 3-degree divisions with protractor and pencil. The accuracy of the master potentiometer will benefit from careful preparation of the dial. Draw in the dial arc and divisions with Indian ink.

Rub-on transfers are suitable for the dials of VR18 and VR19, and will save time, but make sure that the transfer gives main divisions spaced at 30-degree intervals, for a 1-10 calibration.

When dials are complete, drill holes to take the

spindles of VR18-VR20, S9 and S10. Draw in all ink lines, add transfer numerals, and varnish.

BOX CONSTRUCTION

Commence building the UNIT "B" box by cutting out two side panels from hardboard; they are shown in Fig 6.3. Fix $\frac{1}{2}$ in square softwood lengths A, B, C, and D to the inside of the side panels. Join the side panels together by means of horizontal lengths E, and F, using countersunk woodscrews and glue. Square up with the assembly placed on a flat surface.

Cover the box framework with hardboard top, bottom, and front strip panels, and, when firm, reduce overlapping edges with a rasp and sandpaper. Finish off the box with a layer of white plastic laminate, and paint exposed hardboard edges to match the UNIT "B" box.

MASTER POTENTIOMETER AND NULL METER

A d.c. voltmeter connected to the slider of a computing potentiometer will impose a small load, and when the voltmeter is removed the measured coefficient will increase slightly, to the extent of about $1\frac{1}{2}$ per cent in the case of a 10V 20,000 ohms/volt meter, and a 10 kilohm potentiometer set with its slider near mid-track. One way of avoiding the error is to leave the voltmeter connected to the potentiometer after a coefficient reading has been taken, but this is seldom convenient.

Ideally, the instrument used to measure coefficients or computer voltages should impose no load at all, and this condition can be satisfied fairly easily by employing an accurately calibrated master potentiometer.

In Fig 6.4, a permanent load is placed on the coefficient potentiometer CP by the computing resistor R_{in} , thus causing a significant dial setting error. To find the true coefficient of CP, both potentiometers are supplied with a reference voltage of + 10V, so that potentiometer coefficients of 0-1 will be multiplied by 10 to conform to a 0-10 dial calibration. When

COMPONENTS . . .

UNIT "B" FRONT PANEL

NOTE: All front panel controls are numbered consecutively, following on from UNIT "A", but internal sub-assemblies have individual component numbering.

Potentiometers

VR18 100kΩ carbon linear
 VR19 100kΩ carbon linear
 VR20 25kΩ wirewound, 3in, 25W
 instrument potentiometer. (G. W. Smith & Co. (Radio) Ltd., 3 Lisle Street, London, W.C.2)

Switches

S7 Miniature push button, push to make, one pole
 S8 Toggle, single pole changeover
 S9 4 pole, 3 way rotary
 S10 2 pole, 6 way rotary

Sockets

5 red, 3 black, 5 blue, 4 yellow, 4 white, and 2 green

Knobs

One Bulgin K403, 2½in knob with 3in skirt.
 Three Radiospares type PK 1½in knobs with pointers

Meter

MI "Sew" MR85P, 100–0–100μA, internal resistance 1,000Ω

Miscellaneous

Plastic laminate (thick) for front panel, 1 off, 17½in × 8½in. Rub-on dial transfers and letters, black (Radiospares)

UNIT "B" MASTER POTENTIOMETER

Resistors

| | | |
|---------|--------|---------|
| R1 200Ω | R3 47Ω | R5 820Ω |
| R2 820Ω | R4 47Ω | R6 200Ω |

All 5%, ½W carbon film or metal oxide

Pre-set potentiometers

VR1—VR4 100Ω wirewound (4 off)
 panel mounting type

Miscellaneous

16 s.w.g. aluminium sheet 6in × 4in. Tag strip with three tags.

UNIT "B" READOUT METER

Resistors

| | | |
|-------------|--------------|----------------|
| R1 82kΩ 10% | R3 7.5kΩ 5% | All ½W, carbon |
| R2 22kΩ 10% | R4 1.2kΩ 10% | composition |

Pre-set potentiometers

| | |
|-----------|--------------------------|
| VR1 22kΩ | All miniature horizontal |
| VR2 10kΩ | mounting skeleton con- |
| VR3 2.2kΩ | struction |
| VR4 1kΩ | |

Meter protection diodes

D1, D2 OC71 or similar "inverted" germanium transistor (2 off)

Miscellaneous

S.R.B.P. panel 2½in × 2in.

UNIT "B" INTEGRATOR MODE SWITCH

Resistors

| | | |
|---------|----------|----------|
| R1 10kΩ | R4 4.7kΩ | R7 27kΩ |
| R2 10kΩ | R5 27kΩ | R8 4.7kΩ |
| R3 1kΩ | R6 1kΩ | R9 10kΩ |

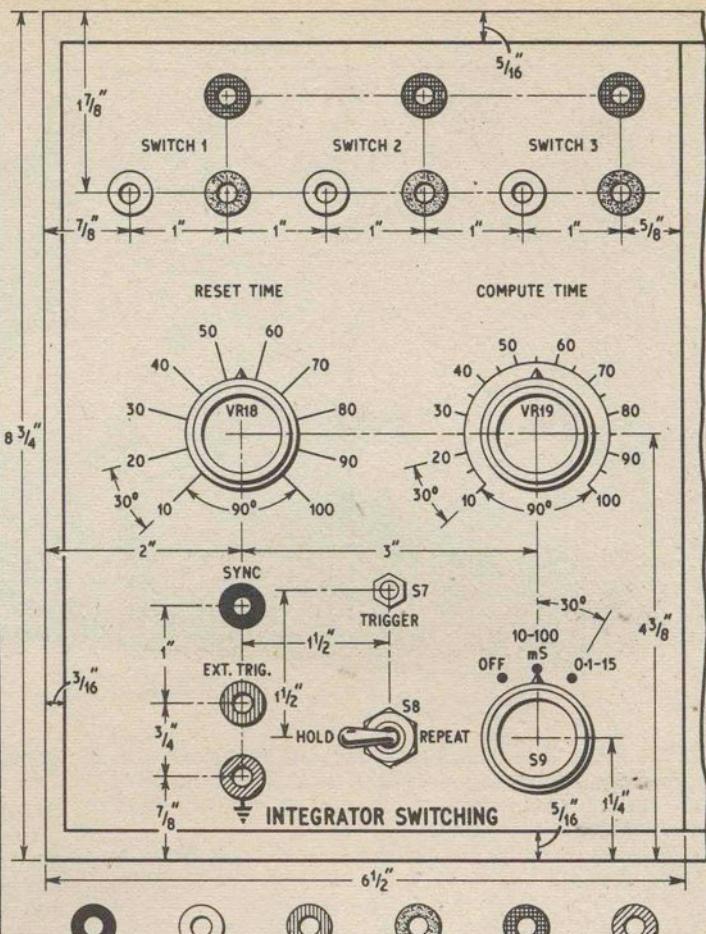


Fig. 6.1. UNIT "B" front panel, integrator switching section

R10 10kΩ R12 3.3kΩ R14 1kΩ
 R11 1kΩ R13 10kΩ R15 560kΩ
 All 10%, ½W carbon composition

Pre-set Potentiometers

VR1 10kΩ VR2 5kΩ Both vertical mounting

Capacitors

| | |
|---|--------------------------------|
| C1 1,000μF elec. 15V | C6 1μF polyester 250V d.c. |
| C2 1μF polyester 250V d.c. | C7 1.4μF polyester 250V d.c. |
| C3 1.4μF polyester 250V d.c. | C8 14μF elec. 25V working. |
| C4 14μF elec. 25V | C5 0.1μF polyester 250V d.c. |
| (The values of C3, C4, C7, and C8 are approximate—see text) | C9 0.068μF polyester 250V d.c. |

Transistors

TR1–TR6 ACY28 or AC126.

Diodes

D1, D2 OA95 (2 off)
 D3–D14 IB30 (Radiospares) (12 off)

Reed Coils

RLA, RLB Miniature triple 12V Osmor type MT12V (2 off)

Reed Switches

RLA1—RLA3 Hamlin MRG2, 20-40AT (R.T.S. Ltd.,
 RLB1—RLB3 P.O. Box 11, Gloucester St. Cambridge) (6 off.)

Miscellaneous

S.R.B.P. panels: 1 off 6½in × 2½in; 1 off 3in × 2in.
 Small turret tags.

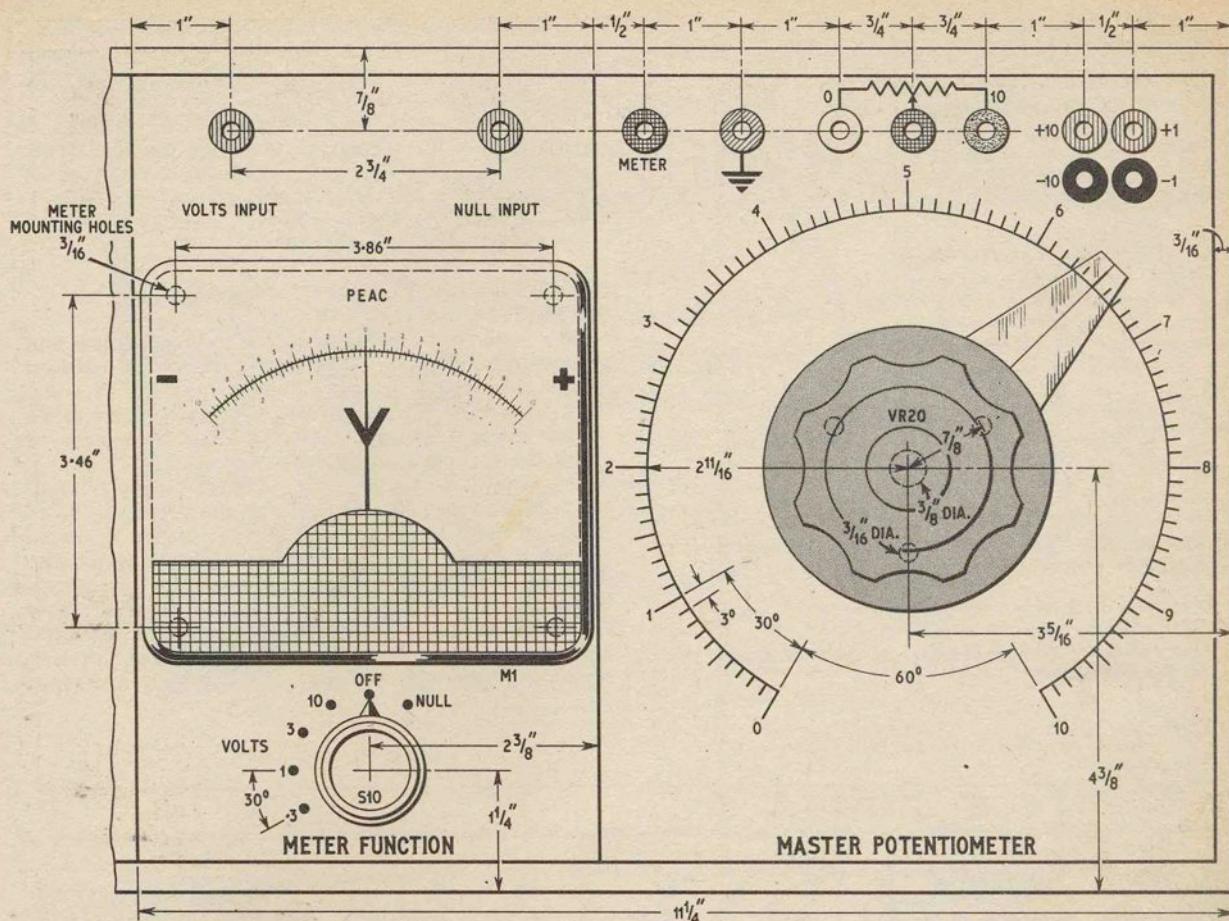


Fig. 6.2. UNIT "B" front panel, readout meter and master potentiometer

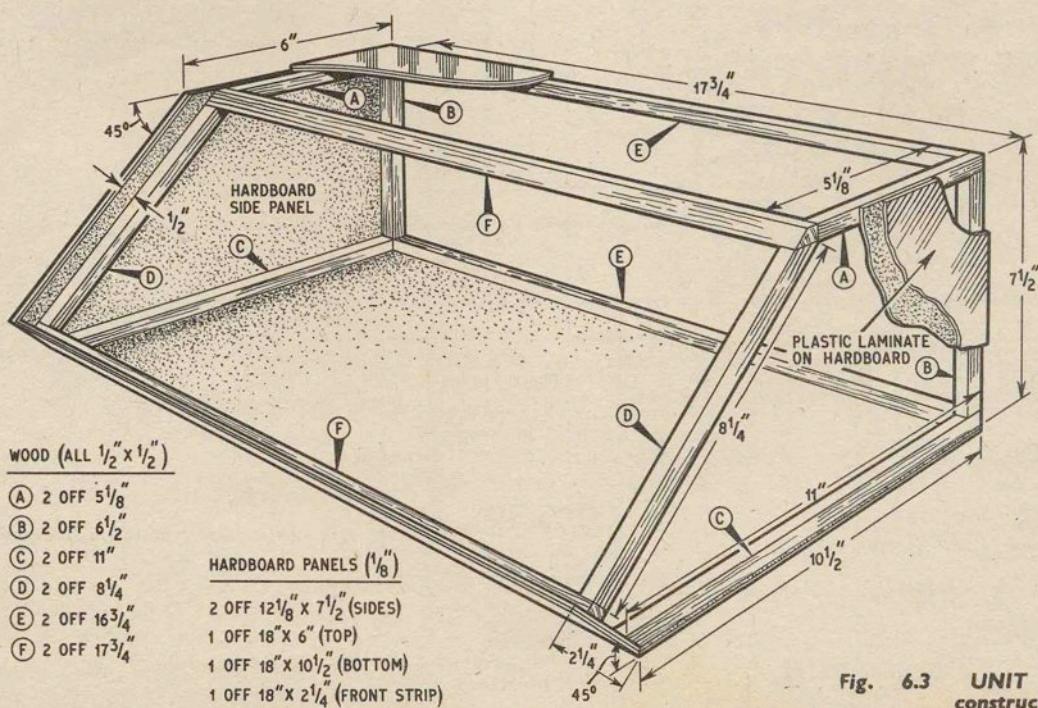


Fig. 6.3. UNIT "B" box constructional details

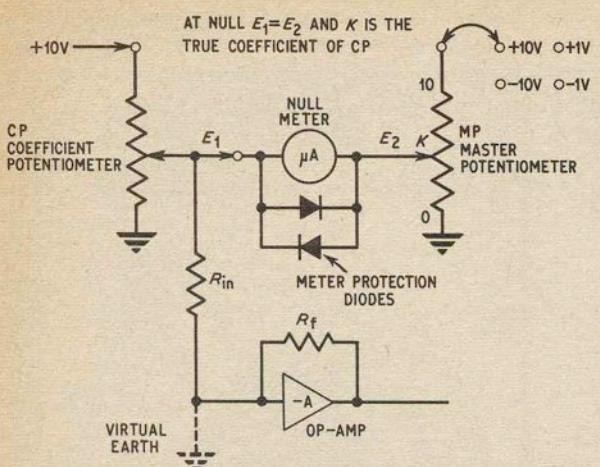


Fig. 6.4. Master potentiometer circuit for measuring coefficients

Fig. 6.5 (below). Circuit diagram of readout meter and master potentiometer

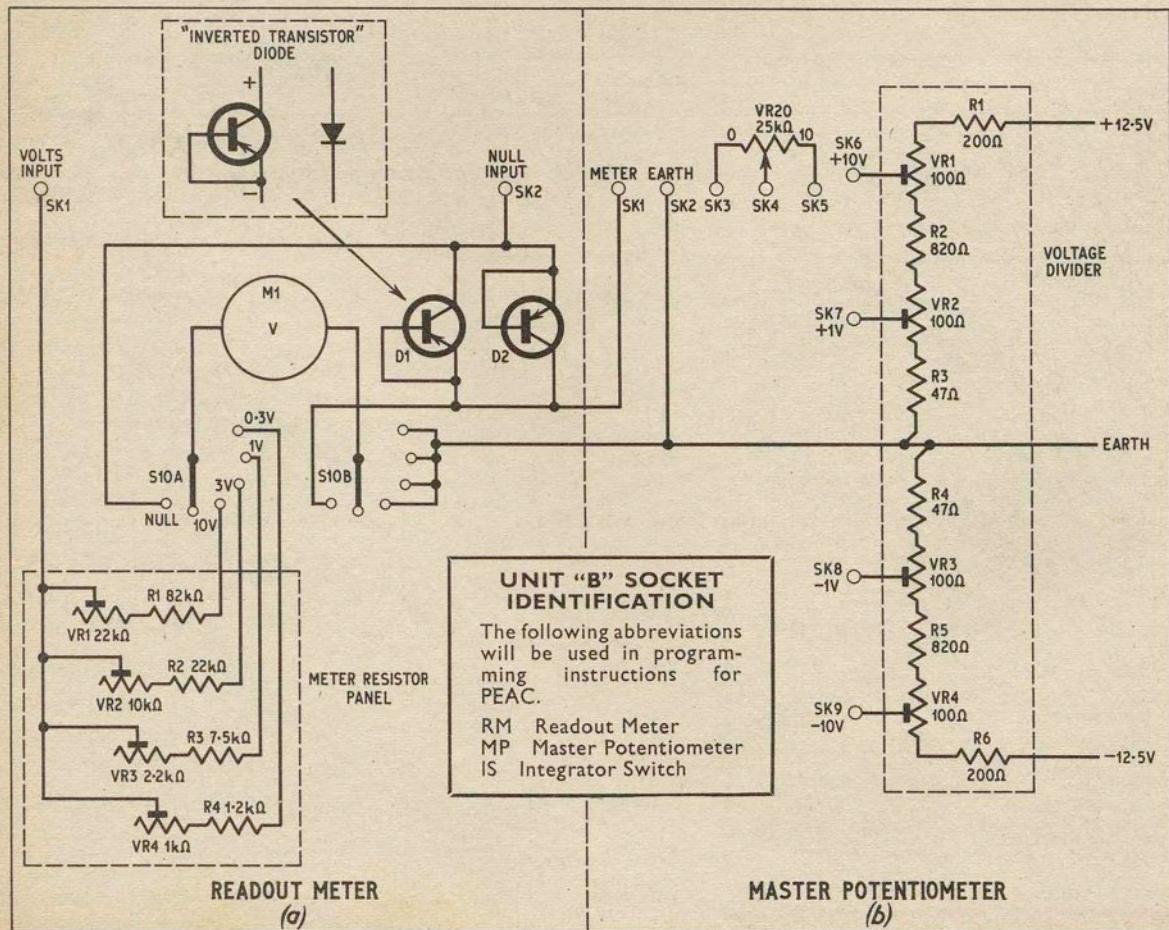
the voltage at the slider of CP is identical to the slider voltage of MP, no current flows through the null meter, and the true coefficient of CP can be read straight off the dial of MP.

Since no current flows at null point, no load is imposed, and the input resistance of the measuring circuit is virtually infinite. Meter protection diodes are included to preserve good meter sensitivity without allowing damaging currents to flow through the meter when the circuit is off balance.

READOUT METER AND MASTER POTENTIOMETER CIRCUITS

One meter movement serves for null indication and voltage measurement. Considering first the readout meter circuit Fig. 6.5a, miniature pre-set resistors VR1-VR4 will permit calibration of each meter range to an external voltage standard, and also help to eliminate discrepancies between ranges.

The way in which meter protection diodes D1 and D2 are wired may be unfamiliar to the reader, so some explanation is called for. If a transistor is operated "inverted", that is with collector-emitter polarities reversed, it will exhibit a very low "on" resistance when the base is near emitter potential. With base connected straight to emitter, the transistor therefore becomes a diode with lower than normal forward resistance, and yet will still offer a high resistance



reverse characteristic. The arrangement eliminates the need for a meter series resistor while still giving adequate protection.

In Fig. 6.5b, VR20 is a 3in instrument potentiometer of good linearity. The voltage divider network, composed of R1-R6 and VR1-VR4, taps off four standard voltages from the computer power supply, so that the master potentiometer will measure inputs of 0 to + 1V, 0 to - 1V, 0 to + 10V, and 0 to - 10V on its 0-10 scale. The accuracy of the master potentiometer, bearing in mind the 14in scale length, approaches that of a laboratory voltmeter.

FRONT PANEL AND MASTER POTENTIOMETER ASSEMBLY

Mount all sockets, potentiometers VR18-VR20, switches S7-S10, and meter, on the UNIT "B" front panel. Make up an aluminium bracket from the measurements given in Fig. 6.6, and glue it to the front panel, along with the small tag strip, in the position shown in Fig. 6.7. A hot soldering iron applied to the aluminium bracket will solidify the epoxy resin glue in a matter of minutes, sufficient to hold the bracket in place until the joint sets hard.

Rest the front panel inside-out on the UNIT "B" box front, to protect panel markings during assembly. Mount pre-set voltage divider potentiometers VR1-VR4 to the aluminium bracket, and then proceed with the

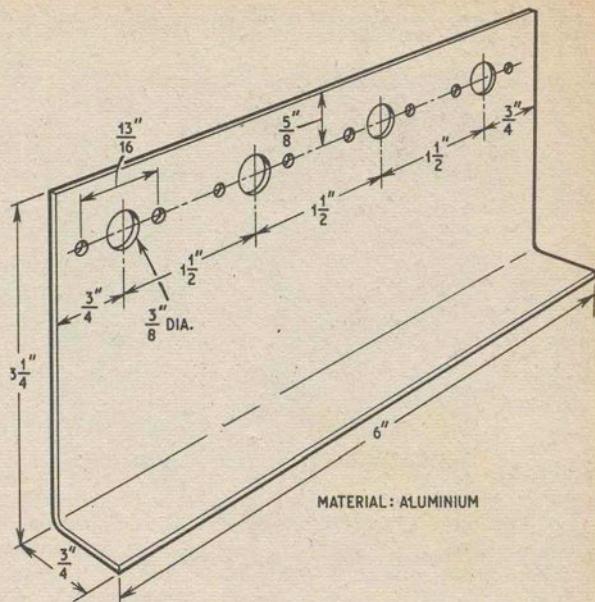


Fig. 6.6. Mounting bracket for pre-set potentiometers

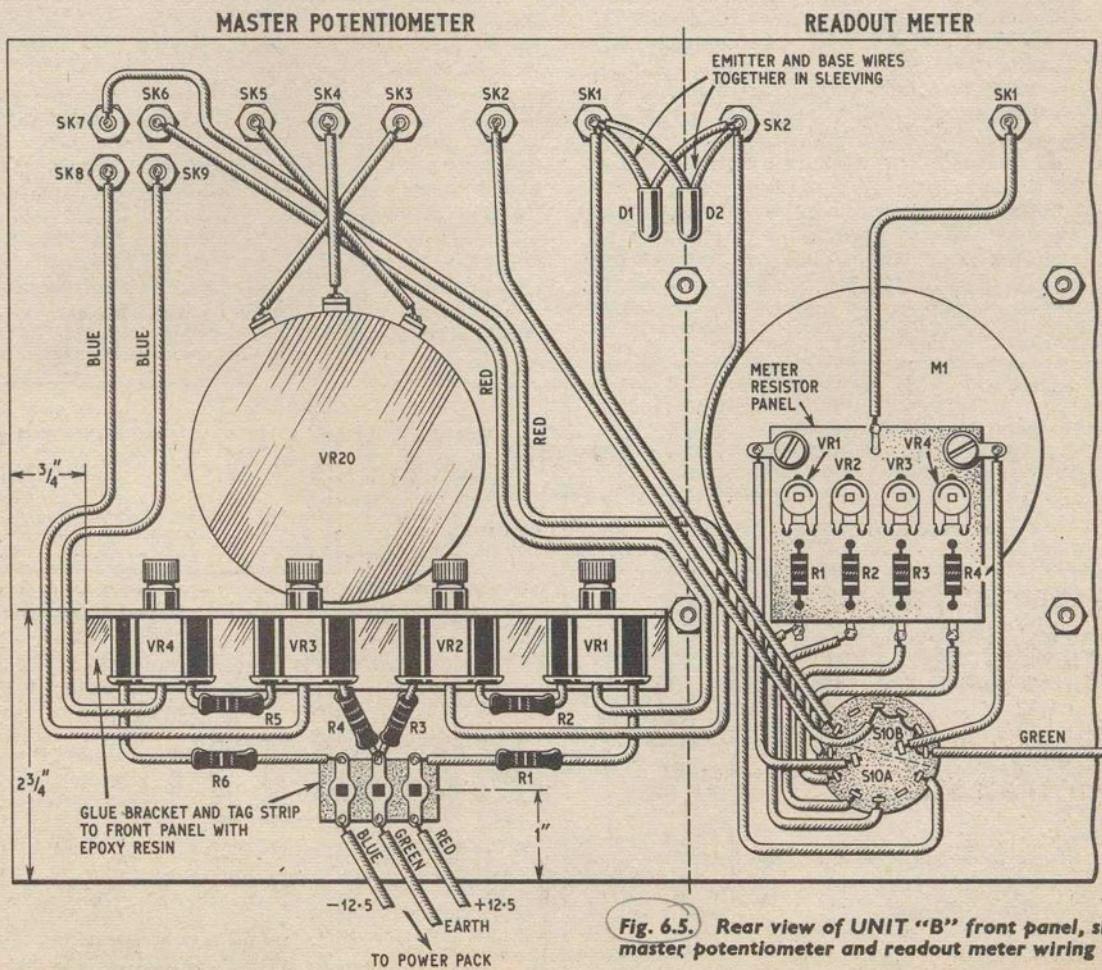


Fig. 6.5. Rear view of UNIT "B" front panel, showing master potentiometer and readout meter wiring

Fig 6.7

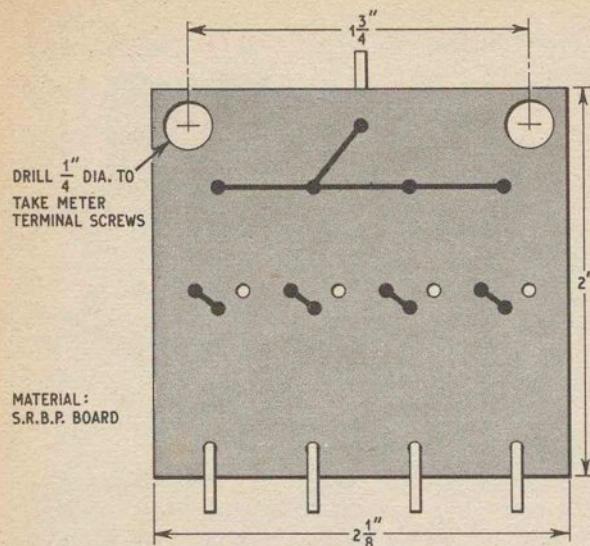


Fig. 6.8. Meter resistor panel, underside view

wiring of master potentiometer components, using 20 s.w.g. tinned copper wire and sleeving.

READOUT METER ASSEMBLY

Make up the meter resistor panel shown in Figs 6.7 and 6.8, and attach to the meter terminals. Solder D1 and D2 to MP/SK1 and RM/SK2, then complete S10 and resistor panel wiring.

As centre-zero voltmeters with 10-0-10 and 3-0-3 scale calibrations are not readily available, a scale will have to be made. Perhaps the most satisfactory way of fabricating a new and really accurate meter scale is to draw it two to four times full size, photograph it, and then have the resulting negative enlarged back to the original size on glossy photographic paper. The enlarging can be done commercially if the oversize drawing carries a thick black line to represent a length of 1in on the finished scale, just outside the scale perimeter.

When taking the photograph, ensure that the camera lens is in line with the centre of the scale card, and that the film plane is parallel to the surface of the oversize drawing, to prevent optical distortion.

Another tip, use white Formica for the drawing, as then mistakes in ink can be erased without leaving unsightly grey areas.

To remove the existing scale from the meter, prise off the transparent meter front, and carefully remove the scale card by undoing the two holding screws. Measurements can then be taken for preparing the oversize drawing.

To fit the new scale, cut out the photographic reproduction and paste it over the old scale, with edges and mounting holes of both scales properly registered.

SETTING UP MASTER POTENTIOMETER AND READOUT METER

With red, green, and blue p.v.c. covered wires, connect the master potentiometer tag strip (Fig 6.7) to the solder tags on the power pack output terminals. Also, temporarily link the rear of MP/SK2 to the green earth wire. Rotate VR20 spindle fully clockwise and patch MP/SK2 to SK3, MP/SK5 to SK6, MP/SK1 to SK4, and link RM/SK2 to VS1/SK1. Switch on the computer and S6, and adjust VS1 for an exact +10V. Now obtain a null on the readout meter by setting VR1 on the voltage divider bracket, from the back of UNIT "B" box.

Repeat for VR2 with an input of +1V by transferring the patching lead plug from MP/SK6 to SK7, and again for VR3, SK8, with an input of -1V, and VR4, SK9, with an input of -10V.

After that, while still nulling with a -10V input, rotate VR20 spindle slightly clockwise, until the meter pointer just begins to move away from zero. Place the large knob on VR20 spindle, with the transparent plastic cursor aligned with the "10" division, and tighten the grub screw. Set VR20 cursor to the "5" division and check for null with an input of -5V. It may be necessary to slightly re-position VR20 knob on the spindle, and trim VR1-VR4 again to minimise errors.

Calibration of the readout meter is straightforward. Apply a selection of known voltages to RM/SK1 and

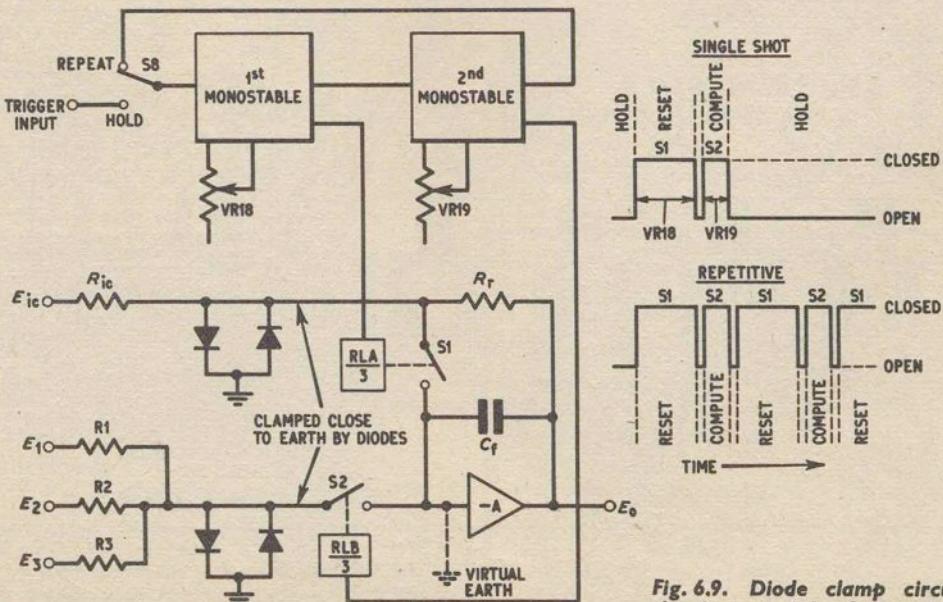


Fig. 6.9. Diode clamp circuit, showing principle of operation

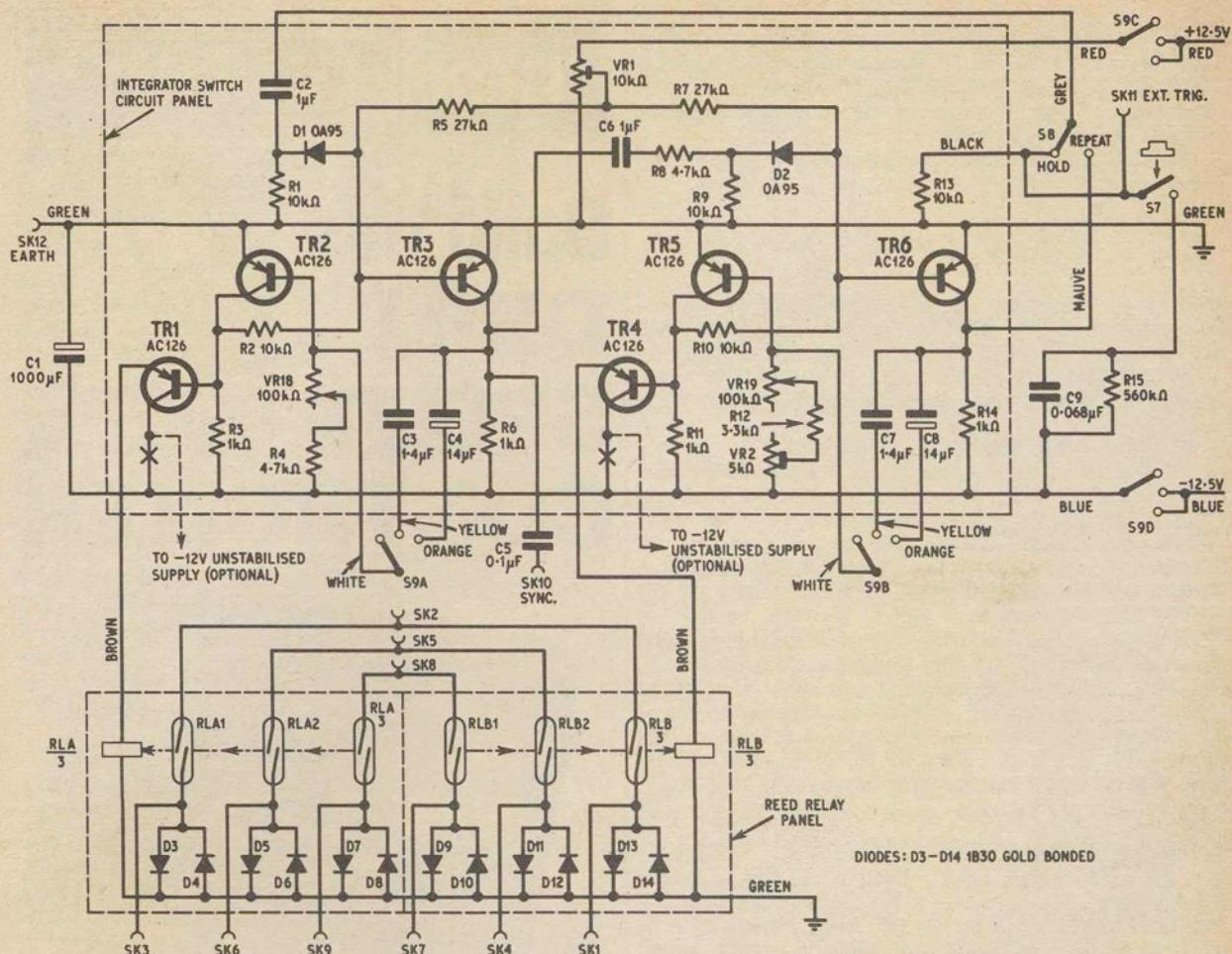


Fig. 6.10. The complete circuit diagram of the integrator switch

adjust VR1-VR4 on the resistor panel for optimum accuracy on each range.

INTEGRATOR MODE SWITCHING

The simplest type of integrator switch employs a mechanical relay with several sets of contacts, driven by an astable multivibrator, and this system is used for small demonstration and educational analogue computers. The relay is arranged to "gate" the inputs of several amplifiers simultaneously.

The PEAC integrator switch goes a stage further, with reed relays for a "clean" switching action at high speeds, full initial condition facilities, and a circuit based on two independently timed monostable multivibrators.

Referring back to the basic integrator switch shown in Fig 1.2c, two changeover switches S1 and S2 are opened and closed in a pre-determined sequence, governed by an external timing circuit. It is important to ensure that integrating amplifier input resistors are not left floating when they are disconnected from the virtual earth summing junction, as this could seriously disturb input and other computer voltages, hence the presence of S1 and S2 earthed contacts.

DIODE CLAMPS

To eliminate the need for expensive reed switches with changeover contacts, diode clamps can be used instead of an earthed contact, see the alternative

amplifier circuit of Fig 6.9. The diodes do not interfere with the normal working of the integrator, but will nevertheless hold resistor junctions close enough to earth to prevent load variations when S1 and S2 are open, and this modification more than halves the cost of switching components.

In the block diagram of Fig 6.9, the 1st monostable—controlled by VR18—determines the period of closure of S1. When S1 opens after a timed interval, a pulse is delivered to the input of the 2nd monostable, thus closing S2. S2 will remain closed for an interval controlled solely by VR19.

For "single shot" operation, a trigger pulse applied to the 1st monostable input, when S8 is switched to "hold", will initiate the closure of S1 (reset) and bring the integrating amplifier to its initial condition.

As soon as S1 opens, S2 closes (compute) and connects input resistors to the summing junction. At the end of the compute period, S1 and S2 are both open (hold), the monostables are quiescent, and the amplifier output voltage is held steady by the action of capacitor Cr. The next computer run is started by another trigger pulse applied to the 1st monostable input.

Repetitive operation is achieved by passing the output pulse from the 2nd monostable back to the input of the 1st monostable, when S8 is switched to "repeat". S1 and S2 are then made to open and close alternately, and the "hold" facility is deleted.

The method of inserting an initial condition voltage is as follows. When S1 is closed the reset resistor R_r is connected between the amplifier output and summing junction, and can therefore be regarded as a feedback resistor in parallel with C_f .

As long as S1 remains closed, R_{ic} will be acting as an input resistor, so that

$$E_o = - E_{ic} \frac{R_r}{R_{ic}}$$

and $E_o = - E_{ic}$ when $R_r = R_{ic}$. R_{ic} and R_r are disconnected from the amplifier summing junction when S1 opens, but C_f will "remember" the initial condition voltage and hold the amplifier output steady prior to the application of compute voltages when S2 closes.

INTEGRATOR SWITCH CIRCUIT

The complete circuit of the integrator switch is shown in Fig. 6.10. The 1st monostable consists of TR2 and TR3, with RLA actuated by emitter follower TR1. VR18 continuously covers two ranges given by C3 (10-100ms), and C4 (0.1-1s). Components associated with the 1st monostable input are C2, R1, and D1.

The 2nd monostable is almost identical to the 1st. TR4 drives RLB, C7 and C8 offer the same timing range coverage as C3 and C4, and input components are C6, R8, R9, and D2. However, more care is taken to establish the correct values for 2nd monostable timing capacitors C7 and C8, and VR2 allows precise calibration of the "fast end" of the VR19 timing scale, so that compute intervals can be determined by a reasonably accurate dial setting.

VR1 establishes the working point of both monostables, to achieve reliable operation at all dial settings. S7 is a push button on the front panel for starting a "single shot" computer run. Full control of an oscilloscope trace, from UNIT "B" front panel, can be realised by suitable connection to the integrator switch circuit. With S8 switched to "hold", the mode sequence can be triggered repetitively, with a variable hold interval, by the oscilloscope timebase output or by a separate oscillator. Consistent synchronisation of the trace, with continuous or single-sweep timebases, is made possible by linking IS/SK10 to an appropriate oscilloscope input.

A SEPARATE SUPPLY

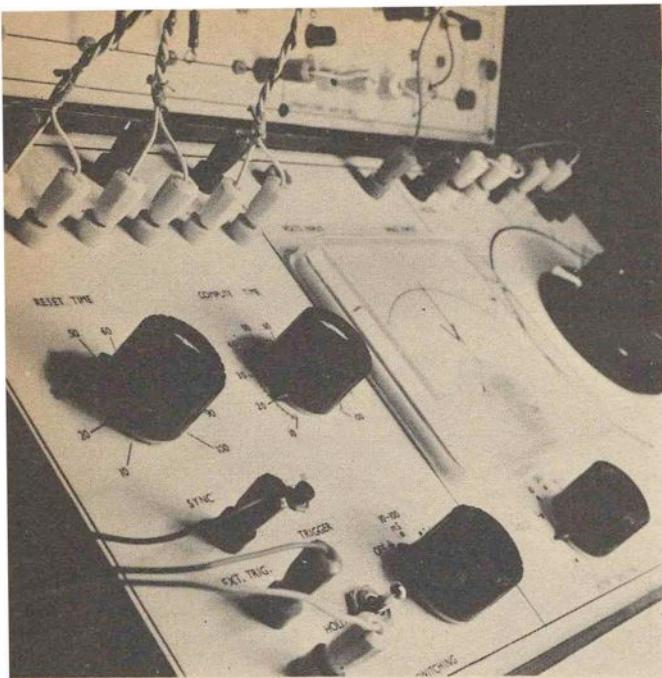
The load capacity of the existing stabilised power supply can be improved by wiring the collectors of TR1 and TR4 (shown dotted in Fig. 6.10) to a separate -12V unregulated supply, which can be housed inside the UNIT "B" box, and in this event C1 could be omitted from the Fig. 6.10 circuit, as it merely serves to prevent current pulses from flowing in the negative stabilised supply line during relay switching.

RLA and RLB consist of two triple-switch coils, catering for the needs of three integrating amplifiers. A duplicate relay panel could be added later, by wiring relay coils in parallel, to increase the switching capacity to six amplifiers.

CORRECTION

In Fig. 5.7, the captions for the first and second oscilloscopes (top row, left and centre) should be transposed.

Next month: Assembly and setting up of the Integrator Switch; practical examples in the use of this section. Introduction of UNIT "C" Function Generator.



ANALOGUE COMPUTER

PEAC

TO COMPLETE the construction of UNIT "B", we have now to deal with the integrator switching section, the circuit diagram for which has already been given, see Fig. 6.10.

INTEGRATOR MODE SWITCH ASSEMBLY

Cut and drill the $6\frac{1}{4}$ in \times $2\frac{1}{4}$ in s.r.b.p. panel shown in Fig 7.1, and rivet turret tags in the positions shown. From six transistors select two with the highest current gain for TR2 and TR5. Mount all components, except range capacitors C3, C4, C7, and C8, on the s.r.b.p. panel and wire up.

Prepare the 3in \times 2in relay panel, from Fig. 7.2. Fix turret tags and mount RLA and RLB reed coils. Next, insert miniature diodes D3-D14, with alternating polarities along the row of diodes, and complete underside wiring. To finish off the relay panel, place three reed switches in each coil and secure by soldering the lead out wires to appropriate turret tags.

Wooden blocks are glued to the rear of the UNIT "B" front panel to serve as mounts for switching circuit panel and relay panel (see Fig. 7.3). Note that the relay panel is fitted end-on into slots cut in its mounting blocks, and the switching circuit panel is secured by two woodscrews.

After first attaching lengths of black and white p.v.c. covered multi-strand wire to the terminals of VR18 and VR19, screw the switching circuit panel in position

on its blocks, and, following Fig. 6.10 and Fig. 7.3, wire all controls and sockets to the turret tags on the two sub-assembly panels, again with p.v.c. covered flexible wire, long enough to allow the switching circuit panel to be turned over for underside inspection. Run red and blue wires from S9, and a green wire from IS/SK12, to the power pack output solder tags, and fit knobs to S9, VR18, and VR19.

SETTING UP THE INTEGRATOR SWITCH

Time intervals can be measured with fair accuracy when an operational amplifier is employed to integrate known voltages, and this method is useful for setting up the integrator switch.

Begin by temporarily soldering $8\mu F$ electrolytic capacitors in the C4 and C8 positions, with $1\mu F$ polyester capacitors for C3 and C7 (circuit Fig. 6.10).

Set VR1 and VR2 with sliders at mid-track, on the integrator switch panel.

Connect integrating switch to the operational amplifier by linking IS/SK7 to OA3/SK9, IS/SK8 to OA3/SK10, and IS/SK9 to OA3/SK4. Fit 100 kilohm computing resistor in S3/I1/SK3 and SK4. Join S3/I1/SK1 to VS1/SK2 and switch off S6. Insert a 2 kilohm reset resistor in OA3/SK5 and SK6, and join S3/SK5 to OA3/SK13.

By D.BOLLEN

Switch on the computer and allow a warm up period before zero setting OA3 from the back of the UNIT "A" box, by means of VR1 on the OA3 amplifier panel. Insert a $1\mu F$ computing capacitor into OA3/SK11 and SK12.

With S8 switched to "hold", S9 on the 0.1-1s range, and VR18 and VR19 rotated fully clockwise, press S7 to run the integrating amplifier through reset, compute, and hold sequence.

Listen for two clicks from the reed relays, and observe that the readout meter pointer will move close to zero. If the relays click more than twice, or not at all, adjust VR1 on the integrator switch panel.

To obtain a true zero output from the amplifier, when integrating a zero input voltage, adjust VR17 (OA3 balance control) while repeatedly pressing S7. If there is a slow drift away from zero output several seconds after S7 was last pressed, retrim VR1 on the OA3 amplifier panel.

As the gain of OA3 is set at 10 ($1\mu F$ for C_f and 100 kilohm for R_{in}), an input of $-0.9V$ "gated" by the integrator switch for an interval of 1s should give rise to an amplifier output of exactly $+9V$. Switch on S6 and adjust VS1 for $-0.9V$, monitored at S3/I1/SK2 by a voltmeter.

Now when S7 is pressed, and with VR19 still rotated fully clockwise, the readout meter reading should rise to somewhere below $+9V$ and stay there.

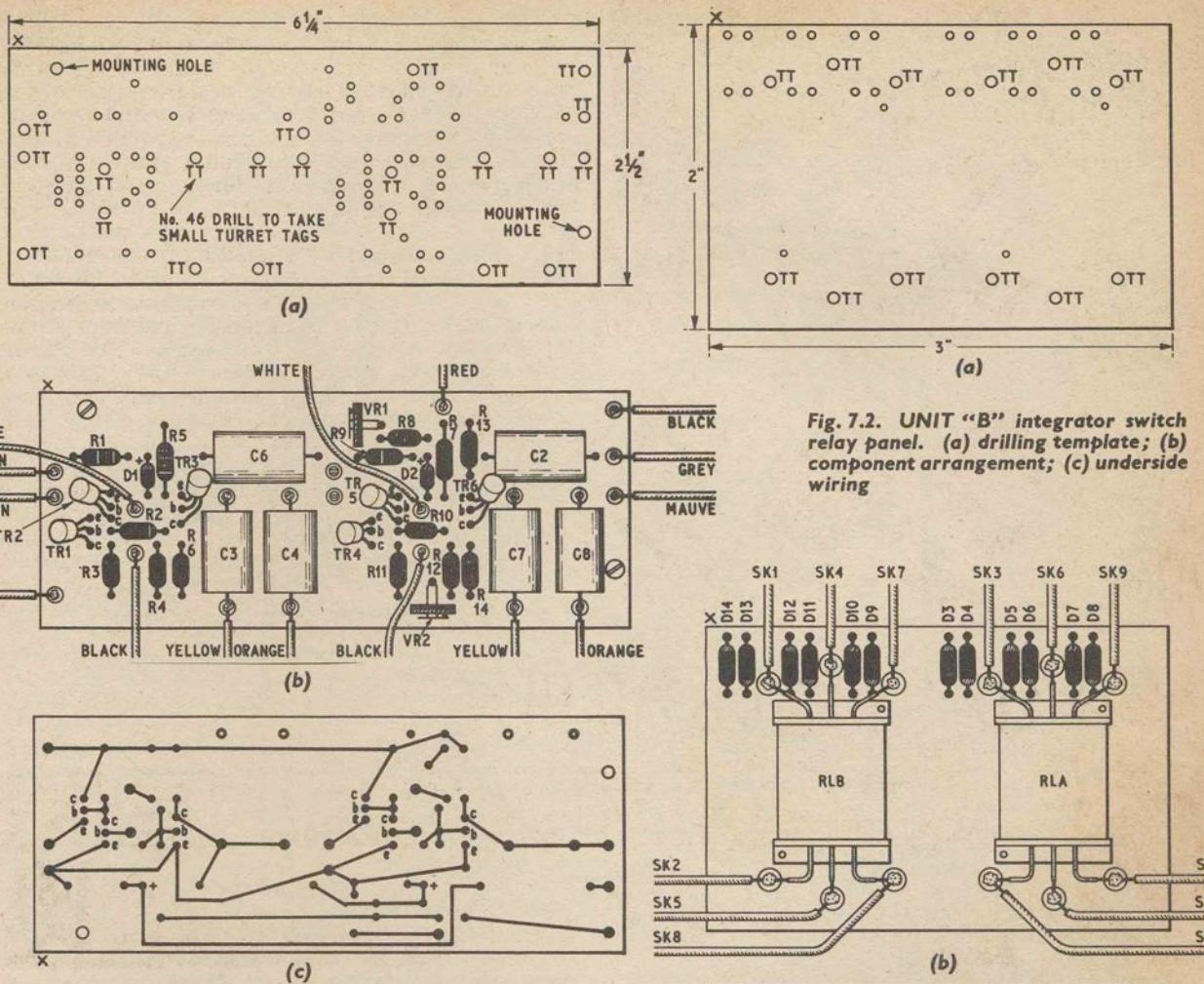
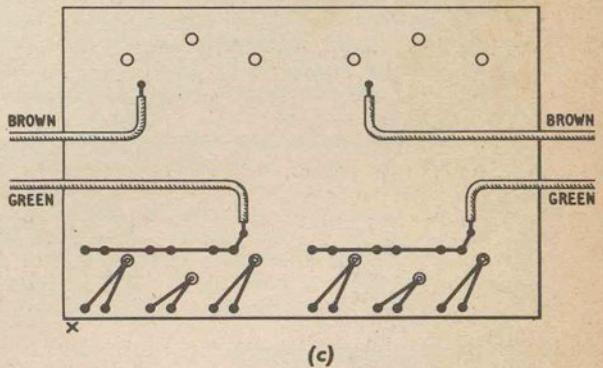
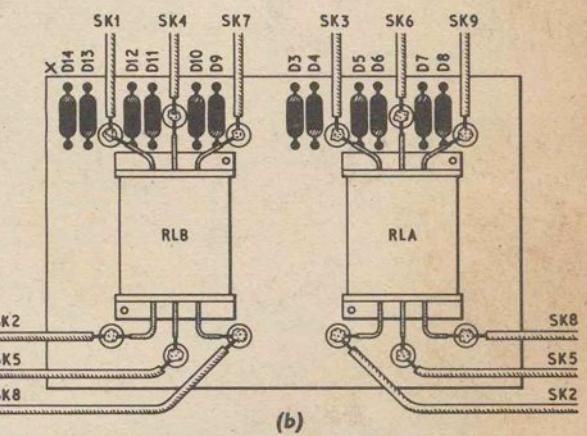


Fig. 7.1. UNIT “B” integrator switch circuit panel, (a) drilling template; (b) component arrangement; (c) underside wiring

Build up the value of C8 timing capacitor by adding more capacitors in parallel, until the +9V output is obtained when S7 is pressed.

To check the “fast” end of VR19 scale, set VS1 for -9V and rotate VR19 fully anti-clockwise. Adjust VR2 on the integrator switch panel to obtain the desired amplifier output of +9V for a compute interval of 0.1s.

Fig. 7.2. UNIT “B” integrator switch relay panel. (a) drilling template; (b) component arrangement; (c) underside wiring



Section of UNIT “B” panel (viewed from rear) showing integrator switch relay assembly

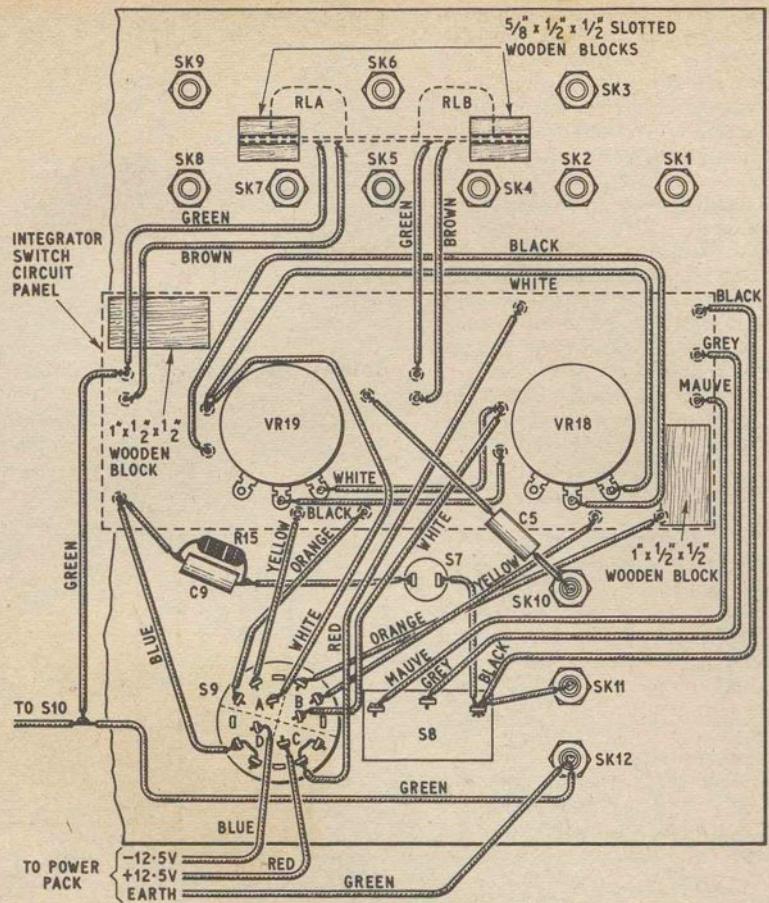


Fig. 7.3. Rear view of UNIT "B" front panel showing integrator switch wiring

CALIBRATING THE SECOND RANGE

To calibrate the 10–100ms S9 range, repeat the above procedures in just the same way, but this time use a $0.1\mu F$ capacitor for C_1 in sockets OA3/SK11 and SK12, and adjust the value of timing capacitor C_7 for correct compute intervals.

1st monostable timing capacitors C_3 and C_4 need not be precise, as VR18 has no effect on the accuracy of computations, and is mainly used to control the switch cycle frequency when integrator output waveforms are displayed by oscilloscope. Therefore, and merely for the sake of conformity, build up C_3 and C_4 capacitor values until the coverage of VR18 is approximately as indicated by the reset interval dial calibration.

CIRCUIT ADJUSTMENTS

The Fig 6.10 circuit should operate reliably at all switch and dial settings, with no noticeable relay bounce or overlap between the closure of reset and compute switches. However, it may be found that the integrator switch will stop running during repetitive operation, when reset and compute intervals approach 10ms, despite the fact that VR1 has already been trimmed for optimum performance. If so, try reducing the value of R_8 .

At the opposite extreme, if the integrator switch suddenly goes into repetitive operation when S8 is at "Hold", and VR18 and VR19 settings are near 1s, increase R_8 , and also try the effect of doubling the value of C_1 to improve decoupling.

PROBLEM EXAMPLE 4

STRAIGHT PATH MOTION OF AN OBJECT

Problem Example 4 is primarily intended as a comprehensive introduction to the use of integrator mode switching, but the programme is sufficiently flexible to allow many experiments in dynamics to be performed.

Several factors can combine to influence the overall motion of an object, and some are shown in the ball problem of Fig. 7.4. A ball thrown vertically into the air will be subject to an initial upward velocity $i v$, retardation or negative acceleration due to gravity $-a$, and air resistance. The situation is further complicated if the ball is projected upwards from an initial height $i s$, and is arrested at some height other than zero.

Ignoring for the moment air resistance, the equations which govern the motion of the ball are,

$$v = \int_0^t a dt + iv \quad (\text{Eq. 7.1})$$

$$\text{and} \quad s = \int_0^t v dt + is \quad (\text{Eq. 7.2})$$

Clearly, integration of a yields v , and a further integration of v will give s .

The formulae used to calculate velocity or distance when acceleration is constant are,

$$v = iv + at \quad (\text{Eq. 7.3})$$

$$\text{and} \quad s = ivt + \frac{1}{2}at^2 + is \quad (\text{Eq. 7.4})$$

Eq. 7.3 and 7.4 will not apply if, for example, acceleration is proportional to time. A discussion of the implications of variable acceleration lies outside the

scope of this series, but time varying voltage analogues of acceleration are fairly easy to generate on the computer.

The drag on a body moving through air or a fluid conforms to an exponential law, and is proportional to velocity when there is little or no turbulence. Viscous friction should not be confused with the friction resulting from solid surfaces in contact, as the latter is independent of velocity except at very low speeds. A general solution to an equation which describes the motion of an object through a viscous medium—where composite velocities are involved—is often unwieldy and can demand extensive calculations.

However, an exponential decay can be set-up on the computer to simulate true viscous friction, in terms of a coefficient value μ which remains constant for all velocities. Nevertheless, as μ will be dependent on such factors as the surface area, shape, and relative smoothness of an object, it can only be determined by practical experiment, or by comparison between the computer solution and the timed motion of an actual object.

Looking at the symbolised diagram of Fig. 7.5, OA1 is employed to integrate a known voltage against time, so that t can be conveniently and accurately displayed as a meter reading. OA2 integrates a to give an output v , and at the same time handles the initial velocity iv . The exponential decay $e^{-(\mu/m)t}$ is introduced by CP1. Resulting velocity v is then integrated by OA3 and initial distance is is included to give distance or height s at any time t .

Routine. Set-up the problem according to the simplified patching circuit of Fig. 7.5 but omit for the time being all C_f capacitors. The integrator switch is linked to the three operational amplifiers by connecting IS/SK1 to OA1/SK9, IS/SK2 to OA1/SK10, IS/SK3 to OA1/SK4, IS/SK4 to OA2/SK9, IS/SK5 to OA2/SK10, IS/SK6 to OA2/SK4, IS/SK7 to OA3/SK9, IS/SK8 to OA3/SK10, and IS/SK9 to OA3/SK4.

Allow the computer to warm up before zero-setting the amplifiers, also make sure that S6 is off. Using the readout meter on its 10V range, zero-set amplifier outputs (OA1/SK13, S3/I5/SK2, and OA3/SK13) by means of VR1 on each amplifier panel, from the back of the UNIT "A" box.

Next insert the C_f computing capacitors into amplifier feedback loop sockets (SK11 and SK12) and set the integrator switching controls to give reset and compute

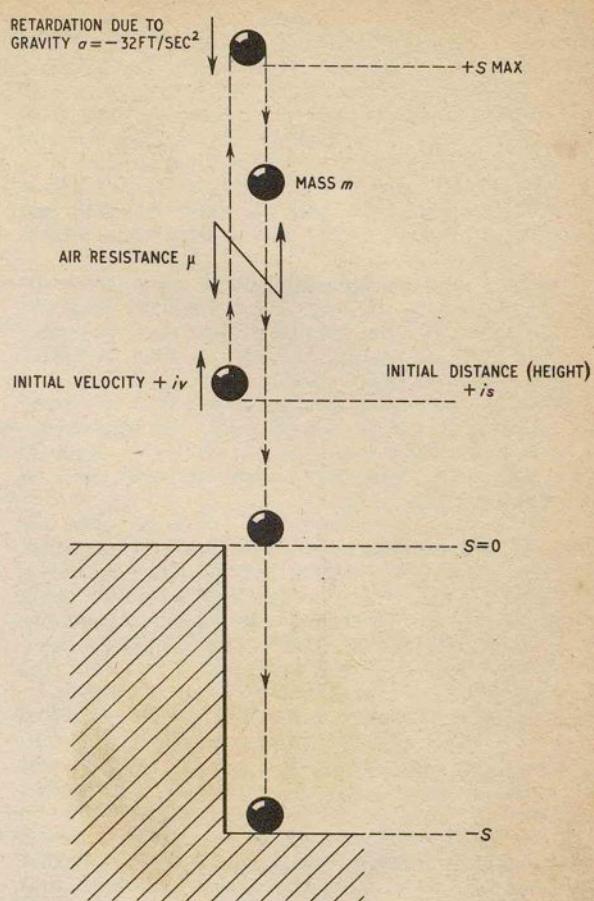
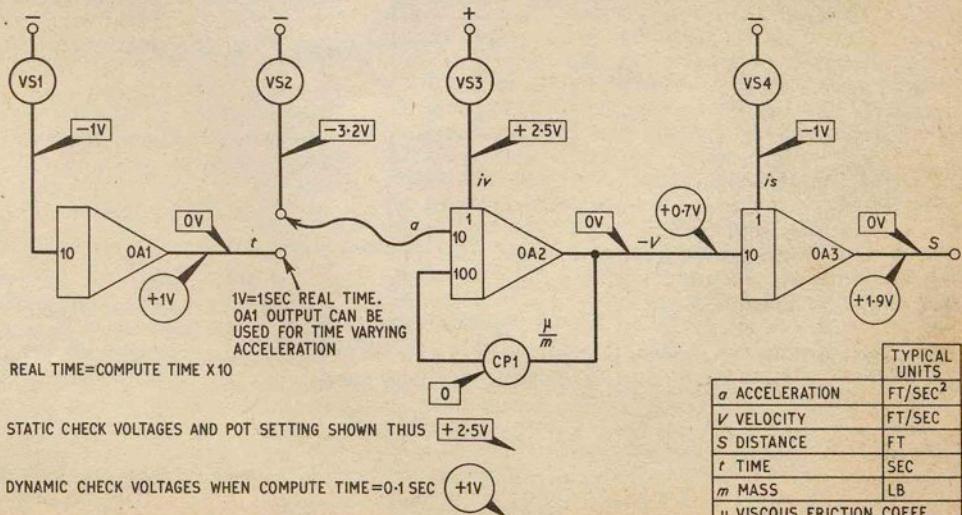


Fig. 7.4. An experiment in dynamics with a ball

times of approximately 0.1 second. Put S8 in the "hold" position. With the readout meter on its 1V range, applied to the output of OA1, press S7 and adjust VR15 for a zero voltage reading. Repeat for OA2 output and VR16, and OA3 output and VR17, in that order. The amplifiers should now be balanced for near zero input offset voltage.

Fig. 7.5. Symbolised diagram of the ball problem illustrated in Fig. 7.4.



To enable static and dynamic checks to be made, trial values are given to the ball problem of Fig. 7.4, as follows: $t_{\text{real}} = 1 \text{ sec}$, $a = -32 \text{ ft/sec}^2$, $iv = 25 \text{ ft/sec}$, $is = 10 \text{ ft}$, $v = -7 \text{ ft/sec}$, $s = 19 \text{ ft}$, and $\mu/m = 0$. The problem scaling is such that 1 computer volt = 10 units in all cases. For example, 1V = 1 sec for t at the output of OA1 ($10 \times$ compute time), and 1.9V = 19ft for s at OA3 output. Calculation from the formula Eq. 7.4 shows that the ball will have travelled just beyond s_{max} after a time of 1 sec, when air resistance is zero.

The next stage is to establish all computer static voltages shown in the Fig. 7.5 symbolised diagram, starting with VS1. Set the dial of the master potentiometer to "10" and patch MP/SK1 to SK4, MP/SK2 to SK3, and MP/SK5 to SK8. Connect RM/SK2 to S1/I1/SK2. Switch on S6, set switch S10 to "null" and adjust VS1 dial for a null meter reading, corresponding to a voltage source output of -1V. Remove the null input patching lead completely, and use it to link RM/SK1 to OA1/SK13.

With the readout meter on its 1V range, press S7, and trim compute time control VR19 for an integrator output of 1V; this will ensure that the compute interval is exactly 0.1 sec. Set up VS2, VS3, and VS4 check voltages, preferably by nulling with the master potentiometer to avoid loading, and rotate CP1 fully anti-clockwise. Switch off S6 and press S7 to reset the amplifiers. Check that amplifier outputs are zero.

To obtain dynamic check voltages, switch on S6 and press S7, while applying the readout meter to the outputs of OA1, OA2, and OA3 in turn. For greater convenience, three separate voltmeters can be left connected as shown in the patching circuit of Fig. 7.5 to give simultaneous readouts of t , v , and s . Before altering other problem variables, introduce air resistance by means of CP1 and arrest the travel of the ball at selected positions along its path by adjusting the compute time. It is instructive to compare the velocity and distance of the ball when $a = -32 \text{ ft/sec}^2$ and friction is present, with a ball projected upwards under moon gravity conditions (approximately $a = -5.3 \text{ ft/sec}^2$) in a vacuum.

The existing scaling of layout Fig. 7.5 will provide the following coverage: VR2 $0 \pm 100 \text{ ft/sec}^2$, VR3 $0 \pm 100 \text{ ft/sec}$, VR4 $0 \pm 100 \text{ ft}$, with amplifier outputs of OA1 $0.1 \text{ to } 10 \text{ sec}$, OA2 $0 \pm 100 \text{ ft/sec}$, and OA3

$0 \pm 100 \text{ ft}$. The coefficient of CP1 covers the range 0-10 for μ/m .

If at any instant during a computer run velocity exceeds 100 ft/sec , or distance is greater than 100 ft , this will result in amplifier overloading, and a false problem solution. Spot checks of velocity or distance voltage trends can be made at selected compute times, using the single shot facility, and s_{max} will correspond with $v = 0$ at a particular time t . Alternatively, during repetitive integrator switching, an oscilloscope will serve to show amplifier overloads as a flattening or clipping of an output waveform, but this should not be confused with the short "hold" interval which separates the opening and closing of reset and compute switches.

RESCALING PROBLEM EXAMPLE 4

The programme of Problem Example 4 need not be confined to the vertical motion of an object in air, but could equally well apply to movement up and down an inclined plane in water, or else the horizontal progress of a fast wheeled vehicle being decelerated by braking forces, for example.

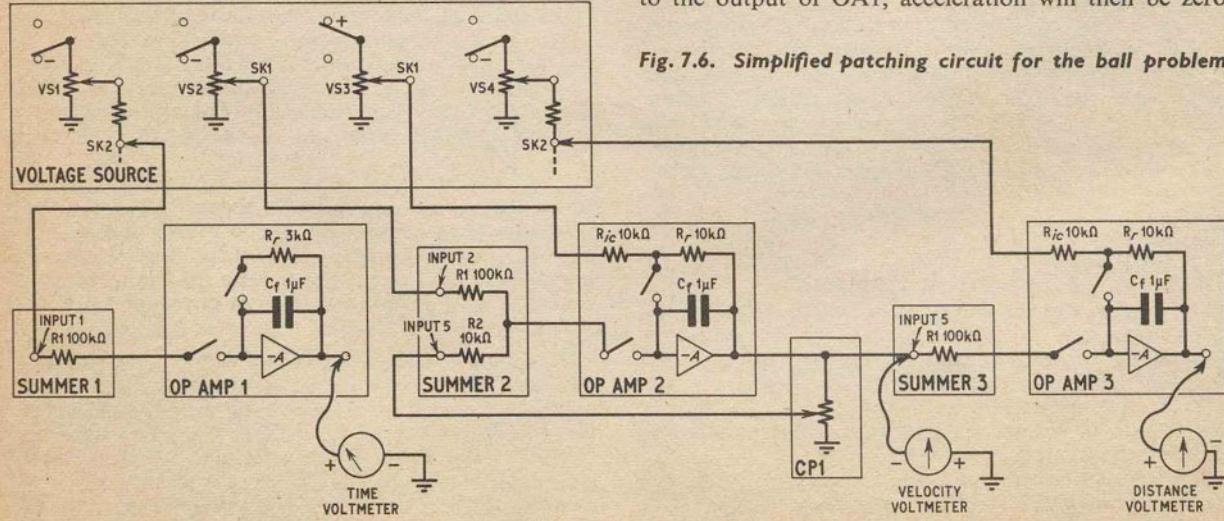
There are several ways of rescaling Problem Example 4, the most obvious being the adoption of other unit systems, such as miles/hour, centimetres/sec, or even inches/year. Providing that compatible units are employed, and computer voltages are correctly interpreted, there are no serious barriers to unit system rescaling. Probably the most straightforward way of verifying a new problem scaling is to set up a simple check problem, where known values of t , a , v , and s are computed for an object in a vacuum, to establish the relationships between static and dynamic voltages.

Where it is desired to extend the range of an existing unit system, increasing the value of computing capacitors by a factor of ten will reduce real time by ten. Similarly, a tenfold increase in real time is achieved when C_r values are divided by ten.

When employing large computing capacitors at short compute times, always ensure that the reset resistor R_r is small enough to completely discharge C_r during the reset interval. It is also possible to alter the computer voltage scaling so that, for example, 1 computer volt will equal 100 units instead of 10 units, but care should be taken to make sure that all voltages and potentiometer settings conform to the new scaling.

Finally, a word or two about variable acceleration. If the input to OA2 is transferred from the VS2 source to the output of OA1, acceleration will then be zero

Fig. 7.6. Simplified patching circuit for the ball problem



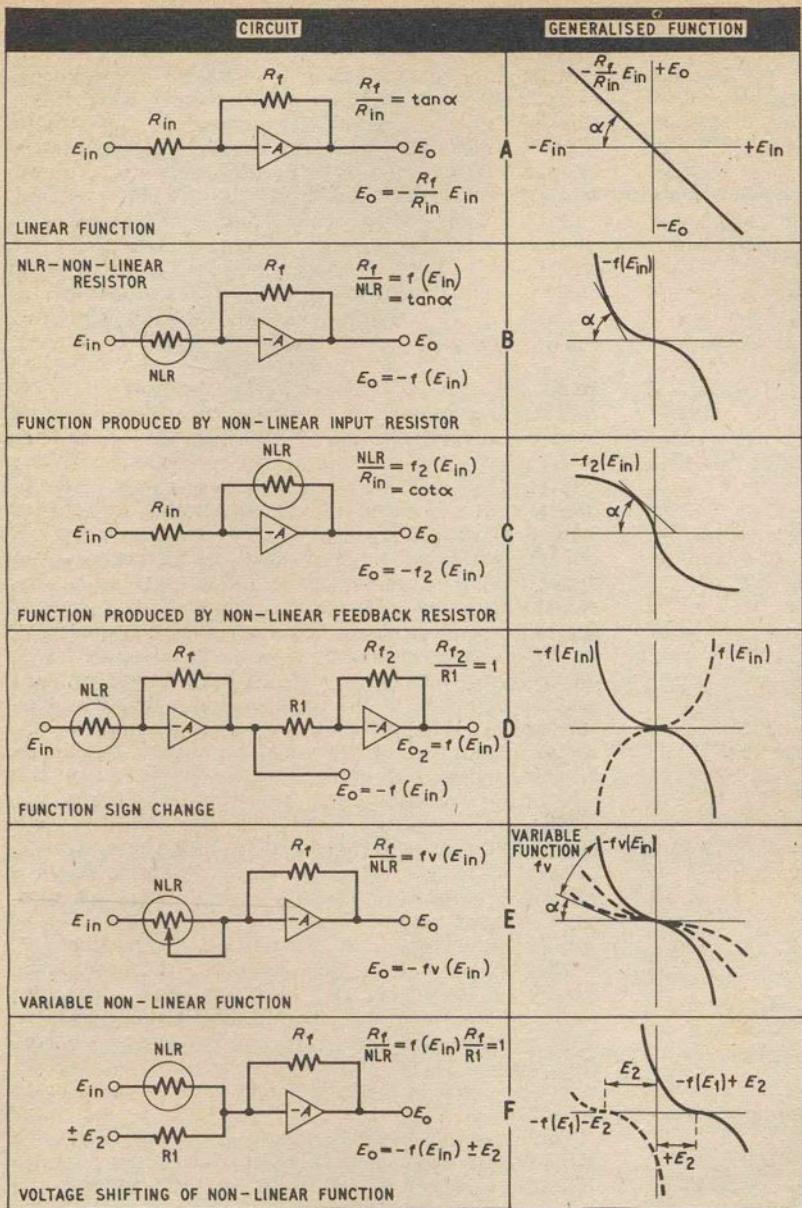


Fig. 7.7. Generating non-linear functions with a voltage dependent resistor

when $t = 0$, and increases linearly to 10ft/sec^2 when $t = 1$ sec real time. VS1 can be used to adjust the magnitude of a when $t > 0$. Also, if OA1 initial conditions are inserted, in a similar manner to OA2 and OA3, many other time functions of a can be generated.

UNIT "C" FUNCTION GENERATOR

UNIT "C" contains two diode-resistor networks, one for positive input voltages, and the other for negative inputs. The characteristics of each network can be adjusted separately by means of miniature pre-set potentiometers to give a wide range of possible functions, and optimum accuracy. The function generator is designed to be used in place of a normal computing resistor, at the input or in the feedback loop of an operational amplifier.

When employed for squaring an input voltage, with both networks operating in parallel, the function generator will accept input voltages of $0 \pm 10\text{V}$, and yields amplifier outputs of up to $\pm 10\text{V}$. Accuracy can be within 2 per cent of the indicated value, depending on the care taken in setting up a function, for input voltages between 0.2V and 9V .

NON-LINEAR FUNCTIONS

Quite often some non-linear function of an applied voltage is needed in analogue computer work, two simple instances being the square or square root of a number. An arbitrary function may also be encountered, perhaps arising from experimental data for which no analytic expression is available.

Servo driven potentiometers and circuits consisting of biased diodes are widely used for generating non-linear functions, but the latter is deservedly popular because it can be adjusted to cater for a range of functions, and does not suffer from a severely limited frequency response.

To show how a diode function generator can give rise to non-linear functions, when allied to operational amplifiers, use is made here of the parallel which exists between the discontinuous behaviour of a biased diode network, and the smooth response of a voltage dependent resistor. Both can display a fall in resistance with an increase in applied voltage.

Consider first of all the circuit and generalised curve of Fig. 7.7a. Input and feedback resistors R_{in} and R_f are not influenced by applied voltage, therefore a straight line function is generated, while amplifier gain and $\tan \alpha$ remains constant. However, if some form of non-linear resistor, or biased diode network, is substituted for R_{in} (NLR in Fig. 7.7b) the gain of the amplifier

tends to grow with an increase of E_{in} , and the tangent to the curve will vary according to some function $f(E_{in})$, arising from the characteristic of NLR. A related function $f_2(E_{in})$ results when NLR is exchanged for R_f , as in Fig. 7.7c, but here the amplifier gain falls off with an increase of E_{in} . The curves of Fig. 7.7b and Fig. 7.7c only occupy two of four possible quadrants, but four quadrant operation can be achieved if the function is inverted by a sign changing amplifier, depicted in Fig. 7.7d.

Fig. 7.7e shows how curves, of widely differing slope and magnitude, may be generated if the characteristic of NLR is alterable. Finally, any fixed function will find wider application if its $E_{in} = 0$ datum is shifted, as in Fig. 7.7f. Moreover, as a voltage shift can also be applied to the E_o axis, it becomes a simple matter to locate any portion of a curve in any quadrant.

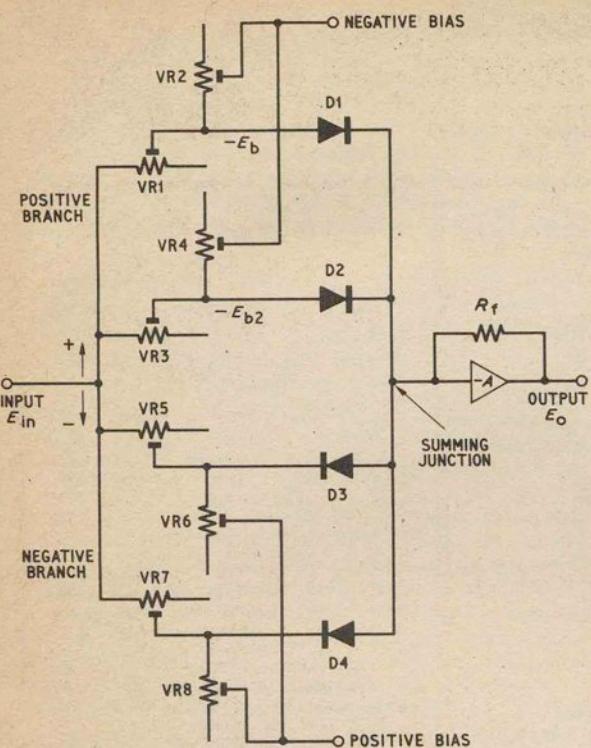
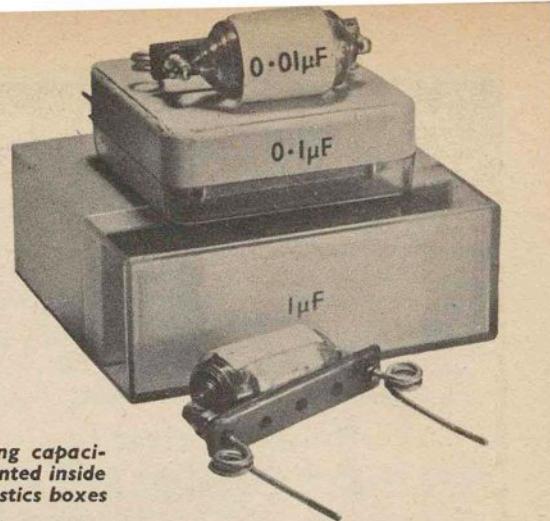


Fig. 7.8a. Circuit of a simple function generator

BIASED DIODE NETWORK

The next step is to see how biased diode networks are used to achieve an increase of resistance with applied voltage, and thus imitate the behaviour of an *ideal* voltage dependent resistor. Unfortunately, currently available silicon carbide, selenium, and copper oxide resistors are far from ideal in many respects, and are not sufficiently accurate for serious use with operational amplifiers.



Computing capacitors mounted inside small plastics boxes

The UNIT "C" function generator is based on the simple circuit of Fig. 7.8a. In the absence of an input voltage all diodes are biased off, and the network can be represented by a very high value of resistance in series with the operational amplifier input, giving an amplifier gain of almost zero. If a positive voltage is gradually applied to the input terminal, there will be virtually no output until a point is reached where E_{in} is slightly larger than $-E_b$, whereupon D1 conducts and connects VR1 to the operational amplifier summing junction. Further increase of E_{in} , beyond $-E_b$, will produce a straight line output of slope determined by the amplifier gain $R_f/VR1$.

When E_{in} reaches approximately the level of $-E_{b2}$, D2 conducts and places VR3 in parallel with VR1, thus reducing even more the effective resistance of the network. It can be easily imagined that where a number of diodes and variable resistances are cascaded, the resistance of the network will continue to fall as E_{in} becomes larger still.

Bias voltage $-E_b$ is determined by the relative resistances of VR1 and VR2, and the same applies to $-E_{b2}$, VR3 and VR4. Furthermore, the setting of VR1 will obviously affect the combined slope of VR1 and VR3 (see Fig. 7.8b), and it follows that all the resistance settings associated with D1 and D2 must be interrelated.

Considerations applying to the positive branch of circuit Fig. 7.8a are also pertinent to the negative branch formed by D3 and D4, and VR5-VR8, except that input and bias voltage polarities are reversed. There is no interaction between the resistance settings of the positive branch and the negative branch, and the two can be separated when required for independent use.

The output characteristic curve of Fig. 7.8b identifies slopes and breakpoints with VR1-VR8. As there are only two diodes in each branch, the result is a very rough approximation to a smooth curve. Generally speaking, the accuracy of a diode function generator is proportional to the number of diodes employed, but a natural rounding at the junction of straight lines does occur at low input voltage levels, due to the dynamic resistance of the diodes (not shown in Fig. 7.8b), so the deviation from a smooth curve is not as great as might be expected. Commercial diode function generators sometimes use more than 20 diodes to achieve accuracies of better than 1 per cent.

Next month: Construction of UNIT "C" and some practical applications of this Function Generator.

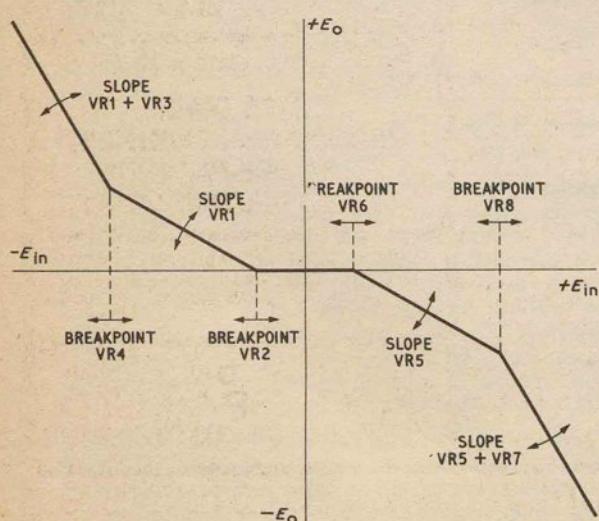
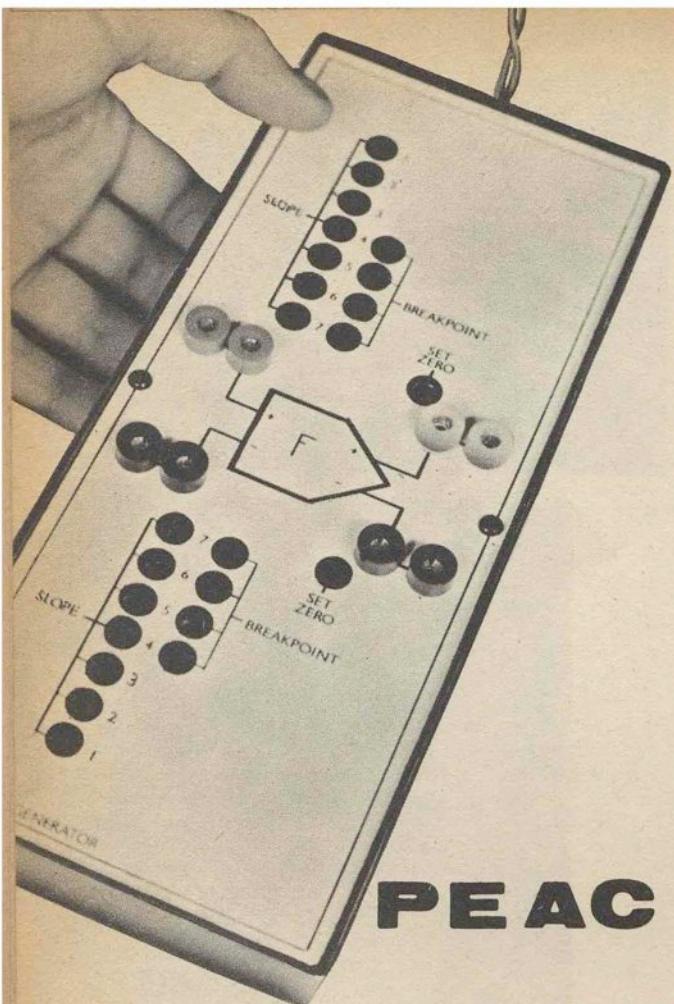


Fig. 7.8b. Adjustable characteristic of simple function generator



ANALOGUE COMPUTER

By D. BOLLEN

LAST month the Function Generator UNIT "C" was introduced. The principle of operation and some of the uses of the function generator were explained. We are continuing with a description of the practical circuit, constructional details, and application information.

FUNCTION GENERATOR CIRCUIT

The function generator circuit of Fig. 8.1 is designed to display a nominal resistance of 100 kilohm when the input voltage is $\pm 1V$. A typical resistance variation with applied voltage is from 500 kilohms at $0.2V$ to 10 kilohms at $10V$. In the Fig. 8.1 circuit, components forming the positive branch are identified by the letter A after a component number, and the letter B is appended to negative branch numbering. As both branches are identical, except for diode and bias polarities, it is not necessary to describe them separately.

D1 is a gold-bonded diode, for a low voltage drop with small input voltages. All other diodes (D2-D7) are of silicon construction to keep reverse leakage low.

The natural forward voltage drop of D1 and D2 furnishes self-bias, and bias conditions for D3 are satisfied by a fixed resistor R1. The values of slope adjusters VR1, VR2, VR3, VR4, VR6, VR8 and VR10 were selected to give a parabolic function approximating to $E_0 = E_{in}^2$ when all sliders are at mid-track, and appropriate bias values for that function are provided by mid-track settings of breakpoint adjusters VR5, VR7, VR9 and VR11. The combination VR12 and R3 serves to eliminate offset voltages resulting from diode leakage currents, and VR12 is therefore used for zero-setting.

With so many possible adjustments, including amplifier closed-loop gains determined by R_f or R_{in} computing resistors, it is obviously impossible to catalogue the coverage of the Fig. 8.1 circuit. As a rough indication though, powers of E_{in} ranging from about $E_{in}^{1.1}$ to beyond E_{in}^3 are available. If both branches are cascaded in series with operational amplifiers, the upper limit will extend beyond E_{in}^6 . Corresponding root functions^{1.1} $\sqrt{E_{in}}$ to $^6\sqrt{E_{in}}$ may also be generated. It is sometimes possible to use the UNIT "C" function generator for certain trigonometrical functions, and logs to the base 10 or e.

UNIT "C" BOX

A wood and plastics laminate box, of small dimensions compared with other PEAC units, will serve to house the two function generator circuit panels. The suggested form of construction is shown in Fig. 8.2. Softwood blocks are glued to a $9\frac{1}{2}\text{in} \times 4\text{in} \times \frac{1}{2}\text{in}$ plywood frame, which has its centre cut out, and white plastics laminate side pieces are then glued to the blocks. The front panel sits on the wooden blocks and is recessed.

UNIT "C" FRONT PANEL

The only items to be mounted on the $9\frac{1}{2}\text{in} \times 4\text{in}$ plastics laminate front panel are eight coloured sockets; the layout is given in Fig. 8.3. A series of $\frac{1}{4}\text{in}$ holes are drilled in the front panel to allow screwdriver access to slope, breakpoint, and set-zero controls. Panel markings are similar to previous PEAC units.

FUNCTION GENERATOR CONSTRUCTION

Two $3\frac{3}{4}\text{in} \times 3\frac{3}{4}\text{in}$ s.r.b.p. panels are drilled and shaped according to the Fig. 8.4a diagram. Before inserting turret tags, lay the prepared panels out as shown in Fig. 8.5, so that one panel is turned over in relation to the other, and components are clearly seen to be mounted on opposite sides. The underside wiring of the positive branch panel is shown in Fig. 8.4b, and the wiring of the negative branch is in Fig. 8.4c.

All diodes are mounted on turret tags to allow them to be disconnected for special purposes, where for

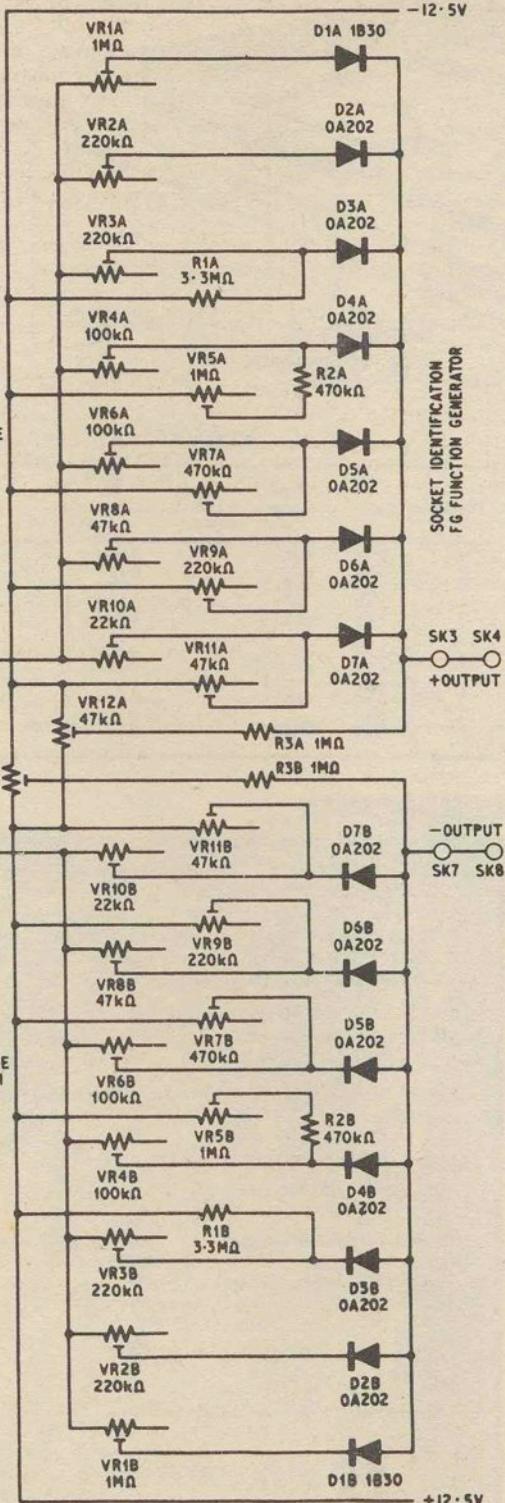
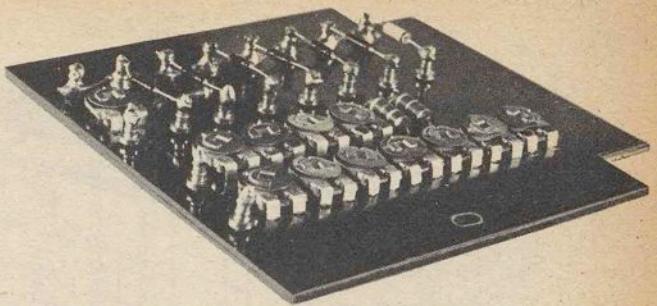


Fig. 8.1. UNIT "C" function generator circuit diagram



Function generator circuit panel

example it is desired to reduce the number of break-points, or combine a curved and straight line function. It is advisable to check the polarity of all diodes with a meter before mounting them on the circuit panels.

After completing the underside wiring, bolt the two circuit panels on the plywood frame, as in Fig. 8.5, and make sure that the front panel holes are aligned with the pre-set miniature potentiometer slots.

SETTING UP THE FUNCTION GENERATOR

Patching leads for the function generator should preferably be terminated at one end by miniature plugs, to permit connection to the UNIT "A" computing component sockets. As the generation of powers and roots is the main area of interest, functions related to the square or cube of a number are used in the following setting-up instructions.

To patch the function generator to OA1, join FG/SK5 to S1/I1/SK3, FG/SK8 to S1/I1/SK4, S1/SK5 to OA1/SK8, and link together OA1/SK9, SK10, and SK4. Insert a 100 kilohm computing resistor into OA1/SK11 and SK12. Take a patching lead from S1/I1/SK1 to VS1/SK2, and ensure that S6 is off.

The task of setting up the function generator is made easier if two voltmeters are used, one for E_{in} connected to S1/I1/SK2, and the other for E_o to OA1/SK13. The Unit "B" readout meter is ideal for monitoring E_o because it can indicate voltages down to 0.01V. Switch on the computer power supply and zero OA1 by means of its balance control VR15. Set all function generator slope and breakpoint potentiometer sliders to mid-track, and connect the red and blue wires from the function generator to the power supply terminals on the side of the UNIT "A" box (TL1 and TL2). Adjust VR12B (zero-set) for zero output from OA1.

Because of the interdependence of slope and breakpoint adjustments, a systematic approach is called for when setting up a function. Start with the lowest E_{in} and VR1 and proceed in an orderly fashion towards VR11 and the maximum E_{in} value. It is a help to tabulate specific input and output voltages and relate them to particular slope or breakpoint controls. To assist the reader, two tables have been prepared covering square and cube functions, Table 8.1 and Table 8.2.

If a square function is to be set up on the function generator, switch on S6 (Voltage Source) and set VS1 for an output of -0.2V, then adjust VR1B for an OA1 output of 0.04V. Next set VS1 for -0.5V and adjust VR2B for an output of 0.25V, and so on, according to Table 8.1. After application of $E_{in} = -2.0V$, and adjustment of VR4, change the 100 kilohm computing resistor in the feedback loop of OA1 to 10 kilohm, to prevent the amplifier overloading when E_{in} exceeds $\sqrt{10}$.

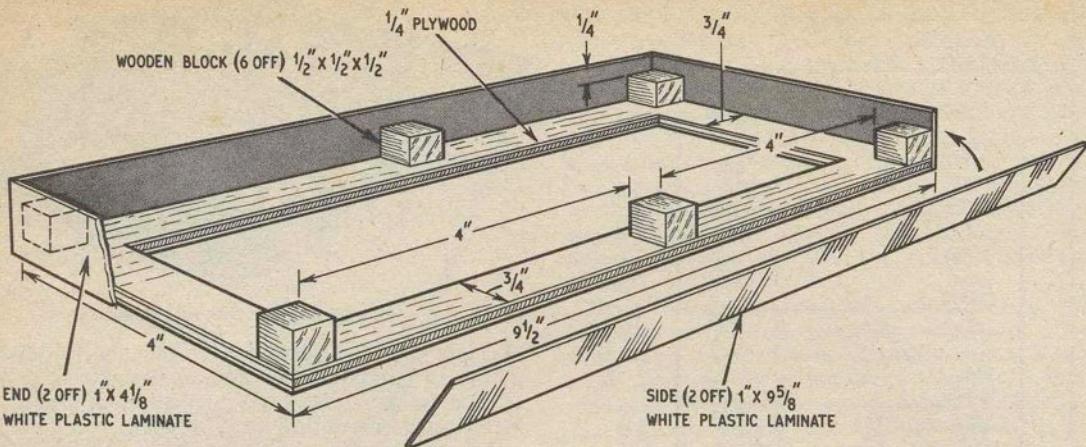


Fig. 8.2. Details and measurements of UNIT "C" function generator case

TABLE 8.1

| Diode | E_{in} | Adjust slope | Adjust break-point | E_o |
|------------------|------------------|--------------|--------------------|------------------------------|
| 1 | -0.2V | VR1 | — | + 0.04V |
| 2 | -0.5V | VR2 | — | + 0.25V |
| 3 | -1.0V | VR3 | — | + 1.0V |
| 4 | { -1.5V -2.0V | VR5 | — | + 2.25V + 4.0V |
| 5 | { -2.5V -3.5V | VR7 | — | + 0.625V |
| 6 | { -4.0V -6.0V | VR9 | — | + 1.25V + 1.6V |
| 7 | { -6.5V -9.0V | VR11 | — | + 3.6V + 4.225V + 8.1V |
| $E_o = E_{in}^2$ | | | | $R_f = 100k\Omega$ |
| $E_o = E_{in}^2$ | | | | $R_f = 10k\Omega$ |

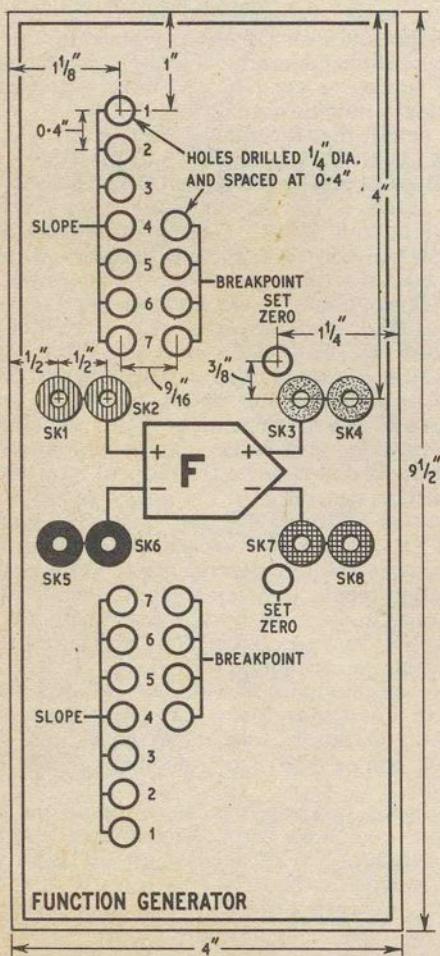


Fig. 8.3. Front panel layout of UNIT "C" function generator

COMPONENTS . . .

UNIT "C" BOX

Plywood $9\frac{1}{2}$ in \times 4 in \times $\frac{1}{4}$ in
Softwood $\frac{1}{2}$ in \times $\frac{1}{2}$ in \times $3\frac{1}{2}$ in
White plastics laminate $9\frac{5}{8}$ in \times 1 in (2 off),
 $4\frac{1}{2}$ in \times 1 in (2 off)
Rubber grommet $\frac{1}{4}$ in \times $\frac{5}{32}$ in

UNIT "C" Front Panel

White plastics laminate $9\frac{1}{2}$ in \times 4 in. Sockets: 2 red, 2 yellow, 2 black, 2 blue.

UNIT "C" Function Generator Components

Resistors

R1 3.3MΩ (2 off)
R2 470kΩ (2 off)
R3 1MΩ (2 off)
All 10%, $\frac{1}{2}$ W carbon composition

Pre-set Potentiometers

| | | |
|---------------|-------|---------|
| VR1, VR5 | 1MΩ | (4 off) |
| VR2, VR3, VR9 | 220kΩ | (6 off) |
| VR4, VR6 | 100kΩ | (4 off) |
| VR7 | 470kΩ | (2 off) |
| VR8 | 47kΩ | (2 off) |
| VR10 | 22kΩ | (2 off) |
| VR11, VR12 | 47kΩ | (4 off) |

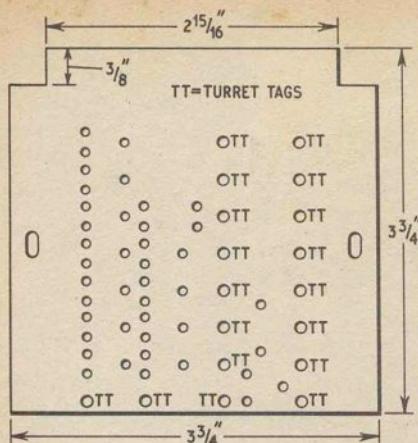
All miniature horizontal mounting

Diodes

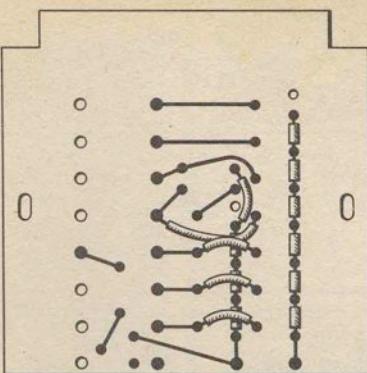
D1 1N30 (2 off) (Radiospares)
D2-D7 OA202 (12 off)

Miscellaneous

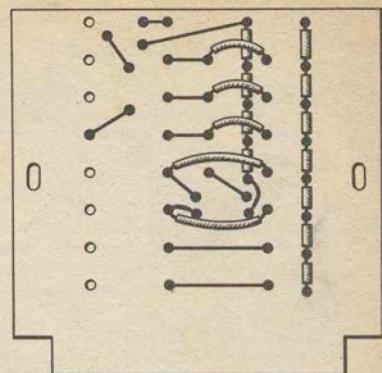
S.R.B.P. $3\frac{3}{8}$ in \times $3\frac{3}{8}$ in (2 off), Small turret tags
4mm stackable plugs, one red, one blue
(Radiospares)



(a) drilling template (2 off)



(b) positive branch underside wiring



(c) negative branch underside wiring

TABLE 8.2

| Diode | E_{in} | Adjust slope | Adjust break-point | E_o |
|-------|-------------------|--------------|--------------------|---------------------|
| 1 | -0.3V | VR1 | — | + 0.027V |
| 2 | -0.5V | VR2 | — | + 0.125V |
| 3 | -0.75V | VR3 | — | + 0.421V |
| 4 | { -1.0V -1.25V | VR4 | VR5 | + 1.0V + 1.953V |
| 5 | { -1.5V -2.0V | — | VR7 | + 3.375V + 8.0V |
| 6 | { -2.5V -3.0V | VR8 | VR9 | + 1.56V + 2.7V |
| 7 | { -3.5V -4.64V | VR10 | VR11 | + 4.287V + 10.0V |

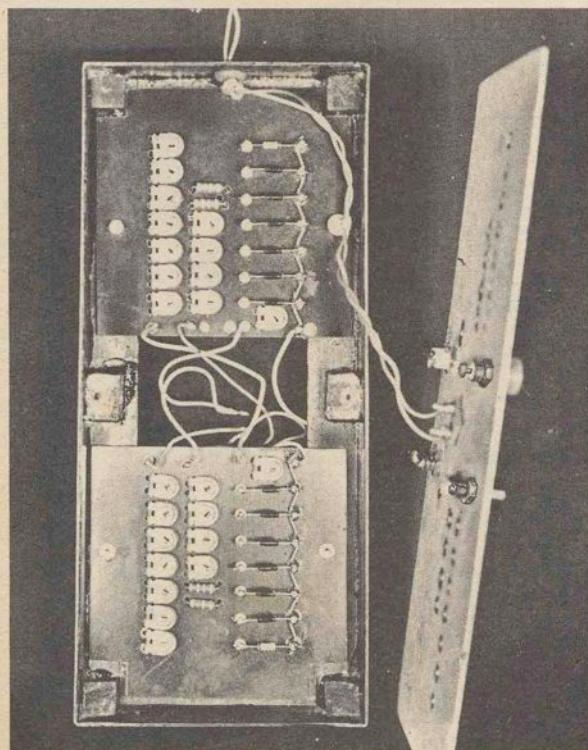
$E_o = E_{in}^3$

$R_t = 100\text{k}\Omega$

$E_o = \frac{E_{in}^3}{10}$

$R_t = 10\text{k}\Omega$

Fig. 8.4. Function generator circuit panels (2 off)



Interior view of UNIT "C" function generator

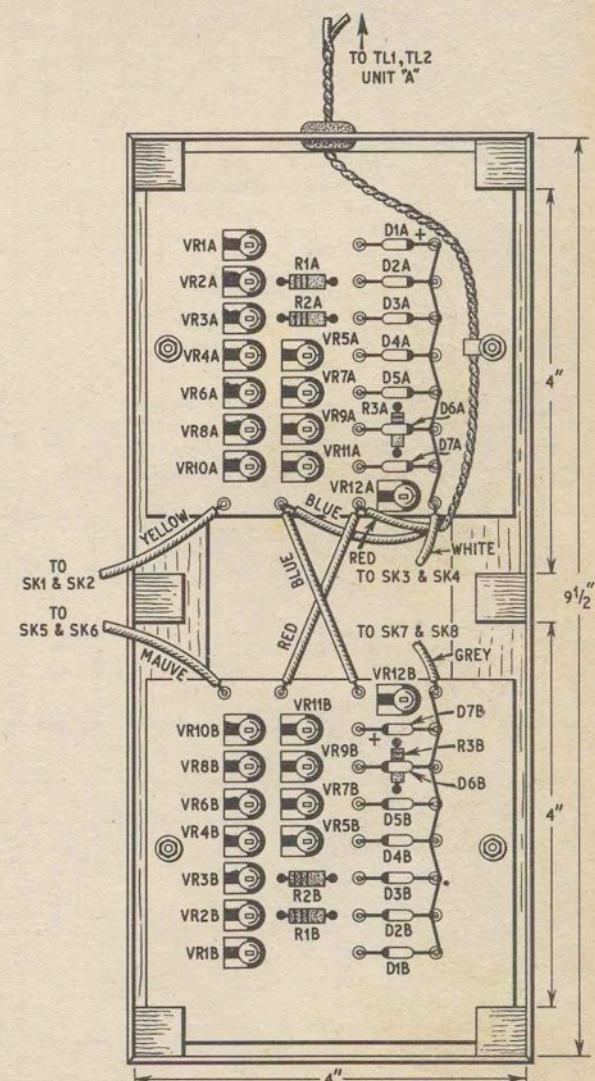


Fig. 8.5. Topside and interconnecting wiring of function generator panels. The circuit boards are shown in position inside the UNIT "C" case

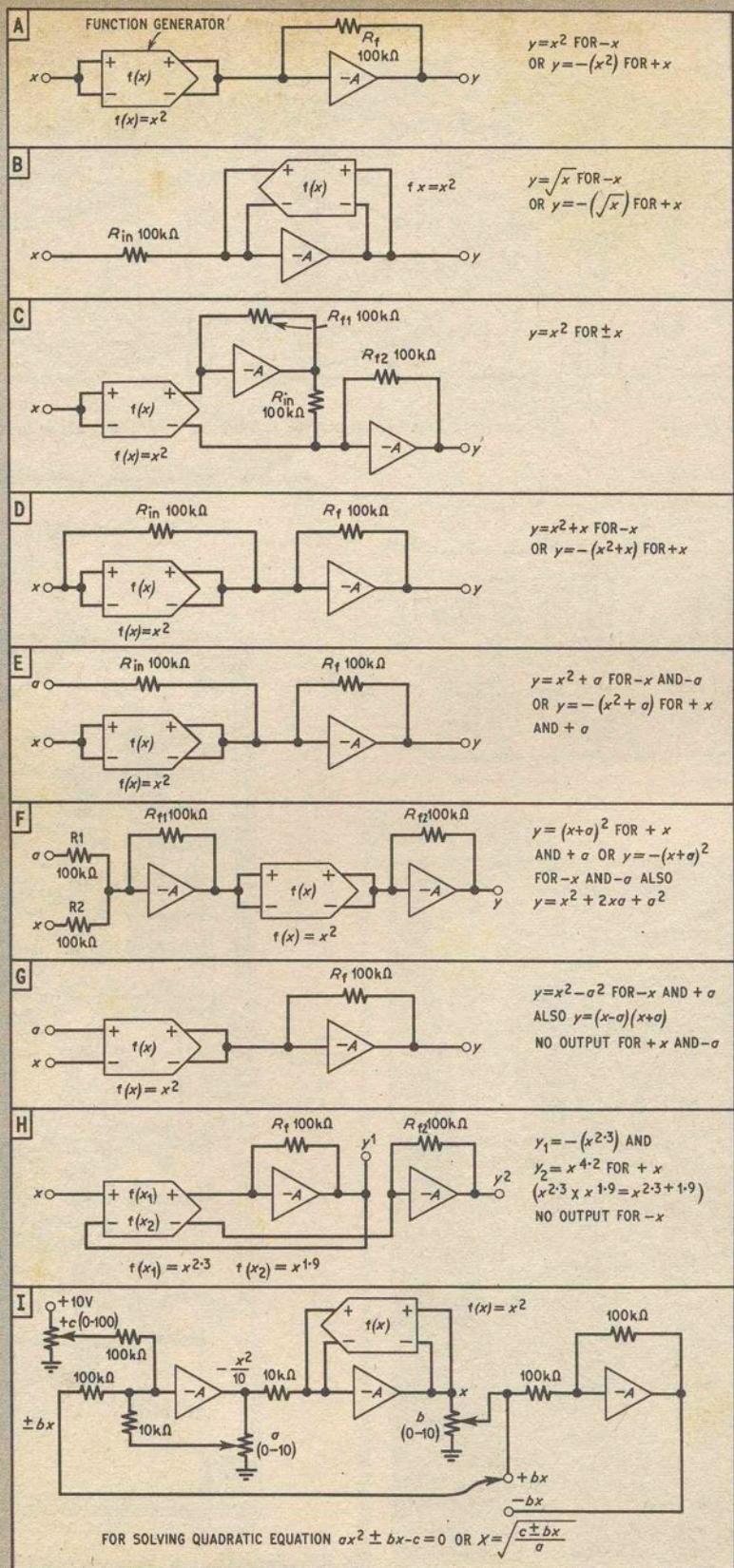
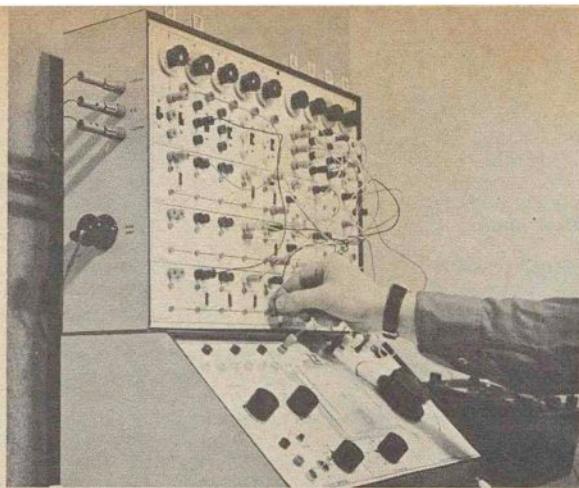


Fig. 8.6. The function generator used for equation solving



This photograph shows PEAC being used to solve simultaneous equations

After the entire range of input voltages listed in Table 8.1 has been covered, return to $E_{in} = -0.2V$ and go through the procedure again, to achieve optimum accuracy. The positive branch can be set up for the same function as the negative branch by transferring patching leads from FG/SK5 to SK1, and FG/SK8 to SK4, but this time trim VR12A for zero-set, and apply positive values of E_{in} . It may be necessary to slightly re-adjust slope controls VR1–VR3 when the two branches are connected in parallel, if there is some small bias voltage imbalance.

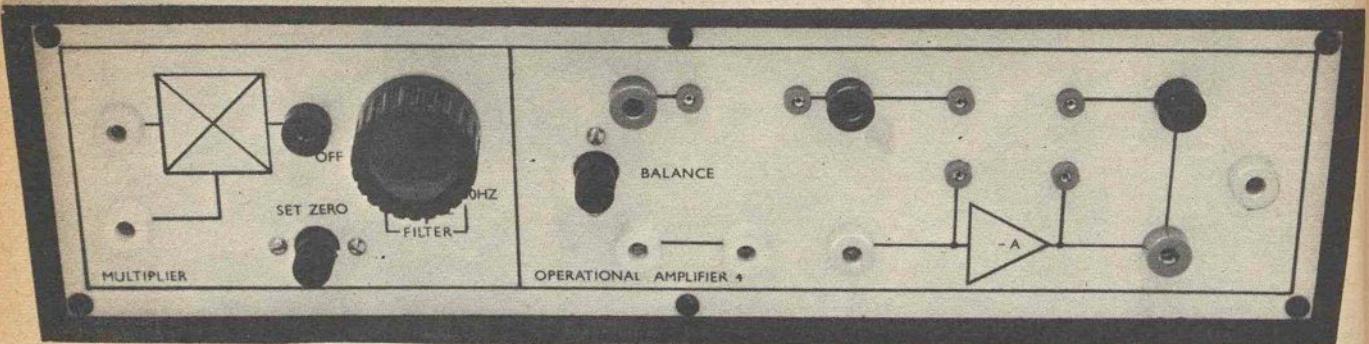
THE FUNCTION GENERATOR IN EQUATION SOLVING

The fact that an analogue computer can produce and handle imaginary numbers will be particularly evident when the function generator is applied to equation solving, see Fig. 8.6. One type of function generator circuit configuration will produce consistent outputs for, say, the cube of a number, but not for its square, or vice versa, because $\pm x^2 = +y$, but $+x^3 = +y$, and $-x^3 = -y$. The computer operator must therefore choose, or devise, the appropriate circuit for a given task.

Output y in Fig. 8.6a will be of the required sign when the input is $-x$, but the sign of y with an input of $+x$ cannot be reconciled with mathematical convention. However, the circuit of Fig. 8.6a does provide a consistent output when the function is x^3 , with inputs of $\pm x$. Much the same applies to the Fig. 8.6b circuit, which shows the function generator arranged for square root operations. Circuit Fig. 8.6c reverses the above situation and gives consistent outputs for a square function, but not for a cube function, by employing an extra sign reversing amplifier.

Getting away now from the complexities of square roots of negative numbers and other mathematical anomalies, Fig. 8.6d can be made to give outputs of $y = x^2 + x$, or some other combination such as $y = x^{2.5} - 3x$, depending on the choice of function, voltage polarities, and computing resistor values. The purpose of other circuits E–H will be self-evident in Fig. 8.6. Fig. 8.6i gives the symbolised layout for solving a quadratic equation, where x is unknown and a , b , and c are constants. The function generator can also be introduced into problem set-ups where integrating amplifiers are used, as its frequency response is well in excess of any frequency likely to be encountered.

Next month: The final item of the PEAC equipment, UNIT "D", will be described.



ANALOGUE PEAC COMPUTER

By D. BOLLEN

THIS month's article deals with UNIT "D"—the multiplier, which is the final piece of PEAC equipment. After a technical description, details of the construction and setting up are given.

The servo driven potentiometer has been widely employed in the past for multiplication of one variable voltage by another, but its frequency response, in most cases, is seldom better than 0-5Hz. Modern analogue computers now tend to use all solid-state multiplier circuits, which have a frequency response extending into the kHz region, but they are both complex and expensive. Taking the quarter-square multiplier as an example, it needs five operational amplifiers and two diode function generators to produce an accurate product voltage from two inputs. It follows, therefore, that analogue multiplier circuit design can be expected to present considerable difficulties when cost is an important consideration.

UNIT "D"—THE MULTIPLIER

Working on the premise that even a multiplier of restricted performance can make a worthwhile contribution to an analogue computer which lacks such a facility, an accuracy of ± 2.5 per cent and a frequency response of 50Hz under the most favourable conditions was considered to be an acceptable specification for the UNIT "D" multiplier. Although 0-50Hz seems rather limited by ordinary electronic standards, in the context of "parallel" computer circuit operation it represents a useful compute time which compares favourably with the servo multiplier.

UNIT "D" contains three distinct circuits, two operational amplifiers and a bistable reed relay driver. One of the amplifiers is identical to those used with UNIT "A", and is available as a multi-purpose operational amplifier when the multiplier is not in service.

TIME DIVISION

With the time division multiplier, a square wave is modulated in such a way that the mark/space ratio is proportional to one input voltage, while the amplitude of the waveform is proportional to another input voltage. The mean value of the resulting waveform is then proportional to the product of the two input voltages.

Looking at Fig. 9.1, which sets out the simplified multiplier circuit with associated waveforms, a voltage E_2 is compared with a fixed voltage E_3 at the input of the integrating amplifier. A bistable relay is arranged to switch S1 and S2 when the integrator output reaches a pre-determined value, conveniently about two thirds of the maximum available amplifier output swing. If the sign of E_3 at the S1 contacts is correct, the feedback will be positive, and a self-sustained oscillation at a frequency determined mainly by E_2 and C_1 will result. When $E_2 = 0$ the output from the integrator will consist of a sawtooth or symmetrical ramp waveform, with identical rising and falling slopes, which is generated by E_3 .

Assume now that a voltage E_2 is applied; this will be added to, or subtracted from E_3 , depending on the position of the S1 switch. The ramp waveform is therefore modified to an asymmetric form where the rising and falling slopes become dependent on the level and sign of E_2 .

Waveform (a) in Fig. 9.1 depicts the asymmetric ramp for $+E_2$ and $-E_2$, while waveform (b) shows the square wave generated by the switch, of mark/space dependent on the magnitude of E_2 . As S2 is synchronised with S1, so the input resistor R1 will be alternately switched to the inverting and non-inverting inputs of the product amplifier, and will remain at each contact for a time dependent on the frequency and mark/space of the switching waveform.

The amplitude of the product amplifier output is

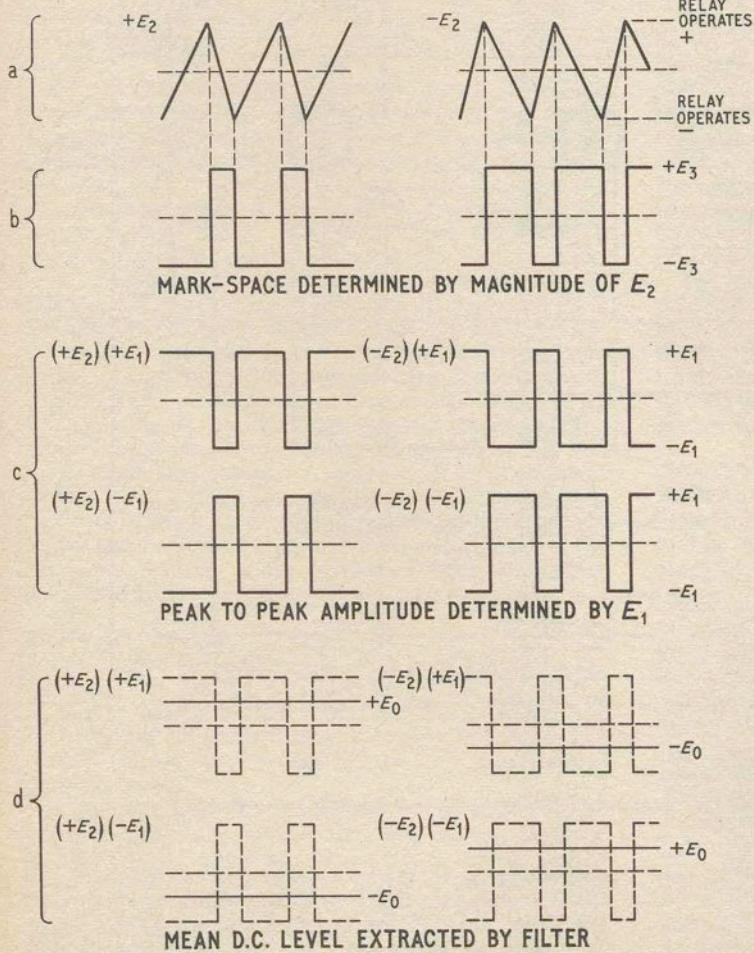
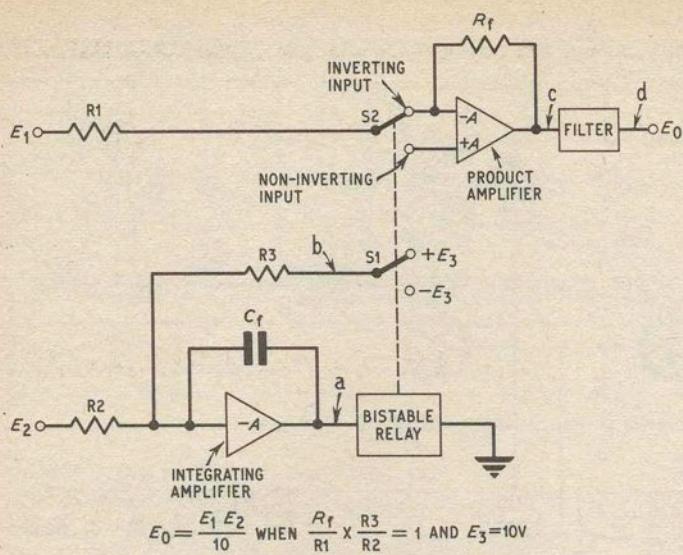


Fig. 9.1. Time division multiplier with associated waveforms

COMPONENTS . . .

UNIT "D" FRONT PANEL AND BOX

Potentiometers

VR25 100 Ω wirewound

VR26 50 Ω wirewound

(both panel mounting type)

Switches

S11 3 pole, 4 way rotary

S12 Double-pole slide switch (c/o contacts)

Sockets

2 red, 2 blue, 1 black, 2 yellow, 3 white,
1 green, and 6 miniature sockets

Miscellaneous

Material for front panel and box. Hardboard,
2 off 12 $\frac{3}{8}$ in \times 4 $\frac{1}{2}$ in, 2 off 4 $\frac{1}{2}$ in \times 3 $\frac{3}{16}$ in.
White plastic laminate, 2 off 12 $\frac{3}{8}$ in \times 4 $\frac{1}{2}$ in,
2 off 3 $\frac{1}{2}$ in \times 4 $\frac{1}{2}$ in, 1 off 12in \times 3 $\frac{1}{8}$ in.
Softwood, 25in \times $\frac{1}{2}$ in \times $\frac{1}{2}$ in. Knob, one
Radiospares 1 $\frac{1}{8}$ in type PK with pointer.

UNIT "D" BISTABLE RELAY AND PRODUCT AMPLIFIER

Resistors

| | | | |
|------|------------------|------|------------------|
| R1 | 1k Ω | *R14 | 10k Ω 1% |
| R2 | 4.3k Ω | R15 | 1k Ω |
| R3 | 4.3k Ω | R16 | 820 Ω |
| R4 | 4.3k Ω | R17 | 820 Ω |
| R5 | 1k Ω | R18 | 1k Ω |
| R6 | 100 Ω | R19 | 8.2k Ω |
| *R7 | 11k Ω 1% | R20 | 22k Ω |
| R8 | 10k Ω | R21 | 22k Ω |
| R9 | 27k Ω | R22 | 8.2k Ω |
| R10 | 2.2k Ω | *R23 | 200 Ω 2% |
| R11 | 100 Ω | *R24 | 1k Ω 2% |
| *R12 | 10k Ω 1% | *R25 | 1.2k Ω 1% |
| *R13 | 9.1k Ω 1% | *R26 | 300 Ω 1% |

(All 10% $\frac{1}{2}$ watt carbon composition except

* = 1W metal oxide)

Potentiometers

VR1 100k Ω vertical skeleton pre-set

VR2 220 Ω miniature horizontal pre-set

Capacitors

C1 1 μ F polyester 250V d.c.

C2 0.25 μ F polyester 250V d.c.

C3 1 μ F elect. 15V

C4 8 μ F elect. 15V

C5 100 μ F elect. 15V

Transistors

TR1, TR2 2N2926 (orange) or 2N3904 (2 off)

TR3 2N3906

TR4 2N3904

TR5, TR6 ACY28 or AC126 (2 off)

Diodes

D1-D4 OA202 (4 off)

Choke

L1 5H (Radiospares "Midget" type)

Reed coils

RLA, RLB Miniature triple 12V

Osmor type MT12V (2 off)

Reed switches

RLA1, RLA2 Hamlin MRG2 20-40AT (4 off)

RLB1, RLB2

Miscellaneous

S.R.B.P., 1 off 3in \times 3 $\frac{1}{2}$ in, 1 off 3in \times 4 $\frac{1}{2}$ in.

Small turret tags. Baseboard 12 in \times 4in s.r.b.p. or plastic laminate

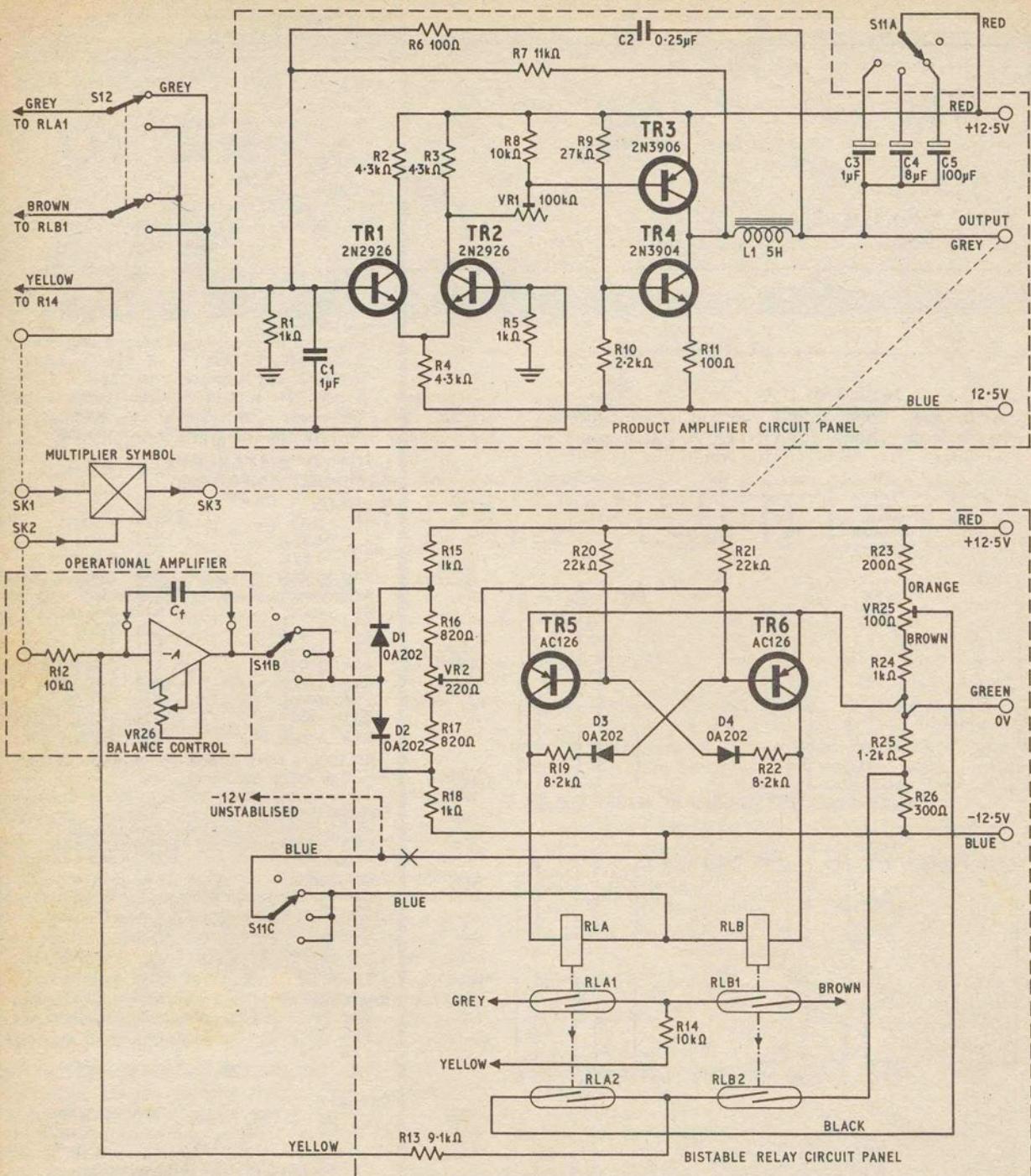


Fig. 9.2. Multiplier circuit, comprising product amplifier panel and bistable relay panel

wholly dependent on E_1 , but whatever the value of E_1 it will be divided by $10/E_2$ (time division), which is the same thing as $(E_1 \times E_2)/10$, assuming of course that appropriate values for R1-R3, R_f and E_3 are chosen.

Waveforms (c) shows what happens to different signs of E_1 and E_2 , in terms of the square wave. If now the mean voltage level of the output from the product

amplifier is extracted by a suitable filter (see waveform (d)) it can be seen that four quadrant multiplication has been achieved. When E_1 and E_2 are both positive, or both negative, the product voltage will be positive, but when E_1 and E_2 are of opposite sign, the product becomes negative.

The multiplier circuit will now be described.

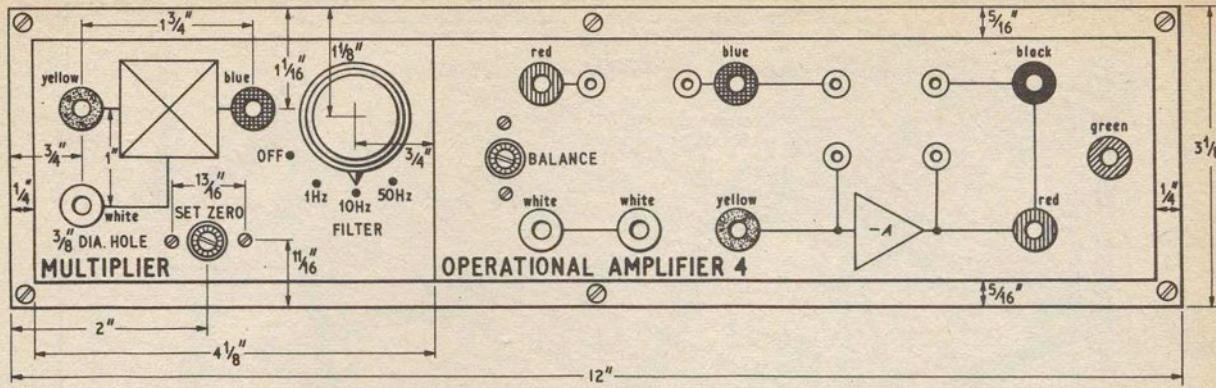


Fig. 9.3. Dimensions and engraving details for UNIT “D” front panel

UNIT “D” MULTIPLIER CIRCUIT

As the operational amplifier circuit has already been given in connection with UNIT “A”, it appears in symbolised form only in the multiplier circuit of Fig. 9.2, with VR26 as the front panel balance control, and a fixed value of input resistor R12 provided internally for use with the multiplier. As the feedback capacitor C_f only affects the integrator waveform frequency, without altering other multiplier characteristics, it is useful to leave it as a plug-in component, so that the multiplier carrier frequency can be adjusted easily.

The output from the integrator, which it will be remembered from Fig. 9.1 carries information as to the magnitude and sign of input E_2 , is fed via S11B to a diode resistor network composed of D1, D2, R15-R18, and VR2, the purpose of which is to allow the following bistable relay driver to be switched at precisely determined voltage levels. VR2 establishes the working point of the diode resistor network.

A conventional cross-coupled multivibrator is utilised as a relay driver, with reed coils RLA and RLB forming the respective collector loads of TR5 and TR6. D3 and D4 are used to ensure a “cleaner” switching action at high repetition rates, and the bistable circuit will function satisfactorily at frequencies in excess of 100Hz without undue relay contact bounce. The reference voltage, which was shown as $\pm E_3$ in Fig. 9.1, is extracted from a resistor network R23-R26 and VR25 in Fig. 9.2. VR25 allows positive and negative values of E_3 to be made equal. E_3 voltages are then fed, via RLA2 and RLB2 switches, and resistor R13, back to the summing junction of the integrator, thus completing the closed-loop to maintain oscillation.

SIGN CHANGE

The square wave switching cycle is presented to the input of the product amplifier by RLA1 and RLB1, with R14 acting as the input resistor. Changeover switch S12 is included to allow the sign of the multiplier output voltage to be changed to suit a particular problem set-up.

A product amplifier open-loop gain of about 1,000, which is the gain of the Fig. 9.2 circuit, is quite satisfactory for good accuracy when working with a fixed, closed-loop gain close to unity. Long-tailed pair TR1 and TR2 provide inverting and non-inverting inputs, while TR3 is the output transistor, and TR4 forms a constant current load for TR3, in place of a fixed resistor, thus enabling larger loads to be driven without excessive dissipation. VR1 serves to zero the amplifier output.

The ratio of resistors R7 and R14 gives a product amplifier gain (closed-loop) of 1·1, while R13/R12 yields an equivalent gain for the integrating amplifier of 0·91. The lower value of gain for the integrator enables E_2 to equal E_3 without stopping the integration cycle, and yet the overall gain of the multiplier is still unity because $1\cdot1 \times 0\cdot91 = 1$.

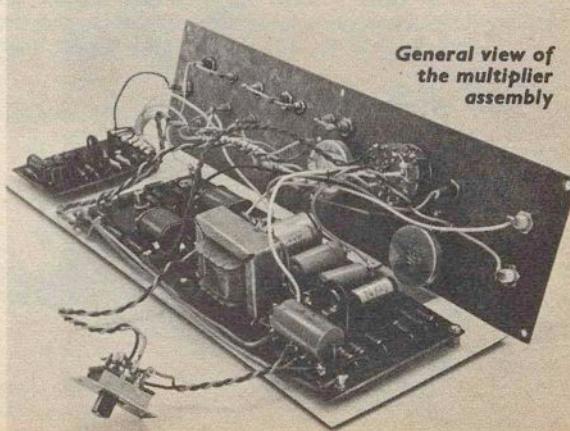
FILTER CIRCUIT

The purpose of the filter circuit L1, C2-C5, R6, and S11A, is to remove the square wave carrier without distorting the product waveform when input voltages are time varying. Bearing in mind that computer waveforms are extremely diverse, it is almost impossible to achieve near perfect results with one filter circuit, especially when the carrier frequency is not far removed from input frequencies. To allow compromise, therefore, the cut-off frequency of the Fig. 9.2 filter can be set by switch S11A to suit the circumstances of a particular problem set-up.

The three switch positions, 1Hz, 10Hz, and 50Hz, represent approximately the roll-off points given by the filter, and the bandwidth handled by the multiplier. In the 1Hz position the filter will virtually eliminate carrier ripple when input voltages are of very low frequency, but the 50Hz setting is used with fast integrator waveform inputs, where ripple may be less objectionable.

CONSTRUCTION OF UNIT “D” FRONT PANEL AND BOX

Details of the UNIT “D” front panel and box appear in Fig. 9.3 and Fig. 9.4. Note that the operational amplifier (OA4) socket positions and panel markings



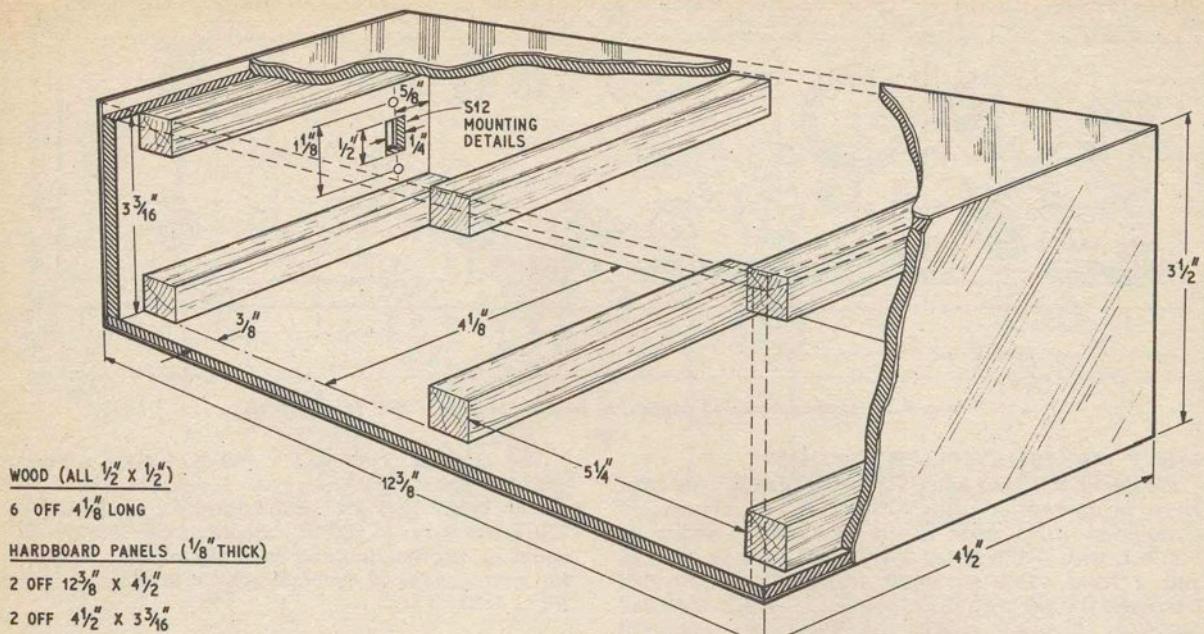


Fig. 9.4. Construction of the box for UNIT "D"

are the same as for UNIT "A" operational amplifiers. S11, VR25, VR26, and all sockets may be mounted after the front panel has been marked and drilled.

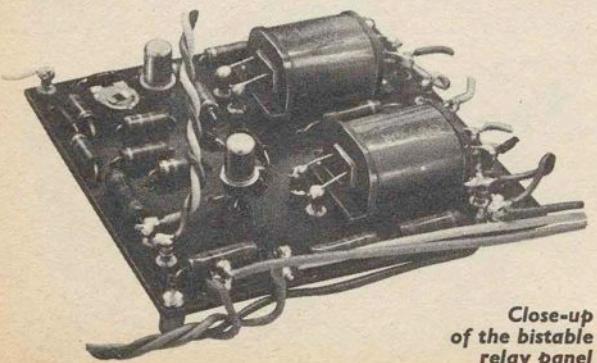
INTERNAL LAYOUT OF THE MULTIPLIER

The internal layout and interconnecting wiring of the multiplier are shown in Fig. 9.5. Operational amplifier, bistable relay driver, and product amplifier circuit panels are bolted with stand-off spacers to a $12\text{in} \times 4\text{in}$ s.r.b.p. or plastics laminate baseboard, which rests on the wooden bearers at the base of the UNIT "D" box.

Component placement positions for the bistable relay circuit panel, and the product amplifier panel, also appear in Fig. 9.5, together with a rear view of the front panel assembly. The operational amplifier (OA4) is made up in accordance with instructions given in the May issue of PRACTICAL ELECTRONICS (pages 209-210).

BISTABLE RELAY CIRCUIT CONSTRUCTION

Drill the bistable relay circuit panel according to Fig. 9.6, and insert turret tags. Then mount all components and complete underside wiring, leaving the reed switches RLA1, RLA2, RLB1, and RLB2 until



last. A triple reed coil is specified for the Fig. 9.2 circuit, to allow the addition of an extra pair of reed switches if the multiplier is to be enlarged to cater for three input voltages; this modification will, of course, also involve the construction of another product amplifier.

PRODUCT AMPLIFIER CIRCUIT CONSTRUCTION

Drilling details and underside wiring of the product amplifier panel appear in Fig. 9.7. Accurate matching of input transistors TR1 and TR2 may not be necessary with this low gain circuit. A 2N2926 transistor should not be employed in the TR4 position, in place of the 2N3904, as its maximum V_{ce} will be exceeded.

After inserting turret tags, mount resistors and transistors first, then follow with L1, and capacitors C2-C5. C1 is soldered into position last of all, across the amplifier input turret tags, as shown in Fig. 9.5.

FINAL ASSEMBLY AND SETTING UP OF UNIT "D"

Mount the three circuit panels on the baseboard and complete all interconnecting wiring between the circuit panels and the front panel, including S12 which can be left floating for the time being. The resulting assembly can be set-up and tested out of its box.

Connect red, green, and blue flexible wires from the bistable relay panel to the UNIT "A" power supply solder tags, or alternatively to TL1, TL2, and TL3 with stackable plugs.

Place S11 in the "off" position and zero-set the operational amplifier (OA4) following instructions given earlier for UNIT "A" amplifiers, after allowing the usual warm-up period. When adjusting the VR26 balance control connect M/SK2 to any earth socket with a patching lead. Next, attach a sensitive d.c. voltmeter (0-1V) to M/SK3 and zero-set the multiplier output by adjustment of VR1 on the product amplifier circuit panel.

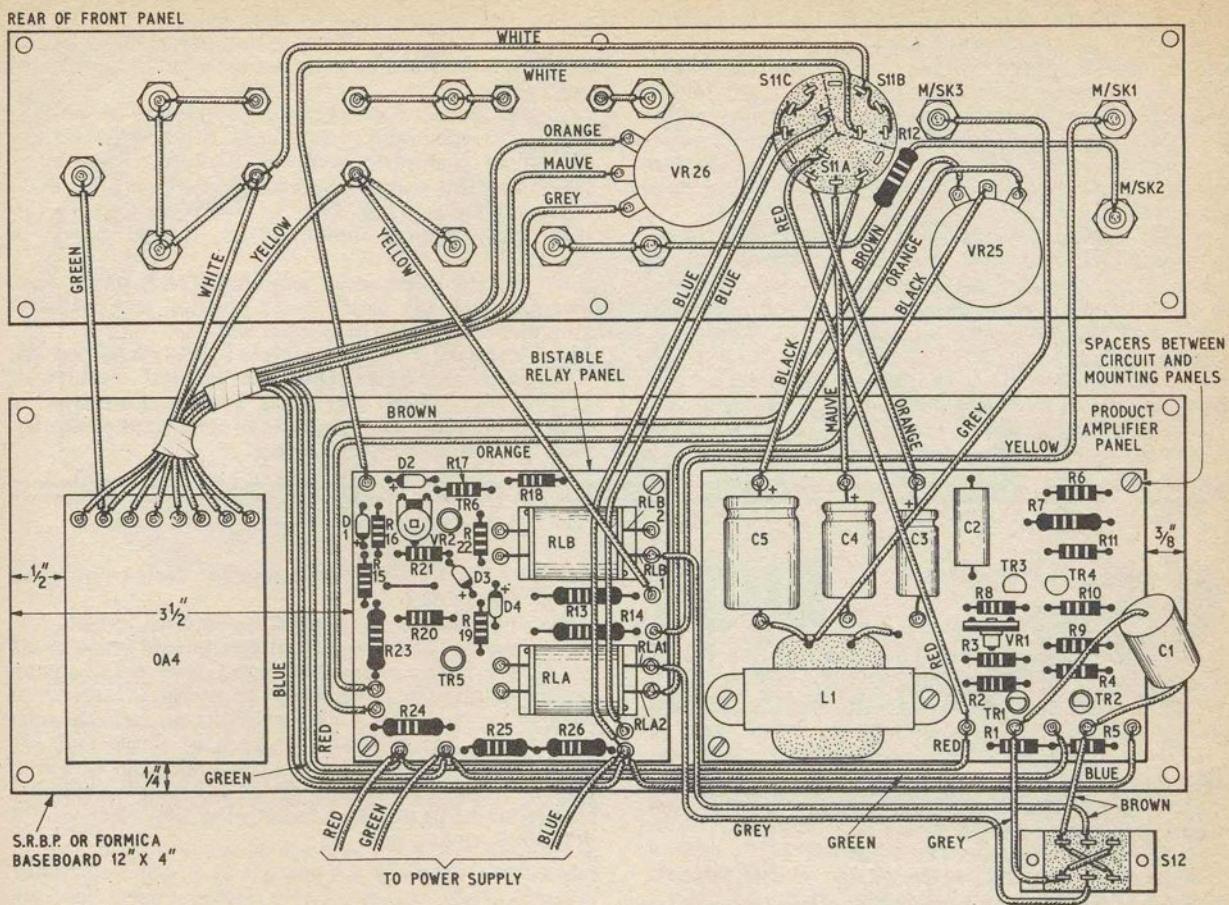


Fig. 9.5. Internal layout and wiring of UNIT “D” multiplier

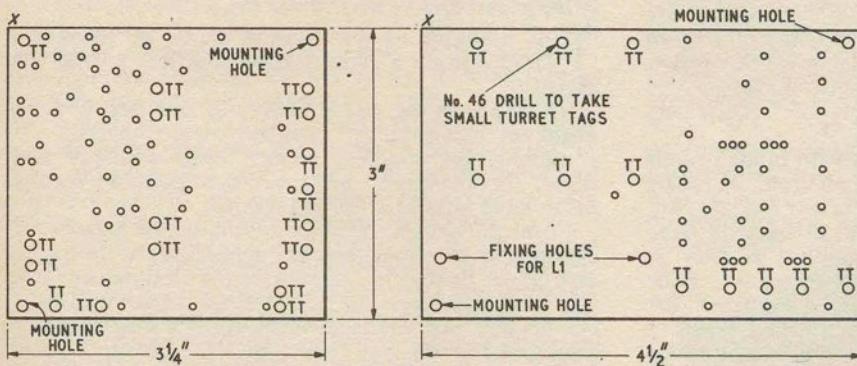


Fig. 9.6 (far left). Top and underside views of bistable relay panel

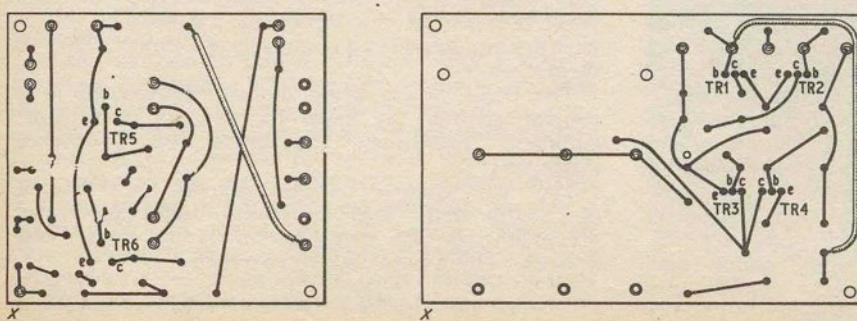


Fig. 9.7 (left). Top and underside views of product amplifier circuit panel

Insert a $0.25\mu\text{F}$ capacitor into OA4/SK11 and SK12, and switch S11 to 10Hz. A "buzz" from the relays should now be heard, which may or may not sound erratic. Transfer the d.c. voltmeter to OA4 output while the relays are still working and adjust VR2 on the bistable relay panel for zero volts; this should produce an even note from the relays. Return the voltmeter lead to the multiplier output M/SK3 and this time zero-set with VR25.

Apply an input of +5V to M/SK2; the relay "buzz" will drop in frequency, but no output should be observed at M/SK3. Transfer the +5V patching lead to M/SK1 and again no output should be seen. Finally, apply +5V to both inputs, M/SK1 and SK2, to produce a multiplier output of $5^2/10$ or 2.5V.

Throw switch S12 to change output polarity and experiment with inputs of differing sign. If all is well, the product voltage should retain its value of 2.5 for any sign combination of input voltages and S12.

For best accuracy it is advisable to go over all adjustments again to obtain optimum settings, and also verify that the multiplier will handle a full range of input voltages.

Due to the fact that the power supply may be working close to its maximum current limit, there could be some fall-off in multiplier accuracy because of switching transients, this can be checked by employing the extra current facility, S1 in Fig. 3.1. The optional -12V relay power supply should obviate the difficulty if it occurs.

To use the operational amplifier (OA4) on its own, merely switch S11 to the "off" position and patch the amplifier sockets in the normal way.

Next month: The final article in the PEAC series. This will complete the operational details of UNIT "D", and will give some examples of special circuits to represent mechanical phenomena, and some general notes.

We now consider the use of the multiplier UNIT "D" in solving equations.

THE MULTIPLIER IN EQUATION SOLVING

Fig. 10.1 sets out four multiplier configurations to show how equation terms may be handled. As a self-contained computing element, UNIT "D" will multiply input voltages X and Y to give a product $XY/10$, see Fig. 10.1a. Note that arrows are normally used with the multiplier symbol to identify input and output terminals.

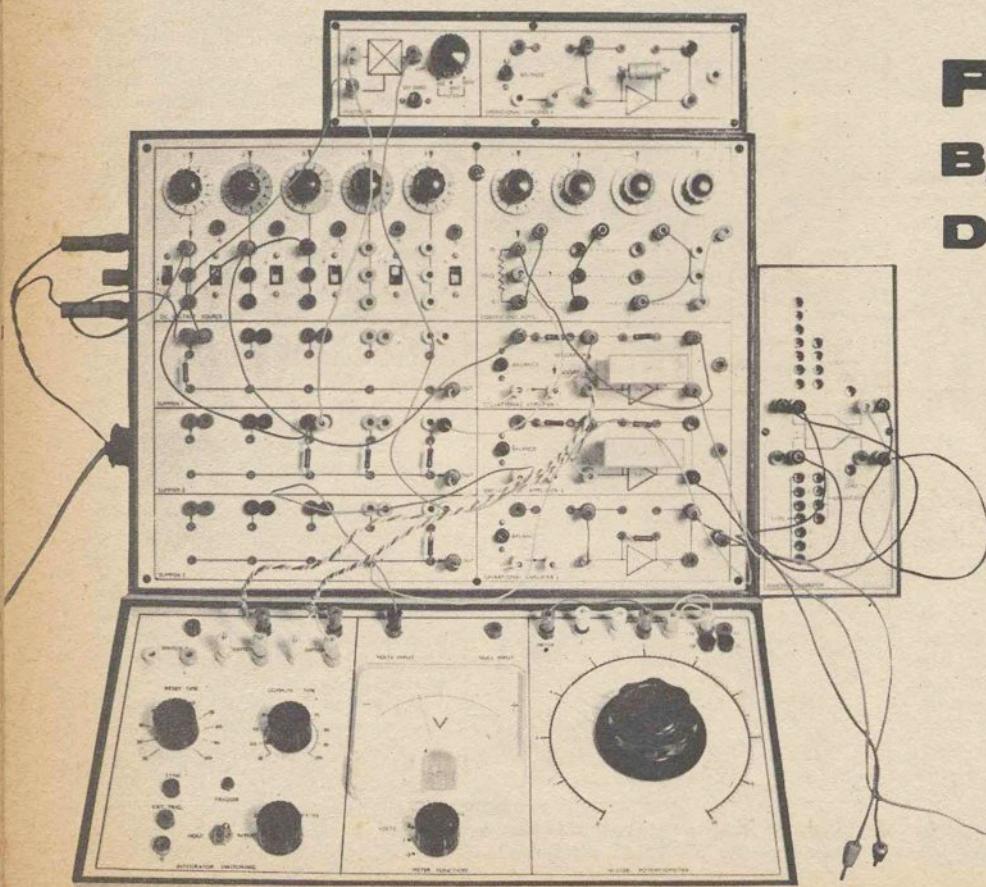
Division of two variable voltages is achieved, in Fig. 10.1b, by placing the multiplier in the feedback loop of an operational amplifier. However, with division, certain limitations are imposed. The Y input must be of single polarity, which rules out a.c. waveforms unless they are d.c. biased above or below $Y = 0$, but ramp or step functions will be accepted if they do not change

their sign. With the X input, voltages can be 0 to $\pm 10V$ d.c., or a.c. peak.

Because an extra filter capacitor (shown dotted in Fig. 10.1b) is needed to prevent amplification of low-level carrier ripple by the open-loop, high gain amplifier, frequency response is restricted to 10Hz for the division operation, when switch S11 is in the 50Hz position. It is sometimes possible to arrange a problem so that the reciprocal is multiplied, and thus avoid the limitations of Fig. 10.1b division. A related configuration in Fig. 10.1c gives an output $XY/(1 + X)$, for inputs of $\pm X$ and $\pm Y$.

In the final example of Fig. 10.1d, the multiplier is combined with integrators, and therefore handles time varying voltages. By solving the equation $dA/dt = 2\pi R \times dR/dt$, which describes the rate at which the area of a circle changes with a growth of radius, the layout of Fig. 10.1d can be used to investigate,

ANALOGUE COMPUTER



PEAC
By
D.BOLLEN

The Practical Electronics Analogue Computer in its complete and comprehensive form. The whole of this equipment has been fully described in this series of articles which is concluded this month

say, the build-up of tape on a spool, the expansion or contraction of metal discs and cylinders when heated, or the surface area of a liquid in a conical reservoir.

SPECIAL ANALOGUE COMPUTER CIRCUITS

Apart from the analogue computing elements already covered are a few specialised diode circuits which are used for simulating various mechanical phenomena. Ordinary silicon diodes, such as the OA202, can be employed with the circuits of Fig. 10.2, and are inserted into the computing component sockets of UNIT "A".

Dead Zone. Amplifier gain in Fig. 10.2a is zero until the limits

$$E_{in} = -\frac{R_1}{RB_1} \times 10$$

or

$$E_{in} = \frac{R_2}{RB_2} \times 10$$

are reached, thereafter gain will depend on the slope given by R_t/R_1 and R_f/R_2 .

Limiter. In Fig. 10.2b, amplifier gain is constant between the limits set by

$$E_o = \frac{R_1}{RB_1} \times 10$$

and

$$E_o = -\frac{R_2}{RB_2} \times 10$$

When the limits are exceeded, the gain falls to zero.

Friction. A frictional force generated by moving surfaces in contact is virtually constant for all values of

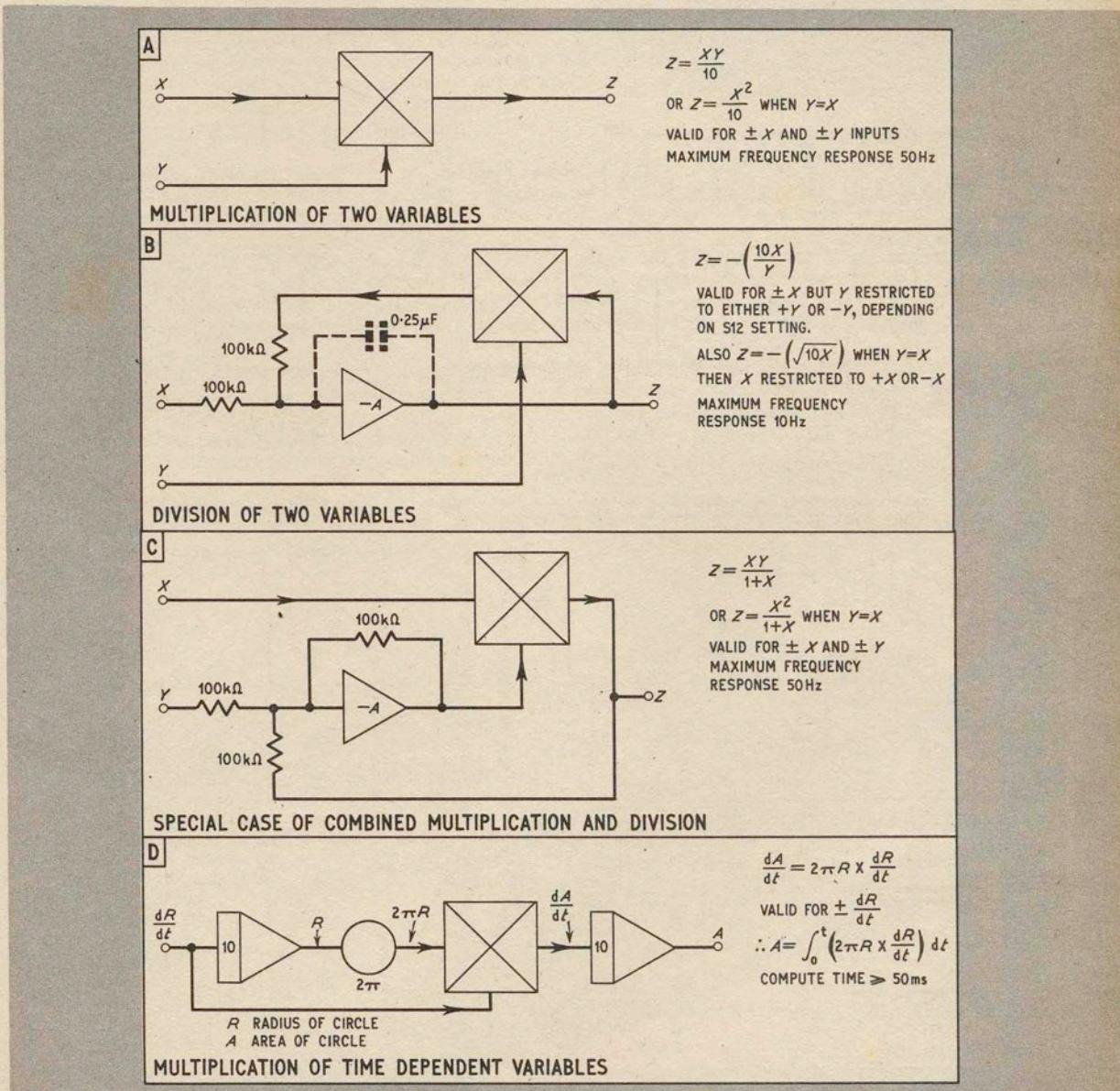


Fig. 10.1. The multiplier used for equation solving

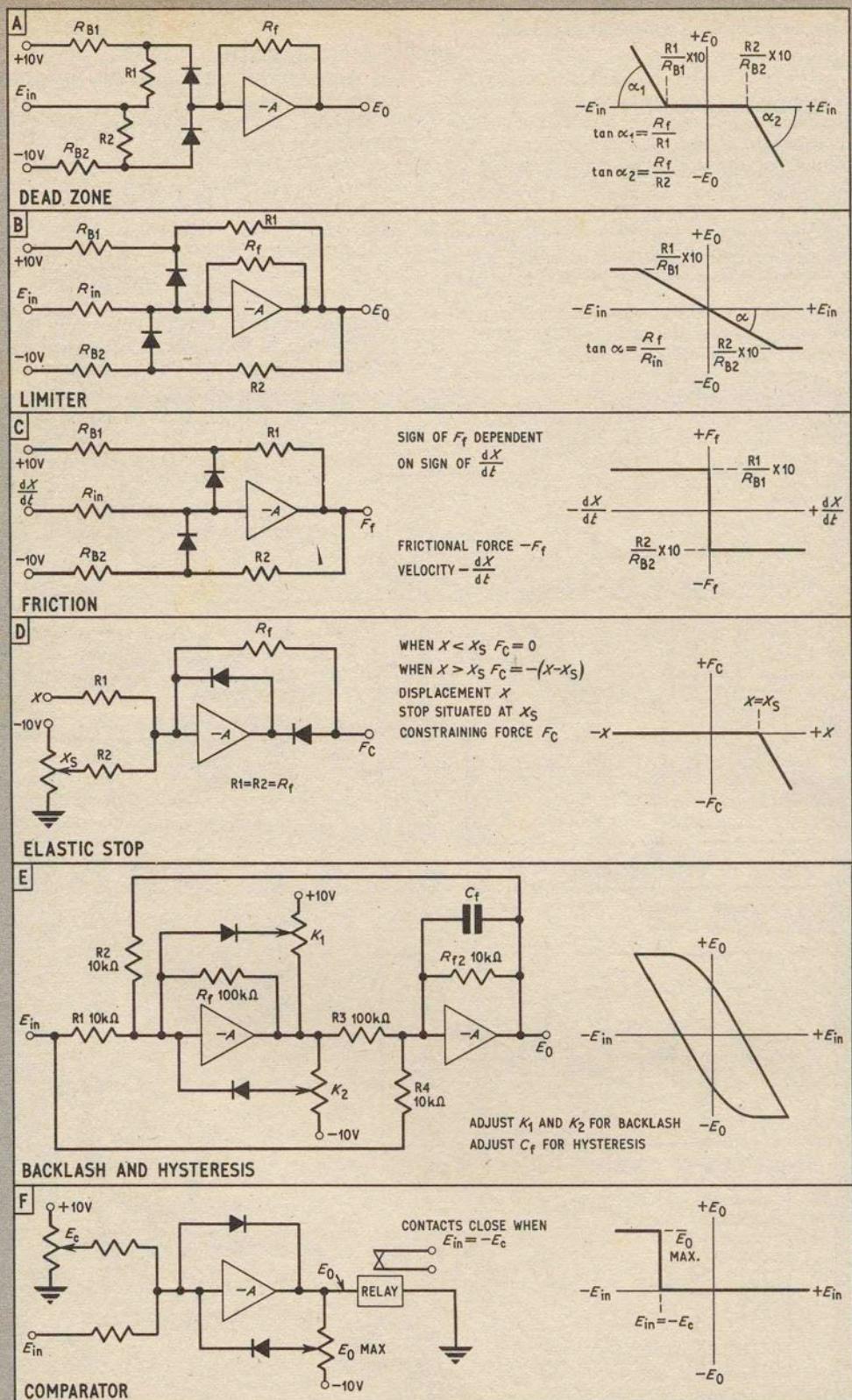


Fig. 10.2. Special circuits for simulating mechanical phenomena

velocity, but will change sign when the direction of the velocity is reversed. Circuit Fig. 10.2c satisfies the above conditions and generates a voltage proportional to a frictional force F_f .

Elastic stop. When an object makes contact with an elastic stop, the resulting constraining force is proportional to the penetration of the object into the stop. In Fig. 10.2d, term X_s represents the position of the elastic stop, while X is the displacement of the object. When $X \geq X_s$, the amplifier provides an output F_c which represents the constraining force.

Backlash and hysteresis. Mechanical linkages, gear trains, and some electrical circuits will often exhibit backlash and hysteresis, which are simulated by the circuit of Fig. 10.2e, using a dead zone and an integrator. Apart from K_1 , K_2 , and C_1 , adjustments to R_2 , R_3 , and R_4 will allow a wide range of characteristics.

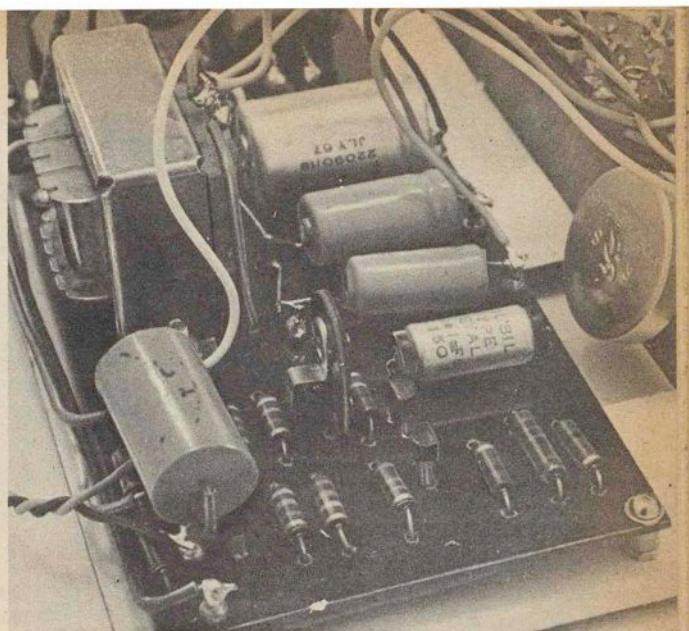
Comparator. As its name suggests, the comparator of Fig. 10.2f compares one voltage with another, and enables some action to be taken at a pre-arranged input level. The comparator can be applied to the simulation of impact forces, where the constraining force is proportional to the rate of penetration; when $E_{in} = -E_c$, the relay contacts will close and insert a voltage representing velocity into an equation.

CONCLUDING NOTES

A brief mention should be made of those aspects of analogue computer usage which were considered to be beyond the scope of the present series. It would have been difficult to include the more complex Calculus problems which PEAC is capable of solving, and also transfer function techniques were avoided because they would have demanded some knowledge of Laplace transforms and the like.

A very important field is the use of analogue computers in controlling processes and evaluating data, so called "In-plant" applications, but here fairly elaborate sensing equipment and servomechanisms are called for, to act as intermediaries between the external process and the computer.

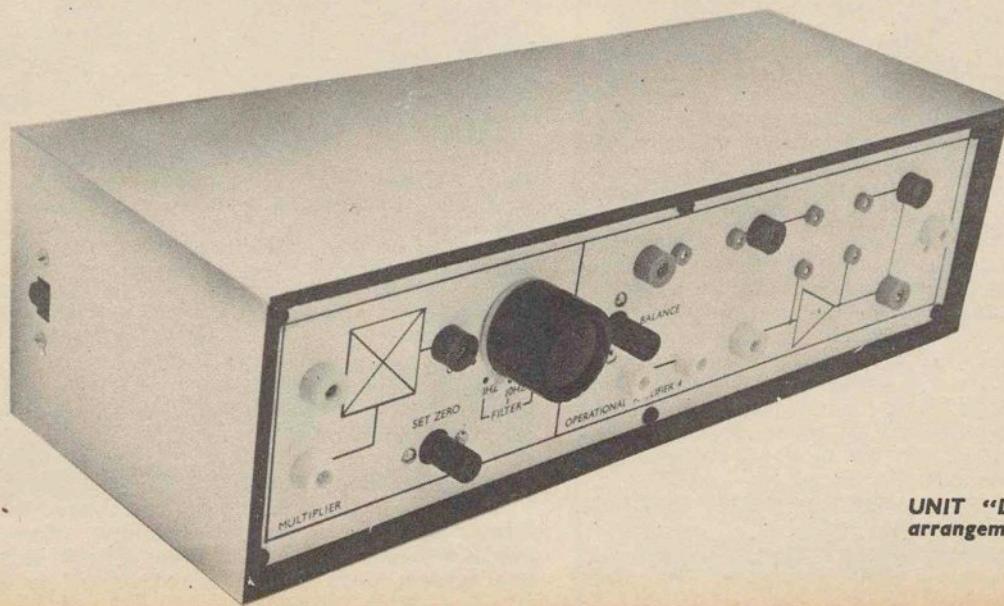
An important omission, brought to light by a reader's letter, concerns the use of a temporary feedback resistor when checking the coefficient of a potentiometer



Product amplifier circuit panel

which is employed for division (Fig. 4.1f). If the feedback resistor is not present, the operational amplifier summing junction will no longer be at virtual earth when the potentiometer is disconnected for measurement purposes, and this can lead to serious errors. Therefore, when checking a division potentiometer coefficient, always insert a 10 kilohm feedback resistor into OA/SK11 and SK12.

If difficulty is experienced in zero-setting a UNIT "A" operational amplifier after construction, by adjustment of VR1 on the amplifier panel, it may be that transistor "spreads" are greater than has been allowed for in the design. The simple cure is to increase R1 (Fig. 3.7) to 4.7 megohm if the amplifier output is fixed close to the negative supply rail voltage, or, when the output remains clamped near to the positive rail, decrease R1 to 3.3 megohm. ★



UNIT "D" front panel arrangement and cabinet