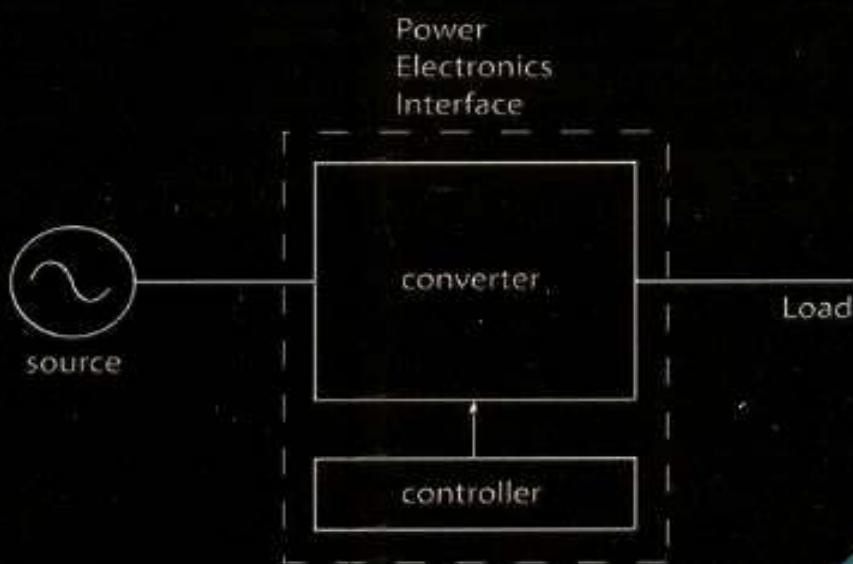


FIRST COURSE ON

Year 2003 Edition

POWER ELECTRONICS AND DRIVES



MNPERE

NED MOHAN

First Course on

POWER ELECTRONICS

AND DRIVES

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To my wife Mary, son Michael and daughter Tara

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PREFACE

Power electronics and drives are enabling technologies but most undergraduates, at best, will take only one course in these subjects. Recognizing this reality, this book is intended to teach students both the fundamentals in the context of exciting new applications and the practical design to meet the following objectives simultaneously:

- Provide solid background in fundamentals to prepare students for advanced courses
- Teach design fundamentals so that students can be productive in industry from the very beginning

In this book, the topics listed below are carefully sequenced to maintain student interest throughout the course and to maintain continuity as much as possible.

1. Applications and Structure of Switch-Mode Power Electronics Systems
2. Practical Details of Implementing a Switching Power-Pole (the building block)
3. DC-DC Converters: Switching Details and their Average Dynamic Models
4. Designing the Feedback Controller in DC-DC Converters
5. Diode Rectifiers and their Design
6. Power-Factor-Correction Circuits (PFCs) including the Controller Design
7. Review of Magnetic Concepts
8. Transformer-Isolated Switch-Mode DC Power Supplies
9. Design of High-Frequency Inductors and Transformers
10. Soft-Switching in DC-DC Converters, and its applications in High-Frequency AC Synthesis in Induction Heating and Compact Fluorescent Lamps (CFLs)
11. Electric Motor Drives
12. Synthesis of DC and Low-Frequency Sinusoidal AC in Motor Drives and Uninterruptible Power Supplies (UPS)
13. Control of Electric Drives and UPS
14. Thyristor Converters
15. Utility Applications of Power Electronics

Instructor's Choice

In a fast pace course with proper student background, this book with all these topics can be covered from front-to-back in one semester. However, the material is arranged in such

a way that an instructor can either omit an entire topic or cover it quickly to provide just an overview using the PowerPoint-based slides on the accompanying CD, without interrupting the flow.

This book is designed to serve as a semester-course textbook in two different curricula: 1) in a Power Electronics course where there is a separate undergraduate course offered on electric machines and drives, and 2) in a Power Electronics and Drives course where only a single course is offered on both of these subjects. The selections of chapters under these two circumstances are suggested below.

Textbook in a Power Electronics Course. In this course, since a separate undergraduate course exists on electric machines and drives, Chapter 11 on Electric Motor Drives and Chapter 13 on Design of Feedback Controllers in Motor Drives can be omitted. Depending on the availability of time, the “deeper” chapters such as Chapter 6 on Power Factor Control, Chapter 9 on Design of High-Frequency Inductors and Transformers, and Chapter 10 on Soft-Switching Converters can be covered very quickly, mainly to provide an overview.

Textbook in a Power Electronics and Drives Course. Since this course is intended to provide a broader coverage in a single semester by covering topics in power electronics as well in electric drives, some of the “deeper” chapters in power electronics listed earlier can be safely omitted.

Simulations

In Power Electronics, simulations using PSpice can be extremely beneficial for reaffirming the fundamentals and in describing the design details by making realistic problems. However, simulations are presented on the accompanying CD-ROM such that not to get in the way of the fundamentals.

CD-ROM

The accompanying CD includes the following:

- Extremely useful for Instructors: PowerPoint-based slides are included for every chapter to quickly prepare lectures and to review the material in class. Students can print all the slides and bring to the classroom to take notes on.
- Simulations and design examples are ready-to-execute, using PSpice that is loaded on this accompanying CD-ROM.

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Chapter 1

POWER ELECTRONICS AND DRIVES: ENABLING TECHNOLOGIES

1-1 INTRODUCTION TO POWER ELECTRONICS AND DRIVES

Power electronics is an enabling technology, providing the needed interface between the electrical source and the electrical load, as depicted in Fig. 1-1 [1]. The electrical source and the electrical load can, and often do, differ in frequency, voltage amplitudes and the number of phases. The power electronics interface facilitates the transfer of power from the source to the load by converting voltages and currents from one form to another, in which it is possible for the source and load to reverse roles. The controller shown in Fig. 1-1 allows management of the power transfer process in which the conversion of voltages and currents should be achieved with as high energy-efficiency and high power density as possible. Adjustable-speed electric drives represent an important application of power electronics.

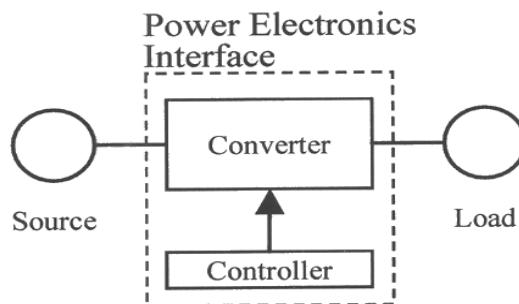


Figure 1-1 Power electronics interface between the source and the load.

1-2 APPLICATIONS AND THE ROLE OF POWER ELECTRONICS AND DRIVES

Power electronics and drives encompass a wide array of applications. A few important applications and their role are described below.

1-2-1 Powering the Information Technology

Most of the consumer electronics equipment such as personal computers (PCs) and entertainment systems supplied from the utility mains internally need very low dc voltages. They, therefore, require power electronics in the form of switch-mode dc power supplies for converting the input line voltage into a regulated low dc voltage, as shown in Fig. 1-2a. Fig. 1-2b shows the distributed architecture typically used in computers in which the incoming ac voltage from the utility is converted into dc voltage, for example,

at 24 V. This semi-regulated voltage is distributed within the computer where on-board power supplies in logic-level printed circuit boards convert this 24 V dc input voltage to a lower voltage, for example 5 V dc, which is very tightly regulated. Very large scale integration and higher logic circuitry speed require operating voltages much lower than 5 V, hence 3.3 V, 1 V, and eventually, 0.5 V levels would be needed.

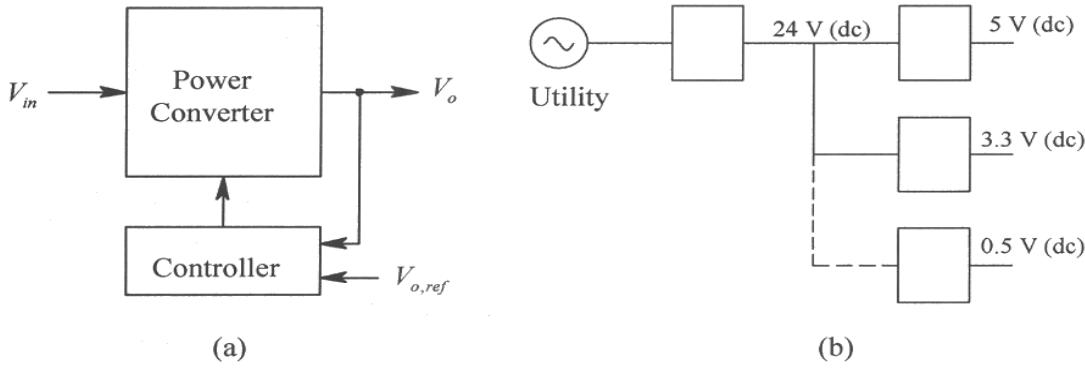


Figure 1-2 Regulated low-voltage dc power supplies.

Many devices such as cell phones operate from low battery voltages with one or two battery cells as inputs. However, the electronic circuitry within them requires higher voltages thus necessitating a circuit to boost input dc to a higher dc voltage as shown in the block diagram of Fig. 1-3.

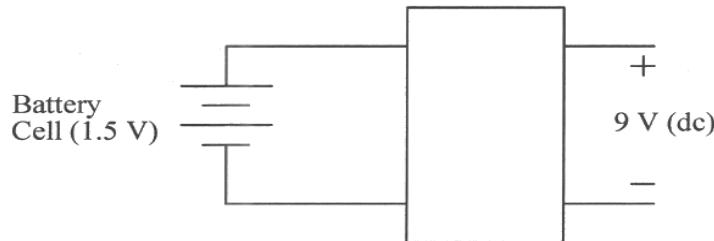


Figure 1-3 Boost dc-dc converter needed in cell operated equipment.

1-2-2 Robotics and Flexible Production

Robotics and flexible production are now essential to industrial competitiveness in a global economy. These applications require adjustable speed drives for precise speed and position control. Fig. 1-4 shows the block diagram of adjustable speed drives in which the ac input from a 1-phase or a 3-phase utility source is at the line frequency of 50 or 60 Hz. The role of the power electronics interface, as a power-processing unit, is to provide the required voltage to the motor. In the case of a dc motor, dc voltage is supplied with adjustable magnitude that controls the motor speed. In case of an ac motor, the power electronics interface provides sinusoidal ac voltages with adjustable amplitude and frequency to control the motor speed. In certain cases, the power electronics interface

may be required to allow bi-directional power flow through it, between the utility and the motor-load.

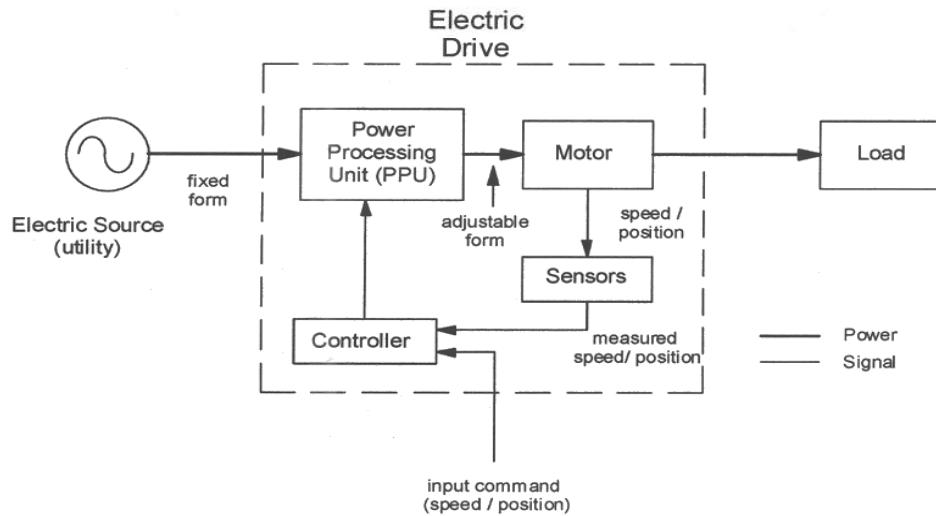


Figure 1-4 Block diagram of adjustable speed drives.

Induction heating and electric welding, shown in Fig. 1-5 and Fig. 1-6 by their block diagrams are other important industrial applications of power electronics for flexible production.

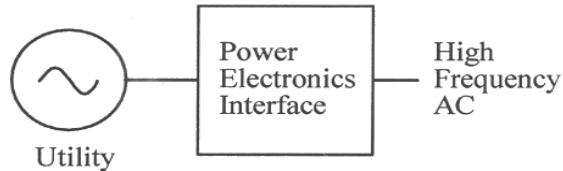


Figure 1-5 Power electronics interface required for induction heating.

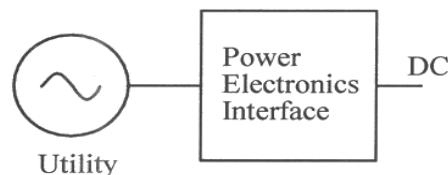


Figure 1-6 Power electronics interface required for electric welding.

1-3 ENERGY AND THE ENVIRONMENT

There is a growing body of evidence that burning of fossil fuels causes global warming that may lead to disastrous environmental consequences. Power electronics and drives can play a crucial role in minimizing the use of fossil fuels, as briefly discussed below.

1-3-1 Energy Conservation

It's an old adage: a penny saved is a penny earned. Not only energy conservation leads to financial savings, it helps the environment. The pie chart in Fig. 1-7 shows the percentages of electricity usage in the United States for various applications. The potentials for energy conservation in these applications are discussed below.

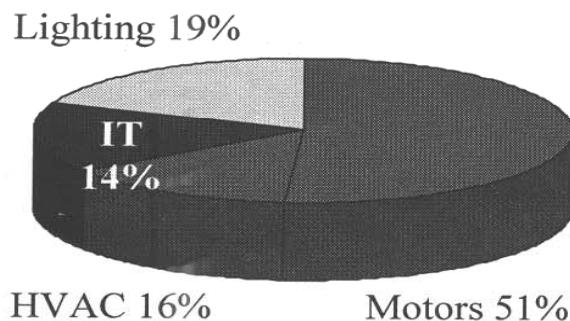


Figure 1-7 Percentage use of electricity in various sectors in the U.S.

1-3-1-1 Electric-Motor Driven Systems

Fig. 1-7 shows that electric motors, including their applications in heating, ventilating and air conditioning (HVAC), are responsible for consuming one-half to two-thirds of all the electricity generated. Traditionally, motor-driven systems run at a nearly constant speed and their output, for example, flow rate in a pump, is controlled by wasting a portion of the input energy across a throttling valve. This waste is eliminated by an adjustable-speed electric drive, as shown in Fig. 1-8 by efficiently controlling the motor speed, hence the pump speed, by means of power electronics [2].

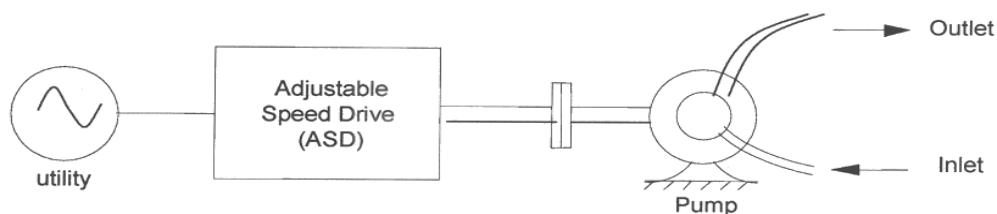


Figure 1-8 Role of adjustable speed drives in pump-driven systems.

One out of three new homes now uses electric heat pump, in which adjustable-speed drive can reduce energy consumption by as much as 30 percent [3] by eliminating on-off cycling of the compressor and running the heat pump at a speed that matches the thermal load of the building. The same is true for air conditioners.

A Department of Energy report [4] estimates that by operating all these motor-driven systems more efficiently in the United States could annually save electricity equivalent to the annual electricity usage by the entire state of New York!

1-3-1-2 Lighting

As shown in the pie chart in Fig. 1-7, approximately one-fifth of electricity produced is used for lighting. Fluorescent lights are more efficient than incandescent lights by a factor of three to four. The efficiency of fluorescent lights can be further improved by using high-frequency power electronic ballasts that supply 30 kHz to 40 kHz to the light bulb, as shown by the block diagram in Fig. 1-9, further increasing the efficiency by approximately 15 percent. Compared to incandescent light bulbs, high-frequency compact fluorescent lamps (CFLs) improve efficiency by a factor of four, last much longer (several thousand hours more), and their relative cost, although high at present, is dropping.

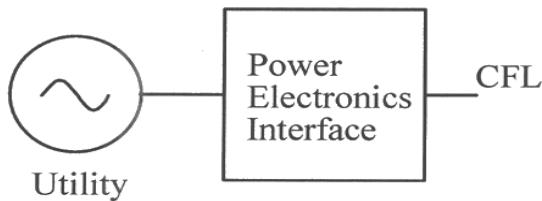


Figure 1-9 Power electronics interface required for CFL.

1-3-1-3 Transportation

Electric drives offer huge potential for energy conservation in transportation. While efforts to introduce commercially-viable Electric Vehicles (EVs) continue with progress in battery [5] and fuel cell technologies [6] being reported, hybrid electric vehicles (HEVs) are sure to make a huge impact [7]. According to the U.S. Environmental Protection Agency, the estimated gas mileage of the hybrid-electrical vehicle shown in Fig. 1-10 in combined city and highway driving is 48 miles per gallon [8]. This is in comparison to the gas mileage of 22.1 miles per gallon for an average passenger car in the U.S. in year 2001 [9]. Since automobiles are estimated to account for about 20% emission of all CO₂ [10] that is a greenhouse gas, doubling the gas mileage of automobiles would have an enormous impact on the environment.

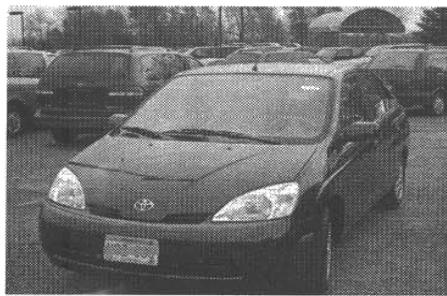


Figure 1-10 Hybrid electric vehicles with much higher gas mileage.

EVs and HEVs, of course, need power electronics in the form of adjustable-speed electric drives. Even in conventional automobiles, power electronic based load has grown to the extent that it is difficult to supply it from a 12/14-V battery system and there are serious proposals to raise it to 36/42-V level in order to keep the copper bus bars needed to carry currents a manageable size [11]. Add to this other transportation systems, such as light rail, fly-by-wire planes, all-electric ships and drive-by-wire automobiles, and transportation represents a major application area of power electronics.

1-3-2 Renewable Energy

Clean and renewable energy that is environmentally friendly can be derived from the sun and the wind. In photovoltaic systems, solar cells produce dc, with an *i-v* characteristic shown in Fig. 1-11a that requires a power electronics interface to transfer power into the utility system, as shown in Fig. 1-11b.

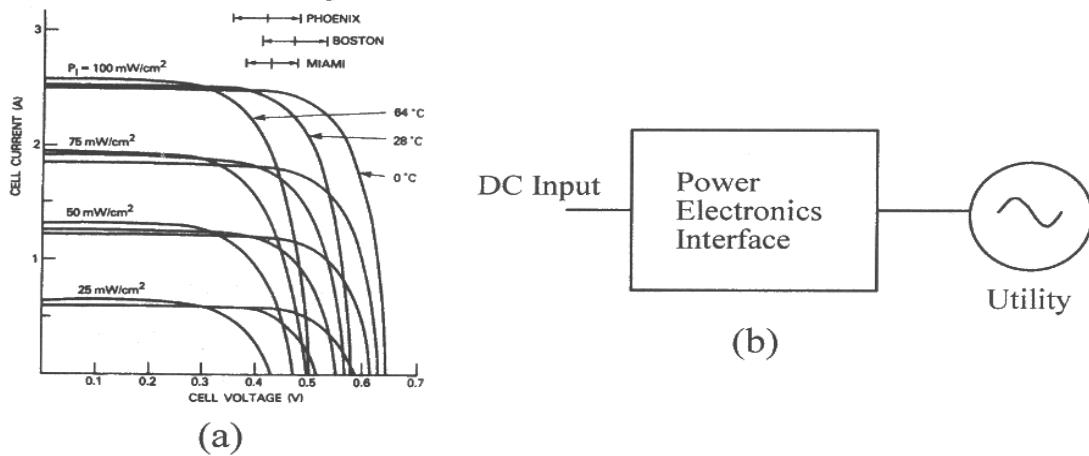


Figure 1-11 Photovoltaic Systems.

Wind is the fastest growing energy resource with enormous potential [12]. Fig. 1-12 shows the need of power electronics in wind-electric systems to interface variable-frequency ac to the line-frequency ac voltages of the utility grid.

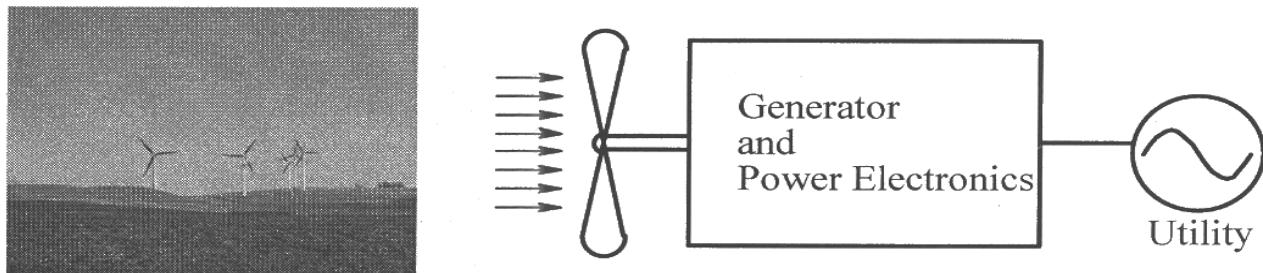


Figure 1-12 Wind-electric systems.

1-3-3 Utility Applications of Power Electronics

Applications of power electronics and electric drives in power systems are growing rapidly. In distributed generation, power electronics is needed to interface non-conventional energy sources such as wind, photovoltaic, and fuel cells to the utility grid. Use of power electronics allows control over the flow of power on transmission lines, an attribute that is especially significant in a deregulated utility environment. Also, the security and the efficiency aspects of power systems operation necessitate increased use of power electronics in utility applications.

Uninterruptible power supplies (UPS) are used for critical loads that must not be interrupted during power outages. The power electronics interface for UPS, shown in Fig. 1-13, has line-frequency voltages at both ends, although the number of phases may be different, and a means for energy storage is provided usually by batteries, which supply power to the load during the utility outage.

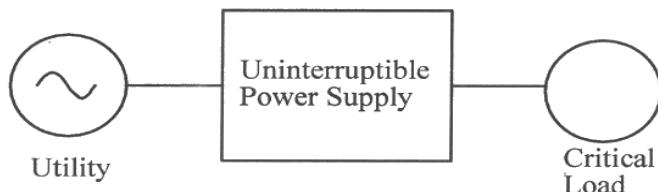


Figure 1-13 Uninterruptible power supply (UPS) system.

1-3-4 Strategic Space and Defense Applications

Power electronics is essential for space exploration and for interplanetary travel. Defense has always been an important application but it has become critical in the post-Sept 11th world. Power electronics will play a huge role in tanks, ships, and planes in which replacement of hydraulic drives by electric drives can offer significant cost, weight and reliability advantages.

1-4 NEED FOR HIGH EFFICIENCY AND HIGH POWER DENSITY

Power electronic systems must be energy efficient and reliable, have a high power density thus reducing their size and weight, and be low cost to make the overall system economically feasible. High energy efficiency is important for several reasons: it lowers operating costs by avoiding the cost of wasted energy, contributes less to global warming, and reduces the need for cooling (by heat sinks discussed later in this book) therefore increasing power density.

We can easily show the relationship in a power electronic system between the energy efficiency, η , and the power density. The energy efficiency is defined in Eq. 1-1 in terms of the output power P_o and the power loss P_{loss} within the system as

$$\eta = \frac{P_o}{P_o + P_{loss}} \quad (1-1)$$

Eq. 1-1 can be rewritten for the output power in terms of the efficiency and the power loss as

$$P_o = \frac{\eta}{1-\eta} P_{loss} \quad (1-2)$$

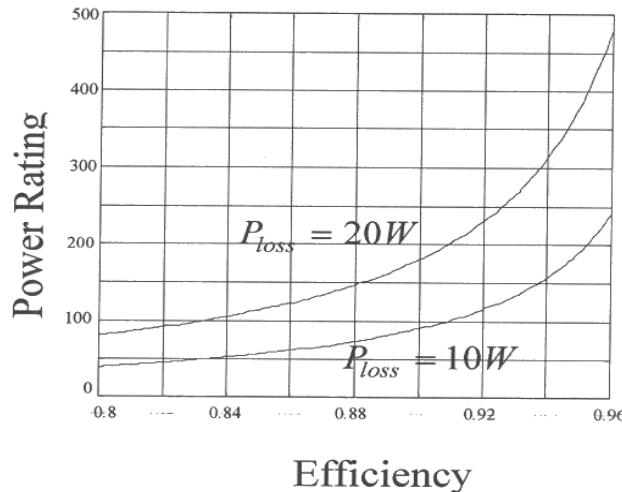


Figure 1-14 Power output capability as a function of efficiency.

In power electronics equipment, the cooling system is designed to transfer dissipated power, as heat, without allowing the internal temperatures to exceed certain limits. Therefore for a system designed to handle certain power loss, the plots in Fig. 1-14 based on Eq. 1-2 show that increasing the efficiency from 84% to 94% increases the power output capability (same as the power rating) of that equipment by a factor of three. This could mean an increase in the power density by approximately the same factor.

1-5 STRUCTURE OF POWER ELECTRONICS INTERFACE

By reviewing the role of power electronics in various applications discussed earlier, we can summarize that power electronics interface is needed to efficiently control the transfer of power between dc-dc, dc-ac, and ac-ac systems. In general, the power is supplied by the utility and hence, as depicted by the block diagram of Fig. 1-15, the line-frequency ac is at one end. At the other end, one of the following is synthesized: adjustable magnitude dc, sinusoidal ac of adjustable frequency and amplitude, or high frequency ac as in the case of compact fluorescent lamps (CFLs) and induction heating. Applications that do not require utility interconnection can be considered as the subset of the block diagram shown in Fig. 1-15.

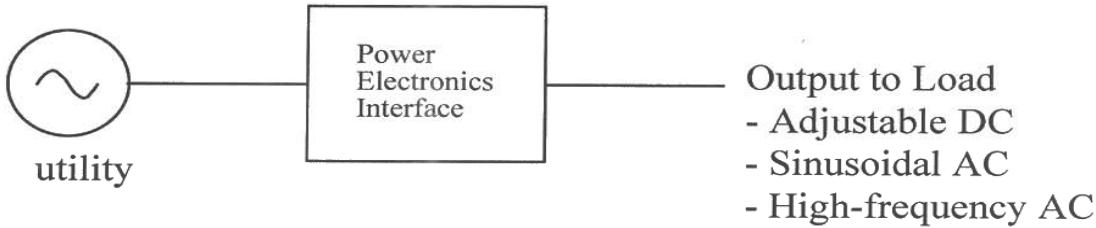


Figure 1-15 Block diagram of power electronic interface.

To provide the needed functionality to the interface in Fig. 1-15, the transistors and diodes, which can block voltage only of one polarity, have led to the structure shown in Fig. 1-16.

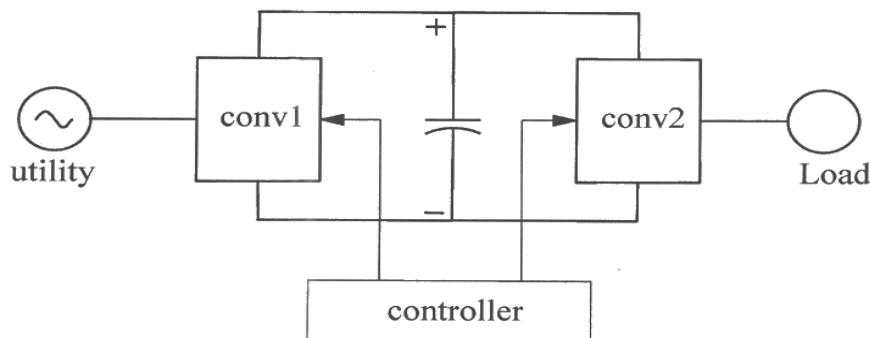


Figure 1-16 Voltage-link structure of power electronics interface.

This structure consists of two separate converters, one on the utility side and the other on the load side. The dc ports of these two converters are connected to each other with a parallel capacitor forming a dc-link, across which the voltage polarity does not reverse, thus allowing unipolar voltage handling transistors to be used within these converters. In certain applications, the power flow through these converters reverses, by currents reversing direction at the dc ports. The converter structure of Fig. 1-16 has the following benefits that explain their popularity:

- Decoupling of Two Converters: the voltage-port (dc-link) created by the capacitor in the middle decouples the operation of the utility-side and the load-side converters, thus allowing their design and operation to be optimized individually.
- Immunity from Momentary Power Interruptions: energy storage in the capacitor allows uninterrupted power flow to the load during momentary power-line disturbances. Continuing developments in increasing capacitor energy density further support this structure for the power electronics interface.

In the structure of Fig. 1-16, the capacitor in parallel with the two converters forms a dc voltage-link, hence this structure is called a *voltage-link* (or a *voltage-source*) structure. This structure is used in a very large power range, from a few tens of watts to several

megawatts, even extending to hundreds of megawatts in utility applications. Therefore, we will mainly focus on this voltage-link structure in this book.

At extremely high power levels, usually in utility-related applications, which we will discuss in the last two chapters in this book, it may be advantageous to use a *current-link* (or a *current-source*) structure, where an inductor in series with the two converters acts as a current-link.

Lately in niche applications, a *matrix converter* structure is being reevaluated, where theoretically there is no energy storage element between the input and the output sides. Discussion of matrix converters is beyond the scope of this book on the first course on power electronics and drives.

1-6 THE SWITCH-MODE LOAD-SIDE CONVERTER

In the structure of Fig. 1-16, the role of the utility-side converter is to convert line-frequency utility voltages to an unregulated dc voltage. This can be done by a diode-rectifier circuit like that discussed in basic electronics courses, although power quality concerns may lead to a different structure discussed in Chapter 6. We will focus our attention on the load-side converter in the structure of Fig. 1-16, where a dc voltage is applied as an input on one end.

Applications dictate the functionality needed of the load-side converter. Based on the desired output of the converter, we can group this functionality as follows:

- Group 1 Adjustable dc or a low-frequency sinusoidal ac output in
 - dc and ac motor drives
 - uninterruptible power supplies
 - regulated dc power supplies without electrical isolation
- Group 2 High-frequency ac in
 - compact fluorescent lamps
 - induction heating
 - regulated dc power supplies where the dc output voltage needs to be electrically isolated from the input, and the load-side converter internally produces high-frequency ac, which is passed through a high-frequency transformer and then rectified into dc.

1-6-1 Switch-Mode Conversion: Switching Power-Pole as the Building Block

Achieving high energy-efficiency for applications belonging to either group mentioned above requires switch-mode conversion, where in contrast to linear power electronics, transistors (and diodes) are operated as switches, either on off.

This switch-mode conversion can be explained by its basic building block, a switching power-pole A , as shown in Fig. 1-17a. It effectively consists of a bi-positional switch, which forms a two-port: a voltage-port across a capacitor with a voltage V_{in} that cannot change instantaneously, and a current-port due the series inductor through which the current cannot change instantaneously. For now, we will assume the switch ideal with two positions: up or down, dictated by a switching signal q_A which takes on two values: 1 and 0, respectively. The practical aspects of implementing this bi-positional switch we will consider in the next chapter.

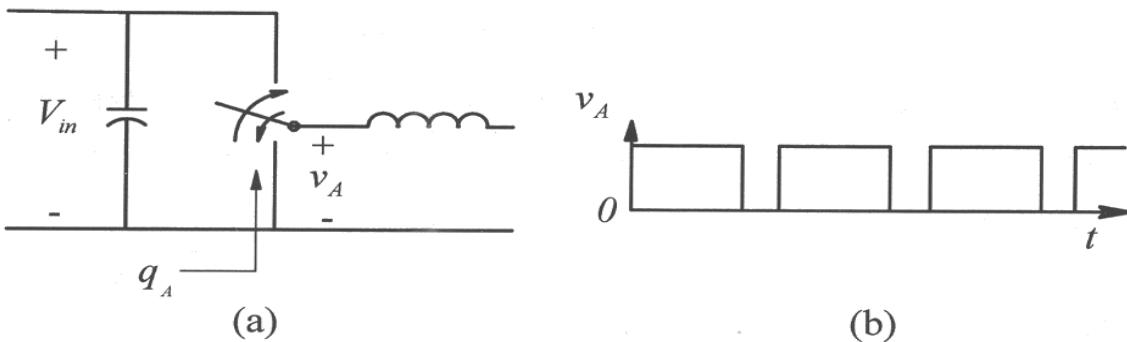


Figure 1-17 Switching power-pole as the building block in converters.

The bi-positional switch “chops” the input dc voltage V_{in} into a train of high-frequency voltage pulses, shown by the v_A waveform in Fig. 1-17b, by switching up or down at a high repetition rate, called the switching frequency f_s . Controlling the pulse width within a switching cycle allows control over the average value of the pulsed output, and this pulse-width modulation forms the basis of synthesizing adjustable dc and low-frequency sinusoidal ac outputs, as described in the next section. High-frequency pulses are clearly needed in applications such as compact fluorescent lamps, induction heating, and internally in dc power supplies where electrical isolation is achieved by means of a high-frequency transformer. A switch-mode converter consists of one or more such switching power-poles.

1-6-2 Pulse-Width Modulation (PWM) of the Switching Power-Pole (constant f_s)

For the applications in Group 1, the objective of the switching power-pole redrawn in Fig. 1-18a is to synthesize the output voltage such that its *average* is of the desired value: dc or ac that varies sinusoidally at a low-frequency. Switching at a constant switching-frequency f_s produces a train of voltage pulses in Fig. 1-18b that repeat with a constant switching time-period T_s , equal to $1/f_s$.

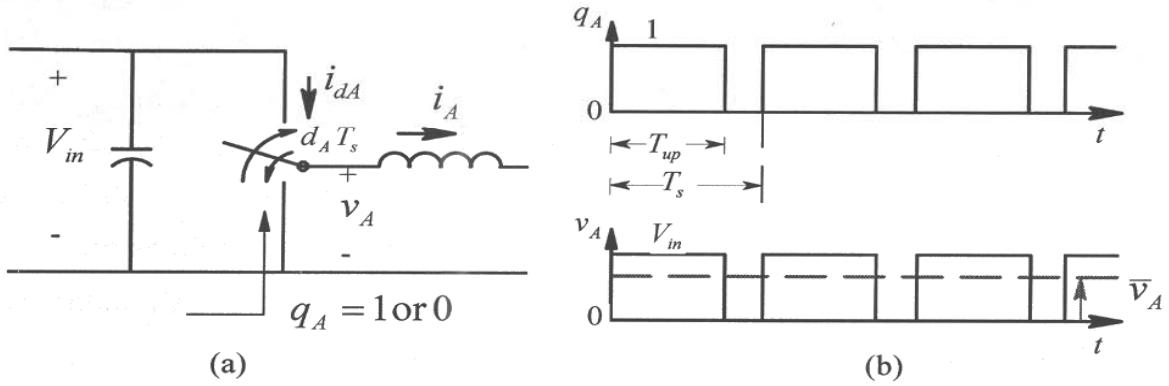


Figure 1-18 PWM of the switching power-pole.

Within each switching cycle with the time-period T_s ($=1/f_s$) in Fig. 1-18b, the *average* value \bar{v}_A of the waveform is controlled by the pulse width T_{up} during which the switch is in the up position, and v_A equals V_{in} :

$$\bar{v}_A = \frac{T_{up}}{T_s} V_{in} = d_A V_{in} \quad 0 \leq d_A \leq 1 \quad (1-3)$$

where $d_A (= T_{up} / T_s)$ is defined as the duty-ratio of the switching power-pole, and the average voltage is indicated by a “-” on top. The average voltage and the pole duty-ratio are expressed by lowercase letters since they may vary as functions of time. The control over the average value of the output voltage is achieved by adjusting or modulating the pulse width, which later on will be referred to as pulse-width-modulation (PWM). This switching power-pole and the control of its output by PWM set the stage for switch-mode conversion with high energy-efficiency.

We should note that \bar{v}_A and d_A in the above discussion are discrete quantities and their values are to be calculated over each switching cycle. However in practical applications, the pulse-width T_{up} changes very slowly over many switching cycles, and hence we can consider them as analog quantities $\bar{v}_A(t)$ and $d_A(t)$ that are continuous functions of time. For simplicity, we may not show their time dependence explicitly.

1-6-3 Switching Power-Pole in a Buck DC-DC Converter: An Example

As an example, we will consider the switching power-pole in a *Buck* converter to step-down the input dc voltage V_{in} , as shown in Fig. 1-19a, where a capacitor is placed across the load to form a low-pass L-C filter to provide a smooth voltage to the load.

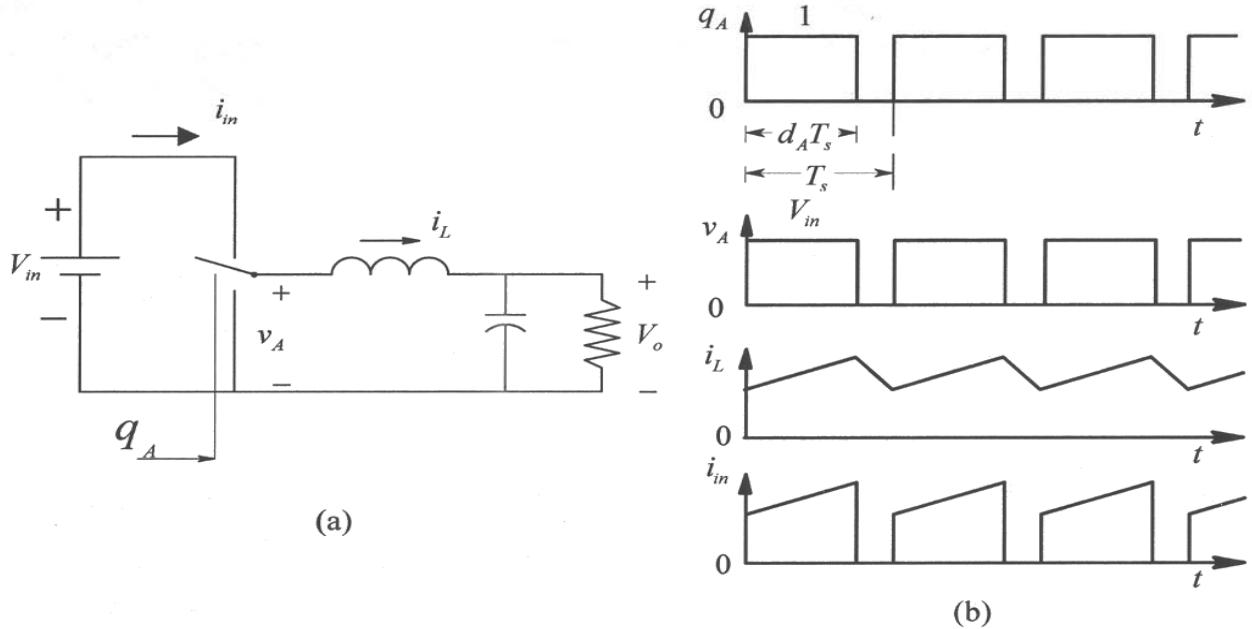


Figure 1-19 Switching power-pole in a Buck converter.

In steady state, the dc (average) input to this L-C filter has no attenuation, hence the average output voltage V_o equals the average, \bar{v}_A , of the applied input voltage. Based on Eq. 1-3, by controlling d_A , the output voltage can be controlled in a range from V_{in} down to 0 :

$$V_o = \bar{v}_A = d_A V_{in} \quad (0 \leq V_o \leq V_{in}) \quad (1-4)$$

In spite of the pulsating nature of the instantaneous output voltage $v_A(t)$, the series inductance at the current-port of the pole ensures that the current $i_L(t)$ remains relatively smooth, as shown in Fig. 1-19b.

1-6-3-1 Realizing the Bi-Positional Switch in a Buck Converter

As shown in Fig. 1-20a, the bi-positional switch in the power-pole can be realized by using a transistor and a diode. When the transistor is gated on (through a gate circuitry discussed in the next chapter by a switching signal $q_A = 1$), it carries the inductor current and the diode is reversed biased, as shown in Fig. 1-20b. When the transistor is switched off ($q_A = 0$), the inductor current “freewheels”, as shown in Fig. 1-20c through the diode until the next switching cycle when the transistor is turned back on. The switching waveforms, shown earlier in Fig. 1-19b, are discussed in detail in Chapter 3.

In the switch-mode circuit of Fig. 1-19a, higher the switching frequency, that is the frequency of the pulses in the $v_A(t)$ waveform, smaller the values needed of the low-pass

L-C filter. On the other hand, higher switching frequency results in higher switching losses in the bi-positional switch, which is the subject of the next chapter. Therefore, an appropriate switching frequency must be selected, keeping these trade-offs in mind.

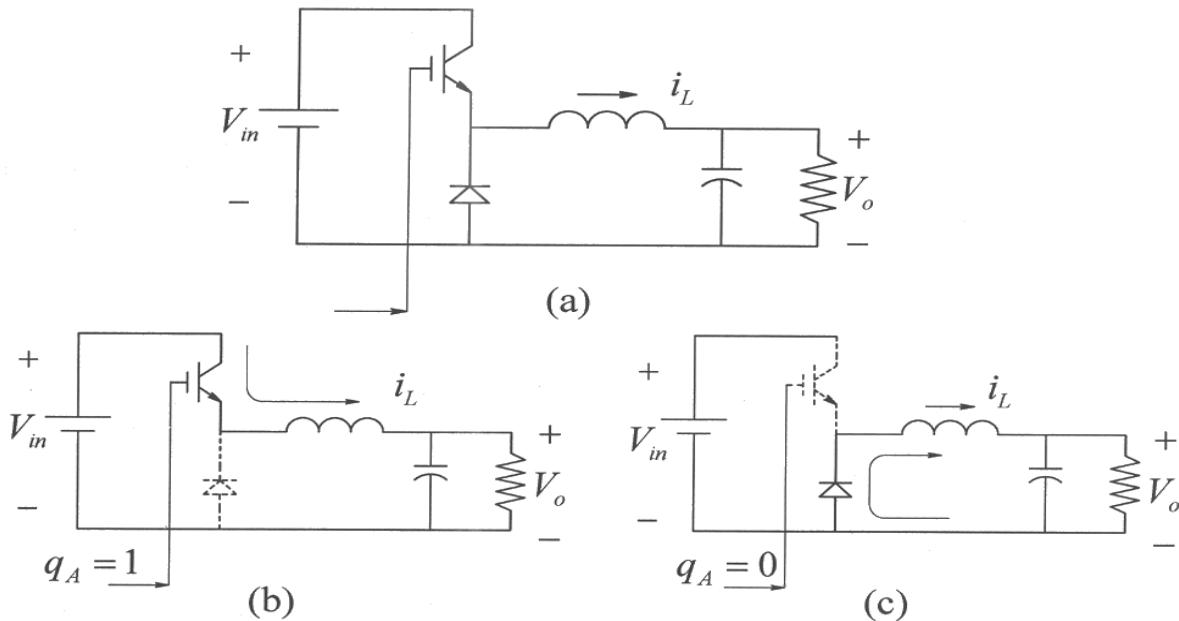


Figure 1-20 Transistor and diode forming a switching power-pole in a Buck converter.

1-7 RECENT AND POTENTIAL ADVANCEMENTS

Given the need in a plethora of applications, the rapid growth of this field is fueled by revolutionary advances in semiconductor fabrication technology. The power electronics interface of Fig. 1-1 consists of solid-state devices, which operate as switches, changing from on to off at a high frequency. There has been a steady improvement in the voltage and current handing capabilities of solid-state devices such as diodes and transistors, and their switching speeds (from on to off, and vice versa) have increased dramatically, with some devices switching in tens of ns . Devices that can handle voltages in kVs and currents in kAs are now available. These semiconductor switches are integrated in a single package with all the circuitry needed to make them switch, and to provide the necessary protection. Moreover, the costs of these devices are in a steady decline.

Power electronics has benefited from advances in the semiconductor fabrication technology in another important way. The availability of Application Specific Integrated Circuits (ASICs), Digital Signal Processor (DSPs), micro-controllers, and Field Programmable Gate Arrays (FPGA) at very low costs makes the controller function in the block diagram of Fig. 1-1 easy and inexpensive to implement, while greatly increasing functionality.

Significant areas for potential advancements in power electronic systems are in integrated and intelligent power modules, packaging, SiC-based solid-state devices, improved high energy density capacitors, and improved topologies and control.

REFERENCES

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.
2. N. Mohan and R.J. Ferraro, "Techniques for Energy Conservation in AC Motor Driven Systems", EPRI-Report EM-2037, Project 1201-1213, Sept. 1981.
3. N. Mohan and James Ramsey, "Comparative Study of Adjustable-Speed Drives for Heat Pumps", EPRI-Report EM-4704, Project 2033-4, Aug. 1986.
4. Turning Point Newsletter, dated November 1998, A Motor Challenge Bimonthly Publication by the U.S. Department of Energy (DOE). www.oit.doe.gov.
5. R. Stempel et al, "Nickel-Metal Hydride: Ready to Serve", IEEE-Spectrum, Nov. 1998, pp. 29-34.
6. Tom Gilchrist, "Fuel Cells to the Fore", IEEE-Spectrum, Nov. 1998, pp. 35-40.
7. D. Hermance and S. Sasaki, "Hybrid Electric Vehicles Take to the Streets", IEEE-Spectrum, Nov. 1998, pp. 48-52.
8. Toyota Motor Corporation (<http://www.toyota.com/html/shop/vehicles/prius>).
9. Energy Information Administration Monthly Energy Review, December 2002 (<http://www.eia.doe.gov/emeu/mer/overview.html>).
10. <http://www.nedo.go.jp/itd/fellow/english/project-e/7e.html>.
11. J. Kassakian, "Automotive Applications of Power Electronics", Proceedings of the NSF-sponsored Faculty Workshop on Teaching of Power Electronics and Electric Drives, Tempe, AZ, Jan 3-5, 2002 (<http://www.ece.umn.edu/groups/workshp2002>).
12. American Wind Energy Association (<http://www.awea.org>).
13. Edison Electric Institute's Statistical Yearbook (<http://www.eei.org>).
14. "‘Infinity’ Variable-Capacity Units Boast SEERS Above16," Air Conditioning, Heating and Refrigeration News, pp. 79-80, Jan 21, 1991.
15. <http://www.sylvania.com/home/energystar>.
16. <http://www.howstuffworks.com/question417.htm>.
17. <http://www.fhwa.dot.gov/ohim/1996/in3.pdf>.
18. <http://www.eia.doe.gov/emeu/25opec/sld000.htm>.
19. <http://www.siemenswestinghouse.com/en/fuelcells/hybrids/performance/index.cfm>.

PROBLEMS

Applications and Energy Conservation

- 1-1 A U.S. Department of Energy report [4] estimates that over 122 billion kWh/year can be saved in the manufacturing sector in the United States by using mature

and cost-effective conservation technologies. Calculate (a) how many 1000-MW generating plants are needed to operate constantly to supply this wasted energy, and (b) the annual savings in dollars if the cost of electricity is 0.10 \$/kWh.

- 1-2 In a process, a blower is used with the flow-rate profile shown in Fig. P1-2a. Using the information in Fig P1-2b, estimate the percentage reduction in power consumption resulting from using an adjustable-speed drive rather than a system with (a) an outlet damper and (b) an inlet vane.

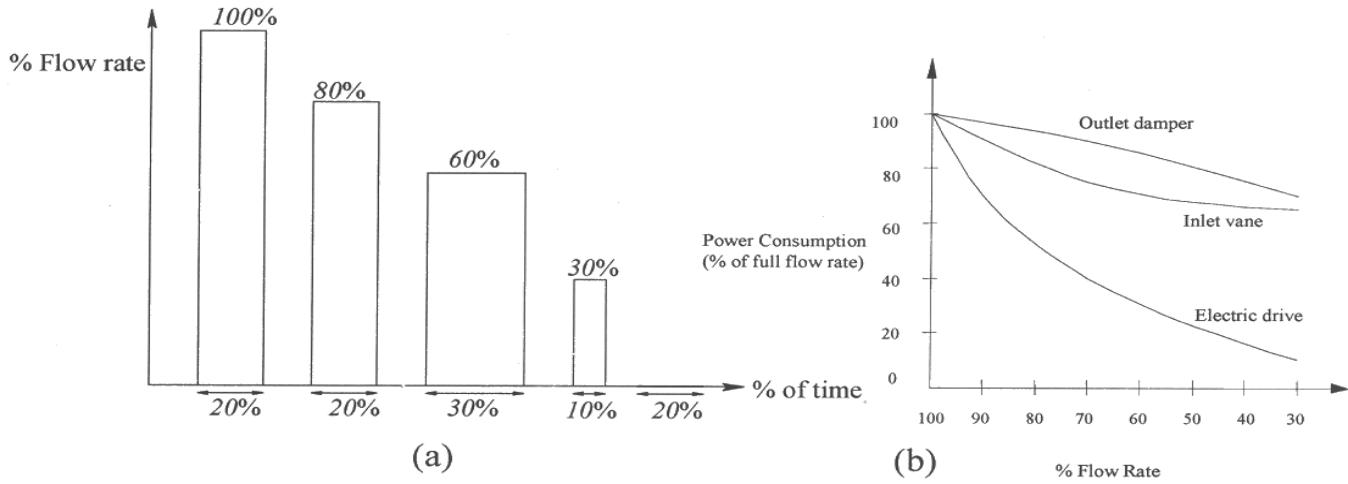


Figure P1-2

- 1-3 In a system, if the system size is based on power dissipation capacity, calculate the improvement in the power density if the efficiency is increased from 85% to 95%.
- 1-4 According to [13], electricity generation in the U.S. in year 2000 was approximately 3.8×10^9 MW-hrs. Fig. 1-7 shows that 16% of that is used for heating, ventilating and air conditioning. Based on [3, 14], as much as 30% of the energy can be saved in such systems by using adjustable speed drives. On this basis, calculate the savings in energy per year and relate that to 1000-MW generating plants needed to operate constantly to supply this wasted energy.
- 1-5 According to [12], the total amount of electricity that could potentially be generated from wind in the United States has been estimated at 10.8×10^9 MW-hrs annually. If one-tenth of this potential is developed, estimate the number of 1-MW windmills that would be required, assuming the capacity factor of the windmills to be 25%.
- 1-6 In problem 1-5, if each 1-MW windmill has 20% of its output power flowing through the power electronics interface, estimate the total rating of these interfaces in kW.
- 1-7 As the pie chart of Fig. 1-7 shows, lighting in the U.S. consumes 19% of the generated electricity. Compact Fluorescent Lamps (CFLs) consume power one-

fourth of that consumed by the incandescent lamps for the same light output [15]. According to [13], electricity generation in the U.S. in year 2000 was approximately 3.8×10^9 MW-hrs. Based on this information, estimate the savings in MW-hrs annually, assuming that all lighting at present is by incandescent lamps, which are to be replaced by CFLs.

- 1-8 An electric-hybrid vehicle offers 52 miles per gallon in mixed (city and highway) driving conditions according to the U.S. Environmental Protection Agency. This is in comparison to the gas mileage of 22.1 miles per gallon for an average passenger car in the U.S. in year 2001 [9], with an average of 11,766 miles driven. Calculate the savings in terms of barrels of oil per automobile annually, if a conventional car is replaced by an electric-hybrid vehicle. In calculating this, assume that a barrel of oil that contains 42 gallons yields approximately 20 gallons of gasoline [16].
- 1-9 Based on the estimate in [17] of approximately 136 million automobiles in 1995, we can project that today there are 150 million cars in the U.S. Using the results of Problem 1-8, calculate the total annual reduction of carbon into the atmosphere, if the consumption of each gallon of gasoline releases approximately 5 pounds of carbon [16].
- 1-10 Relate the savings of barrels of oil annually, as calculated in Problem 1-9, to the imported oil, if the U.S. imports approximately 35,000 million barrels of crude oil per year [18].
- 1-11 Fuel-cell systems that also utilize the heat produced can achieve efficiencies approaching 80% [19], more than double of the gas-turbine based electrical generation. Assume that 25 million households produce an average of 5 kW. Calculate the percentage of electricity generated by these fuel-cell systems compared to the annual electricity generation in the U.S. of 3.8×10^9 MW-hrs [13].
- 1-12 Induction cooking based on power electronics is estimated to be 80% efficient compared to 55% for conventional electric cooking. If an average home consumes 2 kW-hrs daily using conventional electric cooking, and that 50 million households switch to induction cooking in the U.S., calculate the annual savings in electricity usage.
- 1-13 Assume the average energy density of sunlight to be 800 W/m^2 and the overall photovoltaic system efficiency to be 10%. Calculate the land area covered with photovoltaic cells needed to produce 1,000 MW, the size of a typical large central power plant.
- 1-14 In problem 1-13, the solar cells are distributed on top of roofs, each in area of 50 m^2 . Calculate the number of homes needed to produce the same power.

PWM of the Switching Power-Pole

- 1-15 In a Buck converter, the input voltage $V_{in} = 12V$. The output voltage V_o is required to be $9V$. The switching frequency $f_s = 200kHz$. Assuming an ideal switching power-pole, calculate the pulse width T_{up} of the switching signal, and the duty-ratio d_A of the power pole.
- 1-16 In the Buck converter of Problem 1-15, assume the current through the inductor to be ripple-free with a value of $3A$ (the ripple in this current is discussed later in Chapter 3). Draw the waveforms of the voltage at the current-port and the input current at the voltage-port.
- 1-17 Using the input-output specifications given in Problems 1-15 and 1-16, calculate the maximum energy-efficiency expected of a linear regulator where the excess input voltage is dropped across a series element that behaves as a resistor.

Chapter 2

DESIGN OF SWITCHING POWER-POLES

In the previous chapter, we examined a switching power-pole as the building block of power electronic converters, consisting of an ideal bi-positional switch with an ideal transistor and an ideal diode, and pulse-width-modulated (PWM) to achieve regulation of the output. In this chapter, we will discuss the availability of various power semiconductor devices, their switching characteristics and various trade-offs in designing a switching power-pole. We will also briefly discuss a PWM-IC, which is used in regulating the average output of such switching power-poles.

2-1 POWER TRANSISTORS AND POWER DIODES [1]

The power-level diodes and transistors have evolved over decades from their signal-level counterparts to the extent that they can handle voltages and currents in kVs and kAs respectively, with fast switching times of the order of a few tens of ns to a few μs . Moreover, these devices can be connected in series and parallel to satisfy any voltage and current requirements.

Selection of power diodes and power transistors in a given application is based on the following characteristics:

1. Voltage Rating: the maximum instantaneous voltage that the device is required to block in its off-state, beyond which it "breaks down" and irreversible damage occurs.
2. Current Rating: the maximum current, expressed as instantaneous, average, and/or rms, that a device can carry in its on-state, beyond which excessive heating within the device destroys it.
3. Switching Speeds: the speeds with which a device can make a transition from its on-state to off-state, or vice versa. Small switching times associated with fast-switching devices result in low switching losses, or considering it differently, fast-switching devices can be operated at high switching frequencies with acceptable switching power losses.
4. On-State Voltage: the voltage drop across a device during its on-state while conducting a current. The smaller this voltage, the smaller will be the on-state power loss.

2-2 SELECTION OF POWER TRANSISTORS [2-5]

Transistors are controllable switches, which are available in several forms for switch-mode power electronics applications:

- MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors)
- IGBTs (Insulated-Gate Bipolar Transistors)
- IGCTs (Integrated-Gate-Controlled Thyristors)
- GTOs (Gate-Turn-Off thyristors)
- Niche devices for power electronics applications, such as BJTs (Bipolar-Junction Transistors), SITs (Static Induction Transistors), MCTs (MOS-Controlled Thyristors), and so on.

In switch-mode converters, there are two types of transistors which are primarily used: MOSFETs are typically used below a few hundred volts at switching frequencies in excess of 100 kHz, whereas IGBTs dominate very large voltage, current and power ranges extending to MW levels, provided the switching frequencies are below a few tens of kHz. IGCTs and GTOs are used in utility applications of power electronics at power levels beyond a few MWs. The following subsections provide a brief overview of MOSFET and IGBT characteristics and capabilities.

2-2-1 MOSFETs

In applications at voltages below 200 volts and switching frequencies in excess of 100 kHz, MOSFETs are clearly the device of choice because of their low on-state losses in low voltage ratings, their fast switching speeds, and a high impedance gate which requires a small voltage and charge to facilitate on/off transition. The circuit symbol of an n-channel MOSFET is shown in Fig. 2-1a. It consists of three terminals: drain (D), source (S), and gate (G). The forward current in a MOSFET flows from the drain to the source terminal. MOSFETs can block only the forward polarity voltage, that is, a positive v_{DS} . They cannot block a negative-polarity voltage due to an intrinsic anti-parallel diode, which can be used effectively in most switch-mode converter designs. MOSFET i - v characteristics for various gate voltage values are shown in Fig. 2-1b.

For gate voltages below a threshold value $v_{GS(th)}$, typically in a range of 2 to 4 V, a MOSFET is completely off, as shown by the i - v characteristics in Fig. 2-1b, and approximates an open switch. Beyond $v_{GS(th)}$, the drain current i_D through the MOSFET depends on the applied gate voltage v_{GS} , as shown by the transfer characteristic shown in Fig. 2-1c, which is valid almost for any value of the voltage v_{DS} across the MOSFET (note the horizontal nature of i - v characteristics in Fig. 2-1b). To carry $i_D (= I_o)$ would

require a gate voltage of a value, at least equal to $V_{GS(I_o)}$, as shown in Fig. 2-1c. Typically, a higher gate voltage, approximately 10 V, is maintained in order to keep the MOSFET in its on-state and carrying $i_D (= I_o)$.

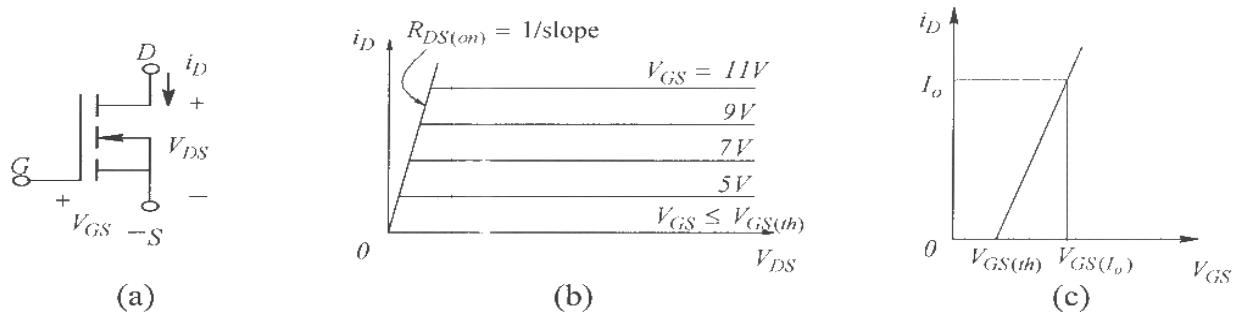


Figure 2-1 MOSFET: (a) symbol, (b) i - v characteristics, (c) transfer characteristic.

In its on-state, a MOSFET approximates a very small resistor $R_{DS(on)}$, and the drain current that flows through it depends on the external circuit in which it is connected. The on-state resistance, inverse of the slope of i - v characteristics as shown in Fig. 2-1b, is a strong function of the blocking voltage rating V_{DSS} of the device:

$$R_{DS(on)} \propto V_{DSS}^{2.5 \text{ to } 2.7} \quad (2-1)$$

The relationship in Eq. 2-1 explains why MOSFETs in low-voltage applications, at less than 200 V, are an excellent choice. The on-state resistance goes up with the junction temperature within the device and proper heatsinking must be provided to keep the temperature below the design limit.

2-2-2 IGBTs

IGBTs combine the ease of control, as in MOSFETs, with low on-state losses even at fairly high voltage ratings. Their switching speeds are sufficiently fast for switching frequencies up to 30 kHz. Therefore, they are used for converters in a vast voltage and power range - from a fractional kW to several MWs where switching frequencies required are below a few tens of kHz.

The circuit symbol for an IGBT is shown in Fig. 2-2a and the i - v characteristics are shown in Fig. 2-2b. Similar to MOSFETs, IGBTs have a high impedance gate, which requires only a small amount of energy to switch the device. IGBTs have a small on-state voltage, even in devices with large blocking-voltage rating, for example, V_{on} is approximately 2 V in 1200-V devices.

IGBTs can be designed to block negative voltages, but most commercially available devices, by design to improve other properties, cannot block any appreciable reverse-

polarity voltage. IGBTs have turn-on and turn-off times on the order of a microsecond and are available as modules in ratings as large as 3.3 kV and 1200 A. Voltage ratings of up to 5 kV are projected.

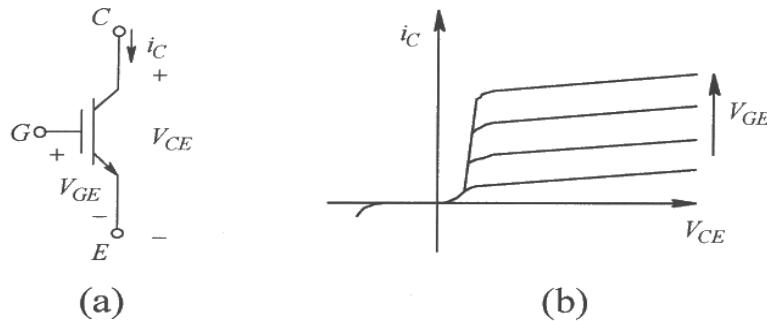


Figure 2-2 IGBT: (a) symbol, (b) i - v characteristics.

2-2-3 Power-Integrated Modules and Intelligent-Power Modules [2-4]

Power electronic converters, for example for three-phase ac drives, require six power transistors. Power-integrated modules (PIMs) combine several transistors and diodes in a single package. Intelligent-power modules (IPMs) include power transistors with the gate-drive circuitry. The input to this gate-drive circuitry is a signal that comes from a microprocessor or an analog integrated circuit, and the output drives the MOSFET gate. IPMs also include fault protection and diagnostics, thereby immensely simplifying the power electronics converter design.

2-2-4 Costs of MOSFETs and IGBTs

As these devices evolve, their relative costs continue to decline. The costs of single devices are approximately 0.25 \$/A for 600-V devices and 0.50 \$/A for 1200-V devices. Power modules for the 3 kV class of devices cost approximately 1 \$/A.

2-3 SELECTION OF POWER DIODES

The circuit symbol of a diode is shown in Fig. 2-3a and its i - v characteristic in Fig. 2-3b shows that a diode is an uncontrolled device that blocks reverse polarity voltage. Power diodes are available in large ranges of reverse voltage blocking and forward current carrying capabilities. Similar to transistors, power diodes are available in several forms as follows, and their selection must be based on their application:

- Line-frequency diodes
- Fast-recovery diodes
- Schottky diodes
- SiC-based Schottky diodes

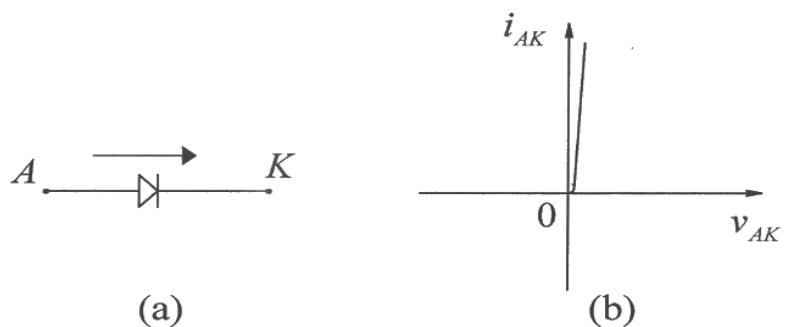


Figure 2-3 Diode: (a) symbol, (b) i - v characteristic.

Rectification of line-frequency ac to dc can be accomplished by slower switching p - n junction power (line-frequency) diodes, which have relatively a slightly lower on-state voltage drop, and are available in voltage ratings of up to 9 kV and current ratings of up to 5 kA. The on-state voltage drop across these diodes is usually on the order of 1 to 3 V, depending on the voltage blocking capability.

Switch-mode converters operating at high switching frequencies, from several tens of kHz to several hundred kHz, require fast-switching diodes. In such applications, fast-recovery diodes, also formed by p - n junction as the line-frequency diodes, must be selected to minimize switching losses associated with the diodes.

In applications with very low output voltages, the forward voltage drop of approximately a volt or so across the conventional p-n junction diodes becomes unacceptably high. In such applications, another type of device called the Schottky diode is used with a voltage drop in the range of 0.3 to 0.5 V. Being majority-carrier devices, Schottky diodes switch extremely fast and keep switching losses to a minimum.

All devices, transistors and diodes, discussed above are silicon based. Lately, silicon-carbide (SiC) based Schottky diodes in voltage ratings of up to 600 V have become available [6]. In spite of their large on-state voltage drop (1.7 V, for example), their capability to switch with a minimum of switching losses makes them attractive in converters with voltages in excess of a few hundred volts.

2-4 SWITCHING CHARACTERISTICS AND POWER LOSSES IN POWER-POLES

In switch-mode converters, it is important to understand switching characteristics of the switching power-pole. As discussed in the previous chapter, the power-pole in a Buck converter shown in Fig. 2-4a is implemented using a transistor and a diode, where the current through the current port is assumed a constant dc, I_o , for discussing switching characteristics. We will assume the transistor to be a MOSFET, although a similar discussion applies if an IGBT is selected.

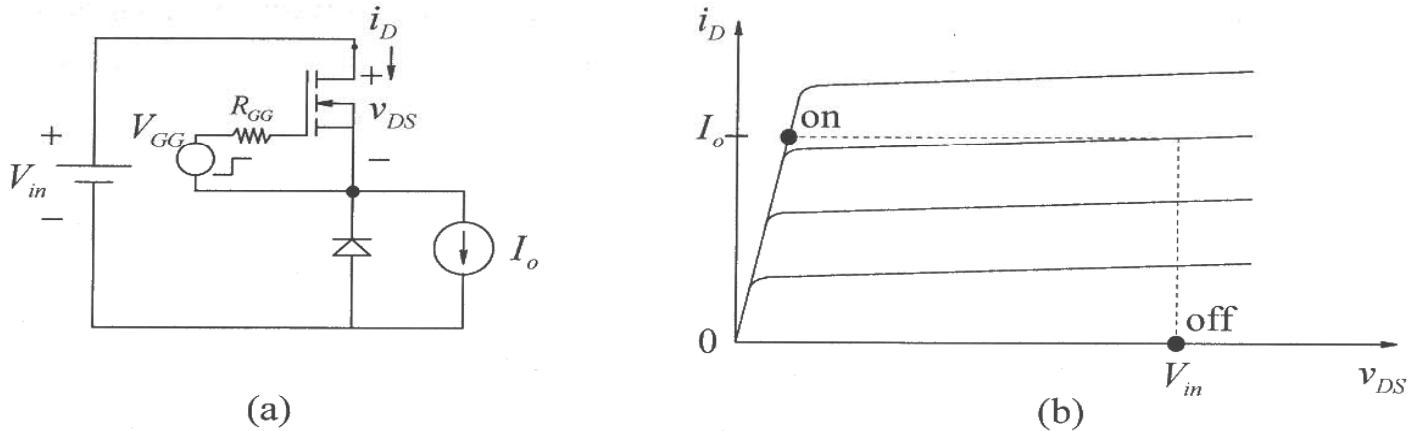


Figure 2-4 MOSFET in a switching power-pole.

For the n-channel MOSFET (p-channel MOSFETs have poor characteristics and are seldom used in power applications), the typical i_D versus v_{DS} characteristics are shown in Fig. 2-4b for various gate voltages. The off-state and the on-state operating points are labeled on these characteristics.

Switching characteristics of MOSFETs, hence of the switching power-pole in Fig. 2-4a are dictated by a combination of factors: the speed of charging and discharging of junction capacitances within the MOSFET, i_D versus v_{DS} characteristics, the circuit of Fig. 2-4a in which the MOSFET is connected and its gate-drive circuitry. We should note that the MOSFET junction capacitances are highly nonlinear functions of drain-source voltage and go up dramatically by several orders of magnitude at lower voltages. In Fig. 2-4a, the gate-drive voltage for the MOSFET is represented as a voltage source, which changes from 0 to V_{GG} , approximately 10 V, and vice versa, and charges or discharges the gate through a resistance R_{gate} that is the sum of an external resistance R_{GG} and the internal gate resistance.

Only a simplified explanation of the turn-on and turn-off characteristics, assuming an ideal diode, is presented here. The switching details including the diode reverse recovery are discussed in the Appendix to this chapter.

2-4-1 Turn-on Characteristic

Prior to turn-on, Fig. 2-5a shows the circuit in which the MOSFET is off and blocks the input dc voltage V_{in} ; I_o “freewheels” through the diode. By applying a positive voltage to the gate, the turn-on characteristic describes how the MOSFET goes from the off-point to the on-point in Fig. 2-5b. To turn the MOSFET on, the gate-drive voltage goes up from 0 to V_{GG} , and it takes the gate-drive a finite amount of time, called the turn-on

delay-time $t_{d(on)}$, to charge the gate-source capacitance through the gate-circuit resistance R_{gate} to the threshold value of $V_{GS(th)}$. During this turn-on delay time, the MOSFET remains off and I_o continues to freewheel through the diode, as shown in Fig. 2-5a.

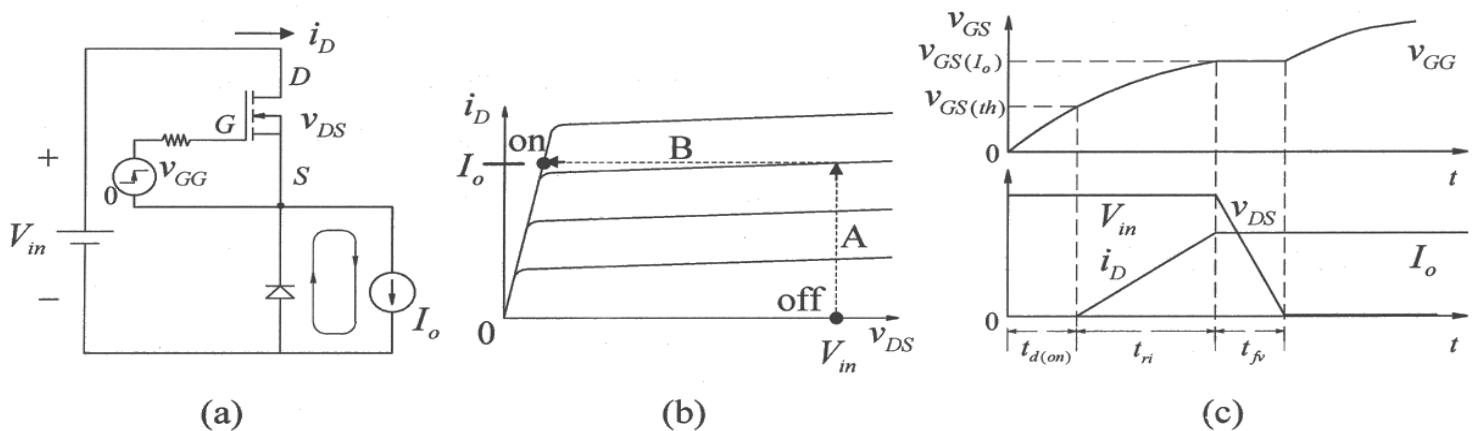


Figure 2-5 MOSFET turn-on.

For the MOSFET to turn on, first the current i_D through it rises. As long as the diode is conducting a positive net current ($I_o - i_D$), the voltage across it is zero and the MOSFET must block the entire input voltage V_{in} . Therefore, during the current rise-time t_{ri} , the MOSFET voltage and the current are along the trajectory A in the i - v characteristics of Fig. 2-5b, and are plotted in Fig. 2-5c. Once the MOSFET current reaches I_o , the diode becomes reverse biased, and the MOSFET voltage falls. During the voltage fall-time t_{fv} , as depicted by the trajectory B in Fig. 2-5b and the plots in Fig. 2-5c, the gate-to-source voltage remains at $V_{GS(I_o)}$. Once the turn-on transition is complete, the gate charges to the gate-drive voltage V_{GG} , as shown in Fig. 2-5c.

2-4-2 Turn-off Characteristic

The turn-off sequence is opposite to the turn-on process. Prior to turn-off, the MOSFET is conducting I_o and the diode is reversed biased as shown in Fig. 2-6a. The MOSFET i - v characteristics are re-plotted in Fig 2-6b. The turn-off characteristic describes how the MOSFET goes from the on-point to the off-point in Fig. 2-6b. To turn the MOSFET off, the gate-drive voltage goes down from V_{GG} to 0. It takes the gate-drive a finite amount of time, called the turn-off delay-time $t_{d(off)}$, to discharge the gate-source capacitance through the gate-circuit resistance R_{gate} , from a voltage of V_{GG} to $V_{GS(I_o)}$. During this turn-off delay time, the MOSFET remains on.

For the MOSFET to turn off, the output current must be able to “freewheel” through the diode. This requires the diode to become forward biased, and thus the voltage across the MOSFET must rise as shown by the trajectory *C* in Fig. 2-6b, while the current through it remains I_o . During this voltage rise-time t_{rv} , the voltage and current are plotted in Fig. 2-6c, while the gate-to-source voltage remains at $V_{GS(I_o)}$. Once the voltage across the MOSFET reaches V_{in} , the diode becomes forward biased, and the MOSFET current falls. During the current fall-time t_{fj} , depicted by the trajectory *D* in Fig. 2-6b and the plots in Fig. 2-6c, the gate-to-source voltage declines to $V_{GS(th)}$. Once the turn-off transition is complete, the gate discharges to 0.

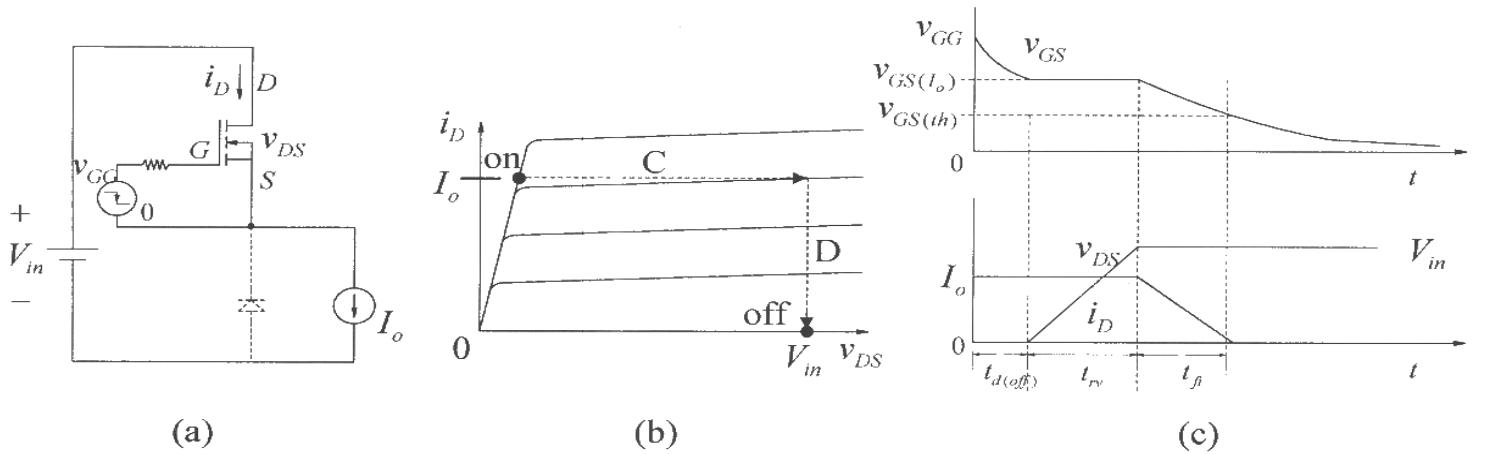


Figure 2-6 MOSFET turn-off.

2-4-3 Calculating Power Losses Within the MOSFET (assuming an ideal diode)

Power losses in the gate-drive circuitry are negligibly small except at very high switching frequencies. The primary source of power losses is across the drain and the source, which can be divided into two categories: the conduction loss, and the switching losses. Both of these are discussed in the following sections.

2-4-3-1 Conduction Loss

In the on-state, the MOSFET conducts a drain current for an interval T_{on} during every switching time-period T_s , with the switch duty-ratio $d = T_{on} / T_s$. Assuming this current a constant I_o during $d T_s$, the average power loss in the on-state resistance $R_{DS(on)}$ of the MOSFET is:

$$P_{cond} = d R_{DS(on)} I_o^2 \quad (2-2)$$

As pointed out earlier, $R_{DS(on)}$ varies significantly with the junction temperature and data sheets often provide its value at the junction temperature equal to $25^\circ C$. However, it will be more realistic to use twice this resistance value that corresponds to the junction temperature equal to $120^\circ C$, for example. Eq. 2-2 can be refined to account for the effect of ripple in the drain current on the conduction loss. The conduction loss is highest at the maximum load on the converter when the drain current would also be at its maximum.

2-4-3-2 Switching Losses

At high switching frequencies, switching power losses can be even higher than the conduction loss. The switching waveforms for the MOSFET voltage v_{DS} and the current i_D , corresponding to the turn-on and the turn-off trajectories in Figs. 2-5 and 2-6, assumed linear with time, are re-plotted in Fig. 2-7. During each transition from on to off, and vice versa, the transistor has simultaneously high voltage and current, as seen from the switching waveforms in Fig. 2-7. The instantaneous power loss $p_{sw}(t)$ in the transistor is the product of v_{DS} and i_D , as plotted. The average value of the switching losses from the plots in Fig. 2-7 is

$$P_{sw} = \frac{1}{2} V_{in} I_o (t_{c,on} + t_{c,off}) f_s \quad (2-3)$$

where $t_{c,on}$ and $t_{c,off}$ are defined in Fig. 2-7 as the sum of the rise and the fall times associated with the MOSFET voltage and current:

$$t_{c,on} = t_{ri} + t_{fv} \quad (2-4)$$

$$t_{c,off} = t_{rv} + t_{fi} \quad (2-5)$$

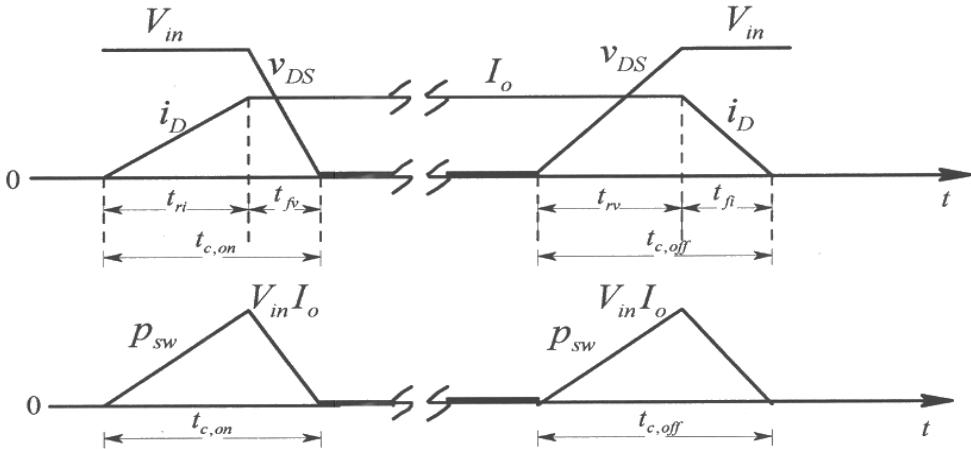


Figure 2-7 MOSFET switching losses.

▲ Example 2-1 Assuming an ideal diode, calculate losses in a MOSFET for the following operating conditions in the power-pole of Fig. 2-4a: $V_{in} = 40V$, $I_o = 5A$, $d = 0.4$, and $f_s = 300\text{kHz}$. Assume that the switching times $t_{c,on} = t_{c,off} = 25\text{ns}$. The on-state resistance $R_{DS(on)} = 0.3\Omega$. Also calculate the percentage efficiency of the converter based just on the losses in the MOSFET.

Solution From Eq. 2-2, the average conduction power loss is $P_{cond} = d R_{DS(on)} I_o^2 = 3W$. From Eq. 2-3, using Eqs. 2-4 and 2-5, the average switching power loss is $P_{sw} = 0.5 \times V_{in} I_o (t_{c,on} + t_{c,off}) f_s = 1.5W$. Therefore, the total power loss $P_{loss} = 4.5W$. The output voltage of the converter is $V_o = d V_{in} = 16V$. The output power $P_o = V_o I_o = 80W$. From Eq. 1-1 of Chapter 1, the converter efficiency based on the MOSFET power losses is $\eta = 94.67\%$.

2-4-4 Gate Driver Integrated Circuits (ICs) with Built-in Fault Protection [2]

Application-Specific ICs (ASICs) for controlling the gate voltages of MOSFETs and IGBTs greatly simplify converter design by including various protection features, for example, the over-current protection that turns off the transistor under fault conditions. This functionality, as discussed earlier, is integrated into Intelligent Power Modules along with the power semiconductor devices.

The IC to drive the MOSFET gate is shown in Fig. 2-8 in a block diagram form. To drive the high-side MOSFET in the power-pole, the input signal v_c from the controller is referenced to the logic level ground, V_{CC} is the logic supply voltage, and V_{ext} to drive the gate is supplied by an isolated power supply referenced to the MOSFET source S .

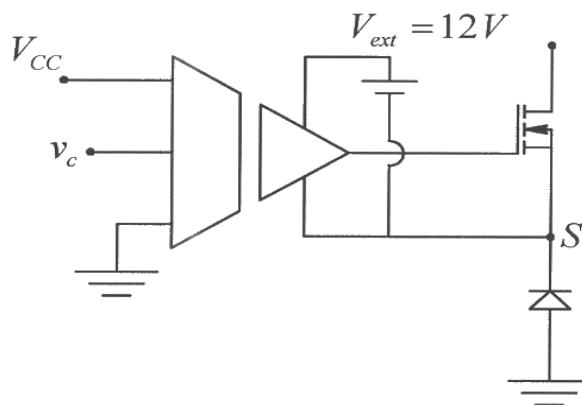


Figure 2-8 Gate-driver IC functional diagram.

One of the ICs for this purpose is IR2127, which can source 200 mA for gate charging and sink 420 mA for gate discharging, with typical turn-on and turn-off times of 200 ns

and 150 ns, respectively. This IC, although it has relatively large switching times, may be a good choice due to its easy-to-use fault protection capability, in which the transistor current, measured via the voltage drop across a small resistance in series with the transistor, disables the gate-drive voltage under over-current conditions.

2-5 JUSTIFYING SWITCHES AND DIODES AS IDEAL

Product reliability and high energy-efficiency are two very important criteria. In designing converters, it is essential that in the selection of semiconductor devices, we consider their voltage and current ratings with proper safety margins for reliability purposes. Achieving high energy-efficiency from converters requires that in selecting power devices, we consider their on-state voltage drops and their switching characteristics. We also need to calculate the heat that needs to be removed for proper thermal design.

Typically, the converter energy efficiency of approximately 90 percent or higher is realized. This implies that semiconductor devices have a very small loss associated with them. Therefore, in analyzing various converter topologies and comparing them against each other, we can assume transistors and diodes ideal. Their non-idealities, although essential to consider in the actual selection and the subsequent design process, represent a second-order phenomena, that will be ignored in analyzing various converter topologies. We will use a generic symbol shown earlier for transistors, regardless of their type, and ignore the need for a specific gate-drive circuitry.

2-6 DESIGN CONSIDERATIONS

In designing any converter, the overall objectives are to optimize their cost, size, weight, energy efficiency, and the reliability. With these goals in mind, we will briefly discuss some important considerations as the criteria for selecting the topology and the components in a given application.

2-6-1 Switching Frequency f_s

As discussed in the Buck converter example of the previous chapter, a switching power-pole results in a waveform pulsating at a high switching frequency at the current-port. The high frequency components in the pulsating waveform need to be filtered. It is intuitively obvious that the benefits of increasing the switching frequencies lie in reducing the filter component values, L and C , hence their physical sizes in a converter. (This is true up to a certain value, for example, up to a few hundred kHz, beyond which, for example, magnetic losses in inductors and the internal inductance within capacitors reverse the trend.) Hence, higher switching frequencies allow a higher control bandwidth, as we will see in Chapter 4.

The negative consequences of increasing the switching frequency are in increasing the switching losses in the transistor and the diode, as discussed earlier. Higher switching frequencies also dictate a faster switching of the transistor by appropriately designed gate-drive circuitry, generating greater problems of electromagnetic interference due to higher di/dt and dv/dt that introduce switching noise in the control loop. We can minimize these problems, at least in dc-dc converters, by adopting a soft-switching topology discussed in Chapter 10.

2-6-2 Selection of Transistors and Diodes

Earlier we discussed the voltage and the switching frequency ranges for selecting between MOSFETs and IGBTs. Similarly, the diode types should be chosen appropriately. The voltage rating of these devices is based on the peak voltage \hat{V} in the circuit (including voltage spikes due to parasitic effects during switching). The current ratings should consider the peak current \hat{I} that the devices can handle and which dictates the switching power loss, the rms current I_{rms} for MOSFETs which behave as a resistor with $R_{DS(on)}$ in their on-state, and the average current I_{avg} for IGBTs and diodes, which can be approximated to have a constant on-state voltage drop. Safety margins, which depend on the application, dictate that the device ratings be greater than the worst-case stresses by a certain factor.

2-6-3 Magnetic components

As discussed earlier, the filter inductance value depends on the switching frequency. Inductor design is discussed later in Chapter 9, which shows that the physical size of a filter inductor, to a first approximation, depends on a quantity called the area-product (A_p) given by the equation below:

$$A_p = L \hat{I} I_{rms} \quad (2-6)$$

Increasing L in many topologies reduces the peak and the rms values (also reducing the transistor and the diode current stresses) but has the negative consequence of increasing the overall inductor size and possibly reducing the control bandwidth.

2-6-4 Capacitor Selection [7]

Capacitors have switching losses designated by an equivalent series resistance, ESR, as shown in Fig. 2-9. They also have an internal inductance, represented as an equivalent series inductance, ESL. The resonance frequency, the frequency beyond which ESL begins to dominate C, depends on the capacitor type. Electrolytic capacitors offer high capacitance per unit volume but have low resonance frequency. On the other hand, capacitors such as metal-polypropylene have relatively high resonance frequency.

Therefore, in switch-mode dc power supplies, an electrolytic capacitor with high C may often be paralleled with a metal-polyester capacitor to form the output filter capacitor.



Figure 2-9 Capacitor ESR and ESL.

2-6-5 Thermal Design [8, 9]

Power dissipated in the semiconductor and the magnetic devices must be removed to limit temperature rise within the device. The reliability of converters and their life expectancy depend on the operating temperatures, which should be well below their maximum allowed values. On the other hand, letting them operate at a high temperature decreases the cost and the size of the heat sinks required. There are several cooling techniques but for general-purpose applications, converters are often designed for cooling by normal air convection, without the use of forced air or liquid.

Semiconductor devices come in a variety of packages, which differ in cost, ruggedness, thermal conduction, and the radiation hardness if the application demands it. Fig. 2-10a shows a semiconductor device affixed to a heat sink through an isolation pad that is thermally conducting but provides electrical isolation between the device case and the heat sink.

An analogy can be drawn with an electrical circuit of Fig. 2-10b where the power dissipation within the device is represented as a dc current source, thermal resistances offered by various paths are represented as series resistances, and the temperatures at various points as voltages. The data sheets specify various thermal resistance values. The heat transfer mechanism is primarily conduction from the semiconductor device to its case and through the isolation pad. The resulting thermal resistances can be represented by $R_{\theta_{jc}}$ and $R_{\theta_{cs}}$, respectively. From the heat sink to the ambient, the heat transfer mechanisms are primarily convection and radiation, and the thermal resistance can be represented by $R_{\theta_{sa}}$. Based on the electrical analogy, the junction temperature can be calculated as follows for the dissipated power P_{diss} :

$$T_j = T_a + (R_{\theta_{jc}} + R_{\theta_{cs}} + R_{\theta_{sa}})P_{diss} \quad (2-7)$$

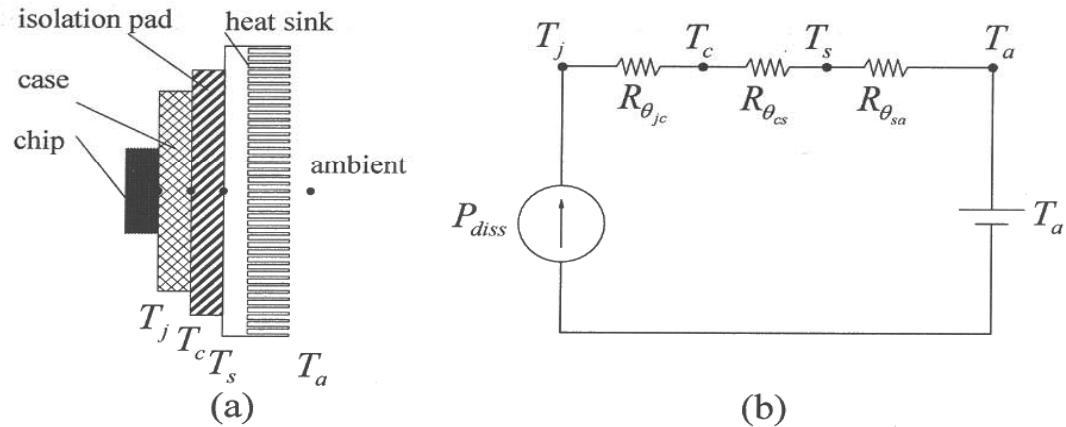


Figure 2-10 Thermal design: (a) semiconductor on a heat sink, (b) electrical analog.

2-6-6 Design Tradeoffs

As a function of switching frequency, Fig. 2-11 qualitatively shows the plot of physical sizes for the magnetic components and the capacitors, and the heat sink. Based on the present state-of-the-art, optimum values of switching frequencies to minimize the overall size in dc-dc converters using MOSFETs range from 200 kHz to 300 kHz with a slight upward trend.

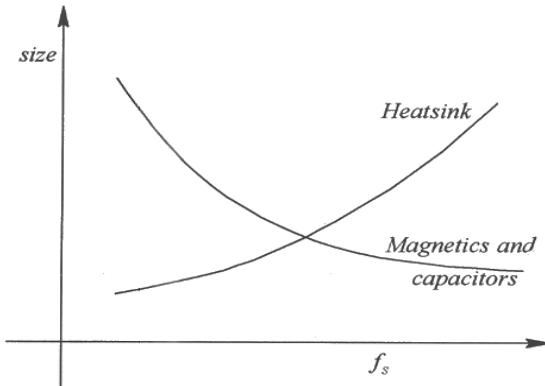


Figure 2-11 Size of magnetic components and heat sink as a function of frequency.

2-7 THE PWM IC [10]

In the pulse-width-modulation of the power-pole in a dc-dc converter, a high speed PWM IC such as the UC3824 from Unitrode/Texas Instruments may be used. Functionally within this PWM-IC, the control voltage $v_c(t)$ generated by the controller is compared with a ramp signal v_r of amplitude \hat{V}_r , at a constant switching frequency f_s , as shown in Fig. 2-12. The output switching signal represents the transistor switching function $q(t)$,

which equals 1 if $v_c(t) \geq v_r$; otherwise 0. The transistor duty-ratio based on Fig. 2-12 is given as

$$d(t) = \frac{v_c(t)}{\hat{V}_r} \quad (2-8)$$

Thus, the control voltage $v_c(t)$ can provide regulation of the average output voltage of the switching power-pole, as discussed further in Chapters 3 and 4.

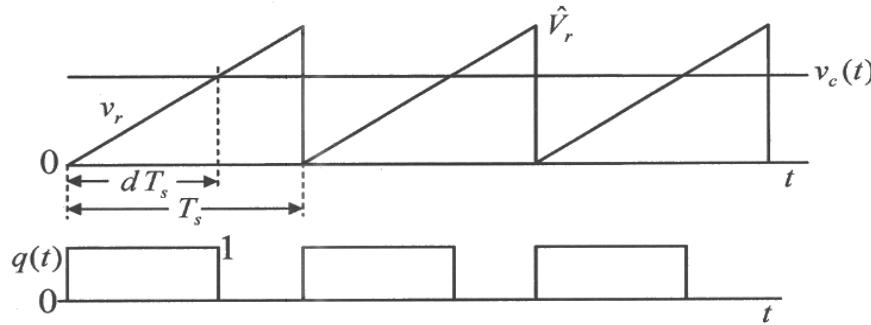


Figure 2-12 PWM IC waveforms.

REFERENCES

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.
2. International Rectifier (<http://www.irf.com>).
3. POWEREX Corporation (<http://www.pwrx.com>).
4. Fuji Semiconductor (<http://www.fujisemiconductor.com>).
5. On Semiconductor (<http://www.onsemiconductor.com>).
6. Infineon Technologies (<http://www.infineon.com>).
7. Panasonic Capacitors (<http://www.panasonic.com/industrial/components/capcitor.htm>).
8. Aavid Corporation for Heat Sinks (<http://www.aavid.com>).
9. Bergquist Company for thermal pads (<http://www.bergquistcompany.com>).
10. Unitrode for PWM Controller ICs (<http://www.unitrode.com>).

PROBLEMS

MOSFET in a Power-Pole of Fig 2-4a

A MOSFET is used in a switching power-pole shown in Fig. 2-4a. Assume the diode ideal. The operating conditions are as follows: $V_{in} = 40V$, $I_o = 5A$, the switching frequency $f_s = 200kHz$, and the duty-ratio $d = 0.3$. Under the operating conditions, the MOSFET has the following switching times: $t_{d(on)} = 100ns$, $t_{ri} = 30ns$, $t_{rf} = 20ns$,

$t_{d(off)} = 50\text{ ns}$, $t_r = 25\text{ ns}$, $t_f = 15\text{ ns}$. The on-state resistance of the MOSFET is $R_{DS(on)} = 20\text{ m}\Omega$. Assume V_{GG} as a step voltage between 0 V and 12 V.

- 2-1 Draw and label the turn-on and turn-off characteristics of the MOSFET and sketch the MOSFET gate-source voltage v_{GS} waveform.
- 2-2 Plot the turn-on and the turn-off switching power losses in the MOSFET. Calculate the average switching power loss in the MOSFET, and the percentage reduction in the converter energy efficiency due to this switching power loss.
- 2-3 Calculate the average conduction loss in the MOSFET.
- 2-4 In stead of an ideal diode, consider that the diode is actual and has a forward voltage drop $V_{FM} = 0.8V$. Calculate the average forward power loss in the diode.
- 2-5 In the diode reverse recovery characteristic shown in Fig. 2A-1, $t_a = 10\text{ ns}$, $t_r = 25\text{ ns}$, and $I_{RRM} = 2\text{ A}$. Calculate the average switching power in the diode.
- 2-6 In the gate-drive circuitry of the MOSFET, assume that the external power supply V_{ext} in Fig. 2-8 has a voltage of 12 V. Each time, to turn the MOSFET *on* under the conditions given requires a charge $Q_g = 45\text{ nC}$. Calculate the average gate-drive power loss.
- 2-7 In this problem, we will calculate new values of the turn-on and the turn-off delay times of the MOSFET, based on the gate driver IC IR2127, as described in section 2-4-4. This IC is supplied with a voltage $V_{ext} = 12V$ with respect to the MOSFET *Source*. Assume this voltage to equal V_{GG} .
 - (a) For the turn-on, assume that this driver IC is a voltage source of V_{GG} with an internal resistance of 60Ω in series. Calculate the turn-on delay time $t_{d(on)}$, assuming that the MOSFET threshold voltage $V_{GS(th)} = 3V$. Assume the MOSFET capacitance to be 1190 pF for this calculation.
 - (b) For turning-off of the MOSFET, assume that this driver IC shorts the MOSFET gate to its source through an internal resistance of 30Ω . Calculate the turn-off delay time $t_{d(off)}$, assuming that the MOSFET voltage $V_{GS(I_o)} = 4.5V$. Assume the MOSFET capacitance to be 1900 pF for this calculation.
- 2-8 In the Buck converter in which this switching power-pole is used, the output filter capacitor consists of a parallel combination of an electrolytic capacitor and a metalized-polyester capacitor. The electrolytic capacitor has the following

measured values: $C = 697 \mu F$, $ESR = 0.037 \Omega$, and $ESL = 16 nH$. The metalized-polyester capacitor has the following measured values: $C = 10 \mu F$, $ESR = 0.04 \Omega$, and $ESL = 34 nH$. Using any computer program, plot the impedance magnitude of each capacitor, and of their parallel combination, on the same log-log plot, as a function of frequency (from 1 kHz to 1 MHz). At $f_s = 200 \text{ kHz}$, what are the relative impedance magnitudes of these two capacitors?

- 2-9 The MOSFET losses are the sum of those computed in Problems 2-2 and 2-3. The junction temperature must not exceed $100^\circ C$, and the ambient temperature is given as $40^\circ C$. From the MOSFET datasheet, $R_{\theta_{jc}} = 1.2^\circ C/W$. The thermal pad has $R_{\theta_{cs}} = 1.8^\circ C/W$. Calculate the maximum value of $R_{\theta_{sa}}$ that the heat sink can have.

APPENDIX 2A DIODE REVERSE RECOVERY AND POWER LOSSES

In this appendix, the diode reverse characteristic is described and the associated power losses are calculated. The increase in the MOSFET turn-on switching loss due to the diode reverse recovery current is discussed in the accompany CD.

2A-1 Average Forward Loss in Diodes

The current flow through a diode results in a forward voltage drop V_{FM} across the diode. The average forward power loss $P_{diode,F}$ in the diode in the circuit of Fig. 2-4a can be calculated as

$$P_{diode,F} = (1 - d) \cdot V_{FM} I_o \quad (2A-1)$$

where d is the MOSFET duty-ratio in the power-pole, and hence the diode conducts for $(1 - d)$ portion of each switching time-period.

2A-2 Diode Reverse Recovery Characteristic

Forward current in power diodes, unlike in Schottky diodes that are majority-carrier devices, is due to the flow of electrons as well as holes. This current results in an accumulation of electrons in the p-region and of holes in the n-region. The presence of these charges allows a flow of current in the negative direction that sweeps away these excess charges, and the negative current quickly comes to zero, as shown in the plot of Fig. 2A-1. The peak reverse recovery current I_{RRM} and the reverse recovery charge Q_{rr} shown in Fig. 2A-1 depend on the initial forward current I_o and the rate di/dt at which this current decreases.

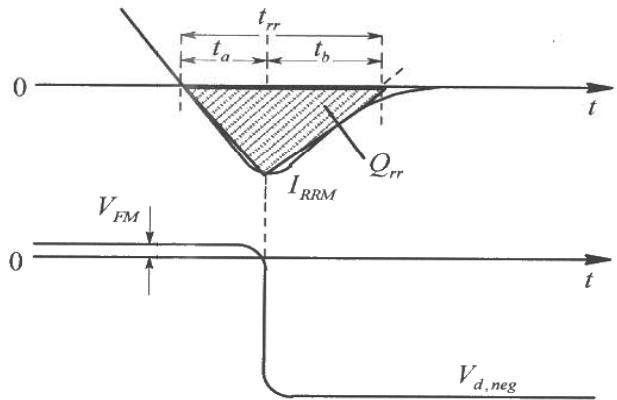


Figure 2A-1 Diode reverse recovery characteristic.

2A-3 Diode Switching Losses

The reverse recovery current results in switching losses within the diode when a negative current is flowing beyond the interval t_a in Fig. 2A-1, while the diode is blocking a negative voltage $V_{d,neg}$. This switching power loss in the diode can be estimated from the plots of Fig. 2A-1 as

$$P_{diode,sw} = \left(\frac{1}{2} I_{RRM} t_b \right) \cdot V_{d,neg} \cdot f_s \quad (2A-2)$$

where f_s is the switching frequency. In switch-mode power electronics, increase in switching losses due to the diode reverse recovery can be significant, and diodes with ultra-fast reverse recovery characteristics are needed to avoid these from becoming excessive.

The reverse recovery current of the diode also increases the turn-on losses in the associated MOSFET of the power-pole, as discussed in the accompanying CD.

Chapter 3

SWITCH-MODE DC-DC CONVERTERS: SWITCHING ANALYSIS, TOPOLOGY SELECTION AND DESIGN

3-1 DC-DC CONVERTERS [1]

In Chapter 1, we discussed the need for Buck, Boost, and Buck-Boost dc-dc converters, shown by the block diagram of Fig. 3-1a, and how the pulse-width modulation process regulates the output voltage. The design of the feedback controller is the subject of the next chapter. The power flow through these converters is in only one direction, thus their voltages and currents remain unipolar and unidirectional, as shown in Fig. 3-1b. Based on these converters, several transformer-isolated dc-dc converter topologies, which are used in all types of electronics equipment, are discussed in Chapter 8.

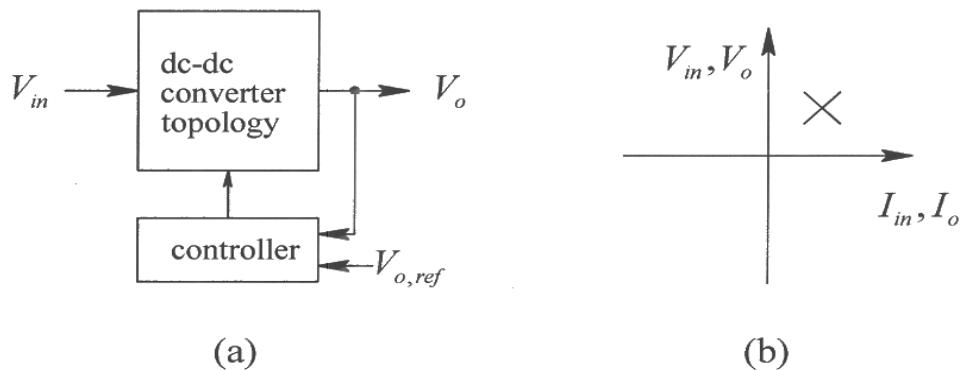


Figure 3-1 Regulated switch-mode dc power supplies.

3-2 SWITCHING POWER-POLE IN DC STEADY STATE

All the converters that we will discuss consist of a switching power-pole that was introduced in Chapter 1, and is redrawn in Fig. 3-2a. In these converter circuits in dc steady state, the input voltage and the output load are assumed constant. The switching power-pole operates with a transistor switching function $q(t)$, whose waveform repeats, unchanged from one cycle to the next, and the corresponding switch duty-ratio remains constant at its dc steady state value D . Therefore, all waveforms associated with the power-pole repeat with the switching time-period T_s in the dc steady state, where the basic principles described below are extremely useful for analysis purposes.

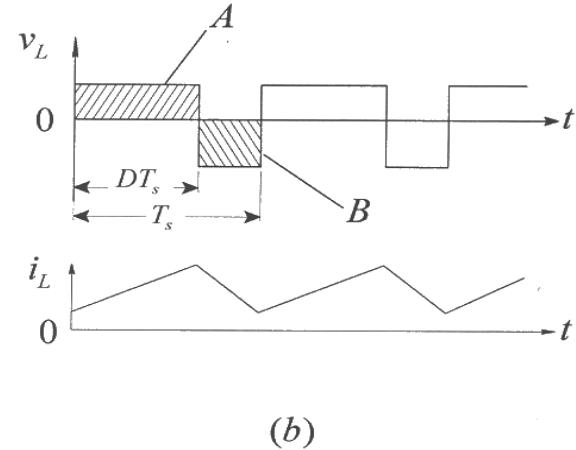
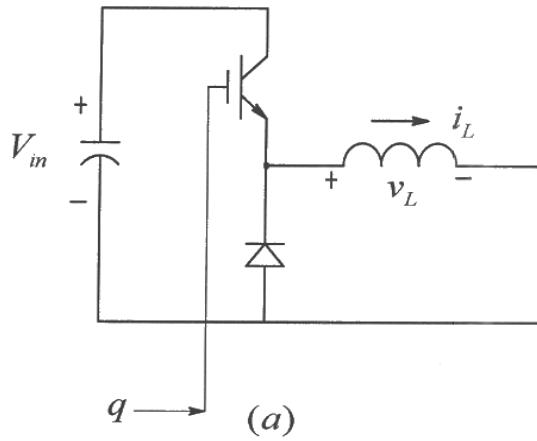


Figure 3-2 Switching power-pole as the building block of dc-dc converters.

First, let us consider the voltage and current of the inductor associated with the power-pole. The inductor current depends on the pulsating voltage waveform shown in Fig. 3-2b. The inductor voltage and current are related by the conventional differential equation, which can be expressed in the integral form as follows:

$$v_L = L \frac{di_L}{dt} \quad \Rightarrow \quad i_L(t) = \frac{1}{L} \int_{\tau} v_L \cdot d\tau \quad (3-1)$$

where τ , representing time, is a variable of integration. For simplicity, we will consider the first time-period starting with $t = 0$ in Fig. 3-2b. Using the integral form in Eq. 3-1, the inductor current at a time t can be expressed in terms of its initial value $i_L(0)$ as:

$$i_L(t) = i_L(0) + \frac{1}{L} \int_0^t v_L \cdot d\tau \quad (3-2)$$

In the dc steady state, the waveforms of all circuit variables must repeat with the switching frequency time-period T_s , resulting in the following conclusions from Eq. 3-2:

1. The inductor current waveforms repeats with T_s , and therefore in Eq. 3-2

$$i_L(T_s) = i_L(0) \quad (3-3)$$

2. Integrating over one switching time-period T_s in Eq. 3-2 and using Eq. 3-3 show that the inductor voltage integral over T_s is zero. This leads to the conclusion that the average inductor voltage, averaged over T_s , is zero:

$$\frac{1}{L} \int_0^{T_s} v_L \cdot d\tau = 0 \quad \Rightarrow \quad V_L = \frac{1}{T_s} \left(\underbrace{\int_0^{DT_s} v_L \cdot d\tau}_{\text{area } A} + \underbrace{\int_{DT_s}^{T_s} v_L \cdot d\tau}_{\text{area } B} \right) = 0 \quad (3-4)$$

In Fig. 3-2a, the area A in volt-s, that causes the current to rise, equals in magnitude the negative area B that causes the current to decline to its initial value.

The above analysis applies to any inductor in a switch-mode converter circuit operating in a dc steady state. By analogy, a similar analysis applies to any capacitor in a switch-mode converter circuit, operating in the dc steady state, as follows: the capacitor voltage and current are related by the conventional differential equation, which can be expressed in the integral form as follows:

$$i_C = C \frac{dv_C}{dt} \quad \Rightarrow \quad v_C(t) = \frac{1}{C} \int_{\tau} i_C \cdot d\tau \quad (3-5)$$

where τ , representing time, is a variable of integration. Using the integral form of Eq. 3-5, the capacitor voltage at a time t can be expressed in terms of its initial value $v_C(0)$ as:

$$v_C(t) = v_C(0) + \frac{1}{C} \int_0^t i_C \cdot d\tau \quad (3-6)$$

In the dc steady state, the waveforms of all circuit variables must repeat with the switching frequency time-period T_s , resulting in the following conclusions from Eq. 3-6:

1. The capacitor voltage waveform repeats with T_s , and therefore in Eq. 3-6

$$v_C(T_s) = v_C(0) \quad (3-7)$$

2. Integrating over one switching time-period T_s in Eq. 3-6 and using Eq. 3-7 show that the capacitor current integral over T_s is zero, which leads to the conclusion that the average capacitor current, averaged over T_s , is zero:

$$\frac{1}{C} \int_0^{T_s} i_C \cdot d\tau = 0 \quad \Rightarrow \quad I_C = \frac{1}{T_s} \int_0^{T_s} i_C \cdot d\tau = 0 \quad (3-8)$$

In addition to the above two conclusions, it is important to recognize that in dc steady state, just like for instantaneous quantities, the Kirchhoff's voltage and current laws apply to average quantities as well. In the dc steady state, average voltages sum to zero in a circuit loop, and average currents sum to zero at a node:

$$\sum_k V_k = 0 \quad (3-9)$$

$$\sum_k I_k = 0 \quad (3-10)$$

3-3 SIMPLIFYING ASSUMPTIONS

To gain a clear understanding in the dc steady state, we will first make certain simplifying assumptions by ignoring the second-order effects listed below, and later on include them for accuracy:

1. Transistors, diodes and other passive components are all ideal unless explicitly stated. For example, we will ignore the inductor equivalent series resistance.
2. The input is a pure dc voltage V_{in} .
3. Design specifications require the ripple in the output voltage to be very small. Therefore, we will initially assume that the output voltage is purely dc without any ripple, that is $v_o(t) \approx V_o$, and later calculate the ripple in it.
4. The current at the current-port of the power-pole through the series inductor flows continuously, resulting in a continuous conduction mode, CCM (the discontinuous conduction mode, DCM, is analyzed later on).

It is, of course possible to analyze a switching circuit in detail, without making the above simplifying assumptions as we will do in computer simulations. However, the two-step approach followed here, where the analysis is first carried out by neglecting the second-order effects and adding them later on, provides a deeper insight into converter operation and the design tradeoffs.

3-4 COMMON OPERATING PRINCIPLES

In all three converters that we will analyze, the inductor associated with the switching power-pole acts as an energy transfer means from the input to the output. Turning on the transistor of the power-pole increases the inductor energy by a certain amount, drawn from the input source, which is transferred to the output stage during the off-interval of the transistor. In addition to this inductive energy-transfer means, depending on the converter, there may be additional energy transfer directly from the input to the output, as discussed in the following sections.

3-5 BUCK CONVERTER SWITCHING ANALYSIS IN DC STEADY STATE

A Buck converter is shown in Fig. 3-3a, with the transistor and the diode making up the bi-positional switch of the power-pole. The equivalent series resistance (ESR) of the capacitor will be ignored. Turning on the transistor increases the inductor current in the sub-circuit of Fig. 3-3b. When the transistor is turned off, the inductor current “freewheels” through the diode, as shown in Fig. 3-3c.

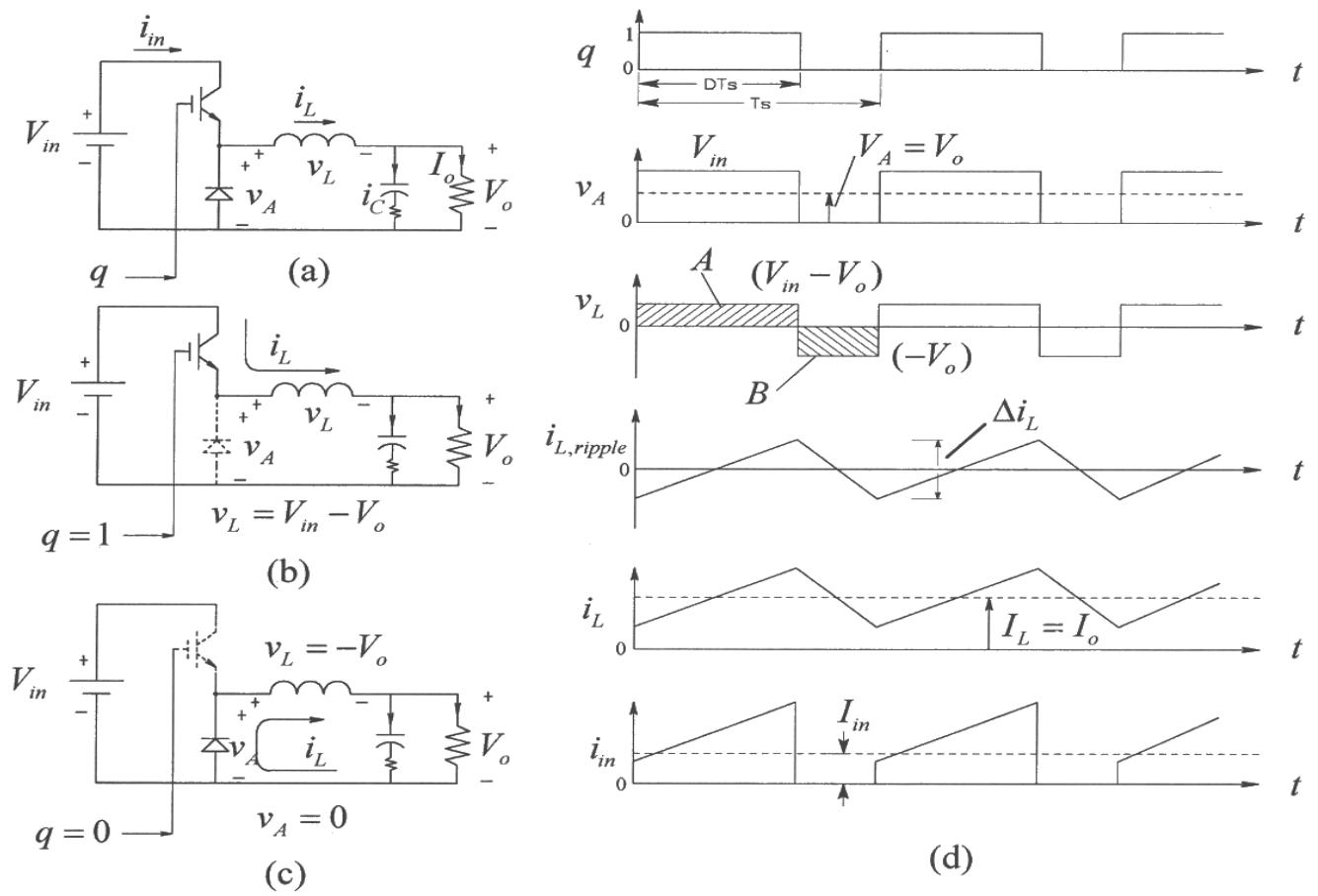


Figure 3-3 Buck dc-dc converter.

For a given transistor switching function waveform $q(t)$ shown in Fig. 3-3d with a switch duty-ratio D in steady state, the waveform of the voltage v_A at the current-port follows $q(t)$ as shown. In Fig. 3-3d, integrating v_A over T_s , the average voltage V_A equals DV_{in} . Recognizing that the average inductor voltage is zero (Eq. 3-4) and the average voltages in the output loop sum to zero (Eq. 3-9),

$$V_o = V_A = DV_{in} \quad (3-11)$$

The inductor voltage v_L pulsates between two values, $(V_{in} - V_o)$ and $(-V_o)$ as plotted in Fig. 3-3d. Since the average inductor voltage is zero, the volt-second areas during two sub-intervals are equal in magnitude and opposite in sign. In dc steady state, the inductor current can be expressed as the sum of its average and the ripple component:

$$i_L(t) = I_L + i_{L,ripple}(t) \quad (3-12)$$

where the average current depends on the output load, and the ripple component is dictated by the waveform of the inductor voltage v_L in Fig. 3-3d. As shown in Fig. 3-3d, the ripple component consists of linear segments, rising when v_L is positive and falling

when v_L is negative. The peak-peak ripple can be calculated as follows, using either area A or B:

$$\Delta i_L = \frac{1}{L} \underbrace{(V_{in} - V_o)DT_s}_{\text{Area A}} = \frac{1}{L} \underbrace{V_o(1-D)T_s}_{\text{Area B}} \quad (3-13)$$

This ripple component is plotted in Fig. 3-3d. Since the average capacitor current is zero in dc steady state, the average inductor current equals the output load current by the Kirchhoff's current law applied at the output node:

$$I_L = I_o = \frac{V_o}{R} \quad (3-14)$$

The inductor current waveform is shown in Fig. 3-3d by superposing the average and the ripple components.

Next, we will calculate the ripple current through the output capacitor. In practice, the filter capacitor is large to achieve the output voltage nearly dc ($v_o(t) \approx V_o$). Therefore, to the ripple-frequency current, the path through the capacitor offers much smaller impedance than through the load resistance, hence justifying the assumption that the ripple component of the inductor current flows entirely through the capacitor. That is, in Fig. 3-3a

$$i_C(t) \approx i_{L,ripple}(t) \quad (3-15)$$

In practice, the voltage drops across the capacitor ESR and the ESL dominate over the voltage drop $\frac{1}{C} \int i_C dt$ across C. The capacitor current i_C , equal to $i_{L,ripple}$ in Fig. 3-3d, can be used to calculate the ripple in the output voltage.

The input current i_{in} pulsates, equal to i_L when the transistor is on, otherwise zero, as plotted in Fig. 3-3d. An input L-C filter is often needed to prevent the pulsating current from being drawn from the input dc source. The average value of the input current in Fig. 3-3d is

$$I_{in} = DI_L = DI_o \quad (\text{using Eq. 3-14}) \quad (3-16)$$

Using Eqs. 3-11 and 3-16, we can confirm that the input power equals the output power, as it should, in this idealized converter:

$$V_{in}I_{in} = V_oI_o \quad (3-17)$$

Eq. 3-11 shows that the voltage conversion ratio of Buck converters in the continuous conduction mode (CCM) depends on D, but is independent of the output load. If the

output load decreases (that is, if the load resistance increases) to the extent that the inductor current becomes discontinuous, then the input-output relationship in CCM is no longer valid, and, if the duty-ratio D were to be held constant, the output voltage in the discontinuous-conduction mode would rise above that given by Eq. 3-11. The discontinuous conduction mode will be considered fully in section 3-15 and in the Appendix to this chapter.

3-6 BOOST CONVERTER SWITCHING ANALYSIS IN DC STEADY STATE

A Boost converter is shown in Fig. 3-4a. Compared to a Buck converter, it has two major differences:

1. Power flow is from a lower voltage dc input to the higher load voltage, in the opposite direction through the switching power-pole. Hence, the current direction through the series inductor of the power pole is chosen as shown, opposite to that in a Buck converter, and this current remains positive in the continuous conduction mode.
2. In the switching power-pole, the bi-positional switch is realized using a transistor and a diode that are placed as shown in Fig. 3-4a. Across the output, a filter capacitor C is placed, which forms the voltage port and minimizes the output ripple voltage.

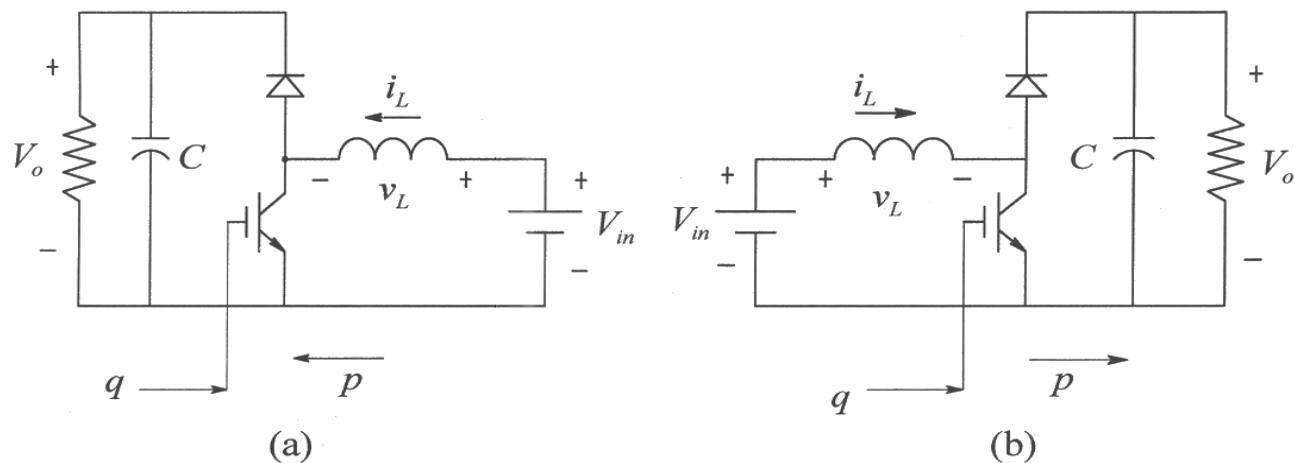


Figure 3-4 Boost dc-dc converter.

It is conventional to show power flow from the left to the right side. To follow this convention, the circuit of Fig. 3-4a is flipped and drawn in Fig. 3-4b. The output stage consists of the output load and a large filter capacitor that is used to minimize the output voltage ripple. This capacitor at the output initially gets charged to a voltage equal to V_{in} through the diode.

In a Boost converter, turning on the transistor in the bottom position applies the input voltage across the inductor such that v_L equals V_{in} , as shown in Fig. 3-5a, and i_L linearly ramps up, increasing the energy in the inductor. Turning off the transistor forces the inductor current to flow through the diode as shown in Fig. 3-5b, and some of the inductively stored energy is transferred to the output stage that consists of the filter capacitor and the output load across it.

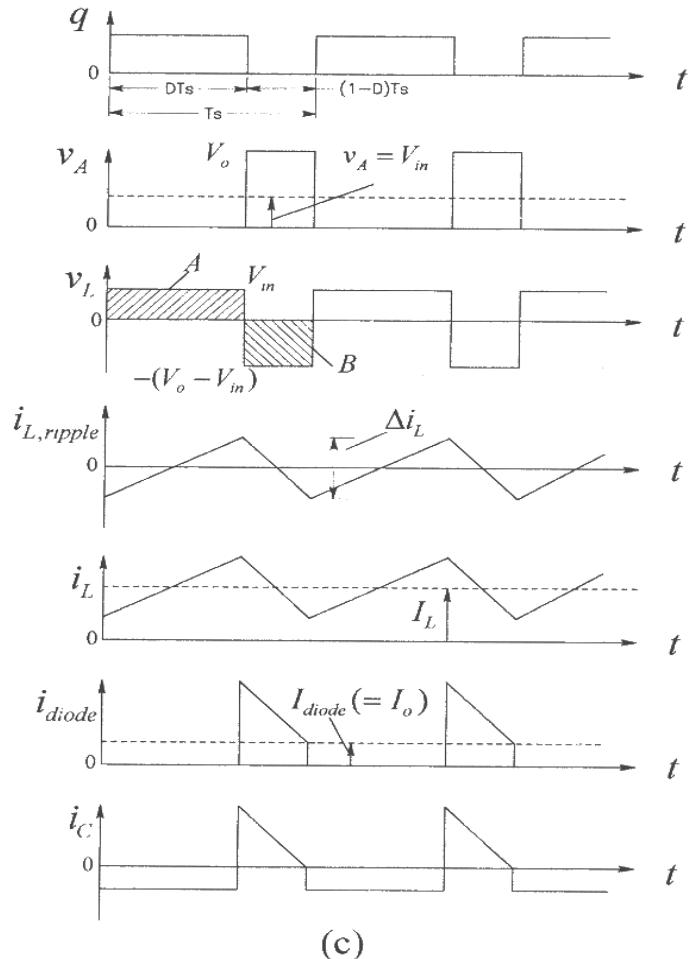
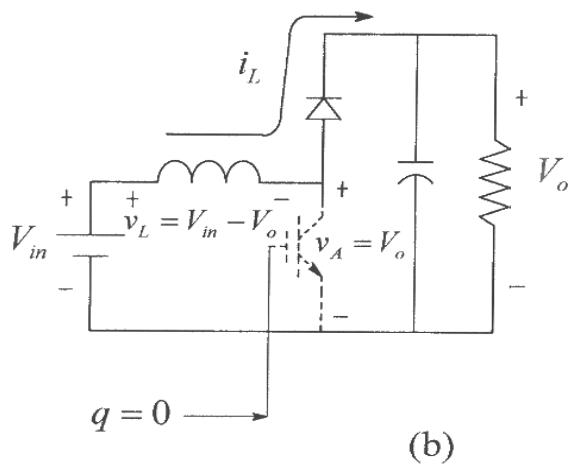
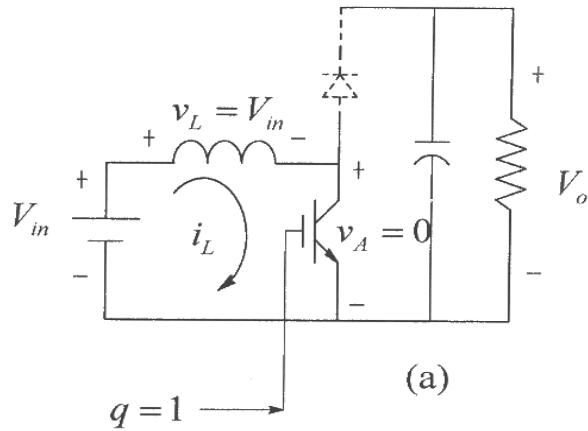


Figure 3-5 Boost converter: operation and waveforms.

The transistor switching function is shown in Fig. 3-5c, with a steady state duty-ratio D . Because of the transistor in the bottom position in the power-pole, the resulting v_A waveform is as plotted in Fig. 3-5c. Since the average voltage across the inductor in the dc steady state is zero, the average voltage V_A equals the input voltage V_{in} . The inductor voltage v_L pulsates between two values: V_{in} and $-(V_o - V_{in})$ as plotted in Fig. 3-5c. Since the average inductor voltage is zero, the volt-second areas during the two sub-intervals are equal in magnitude and opposite in sign.

The input/output voltage ratio can be obtained either by the waveform of v_A or v_L in Fig. 3-5c. Using the inductor voltage waveform whose average is zero in dc steady state,

$$V_{in}(DT_s) = (V_o - V_{in})(1 - D)T_s \quad (3-18)$$

Hence,

$$\frac{V_o}{V_{in}} = \frac{1}{1 - D} \quad (V_o > V_{in}) \quad (3-19)$$

The inductor current waveform consists of its average value, which depends on the output load, and a ripple component that depends on v_L :

$$i_L(t) = I_L + i_{L,ripple}(t) \quad (3-20)$$

where as shown in Fig. 3-5c, $i_{L,ripple} \left(= \frac{1}{L} \int v_L \cdot d\tau \right)$, whose average value is zero, consists of linear segments, rising when v_L is positive and falling when v_L is negative. The peak-peak ripple can be calculated by using either area A or B :

$$\Delta i_L = \frac{1}{L} \underbrace{V_{in}(DT_s)}_{\text{Area A}} = \frac{1}{L} \underbrace{(V_o - V_{in})(1 - D)T_s}_{\text{Area B}} \quad (3-21)$$

In a Boost converter, the inductor current equals the input current, whose average can be calculated from the output load current by equating the input and the output powers:

$$V_{in}I_{in} = V_oI_o \quad (3-22)$$

Hence, using Eq. 3-19 and $I_o = V_o/R$,

$$I_L = I_{in} = \frac{V_o}{V_{in}}I_o = \frac{I_o}{1 - D} = \frac{1}{1 - D} \frac{V_o}{R} \quad (3-23)$$

The inductor current waveform is shown in Fig. 3-5c, superposing its average and the ripple components.

The current through the diode equals 0 when the transistor is on, otherwise it equals i_L , as plotted in Fig. 3-5c. In the dc steady state, the average capacitor current I_C is zero and therefore the average diode current equals the output current I_o . In practice, the filter capacitor is large to achieve the output voltage nearly dc ($v_o(t) \approx V_o$). Therefore, to the ripple-frequency component in the diode current, the path through the capacitor offers much smaller impedance than through the load resistance, hence justifies the assumption

that the ripple component of the diode current flows entirely through the capacitor. That is,

$$i_C(t) \approx i_{diode,ripple}(t) = i_{diode} - I_o \quad (3-24)$$

In practice, the voltage drops across the capacitor ESR and the ESL dominate over the voltage drop $\frac{1}{C} \int i_C dt$ across C. The plot of i_C in Fig. 3-5c can be used to calculate the ripple in the output voltage.

The above analysis shows that voltage conversion ratio (Eq. 3-19) of Boost converters in CCM depends on $1/(1-D)$, and is independent of the output load, as shown in Fig. 3-6. If the output load decreases to the extent that the inductor current becomes discontinuous below a critical value $I_{L,crit}$, the input-output relationship of CCM is no longer valid in DCM. If the duty-ratio D were to be held constant as shown in Fig. 3-6, the output voltage could rise to dangerously high levels in DCM, considered fully in section 3-15 and the Appendix to this chapter.

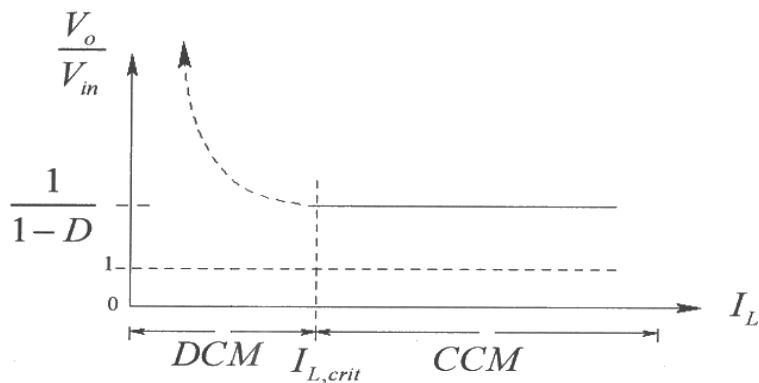


Figure 3-6 Boost converter: voltage transfer ratio.

3-7 BUCK-BOOST CONVERTER ANALYSIS IN DC STEADY STATE

Buck-Boost converters allow the output voltage to be greater or lower than the input voltage based on the switch duty-ratio D . A Buck-Boost converter is shown in Fig. 3-7a, where the switching power-pole is implemented as shown. Conventionally, to make the power flow from left to the right, the Buck-Boost converter is drawn as shown in Fig. 3-7b.

As shown in Fig. 3-8a, turning on the transistor applies the input voltage across the inductor such that v_L equals V_{in} , and the current linearly ramps up, increasing the energy in the inductor. Turning off the transistor results in the inductor current flowing through the diode, as shown in Fig. 3-8b, transferring energy increase in the inductor during the previous transistor state to the output.

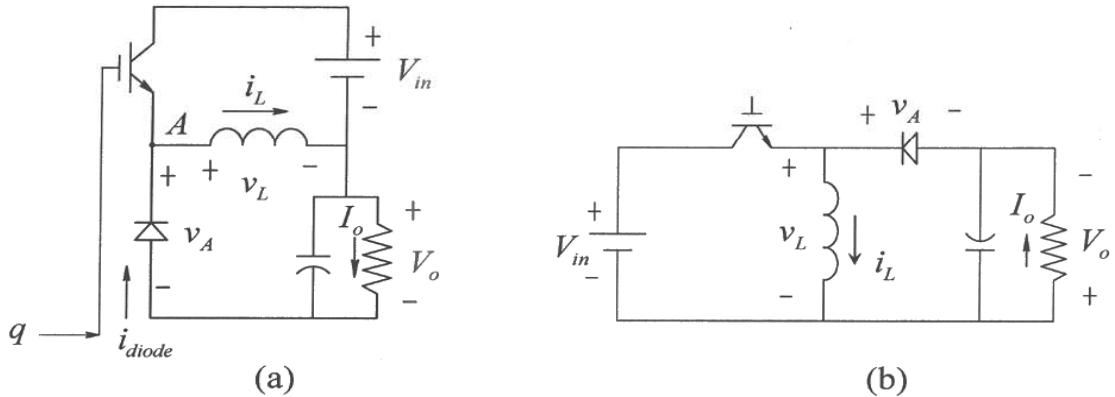


Figure 3-7 Buck-Boost dc-dc converter.

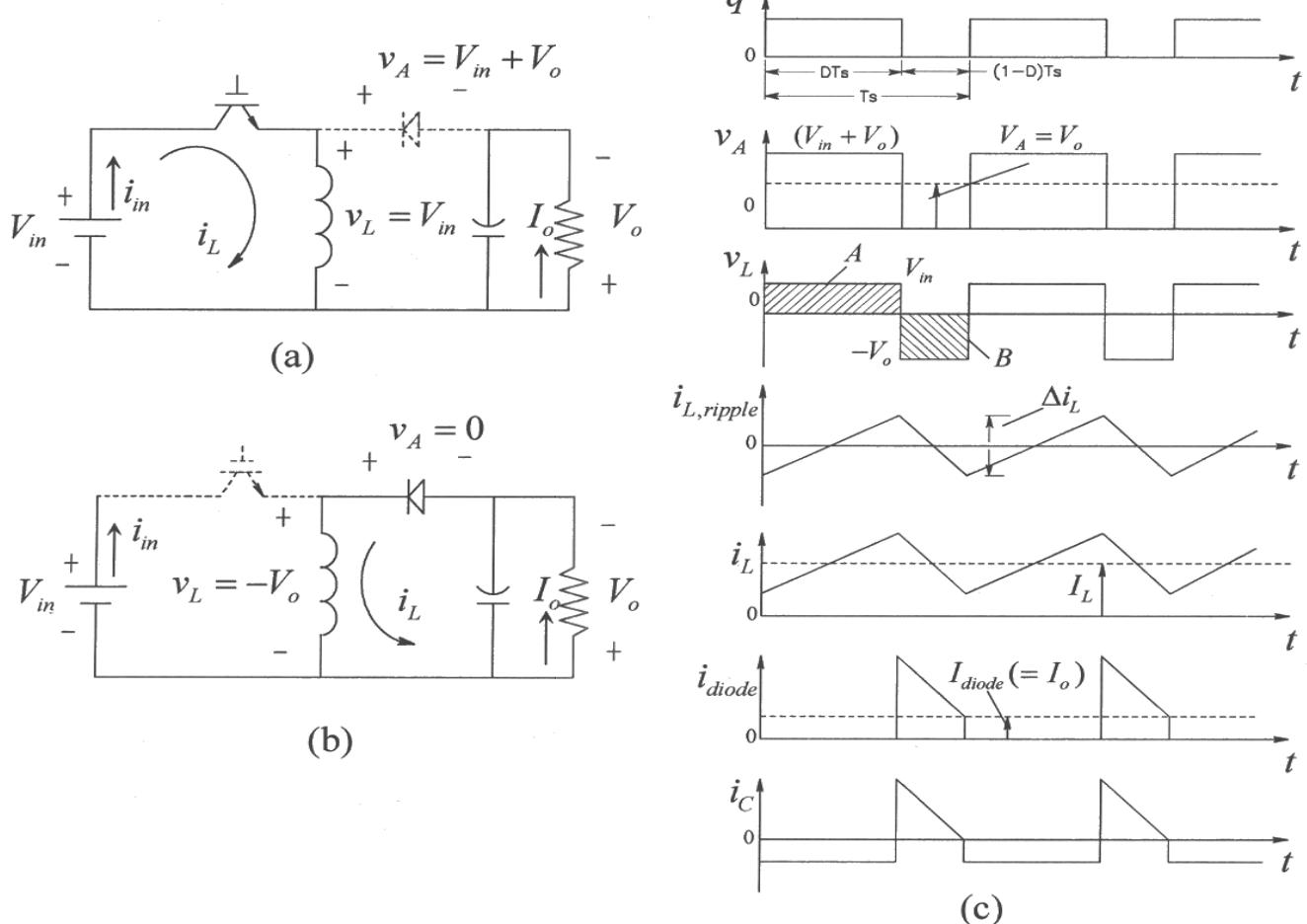


Figure 3-8 Buck-Boost converter: operation and waveforms.

The transistor switching function is shown in Fig. 3-8c, with a steady state duty-ratio D . The resulting v_A waveform is as plotted. Since the average voltage across the inductor in the dc steady state is zero, the average V_A equals the output voltage. The inductor voltage pulsates between two values: V_{in} and $-V_o$, as plotted in Fig. 3-8c. Since the

average inductor voltage is zero, the volt-second areas during the two sub-intervals are equal in magnitude and opposite in sign.

The input/output voltage ratio can be obtained either by the waveform of v_A or v_L in Fig. 3-8c. Using the v_L waveform whose average is zero in the dc steady state,

$$DV_{in} = (1 - D)V_o \quad (3-25)$$

Hence,

$$\frac{V_o}{V_{in}} = \frac{D}{1 - D} \quad (3-26)$$

The inductor current consists of an average value, which depends on the output load, and a ripple component that depends on v_L :

$$i_L(t) = I_L + i_{L,ripple}(t) \quad (3-27)$$

where as shown in Fig. 3-8b, $i_{L,ripple} \left(= \frac{1}{L} \int v_L \cdot d\tau \right)$, whose average value is zero, consists of linear segments, rising when v_L is positive and falling when v_L is negative. The peak-peak ripple can be calculated by using either area A or B

$$\Delta i_L = \frac{1}{L} \underbrace{V_{in} (DT_s)}_{\text{Area A}} = \frac{1}{L} \underbrace{V_o (1 - D) T_s}_{\text{Area B}} \quad (3-28)$$

Applying the Kirchhoff's current law in Fig. 3-7a or b, the average inductor current equals the sum of the average input current and the average output current (note that the average capacitor current is zero in dc steady state)

$$I_L = I_{in} + I_o \quad (3-29)$$

Equating the input and the output powers

$$V_{in} I_{in} = V_o I_o \quad (3-30)$$

and using Eq. 3-26

$$I_{in} = \frac{V_o}{V_{in}} I_o = \frac{D}{1 - D} I_o \quad (3-31)$$

Hence, using Eqs. 3-29 and 3-31,

$$I_L = I_{in} + I_o = \frac{1}{1 - D} I_o = \frac{1}{1 - D} \frac{V_o}{R} \quad (3-32)$$

Superposing the average and the ripple components, the inductor current waveform is shown in Fig. 3-8c.

The diode current is zero, except when it conducts the inductor current, as plotted in Fig. 3-8c. In the dc steady state, the average current I_C through the capacitor is zero, and therefore by the Kirchhoff's current law, the average diode current equals the output current. In practice, the filter capacitor is large to achieve the output voltage nearly dc ($v_o(t) \approx V_o$). Therefore, to the ripple-frequency current, the path through the capacitor offers much smaller impedance than through the load resistance, hence justifies the assumption that the ripple component of the diode current flows entirely through the capacitor. That is,

$$i_C(t) \approx i_{\text{diode,ripple}}(t) \quad (3-33)$$

In practice, the voltage drops across the capacitor ESR and the ESL dominate over the voltage drop $\frac{1}{C} \int i_C dt$ across C. The plot of i_C in Fig. 3-8c can be used to calculate the ripple in the output voltage.

The above analysis shows that the voltage conversion ratio (Eq. 3-26) of Buck-Boost converters in CCM depends on $D/(1-D)$, and is independent of the output load, as shown in Fig. 3-9. If the output load decreases to the extent that the inductor current becomes discontinuous below a critical value $I_{L,\text{crit}}$, the input-output relationship in CCM is no longer valid in DCM. If the duty-ratio D were to be held constant as shown in Fig. 3-9, the output voltage could rise to dangerously high levels in DCM, considered fully in section 3-15 and the Appendix to this chapter.

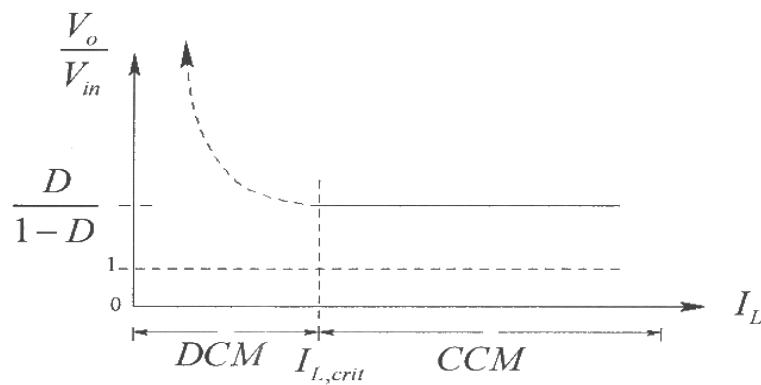


Figure 3-9 Buck-Boost converter: voltage transfer ratio.

3-7-1 Other Buck-Boost Topologies

There are two variations of the Buck-Boost topology, which are used in certain applications. These two topologies are briefly described below.

3-7-1-1 SEPIC Converters (Single-Ended Primary Inductor Converters)

The SEPIC converter shown in Fig. 3-10a is used in certain applications where the current drawn from the input is required to be relatively ripple-free. By applying the Kirchhoff's voltage law and the fact that average inductor voltage is zero in the dc steady state, the capacitor in this converter gets charged to an average value that equals the input voltage V_{in} with the polarity shown. During the on-interval of the transistor, DT_s , as shown in Fig. 3-10b, the diode gets reverse biased by the sum of the capacitor and the output voltages, and i_{L1} and i_{L2} flow through the transistor. During the off-interval $(1-D)T_s$, i_{L1} and i_{L2} flow through the diode, as shown in Fig. 3-10c. The voltage across L_2 equals v_C during the on-interval, and equals $(-V_o)$ during the off-interval. In terms of the average value of the capacitor voltage that equals V_{in} (by applying Eq. 3-9 in Fig. 3-10a), equating the average voltage across L_2 to zero results in

$$DV_{in} = (1-D)V_o \quad (3-34)$$

or,

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \quad (3-35)$$

Unlike the Buck-Boost converters, the output voltage polarity in SEPIC converter remains the same as that of the input.

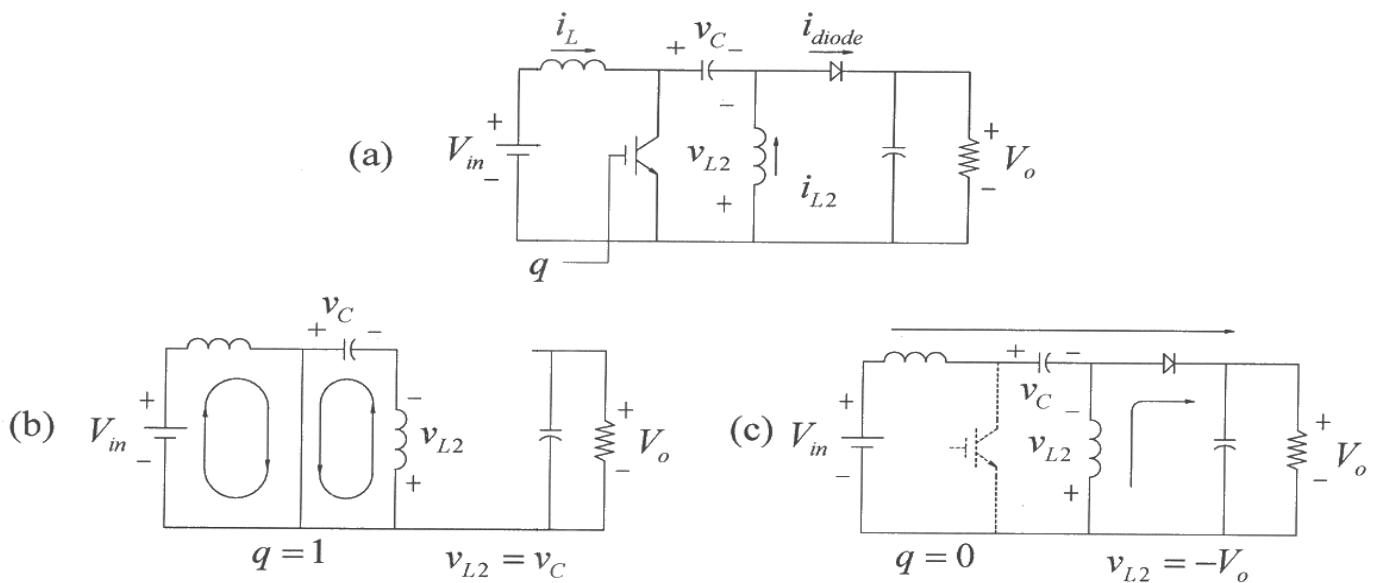


Figure 3-10 SEPIC converter.

3-7-1-2 Cuk Converter

Named after its inventor, the Cuk converter is as shown in Fig. 3-11a, where the energy transfer means is through the capacitor C between the two inductors. Using Eq. 3-9 in Fig. 3-11a, this capacitor voltage has an average value of $(V_{in} + V_o)$ with the polarity shown. During the on-interval of the transistor, DT_s , as shown in Fig. 3-11b, the diode gets reverse biased by the capacitor voltage and the input and the output currents flow through the transistor. During the off-interval $(1 - D)T_s$, the input and the output currents flow through the diode, as shown in Fig. 3-11c. In terms of the average values of the inductor currents, equating the net change in charge on the capacitor over T_s to zero in steady state,

$$DI_o = (1 - D)I_{in} \quad (3-36)$$

or

$$\frac{I_{in}}{I_o} = \frac{D}{1 - D} \quad (3-37)$$

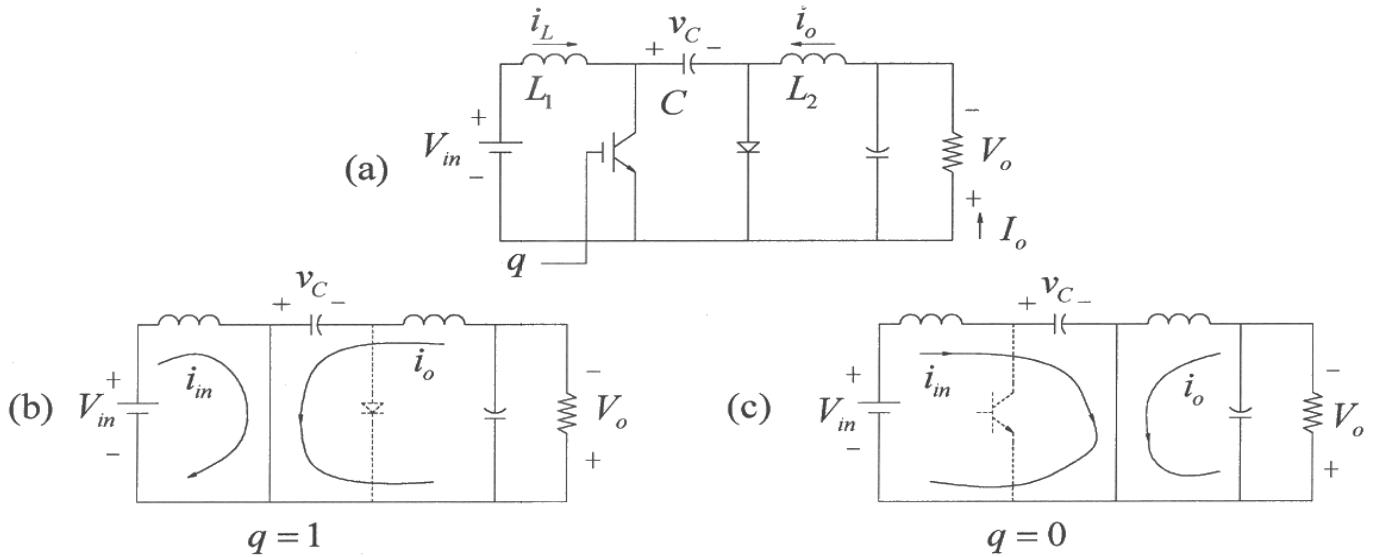


Figure 3-11 Cuk converter.

Equating input and output powers in this idealized converter leads to

$$\frac{V_o}{V_{in}} = \frac{D}{1 - D} \quad (3-38)$$

which shows the same functionality as Buck-Boost converters. One of the advantages of the Cuk converter is that it has non-pulsating currents at the input and the output but it

suffers from the same component stress disadvantages as the Buck-Boost converters and produces an output voltage of the polarity opposite to that of the input.

3-8 TOPOLOGY SELECTION [2]

For selecting between the three converter topologies discussed in this chapter, the stresses listed in Table 3-1 can be compared, which are based on the assumption that the inductor ripple current is negligible.

Table 3-1 Topology Selection Criteria

Criterion		Buck	Boost	Buck-Boost
Transistor \hat{V}		V_{in}	V_o	$(V_{in} + V_o)$
Transistor \hat{I}		I_o	I_{in}	$I_{in} + I_o$
I_{rms}	Transistor	$\sqrt{DI_o}$	$\sqrt{DI_{in}}$	$\sqrt{D}(I_{in} + I_o)$
I_{avg}	Transistor	DI_o	DI_{in}	$D(I_{in} + I_o)$
	Diode	$(1-D)I_o$	$(1-D)I_{in}$	$(1-D)(I_{in} + I_o)$
I_L		I_o	I_{in}	$I_{in} + I_o$
Effect of L on C		significant	little	little
Pulsating Current		input	output	both

From the above table, we can clearly conclude that the Buck-Boost converter suffers from several additional stresses. Therefore, it should be used only if both the Buck and the Boost capabilities are needed. Otherwise, the Buck or the Boost converter should be used based on the desired capability. A detailed analysis is carried out in [2].

3-9 WORST-CASE DESIGN

The worst-case design should consider the ranges in which the input voltage and the output load vary. As mentioned earlier, often converters above a few tens of watts are designed to operate in CCM. To ensure CCM even under very light load conditions would require prohibitively large inductance. Hence, the inductance value chosen is often no larger than three times the critical inductance ($L < 3L_c$), where, as discussed in section 3-15, the critical inductance L_c is the value of the inductor that will make the converter operate at the border of CCM and DCM at full-load.

3-10 SYNCHRONOUS-RECTIFIED BUCK CONVERTER FOR VERY LOW OUTPUT VOLTAGES [3]

Operating voltages in computing and communication equipment have already dropped to an order of 1 V and even lower voltages, such as 0.5 V, are predicted in the near future.

At these low voltages, the diode (even a Schottky diode) of the power-pole in a Buck converter has unacceptably high voltage drop across it in comparison to the output voltage, resulting in extremely poor converter efficiency.

As a solution to this problem, the switching power-pole in a Buck converter is implemented using two MOSFETs, as shown in Fig. 3-12a, which are available with very low $R_{DS(on)}$ in low voltage ratings. The two MOSFETs are driven by almost complimentary gate signals (some delay time, where both signals are low is necessary to avoid the shoot-through of current through the two transistors), as shown in Fig. 3-12b. When the upper MOSFET is off, the inductor current flows through the channel, from the source to the drain, of the lower MOSFET that has gate voltage applied to it. This results in a very low voltage drop across the lower MOSFET. At light load conditions, the inductor current may be allowed to become negative without becoming discontinuous, flowing from the drain to the source of the lower MOSFET [3].

It is possible to achieve soft-switching in such converters, as discussed in Chapter 10, where the ripple in the total output and the input currents can be minimized by interleaving which is discussed in the next section.

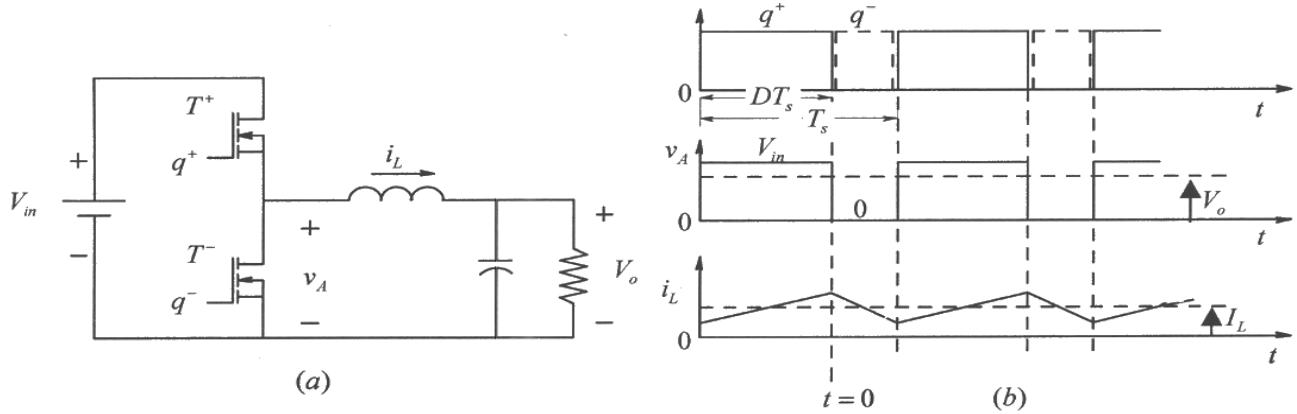


Figure 3-12 Buck converter: synchronous rectified.

3-11 INTERLEAVING OF CONVERTERS [4]

Fig. 3-13a shows two interleaved converters whose switching waveforms are phase shifted by $T_s/2$, as shown in Fig. 3-13b. In general, n such converters can be used, their operation phase shifted by T_s/n . The advantage of such interleaved multi-phase converters is the cancellation of ripple in the input and the output currents to a large degree [4]. This is also a good way to achieve higher control bandwidth.

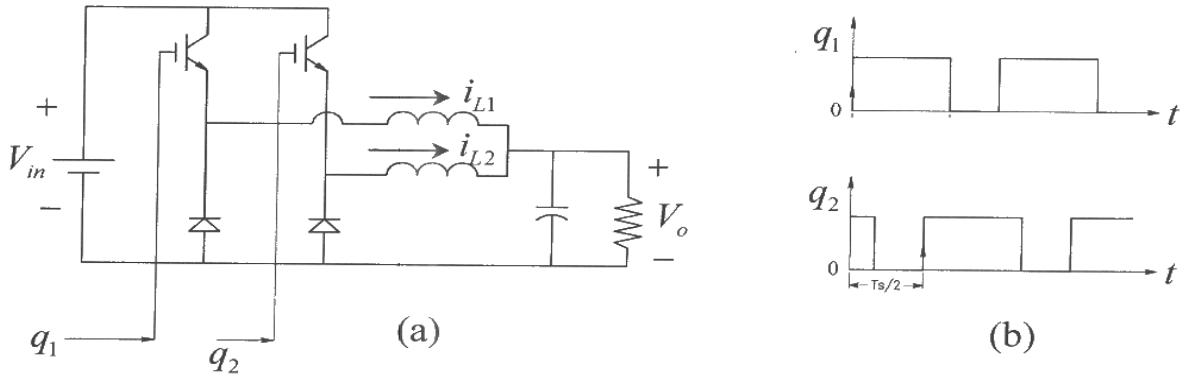


Figure 3-13 Interleaving of converters.

3-12 REGULATION OF DC-DC CONVERTERS BY PWM

Almost all dc-dc converters are operated with their output voltages regulated to equal their reference values within a specified tolerance band (for example, $\pm 1\%$ around its nominal value) in response to disturbances in the input voltage and the output load. The average output of the switching power-pole in a dc-dc converter can be controlled by pulsed-width-modulating (PWM) the duty-ratio $d(t)$ of this power-pole. Fig. 3-14a shows in a block-diagram form of a regulated dc-dc converter. It shows that the converter output voltage is measured and compared with its reference value within a PWM controller IC [5], briefly described in Chapter 2. The error between the two voltages is amplified by an amplifier, whose output is the control voltage $v_c(t)$.

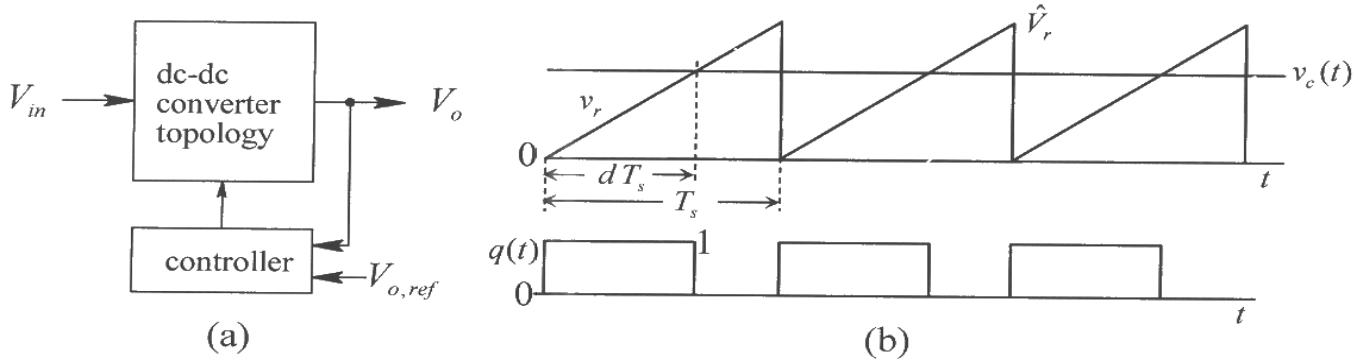


Figure 3-14 Regulation of output by PWM.

Within the PWM-IC [5], the control voltage is compared with a ramp signal $v_r(t)$ as shown in Fig. 3-14b, where the comparator output represents the switching function $q(t)$ whose pulse-width $d(t)$ can be modulated to regulate the output of the converter. The ramp signal v_r has the amplitude \hat{V}_r , and the switching frequency f_s constant. The output voltage of this comparator represents the transistor switching function $q(t)$, which equals 1 if $v_c(t) \geq v_r$; otherwise 0. The switch duty-ratio in Fig. 3-14b is given as

$$d(t) = \frac{v_c(t)}{\hat{V}_r} \quad (3-39)$$

thus the control voltage, limited in a range between 0 and \hat{V}_r , linearly and dynamically controls the pulse-width $d(t)$ in Eq. 3-39 and shown in Fig. 3-14b.

3-13 DYNAMIC AVERAGE REPRESENTATION OF CONVERTERS IN CCM

In all three types of dc-dc converters in CCM, the switching power-pole switches between two sub-circuit states based on the switching function $q(t)$. (It switches between three sub-circuit states in DCM, where the switch can be considered “Stuck” between the on and the off positions during the subinterval when the inductor current is zero, discussed in detail in the Appendix.) It is very beneficial to obtain non-switching average models of these switch-mode converters for simulating the converter performance under dynamic conditions caused by the change of input voltage and/or the output load. Under the dynamic condition, the converter duty-ratio, and the average values of voltages and currents within the converter vary with time, but relatively slowly with frequencies an order of magnitude smaller than the switching frequency.

The switching power-pole is shown in Fig. 3-15a, where the voltages and currents are labeled with the subscript vp for the voltage-port and cp for the current-port. In the above analysis for the three converters in the dc steady state, we can write the average voltage and current relationships for the bi-positional switch of the power-pole as

$$V_{cp} = DV_{vp} \quad (3-40a)$$

$$I_{vp} = D I_o \quad (3-40b)$$

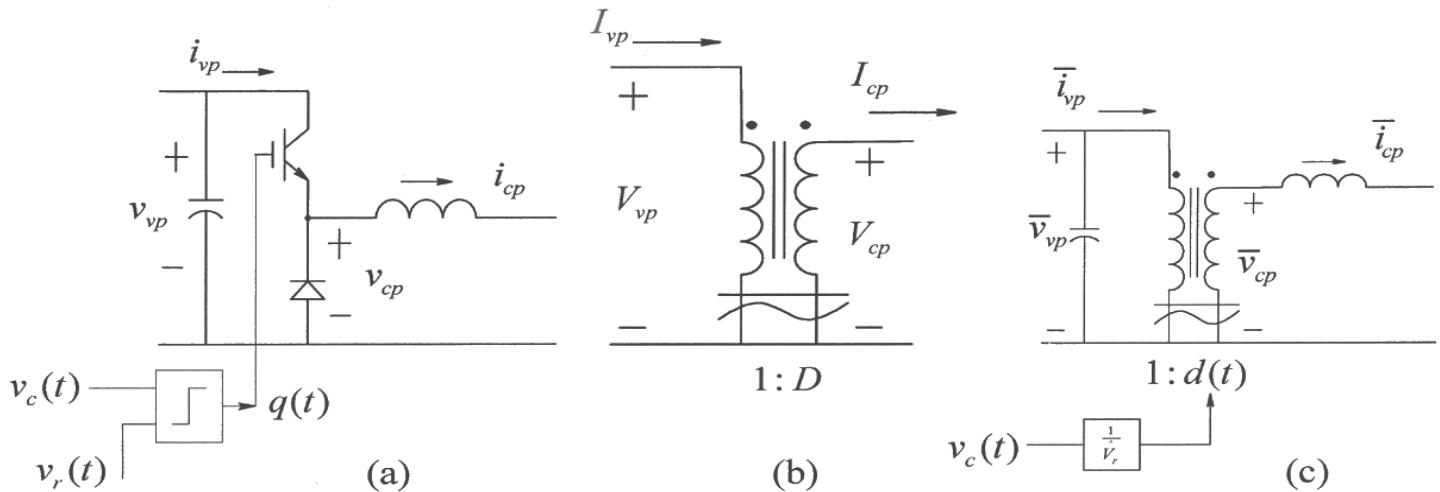


Figure 3-15 Average dynamic model of a switching power-pole.

Relationships in Eq. 3-40 can be represented by an ideal transformer as shown in Fig. 3-15b. Under dynamic conditions, the average model in Fig. 3-15b of the bi-positional switch can be substituted in the power-pole of Fig. 3-15a, resulting in the dynamic average model shown in Fig. 3-15c, using Eq. 3-39 for $d(t)$. Here, the uppercase letters used in the dc steady state relationships are replaced with lowercase letters with a “-” on top to represent average voltages and currents, which may vary dynamically with time: D by $d(t)$, V_{cp} by $\bar{v}_{cp}(t)$, I_{cp} by $\bar{i}_{cp}(t)$, and I_{vp} by $\bar{i}_{vp}(t)$. Therefore, from Eqs. 3-40a and b:

$$\bar{v}_{cp}(t) = d(t)\bar{v}_{vp}(t) \quad (3-41a)$$

$$\bar{i}_{vp}(t) = d(t)\bar{i}_{cp}(t) \quad (3-41b)$$

The above discussion shows that the dynamic average model of a switching power-pole in CCM is an ideal transformer with the turns-ratio $1:d(t)$. Using this model for the switching power-pole, the dynamic average models of the three converters shown in Fig. 3-16a are as in Figs. 3-16b in CCM. Note that in the Boost converter where the transistor is in the bottom position in the power-pole, the transformer turn-ratio is $1:(1-d)$, because the pole duty-ratio d_A is 1 minus the transistor duty-ratio $d(t)$. The average representation of these converters in DCM is described in the Appendix.

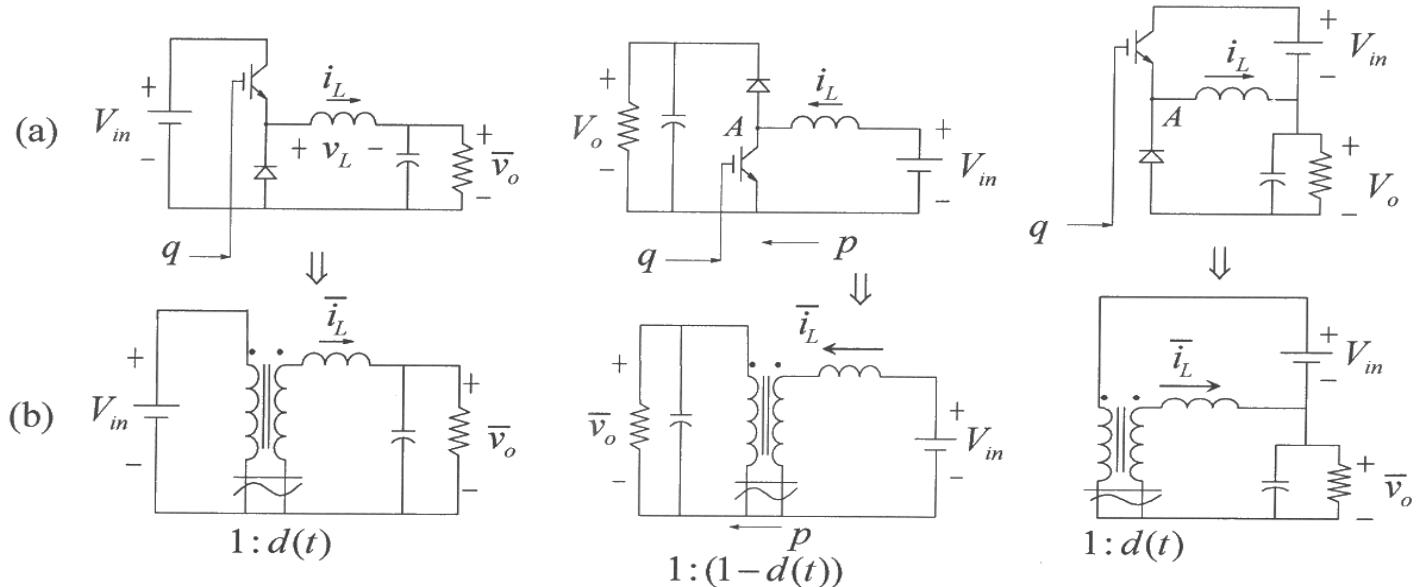


Figure 3-16 Average dynamic models of three converters.

The ideal transformers in the circuits of Fig. 3-16b, being hypothetical and only a convenience for mathematical representation, can operate with ac as well dc voltages and currents, which a real transformer cannot. A symbol consisting of a straight bar with a curve below is used to remind us of this fact. Since no electrical isolation exists between

the voltage-port and the current-port of the switching power-pole, the two windings in the circuits of Fig. 3-15c and Fig. 3-16b are connected at the bottom. Moreover, the voltages in the circuit of Fig. 3-16 cannot become negative (however, depending on the implementation of the power-pole, the currents may become negative, that is, reverse directions), and d is limited to a range between 0 to 1.

In the average representation of the switching power-pole, all the switching information is removed, and hence it provides an uncluttered understanding of achieving desired objectives in various converters. Moreover, the average model in simulating the dynamic response of a converter results in computation speeds orders of magnitude faster than that in the switching model, where the simulation time step must be smaller than at least one-hundredth of the switching time-period T_s in order to achieve an accurate resolution.

3-14 BI-DIRECTIONAL SWITCHING POWER-POLE

In Buck, Boost and Buck-Boost dc-dc converters, the implementation of the switching power-pole by one transistor and one diode dictates the instantaneous current flow to be unidirectional. As shown in Fig. 3-17a, by combining the switching power-pole implementations of Buck and Boost converters, where the two transistors are switched by complimentary signals, allows a continuous bi-directional power and current capability. In such a bi-directional switching power-pole, the positive inductor current as shown in Fig. 3-17b represents a Buck mode, where only the transistor and the diode associated with the Buck converter take part. Similarly, as shown in Fig. 3-17c, the negative inductor current represents a Boost mode, where only the transistor and the diode associated with the Boost converter take part. We will utilize such bi-directional switching power-poles in dc and ac motor drives discussed in Chapters 11 and 12.

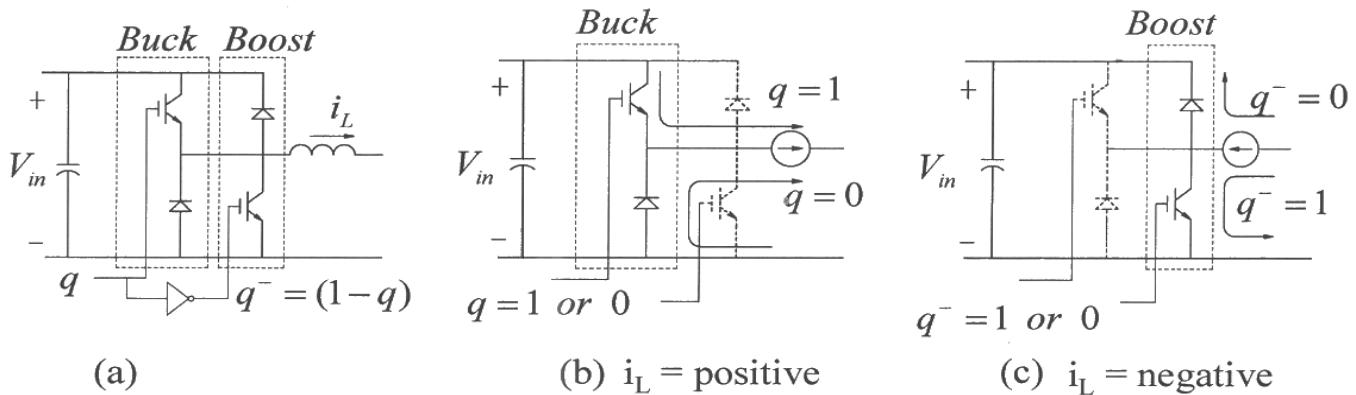


Figure 3-17 Bi-directional power flow through a switching power-pole.

In a bi-directional switching power-pole where the transistors are gated by complimentary signals, the current through it can flow in either direction, and hence ideally, a discontinuous conduction mode does not exist. The average representation of

the bi-directional switching power-pole in Fig. 3-18a is an ideal transformer shown in Fig. 3-18b with a turns-ratio $1:d(t)$, where $d(t)$ represents the pole duty-ratio that is also the duty-ratio of the transistor associated with the Buck mode.

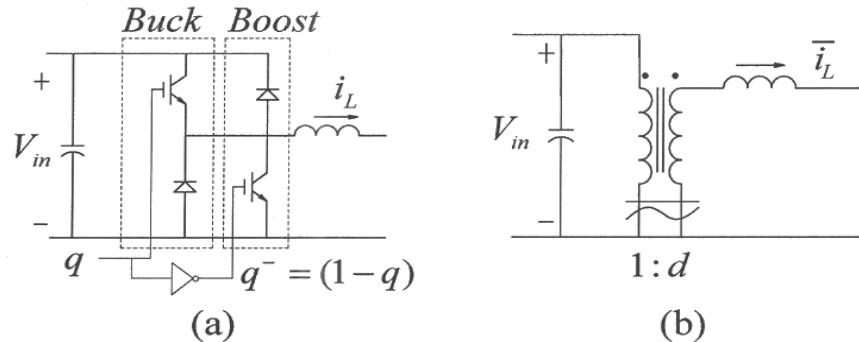


Figure 3-18 Average dynamic model of the switching power-pole with bi-directional power flow.

3-15 DISCONTINUOUS-CONDUCTION MODE (DCM)

All dc-dc converters for unidirectional power and current flow have their switching power-pole implemented by one transistor and one diode, and hence go into a discontinuous conduction mode, DCM, below a certain output load. This operating mode for all three converters is examined in detail in the Appendix, whereas only the critical loads above which converters operate in CCM are examined here.

As an example as shown in Fig. 3-19, if we keep the switch duty-ratio constant, decline in the output load results in the inductor average current to decrease until a critical load value is reached where the inductor current waveform reaches zero at the end of the turn-off interval. The average inductor current in this condition, we will call the critical inductor current, $I_{L,crit}$. For loads below this critical value, the inductor current cannot reverse through the diode in any of the three converters (Buck, Boost and Buck-Boost), and enters DCM where the inductor current remains zero for a finite interval.

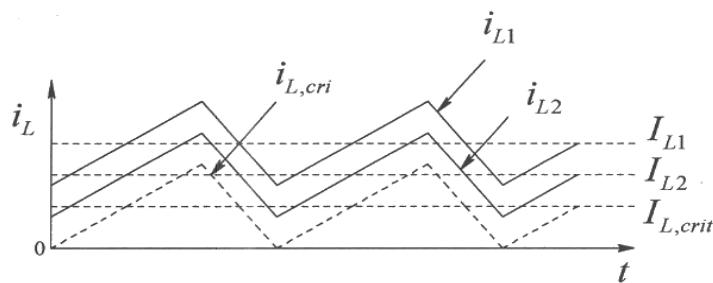


Figure 3-19 Inductor current at various loads; duty-ratio is kept constant.

In DCM, the inductor current conduction becomes discontinuous for an interval during which there is no power drawn from the input source and there is no energy in the

inductor to transfer to the output stage. This interval of inactivity during which the inductor current remains zero generally results in increased device stresses and the ratings of the passive components. DCM also results in noise and EMI, although the diode reverse recovery problem is minimized. Based on these considerations, converters above a few tens of watts are generally designed to operate in CCM, although all of them implemented using one transistor and one diode will enter DCM at very light loads and the feedback controller should be designed to operate adequately in both modes. It should be noted that designing the controller of some converters, such as the Buck-Boost converters, in CCM is much more complicated, thus the designers may prefer to keep such converters in DCM for all possible operating conditions. This we will discuss further in the next chapter dealing with the feedback controller design.

The inductor current at the critical average value, although at the border of CCM and DCM, should be considered to belong to the CCM case. At this critical load condition, the inductor voltage v_L and the current i_L are drawn in Fig. 3-20a-c for the three converters shown in Figs. 3-3a, 3-4a and 3-7a. As can be seen from the i_L waveform in these critical cases in Fig. 3-20, the average inductor current is one-half the peak-peak ripple.

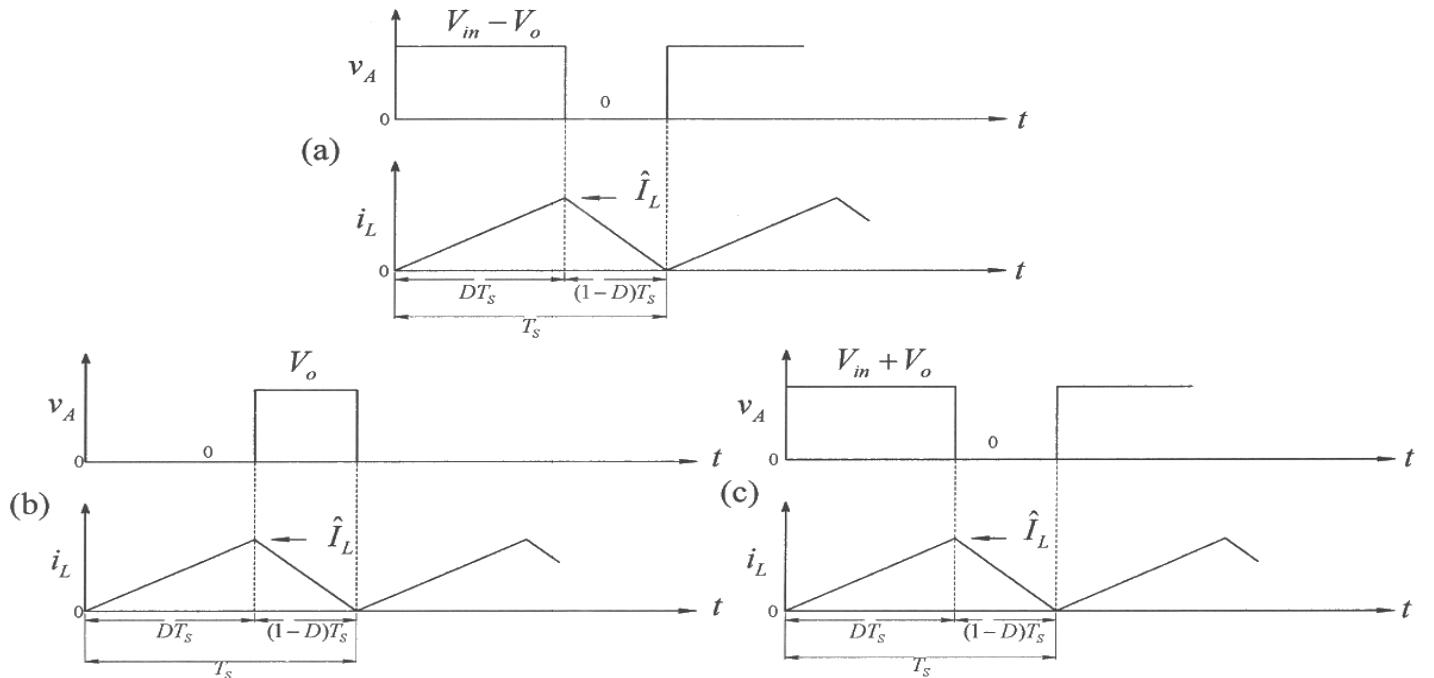


Figure 3-20 Waveforms for the three converters at the border of CCM/DCM.

In the Buck converter of Fig. 3-3a, the peak inductor current in Fig. 3-20a can be calculated by the fact that a voltage ($V_{in} - V_o$) is applied across the inductor for an interval

DT_s interval when the transistor is on, causing the current to rise from zero to its peak value. Therefore, the peak current is

$$\hat{I}_{L,crit,Buck} = \frac{(V_{in} - V_o)}{L} DT_s \quad (3-42)$$

With $f_s = 1/T_s$, and $V_o = DV_{in}$, the average current is

$$I_{L,crit,Buck} = \frac{V_{in}}{2Lf_s} D(1-D) \quad (3-43)$$

In both the Boost and the Buck-Boost converters, V_{in} is applied across the inductor for an interval DT_s interval when the transistor is on, causing the current to rise from zero to its peak value in Figs. 3-20b and c, respectively. Since the average inductor current is one-half of the peak value in these waveforms, the critical value is as follows:

$$I_{L,crit,Boost} = I_{L,crit,Buck-Boost} = \frac{V_{in}}{2Lf_s} D \quad (3-44)$$

If the average inductor current falls below its critical value in a converter, then its operation enters the DCM mode, which is discussed in detail in the Appendix.

REFERENCES

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.
2. B. Carsten, "Converter Component Load Factors; A performance Limitation of Various Topologies" PCI Proceedings, June 1988, pp. 31-49.
3. M. Walters, "An Integrated Synchronous-Rectifier Power IC with Complementary-Switching (HIP5010, HIP5011)" Technical Brief, July 1995, TB332, Intersil Corp.
4. International Rectifier (<http://www.irf.com>).
5. Unitrode for PWM Controller ICs (<http://www.unitrode.com>).

PROBLEMS

Buck DC-DC Converters

In a Buck dc-dc converter, $L = 50 \mu H$. It is operating in dc steady state under the following conditions: $V_{in} = 40V$, $D = 0.3$, $P_o = 24W$, and $f_s = 200 kHz$. Assume ideal components.

- 3-1 Calculate and draw the waveforms as shown in Fig. 3-3d.
- 3-2 Draw the inductor voltage and current waveforms if $P_o = 12W$; all else is unchanged. Compare the ripple in the inductor current with that in Problem 3-1.

- 3-3 In this Buck converter, the output load is changing. Calculate the critical value of the output load P_o below which the converter will enter the discontinuous conduction mode of operation.
- 3-4 Calculate the critical value of the inductance L below which this Buck converter will enter the discontinuous conduction mode at $P_o = 5W$ under all input voltage values.
- 3-5 Draw the waveforms for the variables shown in Fig. 3-3d for this Buck converter at the output load that causes it to operate at the border of continuous and discontinuous modes.
- 3-6 In this Buck converter, the input voltage is varying in a range from 24 V to 50 V. For each input value, the duty-ratio is adjusted to keep the output voltage constant at its nominal value (with $V_{in} = 40V$ and $D = 0.3$). Calculate the minimum value of the inductance L that will keep the converter in the continuous conduction mode at $P_o = 5W$.

Boost DC-DC Converters

In a Boost converter, $L = 50 \mu H$. It is operating in dc steady state under the following conditions: $V_{in} = 12V$, $D = 0.4$, $P_o = 30W$, and $f_s = 200 kHz$. Assume ideal components.

- 3-7 Calculate and draw and the waveforms as shown in Fig. 3-5c.
- 3-8 Draw the inductor voltage and current waveforms, if $P_o = 15W$; all else is unchanged. Compare the ripple in the inductor current with that in Problem 3-7.
- 3-9 In this Boost converter, the output load is changing. Calculate the critical value of the output load P_o below which the converter will enter the discontinuous conduction mode of operation.
- 3-10 Calculate the critical value of the inductance L below which this Boost converter will enter the discontinuous conduction mode of operation at $P_o = 5W$.
- 3-11 Draw the waveforms for the variables in Fig. 3-5c for this Boost converter at the output load that causes it to operate at the border of continuous and discontinuous modes.
- 3-12 In this Boost converter, the input voltage is varying in a range from 9 V to 15 V. For each input value, the duty-ratio is adjusted to keep the output voltage constant at its nominal value (with $V_{in} = 12V$ and $D = 0.4$). Calculate the minimum value of the inductance L that will keep the converter in the continuous conduction mode at $P_o = 5W$ under all input voltage values.

Buck-Boost DC-DC Converters

In a Buck-Boost converter, $L = 50 \mu H$. It is operating in dc steady state under the following conditions: $V_{in} = 12V$, $D = 0.6$, $P_o = 36W$, and $f_s = 200kHz$. Assume ideal components.

- 3-13 Calculate and draw the waveforms as shown in Fig. 3-8c.
- 3-14 Draw the inductor voltage and current waveforms if $P_o = 18W$; all else is unchanged. Compare the ripple in the inductor current with that in Problem 3-13.
- 3-15 In this Buck-Boost converter, the output load is changing. Calculate the critical value of the output load P_o below which the converter will enter the discontinuous conduction mode of operation.
- 3-16 Calculate the critical value of the inductance L below which this Buck-Boost converter will enter the discontinuous conduction mode of operation at $P_o = 5W$.
- 3-17 Draw the waveforms for the variables in Fig. 3-8c for this Buck-Boost converter at the output load that causes it to operate at the border of continuous and discontinuous modes.
- 3-18 In this Buck-Boost converter, the input voltage is varying in a range from 9 V to 15 V. For each input value, the duty-ratio is adjusted to keep the output voltage constant at its nominal value (with $V_{in} = 12V$ and $D = 0.6$). Calculate the minimum value of the inductance L that will keep the converter in the continuous conduction mode of operation at $P_o = 5W$ under all input voltage values.

SEPIC DC-DC Converters

- 3-19 In a SEPIC converter, assume the ripple in the inductor currents and the capacitor voltage to be zero. This SEPIC converter is operating in a dc steady state under the following conditions: $V_{in} = 10V$, $D = 0.333$, $P_o = 50W$, and $f_s = 200kHz$. Assume ideal components. Draw the waveforms for all the converter variables under this dc steady-state condition.

Cuk DC-DC Converters

- 3-20 In a Cuk converter, assume the ripple in the inductor currents and the capacitor voltage to be zero. This Cuk converter is operating in a dc steady state under the following conditions: $V_{in} = 10V$, $D = 0.333$, $P_o = 50W$, and $f_s = 200kHz$. Assume ideal components. Draw the waveforms for all the converter variables under this dc steady-state condition.

Interleaving of DC-DC Converters

- 3-21 Two interleaved Buck converters, each similar to the Buck converter defined earlier before Problem 3-1, are supplying a total of $48W$. Calculate and draw the waveforms of the total input current and the total current ($i_{L_1} + i_{L_2}$) to the output stage. The gate signals to the converters are phase shifted by 180° .

Regulation by PWM

- 3-22 In a Buck converter, consider two values of duty-ratios: 0.3 and 0.4. The switching frequency f_s is 200kHz and $\hat{V}_r = 1.2V$. Draw the waveforms as in Fig 3-14b.

Dynamic Average Models in CCM

- 3-23 Draw the dynamic average representations for Buck, Boost, Buck-Boost, SEPIC and Cuk Converters in the continuous conduction mode.
- 3-24 In the converters based on average representations in Problem 3-23, calculate the average input current for each converter in terms of the output current and the duty-ratio $d(t)$.

Bi-directional Switching Power-Poles

- 3-25 The dc-dc bi-directional converter of Fig. 3-18a interfaces a 12/14-V battery with a 36/42-V battery bank. The internal emfs are $E_1 = 40V$ (dc) and $E_2 = 13V$ (dc). Both these battery sources have an internal resistance of 0.1Ω each. In the dc steady state, calculate the power-pole duty-ratio D_A if (a) the power into the low-voltage battery terminals is 140 W, and (b) the power out of the low-voltage battery terminals is 140 W.

APPENDIX 3A DISCONTINUOUS-CONDUCTION MODE (DCM) IN DC-DC CONVERTERS

As briefly discussed earlier in section 3-15, all dc-dc converters for unidirectional power and current flow (implemented using one transistor and one diode) enter a discontinuous conduction mode, DCM, below a certain output load. The inductor current critical values at the border of CCM and DCM were derived for the three converters, and are given by Eq. 3-43 in Buck converters, and by Eq. 3-44 in both the Boost and the Buck-Boost converters.

3A-1 OUTPUT VOLTAGES IN DCM

3A-1-1 Buck Converters in DCM

For the Buck converter in Fig. 3-3a, an output load less than the critical load (that is, higher than the critical load resistance) results in the inductor current during the off-interval of the transistor to drop to zero, prior to the beginning of the next switching cycle, as shown in Fig. 3A-1a. The inductor current i_L cannot reverse through the diode, and hence becomes discontinuous, remaining zero until the beginning of the new switching cycle. The normalized off interval of the transistor now consists of two subintervals: $D_{off,1}$ and $D_{off,2}$, such that $(D + D_{off,1} + D_{off,2}) = 1$. During $D_{off,2}$, v_A jumps from 0 to V_o as shown in Fig. 3A-1a. The extra volt-seconds, shown as the area hatched in Fig. 3A-1a, averaged over the switching-cycle, result in the output voltage V_o to go higher than its CCM value. The output voltage is plotted in Fig. 3A-1b for a duty-ratio D , which shows that at very light loads in DCM, the output voltage approaches V_{in} . A detailed derivation is presented in the Appendix on the accompanying CD.

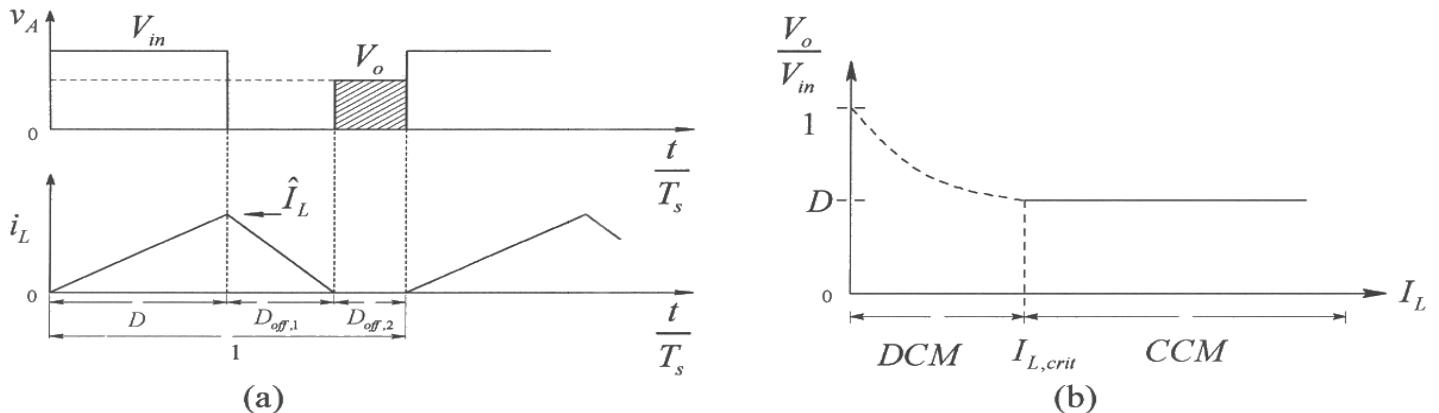


Figure 3A-1 Buck converter in DCM.

3A-1-2 Boost and Buck-Boost Converters in DCM

Unlike Buck converters, Boost and Buck-Boost converters represent a special challenge in DCM, where at very light loads, their output voltage, if not properly regulated can reach dangerously high values, and therefore, care should be taken to avoid this condition. Only the waveforms and the plot of the voltage conversion ratio are presented here in Fig. 3A-2 and Fig. 3A-3 respectively, and the detailed discussion is included in the accompanying CD.

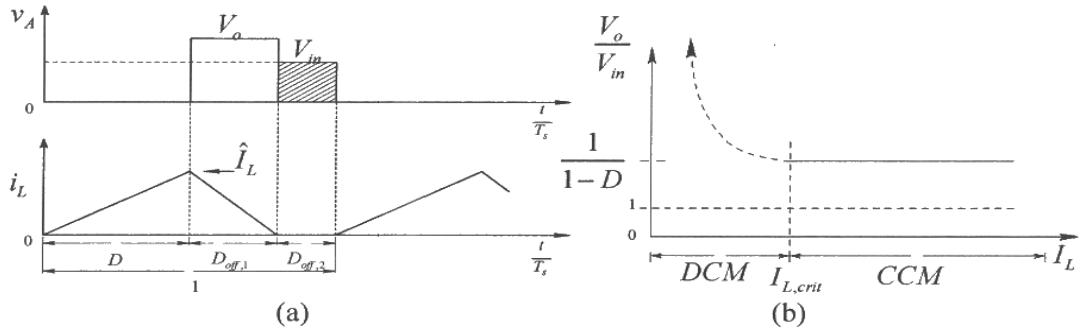


Figure 3A-2 Boost converter in DCM.

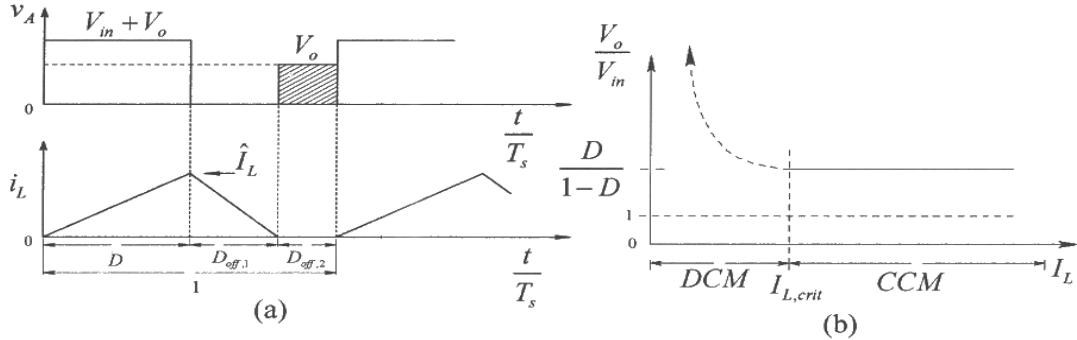


Figure 3A-3 Buck-Boost converter in DCM.

3A-2 AVERAGE REPRESENTATION OF DC-DC CONVERTERS IN DCM

In the previous discussion, we saw that unlike the CCM where the output voltage was independent of the load and was dictated only by the input voltage V_{in} and the transistor duty-ratio $d(t)$, the output voltage in DCM also depends on the converter parameters and the operating condition. The average representation of a switching power-pole in DCM can be obtained by the voltage and current waveforms associated with the converter. In DCM, since the output voltage at the voltage-port is higher than that in the CCM case, the average model of a switching power-pole in CCM by an ideal transformer is augmented by a dependent voltage-source v_k at the current-port and a dependent current-source i_k at the voltage-port. The values of these dependent sources for the three converters are calculated in the Appendix on the accompanying CD, and the results are presented below.

3A-2-1 v_k and i_k for Buck and Buck-Boost Converters in DCM

The average representation of the switching power-pole in Buck and Buck-Boost converters in DCM is shown in Fig. 3A-4 in terms of the dynamic quantities, where

$$v_{k,Buck} = \left[1 - \frac{2L f_s \bar{i}_L}{(V_{in} - \bar{v}_o)d} \right] \bar{v}_o \quad (3A-1)$$

$$i_{k,Buck} = \frac{d^2}{2Lf_s} (V_{in} - \bar{v}_0) - d\bar{i}_L \quad (3A-2)$$

$$v_{k,Buck-Boost} = \left(1 - \frac{2Lf_s \bar{i}_L}{V_{in}d} \right) \bar{v}_o \quad (3A-3)$$

$$i_{k,Buck-Boost} = \frac{d^2}{2Lf_s} V_{in} - d\bar{i}_L \quad (3A-4)$$

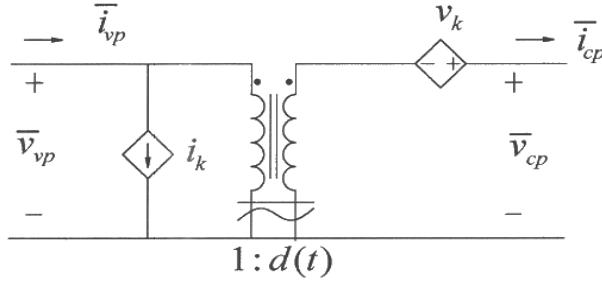


Figure 3A-4 Average dynamic model for Buck and Buck-Boost converters.

If \$v_k\$ and \$i_k\$ are conditional such that they are both zero in CCM and are expressed by the above expressions only in DCM where the average inductor current falls below the critical value, then the representation in Fig. 3A-4 becomes valid for both the CCM and the DCM.

In PSpice the ideal transformer itself is represented by a dependent current source and a dependent voltage sources. The conditional dependent sources \$v_k\$ and \$i_k\$ shown in Fig. 3A-4 are in addition to those used to represent the ideal transformer.

3A-2-2 \$v_k\$ and \$i_k\$ for Boost Converters in DCM

The average representation of the switching power-pole in Boost converters in DCM is shown in Fig. 3A-5 in terms of the dynamic quantities, where

$$v_{k,Boost} = \left(1 - \frac{2Lf_s \bar{i}_L}{V_{in}d} \right) (V_{in} - \bar{v}_0) \quad (3A-5)$$

$$i_{k,Boost} = \frac{d^2}{2Lf_s} V_{in} - d\bar{i}_L \quad (3A-6)$$

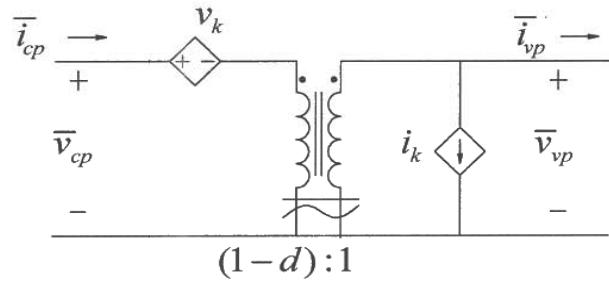


Figure 3A-5 Average dynamic model for Boost converters.

By expressing v_k and i_k conditionally such that they are both zero in CCM and are expressed by Eqs. 3A-5 and 3A-6 only in DCM where the average inductor current falls below the critical value, the representation in Fig. 3A-5 becomes valid for both the CCM and the DCM.

Chapter 4

DESIGNING FEEDBACK CONTROLLERS IN SWITCH-MODE DC POWER SUPPLIES

4-1 INTRODUCTION AND OBJECTIVES OF FEEDBACK CONTROL

As shown in Fig. 4-1, almost all dc-dc converters operate with their output voltage regulated to equal their reference value within a specified tolerance band (for example, $\pm 1\%$ around its nominal value) in response to disturbances in the input voltage and the output load. This regulation is achieved by pulsed-width-modulating the duty-ratio $d(t)$ of their switching power-pole. In this chapter, we will design the feedback controller to regulate the output voltages of dc-dc converters.

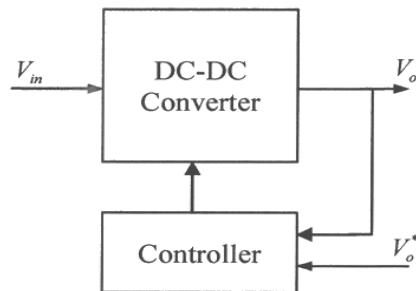


Figure 4-1 Regulated dc power supply.

The feedback controller to regulate the output voltage must be designed with the following objectives in mind: zero steady state error, fast response to changes in the input voltage and the output load, low overshoot, and low noise susceptibility. We should note that in designing feedback controllers, all transformer-isolated topologies discussed later in Chapter 8 can be replaced by their basic single-switch topologies from which they are derived. The feedback control is described using the voltage-mode control, which is later extended to include the current-mode control.

The steps in designing the feedback controller are described as follows:

- Linearize the system for small changes around the dc steady state operating point (bias point). This requires dynamic averaging discussed in the previous chapter.
- Design the feedback controller using linear control theory.

- Confirm and evaluate the system response by simulations for large disturbances.

4-2 REVIEW OF LINEAR CONTROL THEORY

A feedback control system is as shown in Fig. 4-2, where the output voltage is measured and compared with a reference value V_o^* . The error between the two acts on the controller, which produces the control voltage $v_c(t)$. This control voltage acts as the input to the pulse-width-modulator to produce a switching signal $q(t)$ for the power-pole in the dc-dc converter. The average value of this switching signal is $d(t)$, as shown in Fig. 4-2.

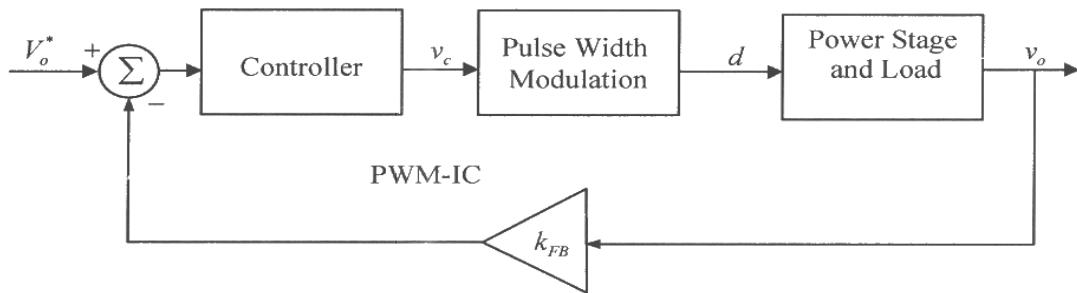


Figure 4-2 Feedback control.

To make use of linear control theory, various blocks in the power supply system of Fig. 4-2 are linearized around the steady state dc operating point, assuming small-signal perturbations. Each average quantity (represented by a “-” on top) associated with the power-pole of the converter topology can be expressed as the sum of its steady state dc value (represented by an uppercase letter) and a small-signal perturbation (represented by a “~” on top), for example,

$$\begin{aligned}\bar{v}_o(t) &= V_o + \tilde{v}_o(t) \\ d(t) &= D + \tilde{d}(t) \\ v_c(t) &= V_c + \tilde{v}_c(t)\end{aligned}\tag{4-1}$$

where $d(t)$ is already an averaged value and $v_c(t)$ does not contain any switching frequency component. Based on the small-signal perturbation quantities in the Laplace domain, the linearized system block diagram is as shown in Fig. 4-3, where the perturbation in the reference input to this feedback-controlled system, \tilde{v}_o^* , is zero since the output voltage is being regulated to its reference value. In Fig. 4-3, $G_{PWM}(s)$ is the transfer function of the pulse-width modulator, and $G_{PS}(s)$ is the power stage transfer function. In the feedback path, the transfer function is of the voltage-sensing network, which can be represented by a simple gain k_{FB} , usually less than unity. $G_C(s)$ is the

transfer function of the feedback controller that needs to be determined to satisfy the control objectives.

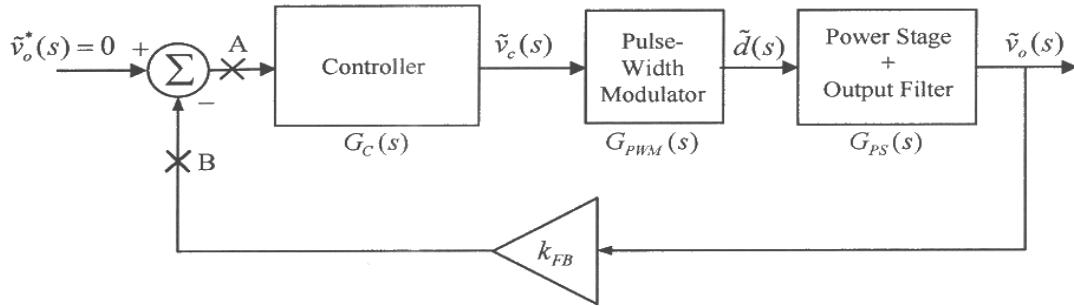


Figure 4-3 Small signal control system representation.

4-2-1 Loop Transfer Function $G_L(s)$

It is the closed-loop response (with the feedback in place) that we need to optimize. Using linear control theory, we can achieve this objective by ensuring certain characteristics of the loop transfer function $G_L(s)$. In the control block diagram of Fig. 4-3, the loop transfer function (from point A to point B) is

$$G_L(s) = G_C(s)G_{PWM}(s)G_{PS}(s)k_{FB} \quad (4-2)$$

4-2-2 Crossover Frequency f_c of $G_L(s)$

In order to define a few necessary control terms, we will consider a generic Bode plot of the loop transfer function $G_L(s)$ in terms of its magnitude and phase angle, shown in Fig. 4-4 as a function of frequency. The frequency at which the gain equals unity (that is $|G_L(s)| = 0 \text{ dB}$) is defined as the crossover frequency f_c (or ω_c). This crossover frequency is a good indicator of the bandwidth of the closed-loop feedback system, which determines the speed of the dynamic response of the control system to various disturbances.

4-2-3 Phase and Gain Margins

For the closed-loop feedback system to be stable, at the crossover frequency f_c , the phase delay introduced by the loop transfer function must be less than 180° . At f_c , the phase angle $\angle G_L(s)|_{f_c}$ of the loop transfer function $G_L(s)$, measured with respect to -180° , is defined as the Phase Margin (ϕ_{PM}) as shown in Fig. 4-4:

$$\phi_{PM} = \angle G_L(s)|_{f_c} - (-180^\circ) = \angle G_L(s)|_{f_c} + 180^\circ \quad (4-3)$$

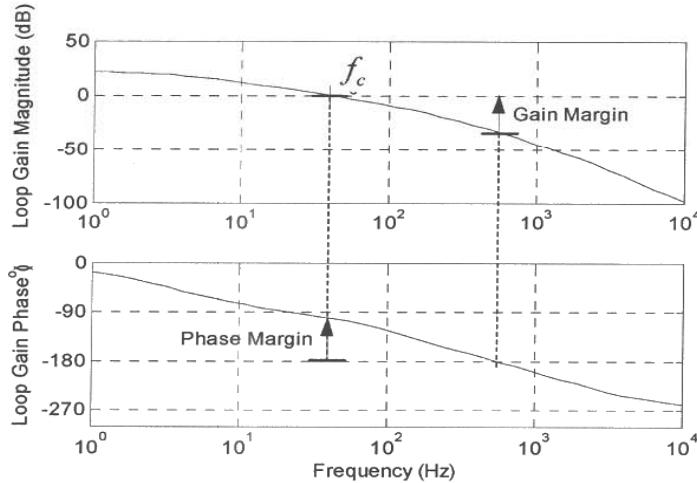


Figure 4-4 Definitions of crossover frequency, gain margin and phase margin.

Note that $\angle G_L(s)|_{f_c}$ is negative, but the phase margin in Eq. 4-3 must be positive. Generally, feedback controllers are designed to yield a phase margin of approximately 60° , since much smaller values result in high overshoots and long settling times (oscillatory response) and much larger values in a sluggish response.

The Gain Margin is also defined in Fig. 4-4, which shows that the gain margin is the value of the magnitude of the loop transfer function, measured below 0 dB, at the frequency at which the phase angle of the loop transfer function may (not always) cross -180° . If the phase angle crosses -180° , the gain margin should generally be in excess of 10 dB in order to keep the system response from becoming oscillatory due to parameter changes and other variations.

4-3 LINEARIZATION OF VARIOUS TRANSFER FUNCTION BLOCKS

To be able to apply linear control theory in the feedback controller design, it is necessary that all the blocks in Fig. 4-2 be linearized around their dc steady state operating point, as shown by transfer functions in Fig. 4-3.

4-3-1 Linearizing the Pulse-Width Modulator

In the feedback control, a high-speed PWM integrated circuit such as the UC3824 [1] from Unitrode/Texas Instruments may be used. Functionally, within this PWM-IC shown in Fig. 4-5a, the control voltage $v_c(t)$ generated by the error amplifier is compared with a ramp signal v_r with a constant amplitude \hat{V}_r at a constant switching frequency f_s , as shown in Fig. 4-5b. The output switching signal is represented by the switching function $q(t)$, which equals 1 if $v_c(t) \geq v_r$; otherwise 0. The switch duty-ratio in Fig. 4-5b is given as

$$d(t) = \frac{v_c(t)}{\hat{V}_r} \quad (4-4)$$

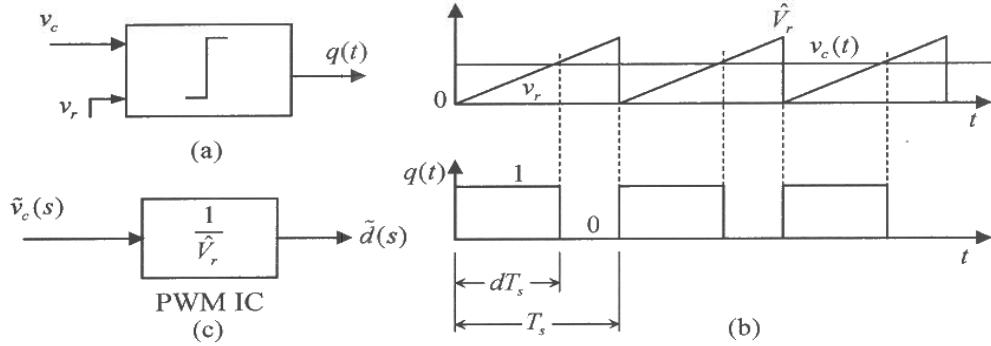


Figure 4-5 PWM waveforms.

In terms of a disturbance around the dc steady state operating point, the control voltage can be expressed as

$$v_c(t) = V_c + \tilde{v}_c(t) \quad (4-5)$$

Substituting Eq. 4-5 into Eq. 4-4,

$$d(t) = \underbrace{\frac{V_c(t)}{\hat{V}_r}}_D + \underbrace{\frac{\tilde{v}_c(t)}{\hat{V}_r}}_{\tilde{d}(t)} \quad (4-6)$$

In Eq. 4-6, the second term on the right side equals $\tilde{d}(t)$, from which the transfer function of the PWM-IC is

$$G_{PWM}(s) = \frac{\tilde{d}(s)}{\tilde{v}_c(s)} = \frac{1}{\hat{V}_r} \quad (4-7)$$

It is a constant gain transfer function, as shown in Fig. 4-5c in the Laplace domain.

Example 4-1 In PWM-ICs, there is usually a dc voltage offset in the ramp voltage, and instead of \hat{V}_r as shown in Fig. 4-5b, a typical Valley-to-Peak value of the ramp signal is defined. In the PWM-IC UC3824, this valley-to-peak value is 1.8 V. Calculate the linearized transfer function associated with this PWM-IC.

Solution The dc offset in the ramp signal does not change its small signal transfer function. Hence, the peak-to-valley voltage can be treated as \hat{V}_r . Using Eq. 4-7

$$G_{PWM}(s) = \frac{1}{\hat{V}_r} = \frac{1}{1.8} = 0.556 \quad (4-8)$$