

4-3-2 Linearizing the Power Stage of DC-DC Converters in CCM

To design feedback controllers, the power stage of the converters must be linearized around the steady state dc operating point, assuming a small-signal disturbance. Fig. 4-6a shows the average model of the switching power-pole, where the subscript “ vp ” refers to the voltage-port and “ cp ” to the current-port. Each average quantity in Fig. 4-6a can be expressed as the sum of its steady state dc value (represented by an uppercase letter) and a small-signal perturbation (represented by a “~” on top):

$$\begin{aligned} d(t) &= D + \tilde{d}(t) \\ \bar{v}_{vp}(t) &= V_{vp} + \tilde{v}_{vp}(t) \\ \bar{v}_{cp}(t) &= V_{cp} + \tilde{v}_{cp}(t) \\ \bar{i}_{vp}(t) &= I_{vp} + \tilde{i}_{vp}(t) \\ \bar{i}_{cp}(t) &= I_{cp} + \tilde{i}_{cp}(t) \end{aligned} \quad (4-9)$$

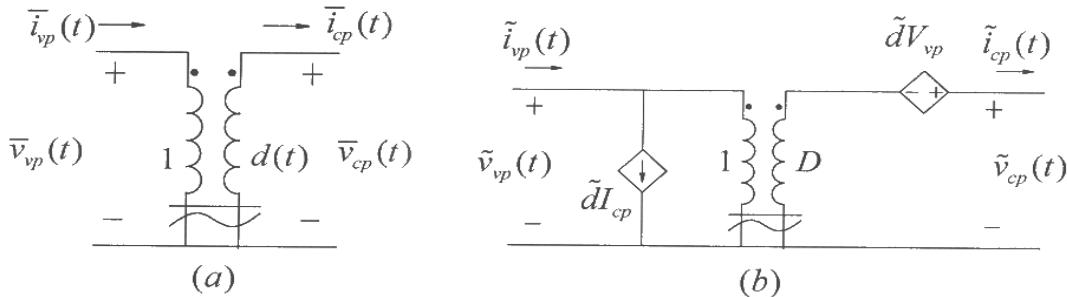


Figure 4-6 Linearizing the switching power-pole.

Utilizing the voltage and current relationships between the two ports in Fig. 4-6a, and expressing each variable as in Eq. 4-9

$$V_{cp} + \tilde{v}_{cp} = (D + \tilde{d})(V_{vp} + \tilde{v}_{vp}) \quad (4-10a)$$

and,

$$I_{vp} + \tilde{i}_{vp} = (D + \tilde{d})(I_{cp} + \tilde{i}_{cp}) \quad (4-10b)$$

Equating the perturbation terms on both sides of the above equations

$$\tilde{v}_{cp}(t) = V_{vp}\tilde{d} + D\tilde{v}_{vp} + \cancel{\tilde{d}\tilde{v}_{cp}} \quad (4-11a)$$

and,

$$\tilde{i}_{vp} = D\tilde{i}_{cp} + I_{cp}\tilde{d} + \cancel{\tilde{d}\tilde{i}_{cp}} \quad (4-11b)$$

The two equations above are linearized by neglecting the products of small perturbation terms (crossed out in Eqs. 4-11a and b). The resulting linear equations are

$$\tilde{v}_{cp}(t) = V_{vp} \tilde{d} + D \tilde{v}_{vp} \quad (4-12)$$

and,

$$\tilde{i}_{vp} = D \tilde{i}_{cp} + I_{cp} \tilde{d} \quad (4-13)$$

Eqs. 4-12 and 4-13 can be represented by means of an ideal transformer shown in Fig. 4-6b, which is a linear representation of the power-pole for small signals around a steady state operating point given by D , V_{vp} , and I_{cp} .

The average representations of Buck, Boost and Buck-Boost converters are shown in Fig. 4-7a. Replacing the power-pole in each of these converters by its small-signals linearized representation, the resulting circuits are shown in Fig. 4-7b, where the perturbation \tilde{v}_{in} is zero based on the assumption of a constant dc input voltage V_{in} , and the output capacitor ESR is represented by r . Note that in Boost converters, since the transistor is in the bottom position of the switching power-pole, D in Eqs. 4-12 and 4-13 needs to be replaced by $(1-D)$ and \tilde{d} by $(-\tilde{d})$.

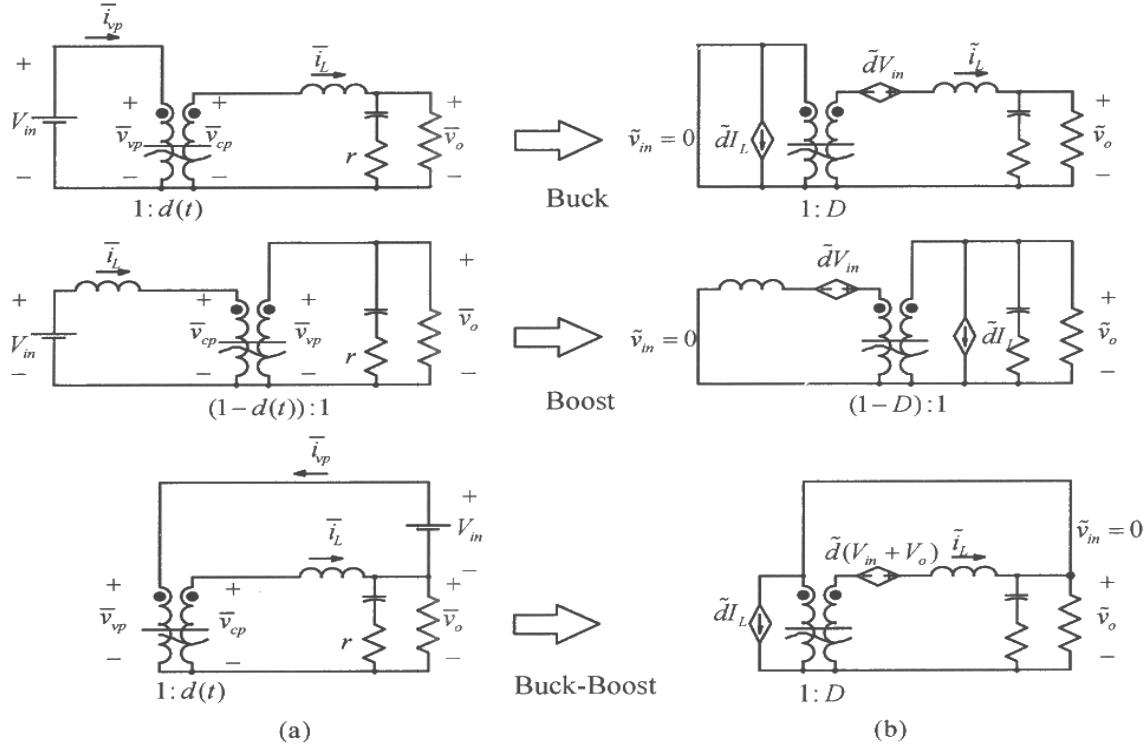


Figure 4-7 Linearizing single-switch converters in CCM.

As fully explained in the Appendix on the accompanying CD, all three circuits for small-signal perturbations in Fig. 4-7b have the same form as shown in Fig. 4-8. In this equivalent circuit, the effective inductance L_e is the same as the actual inductance L in the Buck converter, since in both states of a Buck converter in CCM, L and C are

always connected together. However, in Boost and Buck-Boost converters, these two elements are not always connected, resulting in L_e to be $L/(1-D)^2$ in Fig. 4-8:

$$L_e = L \text{ (Buck); } L_e = \frac{L}{(1-D)^2} \text{ (Boost and Buck-Boost)} \quad (4-14)$$

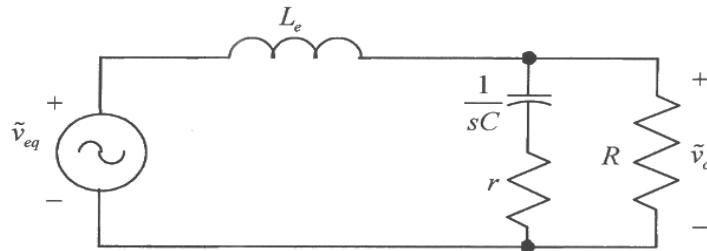


Figure 4-8 Small signal equivalent circuit for Buck, Boost and Buck-Boost converters.

Transfer functions of the three converters in CCM from the Appendix on the accompanying CD are repeated below:

$$\frac{\tilde{v}_o}{\tilde{d}} = \frac{V_{in}}{LC} \frac{1 + srC}{s^2 + s \left(\frac{1}{RC} + \frac{r}{L} \right) + \frac{1}{LC}} \quad (\text{Buck}) \quad (4-15)$$

$$\frac{\tilde{v}_o}{\tilde{d}} = \frac{V_{in}}{(1-D)^2} \left(1 - s \frac{L_e}{R} \right) \frac{1 + srC}{L_e C \left(s^2 + s \left(\frac{1}{RC} + \frac{r}{L_e} \right) + \frac{1}{L_e C} \right)} \quad (\text{Boost}) \quad (4-16)$$

$$\frac{\tilde{v}_o}{\tilde{d}} = \frac{V_{in}}{(1-D)^2} \left(1 - s \frac{DL_e}{R} \right) \frac{1 + srC}{L_e C \left(s^2 + s \left(\frac{1}{RC} + \frac{r}{L_e} \right) + \frac{1}{L_e C} \right)} \quad (\text{Buck-Boost}) \quad (4-17)$$

In the above power-stage transfer functions in CCM, there are several characteristics worth noting. There are two poles created by the low-pass $L-C$ filter in Fig. 4-8, and the capacitor ESR r results in a zero. In Boost and Buck-Boost converters, their transfer functions depend on the steady state operating value D . They also have a right-half-plane zero, whose presence can be explained by the fact that in these converters, increasing the duty-ratio for increasing the output, for example, initially has an opposite consequence by isolating the input stage from the output load for a longer time.

4-3-2-1 Using Computer Simulation to Obtain \tilde{v}_o/\tilde{d}

Transfer functions given by Eqs. 4-15 through 4-17 provide theoretical insight into converter operation. However, the Bode plots of the transfer function can be obtained with similar accuracy by means of linearization and ac analysis, using a computer

program such as PSpice™. The converter circuit is simulated as shown in Figs. 4-9 in the example below for a frequency-domain ac analysis, using the switching power-pole average model discussed in Chapter 3 and shown in Fig. 4-6a. The duty-cycle perturbation \tilde{d} is represented as an ac source whose frequency is swept over several decades of interest, and whose amplitude is kept constant. In such a simulation, PSpice first calculates voltages and currents at the dc steady state operating point, linearizes the circuit around this dc bias point, and then performs the ac analysis.

► **Example 4-2** A Buck converter has the following parameters and is operating in CCM: $L = 100 \mu H$, $C = 697 \mu F$, $r = 0.1 \Omega$, $f_s = 100 kHz$, $V_{in} = 30 V$, and $P_o = 36 W$. The duty-ratio D is adjusted to regulate the output voltage $V_o = 12 V$. Obtain both the gain and the phase of the power stage $G_{PS}(s)$ for the frequencies ranging from 1 Hz to 100 kHz.

Solution The PSpice circuit is shown in Fig. 4-9 where the dc voltage source $\{D\}$, representing the duty-ratio D , establishes the dc operating point. The duty-ratio perturbation \tilde{d} is represented as an ac source whose frequency is swept over several decades of interest, keeping the amplitude constant. (Since the circuit is linearized before the ac analysis, the best choice for the ac source amplitude is 1 V.) The switching power-pole is represented by an ideal transformer, which consists of two dependent sources: a dependent current source and a dependent voltage source. The circuit parameters are specified by means of parameter blocks within PSpice.

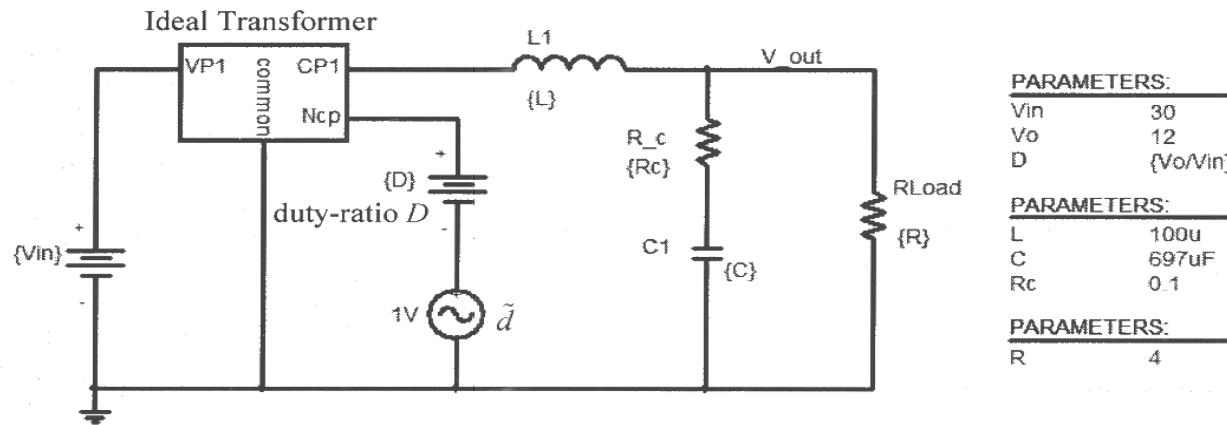


Figure 4-9 PSpice Circuit model for a Buck converter.

The Bode plot of the frequency response is shown in Fig. 4-10. It shows that at the crossover frequency $f_c = 1 kHz$ selected in the next example, Example 4-3, the power stage has $|G_{PS}(s)|_{f_c} = 24.66 dB$ and $\angle G_{PS}(s)|_{f_c} = -138^\circ$. We will make use of these values in Example 4-3.

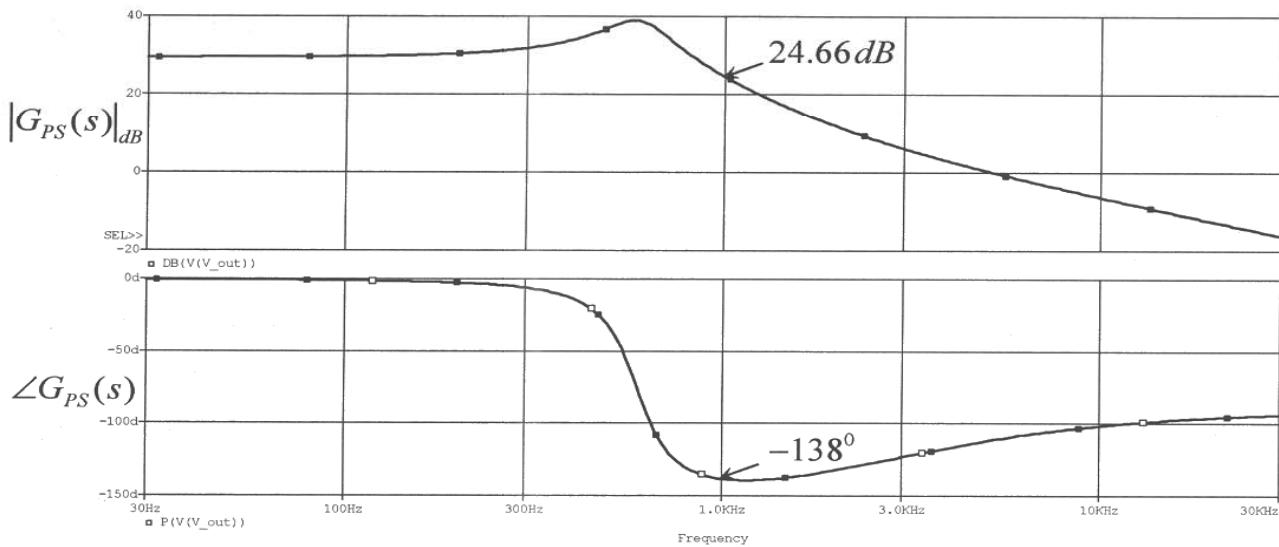


Figure 4-10 The gain and the phase of the power stage $G_{PS}(s)$.

4-4 FEEDBACK CONTROLLER DESIGN IN VOLTAGE-MODE CONTROL

The feedback controller design is presented by means of a numerical example to regulate the Buck converter described in Example 4-2. The controller is designed for the continuous conduction mode (CCM) at full-load, which although not optimum, is stable in DCM.

▲ **Example 4-3** Design the feedback controller for the Buck converter described in Example 4-2. The PWM-IC is as described in Example 4-1. The output voltage-sensing network in the feedback path has a gain $k_{FB} = 0.2$. The steady state error is required to be zero and the phase margin of the loop transfer function should be 60° at as high a crossover frequency as possible.

Solution In deciding on the transfer function $G_C(s)$ of the controller, the control objectives translate into the following simultaneous characteristics of the loop transfer function $G_L(s)$, from which $G_C(s)$ can be designed:

1. The crossover frequency f_c of the loop gain is as high as possible to result in a fast response of the closed-loop system.
2. The phase angle of the loop transfer function has the specified phase margin, typically 60° at the crossover frequency so that the response in the closed-loop system settles quickly without oscillations.
3. The phase angle of the loop transfer function should not drop below -180° at frequencies below the crossover frequency.

The Bode plot for the power stage is obtained earlier, as shown in Fig. 4-10 of Example 4-2. In this Bode plot, the phase angle drops towards -180° due to the two poles of the $L-C$ filter shown in the equivalent circuit of Fig. 4-8 and confirmed by the transfer function of Eq. 4-15. Beyond the $L-C$ filter resonance frequency, the phase angle increases toward -90° because of the zero introduced by the output capacitor ESR in the transfer function of the power stage. We should not rely on this capacitor ESR, which is not accurately known and can have a large variability.

A simple procedure based on the K-factor approach [2] is presented below, which lends itself to a straightforward step-by-step design. For reasons given below, the transfer function $G_C(s)$ of the controller is selected to be of the form in Eq. 4-18 whose Bode plot is shown in Fig. 4-11.

$$G_C(s) = \frac{k_c}{s} \underbrace{\frac{(1+s/\omega_z)^2}{(1+s/\omega_p)^2}}_{\text{phase-boost}} \quad (4-18)$$

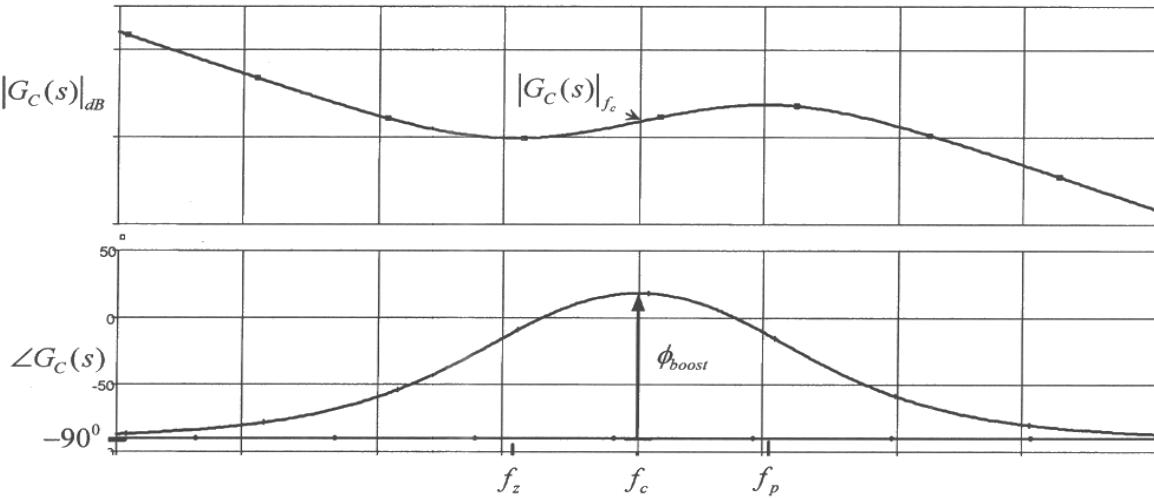


Figure 4-11 Bode plot of $G_C(s)$ in Eq. 4-18.

To yield a zero steady state error, $G_C(s)$ contains a pole at the origin, which introduces -90° phase shift in the loop transfer function. The crossover frequency f_c of the loop is chosen beyond the $L-C$ resonance frequency of the power stage, where, unfortunately, $\angle G_{PS}|_{f_c}$ has a large negative value. The sum of -90° , due to the pole at the origin in $G_C(s)$, and $\angle G_{PS}|_{f_c}$ is more negative than -180° . Therefore, to obtain a phase margin of 60° requires boosting the phase at f_c , by more than 90° , by placing two coincident zeroes at f_z to nullify the effect of the two poles in the power-stage transfer function

$G_{PS}(s)$. Two coincident poles are placed at f_p ($> f_z$) to roll-off the gain rapidly much before the switching frequency. The controller gain $|G_C(s)|_{f_c}$ is such that the loop gain equals unity at the crossover frequency.

The input specifications in determining the parameters of the controller transfer function in Eq. 4-18 are f_c , ϕ_{boost} as shown in Fig. 4-11, and the controller gain $|G_C(s)|_{f_c}$. A step-by-step procedure for designing $G_C(s)$ is described below.

Step 1: Choose the Crossover Frequency. Choose f_c to be *slightly* beyond the $L-C$ resonance frequency $1/(2\pi\sqrt{LC})$, which in this example is approximately 600 Hz. Therefore, we will choose $f_c = 1$ kHz. This ensures that the phase angle of the loop remains greater than -180° at all frequencies.

Step 2: Calculate the needed Phase Boost. The desired phase margin is specified as $\phi_{PM} = 60^\circ$. The required phase boost ϕ_{boost} at the crossover frequency is calculated as follows, noting that G_{PWM} and k_{FB} produce zero phase shift:

$$\angle G_L(s)|_{f_c} = \angle G_{PS}(s)|_{f_c} + \angle G_C(s)|_{f_c} \quad (\text{from Eq. 4-2}) \quad (4-19)$$

$$\angle G_L(s)|_{f_c} = -180^\circ + \phi_{PM} \quad (\text{from Eq. 4-3}) \quad (4-20)$$

$$\angle G_C(s)|_{f_c} = -90^\circ + \phi_{boost} \quad (\text{from Fig. 4-11}) \quad (4-21)$$

Substituting Eqs. 4-20 and 4-21 into Eq. 4-19,

$$\phi_{boost} = -90^\circ + \phi_{PM} - \angle G_{PS}(s)|_{f_c} \quad (4-22)$$

In Fig. 4-10, $\angle G_{PS}(s)|_{f_c} \approx -138^\circ$, substituting which in Eq. 4-22 yields the required phase boost $\phi_{boost} = 108^\circ$.

Step 3: Calculate the Controller Gain at the Crossover Frequency. From Eq. 4-2 at the crossover frequency f_c

$$|G_L(s)|_{f_c} = |G_C(s)|_{f_c} \times |G_{PWM}(s)|_{f_c} \times |G_{PS}(s)|_{f_c} \times k_{FB} = 1 \quad (4-23)$$

In Fig. 4-10, at $f_c = 1$ kHz, $|G_{PS}(s)|_{f_c=1\text{kHz}} = 24.66 \text{ dB} = 17.1$. Therefore in Eq. 4-23, using the gain of the PWM block calculated in Example 4-1,

$$|G_C(s)|_{f_c} \times \underbrace{|G_{PWM}(s)|_{f_c}}_{0.556} \times \underbrace{|G_{PS}(s)|_{f_c}}_{17.1} \times \underbrace{k_{FB}}_{0.2} = 1 \quad (4-24)$$

or

$$|G_C(s)|_{f_c} = 0.5263 \quad (4-25)$$

The controller in Eq. 4-18 with two pole-zero pairs is thoroughly analyzed in the Appendix to this chapter on the accompanying CD. According to this analysis, the phase angle of $G_C(s)$ in Eq. 4-18 reaches its maximum at the geometric mean frequency $\sqrt{f_z f_p}$, where the phase boost ϕ_{boost} , as shown in Fig. 4-11, is measured with respect to -90° . By proper choice of the controller parameters, the geometric mean frequency is made equal to the crossover frequency f_c . We introduce a factor K_{boost} that indicates the geometric separation between poles and zeroes to yield the necessary phase boost:

$$K_{boost} = \sqrt{\frac{\omega_p}{\omega_z}} \quad (4-26)$$

As shown in the Appendix, this factor can be derived in terms of ϕ_{boost} as

$$K_{boost} = \tan\left(45^\circ + \frac{\phi_{boost}}{4}\right), \quad (4-27)$$

In terms of K_{boost} , from Eqs 4-26 and 4-27, the controller parameters can be calculated as follows:

$$f_z = \frac{f_c}{K_{boost}} \quad (4-28)$$

$$f_p = K_{boost} f_c \quad (4-29)$$

$$k_c = |G_C(s)|_{f_c} \frac{\omega_z}{K_{boost}} \quad (4-30)$$

Once the parameters in Eq. 4-18 are determined, the controller transfer function can be synthesized by a single op-amp circuit shown in Fig. 4-12.

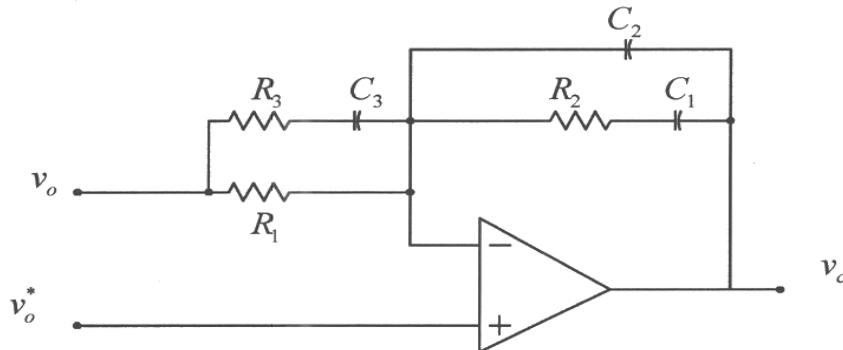


Figure 4-12 Implementation of the controller in Eq. 4-18 by an op-amp.

The choice of R_l in Fig. 4-12 is based on how much current can be drawn from the sensor output; other resistances and capacitances are chosen using the relationships derived in the Appendix and presented below:

$$\begin{aligned}
 C_2 &= \omega_z / (k_c \omega_p R_l) \\
 C_1 &= C_2 (\omega_p / \omega_z - 1) \\
 R_2 &= 1 / (\omega_z C_1) \\
 R_3 &= R_l / (\omega_p / \omega_z - 1) \\
 C_3 &= 1 / (\omega_p R_3)
 \end{aligned} \tag{4-31}$$

In this numerical example with $f_c = 1 \text{ kHz}$, $\phi_{boost} = 108^\circ$, and $|G_C(s)|_{f_c} = 0.5263$, we can calculate $K_{boost} = 3.078$ in Eq. 4-27. Using Eqs. 4-27 through 4-30, $f_z = 324.9 \text{ Hz}$, $f_p = 3078 \text{ Hz}$, and $k_c = 349.1$. For the op-amp implementation, we will select $R_l = 100 \text{ k}\Omega$. From Eq. 4-30, $C_2 = 3.0 \text{ nF}$, $C_1 = 25.6 \text{ nF}$, $R_2 = 19.1 \text{ k}\Omega$, $R_3 = 11.8 \text{ k}\Omega$, and $C_3 = 4.4 \text{ nF}$. We can verify the design of Example 4-3 in PSpice by adding the controller to the converter model. Notice that the op amp is modeled as a high-gain differential amplifier in Fig. 4-13, where a step-change in load is applied at 1 ms. The results are plotted in Fig. 4-14.

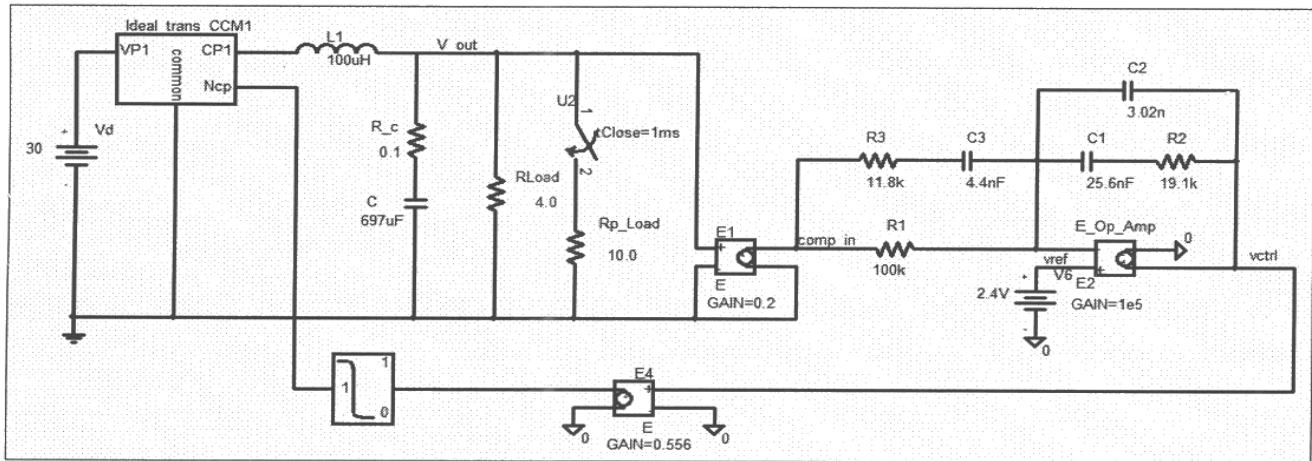


Figure 4-13 PSpice average model of the Buck converter with voltage-mode control.

Note that in the controller transfer function $G_C(s)$ in the example above, both zeroes are at the same frequency; the same is true for both the poles. This need not be the case for possibly achieving a higher crossover frequency.

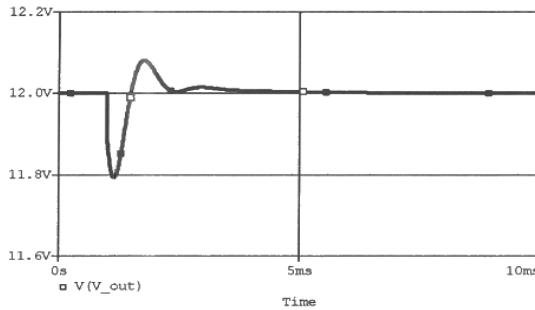


Figure 4-14 Response to a step-change in load.

4-5 PEAK-CURRENT MODE CONTROL

Current-mode control is often used in practice due to its many desirable features, such as simpler controller design and inherent current limiting. In such a control scheme, an inner control loop inside the outer voltage-loop is used as shown in Fig. 4-15, resulting in a peak-current-mode control system. In this control arrangement, another state-variable, the inductor current, is utilized as a feedback signal.

The overall voltage-loop objectives in the current-mode control are the same as in the voltage-mode control discussed earlier. However, the voltage-loop controller here produces the reference value for the current that should flow through the inductor, hence the name current-mode control. There are two types of current-mode control:

- Peak-Current-Mode Control, and
- Average-Current-Mode Control.

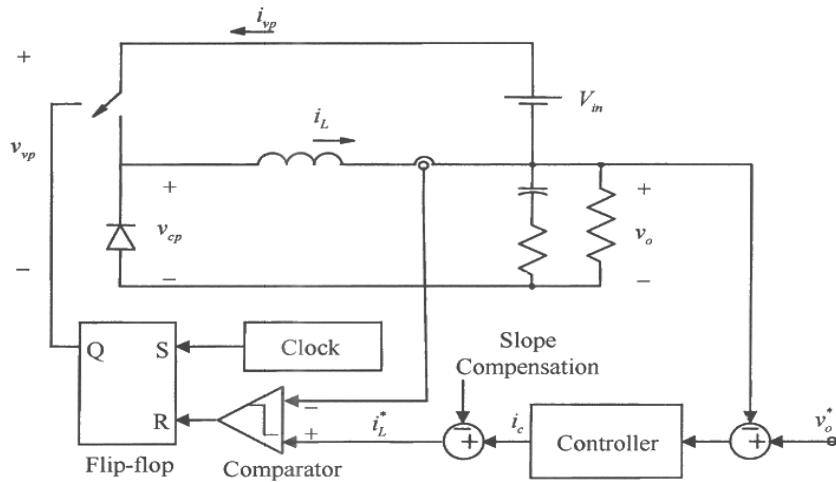


Figure 4-15 Peak current mode control.

In switch-mode dc power supplies, peak-current-mode control is invariably used, and therefore we will concentrate on it here. (We will examine the average-current-mode

control in connection with the power-factor-correction circuits discussed in the next chapter.)

For the current loop, the outer voltage loop in Fig. 4-15 produces the reference value i_L^* of the inductor current. This reference current signal is compared with the measured inductor current i_L to reset the flip-flop when i_L reaches i_L^* . As shown in Figs. 4-15 and 4-16a, in generating i_L^* , the voltage controller output i_c is modified by a signal called the slope compensation, which is necessary to avoid oscillations at the sub-harmonic frequencies of f_s , particularly at the duty-ratio $d > 0.5$. Generally, the slope of this compensation signal is less than one-half of the slope at which the inductor current falls when the transistor in the converter is turned off.

In Fig. 4-16a, when the inductor current reaches the reference value, the transistor is turned off, and is turned back on at a regular interval $T_s (= 1/f_s)$ set by the clock. For small perturbations, this current loop acts extremely fast, and it can be assumed ideal with a gain of unity in the small-signal block diagram of Fig. 4-16b. The design of the outer voltage loop is described by means of the example below of a Buck-Boost converter operating in CCM.

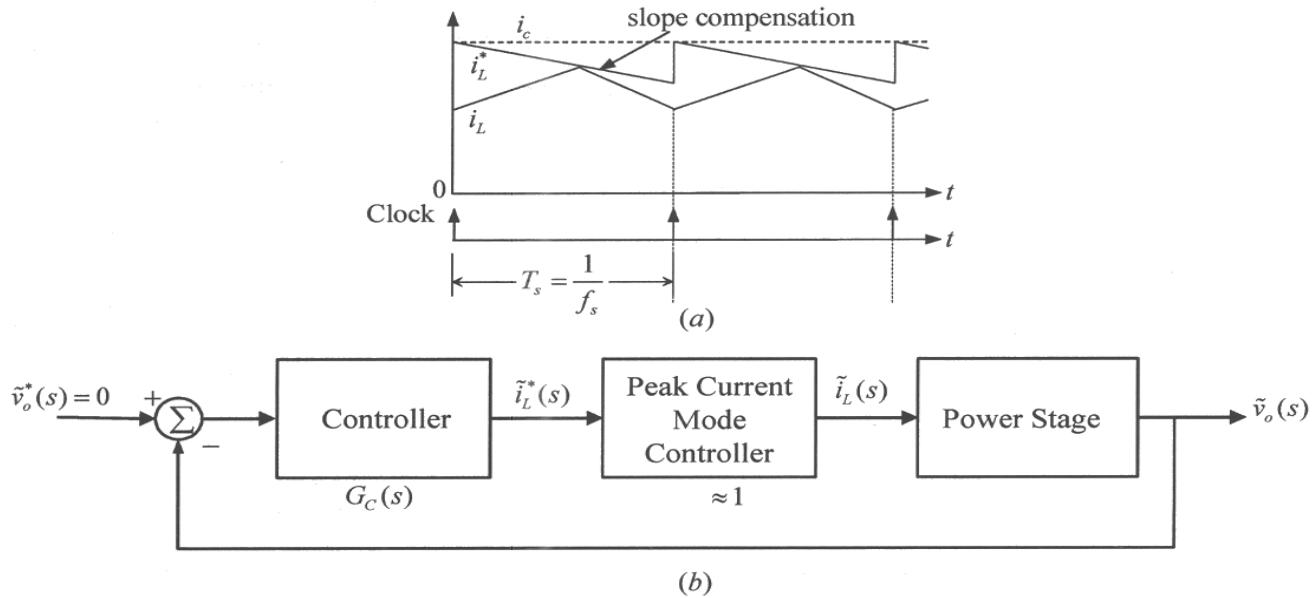


Figure 4-16 Peak-current-mode control with slope compensation.

Example 4-4 In this example, we will design a peak-current-mode controller for a Buck-Boost converter that has the following parameters and operating conditions: $L = 100 \mu\text{H}$, $C = 697 \mu\text{F}$, $r = 0.01 \Omega$, $f_s = 100 \text{ kHz}$, $V_{in} = 30 \text{ V}$. The output power $P_o = 18 \text{ W}$ in CCM and the duty-ratio D is adjusted to regulate the output voltage

$V_o = 12 \text{ V}$. The phase margin required for the voltage loop is 60° . Assume that in the voltage feedback network, $k_{FB} = 1$.

Solution In designing the outer voltage loop in Fig. 4-16b, the transfer function needed for the power stage is $\tilde{v}_o / \tilde{i}_L$. This transfer function in CCM can be obtained theoretically. However, it is much easier to obtain the Bode plot of this transfer function by means of a computer simulation, similar to that used for obtaining the Bode plots of \tilde{v}_o / \tilde{d} in Example 4-2 for a Buck converter. The PSpice simulation diagram is shown in Fig. 4-17 for the Buck-Boost converter, where, as discussed earlier, an ideal transformer is used for the average representation of the switching power-pole in CCM.

In Fig. 4-17, the dc voltage source represents the switch duty-ratio D and establishes the dc steady state, around which the circuit is linearized. In the ac analysis, the frequency of the ac source, which represents the duty-ratio perturbation \tilde{d} , is swept over the desired range, and the ratio of $\tilde{v}_o(s)$ and $\tilde{i}_L(s)$ yields the Bode plot of the power stage $G_{PS}(s)$, as shown in Fig. 4-18.

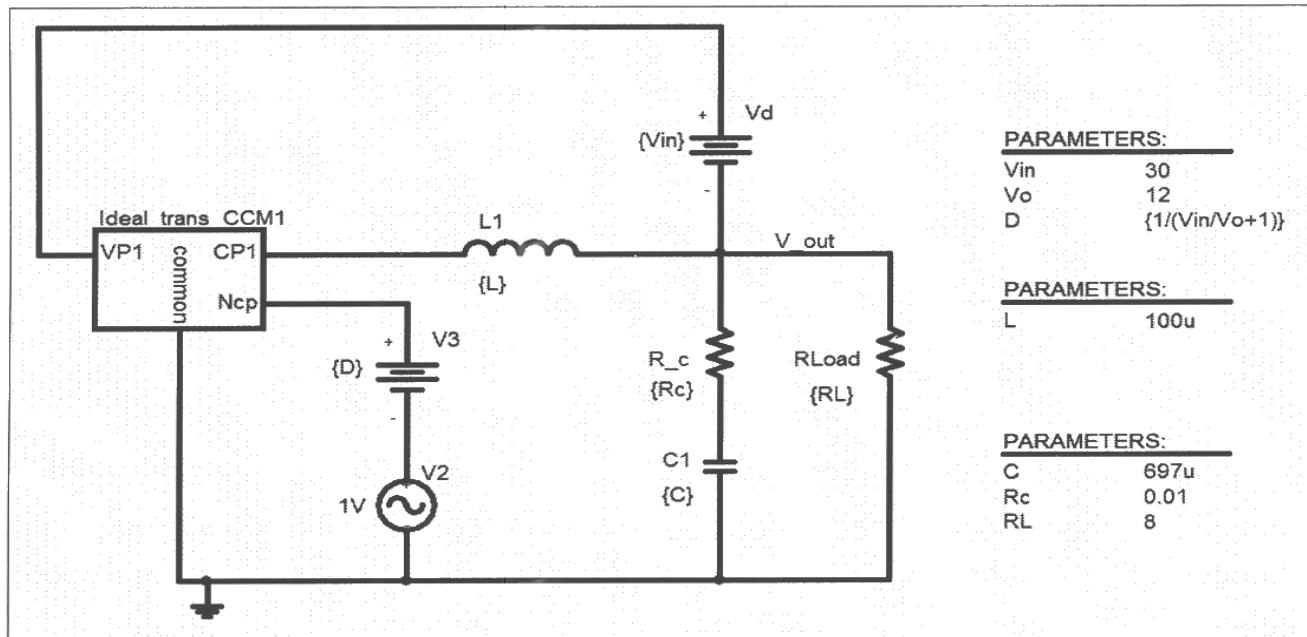


Figure 4-17 PSpice circuit for the Buck-Boost converter.

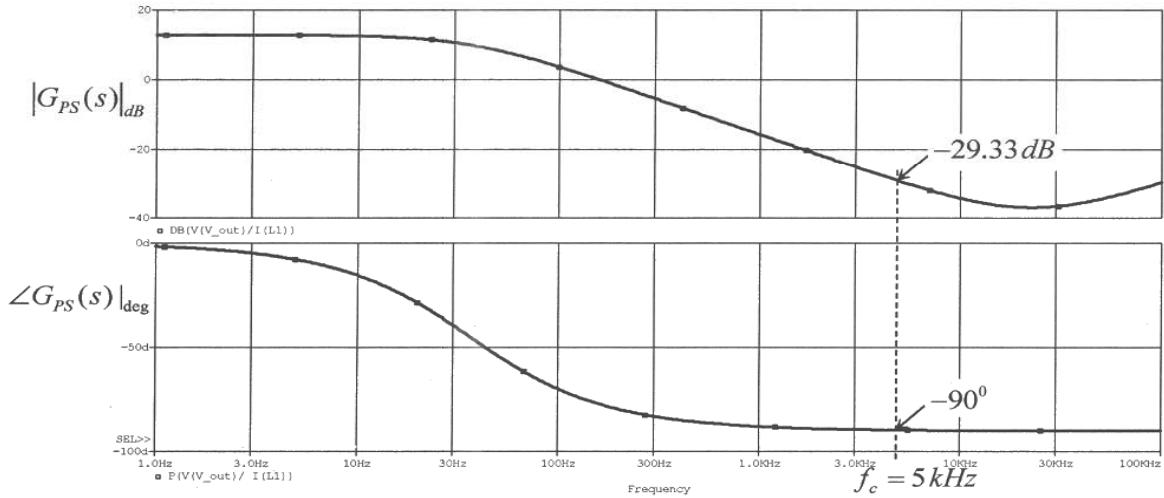


Figure 4-18 Bode plot of $\tilde{v}_o / \tilde{i}_L$.

As shown in Fig. 4-18, the phase angle of the power-stage transfer function levels off at approximately -90° at $\sim 1\text{kHz}$. The crossover frequency is chosen to be $f_c = 5\text{kHz}$, at which in Fig. 4-18, $\angle G_{PS}(s)|_{f_c} \approx -90^\circ$. As explained in the Appendix on the accompanying CD, the power-stage transfer function $\tilde{v}_o(s)/\tilde{i}_L(s)$ of Buck-Boost converters contains a right-half-plane zero in CCM. The crossover frequency is chosen well below the frequency of the right-half-plane zero for reasons discussed in the Appendix.

To achieve the desired phase margin of 60° , the controller transfer function is chosen as expressed as below:

$$G_C(s) = \frac{k_c}{s} \underbrace{\frac{(1 + s/\omega_z)}{(1 + s/\omega_p)}}_{\text{phase-boost}} \quad (4-32)$$

To yield zero steady state error, it contains a pole at the origin which introduces a -90° phase angle. The phase-boost required from this pole-zero combination in Eq. 4-32, using Eq. 4-22 and $\angle G_{PS}(s)|_{f_c} \approx -90^\circ$, is $\phi_{boost} \approx 60^\circ$. Therefore, unlike the controller transfer function of Eq. 4-18 for the voltage-mode control, only a single pole-zero pair is needed to provide phase boost. In Eq. 4-32, the zero and pole frequencies associated with the required phase boost can be derived, as shown in the Appendix on the accompanying CD, where K_{boost} is defined the same as in Eq. 4-26:

$$K_{boost} = \tan\left(45^\circ + \frac{\phi_{boost}}{2}\right) \quad (4-33)$$

$$f_z = \frac{f_c}{K_{boost}} \quad (4-34)$$

$$f_p = K_{boost} f_c \quad (4-35)$$

$$k_c = \omega_z |G_C(s)|_{f_c} \quad (4-36)$$

At the crossover frequency, as shown in Fig. 4-18, the power stage transfer function has a gain $|G_{PS}(s)|_{f_c} = -29.33 \text{ dB}$. Therefore, at the crossover frequency, by definition, in Fig. 4-16b

$$|G_C(s)|_{f_c} \times |G_{PS}(s)|_{f_c} = 1 \quad (4-37)$$

Hence,

$$|G_C(s)|_{f_c} = 29.33 \text{ dB} = 29.27 \quad (4-38)$$

Using the equations above for $f_c = 5 \text{ kHz}$, $\phi_{boost} \approx 60^\circ$, and $|G_C(s)|_{f_c} = 29.27$, $K_{boost} = 3.732$ in Eq. 4-32. Therefore, the parameters in the controller transfer function of Eq. 4-31 are calculated as $f_z = 1340 \text{ Hz}$, $f_p = 18660 \text{ Hz}$, and $k_c = 246.4 \times 10^3$.

The transfer function of Eq. 4-32 can be realized by an op-amp circuit shown in Fig. 4-19. In the expressions derived in the Appendix, selecting $R_1 = 10 \text{ k}\Omega$ and using the transfer-function parameters calculated above, the component values in the circuit of Fig. 4-19 are as follows:

$$\begin{aligned} C_2 &= \frac{\omega_z}{\omega_p R_1 k_c} = 30 \text{ pF} \\ C_1 &= C_2 (\omega_p / \omega_z - 1) = 380 \text{ pF} \\ R_2 &= 1 / (\omega_z C_1) = 315 \text{ k}\Omega \end{aligned} \quad (4-39)$$

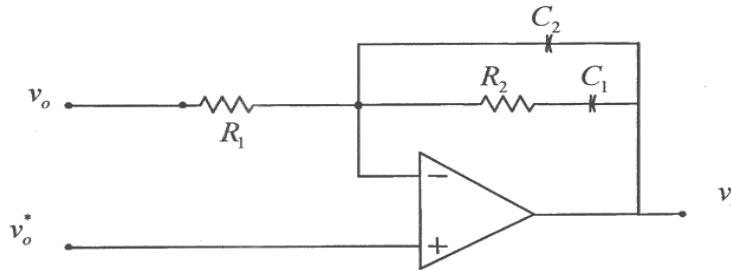


Figure 4-19 Implementation of controller in Eq. 4-32 by an op-amp circuit.

The PSpice circuit diagram is shown in Fig. 4-20 where a load change occurs at 3 ms. Using this simulation, the output voltage and its average are plotted in Fig. 4-21.

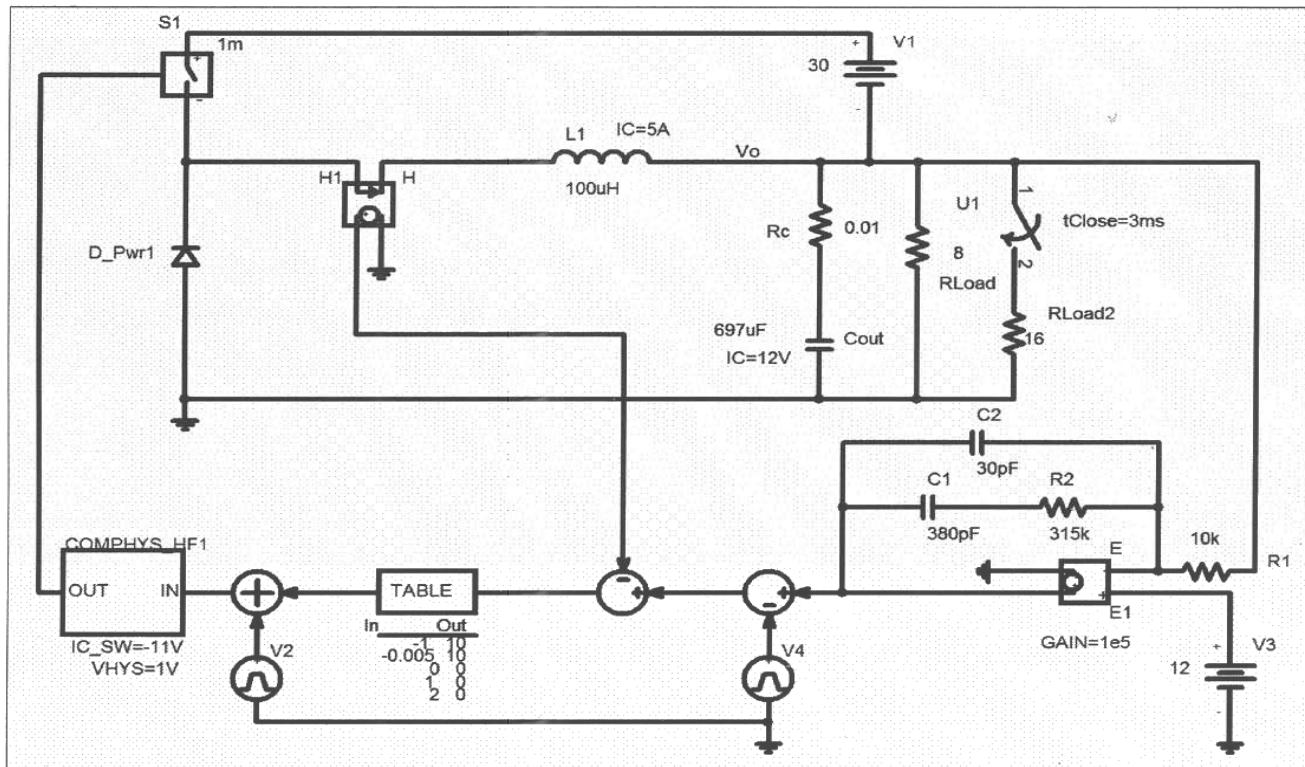


Figure 4-20 PSpice simulation diagram of the peak-current-mode control.

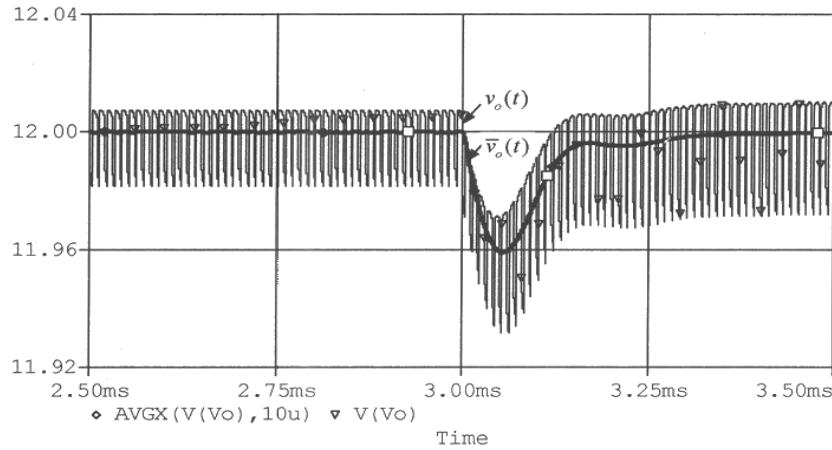


Figure 4-21 Peak current mode control: Output voltage waveform.

4-6 FEEDBACK CONTROLLER DESIGN IN DCM

In sections 4-4 and 4-5, feedback controllers were designed for CCM operation of the converters. The procedure for designing controllers in DCM is the same, except the average model of the power stage in PSpice simulations can be simply replaced by its model which is also valid in DCM, as described in Chapter 3.

REFERENCES

1. Unitrode PWM IC (www.unitrode.com)
2. H. Dean Venable, "The K-Factor: A New Mathematical Tool for Stability Analysis and Synthesis," Proceedings of Powercon 10 (<http://www.venable.biz>).
3. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.

PROBLEMS

- 4-1 In a voltage mode controlled DC-DC converter the loop transfer function has the crossover frequency $f_c = 2 \text{ kHz}$. The power stage transfer function has a phase angle of -160° at the crossover frequency. Calculate w_z and w_p in the voltage controller transfer function of Eq. 4-18, if the required phase margin is 60° .
- 4-2 In the above problem the power stage has a gain equal to 20 at the crossover frequency, $k_{FB} = 0.2$, and $G_{PWM} = 0.6$. Calculate k_c in the voltage controller transfer function of Eq. 4-18.
- 4-3 In a peak-current-mode controlled DC-DC converter the loop crossover frequency in the outer voltage loop is 10 kHz. At this crossover frequency, the power stage in Fig. 4-16b has the gain of 0.1, and the phase angle of -80° . Calculate f_z and f_p in the controller transfer function of Eq. 4-32 if the desired phase margin is 60° .

Chapter 5

RECTIFICATION OF UTILITY INPUT USING DIODE RECTIFIERS

5-1 INTRODUCTION

Power electronic systems generally get their power from the utility source, as shown by the block diagram in Fig. 5-1. Unless a corrective action is taken as described in the next chapter, this power is drawn by means of highly distorted currents, which have a deleterious effect on the power quality of the utility source. Furthermore, the power system disturbances in the utility source can disrupt the power electronics system's operation. Both of these issues are examined in this chapter.

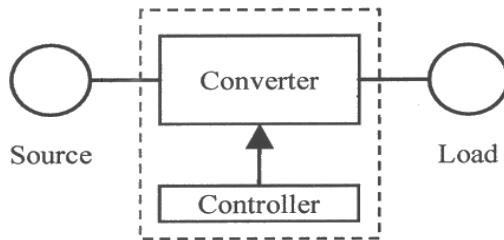


Figure 5-1 Block diagram of power electronic systems.

5-2 DISTORTION AND POWER FACTOR

To quantify distortion in the current drawn by power electronic systems, it is necessary to define certain indices. As a base case, consider the linear $R - L$ load shown in Fig. 5-2a which is supplied by a sinusoidal source in steady state. The voltage and current phasors are shown in Fig. 5-2b, where ϕ is the angle by which the current lags the voltage. Using rms values for the voltage and current magnitudes, the average power supplied by the source is

$$P = V_s I_s \cos \phi \quad (5-1)$$

The power factor (PF) at which power is drawn is defined as the ratio of the real average power P to the product of the rms voltage and the rms current:

$$PF = \frac{P}{V_s I_s} = \cos \phi \quad (\text{using Eq. 5-1}) \quad (5-2)$$

For a given voltage, from Eq. 5-2, the rms current drawn is

$$I_s = \frac{P}{V_s \cdot PF} \quad (5-3)$$

This shows that the power factor PF and the current I_s are inversely proportional. The current flows through the utility distribution lines, transformers, and so on, causing losses in their resistances. This is the reason why utilities prefer unity power factor loads that draw power at the minimum value of the rms current.

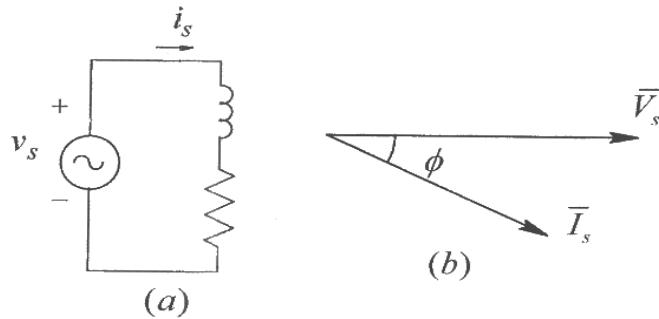


Figure 5-2 Voltage and current phasors in simple $R-L$ circuit.

5-2-1 RMS Value of Distorted Current and the Total Harmonic Distortion (THD)

The sinusoidal current drawn by the linear load in Fig. 5-2 has zero distortion. However, power electronic systems with diode rectifiers as the front-end draw currents with a distorted waveform such as that shown by $i_s(t)$ in Fig. 5-3a. The utility voltage $v_s(t)$ is assumed sinusoidal. The following analysis is general, applying to the utility supply that is either single-phase or three-phase, in which case the analysis is on a per-phase basis.

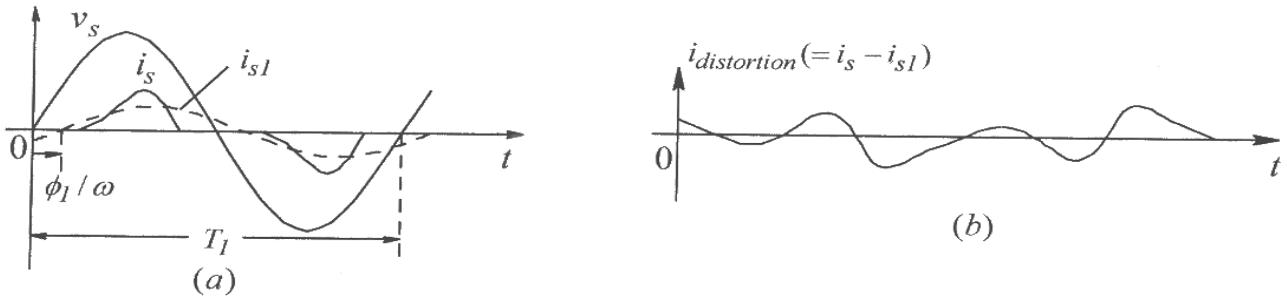


Figure 5-3 Current drawn by power electronics equipment with diode-bridge front-end.

The current waveform $i_s(t)$ in Fig. 5-3a repeats with a time-period T_1 . By Fourier analysis of this repetitive waveform, we can compute its fundamental frequency ($= 1/T_1$) component $i_{s1}(t)$, shown dotted in Fig. 5-3a. The distortion component $i_{distortion}(t)$ in the input current is the difference between $i_s(t)$ and the fundamental-frequency component $i_{s1}(t)$:

$$i_{distortion}(t) = i_s(t) - i_{s1}(t) \quad (5-4)$$

where $i_{distortion}(t)$ using Eq. 5-4 is plotted in Fig. 5-3b. This distortion component consists of components at frequencies that are the multiples of the fundamental frequency.

To obtain the rms value of $i_s(t)$ in Fig. 5-3a, we will apply the basic definition of rms:

$$I_s = \sqrt{\frac{1}{T_1} \int_{T_1} i_s^2(t) \cdot dt} \quad (5-5)$$

Using Eq. 5-4,

$$i_s^2(t) = i_{s1}^2(t) + i_{distortion}^2(t) + 2i_{s1}(t) \times i_{distortion}(t) \quad (5-6)$$

In a repetitive waveform, the integral of the products of the two harmonic components (including the fundamental) at unequal frequencies, over the repetition time-period, equals zero:

$$\int_{T_1} f_{h_1}(t) \cdot g_{h_2}(t) \cdot dt = 0 \quad h_1 \neq h_2 \quad (5-7)$$

Therefore, substituting Eq. 5-6 into Eq. 5-5, and making use of Eq. 5-7 that implies that the integral of the third term on the right side of Eq. 5-6 equals zero,

$$I_s = \sqrt{\underbrace{\frac{1}{T_1} \int_{T_1} i_{s1}^2(t) \cdot dt}_{I_{s1}^2} + \underbrace{\frac{1}{T_1} \int_{T_1} i_{distortion}^2(t) \cdot dt}_{I_{distortion}^2} + 0} \quad (5-8)$$

or,

$$I_s = \sqrt{I_{s1}^2 + I_{distortion}^2} \quad (5-9)$$

where the rms values of the fundamental-frequency component and the distortion component are as follows:

$$I_{s1} = \sqrt{\frac{1}{T_1} \int_{T_1} i_{s1}^2(t) \cdot dt} \quad (5-10)$$

and

$$I_{distortion} = \sqrt{\frac{1}{T_1} \int_{T_1} i_{distortion}^2(t) \cdot dt} \quad (5-11)$$

Based on the rms values of the fundamental and the distortion components in the input current $i_s(t)$, a distortion index called the Total Harmonic Distortion (THD) is defined in percentage as follows:

$$\%THD = 100 \times \frac{I_{\text{distortion}}}{I_{s1}} \quad (5-12)$$

Using Eq. 5-9 into Eq. 5-12,

$$\%THD = 100 \times \frac{\sqrt{I_s^2 - I_{s1}^2}}{I_{s1}} \quad (5-13)$$

The rms value of the distortion component can be obtained based on the harmonic components (except the fundamental) as follows using Eq. 5-7:

$$I_{\text{distortion}} = \sqrt{\sum_{h=2}^{\infty} I_{sh}^2} \quad (5-14)$$

where I_{sh} is the rms value of the harmonic component “ h ”.

▲ Example 5-1 A current i_s of square waveform is shown in Fig. 5-4a. Calculate and plot its fundamental frequency component and its distortion component. What is the %THD associated with this waveform?

Solution From Fourier analysis, $i_s(t)$ can be expressed as

$$i_s = \frac{4}{\pi} I (\sin \omega_1 t + \frac{1}{3} \sin 3\omega_1 t + \frac{1}{5} \sin 5\omega_1 t + \frac{1}{7} \sin 7\omega_1 t + \dots) \quad (5-15)$$

The fundamental frequency component and the distortion component are plotted in Figs. 5-4b and 5-4c.

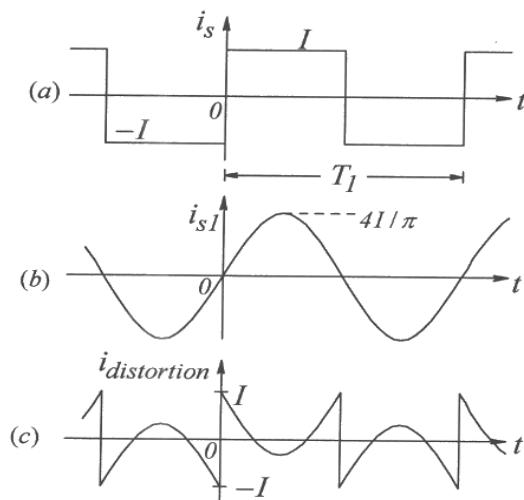


Figure 5-4 Example 5-1.

Since the rms value I_s of the square waveform is equal to I , the rms value of the distortion component can be calculated from using Eq. 5-9 in Eq. 5-15

$$I_{\text{distortion}} = \sqrt{I_s^2 - I_{s1}^2} = \sqrt{I^2 - (0.9I)^2} = 0.436I.$$

Therefore, using the definition of THD ,

$$\% THD = 100 \times \frac{I_{\text{distortion}}}{I_{s1}} = 100 \times \frac{0.436I}{0.9I} = 48.4\%. \quad \blacktriangle$$

5-2-2 The Displacement Power Factor (DPF) and Power Factor (PF)

Next, we will consider the power factor at which power is drawn by a load with a distorted current waveform such as that shown in Fig. 5-3a. As before, it is reasonable to assume that the utility-supplied line-frequency voltage $v_s(t)$ is sinusoidal, with an rms value of V_s and a frequency $f_1 (= \frac{\omega_1}{2\pi})$. Based on Eq. 5-7, which states that the product of the cross-frequency terms has a zero average, the average power P drawn by the load in Fig. 5-3a is due only to the fundamental-frequency component of the current:

$$P = \frac{1}{T_1} \int_{T_1} v_s(t) \cdot i_s(t) \cdot dt = \frac{1}{T_1} \int_{T_1} v_s(t) \cdot i_{s1}(t) \cdot dt \quad (5-16)$$

Therefore, in contrast to Eq. 5-1 for a linear load, in a load that draws distorted current, similar to Eq. 5-1

$$P = V_s I_{s1} \cos \phi_l \quad (5-17)$$

where ϕ_l is the angle by which the fundamental-frequency current component $i_{s1}(t)$ lags behind the voltage, as shown in Fig. 5-3a.

At this point, another term called the Displacement Power Factor (DPF) needs to be introduced, where

$$DPF = \cos \phi_l \quad (5-18)$$

Therefore, using the DPF in Eq. 5-17,

$$P = V_s I_{s1} (\text{DPF}) \quad (5-19)$$

In the presence of distortion in the current, the meaning and therefore the definition of the power factor, at which the real average power P is drawn, remains the same as in Eq. 5-2, that is, the ratio of the real power to the product of the rms voltage and the rms current:

$$PF = \frac{P}{V_s I_s} \quad (5-20)$$

Substituting Eq. 5-19 for P into Eq. 5-20,

$$PF = \left(\frac{I_{s1}}{I_s} \right) (DPF) \quad (5-21)$$

In linear loads that draw sinusoidal currents, the current-ratio (I_{s1}/I_s) in Eq. 5-21 is unity, hence $PF = DPF$. Eq. 5-21 shows the following: a high distortion in the current waveform leads to a low power factor, even if the DPF is high. Using Eq. 5-13, the ratio (I_{s1}/I_s) in Eq. 5-21 can be expressed in terms of the Total Harmonic Distortion as

$$\frac{I_{s1}}{I_s} = \frac{1}{\sqrt{1 + \left(\frac{\%THD}{100} \right)^2}} \quad (5-22)$$

Therefore, in Eq. 5-21,

$$PF = \frac{1}{\sqrt{1 + \left(\frac{\%THD}{100} \right)^2}} \cdot DPF \quad (5-23)$$

The effect of THD on the power factor is shown in Fig. 5-5 by plotting (PF/DPF) versus THD . It shows that even if the displacement power factor is unity, a total harmonic distortion of 100 percent (which is possible in power electronic systems unless corrective measures are taken) can reduce the power factor to approximately 0.7 (or $\frac{1}{\sqrt{2}} = 0.707$ to be exact), which is unacceptably low.

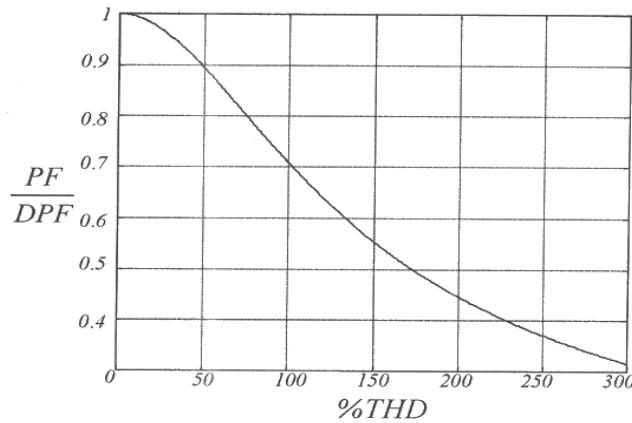


Figure 5-5 Relation between PF/DPF and THD.

5-2-3 Deleterious Effects of Harmonic Distortion and a Poor Power Factor

There are several deleterious effects of high distortion in the current waveform and the poor power factor that results due to it. These are as follows:

- Power loss in utility equipment such as distribution and transmission lines, transformers, and generators increases, possibly to the point of overloading them.
- Harmonic currents can overload the shunt capacitors used by utilities for voltage support and may cause resonance conditions between the capacitive reactance of these capacitors and the inductive reactance of the distribution and transmission lines.
- The utility voltage waveform will also become distorted, adversely affecting other linear loads, if a significant portion of the load supplied by the utility draws power by means of distorted currents.

5-2-3-1 Harmonic Guidelines

In order to prevent degradation in power quality, recommended guidelines (in the form of the IEEE-519) have been suggested by the IEEE (Institute of Electrical and Electronics Engineers). These guidelines place the responsibilities of maintaining power quality on the consumers and the utilities as follows: 1) on the power consumers, such as the users of power electronic systems, to limit the distortion in the current drawn, and 2) on the utilities to ensure that the voltage supply is sinusoidal with less than a specified amount of distortion.

The limits on current distortion placed by the IEEE-519 are shown in Table 5-1, where the limits on harmonic currents, as a ratio of the fundamental component, are specified for various harmonic frequencies. Also, the limits on the *THD* are specified. These limits are selected to prevent distortion in the voltage waveform of the utility supply.

Table 5-1 Harmonic current distortion (I_h/I_1)

I_{sc}/I_1	Odd Harmonic Order h (in %)					Total Harmonic Distortion (%)
	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	
< 20	4.0	2.0	1.5	0.6	0.3	5.0
20 – 50	7.0	3.5	2.5	1.0	0.5	8.0
50 – 100	10.0	4.5	4.0	1.5	0.7	12.0
100 – 1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

Therefore, the limits on distortion in Table 5-1 depend on the “stiffness” of the utility supply, which is shown in Fig. 5-6a by a voltage source \bar{V}_s in series with internal impedance Z_s . An ideal voltage supply has zero internal impedance. In contrast, the voltage supply at the end of a long distribution line, for example, will have large internal impedance.

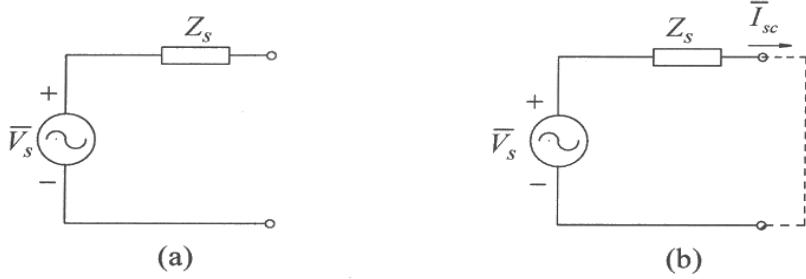


Figure 5-6 (a) Utility supply; (b) short circuit current.

To define the “stiffness” of the supply, the short-circuit current I_{sc} is calculated by hypothetically placing short-circuit at the supply terminals, as shown in Fig. 5-6b. The stiffness of the supply must be calculated in relation to the load current. Therefore, the stiffness is defined by a ratio called the Short-Circuit-Ratio (*SCR*):

$$\text{Short-Circuit-Ratio } SCR = \frac{I_{sc}}{I_{s1}} \quad (5-24)$$

where I_{s1} is the fundamental-frequency component of the load current. Table 5-1 shows that a smaller short-circuit ratio corresponds to lower limits on the allowed distortion in the current drawn. For the short-circuit-ratio of less than 20, the total harmonic distortion in the current must be less than 5 percent. Power electronic systems that meet this limit would also meet the limits of more stiff supplies.

It should be noted that the IEEE-519 does not propose harmonic guidelines for individual pieces of equipment but rather for the aggregate of loads (such as in an industrial plant) seen from the service entrance, which is also the point-of-common-coupling (PCC) with other customers. However, the IEEE-519 is frequently interpreted as the harmonic guidelines for specifying individual pieces of equipment such as motor drives. There are other harmonic standards, such as the IEC-1000, which apply to individual pieces of equipment.

5-3 CLASSIFYING THE “FRONT-END” OF POWER ELECTRONIC SYSTEMS

Interaction between the utility supply and power electronic systems depends on the “front-ends” (within the power-processing units), which convert line-frequency ac into dc. These front-ends can be broadly classified as follows:

- Diode-bridge rectifiers (shown in Fig. 5-7a) in which power flows only in one direction
- Switch-mode converters (shown in Fig. 5-7b) in which the power flow can reverse and the line currents are sinusoidal at the unity power factor
- Thyristor converters (shown in Fig. 5-7c) in which the power flow can be made bi-directional

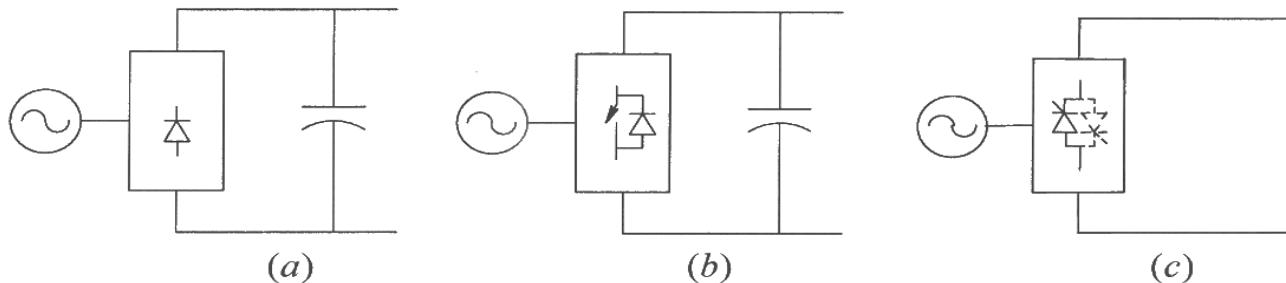


Figure 5-7 Front-end of power electronics equipment.

All of these front-ends can be designed to interface with single-phase or three-phase utility systems. In the following discussion, a brief description of the diode interface shown in Fig. 5-7a is provided, supplemented by analysis of results obtained through computer simulations. Interfaces using switch-mode converters in Fig. 5-7b and thyristor converters in Fig. 5-7c are discussed later in this book.

5-4 DIODE-RECTIFIER BRIDGE “FRONT-ENDS”

Most power electronic systems use diode-bridge rectifiers, like the one shown in Fig. 5-7a, even though they draw currents with highly distorted waveforms and the power through them can flow only in one direction. In switch-mode dc power supplies these diode-bridge rectifiers are supplemented by a power-factor-correction circuit, to meet current harmonic limits, as discussed in the next chapter.

Diode rectifiers rectify line-frequency ac into dc across the dc-bus capacitor, without any control over the dc-bus voltage. For analyzing the interaction between the utility and the power electronic systems, the switch-mode converter and the load can be represented by an equivalent resistance R_{eq} across the dc-bus capacitor. In our theoretical discussion, it is adequate to assume the diodes ideal.

In the following subsections, we will consider single-phase as well as three-phase diode rectifiers operating in steady state, where waveforms repeat from one line-frequency cycle $T_l (= 1/f_l)$ to the next.

5-4-1 Single-Phase Diode-Rectifier Bridge

At power levels below a few kW, for example in residential applications, power electronic systems are supplied by a single-phase utility source. A commonly used full-bridge rectifier circuit is shown in Fig. 5-8, in which L_s is the sum of the inductance internal to the utility supply and an external inductance, which may be intentionally added in series. Losses on the ac side can be represented by the series resistance R_s .

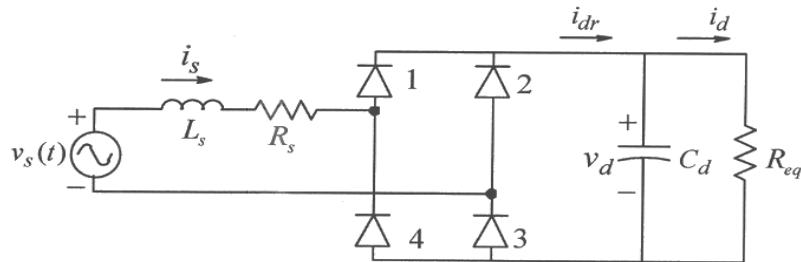


Figure 5-8 Full-bridge diode rectifier.

As shown in Fig. 5-9, at the beginning of the positive half-cycle of the input voltage v_s , the capacitor is already charged to a dc voltage v_d . So long as v_d exceeds the input voltage magnitude, all diodes get reverse biased and the input current is zero. Power to the equivalent resistance R_{eq} is supplied by the energy stored in the capacitor up to t_1 .

Beyond t_1 , the input current $i_s (= i_{dr})$ increases, flowing through diodes D_1 and D_2 . Beyond t_2 , the input voltage becomes smaller than the capacitor voltage and the input current begins to decline, falling to zero at t_3 . Beyond t_3 , until one-half cycle later than t_1 , the input current remains zero and the power to R_{eq} is supplied by the energy stored in the capacitor.

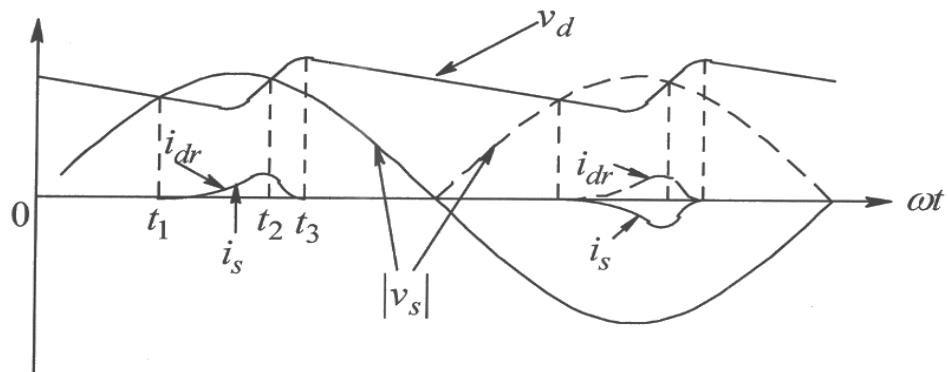


Figure 5-9 Current and voltage waveforms for the full-bridge diode rectifier.

At $(t_1 + \frac{T_1}{2})$ during the negative half-cycle of the input voltage, the input current flows through diodes D_3 and D_4 . The rectifier dc-side current i_{dr} continues to flow in the same direction as during the positive half-cycle; however, the input current $i_s = -i_{dr}$, as shown in Fig. 5-9. Fig. 5-10 shows waveforms obtained by PSpice simulations for two values of the ac-side inductance, with current THD of 86% and 62%, respectively (higher inductance reduces THD, as discussed in the next section).

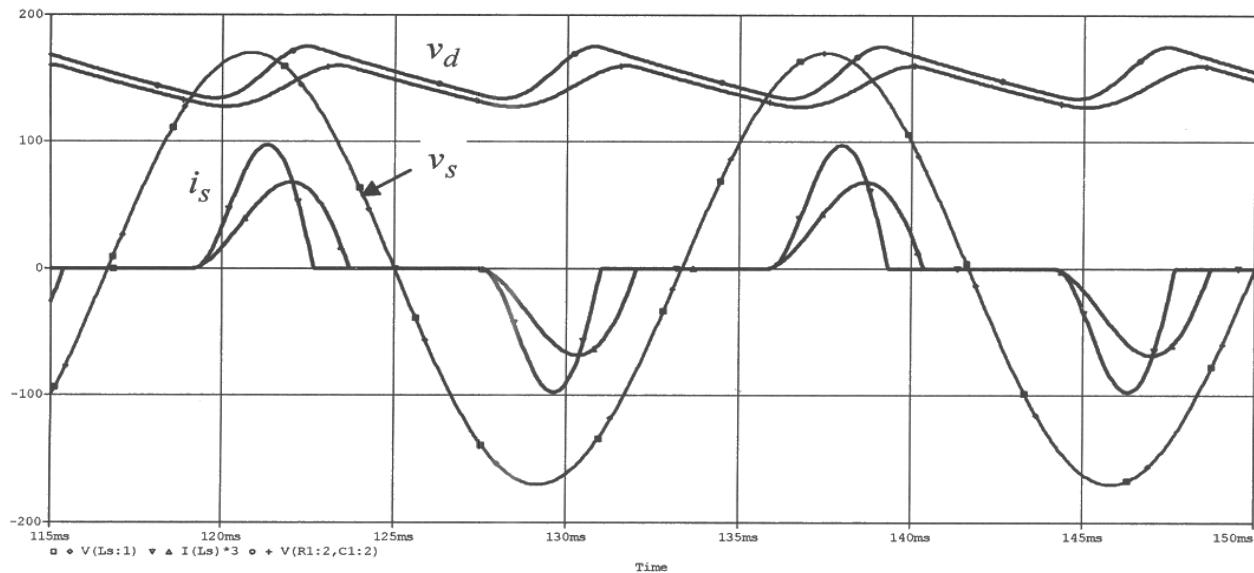


Figure 5-10 Single-phase diode-bridge rectification.

The fact that i_{dr} flows in the same direction during both the positive and the negative half-cycles represents the rectification process. In the circuit of Fig. 5-8 in steady state, all waveforms repeat from one cycle to the next. Therefore, the average value of the capacitor current over a line-frequency cycle must be zero so that the dc-bus voltage is in steady state. As a consequence, the average current through the equivalent load-resistance R_{eq} equals the average of the rectifier dc-side current; that is, $I_d = I_{dr}$.

5-4-1-1 Effects of L_s and C_d on the Waveforms and the THD

As Figs. 5-9 and 5-10 show, power is drawn from the utility supply by means of a pulse of current every half-cycle. The larger the “base” of this pulse during which the current flows, lower its peak value and the total harmonic distortion (THD). This pulse-widening can be accomplished by increasing the ac-side inductance L_s . Another parameter under the designer’s control is the value of the dc-bus capacitor C_d . At its minimum, it should be able to carry the ripple current in i_{dr} and in i_d (which in practice is the input dc-side current, with a pulsating waveform, of a switch-mode converter), and

keep the peak-to-peak ripple in the dc-bus voltage to some acceptable value, for example less than 5 percent of the dc-bus average value. Assuming that these constraints are met, lower the value of C_d , lower the THD and higher the ripple in the dc-bus voltage.

In practice, it is almost impossible to meet the harmonic limits specified by the IEEE-519 by using the above techniques. Rather, the power-factor-correction circuits described in the next chapter are needed to meet the harmonic specifications.

5-4-2 Three-Phase Diode-Rectifier Bridge

It is preferable to use a three-phase utility source, except at a fractional kilowatt, if such a supply is available. A commonly used Full-Bridge rectifier circuit is shown in Fig. 5-11a.

To understand the circuit operation, the rectifier circuit can be drawn as in Fig. 5-11b. The circuit consists of a top group and a bottom group of diodes. Initially, L_s is ignored and the dc-side current is assumed to flow continuously. At least one diode from each group must conduct to facilitate the flow of i_{dr} . In the top group, all diodes have their cathodes connected together. Therefore, the diode connected to the most positive voltage will conduct; the other two will be reverse biased. In the bottom group, all diodes have their anodes connected together. Therefore, the diode connected to the most negative voltage will conduct; the other two will be reverse biased.

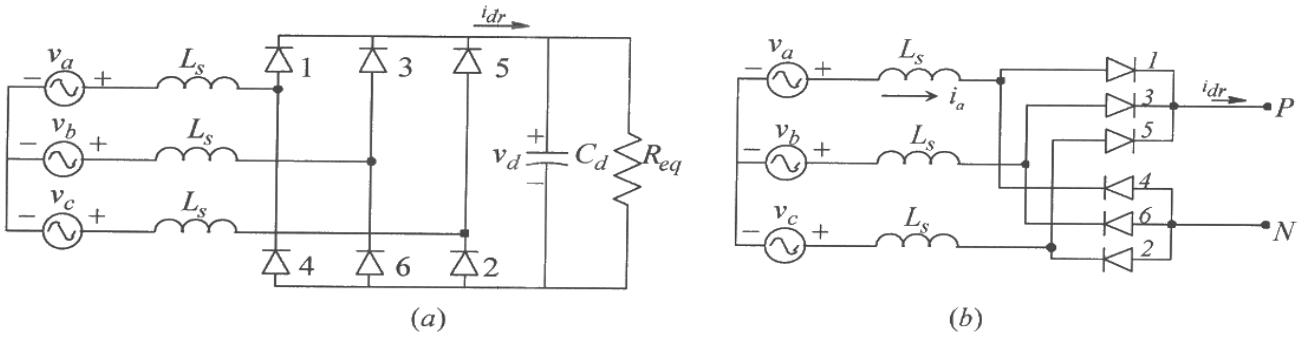


Figure 5-11 Three-phase diode bridge rectifier.

Ignoring L_s and assuming that the dc-side current i_{dr} is a pure dc, the waveforms are as shown in Fig. 5-12. In Fig. 5-12a, the waveforms (identified by the dark portions of the curves) show that each diode, based on the principle described above, conducts during 120° . The diodes are numbered so that they begin conducting sequentially: 1, 2, 3, and so on. The waveforms for the voltages v_p and v_N , with respect to the source-neutral, consist of 120° -segments of the phase voltages, as shown in Fig. 5-12a. The waveform of the dc-side voltage $v_d (= v_p - v_N)$ is shown in Fig. 5-12b. It consists of 60° -segments of the line-line voltages supplied by the utility. Line currents on the ac-side are as shown

in Fig. 5-12c. For example, phase-a current flows for 120° during each half-cycle of the phase-a input voltage; it flows through diode D_1 during the positive half-cycle of v_a , and through diode D_4 during the negative half-cycle.

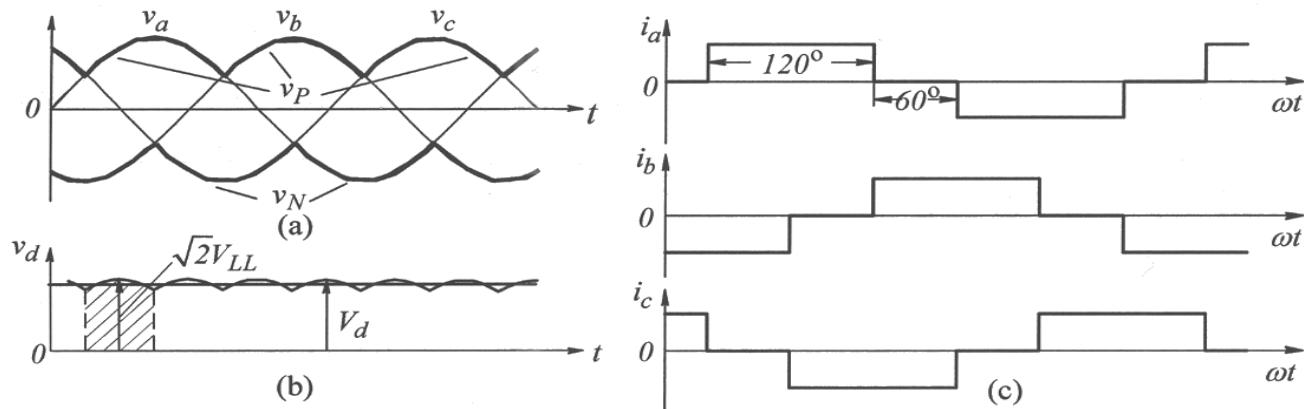


Figure 5-12 Waveforms in a three-phase rectifier (a constant i_{dr}).

The average value of the dc-side voltage can be obtained by considering only a 60° -segment in the 6-pulse (per line-frequency cycle) waveform shown in Fig. 5-12b. Let us consider the instant of the peak in the 60° -segment to be the time-origin, with \hat{V}_{LL} as the peak line-line voltage. The average value V_d can be obtained by calculating the integral from $\omega t = -\pi/6$ to $\omega t = \pi/6$ (the area shown by the hatched area in Fig. 5-12b) and then dividing by the interval $\pi/3$:

$$V_d = \frac{1}{\pi/3} \int_{-\pi/6}^{\pi/6} \hat{V}_{LL} \cos \omega t \cdot d(\omega t) = \frac{3}{\pi} \hat{V}_{LL} \quad (5-25)$$

This average value is plotted as a straight line in Fig. 5-12b. In the three-phase rectifier of Fig. 5-11a with the dc-bus capacitor filter, the input current waveforms obtained by computer simulations are shown in Fig. 5-13.

Fig. 5-13a shows that the input current waveform within each half-cycle consists of two distinct pulses when L_s is small. For example, in the i_a waveform during the positive half-cycle, the first pulse corresponds to the flow of dc-side current through the diode pair (D_1, D_6) and then through the diode pair (D_1, D_2). At larger values of L_s , within each half-cycle, the input current between the two pulses does not go to zero, as shown in Fig. 5-13b.

The effects of L_s and C_d on the waveforms can be determined by a parametric analysis, similar to the case of single-phase rectifiers. The THD in the current waveform of Fig. 5-13b is much smaller than in Fig. 5-13a (23% versus 82%). The ac-side inductance L_s is

required to provide a line-frequency reactance X_{L_s} ($= 2\pi f_l L_s$) that is typically greater than 2 percent of the base impedance Z_{base} , which is defined as follows:

$$\text{Base Impedance } Z_{base} = 3 \frac{V_s^2}{P} \quad (5-26)$$

where P is the three-phase power rating of the power electronic system, and V_s is the rms value of the phase voltage. Therefore, typically, the minimum ac-side inductance should be such that

$$X_{L_s} \geq (0.02 \times Z_{base}) \quad (5-27)$$

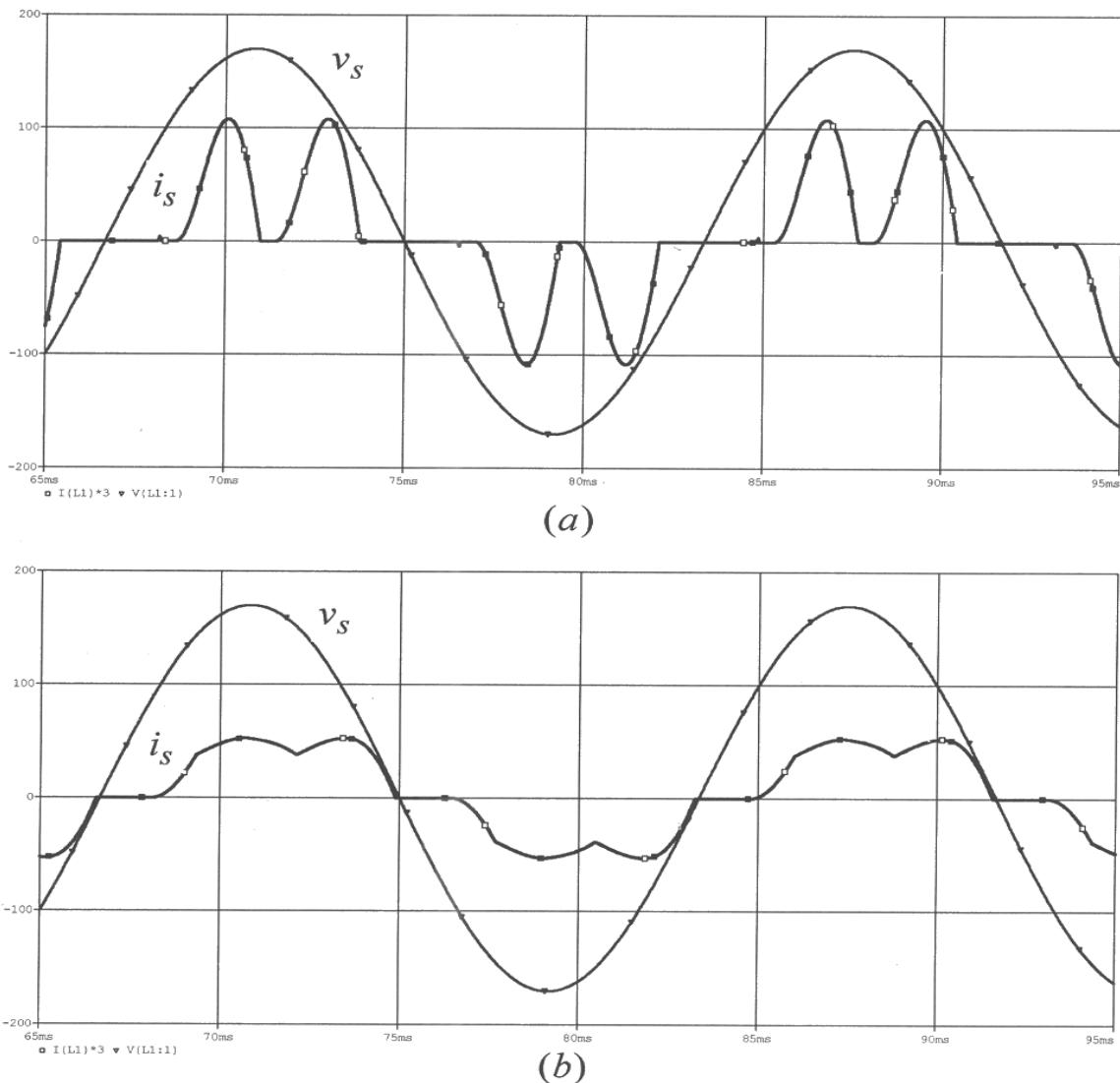


Figure 5-13 Effect of L_s variation (a) $L_s = 0.1 \text{ mH}$; (b) $L_s = 3 \text{ mH}$.

5-4-3 Comparison of Single-Phase and Three-Phase Rectifiers

Examination of single-phase and three-phase rectifier waveforms shows the differences in their characteristics. Three-phase rectification results in six identical “pulses” per cycle in the rectified dc-side voltage, whereas single-phase rectification in two such pulses. Therefore, three-phase rectifiers are superior in terms of minimizing distortion in line currents and ripple across the dc-bus voltage. Consequently, as stated earlier, three-phase rectifiers should be used if a three-phase supply is available. However, three-phase rectifiers, just like single-phase rectifiers, are also unable to meet the harmonic limits specified by the IEEE-519 unless corrective actions such as those described in Chapter 12 are taken.

5-5 Means to Avoid Transient Inrush Currents at Starting

In power electronic systems with rectifier front-ends, it may be necessary to take steps to avoid a large inrush of current at the instant the system is connected to the utility source. In such power electronic systems, the dc-bus capacitor is very large and initially has no voltage across it. Therefore, at the instant the switch in Fig. 5-14a is closed to connect the power electronic system to the utility source, a large current flows through the diode-bridge rectifier, charging the dc-bus capacitor.

This transient current inrush is highly undesirable; fortunately, several means of avoiding it are available. These include using a front-end that consists of thyristors discussed in Chapter 14 or using a series semiconductor switch as shown in Fig. 5-14b. At the instant of starting, the resistance across the switch lets the dc-bus capacitor get charged without a large inrush current, and subsequently the semiconductor switch is turned on to bypass the resistance.

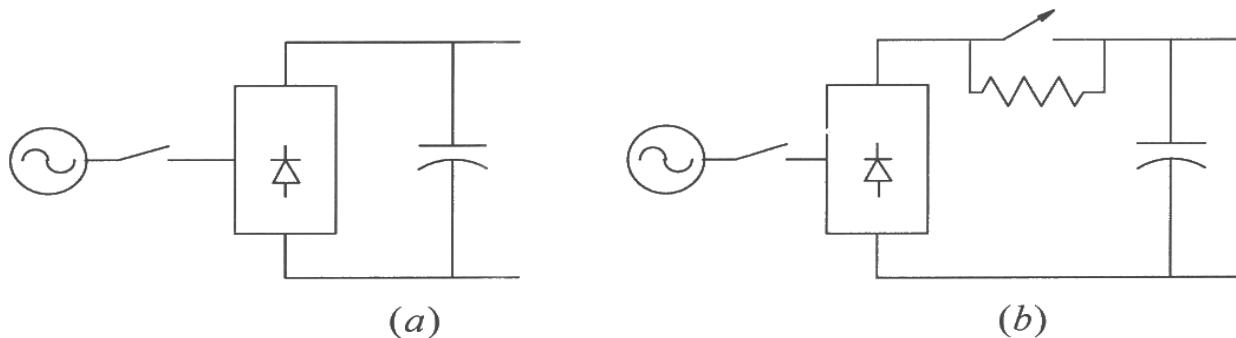


Figure 5-14 Means to avoid inrush current.

5-6 FRONT-ENDS WITH BI-DIRECTIONAL POWER FLOW

In stop-and-go applications such as elevators, it is cost-effective to feed the energy recovered by regenerative braking of the motor drive back into the utility supply. Converter arrangements for such applications are considered in Chapter 12.

REFERENCES

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.
2. N. Mohan, *Power Electronics: Computer Simulation, Analysis and Education using PSpice™*, a complete simulation package available from www.mnpere.com.

PROBLEMS

- 5-1 In a single-phase diode rectifier bridge, $I_s = 10 \text{ A(rms)}$, $I_{s1} = 8 \text{ A(rms)}$, and $DPF = 0.9$. Calculate $I_{distortion}$ and $\%THD$.
- 5-2 In a single-phase diode bridge rectifier circuit, the following operating condition are given: $V_s = 120 \text{ V(rms)}$, $P = 1 \text{ kW}$, $I_{s1} = 10 \text{ A}$, and $THD = 80\%$. Calculate the following: DPF , $I_{distortion}$, I , and PF .
- 5-3 In a single-phase rectifier the input current can be approximated to have a triangular waveform every half cycle with a peak of 10 A and a base of 60° . Calculate the rms current through each diode.
- 5-4 In the above problem, calculate the ripple component in the dc-side current that will flow through the dc-side capacitor.
- 5-5 Repeat Example 5-1 if the current waveform is a rectangular pulse as shown in Fig 5-12c in a three-phase rectifier, with an amplitude of 10 A .

Chapter 6

POWER-FACTOR-CORRECTION (PFC) CIRCUITS AND DESIGNING THE FEEDBACK CONTROLLER

6-1 INTRODUCTION

Technical solutions to the problem of distortion in the input current have been known for a long time. However, only recently has the concern about the deleterious effects of harmonics led to the formulation of guidelines and standards, which in turn have focused attention on ways of limiting current distortion.

In the following sections, power-factor-corrected (*PFC*) interface, as they are often called, are briefly examined for single-phase rectification, where it is assumed that the power needs to flow only in one direction, such as in dc power supplies. The three-phase front-ends in motor-drives applications may require bi-directional power flow capability. Such front-ends, which also allow unity power factor of operation, are discussed in Chapter 12.

6-2 OPERATING PRINCIPLE OF SINGLE-PHASE PFCs

Operating principle of a commonly used single-phase *PFC* is shown in Fig. 6-1a where, between the utility supply and the dc-bus capacitor, a Boost dc-dc converter is introduced. This Boost converter consists of a MOSFET, a diode, and a small inductor L_d . By pulse-width-modulating the MOSFET at a constant switching frequency, the current i_L through the inductor L_d is shaped to have the full-wave-rectified waveform $|\sin \omega t|$, similar to $|v_s(t)|$, as shown in Fig. 6-1b. The inductor current contains high switching-frequency ripple, which is removed by a small filter, and the input current i_s is sinusoidal, and in phase with the supply voltage. In the Boost converter, it is essential that the dc-bus voltage V_d be greater than the peak of the supply voltage \hat{V}_s :

$$V_d > \hat{V}_s \quad (6-1)$$

Using the average model of the Boost converter as shown in Fig. 6-2a and neglecting a small voltage drop across the inductor and assuming the voltage across the capacitor to be a pure dc,

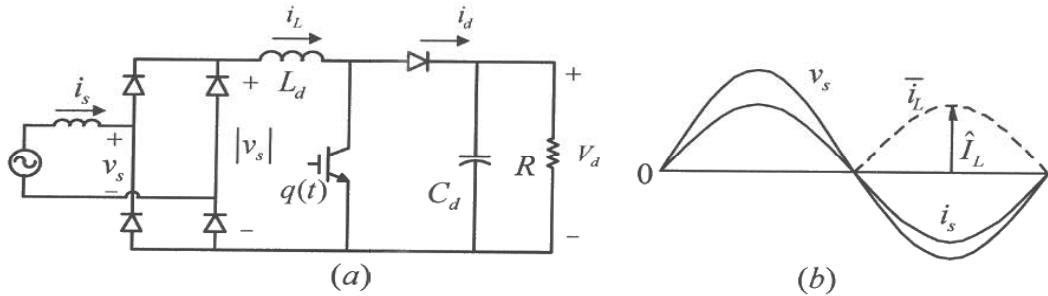


Figure 6-1 PFC circuit and waveforms.

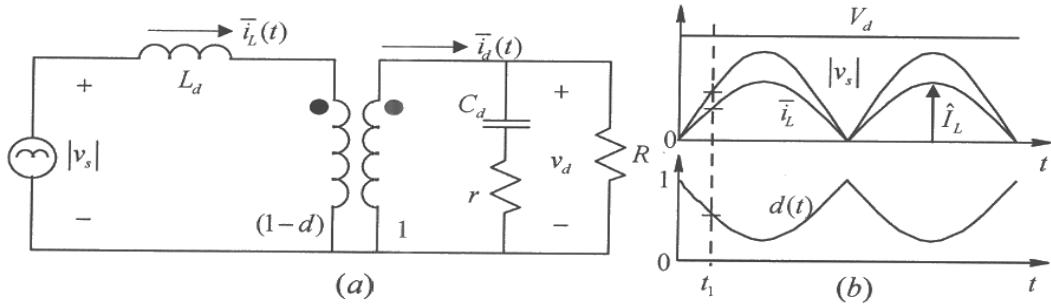


Figure 6-2 Average model and waveforms.

$$\frac{V_d}{|v_s|} = \frac{1}{1 - d(t)} \quad (6-2)$$

thus,

$$d(t) = 1 - \frac{\hat{V}_s |\sin(\omega t)|}{V_d} \quad (6-3)$$

The switch duty-ratio in the average circuit of Fig. 6-2a is plotted in Fig. 6-2b. The output-stage current $\bar{i}_d(t)$ can be calculated from the ideal transformer in Fig. 6-2a in terms of $|v_s| = \hat{V}_s |\sin \omega t|$ and $\bar{i}_L(t) = \hat{I}_L |\sin \omega t|$, and by using Eq. 6-2,

$$\bar{i}_d(t) = (1 - d)\bar{i}_L(t) = \frac{\hat{V}_s}{V_d} \hat{I}_L |\sin \omega t|^2 \quad (6-4)$$

Recognizing that in Eq. 6-4, $|\sin \omega t|^2 = \sin^2 \omega t = \frac{1}{2} - \frac{1}{2} \cos 2\omega t$:

$$\bar{i}_d = \underbrace{\frac{1}{2} \frac{\hat{V}_s}{V_d} \hat{I}_L}_{I_d} - \underbrace{\frac{1}{2} \frac{\hat{V}_s}{V_d} \hat{I}_L \cos 2\omega t}_{i_{d2}(t)} \quad (6-5)$$

Eq. 6-5 shows that the average current to the output stage consists of a dc component I_d and a component $i_{d2}(t)$ at the second-harmonic component. In PFCs, the capacitor in the output stage shown in Fig. 6-3 is quite large such that it is justifiable to approximate that

all the second-harmonic ripple flows through the output capacitor, and only I_d flows through the load equivalent resistor. Based on this assumption, the second-harmonic ripple in the output voltage can be calculated as

$$v_{d2}(t) = \frac{1}{\omega C} \int i_{d2} \cdot d(\omega t) \quad (6-6)$$

Substituting i_{d2} from Eq. 6-5 into Eq. 6-6,

$$v_{d2} = -\frac{1}{\omega C} \frac{\hat{I}_L}{2} \frac{\hat{V}_s}{V_d} \int \cos 2\omega t \cdot d(\omega t) = -\underbrace{\left(\frac{\hat{I}_L \hat{V}_s}{4\omega C V_d} \right)}_{\hat{V}_{d2}} \sin 2\omega t \quad (6-7)$$

where

$$\hat{V}_{d2} = \frac{\hat{I}_L}{4\omega C} \frac{\hat{V}_s}{V_d} \quad (6-8)$$

is the peak value of the ripple in the output capacitor. It depends inversely on the output capacitance, and therefore an appropriate value must be chosen to minimize this ripple.

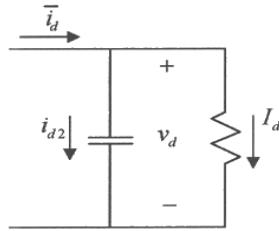


Figure 6-3 Current division in the output stage.

6-3 CONTROL OF PFCs

In controlling a PFC, the main objective is to draw a sinusoidal current, in-phase with the utility voltage. The reference inductor current $i_L^*(t)$ is of the full-wave rectified form, similar to that in Fig. 6-1b. The requirements on the form and the amplitude of the inductor current lead to two control loops, as shown in Fig. 6-4, to pulse-width modulate the switch of the Boost converter:

- The inner current loop ensures the form of $i_L^*(t)$ based on the utility voltage $v_s(t)$.
- The outer voltage loop determines the amplitude \hat{I}_L of $i_L^*(t)$ based on the output voltage feedback. If the inductor current is insufficient for a given load supplied by the PFC, the output voltage will drop below its pre-selected reference value V_d^* . By measuring the output voltage and using it as the feedback signal, the voltage loop adjusts the inductor current amplitude to bring the output voltage to

its reference value. In addition to determining the inductor current amplitude, this voltage feedback control acts to regulate the output voltage of the PFC to the pre-selected dc voltage.

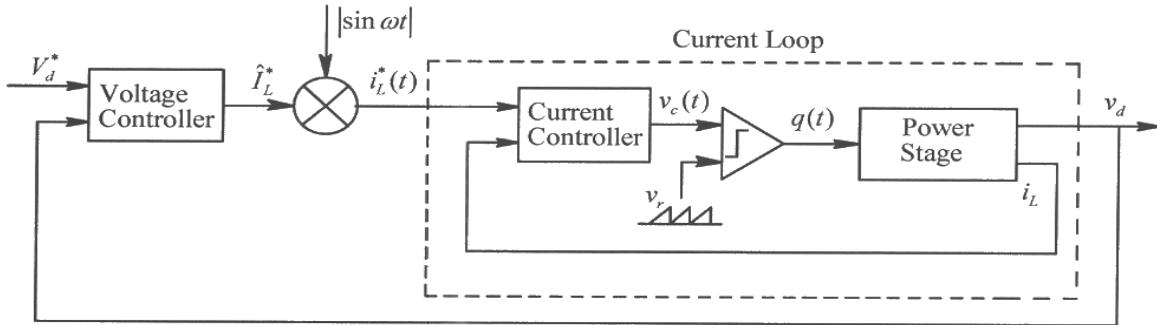


Figure 6-4 PFC control loops.

Fortunately, in Fig. 6-4, the inner current loop is required to have a very high bandwidth compared to the outer voltage loop. Hence, each loop can be designed separately, similar to the approach taken in the peak-current-mode control discussed Chapter 4.

6-4 DESIGNING THE INNER AVERAGE-CURRENT-CONTROL LOOP

The inner current loop is shown within the dotted box in Fig. 6-4. In order to follow the reference with as little THD as possible, an average-current-mode control is used with a high bandwidth, where the error between the reference $i_L^*(t)$ and the measured inductor current $i_L(t)$ is amplified by a current controller to produce the control voltage $v_c(t)$. This control voltage is compared with a ramp signal $v_r(t)$, with a peak of \hat{V}_r at the switching-frequency f_s in the PWM controller IC [1], to produce the switching signal $q(t)$.

Just the inner current loop of Fig. 6-4 can be simplified, as shown in Fig. 6-5a. The reference input $i_L^*(t)$ varies with time as shown in Fig. 6-2b, where the corresponding $v_s(t)$ and $d(t)$ waveforms are also plotted. However, these quantities vary much more slowly compared to the control-loop bandwidth, approximately 10 kHz in the numerical example considered later on. Therefore, at each instant of time, for example at t_1 in Fig. 6-2b, the circuit of Fig. 6-2a can be considered in a “dc” steady state with the associated variables having values of $i_L(t_1)$, $v_s(t_1)$ and $d(t_1)$. This equilibrium condition slowly varies with time, and the current loop is designed to have a large bandwidth around each dc steady state. In Laplace domain, this current loop is shown in Fig. 6-5b, as discussed below, where “~” on top represents small signal perturbations at very high frequencies in the range of the current-loop bandwidth, for example 10 kHz.

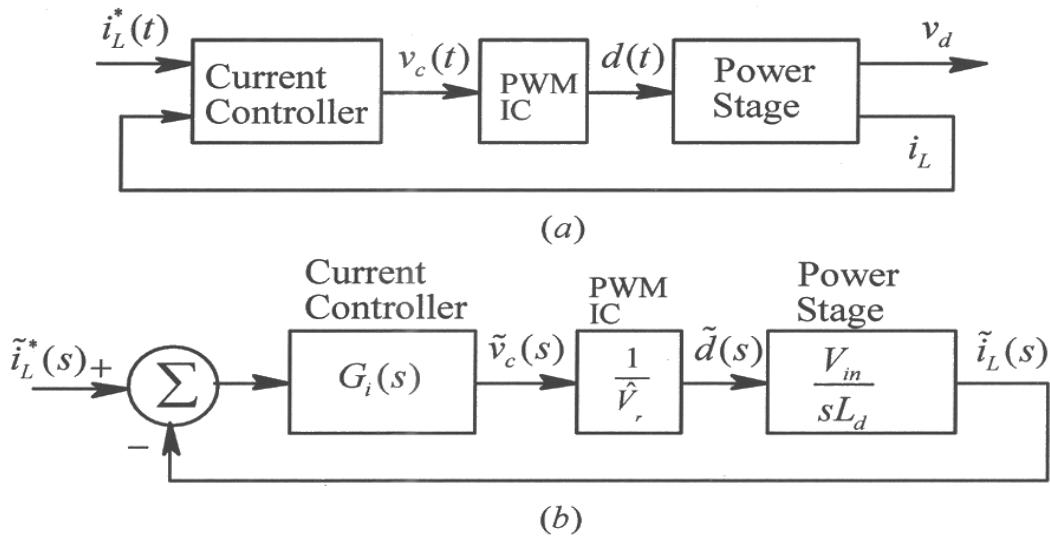


Figure 6-5 PFC current loop.

6-4-1 $\tilde{d}(s)/\tilde{v}_c(s)$ for the PWM Controller

If \hat{V}_r is the difference between the peak and the valley of the ramp voltage in the PWM-IC, then the small-signal transfer function of the PWM controller, as discussed in Chapter 4 is

$$\text{PWM Controller Transfer Function } \frac{\tilde{d}(s)}{\tilde{v}_c(s)} = \frac{1}{\hat{V}_r} \quad (6-9)$$

6-4-2 $\tilde{i}_L(s)/\tilde{d}(s)$ for the Boost Converter in the Power Stage

As described in the Appendix on the accompanying CD, in spite of the varying dc steady state operating point, the transfer function in the Boost converter simplifies as follows at high frequencies, where the current loop has likely to have its bandwidth:

$$\frac{\tilde{i}_L(s)}{\tilde{d}(s)} \approx \frac{V_d}{sL_d} \quad (6-10)$$

6-4-3 Designing the Current Controller $G_i(s)$

The transfer function in Eq. 6-10 is an approximation valid at high frequencies, and not a pure integrator. Therefore, to have a high loop dc gain and a zero dc steady state error in Fig. 6-5b, the current controller transfer function $G_i(s)$ must have a pole at the origin. In the loop in Fig. 6-5b, the phase due to the pole at origin in $G_i(s)$ and that of the power-stage transfer function (Eq. 6-10) add up to -180° . Hence, $G_i(s)$, as in the peak-current mode control discussed in Chapter 4, includes a pole-zero pair that provides a phase

boost, and hence the specified phase margin, for example 60° at the loop crossover frequency:

$$G_i(s) = \frac{k_c}{s} \frac{1 + s/\omega_z}{\underbrace{1 + s/\omega_p}_{\text{phase boost}}} \quad (6-11)$$

where, k_c is the amplifier gain. Knowing the phase boost, ϕ_{boost} , we can calculate the pole-zero locations to provide the necessary phase boost, as discussed in Chapter 4:

$$K_{boost} = \tan(45^\circ + \frac{\phi_{boost}}{2}) \quad (6-12)$$

$$f_z = \frac{f_{ci}}{K_{boost}} \quad (6-13)$$

$$f_p = K_{boost} f_{ci} \quad (6-14)$$

where f_{ci} is the crossover frequency of the current loop transfer function.

6-5 DESIGNING THE OUTER VOLTAGE LOOP

As mentioned earlier, the outer voltage loop is needed to determine the peak, \hat{I}_L , of the inductor current. In this voltage loop, the bandwidth is limited to approximately 15 Hz. The reason has to do with the fact that the output voltage across the capacitor contains a component v_{d2} as derived in Eq. 6-7 at twice the line-frequency (at 120 Hz in 60-Hz line-frequency systems). This output voltage ripple must not be corrected by the voltage loop, otherwise it will lead to third-harmonic distortion in the input current, as explained in the Appendix on the accompanying CD.

In view of such a low bandwidth of the voltage loop (approximately three orders of magnitude below the current-loop bandwidth of ~ 10 kHz), it is perfectly reasonable to assume the current loop ideal at low frequencies around 15 Hz. Therefore, in the voltage-control block diagram shown in Fig. 6-6a, the current closed-loop produces \hat{I}_L equal to its reference value \hat{I}_L^* . In addition to a large dc component, \hat{I}_L^* contains an unwanted second-harmonic component \hat{I}_{L2} due to v_{d2} (Eq. 6-7) in the input to the voltage controller. \hat{I}_{L2} at the second-harmonic component results in a third-harmonic distortion in the current drawn from the utility, as explained in the Appendix on the accompanying CD. Therefore, in the output of the voltage controller block in Fig. 6-6a, \hat{I}_{L2} is limited to approximately 1.5% of the dc component in \hat{I}_L^* .

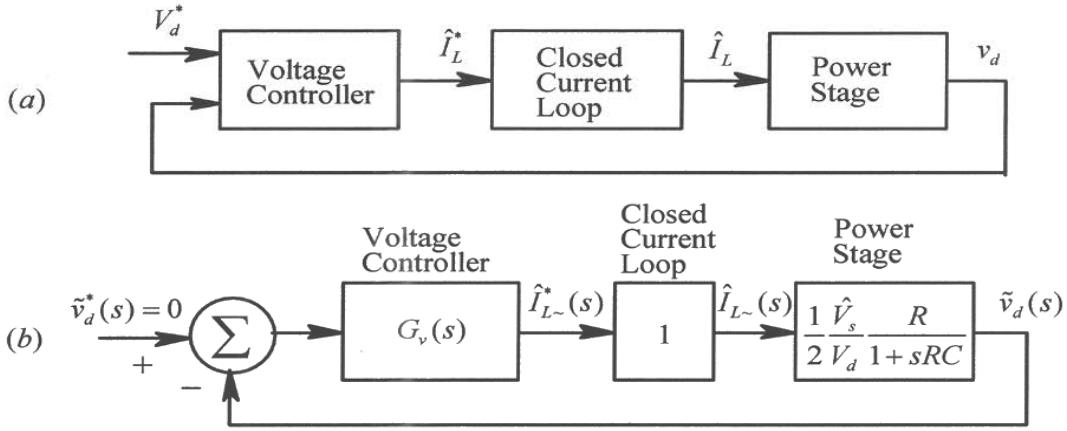


Figure 6-6 Voltage control loop.

The voltage control loop for low-frequency perturbations, in the range of the voltage-loop bandwidth of approximately 15 Hz, is shown in Fig. 6-6b. As derived in the Appendix on the accompanying CD, the transfer function of the power stage in Fig. 6-6b at these low perturbation frequencies (ignoring the capacitor ESR) is:

$$\frac{\tilde{v}_d(s)}{\hat{I}_{L\sim}(s)} = \frac{1}{2} \frac{\hat{V}_s}{V_d} \frac{R}{1 + sRC} \quad (6-15)$$

To achieve a zero steady state error, the voltage-controller transfer function should have a pole at the origin. However, since the PFC circuit is often a pre-regulator (not a strict regulator), this requirement is waived, which otherwise would make the voltage controller design much more complicated. The following simple transfer function is often used for the voltage controller in Fig. 6-6b, where a pole is placed at the voltage-loop crossover frequency ω_{cv} (yet to be determined) below 15 Hz

$$G_v(s) = \frac{k_v}{1 + s/\omega_{cv}} \quad (6-16)$$

At full-load, the power stage transfer function given by Eq. 6-15 has a pole at a very low frequency, for example of the order of one or two Hz, which introduces a phase lag approaching 90 degrees much beyond the frequency at which this pole occurs. The transfer function of the controller given by Eq. 6-16 introduces a lag of 45 degrees at the loop crossover frequency. Therefore, these two phase lags of $\sim 135^\circ$ at the crossover frequency result in a satisfactory phase margin of 45° . By definition, at the crossover frequency f_{cv} , the loop transfer function has a magnitude equal to unity

$$\left| \frac{k_v}{1 + s/\omega_{cv}} \frac{1}{2} \frac{\hat{V}_s}{V_d} \frac{R}{1 + sRC} \right|_{f_{cv}} = 1 \quad (6-17)$$

At the second-harmonic in the voltage controller of Eq. 6-16,

$$\left| \frac{k_v}{1 + s/\omega_{cv}} \right|_{s=j(2\pi \times 120)} = \frac{\hat{I}_{L2}}{\hat{V}_{d2}} \quad (6-18)$$

From Eqs. 6-17 and 6-18, the two unknowns k_v and ω_{cv} in the voltage controller transfer function of Eq. 6-16 can be calculated, as described by a numerical example.

6-6 EXAMPLE OF SINGLE-PHASE PFC SYSTEMS

The operation and control of a PFC is demonstrated by means of an example, where the parameters are as follows in Table 6-1, and the total harmonic distortion in the input line current is required to be less than 3 percent [1, 2]:

Table 6-1
Parameters and Operating Values

Nominal input ac source voltage, $V_{s,rms}$	120V
Line frequency, f	60 Hz
Output Voltage, V_d	250V (dc)
Maximum Power Output	250W
Switching Frequency, f_s	100 kHz
Output Filter capacitor, C	220 μF
ESR of the Capacitor, r	100 m Ω
Inductor, L_d	1 mH
Full-Load Equivalent Resistance, R	250 Ω

6-6-1 Design of the Current Loop

In Eq. 6-9, \hat{V}_r is given as unity. Following the procedure described in Chapter 4 for the peak-current-mode control of dc-dc converters, for the loop crossover frequency of 10 kHz ($\omega_{ci} = 2\pi \times 10^4$ rad/s) and the phase margin of 60° , the parameters in the current controller of Eq. 6-11 are as follows:

$$\begin{aligned} k_c &= 4212 \\ \omega_z &= 1.68 \times 10^4 \text{ rad/s} \\ \omega_p &= 2.35 \times 10^5 \text{ rad/s} \end{aligned} \quad (6-19)$$

Based on these parameter values given in Eq. 6-19 of the transfer function $G_v(s)$ in Eq. 6-11, the op-amp circuit is similar to Fig. 4-19 in Chapter 4 with the following values for a chosen value of $R_1 = 100 k\Omega$:

$$\begin{aligned} C_2 &\approx 0.17 nF \\ C_1 &\approx 2.2 nF \\ R_2 &\approx 27 k\Omega \end{aligned} \quad (6-20)$$

6-6-2 Design of the Voltage Loop

In this example at full-load, the plant transfer function given by Eq. 6-15 has a pole at the frequency of 18.18 rad/s (2.89 Hz). At full-load, $\hat{I}_L = 2.946 A$, and in Eq. 6-8, $\hat{V}_{d2} = 6.029 V$. Based on the previous discussion, the second-harmonic component is limited to 1.5 percent of \hat{I}_L , such that $\hat{I}_{L2} = 0.0442 A$. Using these values, from Eq. 6-17 and 6-18, the parameters in the voltage controller transfer function of Eq. 6-16 are calculated: $k_v = 0.0722$, and $\omega_{cv} = 76.634 \text{ rad/s}$ (12.2 Hz). This transfer function is realized by an op-amp circuit shown in Fig. 6-7 with the following values:

$$\begin{aligned} R_1 &= 100 k\Omega \\ R_2 &= 7.2 k\Omega \\ C_1 &= 1.8 \mu F \end{aligned} \quad (6-21)$$

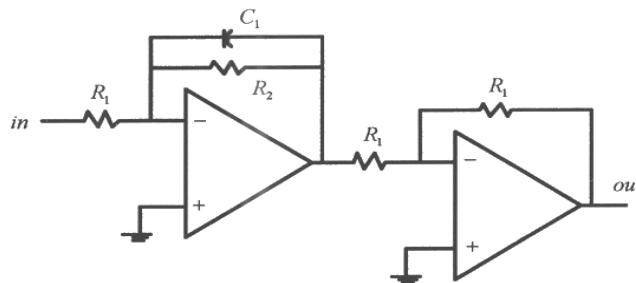


Figure 6-7 Op-amp circuit to implement transfer function $G_v(s)$.

6-7 SIMULATION RESULTS

The PSpice-based simulation of the *PFC* system is shown in Fig. 6-8, where the input voltage and the full-bridge rectifier are combined for simplification purposes. The output load is decreased as a step at 100 ms. The resulting waveforms for the voltage and the inductor current are shown in Fig. 6-9.

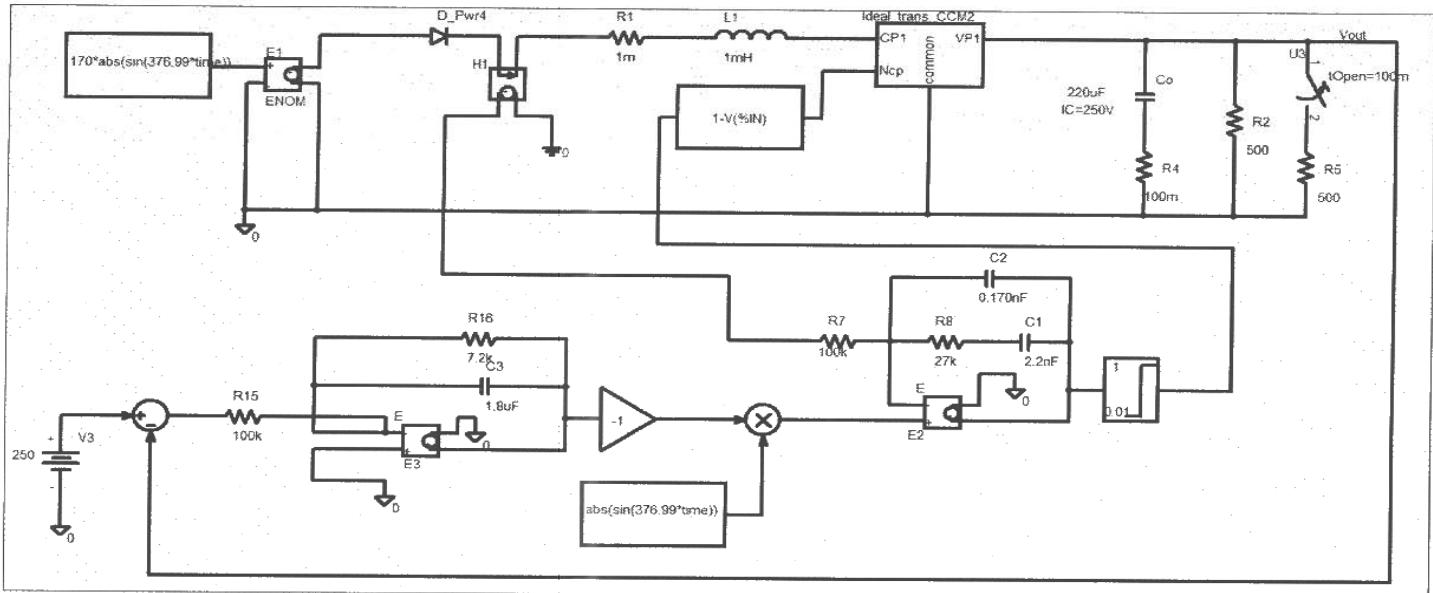


Figure 6-8 PSpice simulation diagram (the load is decreased at 100 ms).

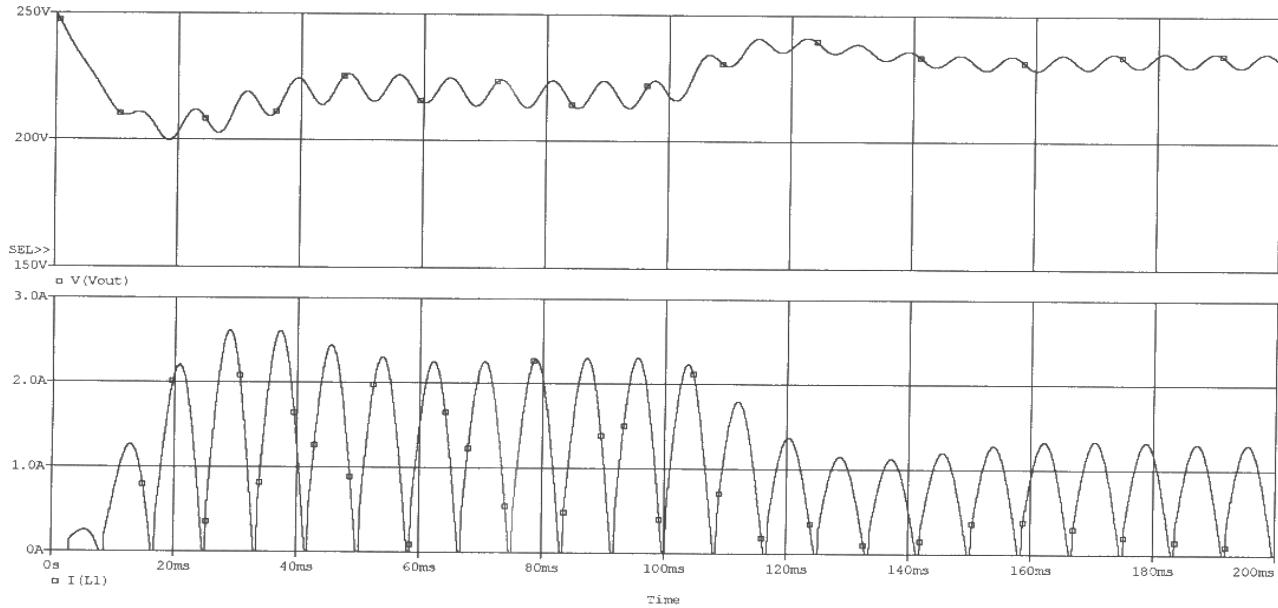


Figure 6-9 Simulation results: output voltage and inductor current.

6-8 FEEDFORWARD OF THE INPUT VOLTAGE

The input voltage is fed forward as shown in Fig. 6-10. In a system with a PFC interface, the output is nearly constant, independent of the changes in the rms value of the input voltage from the utility. Therefore, an increase in the utility voltage \hat{V}_s causes a decrease in \hat{I}_L , and vice versa. To avoid propagating the input voltage disturbance through the PFC feedback loops, the input voltage peak is fed forward, as shown in Fig. 6-10, in determining \hat{I}_L^* .

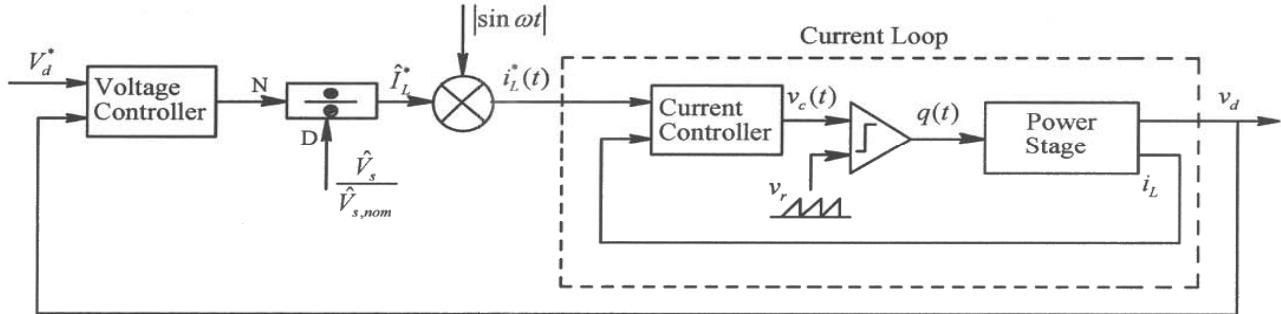


Figure 6-10 Feedforward of the input voltage.

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1. "UC3854 Controlled Power factor Correction Circuit Design," Philip C. Todd, Unitrode Application Note U-134.
2. "High power Factor Switching Pre-Regulator Design Optimization," Lyod Dixon, Unitrode Design Application Manual.
3. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.

PROBLEMS

- 6-1 In a single phase power factor correction circuit, $V_s = 120V(rms)$, $V_d = 225V$, and the output power is $100W$. Calculate and draw the following waveforms, synchronized to v_s waveform: $i_L(t)$, $d(t)$, and the current through the diode.
- 6-2 In the numerical example given in this chapter, calculate the rms input current if the utility voltage is $110V(rms)$, and compare it with its nominal value when $V_s = 120V(rms)$.
- 6-3 In problem 6-1, calculate the second-harmonic peak voltage in the capacitor if $C = 440 \mu F$.
- 6-4 In the numerical example given in this chapter, calculate the maximum peak-peak ripple current in the inductor.
- 6-5 Repeat the design of the current loop in the given numerical example in this chapter, if the loop crossover frequency is $20kHz$.
- 6-6 Repeat the design of the outer voltage loop in the numerical example given in this chapter, if the output capacitance $C = 440 \mu F$.

Chapter 7

MAGNETIC CIRCUIT CONCEPTS

The purpose of this chapter is to review some of the basic concepts associated with magnetic circuits and to develop an understanding of inductors and transformers, which are needed in power electronics.

7-1 AMPERE-TURNS AND FLUX

Let us consider a simple magnetic structure of Fig. 7-1 consisting of an N -turn coil with a current i , on a magnetic core made up of iron. This coil applies Ni ampere-turns to the core. We will assume the magnetic field intensity H_m in the core to be uniform along the mean path length ℓ_m . The magnetic field intensity in the air gap is denoted as H_g . From Ampere's Law, the closed line integral of the magnetic field intensity along the mean path within the core and in the air gap is equal to the applied ampere-turns:

$$H_m \ell_m + H_g \ell_g = Ni \quad (7-1)$$

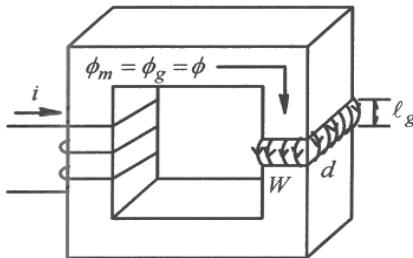


Figure 7-1 Magnetic structure with air gap.

In the core and in the air gap, the flux densities corresponding to H_m and H_g are as follows:

$$B_m = \mu_m H_m \quad (7-2)$$

$$B_g = \mu_o H_g \quad (7-3)$$

In terms of the above flux densities in Eq. 7-1,

$$\frac{B_m}{\mu_m} \ell_m + \frac{B_g}{\mu_o} \ell_g = Ni \quad (7-4)$$

Since flux lines form closed paths, the flux crossing any perpendicular cross-sectional area in the core is the same as that crossing the air gap. Therefore,

$$\phi = A_m B_m = A_g B_g \quad (7-5)$$

$$B_m = \frac{\phi}{A_m} \quad \text{and} \quad B_g = \frac{\phi}{A_g} \quad (7-6)$$

Substituting flux densities from Eq. 7-6 into Eq. 7-4,

$$\phi\left(\frac{\ell_m}{\underbrace{A_m \mu_m}_{\Re_m}} + \frac{\ell_g}{\underbrace{A_g \mu_o}_{\Re_g}}\right) = Ni \quad (7-7)$$

In Eq. 7-7, the two terms within the parenthesis equal the reluctance \mathfrak{R}_m of the core and the reluctance \mathfrak{R}_g of the air gap, respectively. Therefore, the effective reluctance \mathfrak{R} of the whole structure in the path of the flux lines is the sum of the two reluctances:

$$\mathfrak{R} = \mathfrak{R}_m + \mathfrak{R}_g \quad (7-8)$$

Substituting from Eq. 7-8 into Eq. 7-7

$$\phi = \frac{Ni}{\mathfrak{R}} \quad (7-9)$$

Eq. 7-9 allows the flux ϕ to be calculated for the applied ampere-turns, and hence B_m and B_g can be calculated from Eq. 7-6.

7-2 INDUCTANCE L

At any instant of time in the coil of Fig. 7-2a, the flux linkage of the coil λ_m , due to flux lines entirely in the core, is equal to the flux ϕ_m times the number of turns N that are linked. This flux linkage is related to the current i by a parameter defined as the inductance L_m :

$$\lambda_m = N\phi_m = L_m i \quad (7-10)$$

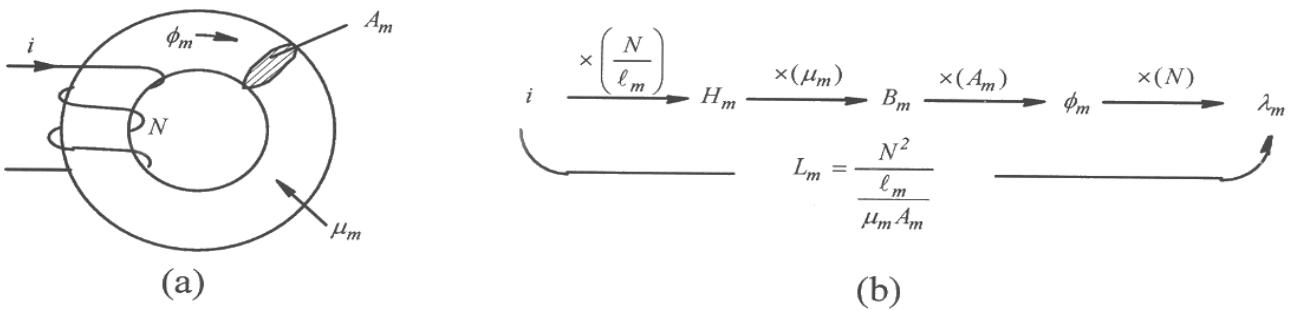


Figure 7-2 Coil Inductance.

where the inductance $L_m (= \lambda_m / i)$ is constant if the core material is in its linear operating region. The coil inductance in the linear magnetic region can be calculated by multiplying all the factors shown in Fig. 7-2b, which are based on earlier equations:

$$L_m = \frac{\lambda_m}{i} = \frac{\left(\frac{Ni}{\ell_m} \right) \mu_m A_m N}{i} = \frac{N^2}{\left(\frac{\ell_m}{\mu_m A_m} \right)} = \frac{N^2}{\mathfrak{R}_m} \quad (7-11)$$

The diagram shows a rectangular magnetic core with a central vertical air gap. The total height of the core is labeled H_m . The width of the core is labeled B_m . The air gap length is labeled ϕ_m .

Eq. 7-11 indicates that the inductance L_m is strictly a property of the magnetic circuit (i.e., the core material, the geometry, and the number of turns), provided the operation is in the linear range of the magnetic material, where the slope of its B - H characteristic can be represented by a constant μ_m .

7-2-1 Energy Storage due to Magnetic Fields

Energy in an inductor is stored in its magnetic field. From the study of electric circuits, we know that at anytime, with a current i , the energy stored in the inductor is

$$W = \frac{1}{2} L_m i^2 [J] \quad (7-12)$$

where [J], for Joules, is a unit of energy. Initially assuming a structure without an air gap, such as in Fig. 7-2a, we can express the energy storage in terms of flux density, by substituting into Eq. 7-12 the inductance from Eq. 7-11, and the current from the Ampere's Law in Eq. 7-1:

$$W_m = \frac{1}{2} \frac{N^2}{\mu_m A_m} \underbrace{\left(\frac{H_m \ell_m}{i} \right)^2}_{i^2} = \frac{1}{2} \frac{(H_m \ell_m)^2}{\mu_m A_m} = \frac{1}{2} \frac{B_m^2}{\mu_m} \underbrace{A_m \ell_m}_{volume} [J] \quad (7-13)$$

where $A_m \ell_m = volume$, and in the linear region $B_m = \mu_m H_m$. Therefore, from Eq. 7-13, the energy density in the core is

$$w_m = \frac{1}{2} \frac{B_m^2}{\mu_m} \quad (7-14)$$

Similarly, the energy density in the air gap depends on μ_o and the flux density in it. Therefore, from Eq. 7-14, the energy density in any medium can be expressed as

$$w = \frac{1}{2} \frac{B^2}{\mu} [J/m^3] \quad (7-15)$$

In inductors, the energy is primarily stored in the air gap purposely introduced in the path of flux lines.

In transformers, there is no air gap in the path of the flux lines. Therefore, the energy stored in the core of an ideal transformer is zero, where the core permeability is assumed infinite, and hence H_m is zero for a finite flux density. In a real transformer, the core permeability is finite, resulting in some energy storage in the core.

7-3 FARADAY'S LAW: INDUCED VOLTAGE IN A COIL DUE TO TIME-RATE OF CHANGE OF FLUX LINKAGE

In our discussion so far, we have established in magnetic circuits relationships between the electrical quantity i and the magnetic quantities H , B , ϕ , and λ . These relationships are valid under dc (static) conditions, as well as at any instant when these quantities are varying with time. We will now examine the voltage across the coil under time-varying conditions. In the coil of Fig. 7-3, Faraday's Law dictates that the time-rate of change of flux-linkage equals the voltage across the coil at any instant:

$$e(t) = \frac{d}{dt} \lambda(t) = N \frac{d}{dt} \phi(t) \quad (7-16)$$

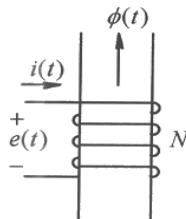


Figure 7-3 Voltage polarity and direction of flux and current.

This assumes that all flux lines link all N -turns such that $\lambda = N\phi$. The polarity of the emf $e(t)$ and the direction of $\phi(t)$ in the above equation are yet to be justified.

The relationship in Eq. 7-16 is valid, no matter what is causing the flux to change. One possibility is that a second coil is placed on the same core. When the second coil is supplied by a time-varying current, mutual coupling causes the flux ϕ through the coil to change with time. The other possibility is that a voltage $e(t)$ is applied across the coil in Fig. 7-3, causing the change in flux, which can be calculated by integrating both sides of Eq. 7-16 with respect to time:

$$\phi(t) = \phi(0) + \frac{1}{N} \int_0^t e(\tau) \cdot d\tau \quad (7-17)$$

where $\phi(0)$ is the initial flux at $t = 0$ and τ is a variable of integration.

Recalling the Ohm's law, $v = Ri$, the current direction through a resistor is into the terminal at the positive polarity. This is the passive sign convention. Similarly, in the coil of Fig. 7-3, we can establish the voltage polarity and the flux direction in order to apply Faraday's law, given by Eqs. 7-16 and 7-17. If the flux direction is given, we can establish the voltage polarity as follows: first determine the direction of a hypothetical current that will produce flux in the same direction as given. Then, the positive polarity for the voltage is at the terminal, which this hypothetical current is entering. Conversely, if the voltage polarity is given, imagine a hypothetical current entering the positive-polarity terminal. This current, based on how the coil is wound, for example in Fig. 7-3, determines the flux direction for use in Eqs. 7-16 and 7-17. Following these rules to determine the voltage polarity and the flux direction is easier than applying Lenz's law (not discussed here).

The voltage is induced due to $d\phi/dt$, regardless of whether any current flows in that coil.

7-4 LEAKAGE AND MAGNETIZING INDUCTANCES

Just as conductors guide currents in electric circuits, magnetic cores guide *flux* in *magnetic circuits*. But there is an important difference. In electric circuits, the conductivity of copper is approximately 10^{20} times higher than that of air, allowing leakage currents to be neglected at dc or at low frequencies such as 60 Hz. In magnetic circuits, however, the permeabilities of magnetic materials are, at best, only 10^4 times greater than that of air. Because of this relatively low ratio, the core window in the structure of Fig. 7-4a has "leakage" flux lines, which do not reach their intended destination that may be another winding, for example in a transformer, or an air gap in an inductor. Note that the coil shown in Fig. 7-4a is drawn schematically. In practice, the coil consists of multiple layers and the core is designed to fit as snugly to the coil as possible, thus minimizing the unused "window" area.

The leakage effect makes accurate analysis of magnetic circuits more difficult that requires sophisticated numerical methods, such as finite element analysis. However, we can account for the effect of leakage fluxes by making certain approximations. We can divide the total flux ϕ into two parts:

1. The magnetic flux ϕ_m , which is completely confined to the core and links all N turns, and
2. The leakage flux, which is partially or entirely in air and is represented by an "equivalent" leakage flux ϕ_ℓ , which also links all N turns of the coil but does not follow the entire magnetic path, as shown in Fig. 7-4b.

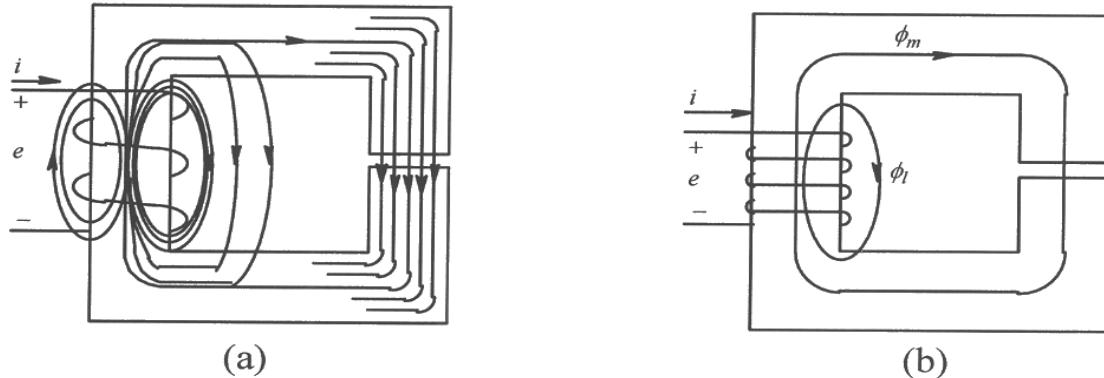


Figure 7-4 (a) Magnetic and leakage fluxes; (b) equivalent representation of magnetic and leakage fluxes.

In Fig. 7-4b, $\phi = \phi_m + \phi_\ell$, where ϕ is the equivalent flux which links all N turns. Therefore, the total flux linkage of the coil is

$$\lambda = N\phi = \underbrace{N\phi_m}_{\lambda_m} + \underbrace{N\phi_\ell}_{\lambda_\ell} = \lambda_m + \lambda_\ell \quad (7-18)$$

The total inductance (called the self-inductance) can be obtained by dividing both sides of Eq. 7-18 by the current i :

$$\frac{\lambda}{i} = \frac{\lambda_m}{i} + \frac{\lambda_\ell}{i} \quad (7-19)$$

$$\therefore L_{self} = L_m + L_\ell \quad (7-20)$$

where L_m is often called the *magnetizing inductance* due to ϕ_m in the magnetic core, and L_ℓ is called the *leakage inductance* due to the leakage flux ϕ_ℓ . From Eqs. 7-19 and 7-20, the total flux linkage of the coil in Eq. 7-18 can be written as

$$\lambda = (L_m + L_\ell)i \quad (7-21)$$

Hence, from Faraday's law in Eq. 7-16,

$$e(t) = \underbrace{L_m \frac{di}{dt}}_{e_m(t)} + L_\ell \frac{di}{dt} \quad (7-22)$$

This results in the electrical circuit of Fig. 7-5a. In Fig. 7-5b, the voltage drop due to the leakage inductance can be shown separately so that the voltage induced in the coil is solely due to the magnetizing flux. The coil resistance R can then be added in series to complete the representation of the coil.

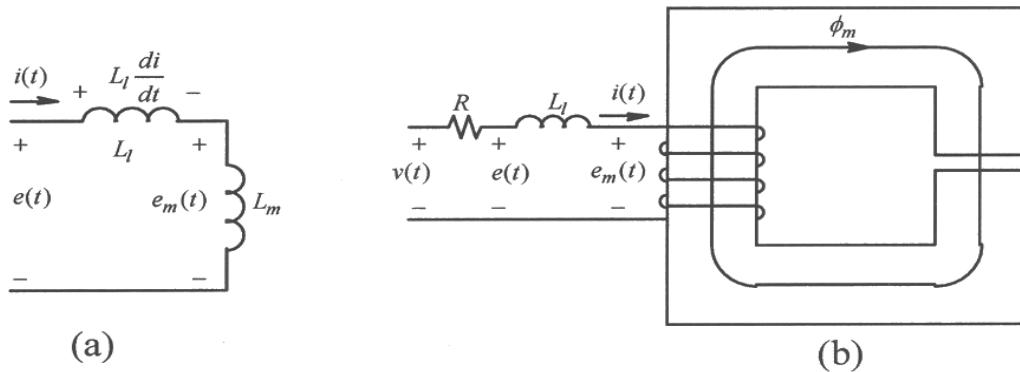


Figure 7-5 (a) Circuit representation;
(b) leakage inductance separated from the core.

7-4-1 Mutual Inductances

Most magnetic circuits, such as those encountered in inductors and transformers consist of multiple coils. In such circuits, the flux established by the current in one coil partially links the other coil or coils. This phenomenon can be described mathematically by means of mutual inductances, as examined in circuit theory courses. However, we will use simpler and more intuitive means to analyze mutually coupled coils, as in a Flyback converter discussed in Chapter 8 dealing with transformer-isolated dc-dc converters.

7-5 TRANSFORMERS

In power electronics, high-frequency transformers are essential to switch-mode dc power supplies. Such transformers often consist of two or more tightly coupled windings where almost all of the flux produced by one winding links the other windings. Including the leakage flux in detail makes the analysis very complicated and not very useful for our purposes here. Therefore, we will include only the magnetizing flux ϕ_m that links all the windings, ignoring the leakage flux whose consequences will be acknowledged separately.

To understand the operating principles of transformers, we will consider a three-winding transformer shown in Fig. 7-6 such that this analysis can be extended to any number of windings. In this transformer, all windings are linked by the same flux ϕ_m . Therefore, from the Faraday's law, the induced voltages at the dotted terminals with respect to their undotted terminals are as follows:

$$e_1 = N_1 \frac{d\phi_m}{dt} \quad (7-23)$$

$$e_2 = N_2 \frac{d\phi_m}{dt} \quad (7-24)$$

$$e_3 = N_3 \frac{d\phi_m}{dt} \quad (7-25)$$

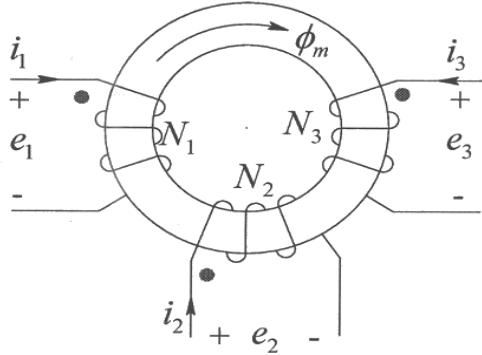


Figure 7-6 Transformer with three windings.

The above equations based on Faraday's law result in the following relationship that shows that the volts-per-turn induced in each winding are the same due to the same rate of change of flux that links them

$$\frac{d\phi_m}{dt} = \frac{e_1}{N_1} = \frac{e_2}{N_2} = \frac{e_3}{N_3} \quad (7-26)$$

In accordance to the Ampere's law given in Eq. 7-9, the flux ϕ_m at any instant of time is supported by the net ampere-turns applied to the core in Fig. 7-6,

$$\phi_m = \frac{N_1 i_1 + N_2 i_2 + N_3 i_3}{R_m} \quad (7-27)$$

In Eq. 7-27, the core of Fig. 7-6 offers reluctance R_m in the flux path and the currents are defined positive into the dotted terminals of each winding such as to produce flux lines in the same direction. Eqs. 7-26 and 7-27 are the key to understanding transformers: at any instant of time, applied voltage (equal to the induced voltage if the winding resistance and the leakage flux are ignored) to one of the windings dictates the flux rate-of-change and hence the induced voltage-per-turn in other windings. The instantaneous flux ϕ_m is obtained by expressing Eq. 7-26 in its integral form below (with proper integral limits)

$$\phi_m = \frac{1}{N_1} \int e_1 dt = \frac{1}{N_2} \int e_2 dt = \frac{1}{N_3} \int e_3 dt \quad (7-28)$$

that requires corresponding net ampere-turns given by Eq. 7-27 to sustain this flux, overcoming the core reluctance. It is important to note that it is immaterial to the core the apportionment of these winding currents.

The analysis above is based on neglecting the leakage flux, assuming that the flux produced by a winding links all the other windings. In a simplified analysis, the leakage flux of a winding can be assumed to result in a leakage inductance, which can be added, along with the winding resistance, in series with the induced voltage $e(t)$ in the winding in the electrical circuit representation.

REFERENCE

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.

PROBLEMS

Inductors

A magnetic core has the following properties: the core area $A_m = 0.931 \text{ cm}^2$, the magnetic path length of $\ell_m = 3.76 \text{ cm}$, and the relative permeability of the material is $\mu_r = \mu_m / \mu_o = 5000$.

- 7-1 Calculate the reluctance \mathfrak{R} of this core.
- 7-2 Calculate the reluctance of an air gap of length $\ell_g = 1 \text{ mm}$, if it is introduced in the core of Problem 7-1.
- 7-3 A coil with $N = 30$ turns is wound on a core with an air gap described in Problem 7-2. Calculate the inductance of this coil.
- 7-4 If the flux density in the core in Problem 7-3 is not to exceed 0.2 T , what is the maximum current that can be allowed to flow through this inductor coil?
- 7-5 At the maximum current calculated in Problem 7-4, calculate the energy stored in the magnetic core and the air gap, and compare the two.

Transformers

A three-winding transformer with $N_1 = 10$ turns, $N_2 = 5$ turns, and $N_3 = 5$ turns uses a magnetic core that has the following properties: $A_m = 0.639 \text{ cm}^2$, the magnetic path length of $\ell_m = 3.12 \text{ cm}$, and the relative permeability of the material $\mu_r = \mu_m / \mu_o = 5000$. A square-wave voltage, of 30-V amplitude and a frequency of 100 kHz, is applied to winding 1. Windings 2 and 3 are open. Ignore the leakage inductances.

- 7-6 Calculate and draw the magnetizing current waveform, along with the applied voltage waveform, and the waveforms of the voltages induced in the open windings 2 and 3.
- 7-7 Calculate the self-inductances of each winding in Problem 7-6.
- 7-8 Calculate the peak flux density in Problem 7-6.
- 7-9 A load resistance of 10Ω is connected to winding 2. Calculate and draw the currents in windings 1 and 2, along with the applied voltage waveform.
- 7-10 Assuming that winding 1 is not applied a voltage, what is the peak amplitude of the square-wave voltage at 100 kHz that can be applied to winding 3 of this transformer, if the peak flux density calculated in Problem 7-8 is not to be exceeded?
- 7-11 In Problem 7-6, what is the peak amplitude of the voltage that can be applied to winding 1 without exceeding the peak flux density calculated in Problem 7-8, if the frequency of the square wave voltage is 200kHz ? What is the peak value of the magnetizing current, as compared to the one at 100 kHz ?

Chapter 8

SWITCH-MODE DC POWER SUPPLIES

8-1 APPLICATIONS OF SWITCH-MODE DC POWER SUPPLIES

Switch-mode dc power supplies represent an important power electronics application area with the worldwide market in excess of several billion dollars per year. Many of these power supplies incorporate transformer isolation for reasons that are discussed below. Within these power supplies, transformer-isolated dc-dc converters are derived from non-isolated dc-dc converter topologies already discussed in chapter 3. For short, we will refer to transformer-isolated switch-mode dc power supplies as SMPS, whose block diagram is shown in Fig. 8-1. As shown in Fig. 8-1, these supplies encompass the rectification of the utility supply and the voltage V_{in} across a large filter capacitor is the input to the transformer-isolated dc-dc converter, which is the focus of discussion in this chapter. Internally, the transformer operates at very high frequencies, upwards of a few hundred kHz are typical, thus resulting in small size and weight, as discussed in the next chapter.

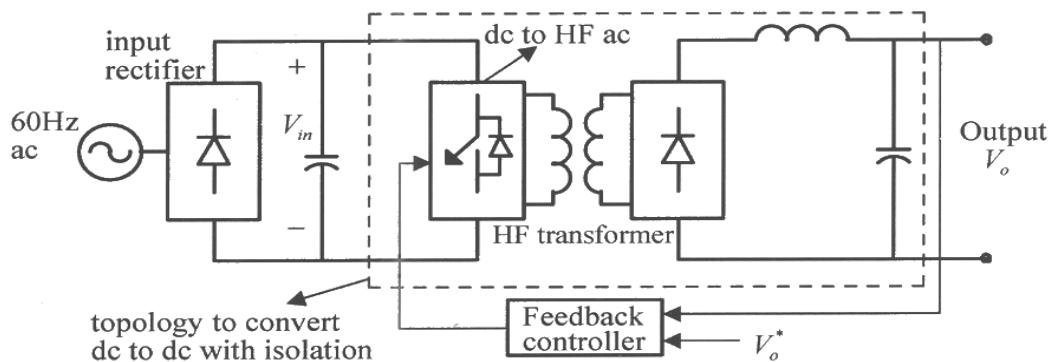


Figure 8-1 Block diagram of switch-mode dc power supplies.

8-2 NEED FOR ELECTRICAL ISOLATION

Electrical isolation by means of transformers is needed in switch-mode dc power supplies for three reasons:

1. Safety. It is necessary for the low-voltage dc output to be isolated from the utility supply to avoid the shock hazard.
2. Different Reference Potentials. The dc supply may have to operate at a different potential, for example, the dc supply to the gate drive for the upper MOSFET in the power-pole is referenced to its Source.

3. Voltage matching. If the dc-dc conversion is large, then to avoid requiring large voltage and current ratings of semiconductor devices, it may be economical and operationally more suitable to use an electrical transformer for conversion of voltage levels.

8-3 CLASSIFICATION OF TRANSFORMER-ISOLATED DC-DC CONVERTERS

In the block diagram of Fig. 8-1, there are following three categories of transformer-isolated dc-dc converters, all of which are discussed in detail in this chapter:

- Flyback converters derived from Buck-Boost dc-dc converters
- Forward converter derived from Buck dc-dc converters
- Full-Bridge and Half-Bridge converters derived from Buck dc-dc converters

8-4 FLYBACK CONVERTERS

Flyback converters are very commonly used in applications at low power levels below 50 W. These are derived from the Buck-Boost converter redrawn in Fig 8-2a, where the inductor is drawn descriptively on a low permeability core.

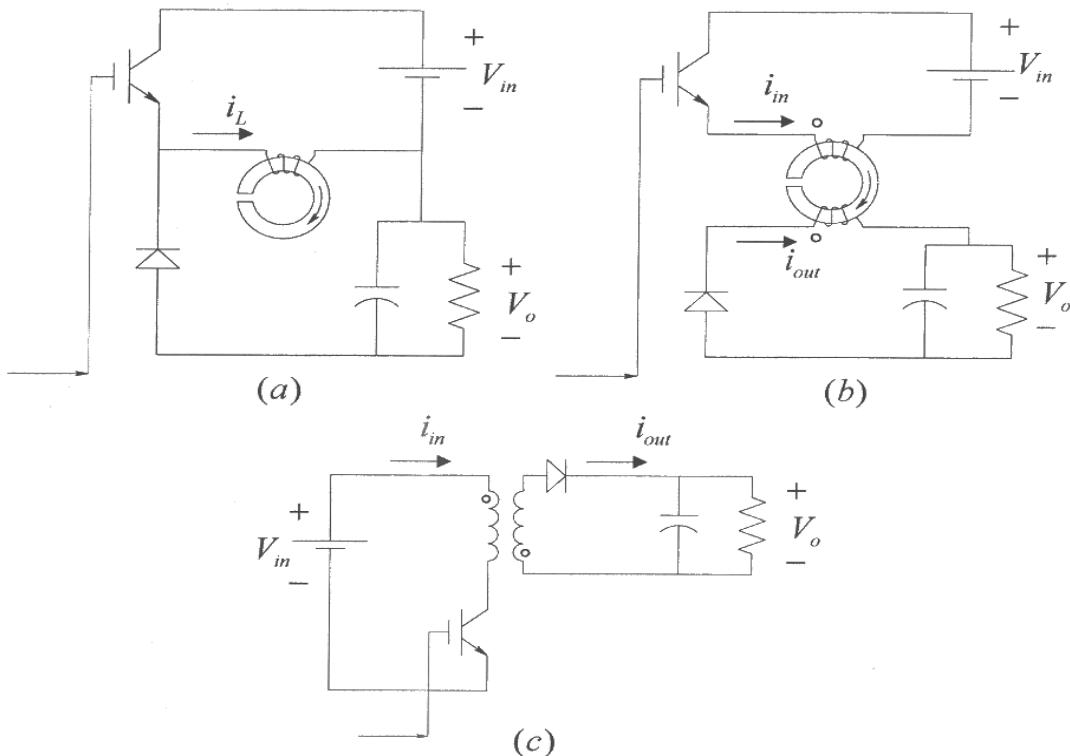


Figure 8-2 Buck-Boost and the Flyback converters.

The Flyback converter in Fig. 8-2b consists of two mutually-coupled coils, where the coil orientations are such that at the instant when the transistor is turned-off, the current switches to the second coil to maintain the same flux in the core. Therefore, the dots on

coils are as shown in Fig. 8-2b where the current into the dot of either coil produces core flux in the same direction. Commonly, the circuit of Fig. 8-2b is redrawn as in Fig. 8-2c.

We will consider the steady state in the incomplete demagnetization mode where the energy is never completely depleted from the magnetic core. This corresponds to the continuous conduction mode (CCM) in Buck-Boost converters. We will assume ideal devices and components, the output voltage $v_o(t) = V_o$, and the leakage inductances to be zero.

Turning on the transistor at $t = 0$ in the circuit in Fig. 8-2c applies the input voltage V_{in} across coil 1, and the core magnetizing flux ϕ_m increases linearly from its initial value $\phi_m(0)$, as shown in the waveforms of Fig. 8-3. During the transistor on-interval DT_s , the increase in flux can be calculated from the Faraday's law as

$$\Delta\phi_{p-p} = \frac{V_{in}}{N_1} DT_s \quad (8-1)$$

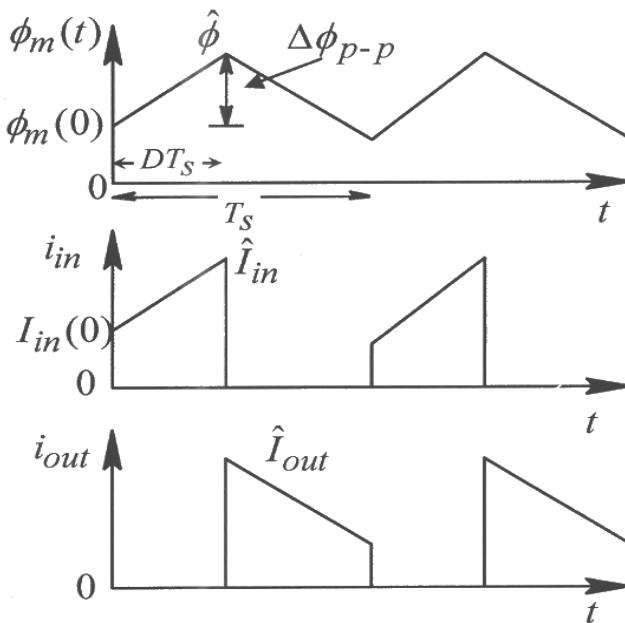


Figure 8-3 Flyback converter waveforms.

Due to increasing ϕ_m , the induced voltage $(N_2/N_1)V_{in}$ across coil 2 adds to the output voltage V_o to reverse bias the diode, resulting in $i_{out} = 0$. Corresponding to the core flux, the current i_{in} can be calculated using the relationship $\phi = Ni/\mathfrak{R}$, where \mathfrak{R} is the core reluctance in the flux path. Therefore, using Eq. 8-1, the increase in the input current during the on-interval, from its initial value $I_{in}(0)$ can be calculated using Eq. 8-1 as

$$\Delta i_{in} = \frac{\Re}{N_1^2} V_{in} DT_s \quad (8-2)$$

During the on-interval DT_s , the output load is entirely supplied by the energy stored in the output capacitor, and the core magnetizing flux and the input current reach their peak values at the end of this interval:

$$\hat{\phi}_m = \phi_m(0) + \frac{V_{in}}{N_1} DT_s \quad (8-3)$$

$$\hat{I}_{in} = I_{in}(0) + \frac{\Re}{N_1^2} V_{in} DT_s \quad (8-4)$$

After the on-interval, turning off the transistor forces the input current in Fig. 8-2c to zero. The magnetic energy stored in the magnetic core due to the flux ϕ_m cannot change instantaneously, and hence the ampere-turns applied to the core must be the same at the instant immediately before and after turning the transistor off. Therefore, the current i_{out} in coil 2 through the diode suddenly jumps to its peak value such that

$$N_2 \hat{I}_{out} \Big|_{i_{in}=0} = N_1 \hat{I}_{in} \Big|_{i_{out}=0} \quad (8-5)$$

$$\therefore \hat{I}_{out} = \frac{N_1}{N_2} \hat{I}_{in} \quad (8-6)$$

With the diode conducting, the output voltage V_o appears across coil 2 with a negative polarity. Hence, during the off-interval $(1-D)T_s$, the core flux declines linearly, as plotted in Fig. 8-3, by $\Delta\phi_{p-p}$, where

$$\Delta\phi_{p-p} = \frac{V_o}{N_2} (1-D) T_s \quad (8-7)$$

Using Eqs. 8-1 and 8-7,

$$\frac{V_o}{V_{in}} = \left(\frac{N_2}{N_1} \right) \frac{D}{1-D} \quad (8-8)$$

The change in the current $i_{out}(t)$ can be calculated in a manner similar to Eq. 8-2, and this current is plotted in Fig. 8-3.

Eq. 8-8 shows that in a Flyback converter, the dependence of the voltage-ratio on the duty-ratio D is identical to that in the Buck-Boost converter, and it also depends on the

coils turns-ratio N_2/N_1 . Flyback converters require minimum number of components by integrating the inductor (needed for a Buck-Boost operation) with the transformer that provides electrical isolation and matching of the voltage levels. These converters are very commonly used in low power applications in the complete demagnetization mode (corresponding to the discontinuous-conduction mode in Buck-Boost), which makes their control easier. A disadvantage of the Flyback converter is the need for snubbers to prevent voltage spikes across the transistor and diode due to leakage inductances associated with the two coils.

8-5 FORWARD CONVERTERS

Forward converter and its variations derived from a Buck converter are commonly used in applications at low power levels up to a kW. A Buck converter is shown in Fig. 8-4a. In this circuit, a three-winding transformer is added as shown in Fig. 8-4b to realize a Forward converter. The third winding in series with a diode D_3 , and the diode D_1 are needed to demagnetize the core every switching cycle. The winding orientations in Fig. 8-4b are such that the current into the dot of any of the windings will produce core flux in the same direction. We will consider steady state converter operation in the continuous conduction mode where the output inductor current i_L flows continuously. In the following analysis, we will assume ideal semiconductor devices, $v_o(t) = V_o$, and the leakage inductances to be zero.

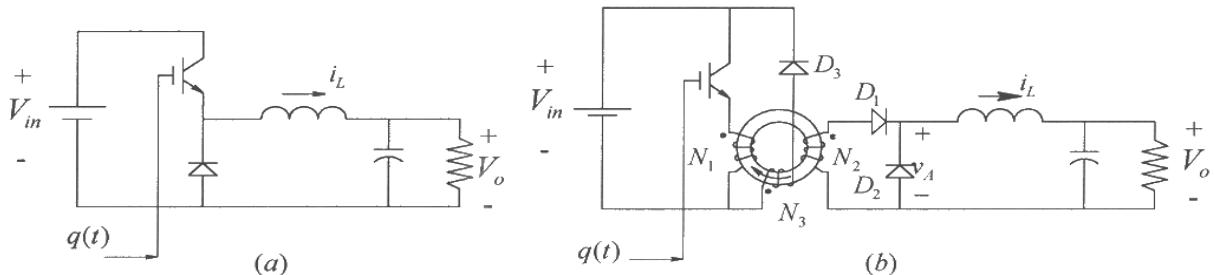


Figure 8-4 Buck and Forward converters.

Initially, assuming an ideal transformer in the Forward converter of Fig. 8-4b, the third winding and the diode D_3 can be removed and D_1 can be replaced by a short circuit. In such an ideal case, the Forward converter operation is identical to that of the Buck converter, as shown by the waveform in Fig. 8-5, except for the presence of the transformer turns-ratio N_2/N_1 . Therefore, in the continuous conduction mode,

$$V_o = \left(\frac{N_2}{N_1} \right) DV_{in} \quad (8-9)$$

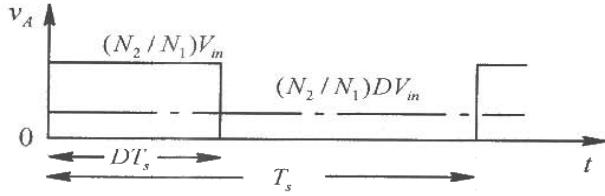


Figure 8-5 Forward converter operation.

In the case with a real transformer, the core must be completely demagnetized during the off-interval of the transistor, and hence the need for the third winding and the diodes D_1 and D_3 , as shown in Fig. 8-4b. Turning on the transistor causes the magnetizing flux in the core to build up as shown in Fig. 8-6. During this on-interval DT_s , D_3 gets reverse biased, thus preventing the current from flowing through the tertiary winding. The diode D_2 also gets reversed biased and the output inductor current flows through D_1 .

When the transistor is turned off, the magnetic energy stored in the transformer core forces a current to flow into the dotted terminal of the tertiary winding, since the current into the dotted terminal of the secondary winding cannot flow due to D_1 , which results in V_{in} to be applied negatively across the tertiary winding, and the core flux to decline, as shown in Fig. 8-6. (The output inductor current freewheels through D_2 .) After an interval T_{demag} , the core flux comes to zero and stays zero during the remaining interval, until the next cycle begins.

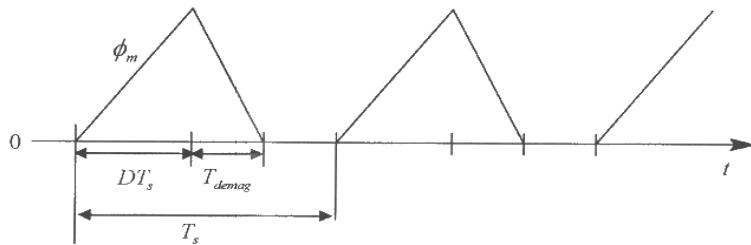


Fig. 8-6 Forward converter core flux.

To avoid the core from saturating, T_{demag} must be less than the off-interval $(1-D)T_s$ of the transistor. Typically, windings 1 and 3 are wound bifilar to provide a very tight mutual coupling between the two, and hence, $N_3 = N_1$. Therefore, to the core is applied an equal magnitude but opposite polarity per-turn voltage during DT_s and T_{demag} , respectively. At the upper limit, T_{demag} equals $(1-D)T_s$, and equating it to the on-interval DT_s of the transistor yields the upper limit on the duty-ratio, D_{max} , to be 0.5, with $N_1 = N_3$.

8-5-1 Two-Switch Forward Converters

Single-switch Forward converters are used in power ratings up to a few hundred watts. However, Two-Switch Forward converters discussed below eliminate the need for a separate demagnetizing winding and are used in much higher power ratings of a kW and even higher.

Fig. 8-7 shows the topology of the Two-Switch Forward converter, where both transistors are gated on and off simultaneously with a duty-ratio $D \leq 0.5$. During the on-interval DT_s , when both transistors are on, diodes D_1 and D_2 get reverse biased and the output inductor current i_L flows through D_o , similar to that in a single-switch Forward converter. During the off interval when both transistors are turned off, the magnetizing current in the transformer core flows through the two primary-side diodes into V_{in} , thus applying $-V_{in}$ negatively to the core and causing it to demagnetize. Application of $-V_{in}$ to the primary winding causes D_o to get reversed biased and the output inductor current i_L freewheels through D_F .

Based on the discussion regarding the demagnetization of the core in a single-switch Forward converter, the switch duty-ratio D is limited to 0.5. The voltage conversion ratio remains the same as in Eq. 8-9.

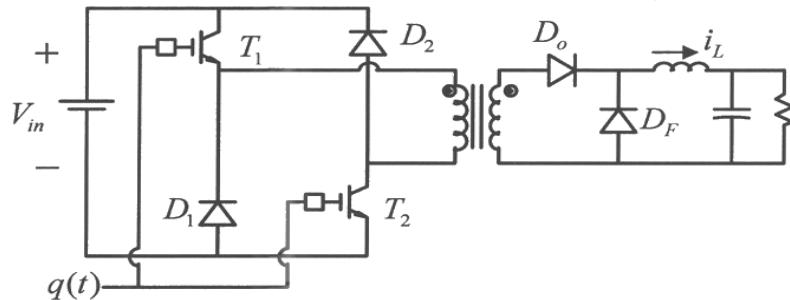


Figure 8-7 Two-switch Forward converter.

8-6 FULL-BRIDGE CONVERTERS

Full-Bridge converters consist of four transistors, hence are economically feasible only at higher power levels in applications at a few hundred watts and higher. Like Forward converters, full-bridge converters are also derived from Buck converters. Unlike Flyback and Forward converters that operate in only one quadrant of the B-H loop, Full-Bridge converters use the magnetic core in two quadrants.

A Full-Bridge converter consists of two switching power-poles, as shown in Fig. 8-8, with a center-tapped transformer secondary winding. In analyzing this converter, we will assume the transformer ideal, although the effects of magnetizing current can be easily

accounted for. We will consider steady state converter operation in the continuous conduction mode where the output inductor current i_L flows continuously. As with previous converters, we will assume ideal devices and components, and $v_o(t) = V_o$.

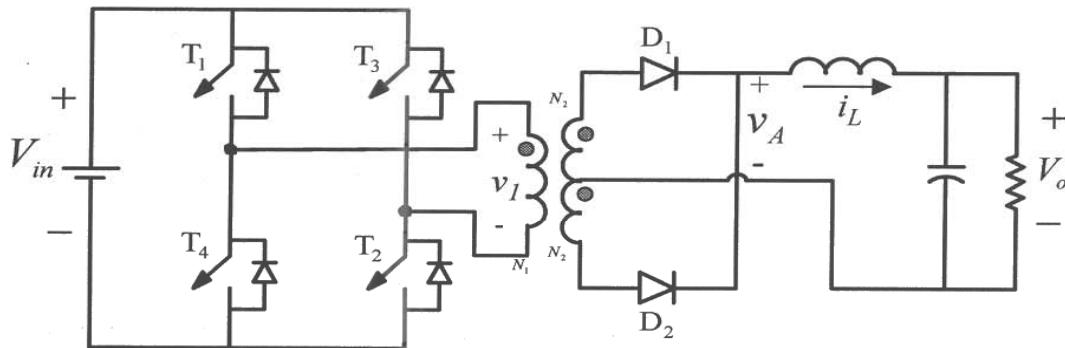


Figure 8-8 Full-Bridge converter.

In the Full-Bridge converter of Fig. 8-8, the voltage v_1 applied to the primary winding alternates without a dc component. The waveform of this voltage is shown in Fig. 8-9, where $v_1 = V_{in}$ when transistors T_1 and T_2 are on during DT_s , and $v_1 = -V_{in}$ when T_3 and T_4 are on for an interval of the same duration. This waveform applies equal positive and negative volt-second areas to the transformer primary. The switch duty-ratio D (< 0.5) is controlled to achieve the output voltage regulation by means of zero intervals between the positive and the negative applied voltages.

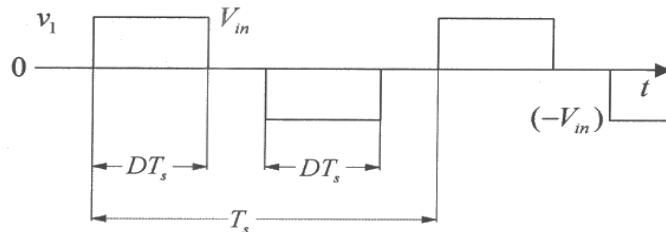


Figure 8-9 Full-Bridge converter waveforms.

The way the voltage across the primary winding, hence the secondary winding, is forced to be zero classifies Full-Bridge converters into the following two categories:

- Pulse-Width Modulated (PWM), and
- Phase-Shift Modulated (PSM)

PWM Control. In PWM control, all four transistors are turned off, resulting in a zero voltage across the transformer windings, as discussed shortly. With all transistors off, the output inductor current freewheels through the two secondary windings, and there are no

conduction losses on the primary side of the transformer. Therefore, the PWM control results in lower conduction losses, and it is the control method discussed in this chapter.

PSM Control. In phase-shift modulated control, the two transistors of each power-pole are operated at nearly 50% duty-ratio, with $D \approx 0.5$. The output of each power-pole pulsates between V_{in} and 0 with a duty-ratio of nearly 50%. The length of the zero intervals is controlled by phase-shifting the two power-pole outputs with respect to each other, as the name of this control implies. During zero intervals, either both transistors at the top, or both transistors at the bottom are on, creating a short circuit (through one of the anti-parallel diodes, depending on the direction of the current) across the primary winding, resulting in $v_1 = 0$. During this short-circuited condition, the output inductor current is reflected to the primary winding and circulates through the primary-side semiconductor devices, causing additional conduction losses. However, increased conduction losses can be offset by the reduction in switching losses by this means of control, as we will discuss in detail in Chapter 10 on soft-switching.

8-6-1 PWM Control

As shown by the block diagram of Fig. 8-10a, the PWM-IC for Full-Bridge converters provides gate signals to the transistor pairs (T_1, T_2 and T_3, T_4) during alternate cycles of the ramp voltage in Fig. 8-10b.

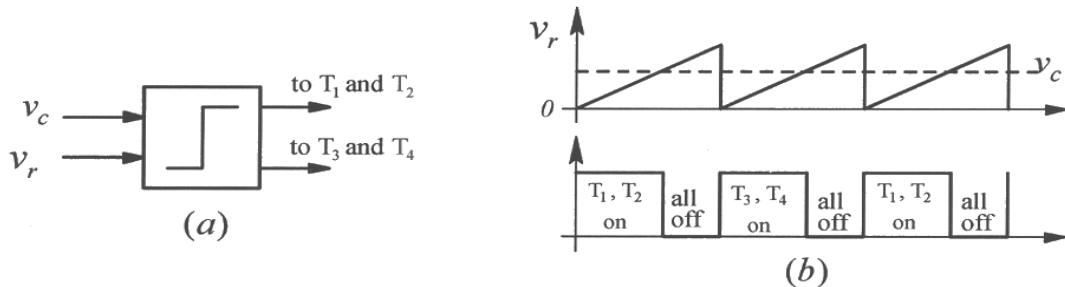


Figure 8-10 PWM-IC and control signals for transistors.

Corresponding to these PWM switching signals, the resulting sub-circuits are shown in Fig. 8-11 for one-half switching cycle, where the other half-cycle is symmetric.

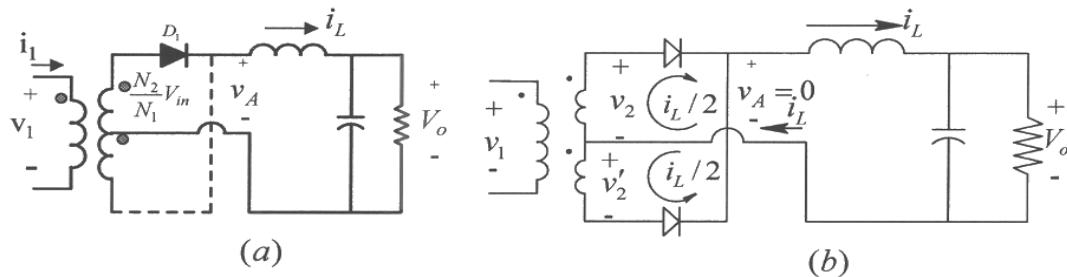


Figure 8-11 Full-Bridge: sub-circuits.

Interval DT_s with transistors T_1, T_2 in their on state. Turning on T_1, T_2 applies positive voltage V_{in} to the primary winding, causing D_2 to become reverse biased and i_L is carried through D_1 , as shown in Fig. 8-11a. During this interval, $v_A = (N_2 / N_1)V_{in}$ as plotted in Fig. 8-12.

Interval $(1/2 - D)T_s$ with all Transistors off. When all the transistors are turned off, there is no current in the primary winding, and the output inductor current divides equally (assuming an ideal transformer) between the two output diodes as shown in the sub-circuit of Fig. 8-11b. This ensures that the total ampere-turns acting on the transformer core equal zero because of $i_L/2$ coming out of the dotted terminal and $i_L/2$ going into the dotted terminal. Applying the Kirchhoff's voltage law in the loop consisting of the two secondaries in Fig. 8-11b shows that $v_2 + v'_2 = 0$. Since $v_2 = v'_2$, the two voltages must be individually zero, and hence also the primary voltage v_1 :

$$v_1 = v_2 = v'_2 = 0 \quad (8-10)$$

During this interval, $v_A = 0$ as plotted in Fig. 8-12.

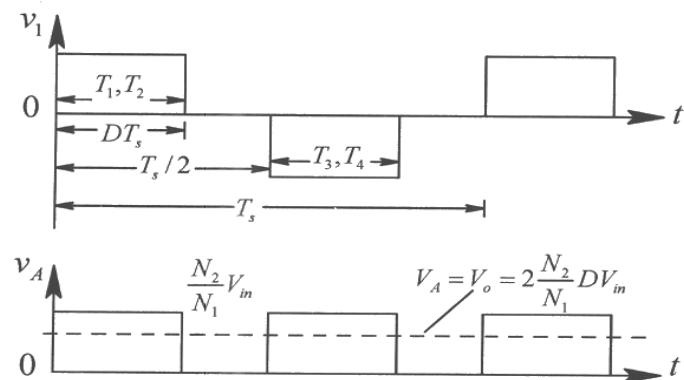


Figure 8-12 Full-Bridge converter waveforms.

The above discussion completes the discussion of one-half switching cycle. The other half-cycle with T_3, T_4 on applies a negative voltage ($-V_{in}$) across the primary winding for an interval DT_s and results in D_2 conducting and D_1 reverse biased. During this interval, $v_A = (N_2 / N_1)V_{in}$ as before when the positive voltage was applied to the primary winding. The waveforms during this half-cycle are as plotted in Fig. 8-12.

From Fig. 8-12, recognizing that $V_A = V_o$ in the dc steady state,

$$\frac{V_o}{V_{in}} = 2 \left(\frac{N_2}{N_1} \right) D \quad (8-11)$$

8-7 Half-Bridge and Push-Pull Converters

Variations of Full-Bridge converters are shown in Fig. 8-13. The Half-Bridge converter in Fig. 8-13a consists of only two transistors but requires two split capacitors to form a dc input mid-point. It is sometimes used at slightly lower power levels compared to the Full-Bridge converter. The Push-Pull converter in Fig. 8-13b has the advantage of having both transistors gates referenced to the low-side of the input voltage. The penalty is in the transformer where during the power transfer interval, only one half of the primary winding and one half of the secondary winding are utilized.

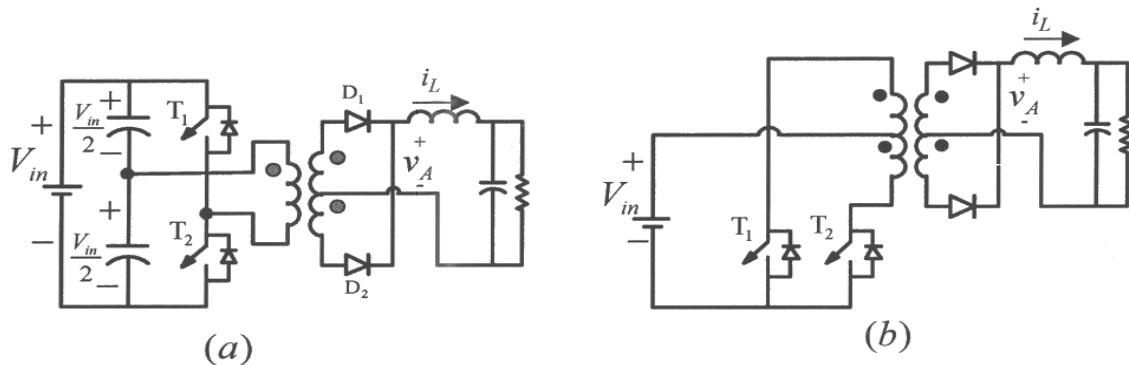


Figure 8-13 Half-Bridge and Push-Pull converters.

8-8 PRACTICAL CONSIDERATIONS

To provide electrical isolation between the input and the output, the feedback control loop should also have electrical isolation. There are several ways of providing this isolation as discussed in Reference [1].

REFERENCE

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.

PROBLEMS

Flyback Converters:

In a Flyback converter, $V_{in} = 30V$, $N_1 = 30$ turns, and $N_2 = 15$ turns. The self-inductance of winding 1 is $50\mu H$, and $f_s = 200kHz$. The output voltage is regulated at $V_o = 9V$.

- 8-1 Calculate and draw the waveforms shown in Fig 8-3 along with the ripple current in the output capacitor, if the load is $27W$.
- 8-2 For the same duty-ratio as in Problem 8-1, calculate the critical power which makes this converter operate at the border of incomplete and complete demagnetization modes.

- 8-3 Draw the waveforms, similar to those in Problem 8-1, in Problem 8-2.
- 8-4 If a Flyback converter is operating in a complete de-magnetization mode, derive the voltage transfer ratio in terms of the load resistance R , the switching frequency f_s , the self-inductance L_1 of winding 1, and the duty-ratio D .

Forward converter:

In a Forward converter, $V_{in} = 30V$, $N_1 = 10$ turns, $N_2 = 5$ turns, and $N_3 = 10$ turns. The self-inductance of winding 1 is $150 \mu H$, and the switching frequency $f_s = 200 kHz$. The output voltage is regulated such that $V_o = 5V$. The output filter inductance is $50 \mu H$, and the output load is $25W$.

- 8-5 Calculate and draw the waveforms for v_A , i_L , i_m , and i_{D_3} in Fig. 8-4b.
- 8-6 If the maximum duty ratio needs to be increased to 0.7, calculate N_1 / N_3 ?
- 8-7 Why is diode D_1 necessary in Fig 8-4b?

Two-Switch Forward Converters

In a two-switch Forward converter, $V_{in} = 30V$, $N_1 / N_2 = 2$, and the switching frequency $f_s = 200 kHz$. The output voltage is regulated such that $V_o = 5V$. The self-inductance of winding 1 is $150 \mu H$, and the output filter inductance is $50 \mu H$.

- 8-8 Calculate and draw waveforms if the output load is $200W$.
- 8-9 Why is the duty-ratio in this converter limited to 0.5?

Full-Bridge Converters

- 8-10 In a Full-bridge converter shown in Fig. 8-8, consider the output current through the filter inductor to be ripple-free dc. $V_{in} = 30V$, $f_s = 200 kHz$, and $N_1 / N_2 = 4$. The output voltage is regulated such that $V_o = 5V$. Calculate the PWM waveforms in this converter. Assume the transformer ideal.

Chapter 9

Design of High-Frequency Inductors and Transformers

9-1 INTRODUCTION

As discussed Chapter 8, inductors and transformers are needed in switch-mode dc power supplies, where switching frequencies are in excess of 100 kHz. High-frequency inductors and transformers are generally not available off-the-shelf, and must be designed based on the application specifications. A detailed design discussion is presented in Reference [1]. In this chapter, a simple and a commonly used approach called the Area-Product method is presented, where the thermal considerations are ignored. This implies that the magnetic component built on the design basis presented here should be evaluated for its temperature rise and efficiency, and the core and the conductor sizes should be adjusted accordingly.

9-2 BASICS OF MAGNETIC DESIGN

In designing high frequency inductors and transformers, a designer is faced with countless choices. These include choice of core materials, core shapes (some offer better thermal conduction whereas others offer better shielding to stray flux), cooling methods (natural convection versus forced cooling), and losses (lower losses offer higher efficiency at the expense of higher size and weight) to name a few. However, all magnetic design-optimization programs calculate two basic quantities from given electrical specifications:

- The peak flux density B_{\max} in the magnetic core to limit core losses, and
- The peak current density J_{\max} in the winding conductors to limit conduction losses

The design procedure presented in this chapter assumes values for these two quantities based on the intended applications of inductors and transformers. However, they may be far from optimum in certain situations.

9-3 INDUCTOR AND TRANSFORMER CONSTRUCTION

Figs. 9-1a and b represent the cross-section of an inductor and a transformer wound on toroidal cores. In Fig. 9-1a for an inductor, the same current i passes through all N turns of a winding. In the transformer of Fig. 9-1b, there are two windings where the

current i_1 in winding 1, with N_1 bigger cross-section conductors, is in opposite direction to that of i_2 in winding 2 with N_2 smaller cross-section conductors. In each winding, the conductor cross-section is chosen such that the peak current density J_{\max} is not exceeded at the maximum specified current in that winding. The core area A_{core} in Figs. 9-1a and b allows the flow of flux lines without exceeding the maximum flux density B_{\max} in the core.

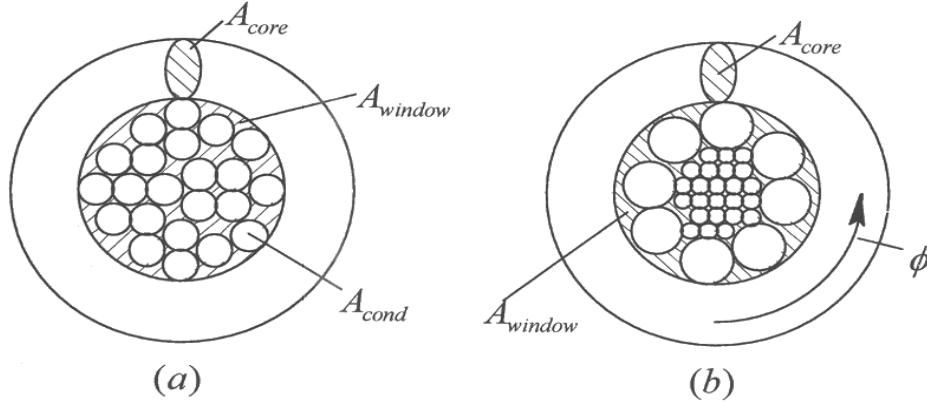


Figure 9-1 Cross-sections.

9-4 AREA-PRODUCT METHOD

The area-product method, based on pre-selected values of the peak flux density B_{\max} in the core and the peak current density J_{\max} in the conductors, allows an appropriate core size to be chosen, as described below.

9-4-1 Core Window Area A_{window}

The windows of the toroidal cores in Figs. 9-1a and b accommodate the winding conductors, where the conductor cross-sectional area A_{cond} depends on the maximum rms current for which the winding is designed. In the expression for the window area below, the window fill-factor k_w in a range from 0.3 to 0.6 accounts for the fact that the entire area of the window cannot be filled, and the subscript y designates a winding, where in general there may be more than one, like in a transformer

$$A_{window} = \frac{1}{k_w} \sum_y (N_y A_{cond,y}) \quad (9-1)$$

In Eq. 9-1, the conductor cross-sectional area in winding y depends on its maximum rms current and the maximum allowed current density J_{\max} that is generally chosen to be the same for all windings:

$$A_{cond,y} = \frac{I_{rms,y}}{J_{max}} \quad (9-2)$$

Substituting Eq. 9-2 into Eq. 9-1,

$$A_{window} = \frac{\sum_y (N_y I_{rms,y})}{k_w J_{max}} \quad (9-3)$$

which shows that the window area is linearly proportional to the number of turns chosen by the designer.

9-4-2 Core Cross-Sectional Area A_{core}

The core cross-sectional area in Figs. 9-1a and b depends on the peak flux $\hat{\phi}$ and the choice of the maximum allowed flux density B_{max} to limit core losses:

$$A_{core} = \frac{\hat{\phi}}{B_{max}} \quad (9-4)$$

How the flux is produced depends if the device is an inductor or a transformer. In an inductor, $\hat{\phi}$ depends on the peak current, where $L\hat{I}$ equals the peak flux linkage $N\hat{\phi}$. Hence,

$$\hat{\phi} = \frac{L\hat{I}}{N} \quad (\text{inductor}) \quad (9-5)$$

In a transformer, based on the Faraday's law, the flux depends linearly on the applied volt-seconds and inversely on the number of turns. This is shown in Fig. 9-2 for a Forward converter transformer with $N_1 = N_3$, and the duty-ratio D , which is limited to 0.5. Therefore, we can express the peak flux in Fig. 9-2 as

$$\hat{\phi} = \frac{k_{conv} V_{in}}{N_1 f_s} \quad (9-6)$$

where the factor k_{conv} equals D in Forward converter, and typically has a maximum value of 0.5. The factor k_{conv} can be derived for transformers in other converter topologies based on the specified operating conditions, for example, it equals $D/2$ in a Full-Bridge converter. In general, the peak flux can be expressed in terms of any one of the windings, y for example, as

$$\hat{\phi} = \frac{k_{conv} V_y}{N_y f_s} \quad (\text{transformer}) \quad (9-7)$$

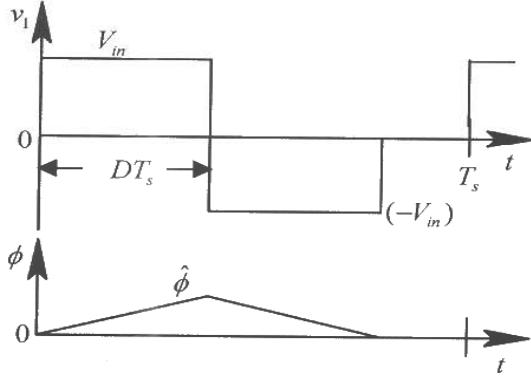


Figure 9-2 Waveforms in a transformer for a Forward converter.

Substituting for $\hat{\phi}$ from Eq. 9-5 or 9-7 into Eq. 9-4,

$$A_{core} = \frac{L\hat{I}}{NB_{max}} \quad (\text{inductor}) \quad (9-8)$$

$$A_{core} = \frac{k_{conv}V_y}{N_y f_s B_{max}} \quad (\text{transformer}) \quad (9-9)$$

Eqs. 9-8 and 9-9 show that in both cases, the core cross-sectional area is inversely proportional to the number of turns chosen by the designer.

9-4-3 Core Area-Product $A_p (= A_{core} A_{window})$

The core area-product is obtained by multiplying the core cross-sectional area A_{core} with its window area A_{window} :

$$A_p = A_{core} A_{window} \quad (9-10)$$

Substituting for A_{window} and A_{core} from the previous equations,

$$A_p = \frac{L\hat{I} I_{rms}}{k_w J_{max} B_{max}} \quad (\text{inductor}) \quad (9-11)$$

$$A_p = \frac{k_{conv} \sum V_y I_{y,rms}}{k_w B_{max} J_{max} f_s} \quad (\text{transformer}) \quad (9-12)$$

Eqs. 9-11 and 9-12 show that the area-product that represents the overall size of the device is independent (as it ought to be) of the number of turns. After all, the core and the overall component size should depend on the electrical specifications and the assumed values of B_{max} and J_{max} , and *not* on the number of turns which is an internal design variable.

9-4-4 Design Procedure Based on Area-Product A_p

Once we pick the appropriate material and the shape for a core, the cores by various manufacturers are cataloged based on the area-product A_p . Having calculated the value of A_p above, we can select the appropriate core. It should be noted that there are infinite combinations of the core cross-sectional area A_{core} and the window area A_{window} that yield a desired area-product A_p . However, manufacturers take pains in producing cores such that for a given A_p , a core has A_{core} and A_{window} that are individually optimized for power density. Once we select a core, it has specific A_{core} and A_{window} , which allow the number of turns to be calculated as follows:

$$N = \frac{LI}{B_{\max} A_{core}} \quad (\text{inductor ; from Eq. 9-8}) \quad (9-13)$$

$$N_y = \frac{k_{conv}V_y}{A_{core}f_s B_{\max}} \quad (\text{transformer ; from Eq. 9-9}) \quad (9-14)$$

In an inductor, to ensure that it has the specified inductance, an air gap of an appropriate length ℓ_g is introduced in the path of flux lines. Assuming the chosen core material to have very high permeability, the core inductance is primarily dictated by the reluctance \mathfrak{R}_g of the air gap, such that

$$L = \frac{N^2}{\mathfrak{R}_g} \quad (9-15)$$

where,

$$\mathfrak{R}_g \approx \frac{\ell_g}{\mu_o A_{core}} \quad (9-16)$$

Using Eqs. 9-15 and 9-16, the air gap length ℓ_g can be calculated as

$$\ell_g = \frac{N^2 \mu_o A_{core}}{L} \quad (9-17)$$

The above equations are approximate because they ignore the effects of finite core permeability and the fringing flux, which can be substantial. Core manufacturers generally specify measured inductance as a function of the number of turn for various values of the air gap length. In this section, we used a toroidal core for descriptive purposes in which it will be difficult to introduce an air gap. If a toroidal core must be used, it can be picked with a distributed air gap such that it has the effective air gap

length as calculated above. The above procedure explained for toroidal cores is equally valid for other types of cores. The actual design described in the next section illustrates the introduction of air gap in a pot core.

9-5 DESIGN EXAMPLE OF AN INDUCTOR

In this example, we will discuss the design of an inductor that has an inductance $L = 100\mu H$. The worst-case current through the inductor is shown in Fig. 9-3, where the average current $I = 5.0 A$, and the peak-peak ripple $\Delta I = 0.75 A$ at the switching frequency $f_s = 100kHz$. We will assume the following maximum values for the flux density and the current density: $B_{max} = 0.25T$, and $J_{max} = 6.0A/mm^2$ (for larger cores, this is typically in a range of 3 to $4A/mm^2$). The window fill factor is assumed to be $k_w = 0.5$.

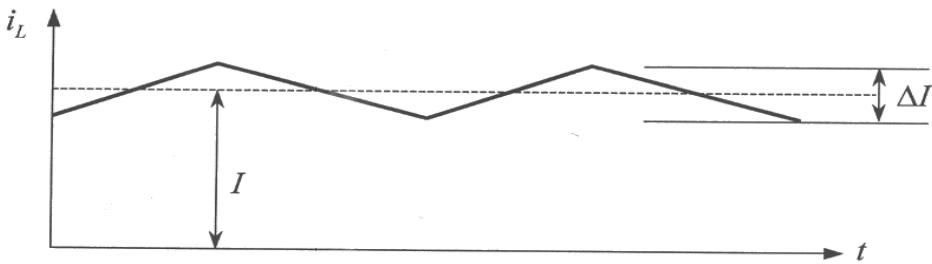


Figure 9-3 Inductor current waveforms.

The peak value of the inductor current from Fig. 9-3 is $\hat{I} = I + \frac{\Delta I}{2} = 5.375 A$. The rms value of the current for the waveform shown in Fig. 9-3 can be calculated as $I_{rms} = \sqrt{I^2 + \frac{1}{12}\Delta I^2} \approx 5.0 A$ (the derivation is left as a homework problem).

From Eq. 9-11,

$$\text{Area-Product } A_p = \frac{100 \times 10^{-6} \times 5.375 \times 5}{0.5 \times 0.25 \times 6 \times 10^6} \times 10^{12} = 3587 mm^4$$

From the Magnetics, Inc. catalog [2], we will select a P-type material, which has the saturation flux density of $0.5T$ and is quite suitable for use at the switching frequency of $100kHz$. A pot core 26×16 , which is shown in Fig. 9-4 for a laboratory experiment, has the core Area $A_{core} = 93.1 mm^2$ and the window Area $A_{window} = 39 mm^2$. Therefore, we will select this core, which has an Area-Product $A_p = 93.1 \times 39 = 3631 mm^4$. From Eq. 9-13,

$$N = \frac{100\mu \times 5.375}{0.25 \times 93.1 \times 10^{-6}} \approx 23 \text{ Turns}$$

Winding wire cross sectional area $A_{cond} = I_{rms} / J_{max} = 5.0 / 6.0 = 0.83 mm^2$. We will use five strands of American Wire Gauge AWG 25 wires [3], each with a cross-sectional area of $0.16 mm^2$, in parallel. From Eq. 9-17, the air gap length can be calculated as

$$\ell_g = \frac{23^2 \times 4\pi \times 10^{-7} \times 93.1 \times 10^{-6}}{100\mu} \approx 0.62 mm.$$

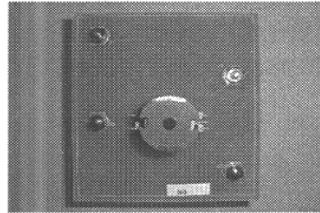


Figure 9-4 Pot core mounted on a plug-in board.

9-6 DESIGN EXAMPLE OF A TRANSFORMER FOR A FORWARD CONVERTER

The required electrical specifications for the transformer in a Forward converter are as follows: $f_s = 100 kHz$ and $V_1 = V_2 = V_3 = 30V$. Assume the rms value of the current in each winding to be $2.5 A$. We will choose the following values for this design: $B_{max} = 0.25 T$ and $J_{max} = 5 A/mm^2$. From Eq. 9-12, where $k_w = 0.5$ and $k_{conv} = 0.5$,

$$A_p = \frac{k_{conv}}{k_w f_s B_{max} J_{max}} \sum_y \hat{V}_y I_{rms,y} = 1800 mm^4$$

For the pot core 22×13 [2], $A_{core} = 63.9 mm^2$, $A_{window} = 29.2 mm^2$, and therefore $A_p = 1866 mm^4$. For this core, the winding wire cross-sectional area is obtained as

$$A_{cond,1} = \frac{I_{1,rms}}{J_{max}} = \frac{2.5}{5} = 0.5 mm^2.$$

We will use three strands of AWG 25 wires [3], each with a cross-sectional area of $0.16 mm^2$, in parallel for each winding. From Eq. 9-14,

$$N_1 = \frac{0.5 \times 30}{(63.9 \times 10^{-6}) \times (100 \times 10^3) \times 0.25} \approx 10.$$

Hence,

$$N_1 = N_2 = N_3 = 10.$$

9-7 THERMAL CONSIDERATIONS

Designs presented here do not include eddy current losses in the windings, which can be very substantial due to proximity effects in inductors. These effects are carefully considered in [1]. Therefore, the area-product method is a good starting point, but the designs must be evaluated for temperature rise based on thermal considerations.

REFERENCES

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.
2. Magnetics, Inc. Ferrite Cores (www.mag-inc.com).
3. Wire Gauge Comparison Chart (www.tool-portals.com/de/umrechnung/gaugesolid.asp).

PROBLEMS

Inductor Design

- 9-1 Derive the expression for the rms current for the current waveform in Fig. 9-3.
- 9-2 In the design example of the inductor in this chapter, the core has an area $A_{core} = 93.1 \text{ mm}^2$, the magnetic path $\ell = 37.6 \text{ mm}$, and the relative permeability of the core material is $\mu_r = \mu_m / \mu_0 = 5000$. Calculate the inductance with 31 turns if the air gap is not introduced in this core in the flux path.
- 9-3 In the inductor design presented in this chapter, what is the reluctance offered by the magnetic core as compared to that offered by the air gap?
- 9-4 In Problem 9-2, what is the maximum current that will cause the peak flux density to reach 0.25 T ?
- 9-5 In the inductor designed in this chapter, what will be the inductance and the maximum current that can be passed without exceeding the B_{max} specified, if the air gap introduced by mistake is only one-half of the required value $\ell_g = 1 \text{ mm}$.
What is the stored energy with $\ell_g = 0.5 \text{ mm}$ compared to that at $\ell_g = 1 \text{ mm}$?

Transformer Design

- 9-6 In the design example of the transformer in this chapter, the core has an area $A_{core} = 63.9 \text{ mm}^2$, the magnetic path $\ell = 31.2 \text{ mm}$, and the relative permeability of the core material is $\mu_r = \mu_m / \mu_0 = 5000$. Calculate the peak magnetizing current at duty-ratio of 0.5.
- 9-7 What is the tertiary winding conductor diameter needed for the magnetizing current calculated in Problem 9-6?
- 9-8 Derive k_{conv} for a transformer in a Full-Bridge converter.

Chapter 10

SOFT-SWITCHING IN DC-DC CONVERTERS AND CONVERTERS FOR INDUCTION HEATING AND COMPACT FLUORESCENT LAMPS

10-1 INTRODUCTION

In converters so far, we have discussed hard switching in the switching power-pole, as described in Chapter 2. In this chapter, we will look at the problems associated with hard switching, and some of the practical circuits where this problem can be minimized with soft-switching.

10-2 HARD-SWITCHING IN SWITCHING POWER-POLES

In the switching power-pole repeated in Fig. 10-1a, the hard-switching waveforms are as shown in Fig. 10-1b, which were discussed in Chapter 2. Because of the simultaneously high voltage and current associated with the transistor during the switching transition, the switching power losses in the transistor increase linearly proportional to the switching frequency and the times $t_{c(on)}$ and $t_{c(off)}$ shown in Fig. 10-1b, assuming an ideal diode

$$P_{sw} \propto f_s (t_{c(on)} + t_{c(off)}) \quad (10-1)$$

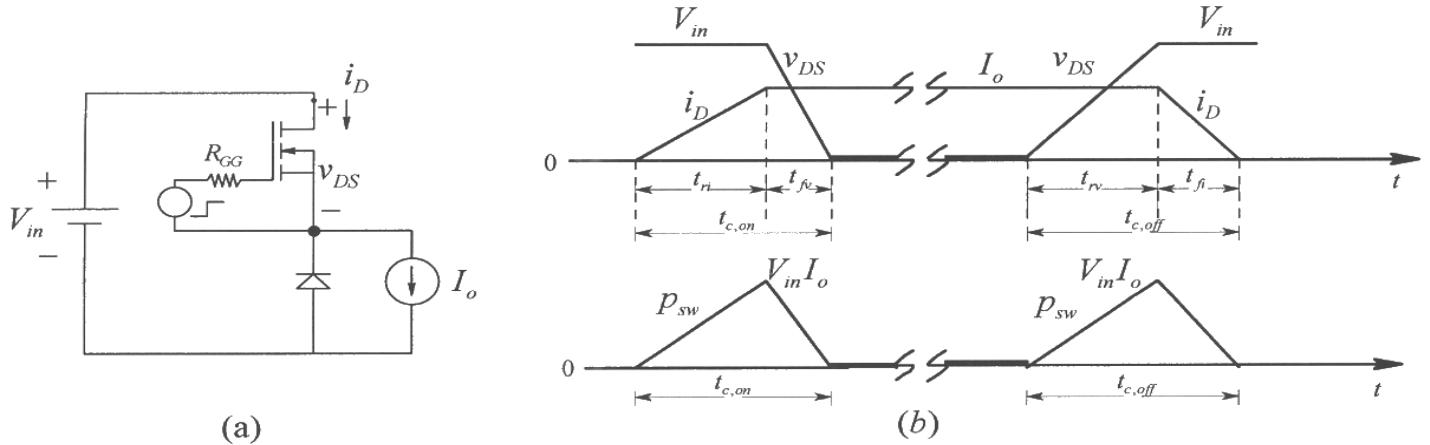


Figure 10-1 Hard switching in a power-pole.

In hard-switching converters, in addition to the switching power losses decreasing the energy efficiency, the other problems are device stresses, thermal management of power losses, and electromagnetic interference resulting from high di/dt and dv/dt due to fast

transitions in the converter voltages and currents. The above problems are exacerbated by the presence of the stray capacitances and leakage inductances associated with the converter layout and the components.

In order to reduce the overall converter size, while maintaining high energy efficiency, the trend is to design dc-dc converters operating at as high a switching frequency as possible (typically 100-200 kHz in small power ratings), using fast-switching MOSFETs. At high switching frequency, the switching power losses become unacceptable if hard-switching is used, and hence soft-switching is often employed, as briefly described in this chapter.

The problems described above, associated with hard-switching, can be minimized by means of the following:

- Circuit layout to reduce stray capacitances and inductances
- Snubbers to reduce di/dt and dv/dt
- Gate-drive control to reduce di/dt and dv/dt
- Soft-switching

It is always recommended to have a layout to reduce stray capacitances and inductances. Snubbers, as describe in the Appendix on the accompanying CD, consist of passive elements (R, C and possibly a diode) to reduce di/dt and dv/dt during the switching transient, by shaping the switching trajectory. The trend in modern power electronics is to use snubbers only in transformer-isolated dc-dc converters, where the leakage inductance associated with the high-frequency transformer can be substantial, in spite of a good circuit layout. Generally, snubbers do not reduce the overall losses; rather they shift some of the switching losses in the transistor to the snubber resistor.

By controlling the gate voltage of MOSFETs and IGBTs, it is possible to slow down the turn-on and turn-off speed, thereby resulting in reduced di/dt and dv/dt , at the expense of higher switching losses in the transistor. The above techniques, at best, result in a partial solution to the problems of hard-switching.

However, there are certain topologies and control, as described in the next section, that allow soft-switching that essentially eliminate the drawbacks of hard-switching without creating new problems.

10-3 SOFT-SWITCHING IN SWITCHING POWER-POLES

There are many such circuits and control techniques proposed in the literature, most of which may make the problem of EMI and the overall losses worse due to large conduction losses in the switches and other passive components. Avoiding these topologies, only a few soft-switching circuits are practical.

The goal in soft-switching is that the switching transition in the power-pole occurs under very favorable conditions, that is, the switching transistor has a zero voltage and/or zero current associated with it. Based on these conditions, the soft-switching circuits can be classified as follows:

- ZVS (zero voltage switching), and
- ZCS (zero current switching)

We will consider only the converter circuits using MOSFETs, which result in ZVS (zero voltage switching). The reason is that, based on Eq. 10-1, soft-switching is of interest at high switching frequencies where MOSFETs are used. In MOSFETs operating at high switching frequencies, a significant reduction of switching loss is achieved by not dissipating the charge associated with the junction capacitance inside the MOSFET each time it turns on. This implies that for a meaningful soft-switching, the MOSFETs should be turned on under a zero voltage switching (ZVS) condition. As we will see shortly, the turn-off also occurs at ZVS.

10-3-1 Zero Voltage Switching (ZVS)

To illustrate the ZVS principle, the intrinsic anti-parallel diode of the MOSFET is shown as being distinct in Figs. 10-2a and b, where a capacitor is used in parallel. This MOSFET is connected in a circuit such that before applying the gate voltage to turn the MOSFET on, the switch voltage is brought to zero and the anti-parallel diode is conducting as shown in Fig. 10-2a. This results in an ideal loss-less turn on at ZVS. At turn-off, as shown in Fig. 10-2b, the capacitor across the switch results in an essentially ZVS turn-off where the current through the MOSFET channel is removed while the voltage across the device remains small (essentially zero) due to the parallel capacitor. This ZVS principle is illustrated by modifying the synchronous-rectified Buck dc-dc converter, as discussed below.

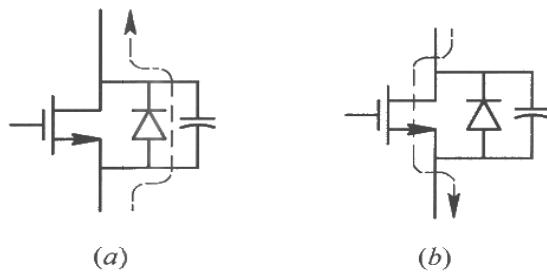


Figure 10-2 ZVS in a MOSFET.

10-3-2 Synchronous Buck Converter with ZVS

As discussed in section 3-10 of Chapter 3, a synchronous-rectified Buck dc-dc converter, used in applications where the output voltage is very low, is shown in Fig. 10-3a where the diode is replaced by another MOSFET and the two MOSFETs are provided

complimentary gate signals q^+ and q^- . The waveforms associated with this synchronous Buck converter are shown in Fig. 10-3b, where the inductor is large such that the inductor-current ripple is small (shown by the solid curve in Fig. 10-3b), and the inductor current remains positive in the direction shown in Fig. 10-3a in the continuous conduction mode.

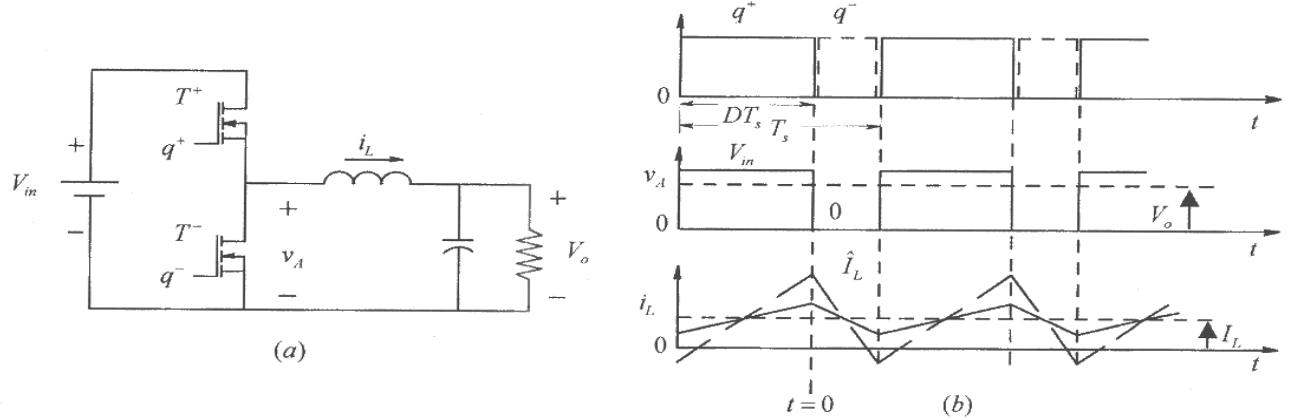


Figure 10-3 Synchronous-rectified Buck converter.

To achieve ZVS, the circuit of Fig. 10-3a is modified as shown in Fig. 10-4a by showing the internal diode of the MOSFET explicitly, and adding small external capacitances (in addition to the junction capacitances inherent in MOSFETs). The inductance value in this circuit is chosen to be much smaller such that the inductor current has a waveform shown dotted in Fig. 10-3b with a large ripple, such that the current i_L is both positive as well negative during every switching cycle.

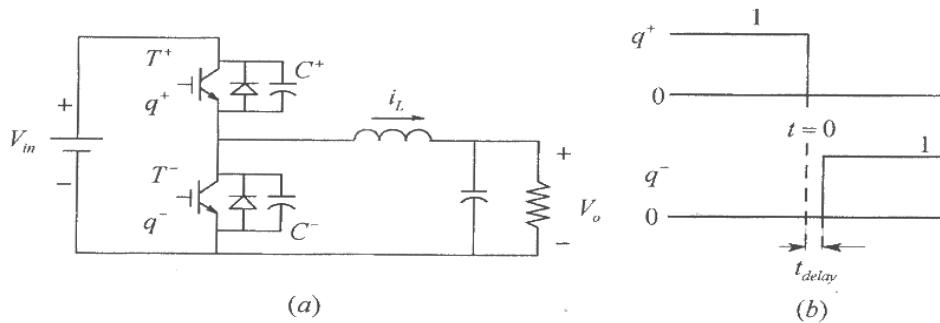


Figure 10-4 Synchronous-rectified Buck converter with ZVS.

We will consider the transition at the time $t = 0$ labeled in Fig. 10-3b and Fig. 10-4b, when the inductor current is at its peak \hat{I}_L in Fig. 10-4a. The gate signal q^+ of the transistor T^+ , which is initially conducting \hat{I}_L , goes to zero, while q^- remains zero, as shown in Fig. 10-4b. During the transition time during which the current transfers from T^+ to T^- is very short, and it is reasonable to assume for discussion purposes that the inductor current remains constant at \hat{I}_L as shown in Fig. 10-5a.

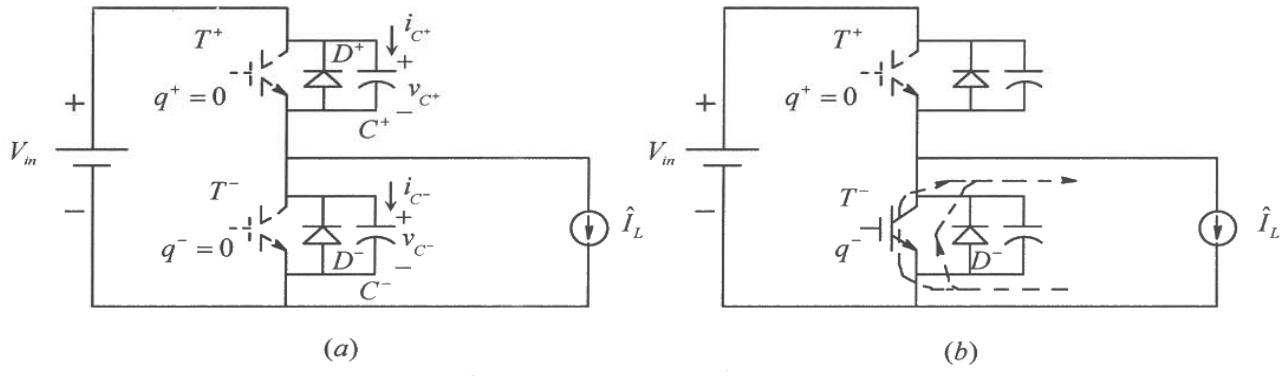


Fig. 10-5 Transition in synchronous-rectified Buck converter with ZVS.

In the circuit of Fig. 10-5a with both q^+ and q^- equal to zero, initially $v_{C^+}(0)=0$ and $v_{C^-}(0)=V_{in}$, where from Kirchhoff's law these two voltages must add to the input voltage

$$v_{C^+} + v_{C^-} = V_{in} \quad (10-2)$$

As the current through T^+ declines, equal and opposite currents flow through the two capacitors in Fig. 10-5a, which can be derived from Eq. 10-2 as follows, assuming equal capacitances C : differentiating both sides of Eq. 10-2 and multiplying both sides by C

$$C \frac{d}{dt} v_{C^+} + C \frac{d}{dt} v_{C^-} = 0 \quad (10-3)$$

$$i_{C^+} + i_{C^-} = 0 \quad \Rightarrow \quad i_{C^+} = -i_{C^-} \quad (10-4)$$

As the current through T^+ declines, a positive i_{C^+} causes v_{C^+} to rise from 0, and a negative i_{C^-} causes v_{C^-} to decline from its initial value of V_{in} . If this voltage transition happens slowly compared to the current fall time of the MOSFET T^+ , then the turn-off of T^+ is achieved at essentially zero voltage (ZVS). After the current through T^+ has gone to zero, applying the Kirchhoff's current law in Fig. 10-5a and using Eq. 10-4 results in

$$i_{C^+} = -i_{C^-} = \frac{\hat{I}_L}{2} \quad (10-5)$$

In Fig. 10-5a, during the turn-off transition of T^+ , v_{C^+} rises to V_{in} and v_{C^-} declines to 0. The voltage v_{C^-} cannot become negative because of the diode D^- (assuming an ideal diode with zero forward voltage drop), which begins to conduct the entire \hat{I}_L in Fig. 10-5b, marking the ZVS turn-off of T^+ .

Once D^- begins to conduct, the voltage is zero across T^- , which is applied a gate signal q^- to turn-on, as shown in Fig. 10-4b, thus resulting in the ZVS turn-on of T^- . Subsequently, the entire inductor current begins to flow through the channel of T^- in Fig. 10-5b. The important item to note here is that the gate signal to T^- is appropriately delayed by an interval T_{delay} shown in Fig. 10-4b, making sure that q^- is applied after D^- begins to conduct.

The next half-cycle in this converter is similar with the ZVS turn-off of T^- , followed by the ZVS turn-on of T^+ , facilitated by the negative peak of the inductor current.

Although this Buck converter results in ZVS turn-on and turn-off of both transistors, the inductor current has a large ripple, which will also make the size of the filter capacitor large since it has to carry the inductor current ripple. In order to make this circuit practical, the overall ripple that the output capacitor has to carry can be made much smaller (similar ripple reduction occurs in the current drawn from the input source) by interleaving of two or more such converters, as discussed in section 3-11 of Chapter 3.

10-3-3 Phase-Shift Modulated (PSM) DC-DC Converter

Another practical soft-switching technology is the phase-shift modulated (PSM) dc-dc converter shown in Fig. 10-6a.

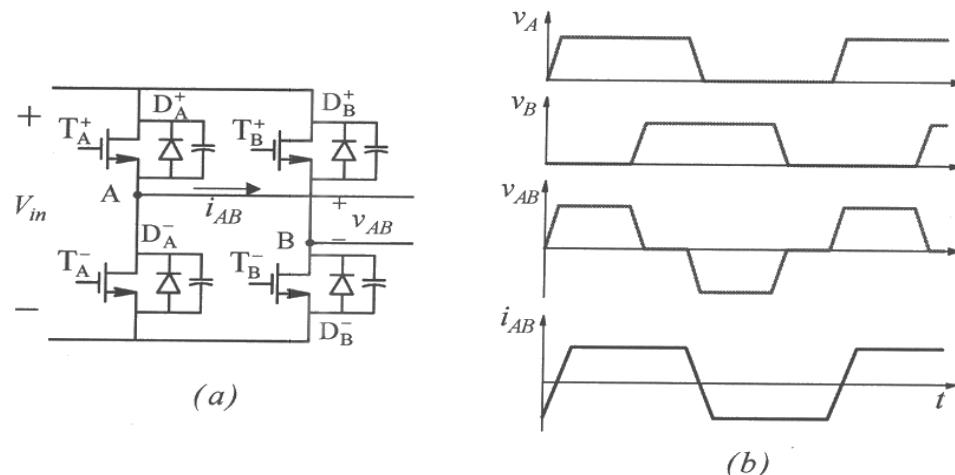


Figure 10-6 Phase-Shift Modulated (PSM) DC-DC Converter.

It is a variation of the PWM dc-dc converters discussed in Chapter 8. The switches in each power-pole of the PSM converter operate at nearly 50 percent duty-ratio and the regulation of the output voltage is provided by shifting the output of one switching power-pole with respect to the other, as shown in Fig. 10-6b, to control the zero-voltage intervals in the transformer primary voltage v_{AB} . To provide the ZVS turn-on and turn-off of switches, a capacitor is placed across each switch. This topology makes use of the transformer leakage inductance and the magnetizing current. The operation of this circuit

and a superior hybrid topology shown in Fig. 10-7, patented by the University of Minnesota [3-5], are fully described in the Appendix to this chapter on the accompanying CD.

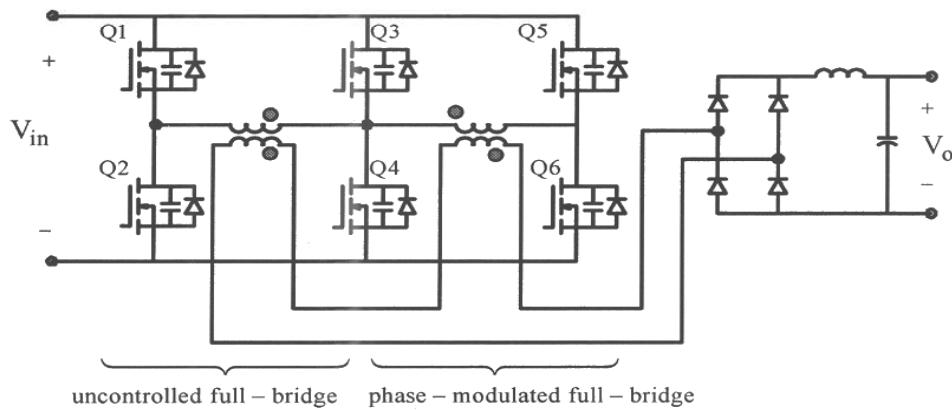


Figure 10-7 A superior hybrid topology to achieve ZVS down to no load [3-5].

10-4 INVERTERS FOR INDUCTION HEATING AND COMPACT FLUORESCENT LAMPS

It is possible to achieve soft-switching in converters for induction heating and compact fluorescent lamps. These converters are discussed in the Appendix to this chapter on the accompanying CD.

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2. R. Ayyanar, N. Mohan, and E. Persson, “Soft-Switching in DC-DC Converters: Principles, Practical Topologies, Design Techniques, Latest Developments,” Tutorial at IEEE-APEC 2002.
3. R. Ayyanar and N. Mohan, US Patent 6,310,785, University of Minnesota, 2001.
4. R. Ayyanar and N. Mohan, “Novel soft-switching dc-dc converter with full ZVS-range and reduced filter requirement – Part I: Regulated output applications”, IEEE Transactions on Power Electronics, vol. 16 (2001), March 2001, p. 184-192.
5. R. Ayyanar and N. Mohan, “Novel soft-switching dc-dc converter with full ZVS-range and reduced filter requirement – Part II: Constant-input, variable output applications”, IEEE Transactions on Power Electronics, vol. 16 (2001), March 2001, p. 193-200.

PROBLEMS

- 10-1 In a synchronous-rectified Buck converter with ZVS shown in Fig. 10-4a, $V_{in} = 12V$, $V_o = 5V$, $f_s = 100\text{ kHz}$, and the maximum load is $20W$. Calculate the filter inductance such that the negative peak current is at least 1.5Amps.

- 10-2 In Problem 10-1, calculate the capacitances across the MOSFETs if the charge/discharge time is to be no more than $0.5 \mu s$.

Chapter 11

ELECTRIC MOTOR DRIVES

11-1 INTRODUCTION

Motor drives (ac and dc) form an extremely important application area of power electronics with market value of tens of billions dollars annually in applications described in Chapter 1. Figure 11-1 shows the block diagram of an electric-motor drive, or for short, an electric drive. In response to an input command, electric drives efficiently control the speed and/or the position of the mechanical load. The controller, by comparing the input command for speed and/or position with the actual values measured through sensors, provides appropriate control signals to the power-processing unit (PPU) consisting of power semiconductor devices.

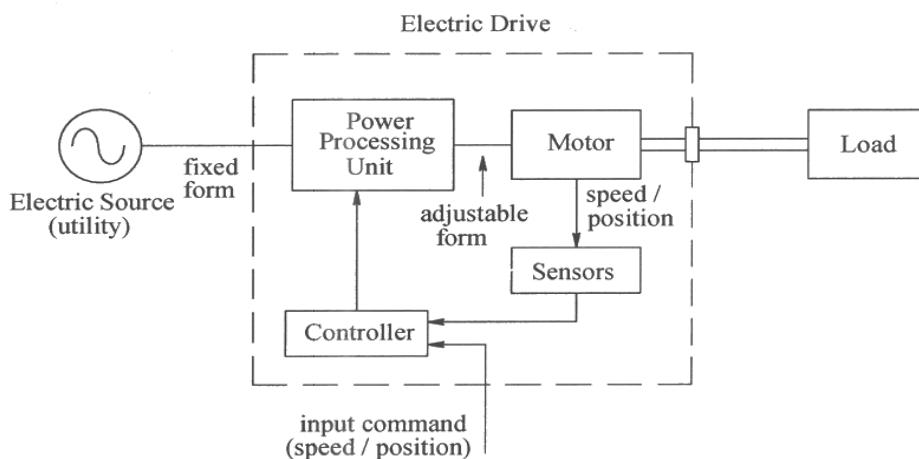


Figure 11-1 Block diagram of an electric drive system.

As Fig. 11-1 shows, the power-processing unit gets its power from the utility source with single-phase or three-phase sinusoidal voltages of a fixed frequency and constant amplitude. The power-processing unit, in response to the control inputs, efficiently converts these fixed-form input voltages into an output of the appropriate form (in frequency, amplitude, and the number of phases) that is optimally suited for operating the motor. The input command to the electric drive in Fig. 11-1 may come from a process computer, which considers the objectives of the overall process and issues a command to control the mechanical load. However, in general-purpose applications, electric drives operate in an open-loop manner without any feedback.

Prior to discussing the need for power electronics in electric drives for speed and position control of mechanical systems, we will briefly examine the requirements of mechanical

systems, and various types of electric machines in terms of their terminal characteristics in steady state in order to determine the voltage and current ratings in designing the power electronics interface.

11-2 MECHANICAL SYSTEM REQUIREMENTS

Electric drives must satisfy the requirements of torque and speed imposed by mechanical loads connected to them. Most electric motors are of rotating type.

11-2-1 Rotational Motor-Load Systems

To understand rotating systems, consider a lever, pivoted and free to move. When an external force f is applied in a *perpendicular* direction at a radius r from the pivot, then the torque acting on the lever is

$$\frac{T}{[Nm]} = \frac{f}{[N]} r \quad (11-1)$$

which acts in a counter-clockwise direction, considered here to be positive.

In a rotational system, the angular acceleration due to a net torque acting on it is determined by its moment-of-inertia J . The net torque T_J acting on the rotating body of inertia J causes it to accelerate. Similar to systems with linear motion, Newton's Law in rotational systems becomes

$$T_J = J\alpha \quad (11-2)$$

where the angular acceleration $\alpha (= d\omega_m / dt)$ in rad/s^2 is

$$\alpha = \frac{d\omega_m}{dt} = \frac{T_J}{J} \quad (11-3)$$

In MKS units, a torque of $1 Nm$, acting on an inertia of $1 kg \cdot m^2$ results in an angular acceleration of $1 rad/s^2$.

In systems such as the one shown in Fig. 11-2a, the motor produces an electromagnetic torque T_{em} . The bearing friction and wind resistance (drag) can be combined with the load torque T_L opposing the rotation. In most systems, we can assume that the rotating part of the motor with inertia J_M is rigidly coupled (without flexing) to the load inertia J_L . The net torque, the difference between the electromagnetic torque developed by the motor and the load torque opposing it, causes the combined inertias of the motor and the load to accelerate in accordance with Eq. 11-3: