

With the equations and values given in Fig. 20-3, the closed-loop voltage gain is

$$A_v = \frac{-100 \text{ k}\Omega}{10 \text{ k}\Omega} = -10$$

The minimum feedback fraction is:

$$B_{\min} \cong \frac{10 \text{ k}\Omega \parallel 100 \text{ }\Omega}{100 \text{ k}\Omega} \cong 0.001$$

The maximum feedback fraction is:

$$B_{\max} \cong \frac{10 \text{ k}\Omega \parallel 10.1 \text{ k}\Omega}{100 \text{ k}\Omega} \cong 0.05$$

If  $f_{\text{unity}} = 1 \text{ MHz}$ , the minimum and maximum bandwidths are:

$$f_{2(CL)\min} = (0.001)(1 \text{ MHz}) = 1 \text{ kHz}$$

$$f_{2(CL)\max} = (0.05)(1 \text{ MHz}) = 50 \text{ kHz}$$

In summary, when  $R$  varies from  $100 \Omega$  to  $10 \text{ k}\Omega$ , the voltage gain remains constant but the bandwidth varies from 1 to 50 kHz.

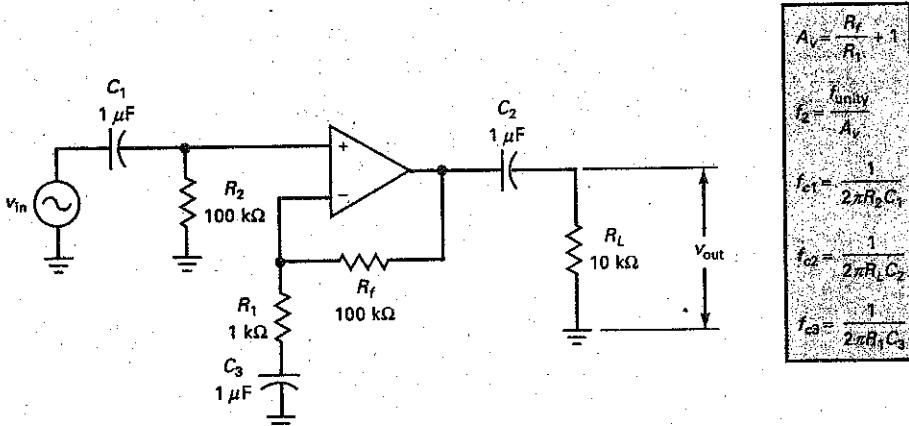
## 20-2 Noninverting-Amplifier Circuits

The noninverting amplifier is another basic op-amp circuit. Advantages include stable voltage gain, high input impedance, and low output impedance. Here are some applications.

### AC-Coupled Amplifier

Figure 20-4 shows an ac-coupled noninverting amplifier and its analysis equations.  $C_1$  and  $C_2$  are coupling capacitors.  $C_3$  is a bypass capacitor. Using a bypass capacitor has the advantage of minimizing the output offset voltage. Here's why: In the midband of the amplifier, the bypass capacitor has a very low impedance.

**Figure 20-4** AC-coupled noninverting amplifier.



Therefore, the bottom of  $R_1$  is at ac ground. In the midband, the feedback fraction is:

$$B = \frac{R_f}{R_1 + R_f} \quad (20-1)$$

In this case, the circuit amplifies the input voltage as previously described.

When the frequency is zero, the bypass capacitor  $C_3$  is open and the feedback fraction  $B$  increases to unity because:

$$B = \frac{\infty}{\infty + 1} = 1$$

This equation is valid if we define  $\infty$  as an extremely large value, which is what the impedance equals at zero frequency. With  $B$  equal to 1, the closed-loop voltage gain is unity. This reduces the output offset voltage to a minimum.

With values given in Fig. 20-4, we can calculate the midband voltage gain as:

$$A_v = \frac{100 \text{ k}\Omega}{1 \text{ k}\Omega} + 1 = 101$$

If  $f_{\text{unity}}$  is 15 MHz, the bandwidth is:

$$f_{2(\text{CL})} = \frac{15 \text{ MHz}}{101} = 149 \text{ kHz}$$

The input coupling capacitor produces a cutoff frequency of:

$$f_{c1} = \frac{1}{2\pi(100 \text{ k}\Omega)(1 \mu\text{F})} = 1.59 \text{ Hz}$$

Similarly, the output coupling capacitor,  $C_2$  and the load resistance  $R_L$  produce a cutoff frequency  $f_{c2}$ :

$$f_{c2} = \frac{1}{2\pi(10 \text{ k}\Omega)(1 \mu\text{F})} = 15.9 \text{ Hz}$$

The bypass capacitor produces a cutoff frequency of:

$$f_{c3} = \frac{1}{2\pi(1 \text{ k}\Omega)(1 \mu\text{F})} = 159 \text{ Hz}$$

## Audio Distribution Amplifier

Figure 20-5 shows an ac-coupled noninverting amplifier driving three voltage followers. This is one way to distribute an audio signal to several different outputs. The closed-loop voltage gain and bandwidth of the first stage are given by the familiar equations shown in Fig. 20-5. For the values shown, the closed-loop voltage gain is 40. If  $f_{\text{unity}}$  is 1 MHz, the closed-loop bandwidth is 25 kHz.

Incidentally, an op amp like an LM348 is convenient to use in a circuit like Fig. 20-5 because the LM348 is a quad 741—four 741s in a 14-pin package. One of the op amps can be the first stage, and the others can be the voltage followers.

## JFET-Switched Voltage Gain

Some applications require a change in closed-loop voltage gain. Figure 20-6 shows a noninverting amplifier whose voltage gain is controlled by a JFET that acts like a switch. The input voltage to the JFET is a two-state voltage, either zero or  $V_{GS(\text{off})}$ . When the control voltage is low, it equals  $V_{GS(\text{off})}$  and the JFET is open.

Figure 20-5 Distribution amplifier.

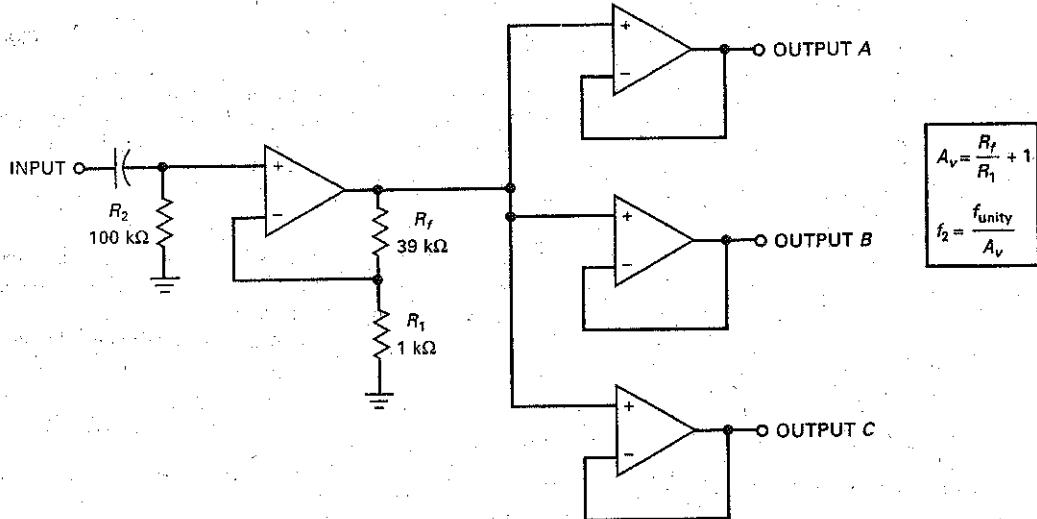
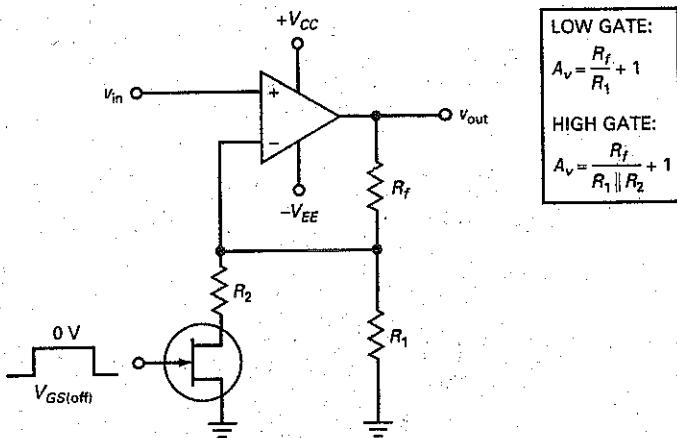


Figure 20-6 JFET switch controls voltage gain.



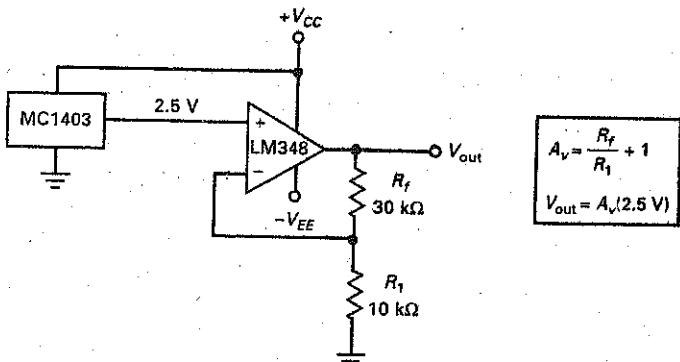
In this case,  $R_2$  is ungrounded and the voltage gain is given by the usual equation for a noninverting amplifier (the top equation in Fig. 20-6).

When the control voltage is high, it equals 0 V and the JFET switch is closed. This puts  $R_2$  in parallel with  $R_1$ , and the closed-loop voltage gain decreases to:

$$A_v = \frac{R_f}{R_1 \parallel R_2} + 1 \quad (20-2)$$

In most designs,  $R_2$  is made much larger than  $r_{ds(\text{on})}$  to prevent the JFET resistance from affecting the closed-loop voltage gain. Sometimes, you may see several resistors and JFET switches in parallel with  $R_1$  to provide a selection of different voltage gains.

Figure 20-7 Voltage reference.



## Voltage Reference

The MC1403 is a special-function IC called a **voltage reference**, a circuit that produces an extremely accurate and stable value of output voltage. For any positive supply voltage between 4.5 to 40 V, it produces an output voltage of 2.5 V with a tolerance of  $\pm 1$  percent. The temperature coefficient is only 10 ppm/ $^{\circ}\text{C}$ . The abbreviation *ppm* stands for "part per million" (1 ppm is equivalent to 0.0001 percent). Therefore, 10 ppm/ $^{\circ}\text{C}$  produces a change of only 2.5 mV for a 100 $^{\circ}\text{C}$  change in temperature ( $10 \times 0.0001 \text{ percent} \times 100 \times 2.5 \text{ V}$ ). The point is that the output voltage is ultra-stable and equal to 2.5 V over a large temperature range.

The only problem is that 2.5 V may be too low a voltage reference for many applications. For instance, suppose we want a voltage reference of 10 V. Then, one solution is to use an MC1403 and a noninverting amplifier as shown in Fig. 20-7. With the circuit values shown, the voltage gain is:

$$A_v = \frac{30 \text{ k}\Omega}{10 \text{ k}\Omega} + 1 = 4$$

and the output voltage is:

$$V_{out} = 4(2.5 \text{ V}) = 10 \text{ V}$$

Because the closed-loop voltage gain of the noninverting amplifier is only 4, the output voltage will be a stable voltage reference of 10 V.

## Example 20-1

One application for Fig. 20-6 is in a **squelch circuit**. This kind of circuit is used in communication receivers to reduce listener fatigue by having a low voltage gain when no signal is being received. This way, the user does not have to listen to static when there is no communication signal. When a signal comes in, the voltage gain is switched to high.

If  $R_1 = 100 \text{ k}\Omega$ ,  $R_f = 100 \text{ k}\Omega$ , and  $R_2 = 1 \text{ k}\Omega$  in Fig. 20-6, what is the voltage gain when the JFET is on? What is the voltage gain when the JFET is off? Explain how the circuit can be used as part of a squelch circuit.

**SOLUTION** With the equations given in Fig. 20-6, the maximum voltage gain is:

$$A_v = \frac{100 \text{ k}\Omega}{100 \text{ k}\Omega \parallel 1 \text{ k}\Omega} + 1 = 102$$

The minimum voltage gain is:

$$A_v = \frac{100 \text{ k}\Omega}{100 \text{ k}\Omega} + 1 = 2$$

When a communication signal is being received, we can use a peak detector and other circuits to produce a high gate voltage for the JFET in Fig. 20-6. This produces maximum voltage gain while the signal is being received. On the other hand, when no signal is being received, the output of the peak detector is low and the JFET is cut off, producing minimum voltage gain.

## 20-3 Inverter/Noninverter Circuits

In this section, we will discuss circuits in which the input signal drives both inputs of the op amp simultaneously. When an input signal drives both inputs, we get both inverting and noninverting amplification at the same time. This produces some interesting results because the output is the superposition of two amplified signals.

The total voltage gain with an input signal driving both sides of the op amp equals the voltage gain of the inverting channel plus the voltage gain of the noninverting channel:

$$A_v = A_{v(\text{inv})} + A_{v(\text{non})} \quad (20-3)$$

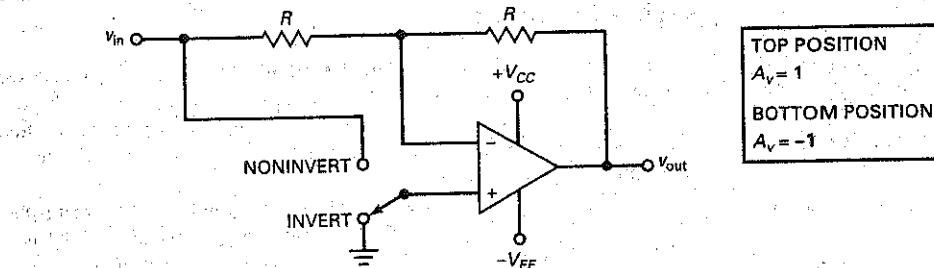
We will use this equation to analyze the circuits of this section.

### Switchable Inverter/Noninverter

Figure 20-8 shows an op amp that can function as either an inverter or a noninverter. With the switch in the lower position, the noninverting input is grounded and the circuit is an inverting amplifier. Since the feedback and input resistances are equal, the inverting amplifier has a closed-loop voltage gain of:

$$A_v = \frac{-R}{R} = -1$$

**Figure 20-8** Reversible voltage gain.



When the switch is moved to the upper position, the input signal drives both the inverting and the noninverting inputs simultaneously. The voltage gain of the inverting channel is still:

$$A_{v(\text{inv})} = -1$$

The voltage gain of the noninverting channel is:

$$A_{v(\text{non})} = \frac{R}{R} + 1 = 2$$

The total voltage gain is the superposition or algebraic sum of the two gains:

$$A_v = A_{v(\text{inv})} + A_{v(\text{non})} = -1 + 2 = 1$$

The circuit is a switchable inverter/noninverter. It has a voltage gain of either 1 or  $-1$ , depending on the position of the switch. In other words, the circuit produces an output voltage with the same magnitude as the input voltage, but the phase can be switched between  $0^\circ$  and  $-180^\circ$ .

### JFET-Controlled Switchable Inverter

Figure 20-9 is a modification of Fig. 20-8. The JFET acts like a voltage-controlled resistance  $r_{ds}$ , discussed in Sec. 13-9. The JFET has either a very low or a very high resistance, depending on the gate voltage.

When the gate voltage is low, it equals  $V_{GS(\text{off})}$  and the JFET is open. Therefore, the input signal drives both inputs. In this case:

$$A_{v(\text{non})} = 2$$

$$A_{v(\text{inv})} = -1$$

and

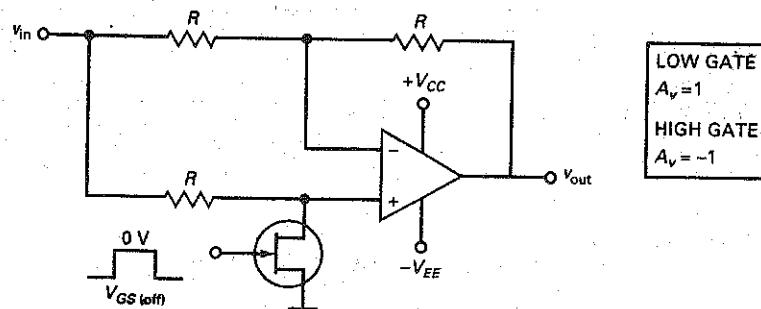
$$A_v = A_{v(\text{inv})} + A_{v(\text{non})} = 1$$

The circuit acts like a noninverting voltage amplifier with a closed-loop voltage gain of 1.

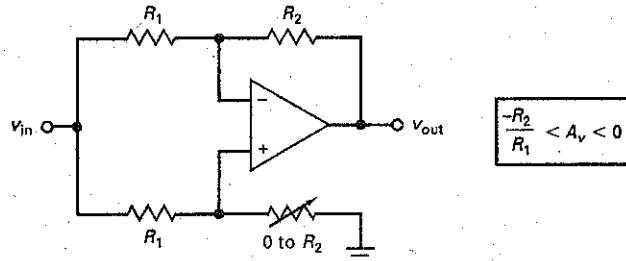
When the gate voltage is high, it equals 0 V and the JFET has a very low resistance. Therefore, the noninverting input is approximately grounded. In this case, the circuit acts like an inverting voltage amplifier with a closed-loop voltage gain of  $-1$ . For proper operation,  $R$  should be at least 100 times greater than the  $r_{ds}$  of the JFET.

In summary, the circuit has a voltage gain that can be either 1 or  $-1$ , depending on whether the control voltage to the JFET is low or high.

Figure 20-9 JFET-controlled reversible gain.



**Figure 20-10** Inverter with adjustable gain.



### Inverter with Adjustable Gain

When the variable resistor of Fig. 20-10 is zero, the noninverting input is grounded and the circuit becomes an inverting amplifier with a voltage gain of  $-R_2/R_1$ . When the variable resistor is increased to  $R_2$ , equal voltages drive the noninverting and inverting inputs of the op amp (common-mode input). Because of the common-mode rejection, the output voltage is approximately zero. Therefore, the circuit of Fig. 20-10 has a voltage gain that is continuously variable from  $-R_2/R_1$  to 0.

### Sign Changer

The circuit of Fig. 20-11 is called a **sign changer**, a rather unusual circuit because its voltage gain can be varied from  $-1$  to  $1$ . Here is the theory of operation: When the wiper is all the way to the right, the noninverting input is grounded and the circuit has a voltage gain of  $-1$ .

$$A_v = -1$$

When the wiper is all the way to the left, the input signal drives the noninverting input as well as the inverting input. In this case, the total voltage gain is the superposition of the inverting and noninverting voltage gains:

$$A_{v(\text{non})} = 2$$

$$A_{v(\text{inv})} = -1$$

$$A_v = A_{v(\text{inv})} + A_{v(\text{non})} = 1$$

In summary, when the wiper is moved from right to left, the voltage gain changes continuously from  $-1$  to  $1$ . At the crossover point (wiper at center), a common-mode signal drives the op amp and the output is ideally zero.

**Figure 20-11** Reversible and adjustable gain of  $\pm 1$ .

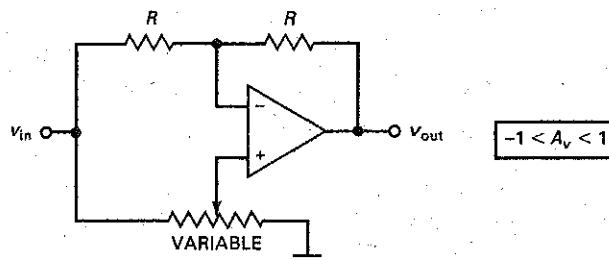
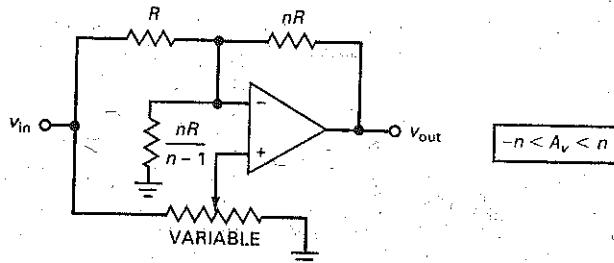


Figure 20-12 Reversible and adjustable gain of  $\pm n$ .



### Adjustable and Reversible Gain

Figure 20-12 shows another unusual circuit. It allows us to adjust the voltage gain between  $-n$  and  $n$ . The theory of operation is similar to that of the sign changer. When the wiper is all the way to the right, the noninverting input is grounded and the circuit becomes an inverting amplifier with a closed-loop voltage gain of:

$$A_v = \frac{-nR}{R} = -n$$

When the wiper is all the way to the left, it can be shown that:

$$A_{v(\text{inv})} = -n$$

$$A_{v(\text{non})} = 2n$$

$$A_v = A_{v(\text{non})} + A_{v(\text{inv})} = n$$

These results can be derived by applying Thevenin's theorem to the circuit and simplifying with algebra.

Circuits like those in Figs. 20-11 and 20-12 are unusual because they have no simple discrete counterparts. They are good examples of circuits that would be difficult to implement with discrete components but are easy to build with op amps.

### Phase Shifter

Figure 20-13 shows a circuit that can ideally produce a phase shift of  $0^\circ$  to  $-180^\circ$ . The noninverting channel has an  $RC$  lag circuit, and the inverting channel has two equal resistors with a value of  $R'$ . Therefore, the voltage gain of the inverting channel is always unity. But the voltage gain of the noninverting channel depends on the cutoff frequency of  $RC$  lag circuit.

When the input frequency is much lower than the cutoff frequency ( $f \ll f_c$ ), the capacitor appears open and:

$$A_{v(\text{non})} = 2$$

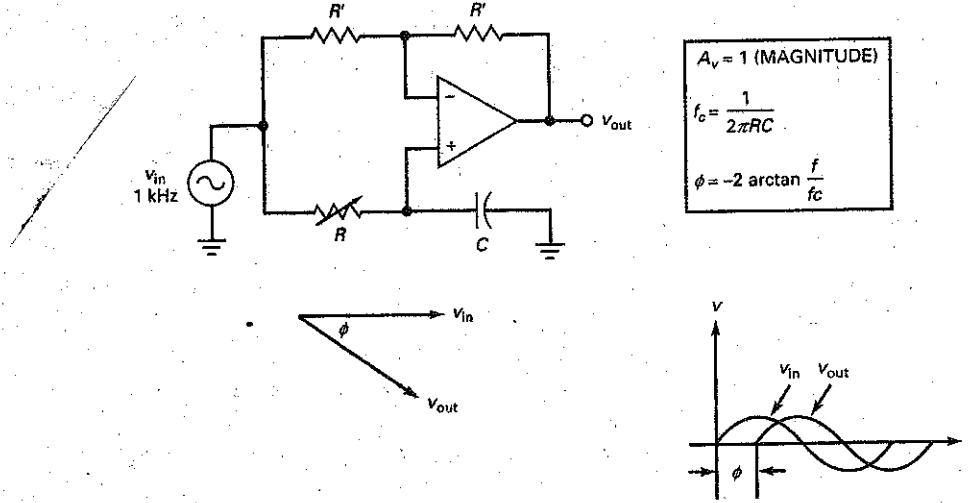
$$A_{v(\text{inv})} = -1$$

$$A_v = A_{v(\text{non})} + A_{v(\text{inv})} = 1$$

This means that the output signal has the same magnitude as the input signal, and the phase shift is  $0^\circ$ , well below the cutoff frequency of the lag network.

When the input frequency is much greater than the cutoff frequency ( $f \gg f_c$ ), the capacitor appears shorted. In this case, the noninverting channel has

**Figure 20-13** Phase shifter.



a voltage gain of zero. The overall gain therefore equals the gain of inverting channel, which is  $-1$ , equivalent to a phase shift of  $-180^\circ$ .

To calculate the phase shift between the two extremes, we need to calculate the cutoff frequency using the equation given in Fig. 20-13. For instance, if  $C = 0.022 \mu\text{F}$  and variable resistor of Fig. 20-13 is set to  $1 \text{k}\Omega$ , the cutoff frequency is:

$$f_c = \frac{1}{2\pi(1 \text{k}\Omega)(0.022 \mu\text{F})} = 7.23 \text{ kHz}$$

With a source frequency of 1 kHz, the phase shift is:

$$\phi = -2 \arctan \frac{1 \text{ kHz}}{7.23 \text{ kHz}} = -15.7^\circ$$

If the variable resistor is increased to  $10 \text{k}\Omega$ , the cutoff frequency decreases to 723 Hz and the phase shift increases to:

$$\phi = -2 \arctan \frac{1 \text{ kHz}}{723 \text{ Hz}} = -108^\circ$$

If the variable resistor is increased to  $100 \text{k}\Omega$ , the cutoff frequency decreases to 72.3 Hz and the phase shift increases to:

$$\phi = -2 \arctan \frac{1 \text{ kHz}}{72.3 \text{ Hz}} = -172^\circ$$

In summary, the phase shifter produces an output voltage with the same magnitude as the input voltage, but with a phase angle that can be varied continuously between  $0^\circ$  and  $-180^\circ$ .

## Example 20-2

When we need to vary the amplitude of an out-of-phase signal, we can use a circuit like the one in Fig. 20-10. If  $R_1 = 1.2\text{ k}\Omega$  and  $R_2 = 91\text{ k}\Omega$ , what are the values of the maximum and minimum voltage gain?

**SOLUTION** With the equation given in Fig. 20-10, the maximum voltage gain is:

$$A_v = \frac{-91\text{ k}\Omega}{1.2\text{ k}\Omega} = -75.8$$

The minimum voltage gain is zero.

**PRACTICE PROBLEM 20-2** In Example 20-2, what value should  $R_2$  be changed to for a maximum gain of  $-50$ ?

## Example 20-3

If  $R = 1.5\text{ k}\Omega$  and  $nR = 7.5\text{ k}\Omega$  in Fig. 20-12, what is the maximum positive voltage gain? What is the value of the other fixed resistance?

**SOLUTION** The value of  $n$  is:

$$n = \frac{7.5\text{ k}\Omega}{1.5\text{ k}\Omega} = 5$$

The maximum positive voltage gain is 5. The other fixed resistor has a value of:

$$\frac{nR}{n-1} = \frac{5(1.5\text{ k}\Omega)}{5-1} = 1.875\text{ k}\Omega$$

With a circuit like this, we have to use a precision resistor to get a nonstandard value like  $1.875\text{ k}\Omega$ .

**PRACTICE PROBLEM 20-3** Using Fig. 20-12, if  $R = 1\text{ k}\Omega$ , what is the maximum positive voltage gain and value of the other fixed resistance?

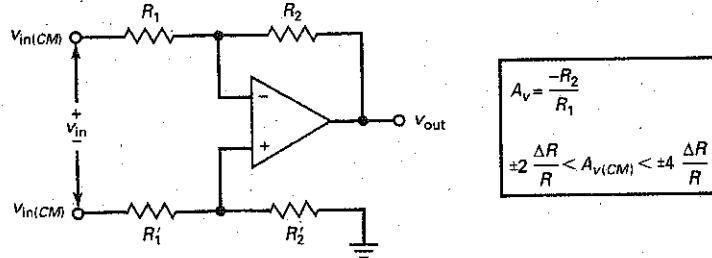
## 20-4 Differential Amplifiers

This section will discuss how to build a differential amplifier using an op amp. One of the most important characteristics of a differential amplifier is its CMRR because the typical input signal is a small differential voltage and a large common-mode voltage.

### Basic Differential Amplifier

Figure 20-14 shows an op amp connected as a differential amplifier. The resistor  $R'_1$  has the same nominal value as  $R_1$  but differs slightly in value because of tolerances.

**Figure 20-14** Differential amplifier.



## GOOD TO KNOW

The basic diff-amp circuits shown in Figs. 20-14 through 20-20 are used very frequently in the biomedical and electromechanical fields of electronics.

For instance, if the resistors are  $1\text{ k}\Omega \pm 1$  percent,  $R_1$  may be as high as  $1010\text{ }\Omega$  and  $R_1'$  may be as low as  $990\text{ }\Omega$ , and vice versa. Similarly,  $R_2$  and  $R_2'$  are nominally equal but may differ slightly because of tolerances.

In Fig. 20-14, the desired input voltage  $v_{in}$  is called the **differential input voltage** to distinguish it from the common-mode input voltage  $v_{in(CM)}$ . A circuit like Fig. 20-14 amplifies the differential input voltage  $v_{in}$  to get an output voltage of  $v_{out}$ . Using the superposition theorem, it can be shown that:

$$v_{out} = A_v v_{in}$$

where

$$A_v = \frac{-R_2}{R_1} \quad (20-4)$$

This voltage gain is called the **differential voltage gain** to distinguish it from the common-mode voltage gain  $A_{v(CM)}$ . By using precision resistors, we can build a differential amplifier with a precise voltage gain.

A differential amplifier is often used in applications in which the differential input signal  $v_{in}$  is a small dc voltage (millivolts) and the common-mode input signal is a large dc voltage (volts). As a result, the CMRR of the circuit becomes a critical parameter. For instance, if the differential input signal is  $7.5\text{ mV}$  and the common-mode signal is  $7.5\text{ V}$ , the differential input signal is  $60\text{ dB}$  less than the common-mode input signal. Unless the circuit has a very high CMRR, the common-mode output signal will be objectionably large.

## CMRR of the Op Amp

In Fig. 20-14, two factors determine the overall CMRR of the circuit. First, there is the CMRR of the op amp itself. For a 741C, the minimum CMRR is  $70\text{ dB}$  at low frequencies. If the differential input signal is  $60\text{ dB}$  less than the common-mode input signal, the differential output signal will be only  $10\text{ dB}$  greater than the common-mode output signal. This means that the desired signal is only  $3.16$  times greater than the undesired signal. Therefore, a 741C would be useless in an application such as this.

The solution is to use a precision op amp like an OP-07A. It has a minimum CMRR of  $110\text{ dB}$ . This will significantly improve the operation. If the differential input signal is  $60\text{ dB}$  less than the common-mode input signal, the differential output signal will be  $50\text{ dB}$  greater than the common-mode output signal. This would be fine if the CMRR of the op amp were the only source of error.

## CMRR of External Resistors

There is a second source of common-mode error: the tolerance of the resistors in Fig. 20-14. When the resistors are perfectly matched:

$$R_1 = R'_1$$

$$R_2 = R'_2$$

In this case, the common-mode input voltage of Fig. 20-14 produces zero voltage across the op-amp input terminals.

On the other hand, when the resistors have a tolerance of  $\pm 1$  percent, the common-mode input voltage of Fig. 20-14 will produce a common-mode output voltage because the mismatch in the resistances produces a differential input voltage to the op amp.

As discussed in Sec. 20-3, the overall voltage gain when the same signal drives both sides of an op amp is given by:

$$A_{v(CM)} = A_{v(inv)} + A_{v(non)} \quad (20-5)$$

In Fig. 20-14, the inverting voltage gain is:

$$A_{v(inv)} = \frac{-R_2}{R_1} \quad (20-6)$$

and the noninverting voltage gain is:

$$A_{v(non)} = \left( \frac{R_2}{R_1} + 1 \right) \left( \frac{R'_2}{R'_1 + R'_2} \right) \quad (20-7)$$

where the second factor is the decrease in the noninverting input signal caused by the voltage divider on the noninverting side.

With Eqs. (20-5) to (20-7), we can derive these useful formulas:

$$A_{v(CM)} = \pm 2 \frac{\Delta R}{R} \quad \text{for } R_1 = R_2 \quad (20-8)$$

$$A_{v(CM)} = \pm 4 \frac{\Delta R}{R} \quad \text{for } R_1 \ll R_2 \quad (20-9)$$

or

$$\pm 2 \frac{\Delta R}{R} < A_{v(CM)} < \pm 4 \frac{\Delta R}{R} \quad (20-10)$$

In these equations,  $\Delta R/R$  is the tolerance of the resistors converted to the decimal equivalent.

For instance, if the resistors have a tolerance of  $\pm 1$  percent, Eq. (20-8) gives:

$$A_{v(CM)} = \pm 2(1\%) = \pm 2(0.01) = \pm 0.02$$

Equation (20-9) gives:

$$A_{v(CM)} = \pm 4(1\%) = \pm 4(0.01) = \pm 0.04$$

Inequality (20-10) gives:

$$\pm 0.02 < A_{v(CM)} < \pm 0.04$$

This says that the common-mode voltage gain is between  $\pm 0.02$  and  $\pm 0.04$ . When necessary, we can calculate the exact value of  $A_{v(CM)}$  with Eqs. (20-5) to (20-7).

## Calculating CMRR

Here is an example of how to calculate the CMRR: In a circuit like the one in Fig. 20-14, resistors with a tolerance of  $\pm 0.1$  percent are commonly used. When  $R_1 = R_2$ , Eq. (20-4) gives a differential voltage gain of:

$$A_v = -1$$

and Eq. (20-8) gives a common-mode voltage gain of:

$$A_{v(CM)} = \pm 2(0.1\%) = \pm 2(0.001) = \pm 0.002$$

The CMRR has a magnitude of:

$$\text{CMRR} = \frac{|A_v|}{|A_{v(CM)}|} = \frac{1}{0.002} = 500$$

which is equivalent to 54 dB. (Note: The vertical bars around  $A_v$  and  $A_{v(CM)}$  indicate absolute values.)

## Buffered Inputs

The source resistances driving the differential amplifier of Fig. 20-14 effectively become part of  $R_1$  and  $R'_1$ , which changes the voltage gain and may degrade the CMRR. This is a very serious disadvantage. The solution is to increase the input impedance of the circuit.

Figure 20-15 shows one way to do it. The first stage (the preamp) consists of two voltage followers that buffer (isolate) the inputs, as shown in Fig. 20-15. This can increase the input impedance to well over 100 MΩ. The voltage gain of the first stage is unity for both the differential and the common-mode input signal. Therefore, the second stage (the differential amplifier) still has to provide all the CMRR for the circuit.

## Wheatstone Bridge

As previously mentioned, the differential input signal is often a small dc voltage. The reason it is small is because it is usually the output of a Wheatstone bridge like that in Fig. 20-16a. A Wheatstone bridge is balanced when the ratio of resistances on the left side equals the ratio of resistances on the right side:

$$\frac{R_1}{R_2} = \frac{R_3}{R_4} \quad (20-11)$$

When this condition is satisfied, the voltage across  $R_2$  equals the voltage across  $R_4$  and the output voltage of the bridge is zero.

Figure 20-15 Differential input with buffered inputs.

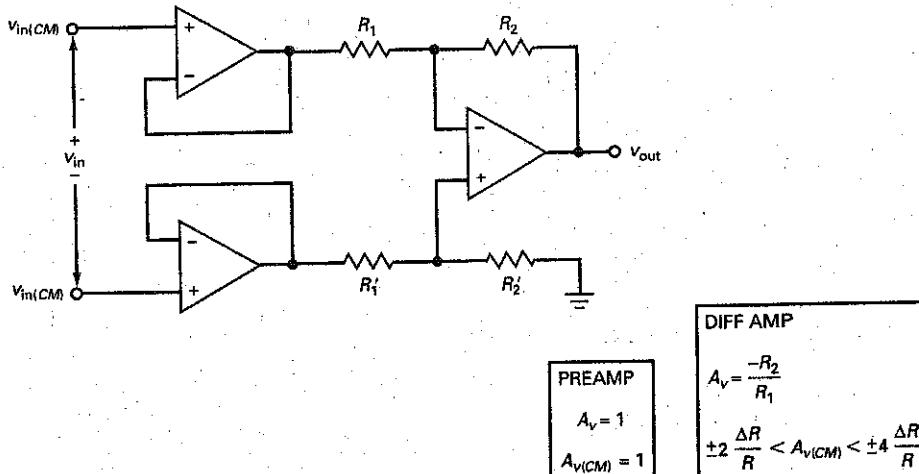
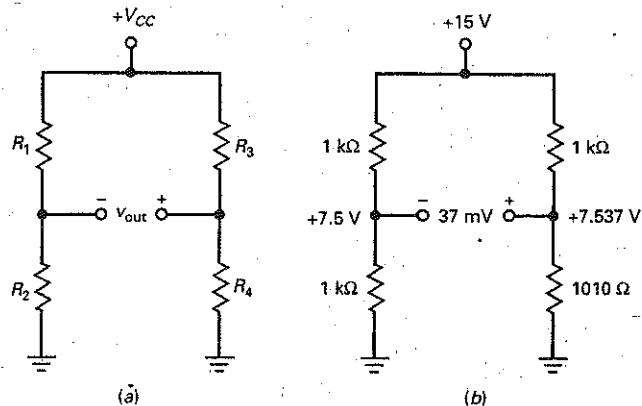


Figure 20-16 (a) Wheatstone bridge; (b) slightly unbalanced bridge.



The Wheatstone bridge can detect small changes in one of the resistors. For instance, suppose we have a bridge with three resistors of  $1\text{ k}\Omega$  and a fourth resistor of  $1010\text{ }\Omega$ , as shown in Fig. 20-16b. The voltage across  $R_2$  is:

$$v_2 = \frac{1\text{ k}\Omega}{2\text{ k}\Omega} (15\text{ V}) = 7.5\text{ V}$$

and the voltage across  $R_4$  is approximately:

$$v_4 = \frac{1010\text{ }\Omega}{2010\text{ }\Omega} (15\text{ V}) = 7.537\text{ V}$$

The output voltage of the bridge is approximately:

$$v_{\text{out}} = v_4 - v_2 = 7.537\text{ V} - 7.5\text{ V} = 37\text{ mV}$$

## Transducers

Resistance  $R_4$  may be an **input transducer**, a device that converts a nonelectrical quantity into an electrical quantity. For instance, a photoresistor converts a change in light intensity into a change in resistance and a **thermistor** converts a change in temperature into a change in resistance.

There is also the **output transducer**, a device that converts an electrical quantity into a nonelectrical quantity. For instance, an LED converts current into light and a loudspeaker converts ac voltage into sound waves.

A wide variety of transducers are commercially available for quantities such as temperature, sound, light, humidity, velocity, acceleration, force, radioactivity, strain, and pressure, to mention a few. These transducers can be used with a Wheatstone bridge to measure nonelectrical quantities. Because the output of a Wheatstone bridge is a small dc voltage with a large common-mode voltage, we need to use dc amplifiers that have very high CMRRs.

## A Typical Application

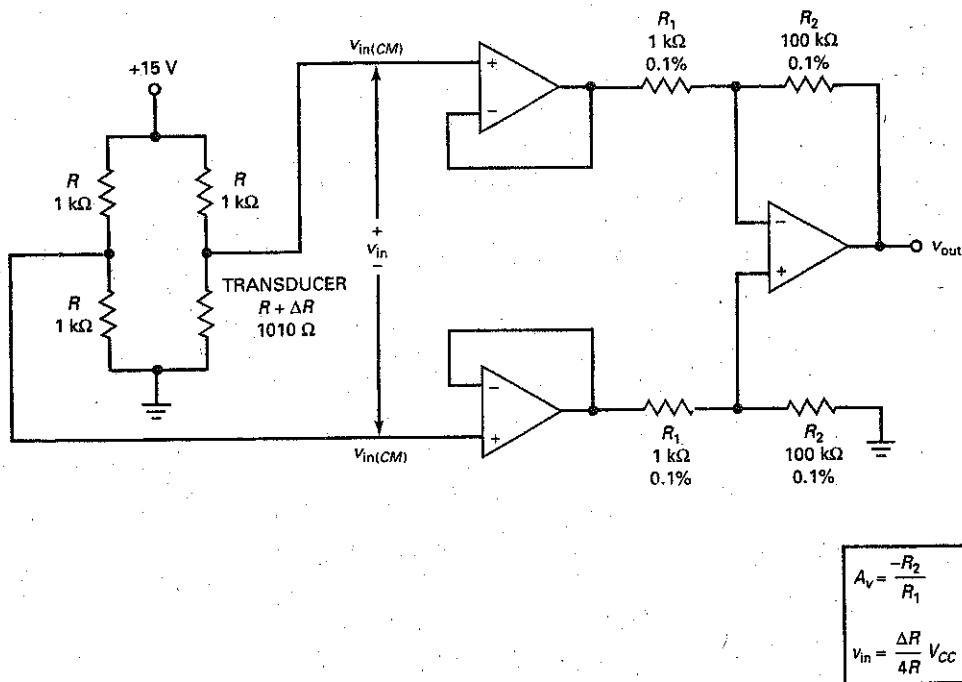
Figure 20-17 shows a typical application. Three of the bridge resistors have a value of:

$$R = 1\text{ k}\Omega$$

The transducer has a resistance of:

$$R + \Delta R = 1010\text{ }\Omega$$

Figure 20-17 Bridge with transducer drives instrumentation amplifier.



The common-mode signal is:

$$v_{in(CM)} = 0.5V_{CC} = 0.5(15\text{ V}) = 7.5\text{ V}$$

This is the voltage across each of the lower bridge resistors when  $\Delta R = 0$ .

When a bridge transducer is acted on by an outside quantity such as light, temperature, or pressure, its resistance will change. Figure 20-17 shows a transducer resistance of  $1010\Omega$ , which implies that  $\Delta R = 10\Omega$ . It is possible to derive this equation for the input voltage in Fig. 20-17:

$$v_{in} = \frac{\Delta R}{4R + 2\Delta R} V_{CC} \quad (20-12)$$

In a typical application,  $2\Delta R \ll 4R$  and the equation simplifies to:

$$v_{in} \cong \frac{\Delta R}{4R} V_{CC} \quad (20-13)$$

For the values shown in Fig. 20-17:

$$v_{in} \cong \frac{10\Omega}{4\text{ k}\Omega} (15\text{ V}) = 37.5\text{ mV}$$

Since the differential amplifier has a voltage gain of  $-100$ , the differential output voltage is:

$$v_{out} = -100(37.5\text{ mV}) = -3.75\text{ V}$$

As far as the common-mode signal is concerned, Eq. (20-9) gives:

$$A_{v(CM)} = \pm 4(0.1\%) = \pm 4(0.001) = \pm 0.004$$

for the tolerance of  $\pm 0.1$  percent shown in Fig. 20-17. Therefore, the common-mode output voltage is:

$$V_{out(CM)} = \pm 0.004(7.5 \text{ V}) = \pm 0.03 \text{ V}$$

The magnitude of CMRR is:

$$\text{CMRR} = \frac{100}{0.004} = 25000$$

which is equivalent to 88 dB.

That gives you the basic idea of how a differential amplifier is used with a Wheatstone bridge. A circuit like Fig. 20-17 is adequate for some applications but can be improved, as will be discussed in the following section.

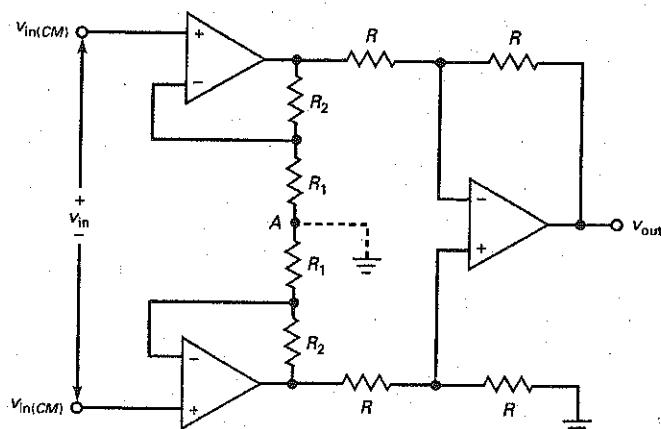
## 20-5 Instrumentation Amplifiers

This section discusses the **instrumentation amplifier**, a differential amplifier optimized for its dc performance. An instrumentation amplifier has a large voltage gain, a high CMRR, low input offsets, low temperature drift, and high input impedance.

### Basic Instrumentation Amplifier

Figure 20-18 shows the classic design used for most instrumentation amplifiers. The output op amp is a differential amplifier with the voltage gain of unity. The resistors used in this output stage are usually matched to within  $\pm 0.1$  percent or better. This means that the CMRR of the output stage is at least 54 dB.

**Figure 20-18** Standard three op-amp instrumentation amplifier.



<b>PREAMP</b>
$A_v = \frac{R_2}{R_1} + 1$
$A_{v(CM)} = 1$

<b>DIFF AMP</b>
$A_v = -1$
$A_{v(CM)} = \pm 2 \frac{\Delta R}{R}$

Precision resistors are commercially available from less than  $1\ \Omega$  to more than  $10\ M\Omega$ , with tolerances of  $\pm 0.01$  to  $\pm 1$  percent. If we use matched resistors that are within  $\pm 0.01$  percent of each other, the CMRR of the output stage can be as high as 74 dB. Also, temperature drift of precision resistors can be as low as  $1\ \mu\text{V}/^\circ\text{C}$ .

The first stage consists of two input op amps that act like a preamplifier. The design of the first stage is extremely clever. What makes it so ingenious is the action of point A, the junction between the two  $R_1$  resistors. Point A acts like a virtual ground for a differential input signal and like a floating point for the common-mode signal. Because of this action, the differential signal is amplified but the common-mode signal is not.

### Point A

The key to understanding how the first stage works is to understand what point A does. With the superposition theorem, we can calculate the effect of each input with the other zeroed. For instance, assume that the differential input signal is zero. Then only the common-mode signal is active. Since the common-mode signal applies the same positive voltage to each noninverting input, equal voltages appear at the op-amp outputs. Because of this, the same voltage appears everywhere along the branch that contains  $R_1$  and  $R_2$ . Therefore, point A is floating and each input op amp acts like a voltage follower. As a result, the first stage has a common-mode gain of:

$$A_{v(CM)} = 1$$

Unlike the second stage, where the  $R$  resistors have to be closely matched to minimize the common-mode gain, in the first stage the tolerance of the resistors has no effect on the common-mode gain. This is because the entire branch containing these resistors is floating at a voltage of  $v_{in(CM)}$  above ground. So, the resistor values do not matter. This is another advantage of the three op-amp design of Fig. 20-18.

The second step in applying the superposition theorem is to reduce the common-mode input to zero and to calculate the effect of the differential input signal. Since the differential input signal drives the noninverting inputs with equal and opposite input voltages, one op-amp output will be positive and the other will be negative. With equal and opposite voltages across the branch containing the  $R_1$  and  $R_2$  resistors, point A will have a voltage of zero with respect to ground.

In other words, point A is a virtual ground for the differential signal. For this reason, each input op amp is a noninverting amplifier and the first stage has a differential voltage gain of:

$$A_v = \frac{R_2}{R_1} + 1 \quad (20-14)$$

Since the second stage has a gain of unity, the differential voltage gain of the instrumentation amplifier is given by Eq. (20-14).

Because the first stage has a common-mode gain of unity, the overall common-mode gain equals the common-mode gain of the second stage:

$$A_{v(CM)} = \pm 2 \frac{\Delta R}{R} \quad (20-15)$$

To have high CMRR and low offsets, precision op amps must be used when building the instrumentation amplifier of Fig. 20-18. A typical op amp used in the three op-amp approach of Fig. 20-18 is the OP-07A. It has the following worst-case parameters: Input offset voltage is  $0.025\ \text{mV}$ , input bias current is  $2\ \text{nA}$ , input offset current is  $1\ \text{nA}$ ,  $A_{OL}$  is  $110\ \text{dB}$ , CMRR is  $110\ \text{dB}$ , and temperature drift is  $0.6\ \mu\text{V}/^\circ\text{C}$ .

A final point about Fig. 20-18: Since point A is a virtual ground rather than a mechanical ground, the  $R_1$  resistors in the first stage do not have to be separate resistors. We can use a single resistor  $R_G$  that equals  $2R_1$  without changing the operation of the first stage. The only difference is that the differential voltage gain is written as:

$$A_v = \frac{2R_2}{R_G} + 1 \quad (20-16)$$

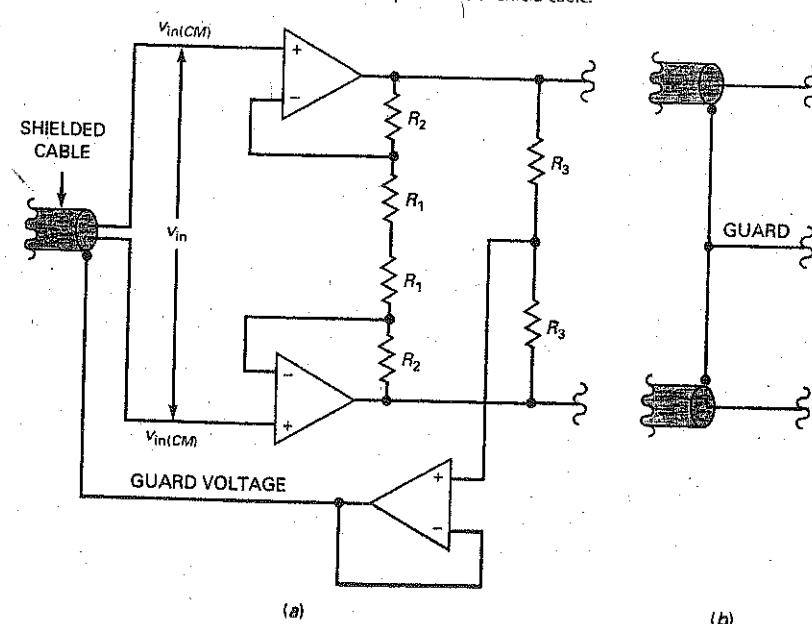
The factor of 2 appears because  $R_G = 2R_1$ .

## Guard Driving

Because the differential signal out of a bridge is small, a shielded cable is often used to isolate the signal-carrying wires from electromagnetic interference. But this creates a problem. Any leakage current between the inner wires and the shield will add to the low input bias and offset currents. Besides the leakage current, the shielded cable adds capacitance to the circuit, which slows down the response of the circuit to a change in transducer resistance. To minimize the effects of leakage current and cable capacitance, the shield should be bootstrapped to the common-mode potential. This technique is known as **guard driving**.

Figure 20-19a shows one way to bootstrap the shield to the common-mode voltage. A new branch containing the resistors labeled  $R_3$  is added to the output of the first stage. This voltage divider picks off the common-mode voltage and feeds it to a voltage follower. The guard voltage is fed back to the shield, as shown. Sometimes, separate cables are used for each input. In this case, the guard voltage is connected to both shields, as shown in Fig. 20-19b.

**Figure 20-19** Guard driving to reduce leakage currents and capacitance of shield cable.



## Integrated Instrumentation Amplifiers

The classic design of Fig. 20-18 can be integrated on a chip with all the components shown in Fig. 20-18, except  $R_G$ . This external resistance is used to control the voltage gain of the instrumentation amplifier. For instance, the AD620 is a monolithic instrumentation amplifier. The data sheet gives this equation for its voltage gain:

$$A_v = \frac{49.4 \text{ k}\Omega}{R_G} + 1 \quad (20-17)$$

The quantity 49.4 k $\Omega$  is the sum of the two  $R_2$  resistors. The IC manufacturer uses laser trimming to get a precise value of 49.4 k $\Omega$ . The word *trim* refers to a fine adjustment rather than a coarse adjustment. Laser trimming means burning off resistor areas on a semiconductor chip with a laser to get an extremely precise value of resistance.

Figure 20-20a shows the AD620 with an  $R_G$  of 499  $\Omega$ . This is a precision resistor with a tolerance of  $\pm 0.1$  percent. The voltage gain is:

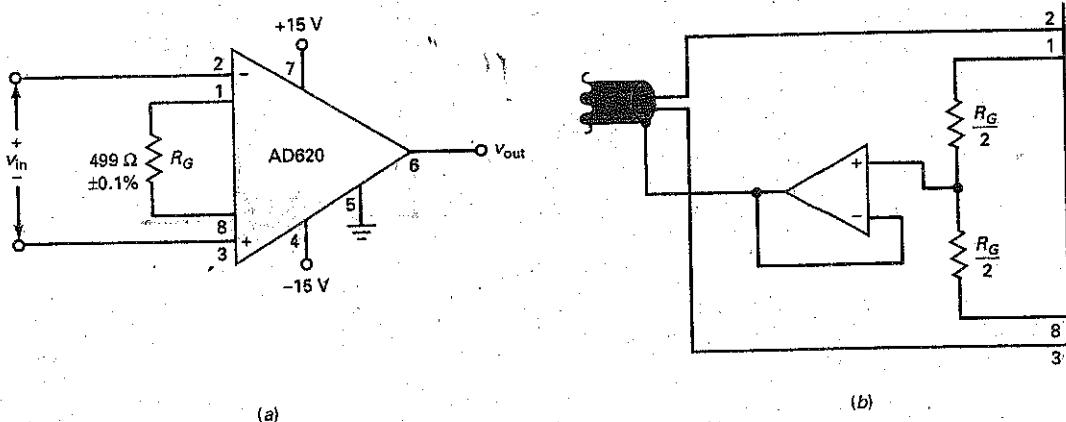
$$A_v = \frac{49.4 \text{ k}\Omega}{499} + 1 = 100$$

The *pinout* (pin numbers) of the AD620 is similar to that of a 741C since pins 2 and 3 are for the input signals, pins 4 and 7 are for the supply voltages, and pin 6 is the output. Pin 5 is shown grounded, the usual case for the AD620. But this pin does not have to be grounded. If necessary for interfacing with another circuit, we can offset the output signal by applying a dc voltage to pin 5.

If guard driving is used, the circuit can be modified as shown in Fig. 20-20b. The common-mode voltage drives a voltage follower, whose output is connected to the shield of the cable. A similar modification is used if separate cables are used for the inputs.

In summary, monolithic instrumentation amplifiers typically have a voltage gain between 1 and 1000 that can be set with one external resistor, a CMRR greater than 100 dB, an input impedance greater than 100 M $\Omega$ , an input offset voltage less than 0.1 mV, a drift of less than 0.5  $\mu\text{V}/^\circ\text{C}$ , and other outstanding parameters.

Figure 20-20 (a) A monolithic instrumentation amplifier; (b) guard driving with an AD620.



## Example 20-4

In Fig. 20-18,  $R_1 = 1\text{ k}\Omega$ ,  $R_2 = 100\text{ k}\Omega$ , and  $R = 10\text{ k}\Omega$ . What is the differential voltage gain of the instrumentation amplifier? What is the common-mode voltage gain if the resistor tolerances in the second stage are  $\pm 0.01$  percent? If  $v_{in} = 10\text{ mV}$  and  $v_{in(CM)} = 10\text{ V}$ , what are the values of the differential and common-mode output signals?

**SOLUTION** With the equations given in Fig. 20-18, the voltage gain of the preamp is:

$$A_v = \frac{100\text{ k}\Omega}{1\text{ k}\Omega} + 1 = 101$$

Since the voltage gain of the second stage is  $-1$ , the voltage gain of the instrumentation amplifier is  $-101$ .

The common-mode voltage gain of the second stage is:

$$A_{v(CM)} = \pm 2(0.01\%) = \pm 2(0.0001) = \pm 0.0002$$

Since the first stage has a common-mode voltage gain of  $1$ , the common-mode voltage gain of the instrumentation amplifier is  $\pm 0.0002$ .

A differential input signal of  $10\text{ mV}$  will produce an output signal of:

$$v_{out} = -101(10\text{ mV}) = -1.01\text{ V}$$

A common-mode signal of  $10\text{ V}$  will produce an output signal of:

$$v_{out(CM)} = \pm 0.0002(10\text{ V}) = \pm 2\text{ mV}$$

Even though the common-mode input signal is 1000 times greater than the differential input, the CMRR of the instrumentation amplifier produces a common-mode output signal that is approximately 500 times smaller than the differential output signal.

**PRACTICE PROBLEM 20-4** Repeat Example 20-4 with  $R_2 = 50\text{ }\Omega$  and  $\pm 0.1\%$  second stage resistor tolerance.

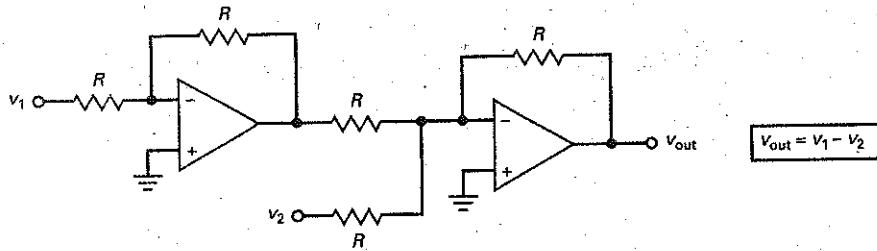
## 20-6 Summing Amplifier Circuits

We discussed the basic summing amplifier in Chap. 18. Now, let us look at some variations of this circuit.

### The Subtractor

Figure 20-21 shows a circuit that subtracts two input voltages to produce an output voltage equal to the difference of  $v_1$  and  $v_2$ . Here is how it works: Input  $v_1$  drives an inverter with a voltage gain of unity. The output of the first stage is  $-v_1$ . This voltage is one of the inputs to the second-stage summing circuit. The other input is  $v_2$ . Since the gain of each channel is unity, the final output voltage equals  $v_1$  minus  $v_2$ .

Figure 20-21 Subtractor.



### Summing on Both Inputs

Sometimes you may see a circuit like Fig. 20-22. It is nothing more than a summing circuit that has inverting and noninverting inputs. The inverting side of the amplifier has two input channels, and the noninverting side has two input channels. The total gain is the superposition of the channel gains.

The gain of each inverting channel is the ratio of the feedback resistor  $R_f$  to input channel resistance, either  $R_1$  or  $R_2$ . The gain of each noninverting channel is:

$$\frac{R_f}{R_1 \parallel R_2} + 1$$

reduced by the voltage-divider factor of the channel, either:

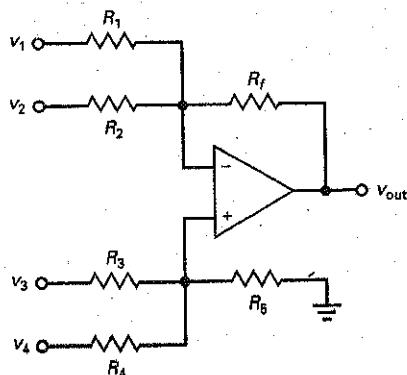
$$\frac{R_4 \parallel R_5}{R_3 + R_4 \parallel R_5}$$

or

$$\frac{R_3 \parallel R_5}{R_4 + R_3 \parallel R_5}$$

Figure 20-22 gives the equations for the gain of each channel. After getting each channel gain, we can calculate total output voltage.

Figure 20-22 Summing amplifier using both sides of op amp.



$$V_{\text{out}} = A_{v1}V_1 + A_{v2}V_2 + A_{v3}V_3 + A_{v4}V_4$$

$$A_{v1} = \frac{-R_f}{R_1}$$

$$A_{v2} = \frac{-R_f}{R_2}$$

$$A_{v3} = \left( \frac{R_f}{R_1 \parallel R_2} + 1 \right) \left( \frac{R_4 \parallel R_5}{R_3 + R_4 \parallel R_5} \right)$$

$$A_{v4} = \left( \frac{R_f}{R_1 \parallel R_2} + 1 \right) \left( \frac{R_3 \parallel R_5}{R_4 + R_3 \parallel R_5} \right)$$

## Example 20-5

**III** **Solutions**

In Fig. 20-22,  $R_1 = 1 \text{ k}\Omega$ ,  $R_2 = 2 \text{ k}\Omega$ ,  $R_3 = 3 \text{ k}\Omega$ ,  $R_4 = 4 \text{ k}\Omega$ ,  $R_5 = 5 \text{ k}\Omega$ , and  $R_f = 6 \text{ k}\Omega$ . What is the voltage gain of each channel?

**SOLUTION** With the equations given in Fig. 20-22, the voltage gains are:

$$A_{v1} = \frac{-6 \text{ k}\Omega}{1 \text{ k}\Omega} = -6$$

$$A_{v2} = \frac{-6 \text{ k}\Omega}{2 \text{ k}\Omega} = -3$$

$$A_{v3} = \left( \frac{6 \text{ k}\Omega}{1 \text{ k}\Omega \parallel 2 \text{ k}\Omega} + 1 \right) \frac{4 \text{ k}\Omega \parallel 5 \text{ k}\Omega}{3 \text{ k}\Omega + 4 \text{ k}\Omega \parallel 5 \text{ k}\Omega} = 4.26$$

$$A_{v4} = \left( \frac{6 \text{ k}\Omega}{1 \text{ k}\Omega \parallel 2 \text{ k}\Omega} + 1 \right) \frac{3 \text{ k}\Omega \parallel 5 \text{ k}\Omega}{4 \text{ k}\Omega + 3 \text{ k}\Omega \parallel 5 \text{ k}\Omega} = 3.19$$

**PRACTICE PROBLEM 20-5** Repeat Example 20-5 using  $1 \text{ k}\Omega$  for  $R_f$ .

## The Averager

Figure 20-23 is an **averager**, a circuit whose output equals the average of the input voltages. Each channel has a voltage gain of:

$$A_v = \frac{R}{3R} = \frac{1}{3}$$

When all amplified outputs are added, we get an output that is the average of all input voltages.

The circuit shown in Fig. 20-23 has three inputs. Any number of inputs can be used, as long as each channel input resistance is changed to  $nR$ , where  $n$  is the number of channels.

## D/A Converter

In digital electronics, a **digital-to-analog (D/A) converter** takes a binary represented value and converts it into a voltage or current. This voltage or current will be proportional to the input binary value. Two methods of D/A conversion are

Figure 20-23 Averaging circuit.

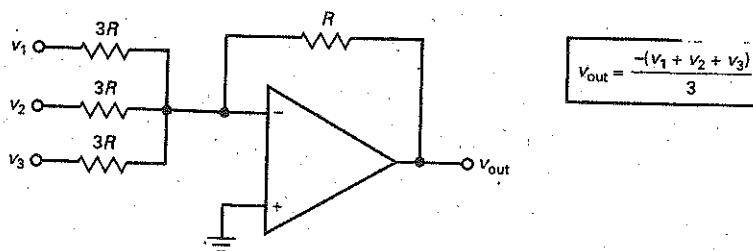
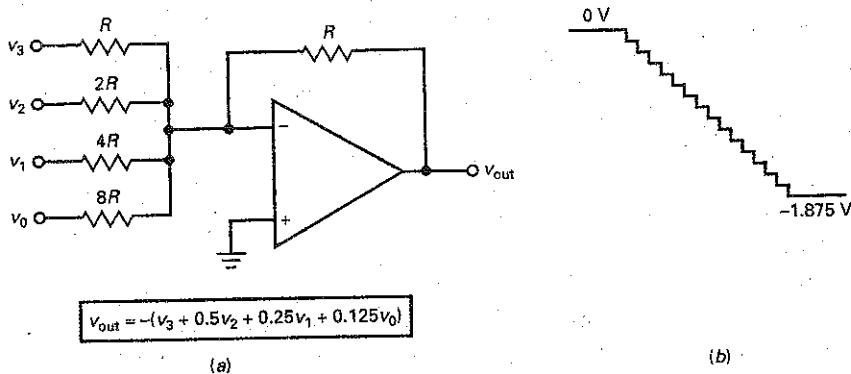


Figure 20-24 Binary-weighted D/A converter changes digital input to analog voltage.



often used, the binary-weighted D/A converter and the R/2R ladder D/A converter.

The binary-weighted D/A converter is shown in Fig. 20-24. This circuit produces an output voltage equal to the weighted sum of the inputs. The *weight* is the same as the gain of the channel. For instance, in Fig. 20-24a the channel gains are:

$$\begin{aligned}A_{v3} &= -1 \\A_{v2} &= -0.5 \\A_{v1} &= -0.25 \\A_{v0} &= -0.125\end{aligned}$$

The input voltages are digital or two-state, which means that they have a value of either 1 or 0. With 4 inputs, there are 16 possible input combinations of  $v_3v_2v_1v_0$ : 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, and 1111.

When all inputs are zero (0000), the output is:

$$v_{\text{out}} = 0$$

When  $v_3v_2v_1v_0$  is 0001, the output is:

$$v_{\text{out}} = -(0.125) = -0.125$$

When  $v_3v_2v_1v_0$  is 0010, the output is:

$$v_{\text{out}} = -(0.25) = -0.25$$

and so on. When the inputs are all 1s (1111), the output is maximum and equals:

$$v_{\text{out}} = -(1 + 0.5 + 0.25 + 0.125) = -1.875$$

If the D/A converter of Fig. 20-24 is driven by a circuit that produces the 0000 to 1111 sequence of numbers given earlier, it will produce these output voltages: 0, -0.125, -0.25, -0.375, -0.5, -0.625, -0.75, -0.875, -1, -1.125, -1.25, -1.375, -1.5, -1.625, -1.75, and -1.875. When viewed on an oscilloscope, the output voltage of the D/A converter will look like the negative-going staircase shown in Fig. 20-24b.

The staircase voltage demonstrates that the D/A converter does not produce a continuous range of output values. Therefore, strictly speaking its output is not truly analog. Low-pass filter circuits can be connected to the output to provide a smoother transition between output steps.

A 4-input D/A converter has 16 possible outputs, an 8-input A/D converter has 256 possible outputs, and a 16-input D/A converter has 65,536 possible outputs. This means that the negative-going staircase voltage of Fig. 20-24b can have 256 steps with an 8-input converter and 65,536 steps with a 16-input converter. A negative-going staircase voltage like this is used in a digital multimeter along with other circuits to measure the voltage numerically.

The binary-weighted D/A converter can be used in applications where the number of inputs are limited and where high precision is not required. When a higher number of inputs is used, a higher number of different resistor values is required. The accuracy and stability of the D/A converter depends on the absolute accuracy of the resistors and their ability to track each other with temperature variations. Because the input resistors all have different values, identical tracking characteristics is difficult to obtain. Loading problems can also exist with this type of D/A converter because each input has a different input impedance value.

The R/2R ladder D/A converter, shown in Fig. 20-25, overcomes the limitations of the binary-weighted D/A converter and is the method most often used in integrated-circuit D/A converters. Because only two resistor values are required, this method lends itself to ICs with 8 bit or higher binary inputs and provides a higher degree of accuracy. For simplicity, Fig. 20-25 is shown as a 4-bit D/A converter. The switches,  $D_0 - D_3$ , would normally be some type of active switch. The switches connect the four inputs to either ground (logic 0) or  $+V_{ref}$  (logic 1). The ladder network converts the possible binary input values from 0000 through 1111 to one of 16 unique output voltage levels. In the D/A converter shown in Fig. 20-25,  $D_0$  is considered to be the least significant input bit (LSB) while  $D_3$  is the most significant bit (MSB).

To determine the D/A converter's output voltage, you must first change the binary input value to its decimal equivalent value, BIN. This can be done by:

$$BIN = (D_0 \times 2^0) + (D_1 \times 2^1) + (D_2 \times 2^2) + (D_3 \times 2^3) \quad (20-18)$$

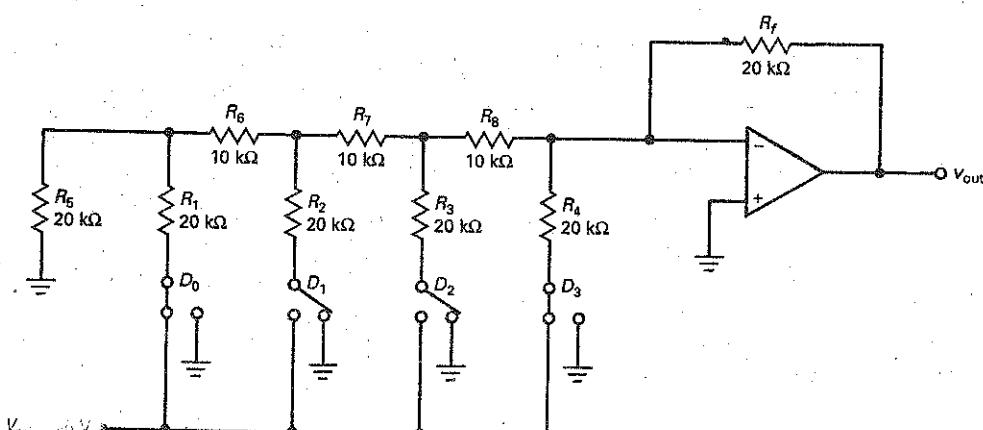
Then, the output voltage will be found by:

$$V_{out} = -\left(\frac{BIN}{2^N} \times 2V_{ref}\right) \quad (20-19)$$

where  $N$  equals the number of inputs.

For more detail of this circuit's operation, the D/A converter can be Thevenized. This analysis can be found in Appendix D.

Fig. 20-25 R/2R ladder D/A converter.



## Example 20-6

In Fig. 20-25,  $D_0 = 1$ ,  $D_1 = 0$ ,  $D_2 = 0$ , and  $D_3 = 1$ . Using a  $V_{ref}$  value of +5 V, determine the decimal equivalent of the binary input (BIN) and the output voltage of the converter.

**SOLUTION** Using Eq. 20-18, the decimal equivalent can be found by:

$$\text{BIN} = (1 \times 2^0) + (0 \times 2^1) + (0 \times 2^2) + (1 \times 2^3) = 9$$

The output voltage of the converter is found by using Eq. 20-19 as:

$$V_{\text{out}} = -\left(\frac{9}{2^4}\right) \times 2(5 \text{ V})$$

$$V_{\text{out}} = -\left(\frac{9}{16}\right)(10 \text{ V}) = -5.625 \text{ V}$$

**PRACTICE PROBLEM 20-6** Using Fig. 20-25, what is the largest and smallest output voltage possible with at least one input being a logic 1.

## 20-7 Current Boosters

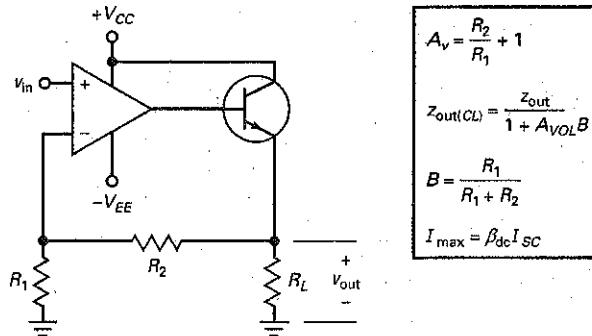
The short-circuit output current of an op amp is typically 25 mA or less. One way to get more output current is to use a power op amp like the LM675 or LM12. These op amps have short-circuit output currents of 3 and 10 A. Another way to get more short-circuit output current is to use a **current booster**, a power transistor or other device that has a current gain and a higher current rating than the op amp.

### Unidirectional Booster

Figure 20-26 shows one way to increase the maximum load current. The output of an op amp drives an emitter follower. The closed-loop voltage gain is:

$$A_v = \frac{R_2}{R_1} + 1 \quad (20-20)$$

**Figure 20-26** Unidirectional current booster increases short-circuit output current.



In this circuit, the op amp no longer has to supply the load current. Instead, it only has to supply base current to the emitter follower. Because of the current gain of the transistor, the maximum load current is increased to:

$$I_{\max} = \beta_{dc} I_{SC} \quad (20-21)$$

where  $I_{SC}$  is the short-circuit output current of the op amp. This means that an op amp like a 741C can have a maximum output current of 25 mA increased by a factor of  $\beta_{dc}$ . For instance, a BU806 is an *npn* power transistor with  $\beta_{dc} = 100$ . If it is used with a 741C, the short-circuit output current increases to:

$$I_{\max} = 100(25 \text{ mA}) = 2.5 \text{ A}$$

The circuit can drive low-impedance loads because the negative feedback reduces the output impedance of the emitter follower by a factor of  $1 + A_{VOL}B$ . Since the emitter follower already has a low output impedance, the closed-loop output impedance will be very small.

### Bidirectional Current

The disadvantage of the current booster shown in Fig. 20-26 is its *unidirectional load current*. Figure 20-27 shows one way to get a *bidirectional load current*. An inverting amplifier drives a class B push-pull emitter follower. In this circuit, the closed-loop voltage gain is:

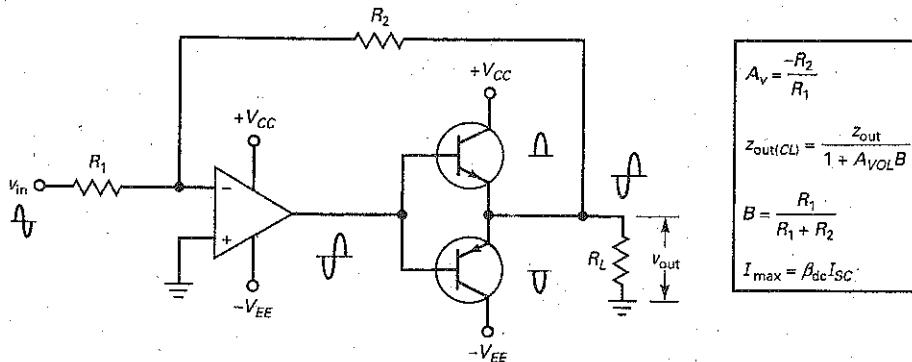
$$A_V = \frac{-R_2}{R_1} \quad (20-22)$$

When the input voltage is positive, the lower transistor is conducting and the load voltage is negative. When the input voltage is negative, the upper transistor is conducting and the output voltage is positive. In either case, the maximum output current is increased by the current gain of the conducting transistor. Since the class B push-pull emitter follower is inside the feedback loop, the closed-loop output impedance is very small.

### Rail-to-Rail Op Amps

Current boosters are sometimes used in the final stage of an op amp. For instance, the MC33206 is a *rail-to-rail op amp* that has a current-boosted output of 80 mA. *Rail-to-rail* refers to the supply lines of an op amp because they look like rails on a schematic diagram. *Rail-to-rail operation* means that the input and output voltages can swing all the way to the positive or negative supply voltages.

**Figure 20-27** Bidirectional current booster.



For instance, the 741C does not have a rail-to-rail output because the output is always 1 to 2 V less than either supply voltage. On the other hand, the MC33206 does have a rail-to-rail output because its output voltage can swing to within 50 mV of either supply voltage, close enough to qualify as rail-to-rail. Rail-to-rail op amps allow a designer to make full use of the available supply voltage range.

## Example 20-7

In Fig. 20-27,  $R_1 = 1 \text{ k}\Omega$ , and  $R_2 = 51 \text{ k}\Omega$ . If a 741C is used for the op amp, what is the voltage gain of the circuit? What is the closed-loop output impedance? What is the shorted-load current of the circuit if each transistor has a current gain of 125?

**SOLUTION** With the equations given in Fig. 20-26, the voltage gain is:

$$A_v = \frac{-51 \text{ k}\Omega}{1 \text{ k}\Omega} = -51$$

The feedback fraction is:

$$B = \frac{1 \text{ k}\Omega}{1 \text{ k}\Omega + 51 \text{ k}\Omega} = 0.0192$$

Since the 741C has a typical voltage gain of 100,000 and an open-loop output impedance of  $75 \Omega$ , the closed-loop output impedance is:

$$z_{\text{out(CL)}} = \frac{75 \Omega}{1 + (100,000)(0.0192)} = 0.039 \Omega$$

Since the 741C has a shorted-load current of 25 mA, the boosted value of the shorted-load current is:

$$I_{\text{max}} = 125(25 \text{ mA}) = 3.13 \text{ A}$$

**PRACTICE PROBLEM 20-7** Using Fig. 20-27, change  $R_2$  to  $27 \text{ k}\Omega$ . Determine the new voltage gain,  $z_{\text{out(CL)}}$  and  $I_{\text{max}}$ , when each transistor has a current gain of 100.

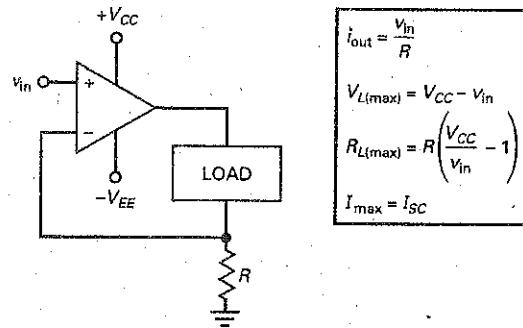
## 20-8 Voltage-Controlled Current Sources

This section discusses circuits that allow an input voltage to control an output current. The load may be floating or grounded. All the circuits are variations of the VCIS prototype discussed in Chap. 19, which means that they are voltage-controlled current sources also known as voltage-to-current converters.

### Floating Load

Figure 20-28 shows the VCIS prototype. The load may be a resistor, a relay, or a motor. Because of the virtual short between the input terminals, the inverting

Figure 20-28 Unidirectional VCIS with floating load.



input is bootstrapped to within microvolts of the noninverting input. Since voltage  $v_{\text{in}}$  appears across  $R$ , the load current is:

$$i_{\text{out}} = \frac{v_{\text{in}}}{R} \quad (20-23)$$

Since the load resistance does not appear in this equation, the current is independent of the load resistance. Stated another way, the load appears to be driven by a very stiff current source. As an example, if  $v_{\text{in}}$  is 1 V and  $R$  is  $1 \text{ k}\Omega$ ,  $i_{\text{out}}$  is 1 mA.

If the load resistance is too large in Fig. 20-28, the op amp goes into saturation and the circuit no longer acts like a stiff current source. If a rail-to-rail op amp is used, the output can swing all the way to  $+V_{CC}$ . Therefore, the maximum load voltage is:

$$V_{L(\text{max})} = V_{CC} - v_{\text{in}} \quad (20-24)$$

For example, if  $V_{CC}$  is 15 V and  $v_{\text{in}}$  is 1 V,  $V_{L(\text{max})}$  is 14 V. If the op amp does not have a rail-to-rail output, we can subtract 1 to 2 V from  $V_{L(\text{max})}$ .

Since the load current equals  $v_{\text{in}}/R$ , we can derive this equation for the maximum load resistance that can be used without saturating the op amp:

$$R_{L(\text{max})} = R \left( \frac{V_{CC}}{v_{\text{in}}} - 1 \right) \quad (20-25)$$

As an example, if  $R$  is  $1 \text{ k}\Omega$ ,  $V_{CC}$  is 15 V, and  $v_{\text{in}}$  is 1 V, then  $R_{L(\text{max})} = 14 \text{ k}\Omega$ .

Another limitation on a voltage-controlled current source is the short-circuit output current of the op amp. For instance, a 741C has a short-circuit output current of 25 mA. Short-circuit output currents for various op amps were discussed in Chap. 18 and listed in Table 18-2. As an equation, the short-circuit current out of the controlled current source in Fig. 20-28 is:

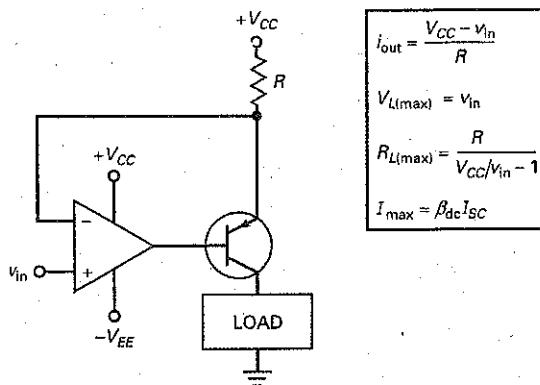
$$I_{\text{max}} = I_{SC} \quad (20-26)$$

where  $I_{SC}$  is the short-circuit output current of the op amp.

## Grounded Load

If a floating load is all right and the short-circuit current is adequate, a circuit like Fig. 20-28 works well. But if the load needs to be grounded or more short-circuit current is needed, we can modify the basic circuit as shown in Fig. 20-29. Since the collector and emitter currents of the transistor are almost equal, the current through  $R$  is approximately equal to the load current. Because of the virtual short

Figure 20-29 Unidirectional VCIS with single-ended load.



between the op-amp inputs, the inverting input voltage approximately equals  $v_{in}$ . Therefore, the voltage across  $R$  equals  $V_{CC}$  minus  $v_{in}$  and the current through  $R$  is given by:

$$i_{out} = \frac{V_{CC} - v_{in}}{R} \quad (20-27)$$

Figure 20-29 shows the equations for maximum load voltage, maximum load resistance, and short-circuit output current. Notice that the circuit uses a current booster on the output side. This increases the short-circuit output current to:

$$I_{max} = \beta_{dc} I_{sc} \quad (20-28)$$

### Output Current Directly Proportional to Input Voltage

In Fig. 20-29, the load current decreases when the input voltage increases. Figure 20-30 shows a circuit in which the load current is directly proportional to the input voltage. Because of the virtual short between the input terminals of the first op amp, the emitter current in  $Q_1$  is  $v_{in}/R$ . Since the  $Q_1$  collector current is approximately the same as the emitter current, the voltage across the collector  $R$  is  $v_{in}$  and the voltage at node  $A$  is:

$$V_A = V_{CC} - v_{in}$$

This is the noninverting input to the second op amp.

Because of the virtual short between the input terminals of the second op amp, the voltage at node  $B$  is:

$$V_B = V_A$$

The voltage across the final  $R$  is:

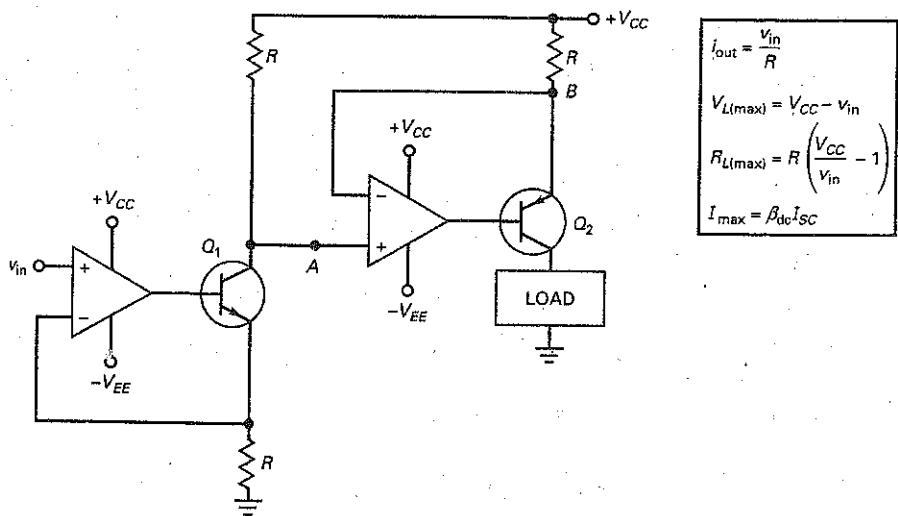
$$V_R = V_{CC} - V_B = V_{CC} - (V_{CC} - v_{in}) = v_{in}$$

Therefore, the output current is approximately:

$$i_{out} = \frac{v_{in}}{R} \quad (20-29)$$

Figure 20-30 shows the equations for analyzing this circuit. Again, a current booster increases the short-circuit output current by a factor  $\beta_{dc}$ .

Figure 20-30 Another unidirectional VCIS with single-ended load.



### Howland Current Source

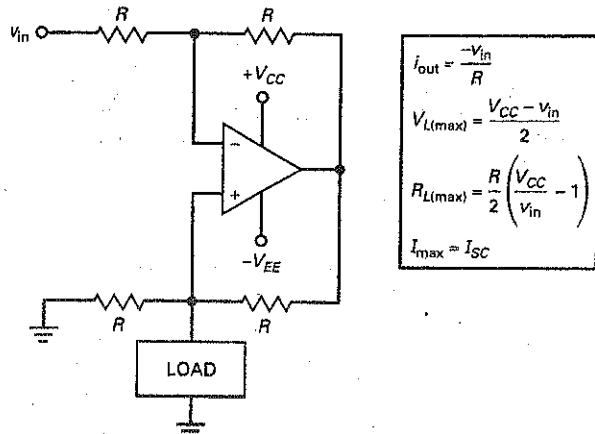
The current source of Fig. 20-30 produces a unidirectional load current. When a bidirectional current is needed, the Howland current source of Fig. 20-31 may be used. For a preliminary understanding of how it works, consider the special case of  $R_L = 0$ . When the load is shorted, the noninverting input is grounded, the inverting input is at virtual ground, and the output voltage is:

$$v_{\text{out}} = -v_{\text{in}}$$

On the lower side of the circuit, the output voltage will appear across  $R$  in series with the shorted load. The current through  $R$  is:

$$i_{\text{out}} = \frac{-v_{\text{in}}}{R} \quad (20-30)$$

Figure 20-31 Howland current source is a bidirectional VCIS.



When the load is shorted, all this current flows through the load. The minus sign means that the load voltage is inverted.

When the load resistance is greater than zero, the analysis is much more complicated because the noninverting input is no longer grounded and the inverting input is no longer a virtual ground. Instead, the noninverting input voltage equals the voltage across the load resistor. After writing and solving several equations, we can show that Eq. (20-30) is still valid for any load resistance, provided the op amp does not go into saturation. Since  $R_L$  does not appear in the equation, the circuit acts like a stiff current source.

Figure 20-31 shows the analysis equations. For instance, if  $V_{CC} = 15$ ,  $v_{in} = 3$  V, and  $R = 1$  k $\Omega$ , the maximum load resistance that can be used without saturating the op amp is:

$$R_{L(\max)} = \frac{1 \text{ k}\Omega}{2} \left( \frac{15 \text{ V}}{3 \text{ V}} - 1 \right) = 2 \text{ k}\Omega$$

### Example 20-8

 Multisim

If the current source of Fig. 20-28 has  $R = 10$  k $\Omega$ ,  $v_{in} = 1$  V, and  $V_{CC} = 15$  V, what is the output current? What is the maximum load resistance that can be used with this circuit if  $v_{in}$  can be as large as 10 V?

**SOLUTION** With the equations of Fig. 20-28, the output current is:

$$i_{out} = \frac{1 \text{ V}}{10 \text{ k}\Omega} = 0.1 \text{ mA}$$

The maximum load resistance is:

$$R_{L(\max)} = (10 \text{ k}\Omega) \left( \frac{15 \text{ V}}{10 \text{ V}} - 1 \right) = 5 \text{ k}\Omega$$

**PRACTICE PROBLEM 20-8** Change  $R$  to 2 k $\Omega$  and repeat Example 20-8.

### Example 20-9

The Howland current source of Fig. 20-31 has  $R = 15$  k $\Omega$ ,  $v_{in} = 3$  V, and  $V_{CC} = 15$  V. What is the output current? What is the largest load resistance that can be used with this circuit if the maximum input voltage is 9 V?

**SOLUTION** With the equations of Fig. 20-31:

$$i_{out} = \frac{-3 \text{ V}}{15 \text{ k}\Omega} = -0.2 \text{ mA}$$

The maximum load resistance is:

$$R_{L(\max)} = \frac{15 \text{ k}\Omega}{2} \left( \frac{15 \text{ V}}{12 \text{ V}} - 1 \right) = 1.88 \text{ k}\Omega$$

**PRACTICE PROBLEM 20-9** Repeat Example 20-9 with  $R = 10$  k $\Omega$ .

## 20-9 Automatic Gain Control

AGC stands for automatic gain control. In many applications like radio and television, we want the voltage gain to change automatically when the input signal changes. Specifically, when the input signal increases, we want the voltage gain to decrease. In this way, the output voltage of an amplifier will be approximately constant. One reason for wanting AGC in a radio or television is to keep the volume from changing abruptly when we tune in different stations.

### Audio AGC

Figure 20-32 shows an audio AGC circuit.  $Q_1$  is a JFET used as a voltage-controlled resistance. For small-signal operation with drain voltages near zero, the JFET operates in the ohmic region and has a resistance of  $r_{ds}$  to ac signals (discussed in Sec. 13-9). The  $r_{ds}$  of a JFET can be controlled by the gate voltage. The more negative the gate voltage is, the larger  $r_{ds}$  becomes. With a JFET like the 2N4861,  $r_{ds}$  can vary from  $100 \Omega$  to more than  $10 M\Omega$ .

$R_3$  and  $Q_1$  act like a voltage divider whose output varies between  $0.001v_{in}$  and  $v_{in}$ . Therefore, the noninverting input voltage is between  $0.001v_{in}$  and  $v_{in}$ , a 60-dB range. The output voltage of the noninverting amplifier is  $(R_2/R_1 + 1)$  times this input voltage.

In Fig. 20-32, the output voltage is coupled to the base of  $Q_2$ . For a peak-to-peak output less than  $1.4$  V,  $Q_2$  is cut off because there is no bias on it. With  $Q_2$  off, capacitor  $C_2$  is uncharged and the gate of  $Q_1$  is at  $-V_{EE}$ , enough negative voltage to cut off the JFET. This means that maximum input voltage reaches the noninverting input. In other words, an output voltage of less than  $1.4$  V pp implies that the circuit acts like a noninverting voltage amplifier with a maximum input signal.

When the output peak-to-peak voltage is greater than  $1.4$  V,  $Q_2$  conducts and charges capacitor  $C_2$ . This increases the gate voltage and decreases  $r_{ds}$ . With a smaller  $r_{ds}$ , the output of the  $R_3$  and  $Q_1$  voltage divider decreases and there is less input voltage to the noninverting input. In other words, the overall voltage gain of the circuit decreases when the peak-to-peak output voltage is greater than  $1.4$  V.

Figure 20-32 JFET used as a voltage-controlled resistance in AGC circuit.

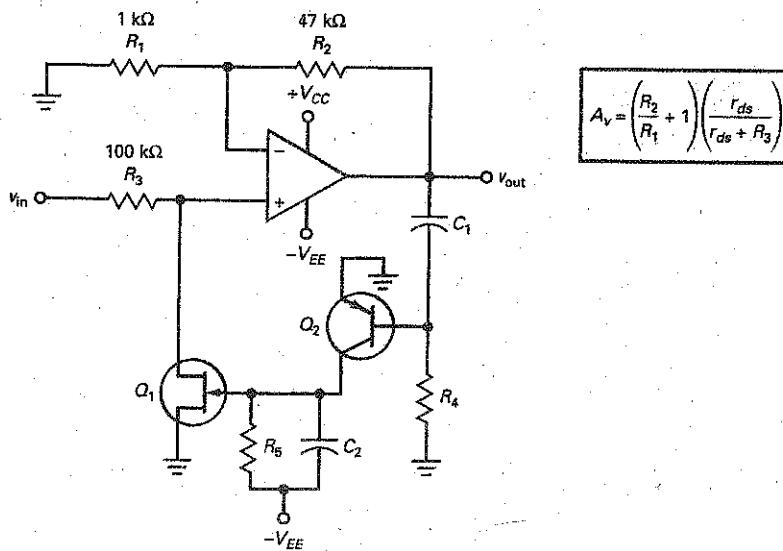
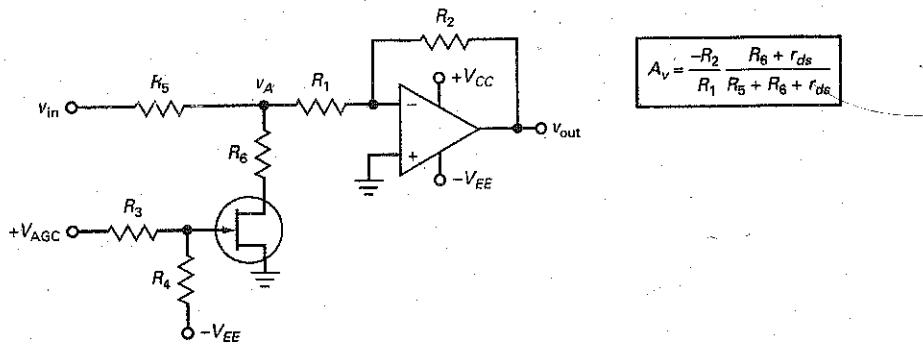


Figure 20-33 AGC circuit used with small input signals.



The larger the output voltage, the smaller the voltage gain. This way, the output voltage increases only slightly for large increases in the input signal. One reason for using AGC is to reduce sudden increases in signal level and prevent overdriving a loudspeaker. If you are listening to a radio, you do not want an unexpected increase in the signal level to bombard your ears. In summary, even though the input voltage of Fig. 20-32 varies over a 60-dB range, the peak-to-peak output is only slightly more than 1.4 V.

### Low-Level Video AGC

The signal out of a television camera has frequencies from 0 to well over 4 MHz. Frequencies in this range are called *video frequencies*. Figure 20-33 shows a standard technique for video AGC that has been used for frequencies up to 10 MHz. In this circuit the JFET acts like a voltage-controlled resistance. When the AGC voltage is zero, the JFET is cut off by the negative bias and its  $r_{ds}$  is maximum. As the AGC voltage increases, the  $r_{ds}$  of the JFET decreases.

The input voltage to the inverting amplifier comes from the voltage divider formed by  $R_5$ ,  $R_6$ , and  $r_{ds}$ . This voltage is given by:

$$v_A = \frac{R_6 + r_{ds}}{R_5 + R_6 + r_{ds}} v_{in}$$

The voltage gain of the inverting amplifier is:

$$A_v = \frac{-R_2}{R_1}$$

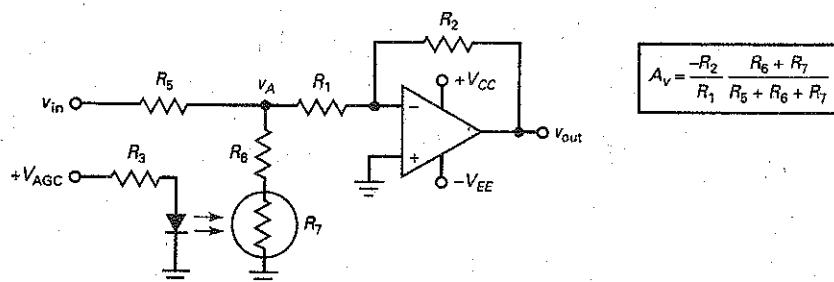
In this circuit the JFET is a voltage-controlled resistance. The more positive the AGC voltage, the smaller the value of  $r_{ds}$  and the lower the input voltage to the inverting amplifier. This means that the AGC voltage controls the overall voltage gain of the circuit.

With a wideband op amp, the circuit works well for input signals up to approximately 100 mV. Beyond this level, the JFET resistance becomes a function of the signal level in addition to the AGC voltage. This is undesirable because only the AGC voltage should control the overall voltage gain.

### High-Level Video AGC

For high-level video signals, we can replace the JFET by an LED-photoresistor combination like Fig. 20-34. The resistance  $R_7$  of the photoresistor decreases as the amount of light increases. Therefore, the larger the AGC voltage, the lower the

Figure 20-34 AGC circuit used with large input signals.



value of  $R_7$ . As before, the input voltage divider controls the amount of voltage driving the inverting voltage amplifier. This voltage is given by:

$$v_A = \frac{R_6 + R_7}{R_5 + R_6 + R_7} v_{in}$$

The circuit can handle high-level input voltages up to 10 V because the photocell resistance is unaffected by larger voltages and is a function only of  $V_{AGC}$ . Also, there is almost total isolation between the AGC voltage and the input voltage  $v_{in}$ .

### Example 20-10

If  $r_{ds}$  varies from  $50\ \Omega$  to  $120\ k\Omega$  in Fig. 20-32, what is the maximum voltage gain? What is the minimum voltage gain?

**SOLUTION** Using the values and equations of Fig. 20-32, the maximum voltage gain is:

$$A_v = \left( \frac{47\ k\Omega}{1\ k\Omega} + 1 \right) \frac{120\ k\Omega}{120\ k\Omega + 100\ k\Omega} = 26.2$$

The minimum voltage gain is:

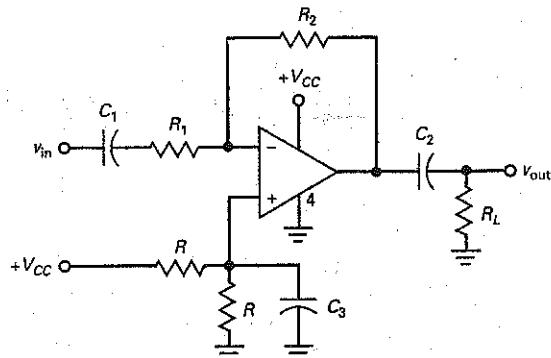
$$A_v = \left( \frac{47\ k\Omega}{1\ k\Omega} + 1 \right) \frac{50\ \Omega}{50\ \Omega + 100\ k\Omega} = 0.024$$

**PRACTICE PROBLEM 20-10** In Example 20-10, what value should  $r_{ds}$  drop to for a voltage gain of 1?

## 20-10 Single-Supply Operation

Using dual supplies is the typical way to power op amps. But this is not necessary or even desirable in some applications. This section discusses the inverting and noninverting amplifiers running off a single positive supply.

Figure 20-35 Single-supply inverting amplifier.



$$A_v = \frac{-R_2}{R_1}$$

$$f_1 = \frac{1}{2\pi R_1 C_1}$$

$$f_2 = \frac{1}{2\pi R_L C_2}$$

$$f_3 = \frac{1}{2\pi(R/2)C_3}$$

### Inverting Amplifier

Figure 20-35 shows a single-supply inverting voltage amplifier that can be used with ac signals. The  $V_{EE}$  supply (pin 4) is grounded, and a voltage divider applies half the  $V_{CC}$  supply to the noninverting input. Because the two inputs are virtually shorted, the inverting input has a quiescent voltage of approximately  $+0.5V_{CC}$ .

In the dc equivalent circuit, all capacitors are open and the circuit is a voltage follower that produces a dc output voltage of  $+0.5V_{CC}$ . Input offsets are minimized because the voltage gain is unity.

In the ac equivalent circuit, all capacitors are shorted and the circuit is an inverting amplifier with a voltage gain of  $-R_2/R_1$ . Figure 20-35 shows the analysis equations. With these, we calculate the three lower cutoff frequencies.

A bypass capacitor is used on the noninverting input, as shown in Fig. 20-35. This reduces the power-supply ripple and noise appearing at the noninverting input. To be effective, the cutoff frequency of this bypass circuit should be much lower than the ripple frequency out of the power supply. You can calculate the cutoff frequency of this bypass circuit with the equation given in Fig. 20-35.

### Noninverting Amplifier

In Fig. 20-36, only a positive supply is being used. To get maximum output swing, you need to bias the noninverting input at half the supply voltage, which is conveniently done with an equal-resistor voltage divider. This produces a dc input of  $+0.5V_{CC}$  at the noninverting input. Because of the negative feedback, the inverting input is bootstrapped to the same value.

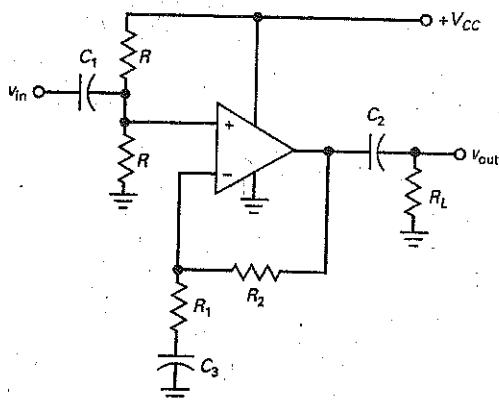
In the dc equivalent circuit, all capacitors are open and the circuit has a voltage gain of unity, which minimizes the output offset voltage. The dc output voltage of the op amp is  $+0.5V_{CC}$ , but this is blocked from the final load by the output coupling capacitor.

In the ac equivalent circuit, all capacitors are shorted. When an ac signal drives the circuit, an amplified output signal appears across  $R_L$ . If a rail-to-rail op amp is used, the maximum peak-to-peak unclipped output is  $V_{CC}$ . Figure 20-36 gives the equations for calculating the cutoff frequencies.

### Single-Supply Op Amps

Although we can use ordinary op amps with a single supply, as shown in Figs. 20-35 and 20-36, there are some op amps that are optimized for single-supply operation. For instance, the LM324 is a quad op amp that eliminates the

Figure 20-36 Single-supply noninverting amplifier.



$$A_v = \frac{R_2}{R_1} + 1$$

$$f_1 = \frac{1}{2\pi(R/2)C_1}$$

$$f_2 = \frac{1}{2\pi R_L C_2}$$

$$f_3 = \frac{1}{2\pi R_1 C_3}$$

need for dual supplies. It contains four internally compensated op amps in a single package, each with an open-loop voltage gain of 100 dB, input biasing current of 45 nA, input offset current of 5 nA, and input offset voltage of 2 mV. It runs off a single positive supply voltage that can have any value between 3 and 32 V. Because of this, the LM324 is convenient to use as an interface with digital circuits that run off a single positive supply of +5 V.

## Summary

### SEC. 20-1 INVERTING-AMPLIFIER CIRCUITS

Inverting-amplifier circuits discussed in this section included a high-impedance probe (X10 and X1), an ac-coupled amplifier, and an adjustable-bandwidth circuit.

### SEC. 20-2 NONINVERTING-AMPLIFIER CIRCUITS

Noninverting-amplifier circuits discussed in this section included an ac-coupled amplifier, an audio distribution amplifier, a JFET-switched amplifier, and a voltage reference.

### SEC. 20-3 INVERTER/NONINVERTER CIRCUITS

The circuits discussed in this section are the switchable inverter/noninverter, the JFET-controlled switchable inverter, the

sign changer, the adjustable and reversible gain circuit, and the phase shifter.

### SEC. 20-4 DIFFERENTIAL AMPLIFIERS

Two factors determine the overall CMRR of a differential amplifier: the CMRR of each op amp and the CMRR of the matched resistors. The input signal is usually a small differential voltage and a large common-mode voltage coming from a Wheatstone bridge.

### SEC. 20-5 INSTRUMENTATION AMPLIFIERS

An instrumentation amplifier is a differential amplifier optimized for large voltage gain, high CMRR, low input offsets, low-temperature drift, and high input impedance. Instrumentation amplifiers can be built with the classic

three op-amp circuit, using precision op amps, or with an integrated instrumentation amplifier.

### SEC. 20-6 SUMMING AMPLIFIER CIRCUITS

The topics discussed in this section were the subtracter, summing on both inputs, the averager, and the D/A converter. The D/A converter is used in digital multimeters to measure voltages, currents, and resistances.

### SEC. 20-7 CURRENT BOOSTERS

When the short-circuit output current of an op amp is too low, one solution is to use a current booster on the output side of the circuit. Typically, the current booster is a transistor whose base current is supplied by the op amp. Because of the transistor current gain, the short-circuit output current is increased by the  $\beta$  factor.

### SEC. 20-8 VOLTAGE-CONTROLLED CURRENT SOURCES

We can build current sources that are controlled by an input voltage. The loads may be floating or grounded. The load currents may be unidirectional or bidirectional. The Howland current source is a bidirectional voltage-controlled current source.

## Derivations

(20-3) Gain for inverter/noninverter circuits:

$$A_v = A_{v(\text{inv})} + A_{v(\text{non})}$$

See Figs. 20-8 to 20-13. The total voltage gain is the superposition of the inverting and noninverting voltage gains. We use it when the input signal is being applied to both inputs.

(20-5) Common-mode voltage gain:

$$A_{v(\text{CM})} = A_{v(\text{inv})} + A_{v(\text{non})}$$

See Fig. 20-14, 20-15, and 20-18. This is similar to Eq. (20-3) because it is the superposition of gains.

(20-7) Overall noninverter gain:

$$A_{v(\text{non})} = \left( \frac{R_2}{R_1} + 1 \right) \left( \frac{R'_2}{R'_1 + R'_2} \right)$$

See Fig. 20-14. This is the voltage gain of the noninverting side reduced by the voltage-divider factor.

(20-8) Common-mode gain for  $R_1 = R_2$ :

$$A_{v(\text{CM})} = \pm 2 \frac{\Delta R}{R}$$

See Figs. 20-15 and 20-18. This is the common-mode gain caused by the resistor tolerances when the resistors of the differential amplifier are equal and matched.

(20-11) Wheatstone bridge:

$$\frac{R_1}{R_2} = \frac{R_3}{R_4}$$

See Fig. 20-16a. This is the equation for balance in a Wheatstone bridge.

### SEC. 20-9 AUTOMATIC GAIN CONTROL

In many applications we want the voltage gain of a system to change automatically as needed to maintain an almost constant output voltage. In radio and television receivers, AGC prevents sudden and large changes in the volume of the sound out of the speakers.

### SEC. 20-10 SINGLE-SUPPLY OPERATION

Although op amps normally use dual supplies, there are applications for which only a single supply is preferred. When ac-coupled amplifiers are needed, single-supply amplifiers are easily implemented by biasing the nonsignal side of the op amp to half the positive supply voltage. Some op amps are optimized for single-supply operation.

(20-13) Unbalanced Wheatstone bridge:

$$V_{\text{in}} \approx \frac{\Delta R}{4R} V_{\text{cc}}$$

See Fig. 20-17. This equation is valid for small changes in the resistance of the transducer.

(20-16) Instrumentation amplifier:

$$A_v = \frac{2R_2}{R_G} + 1$$

See Figs. 20-18 and 20-20. This is the voltage gain of the first stage of the classic three op-amp instrumentation amplifier.

(20-18) Binary-to-decimal equivalent:

$$\text{BIN} = (D_0 \times 2^0) + (D_1 \times 2^1) + (D_2 \times 2^2) + (D_3 \times 2^3)$$

(20-19) R/2R Ladder output voltage:

$$V_{\text{out}} = -\left( \frac{\text{BIN}}{2^N} \times 2V_{\text{ref}} \right)$$

(20-21) Current booster:

$$I_{\text{max}} = \beta_{\text{dc}} I_{\text{sc}}$$

See Figs. 20-26 to 20-30. The short-circuit current of an op amp is increased by the current gain of a transistor between the op amp and the load.

(20-23) Voltage-controlled current sources:

$$i_{\text{out}} = \frac{V_{\text{in}}}{R}$$

See Figs. 20-28 to 20-31. In voltage-controlled current sources, the input voltage is converted to a stiff output current.

## Student Assignments

- In a linear op-amp circuit, the
  - Signals are always sine waves
  - Op amp does not go into saturation
  - Input impedance is ideally infinite
  - Gain-bandwidth product is constant

- In an ac amplifier using an op amp with coupling and bypass capacitors, the output offset voltage is
  - Zero
  - Minimum
  - Maximum
  - Unchanged

- To use an op amp, you need at least
  - One supply voltage
  - Two supply voltages
  - One coupling capacitor
  - One bypass capacitor

4. In a controlled current source with op amps, the circuit acts like a
- Voltage amplifier
  - Current-to-voltage converter
  - Voltage-to-current converter
  - Current amplifier
5. An instrumentation amplifier has a high
- Output impedance
  - Power gain
  - CMRR
  - Supply voltage
6. A current booster on the output of an op amp will increase the short-circuit current by
- $A_{v(\text{dc})}$
  - $\beta_{\text{dc}}$
  - $f_{\text{unity}}$
  - $A_v$
7. Given a voltage reference of  $+2.5 \text{ V}$ , we can get a voltage reference of  $+15 \text{ V}$  by using
- An inverting amplifier
  - A noninverting amplifier
  - A differential amplifier
  - An instrumentation amplifier
8. In a differential amplifier, the CMRR is limited mostly by the
- CMRR of the op amp
  - Gain-bandwidth product
  - Supply voltages
  - Tolerance of the resistors
9. The input signal for an instrumentation amplifier usually comes from
- An inverting amplifier
  - A resistor
  - A differential amplifier
  - A Wheatstone bridge
10. In the classic three op-amp instrumentation amplifier, the differential voltage gain is usually produced by the
- First stage
  - Second stage
  - Mismatched resistors
  - Output op amp
11. Guard driving reduces the
- CMRR of an instrumentation amplifier
  - Leakage current in the shielded cable
  - Voltage gain of the first stage
  - Common-mode input voltage
12. In an averaging circuit, the input resistances are
- Equal to the feedback resistance
  - Less than the feedback resistance
  - Greater than the feedback resistance
  - Unequal
13. A D/A converter is an application of the
- Adjustable bandwidth circuit
  - Noninverting amplifier
  - Voltage-to-current converter
  - Summing amplifier
14. In a voltage-controlled current source,
- A current booster is never used
  - The load is always floated
  - A stiff current source drives the load
  - The load current equals  $I_{\text{sc}}$
15. The Howland current source produces a
- Unidirectional floating load current
  - Bidirectional single-ended load current
  - Unidirectional single-ended load current
  - Bidirectional floating load current
16. The purpose of AGC is to
- Increase the voltage gain when the input signal increases
  - Convert voltage to current
  - Keep the output voltage almost constant
  - Reduce the CMRR of the circuit
17. 1 ppm is equivalent to
- 0.1 percent
  - 0.01 percent
  - 0.001 percent
  - 0.0001 percent
18. An input transducer converts
- Voltage to current
  - Current to voltage
  - An electrical quantity to a nonelectrical quantity
  - A nonelectrical quantity to an electrical quantity
19. A thermistor converts
- Light to resistance
  - Temperature to resistance
  - Voltage to sound
  - Current to voltage
20. When we trim a resistor, we are
- Making a fine adjustment
  - Reducing its value
  - Increasing its value
  - Making a coarse adjustment
21. A D/A converter with four inputs has
- Two output values
  - Four output values
  - Eight output values
  - Sixteen output values
22. An op amp with a rail-to-rail output
- Has a current-boosted output
  - Can swing all the way to either supply voltage
  - Has a high output impedance
  - Cannot be less than 0 V
23. When a JFET is used in an AGC circuit, it acts like a
- Switch
  - Voltage-controlled current source
  - Voltage-controlled resistance
  - Capacitance
24. If an op amp has only a positive supply voltage, its output cannot
- Be negative
  - Be zero
  - Equal the supply voltage
  - Be ac-coupled

## Problems

### SEC. 20-1 INVERTING-AMPLIFIER CIRCUITS

- 20-1 In the probe of Fig. 20-1,  $R_1 = 10 \text{ M}\Omega$ ,  $R_2 = 20 \text{ M}\Omega$ ,  $R_3 = 15 \text{ k}\Omega$ ,  $R_4 = 15 \text{ k}\Omega$ , and  $R_5 = 75 \text{ k}\Omega$ . What is the attenuation of the probe in each switch position?
- 20-2 In the ac-coupled inverting amplifier of Fig. 20-2,  $R_1 = 1.5 \text{ k}\Omega$ ,  $R_f = 75 \text{ k}\Omega$ ,  $R_L = 15 \text{ k}\Omega$ ,  $C_1 = 1 \mu\text{F}$ ,  $C_2 = 4.7 \mu\text{F}$ , and  $f_{\text{unity}} = 1 \text{ MHz}$ . What is the voltage gain in the midband of the amplifier? What are the upper and lower cutoff frequencies?
- 20-3 In the adjustable-bandwidth circuit of Fig. 20-3,  $R_1 = 10 \text{ k}\Omega$  and  $R_f = 180 \text{ k}\Omega$ . If the  $100\text{-}\Omega$  resistor is changed to  $130 \text{ }\Omega$  and the variable resistor to  $25 \text{ k}\Omega$ , what is the voltage gain? What are the minimum and maximum bandwidth if  $f_{\text{unity}} = 1 \text{ MHz}$ ?
- 20-4 What is the output voltage in Fig. 20-37? What are the minimum and maximum bandwidth? (Use  $f_{\text{unity}} = 1 \text{ MHz}$ .)

Figure 20-37

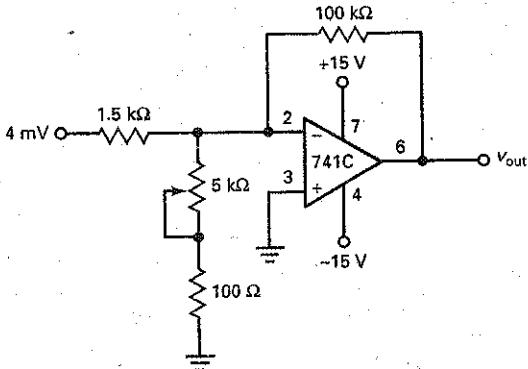
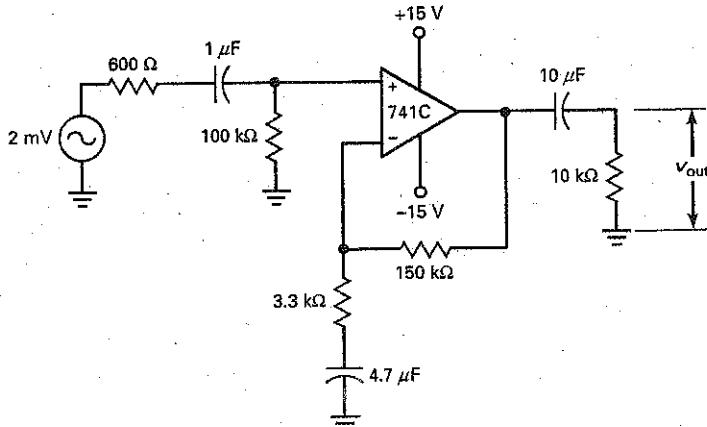


Figure 20-38



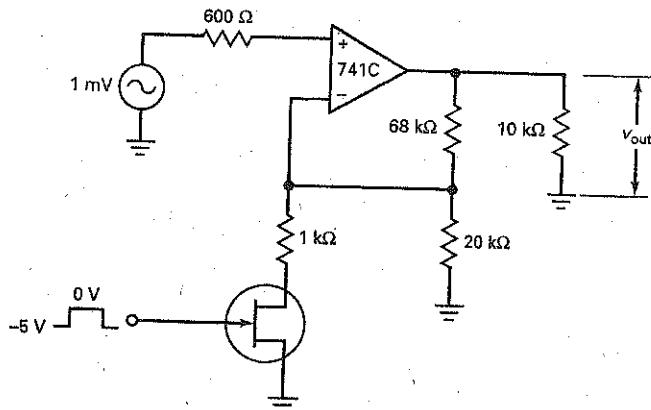
### SEC. 20-2 NONINVERTING-AMPLIFIER CIRCUITS

- 20-5 In Fig. 20-4,  $R_1 = 2 \text{ k}\Omega$ ,  $R_f = 82 \text{ k}\Omega$ ,  $R_L = 25 \text{ k}\Omega$ ,  $C_1 = 2.2 \mu\text{F}$ ,  $C_2 = 4.7 \mu\text{F}$ , and  $f_{\text{unity}} = 3 \text{ MHz}$ . What is the voltage gain in the midband of the amplifier? What are the upper and lower cutoff frequencies?
- 20-6 What is the voltage gain in the midband of Fig. 20-38? What are the upper and lower cutoff frequencies?
- 20-7 **Multisim** In the distribution amplifier of Fig. 20-5,  $R_1 = 2 \text{ k}\Omega$ ,  $R_f = 100 \text{ k}\Omega$ , and  $V_{\text{in}} = 10 \text{ mV}$ . What is the output voltage for A, B, and C?
- 20-8 The JFET-switched amplifier of Fig. 20-6 has these values:  $R_1 = 91 \text{ k}\Omega$ ,  $R_f = 12 \text{ k}\Omega$ , and  $R_2 = 1 \text{ k}\Omega$ . If  $V_{\text{in}} = 2 \text{ mV}$ , what is the output voltage when the gate is low? When it is high?
- 20-9 If  $V_{GS(\text{off})} = -5 \text{ V}$ , what are the minimum and maximum output voltage in Fig. 20-39?
- 20-10 The voltage reference of Fig. 20-7 is modified to get  $R_1 = 10 \text{ k}\Omega$  and  $R_f = 10 \text{ k}\Omega$ . What is the new output reference voltage?

### SEC. 20-3 INVERTER/NONINVERTER CIRCUITS

- 20-11 In the adjustable inverter of Fig. 20-10,  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 10 \text{ k}\Omega$ . What is the maximum positive gain? The maximum negative gain?
- 20-12 What is the voltage gain in Fig. 20-11 when the wiper is at the ground end? When it is 10 percent away from ground?
- 20-13 Precision resistors are used in Fig. 20-12. If  $R = 5 \text{ k}\Omega$ ,  $nR = 75 \text{ k}\Omega$ , and  $nR/(n-1)R = 5.36 \text{ k}\Omega$ , what are the maximum positive and negative gains?
- 20-14 In the phase shifter of Fig. 20-13,  $R' = 10 \text{ k}\Omega$ ,  $R = 22 \text{ k}\Omega$ , and  $C = 0.02 \mu\text{F}$ . What is the phase shift when the input frequency is 100 Hz? 1 kHz? 10 kHz?

Figure 20-39



#### SEC. 20-4 DIFFERENTIAL AMPLIFIERS

20-15 The differential amplifier of Fig. 20-14 has  $R_1 = 1.5 \text{ k}\Omega$  and  $R_2 = 30 \text{ k}\Omega$ . What is the differential voltage gain? The common-mode gain? (Resistor tolerance =  $\pm 0.1$  percent.)

20-16 In Fig. 20-15,  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 20 \text{ k}\Omega$ . What is the differential voltage gain? The common-mode gain? (Resistor tolerance =  $\pm 1$  percent.)

20-17 In the Wheatstone bridge of Fig. 20-16,  $R_1 = 10 \text{ k}\Omega$ ,  $R_2 = 20 \text{ k}\Omega$ ,  $R_3 = 20 \text{ k}\Omega$ , and  $R_4 = 10 \text{ k}\Omega$ . Is the bridge balanced?

20-18 In the typical application of Fig. 20-17, transducer resistance changes to  $985 \Omega$ . What is the final output voltage?

#### SEC. 20-5 INSTRUMENTATION AMPLIFIERS

20-19 In the instrumentation amplifier of Fig. 20-18,  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 99 \text{ k}\Omega$ . What is the output voltage if  $v_{in} = 2 \text{ mV}$ ? If three OP-07A op amps are used and  $R = 10 \text{ k}\Omega \pm 0.5$  percent, what is the CMRR of the instrumentation amplifier?

20-20 In Fig. 20-19,  $v_{in(CM)} = 5 \text{ V}$ . If  $R_3 = 10 \text{ k}\Omega$ , what does the guard voltage equal?

20-21 The value of  $R_B$  is changed to  $1008 \Omega$  in Fig. 20-20. What is the differential output voltage if the differential input voltage is  $20 \text{ mV}$ ?

#### SEC. 20-6 SUMMING AMPLIFIER CIRCUITS

20-22 What does the output voltage equal in Fig. 20-21 if  $R = 10 \text{ k}\Omega$ ,  $v_1 = -50 \text{ mV}$  and  $v_2 = -30 \text{ mV}$ ?

20-23 **Multisim** In the summing circuit of Fig. 20-22,  $R_1 = 10 \text{ k}\Omega$ ,  $R_2 = 20 \text{ k}\Omega$ ,  $R_3 = 15 \text{ k}\Omega$ ,  $R_4 = 15 \text{ k}\Omega$ ,  $R_5 = 30 \text{ k}\Omega$ , and  $R_f = 75 \text{ k}\Omega$ . What is the output voltage if  $v_0 = 1 \text{ mV}$ ,  $v_1 = 2 \text{ mV}$ ,  $v_2 = 3 \text{ mV}$ , and  $v_3 = 4 \text{ mV}$ ?

20-24 The averaging circuit of Fig. 20-23 has  $R = 10 \text{ k}\Omega$ . What is the output if  $v_1 = 1.5 \text{ V}$ ,  $v_2 = 2.5 \text{ V}$ , and  $v_3 = 4.0 \text{ V}$ ?

20-25 The D/A converter of Fig. 20-24 has an input of  $v_0 = 5 \text{ V}$ ,  $v_1 = 0$ ,  $v_2 = 5 \text{ V}$ , and  $v_3 = 0$ . What is the output voltage?

20-26 In Fig. 20-25, if the number of binary inputs is expanded to eight and  $D_7$  to  $D_0$  equals 10100101, determine the decimal equivalent input value, BIN.

20-27 In Fig. 20-25, if the binary inputs were expanded so  $D_7$  to  $D_0$  equaled 01100110, what would be the output voltage?

20-28 In Fig. 20-25, using an input reference voltage of  $2.5 \text{ V}$ , determine the smallest incremental output voltage step.

#### SEC. 20-7 CURRENT BOOSTERS

20-29 The noninverting amplifier of Fig. 20-40 has a current-boosted output. What is the voltage gain of the circuit? If the transistor has a current gain of 100, what is the short-circuit output current?

20-30 What is the voltage gain in Fig. 20-41? If the transistors have a current gain of 125, what is the short-circuit output current?

Figure 20-40

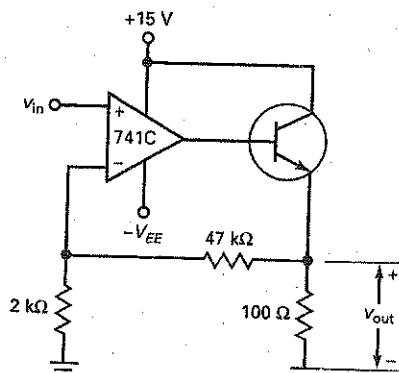
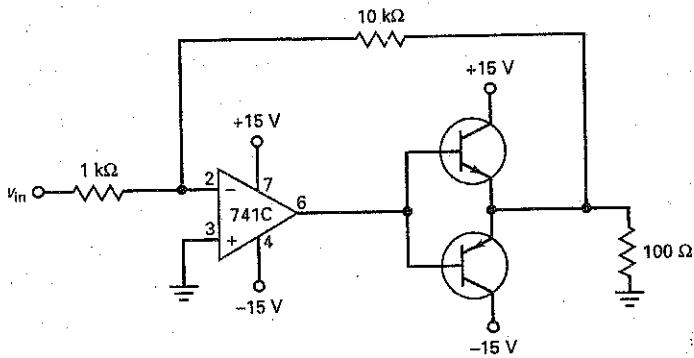


Figure 20-41



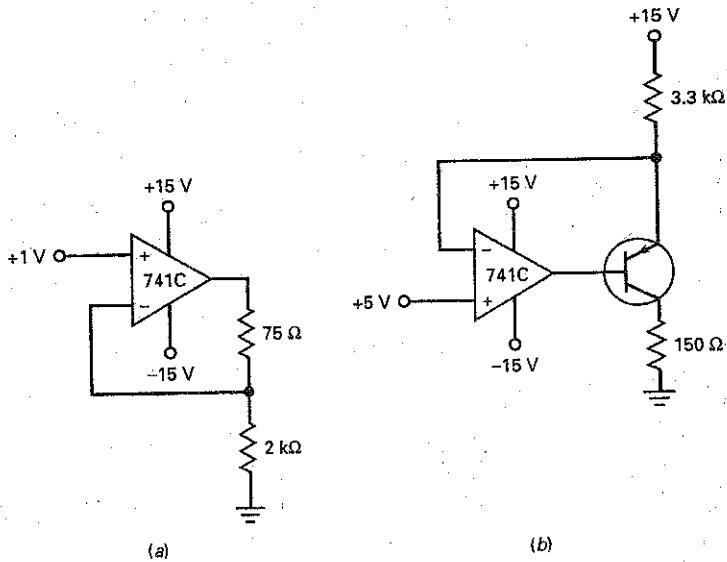
#### SEC. 20-8 VOLTAGE-CONTROLLED CURRENT SOURCES

- 20-31 What is the load current in Fig. 20-42a? The maximum load resistance that can be used without saturating the op amp?
- 20-32 Calculate the output current in Fig. 20-42b. Also, work out the maximum value of load resistance.
- 20-33 If  $R = 10 \text{ k}\Omega$  and  $V_{cc} = 15 \text{ V}$  in the voltage-controlled current source of Fig. 20-30, what is the output current when the input voltage is 3 V? The maximum load resistance?
- 20-34 The Howland current source of Fig. 20-31 has  $R = 2 \text{ k}\Omega$  and  $R_f = 500 \text{ }\Omega$ . What is the output current when the input voltage is 6 V? What is the maximum load resistance that can be used with this circuit if the input voltage is never greater than 7.5 V? (Use supply voltages of  $\pm 15 \text{ V}$ .)

#### SEC. 20-9 AUTOMATIC GAIN CONTROL

- 20-35 In the AGC circuit of Fig. 20-32,  $R_1 = 10 \text{ k}\Omega$ ,  $R_2 = 100 \text{ k}\Omega$ ,  $R_3 = 100 \text{ k}\Omega$ , and  $R_4 = 10 \text{ k}\Omega$ . If  $r_{ds}$  can vary from  $200 \text{ }\Omega$  to  $1 \text{ M}\Omega$ , what is the minimum voltage gain of the circuit? The maximum?
- 20-36 In the low-level AGC circuit of Fig. 20-33,  $R_1 = 5.1 \text{ k}\Omega$ ,  $R_2 = 51 \text{ k}\Omega$ ,  $R_5 = 68 \text{ k}\Omega$ , and  $R_6 = 1 \text{ k}\Omega$ . If  $r_{ds}$  can vary from  $120 \text{ }\Omega$  to  $5 \text{ M}\Omega$ , what is the minimum voltage gain of the circuit? The maximum?
- 20-37 In the high-level AGC circuit of Fig. 20-34,  $R_1 = 10 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$ ,  $R_5 = 75 \text{ k}\Omega$ , and  $R_6 = 1.2 \text{ k}\Omega$ . If  $R_7$  can vary from  $180 \text{ }\Omega$  to  $10 \text{ M}\Omega$ , what is the minimum voltage gain of the circuit? The maximum?

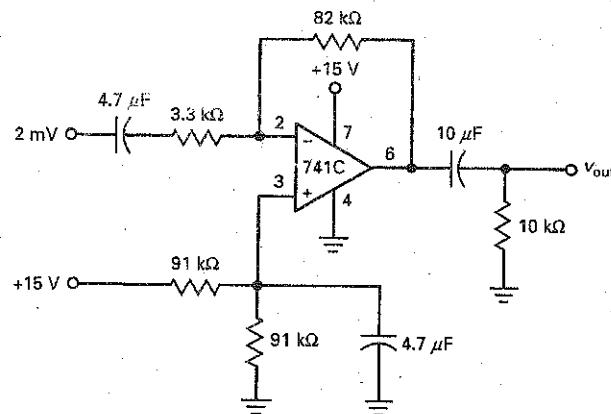
Figure 20-42



- 20-38 What is the voltage gain in the single-supply inverting amplifier of Fig. 20-43? The three lower cutoff frequencies?

- 20-39 In the single-supply noninverting amplifier of Fig. 20-36,  $R = 68 \text{ k}\Omega$ ,  $R_1 = 1.5 \text{ k}\Omega$ ,  $R_2 = 15 \text{ k}\Omega$ ,  $R_L = 15 \text{ k}\Omega$ ,  $\Omega_1 = 1 \mu\text{F}$ ,  $C_2 = 2.2 \mu\text{F}$ , and  $C_3 = 3.3 \mu\text{F}$ . What is the voltage gain? The three lower cutoff frequencies?

Figure 20-43

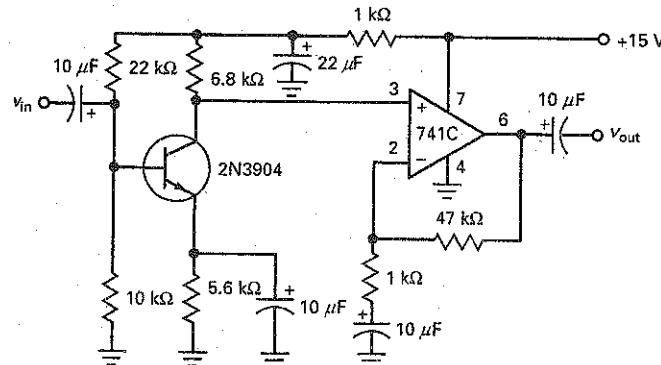


## Critical Thinking

- 20-40 When switching between the positions of Fig. 20-8, there is a brief period of time when the switch is temporarily open. What is the output voltage at this time? Can you suggest how to prevent this from happening?
- 20-41 An inverting amplifier has  $R_1 = 1 \text{ k}\Omega$  and  $R_f = 100 \text{ k}\Omega$ . If these resistances have tolerances of  $\pm 1$  percent, what is the maximum possible voltage gain? The minimum?

- 20-42 What is the voltage gain in the midband of the circuit shown in Fig. 20-44?
- 20-43 The transistors of Fig. 20-41 have  $\beta_{dc} = 50$ . If the input voltage is 0.5 V, what is the base current in the conducting transistor?

Figure 20-44



## Troubleshooting

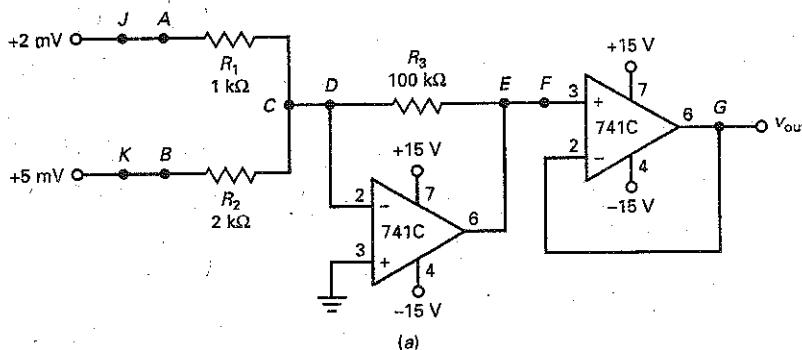
**Multisim** Use Fig. 20-45 for the remaining problems. Any resistor may be open or shorted. Also, connecting wires CD, EF, JA, or KB may be open. Voltage values are in millivolts unless otherwise indicated.

20-44 Find Troubles T1 to T3.

20-45 Find Troubles T4 to T6.

20-46 Find Troubles T7 to T10.

Figure 20-45



(a)

Troubleshooting

Trouble	$V_A$	$V_B$	$V_C$	$V_D$	$V_E$	$V_F$	$V_G$
OK	2	5	0	0	450	450	450
T1	2	5	0	0	450	0	0
T2	2	5	0	0	200	200	200
T3	2	5	2	2	-13.5 V	-13.5 V	-13.5 V
T4	2	0	0	0	200	200	200
T5	2	5	3	0	0	0	0
T6	0	5	0	0	250	250	250
T7	2	5	3	3	-13.5 V	-13.5 V	-13.5 V
T8	2	5	0	0	250	250	250
T9	2	5	0	0	0	0	0
T10	2	5	5	5	-13.5 V	-13.5 V	-13.5 V

(b)

## Job Interview Questions

1. Draw the schematic diagram of an ac-coupled inverting amplifier with a voltage gain of 100. Discuss the theory of operation.
2. Draw the schematic diagram of a differential amplifier built with an op amp. What are the factors that determine the CMRR?

3. Draw the schematic diagram of the classic three op-amp instrumentation amplifier. Tell me what the first stage does to the differential and common-mode signals.
4. Why does the instrumentation amplifier have more than one stage?
5. You have designed a simple op-amp circuit for a particular application. During your initial testing, you find that the op amp is very hot to the touch. Assuming that the circuit has been correctly breadboarded, what is the most likely problem and what can you do to correct it?
6. Explain how an inverting amplifier is used in a high-impedance probe (X10 and X1).
7. In Fig. 20-1, why does the probe see a high impedance? Explain how the voltage gain is calculated in each switch position.
8. What can be said about the analog output of a D/A converter when it is compared with the digital input?
9. You want to construct a portable op-amp circuit that runs off a single 9-V battery using a 741C. What is one way you can do this? How would you have to modify this circuit if a dc response is required?
10. How could you increase the output current of an op amp?
11. Why is no resistor or diode biasing required in the circuit of Fig. 20-27?
12. When working with op amps, one often hears the term *rail*, as in a *rail-to-rail amplifier*. To what does that term refer?
13. Can a 741 be operated with a single supply voltage? If so, discuss what would be required for an inverting amplifier.

## Self-Test Answers

- |      |       |       |
|------|-------|-------|
| 1. b | 9. d  | 17. d |
| 2. b | 10. a | 18. d |
| 3. a | 11. b | 19. b |
| 4. c | 12. c | 20. a |
| 5. c | 13. d | 21. d |
| 6. b | 14. c | 22. b |
| 7. b | 15. b | 23. c |
| 8. d | 16. c | 24. a |

## Practice Problem Answers

- |  |   |  |
|--|---|--|
| 20-2 $R_2 = 60 \text{ k}\Omega$  | 20-5 $A_{v1} = -1; A_{v2} = -0.5;$<br>$A_{v3} = -1.06; A_{v4} = -0.798$             | 20-8 $i_{out} = 0.5 \text{ mA}; R_{L(\max)} = 1 \text{ k}\Omega$     |
| 20-3 $N = 7.5; nR = 1.154 \text{ k}\Omega$   | 20-6 largest $V_{out} = -9.375 \text{ V};$<br>smallest $V_{out} = -0.625 \text{ V}$ | 20-9 $i_{out} = -0.3 \text{ mA}; R_{L(\max)} = 1.25 \text{ k}\Omega$ |
| 20-4 $A_v = 51; A_{v(CM)} = 0.002;$<br>$V_{out} = -510 \text{ mV};$<br>$V_{out(CM)} = \pm 20 \text{ mV}$ | 20-7 $A_v = -27; Z_{out(CL)} = 0.021 \Omega;$<br>$I_{max} = 2.5 \text{ A}$          | 20-10 $r_{ds} = 2.13 \text{ k}\Omega$                                |

# 21

# Active Filters

- Almost all communication systems use filters. A filter passes one band of frequencies while rejecting another. A filter can be either passive or active. Passive filters are built with resistors, capacitors, and inductors. They are generally used above 1 MHz, have no power gain, and are relatively difficult to tune. Active filters are built with resistors, capacitors, and op amps. They are useful below 1 MHz, have power gain, and are relatively easy to tune. Filters can separate desired signals from undesired signals, block interfering signals, enhance speech and video, and alter signals in other ways.

## Chapter Outline

- 21-1 Ideal Responses
- 21-2 Approximate Responses
- 21-3 Passive Filters
- 21-4 First-Order Stages
- 21-5 VCVS Unity-Gain Second-Order Low-Pass Filters
- 21-6 Higher-Order Filters
- 21-7 VCVS Equal-Component Low-Pass Filters
- 21-8 VCVS High-Pass Filters
- 21-9 MFB Bandpass Filters
- 21-10 Bandstop Filters
- 21-11 The All-Pass Filter
- 21-12 Biquadratic and State-Variable Filters

## Objectives

*After studying this chapter, you should be able to:*

- Discuss the five basic filter responses.
- Describe the difference between passive and active filters.
- Differentiate between brick wall responses and approximate responses.
- Explain filter terminology, including passband, stopband, cutoff,  $Q$ , ripple, and order.
- Determine the order of passive and active filters.
- Discuss the reasons why filter stages are sometimes cascaded, and describe the results.

## Vocabulary

active filters	elliptic approximation	passive filters
all-pass filter	frequency scaling factor (FSF)	pole frequency ( $f_p$ )
attenuation	geometric average	poles
bandpass filter	high-pass filter	predistortion
bandstop filter	inverse Chebyshev approximation	Sallen-Key equal-component filter
Bessel approximation	linear phase shift	Sallen-Key low-pass filter
biquadratic bandpass/lowpass filter	low-pass filter	Sallen-Key second-order notch filter
Butterworth approximation	monotonic	state-variable filter
Chebyshev approximation	multiple-feedback (MFB)	stopband
damping factor	narrowband filter	transition
delay equalizer	order of a filter	wideband filter
edge frequency	passband	

## 21-1 Ideal Responses

This chapter is a comprehensive look at a variety of passive and active filter circuits. Basic filter terminology and first-order stages are covered through Sec. 21-4. Sections 21-5 and beyond contain more detailed circuit analysis of higher-order filters.

The *frequency response of a filter* is the graph of its voltage gain versus frequency. There are five types of filters: *low-pass*, *high-pass*, *bandpass*, *band-stop*, and *all-pass*. This section discusses the ideal frequency response of each. The next section describes the approximations for these ideal responses.

### Low-Pass Filter

Figure 21-1 shows the ideal frequency response of a **low-pass filter**. It is sometimes called a *brick wall response* because the right edge of the rectangle looks like a brick wall. A low-pass filter passes all frequencies from zero to the cutoff frequency and blocks all frequencies above the cutoff frequency.

With a low-pass filter, the frequencies between zero and the cutoff frequency are called the **passband**. The frequencies above the cutoff frequency are called the **stopband**. The roll-off region between the passband and the stopband is called the **transition**. An ideal low-pass filter has zero **attenuation** (signal loss) in the passband, infinite attenuation in the stopband, and a vertical transition.

One more point: The ideal low-pass filter has zero phase shift for all frequencies in the passband. Zero phase shift is important when the input signal is nonsinusoidal. When a filter has zero phase shift, the shape of the nonsinusoidal signal is preserved as it passes through the ideal filter. For instance, if the input signal is a square wave, it has a fundamental frequency and harmonics. If the fundamental frequency and all significant harmonics (approximately the first 10) are inside the passband, the square wave will have approximately the same shape at the output.

### High-Pass Filter

Figure 21-2 shows the ideal frequency response of a **high-pass filter**. A high-pass filter blocks all frequencies from zero up to the cutoff frequency and passes all frequencies above the cutoff frequency.

With a high-pass filter, the frequencies between zero and the cutoff frequency are the **stopband**. The frequencies above the cutoff frequency are the **passband**. An ideal high-pass filter has infinite attenuation in the stopband, zero attenuation in the passband, and a vertical transition.

Figure 21-1 Ideal low-pass response.

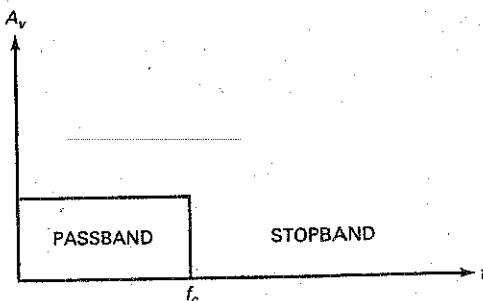
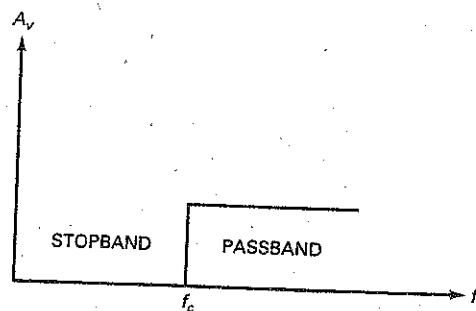


Figure 21-2 Ideal high-pass response.



### Bandpass Filter

A bandpass filter is useful when you want to tune in a radio or television signal. It is also useful in telephone communications equipment for separating the different phone conversations that are being simultaneously transmitted over the same communication path.

Figure 21-3 shows the ideal frequency response of a bandpass filter. A brick wall response like this blocks all frequencies from zero up to the lower cutoff frequency. Then, it passes all the frequencies between the lower and upper cutoff frequencies. Finally, it blocks all frequencies above the upper cutoff frequency.

With a bandpass filter, the passband is all the frequencies between the lower and upper cutoff frequencies. The frequencies below the lower cutoff frequency and above the upper cutoff frequency are the stopband. An ideal bandpass filter has zero attenuation in the passband, infinite attenuation in the stopband, and two vertical transitions.

The *bandwidth (BW)* of a bandpass filter is the difference between its upper and lower 3-dB cutoff frequencies:

$$BW = f_2 - f_1 \quad (21-1)$$

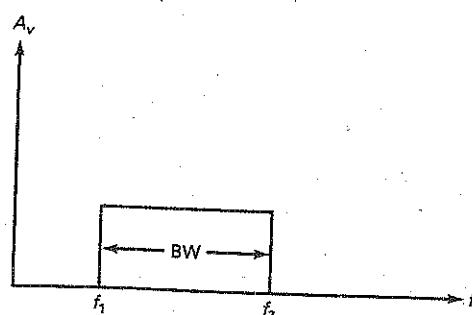
For instance, if the cutoff frequencies are 450 and 460 kHz, the bandwidth is:

$$BW = 460 \text{ kHz} - 450 \text{ kHz} = 10 \text{ kHz}$$

As another example, if the cutoff frequencies are 300 and 3300 Hz, the bandwidth is:

$$BW = 3300 \text{ Hz} - 300 \text{ Hz} = 3000 \text{ Hz}$$

Figure 21-3 Ideal bandpass response.



The center frequency is symbolized by  $f_0$  and is given by the geometric average of the two cutoff frequencies:

$$f_0 = \sqrt{f_1 f_2} \quad (21-2)$$

For instance, telephone companies use a bandpass filter with cutoff frequencies of 300 and 3300 Hz to separate phone conversations. The center frequency of these filters is:

$$f_0 = \sqrt{(300 \text{ Hz})(3300 \text{ Hz})} = 995 \text{ Hz}$$

To avoid interference between different phone conversations, the bandpass filters have responses that approach the brick wall response shown in Fig. 21-3.

The  $Q$  of a bandpass filter is defined as the center frequency divided by the bandwidth:

$$Q = \frac{f_0}{\text{BW}} \quad (21-3)$$

For instance, if  $f_0 = 200 \text{ kHz}$  and  $\text{BW} = 40 \text{ kHz}$ , then  $Q = 5$ .

When the  $Q$  is greater than 10, the center frequency can be approximated by the *arithmetic average* of the cutoff frequencies:

$$f_0 \approx \frac{f_1 + f_2}{2}$$

For instance, in a radio receiver the cutoff frequencies of the bandpass filter (IF stage) are 450 and 460 kHz. The center frequency is approximately:

$$f_0 \approx \frac{450 \text{ kHz} + 460 \text{ kHz}}{2} = 455 \text{ kHz}$$

If  $Q$  is less than 1, the bandpass filter is called a **wideband filter**. If  $Q$  is greater than 1, the filter is called a **narrowband filter**. For example, a filter with cutoff frequencies of 95 and 105 kHz has a bandwidth of 10 kHz. This is a narrowband because  $Q$  is approximately 10. A filter with cutoff frequencies of 300 and 3300 Hz has a center frequency of approximately 1000 Hz and a bandwidth of 3000 Hz. This is wideband because  $Q$  is approximately 0.333.

### Bandstop Filter

Figure 21-4 shows the ideal frequency response of a **bandstop filter**. This type of filter passes all frequencies from zero up to the lower cutoff frequency. Then, it blocks all the frequencies between the lower and upper cutoff frequencies. Finally, it passes all frequencies above the upper cutoff frequency.

**Figure 21-4** Ideal bandstop response.

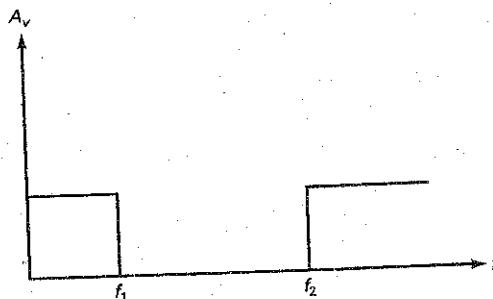
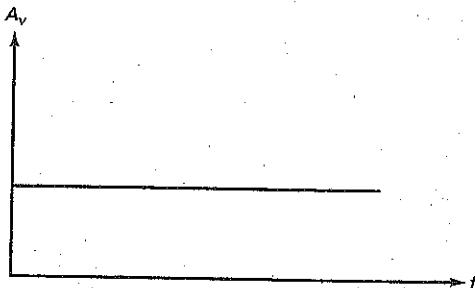


Figure 21-5 Ideal all-pass response.



With a bandstop filter, the stopband is all the frequencies between the lower and upper cutoff frequencies. The frequencies below the lower cutoff frequency and above the upper cutoff frequency are the passband. An ideal bandstop filter has infinite attenuation in the stopband, no attenuation in the passband, and two vertical transitions.

The definitions for bandwidth, narrowband, and center frequency are the same as before. In other words, with a bandstop filter, we use Eqs. (21-1) through (21-3) to calculate BW,  $f_0$ , and  $Q$ . Incidentally, the bandstop filter is sometimes called a *notch filter* because it notches out or removes all frequencies in the stopband.

### All-Pass Filter

Figure 21-5 shows the frequency response of an ideal all-pass filter. It has a passband and no stopband. Because of this, it passes all frequencies between zero and infinite frequency. It may seem rather unusual to call it a filter since it has zero attenuation for all frequencies. The reason it is called a filter is because of the effect it has on the *phase* of signals passing through it. The all-pass filter is useful when we want to produce a certain amount of phase shift for the signal being filtered without changing its amplitude.

The *phase response of a filter* is defined as the graph of phase shift versus frequency. As mentioned earlier, the ideal low-pass filter has a phase response of  $0^\circ$  at all frequencies. Because of this, a nonsinusoidal input signal has the same shape after passing through an ideal low-pass filter, provided its fundamental frequency and all significant harmonics are in the passband.

The phase response of an all-pass filter is different from that of the ideal low-pass filter. With the all-pass filter, each distinct frequency can be shifted by a certain amount as it passes through the filter. For instance, the phase shifter discussed in Sec. 20-3 was a noninverting op-amp circuit with zero attenuation at all frequencies but an output phase angle between  $0$  and  $-180^\circ$ . The phase shifter is a simple example of an all-pass filter. In later sections, we will discuss more complicated all-pass filters that can produce larger phase shifts.

## 21-2 Approximate Responses

The ideal responses discussed in the preceding section are impossible to realize with practical circuits, but there are five standard approximations used as compromises for the ideal responses. Each of these approximations offers an

advantage that the others do not have. The approximation chosen by a designer will depend on what is acceptable in an application.

## Attenuation

Attenuation refers to a loss of signal. With a constant input voltage, attenuation is defined as the output voltage at any frequency divided by the output voltage in the midband:

$$\text{Attenuation} = \frac{V_{\text{out}}}{V_{\text{out(mid)}}} \quad (21-3a)$$

For instance, if the output voltage is 1 V at some frequency and the output voltage in the midband is 2 V, then:

$$\text{Attenuation} = \frac{1 \text{ V}}{2 \text{ V}} = 0.5$$

Attenuation is normally expressed in decibels using this equation:

$$\text{Decibel attenuation} = 20 \log \text{attenuation} \quad (21-3b)$$

For an attenuation of 0.5, the decibel attenuation is:

$$\text{Decibel attenuation} = -20 \log 0.5 = 6 \text{ dB}$$

Because of the minus sign, decibel attenuation always is a positive number. Decibel attenuation uses the midband output voltage as a reference. Basically, we are comparing the output voltage at any frequency to the output voltage in the midband of the filter. Because attenuation is almost always expressed in decibels, we will use the term *attenuation* to mean decibel attenuation.

For instance, an attenuation of 3 dB means that the output voltage is 0.707 of its midband value. An attenuation of 6 dB means that the output voltage is 0.5 of its midband value. An attenuation of 12 dB means that the output voltage is 0.25 of its midband value. An attenuation of 20 dB means that the output voltage is 0.1 of its midband value.

## Passband and Stopband Attenuation

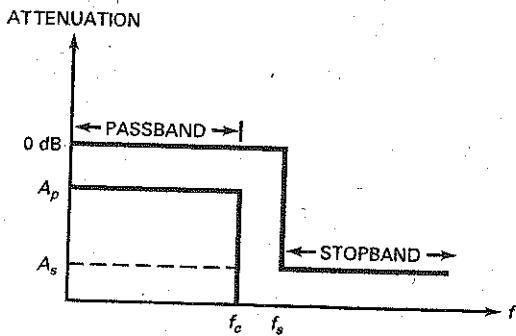
In filter analysis and design, the low-pass filter is a *prototype*, a basic circuit that can be modified to get other circuits. Typically, any filter problem is converted into an equivalent low-pass filter problem and solved as a low-pass filter problem; the solution is converted back to the original filter type. For this reason, our discussion will focus on the low-pass filter and extend the discussion to other filters.

Zero attenuation in the passband, infinite attenuation in the stopband, and a vertical transition are unrealistic. To build a practical low-pass filter, the three regions are approximated as shown in Fig. 21-6. The passband is the set of frequencies between 0 and  $f_c$ . The stopband is all the frequencies above  $f_s$ . The transition region is between  $f_c$  and  $f_s$ .

As shown in Fig. 21-6, the passband no longer has zero attenuation. Instead, we are allowing for an attenuation between 0 and  $A_p$ . For instance, in some applications the passband can have  $A_p = 0.5$  dB. This means that we are compromising the ideal response by allowing up to 0.5 dB of signal loss anywhere in the passband.

Similarly, the stopband no longer has infinite attenuation. Instead, we are allowing the stopband attenuation to be anywhere from  $A_s$  to infinity. For instance, in some applications,  $A_s = 60$  dB may be adequate. This means that we are accepting an attenuation of 60 dB or more anywhere in the stopband.

Figure 21-6 Realistic low-pass response.



In Fig. 21-6, the transition region is no longer vertical. Instead, we are accepting a nonvertical roll-off. The roll-off rate will be determined by the values of  $f_c$ ,  $f_s$ ,  $A_p$ , and  $A_s$ . For instance, if  $f_c = 1$  kHz,  $f_s = 2$  kHz,  $A_p = 0.5$  dB, and  $A_s = 60$  dB, the required roll-off is approximately 60 dB per octave.

The five approximations we are about to discuss are a trade-off between the characteristics of the passband, stopband, and transition region. The approximations may optimize the flatness of the passband, or the roll-off rate, or the phase shift.

A final point: The highest frequency in the passband of a low-pass filter is called the *cutoff frequency* ( $f_c$ ). This frequency is also referred to as the *edge frequency* because it is on the edge of the passband. In some filters, the attenuation at the edge frequency is less than 3 dB. For this reason, we will use  $f_{3dB}$  for the frequency when the attenuation is down 3 dB and  $f_c$  for the edge frequency, which may have a different attenuation.

## Order of Filter

The **order of a passive filter** (symbolized by  $n$ ) equals the number of inductors and capacitors in the filter. If a passive filter has two inductors and two capacitors,  $n = 4$ . If a passive filter has five inductors and five capacitors,  $n = 10$ . Therefore, the order tells us how complicated the filter is. The higher the order, the more complicated the filter.

The **order of an active filter** depends on the number of *RC* circuits (called *poles*) it contains. If an active filter contains eight *RC* circuits,  $n = 8$ . Counting the individual *RC* circuits in an active filter is usually difficult. Therefore, we will use a simpler method to determine the order of an active filter:

$$n \cong \# \text{ capacitors} \quad (21-4)$$

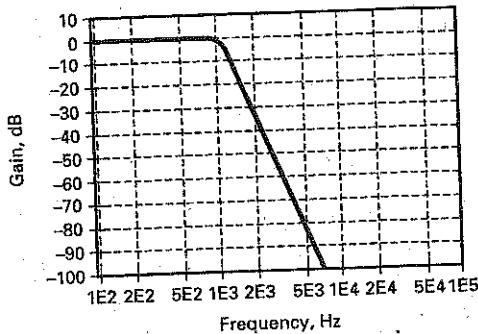
where the symbol # stands for "the number of." For instance, if an active filter contains 12 capacitors, it has an order of 12.

Bear in mind that Eq. (21-4) is a guideline. Since we are counting capacitors rather than *RC* circuits, exceptions may occur. Aside from the occasional exception, Eq. (21-4) gives us a quick and easy way to determine the order or number of poles in an active filter.

## Butterworth Approximation

The **Butterworth approximation** is sometimes called the *maximally flat approximation* because the passband attenuation is zero through most of the passband

Figure 21-7 Butterworth low-pass response.



and decreases gradually to  $A_p$  at the edge of the passband. Well above the edge frequency, the response rolls off at a rate of approximately  $20n$  dB per decade, where  $n$  is the order of the filter:

$$\text{Roll-off} = 20n \quad \text{dB/decade} \quad (21-4a)$$

An equivalent roll-off in terms of octaves is:

$$\text{Roll-off} = 6n \quad \text{dB/octave} \quad (21-4b)$$

For instance, a first-order Butterworth filter rolls off at a rate of 20 dB decade, or 6 dB per octave; a fourth-order filter rolls off at a rate of 80 dB per decade, or 24 dB per octave; a ninth-order filter rolls off at a rate of 180 dB per decade, or 54 dB per octave; and so on.

Figure 21-7 shows the response of a Butterworth low-pass filter with the following specifications:  $n = 6$ ,  $A_p = 2.5$  dB, and  $f_c = 1$  kHz. These specifications tell us that it is a sixth-order or 6-pole filter with passband attenuation of 2.5 dB and an edge frequency of 1 kHz. The numbers along the frequency axis of Fig. 21-7 are abbreviated as follows:  $2E3 = 2 \times 10^3 = 2000$ . (Note:  $E$  stands for "exponent.")

Notice how flat the response is in the passband. The major advantage of a Butterworth filter is the flatness of the passband response. The major disadvantage is the relatively slow roll-off rate compared with the other approximations.

### Chebyshev Approximation

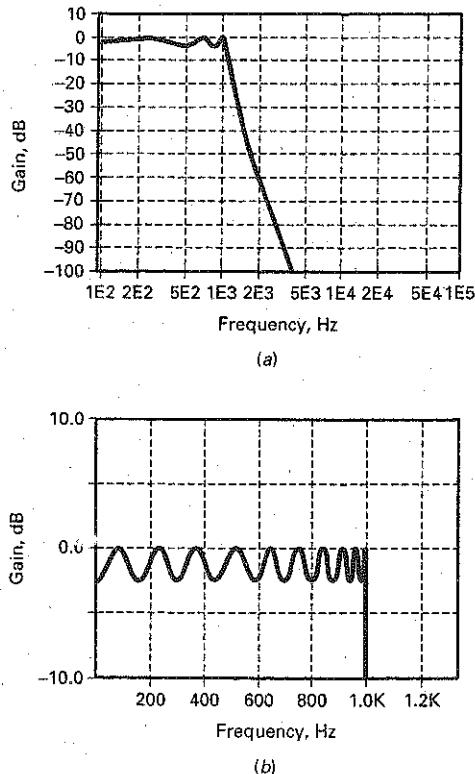
In some applications, a flat passband response is not important. In this case, a Chebyshev approximation may be preferred because it rolls off faster in the transition region than a Butterworth filter. The price paid for this faster roll-off is that ripples appear in the passband of the frequency response.

Figure 21-8a shows the response of a Chebyshev low-pass filter with the following specifications:  $n = 6$ ,  $A_p = 2.5$  dB, and  $f_c = 1$  kHz. These are the same specifications as those of the preceding Butterworth filter. When we compare Fig. 21-7 with Fig. 21-8a, we can see that a Chebyshev filter of the same order has a faster roll-off in the transition region. Because of this, the attenuation with a Chebyshev filter is always greater than the attenuation of a Butterworth filter of the same order.

The number of ripples in the passband of a Chebyshev low-pass filter equals half of the filter order:

$$\# \text{Ripples} = \frac{n}{2} \quad (21-5)$$

Figure 21-8. (a) Chebyshev low-pass response; (b) magnified view of passband ripples.



If a filter has an order of 10, it will have 5 ripples in the passband; if a filter has an order of 15, it will have 7.5 ripples. Figure 21-8b shows a magnified view of a Chebyshev response for an order of 20. It has 10 ripples in the passband.

In Fig. 21-8b, the ripples have the same peak-to-peak value. This is why the Chebyshev approximation is sometimes called the *equal-ripple approximation*. Typically, a designer will choose a ripple depth between 0.1 and 3 dB, depending on the needs of the application.

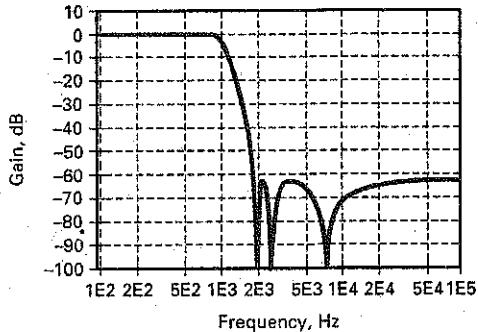
### Inverse Chebyshev Approximation

In applications in which a flat passband response is required, as well as a fast roll-off, a designer may use the **inverse Chebyshev approximation**. It has a flat passband response and a rippled stopband response. The roll-off rate in the transition region is comparable to the roll-off rate of a Chebyshev filter.

Figure 21-9 shows the response of an inverse Chebyshev low-pass filter with the following specifications:  $n = 6$ ,  $A_p = 2.5$  dB, and  $f_c = 1$  kHz. When we compare Fig. 21-9 with Figs. 21-7 and 21-8a, we can see that the inverse Chebyshev filter has a flat passband, a fast roll-off, and a rippled stopband.

**Monotonic** means that the stopband has no ripples. With the approximations discussed so far, the Butterworth and Chebyshev filters have monotonic stopbands. The inverse Chebyshev has a rippled stopband.

**Figure 21-9** Inverse Chebyshev low-pass response.



When specifying an inverse Chebyshev filter, the minimum acceptable attenuation throughout the stopband must be given because the stopband has ripples that may reach this value. For instance, in Fig. 21-9, the inverse Chebyshev filter has a stopband attenuation of 60 dB. As you can see, the ripples do approach this level at different frequencies in the stopband.

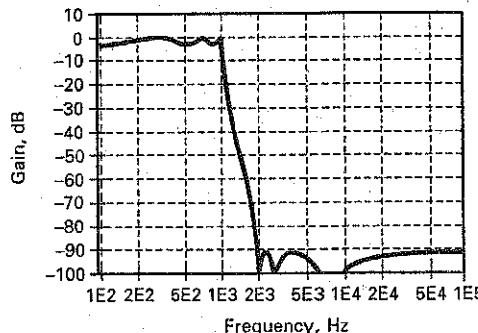
The unusual stopband response of Fig. 21-9 occurs because the inverse Chebyshev filter has components that notch the response at certain frequencies in the stopband. In other words, there are frequencies in the stopband at which the attenuation approaches infinity.

### Elliptic Approximation

Some applications need the fastest possible roll-off in the transition region. If a rippled passband and a rippled stopband are acceptable, a designer may choose the **elliptic approximation**. Also known as the *Cauer filter*, this filter optimizes the transition region at the expense of the passband and stopband.

Figure 21-10 shows the response of an elliptic low-pass filter with the same specifications as before:  $n = 6$ ,  $A_p = 2.5$  dB, and  $f_c = 1$  kHz. Notice that the elliptic filter has a rippled passband, a very fast roll-off, and a rippled stopband. After the response breaks at the edge frequency, the initial roll-off is very rapid, slows down slightly in the middle of the transition, and then becomes very rapid toward the end of the transition. Given a set of specifications for any complicated filter, the elliptic approximation will always produce the most efficient design; that is, it will have the lowest order.

**Figure 21-10** Elliptic low-pass response.



For instance, suppose we are given the following specifications:  $A_p = 0.5$  dB,  $f_c = 1$  kHz,  $A_s = 60$  dB, and  $f_s = 1.5$  kHz. Here are the required orders or number of poles for each of the approximations: Butterworth (20), Chebyshev (9), inverse Chebyshev (9), and elliptic (6). In other words, the elliptic filter requires the fewest capacitors, which translates to the simplest circuit.

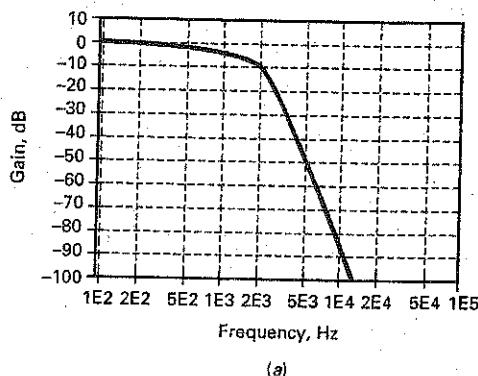
## Bessel Approximation

The Bessel approximation has a flat passband and a monotonic stopband similar to those of the Butterworth approximation. For the same filter order, however, the roll-off in the transition region is much less with a Bessel filter than with a Butterworth filter.

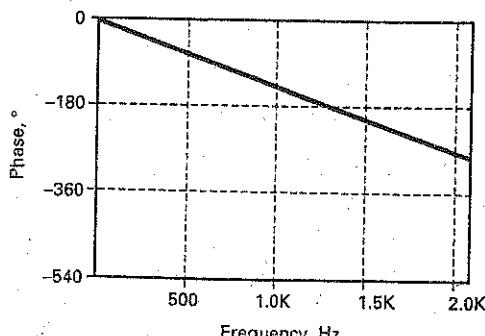
Figure 21-11a shows the response of a Bessel low-pass filter with the same specifications as before:  $n = 6$ ,  $A_p = 2.5$  dB, and  $f_c = 1$  kHz. Notice that the Bessel filter has a flat passband, a relatively slow roll-off, and a monotonic stopband. Given a set of specifications for a complicated filter, the Bessel approximation will always produce the least roll-off of all the approximations. Stated another way: It has the highest order or greatest circuit complexity of all approximations.

Why is the order of a Bessel filter the highest for the same specifications? Because the Butterworth, Chebyshev, inverse Chebyshev, and elliptic approximations are optimized for frequency response only. With these approximations, no

**Figure 21-11** (a) Bessel low-pass frequency response; (b) Bessel low-pass phase response.



(a)



(b)

attempt is made to control the phase of the output signal. On the other hand, the Bessel approximation is optimized to produce a **linear phase shift** with frequency. In other words, the Bessel filter trades off some of the roll-off rate to get a linear phase shift.

Why bother with a linear phase shift? Recall the earlier discussion of the ideal low-pass filter. One of its ideal properties was a phase shift of  $0^\circ$ . This was desirable because it meant that the shape of a nonsinusoidal signal would be preserved as it passed through the filter. With a Bessel filter, we cannot get a phase shift of  $0^\circ$ , but we can get a linear phase response. This is a phase response in which the phase shift increases linearly with frequency.

Figure 21-11b shows the phase response of a Bessel filter with  $n = 6$ ,  $A_p = 2.5$  dB, and  $f_c = 1$  kHz. As you can see, the phase response is linear. The phase shift is approximately  $14^\circ$  at 100 Hz,  $28^\circ$  at 200 Hz,  $42^\circ$  at 300 Hz, and so on. This linearity exists through the entire passband and somewhat beyond. At higher frequencies, the phase response becomes nonlinear, but that is not what matters. What counts is the linear phase response to all frequencies in the passband.

The linear phase shift for all frequencies in the passband means that the fundamental frequency and harmonics of a nonsinusoidal input signal will shift linearly in phase as they pass through the filter. Because of this, the shape of the output signal will be the same as the shape of the input signal.

The major advantage of the Bessel filter is that it produces the least distortion of nonsinusoidal signals. One easy way to measure this type of distortion is by the step response of the filter. This means applying a voltage step to the input and looking at the output with an oscilloscope. The Bessel filter has the best step response of all the filters.

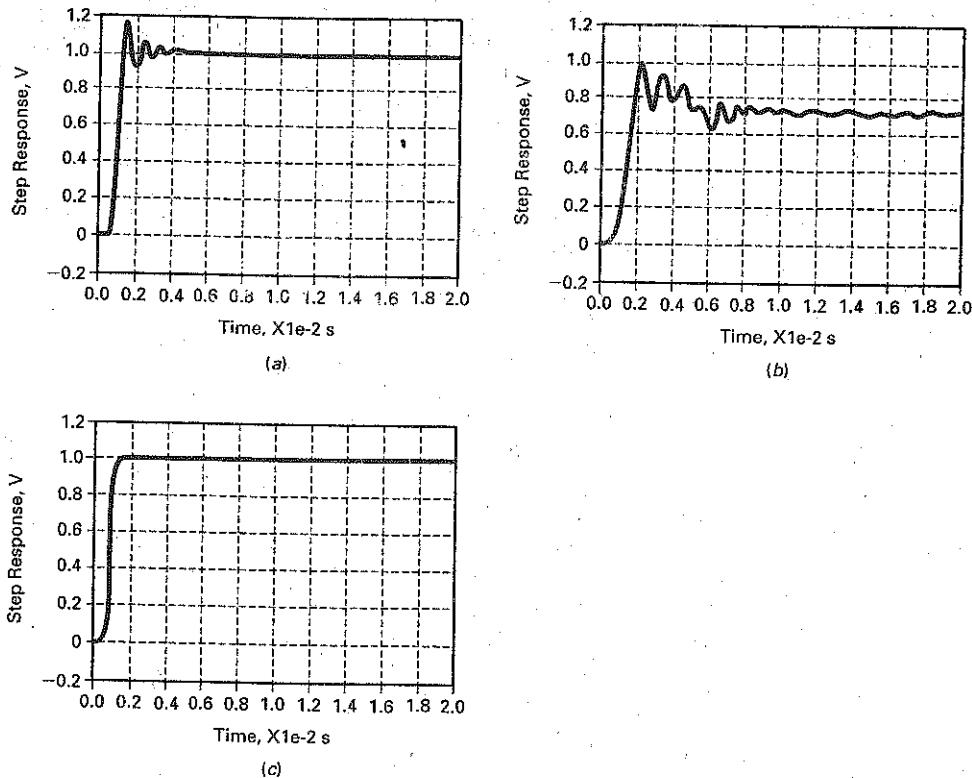
Figure 21-12a to c shows the different step responses for a low-pass filter with  $A_p = 3$  dB,  $f_c = 1$  kHz, and  $n = 10$ . Notice how the step response of a Butterworth filter (Fig. 21-12a) overshoots the final level, rings a couple of times, and then settles on the final value of 1 V. A step response like this might be acceptable in some applications, but it is not ideal. The step response of a Chebyshev filter (Fig. 21-12b) is worse. It overshoots and rings many times before settling on its final value. A step response like this is far from ideal and not acceptable in some applications. The step response of the inverse Chebyshev filter is similar to that of the Butterworth because both responses are maximally flat in the passband. The step response of the elliptic filter is similar to that of the Chebyshev because both responses have rippled passbands.

Figure 21-12c shows the step response of a Bessel filter. This is almost an ideal reproduction of an input voltage step. The only deviation from a perfect step is the risetime. The Bessel step response has no noticeable overshoot or ringing. Since digital data consist of positive and negative steps, a clean step response like that shown in Fig. 21-12c is preferred to the distortion of Fig. 21-12a and b. For this reason, the Bessel filter may be used in some data communication systems.

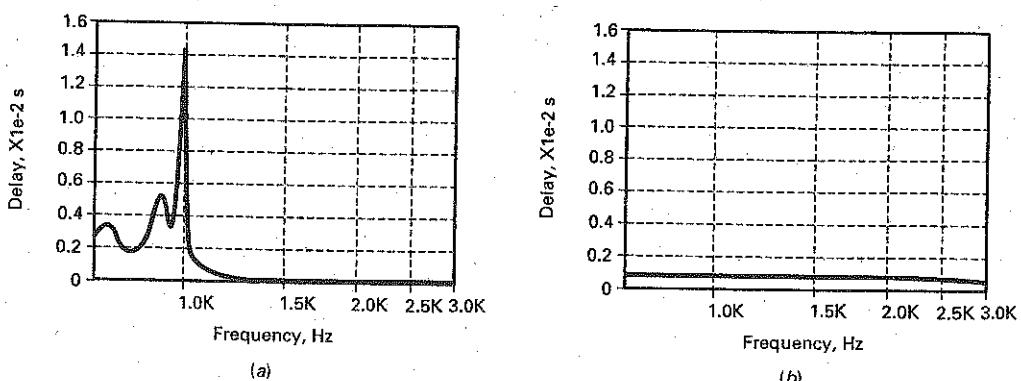
A linear phase response implies a *constant time delay*, which means that all frequencies in the passband are delayed by the same amount of time as they pass through the filter. The amount of time it takes for a signal to pass through a filter depends on the order of the filter. With all filters except the Bessel filter, this amount of time changes with the frequency. With the Bessel filter, the time delay is constant at all frequencies in the passband.

As an illustration, Fig. 21-13a shows the time delay for an elliptic filter with  $A_p = 3$  dB,  $f_c = 1$  kHz, and  $n = 10$ . Notice how the time delay changes with frequency. Figure 21-13b shows the time delay of a Bessel filter with the same specifications. Notice how the time delay is constant through the passband and beyond. This is why the Bessel filter is sometimes referred to as a *maximally flat delay filter*. Constant time delay implies linear phase shift, and vice versa.

**Figure 21-12** Step responses: (a) Butterworth and inverse Chebyshev; (b) Chebyshev and elliptic; (c) Bessel.



**Figure 21-13** Time delays: (a) Elliptic; (b) Bessel.



### Roll-off of Different Approximations

The Butterworth roll-off rate is neatly summarized by Eqs. (21-4a) and (21-4b):

$$\text{Roll off} = 20n \quad \text{dB/decade}$$

$$\text{Roll off} = 6n \quad \text{dB/octave}$$

The Chebyshev, inverse Chebyshev, and elliptic approximations have faster roll-offs in the transition region, but the Bessel has a slower roll-off.

Table 21-1

Attenuation for Sixth-Order Approximations

Type	$f_c$ , dB	$2f_c$ , dB
Bessel	3	14
Butterworth	3	36
Chebyshev	3	63
Inverse Chebyshev	3	63
Elliptic	3	93

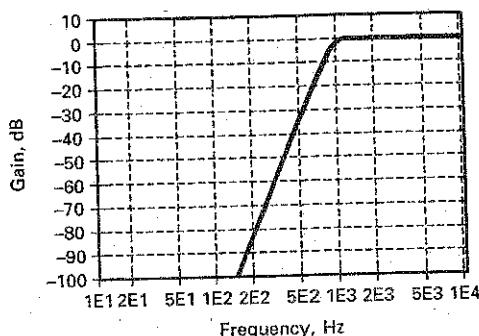
The transition roll-off rates of non-Butterworth filters cannot be summarized with simple equations because the roll-offs are nonlinear and depend on the filter order, the ripple depth, and the other factors. Although we cannot write equations for these nonlinear roll-offs, we can compare the different roll-off rates in the transition region as follows.

Table 21-1 shows the attenuation for  $n = 6$  and  $A_p = 3$  dB. The filters have been ranked by their attenuations 1 octave above the edge frequency. The Bessel filter has the slowest roll-off, the Butterworth filter is next, and so on. All filters with rippled passbands or stopbands have transition roll-off rates that are faster than those of the Bessel and Butterworth filters, which have no ripples in their frequency response.

### Other Types of Filters

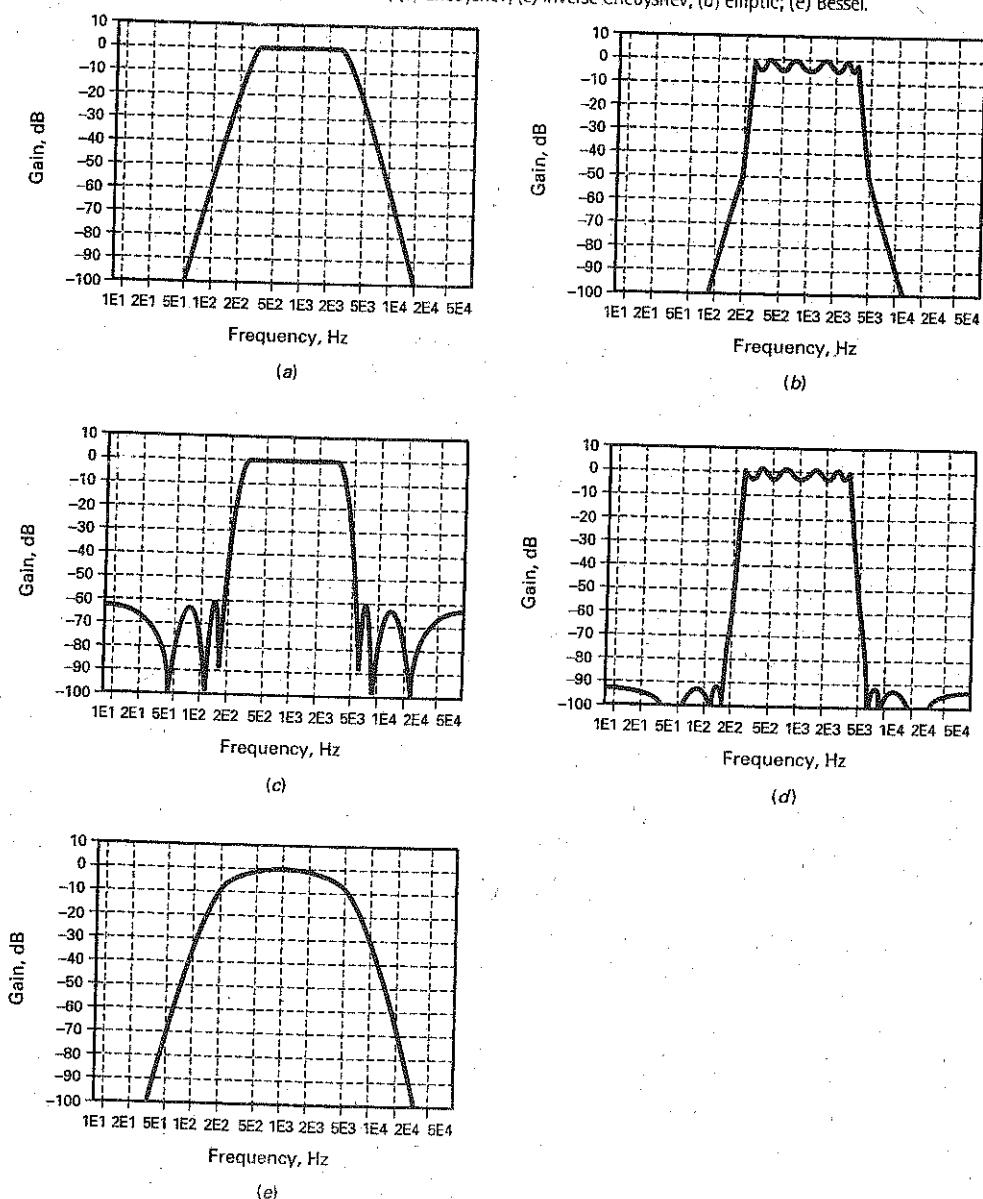
Most of the preceding discussion applies to the high-pass, bandpass, and bandstop filters. The approximations for a high-pass filter are the same as those for a low-pass filter, except that the responses are rotated horizontally around the edge frequency. For instance, Fig. 21-14 shows the Butterworth response for a high-pass filter with  $n = 6$ ,  $A_p = 2.5$  dB, and  $f_c = 1$  kHz. This is a mirror image of the low-pass response discussed earlier. The Chebyshev, inverse Chebyshev, elliptic, and Bessel high-pass responses are likewise mirror images of their low-pass counterparts.

Figure 21-14 Butterworth high-pass response.



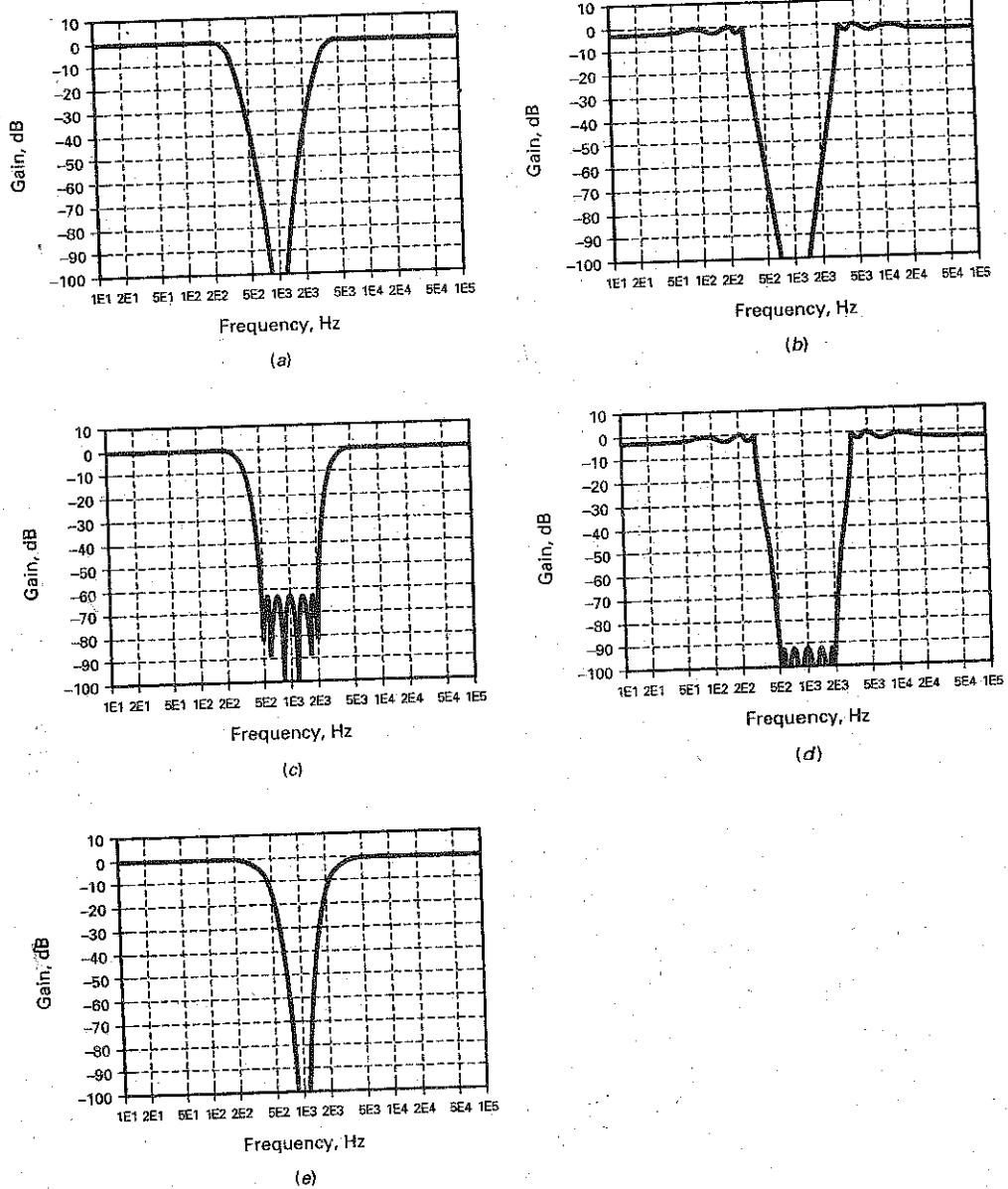
The bandpass responses are different. Here are the specifications used for the following examples:  $n = 12$ ,  $A_p = 3$  dB,  $f_0 = 1$  kHz, and  $\text{BW} = 3$  kHz. Figure 21-15a shows the Butterworth response. As expected, the passband is maximally flat and the stopband is monotonic. The Chebyshev response of Fig. 21-15b shows a rippled passband and a monotonic stopband. There are six passband ripples, half the order, which agrees with Eq. (21-5). Figure 21-15c is the response for an inverse Chebyshev filter. Here we see the flat passband and a rippled stopband. Figure 21-15d shows the elliptic response with its rippled passband and rippled stopband. Finally, Fig. 21-15e shows the Bessel response.

**Figure 21-15** Bandpass responses: (a) Butterworth; (b) Chebyshev; (c) inverse Chebyshev; (d) elliptic; (e) Bessel.



The bandstop responses are the opposite of the bandpass responses. Here are the bandstop responses for  $n = 12$ :  $A_p = 3B$ ,  $f_0 = 1$  kHz, and  $\text{BW} = 3$  kHz. Figure 21-16a shows the Butterworth response. As expected, the passband is maximally flat and the stopband is monotonic. The Chebyshev response of Fig. 21-16b shows a rippled passband and a monotonic stopband. Figure 21-16c is the response for an inverse Chebyshev filter. Here we see a flat passband and a rippled stopband. Figure 21-16d shows the elliptic response with its rippled passband and rippled stopband. Finally, Fig. 21-16e shows the bandstop response for a Bessel filter.

Figure 21-16 Bandstop responses: (a) Butterworth; (b) Chebyshev; (c) inverse Chebyshev; (d) elliptic; (e) Bessel.



**Table 21-2** Filter Approximations

Type	Passband	Stopband	Roll-off	Step response
Butterworth	Flat	Monotonic	Good	Good
Chebyshev	Rippled	Monotonic	Very good	Poor
Inverse Chebyshev	Flat	Rippled	Very good	Good
Elliptic	Rippled	Rippled	Best	Poor
Bessel	Flat	Monotonic	Poor	Best

## Conclusion

Table 21-2 summarizes the five approximations used in designing filters. Each has its advantages and disadvantages. When a flat passband is needed, the Butterworth and inverse Chebyshev filters are the logical candidates. The required roll-off, order, and other design considerations will then determine which of the two will be used.

If a rippled passband is acceptable, the Chebyshev and elliptic filters are the best candidates. Again, the required roll-off, order, and other design considerations will then determine the final choice.

When the step response is important, the Bessel filter is the logical candidate if it can meet the attenuation requirements. The Bessel approximation is the only one shown in the table that preserves the shape of a nonsinusoidal signal. This is critical in data communications because digital signals consist of positive and negative steps.

In applications in which a Bessel filter cannot provide sufficient attenuation, we can cascade an all-pass filter with a non-Bessel filter. When properly designed, the all-pass filter can linearize the overall phase response to get an almost perfect step response. A later section discusses this in more detail.

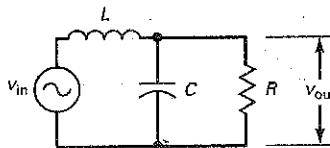
Op-amp circuits with resistors and capacitors can implement any of the five approximations. As we will see, many different circuits are available that offer a trade-off between complexity of design, sensitivity of components, and ease of tuning. For instance, some second-order circuits use only one op amp and a few components. But these simple circuits have cutoff frequencies that are heavily dependent on component tolerance and drift. Other second-order circuits may use three or more op amps, but these complex circuits are much less dependent on component tolerance and drift.

---

## 21-3 Passive Filters

Before discussing active-filter circuits, there are two more ideas that we need to explore. A second-order low-pass *LC* filter has a resonant frequency and a *Q*—similar to a series or parallel resonant circuit. By keeping the resonant frequency constant but varying the *Q*, we can get ripples to appear in the passband of higher-order filters. This section will describe the concept because it explains a great deal about the operation of active filters.

Figure 21-17 Second-order LC filter.



### Resonant Frequency and Q

Figure 21-17 shows a low-pass *LC* filter. It has an order of 2 because it contains two reactive components, an inductor and a capacitor. A second-order *LC* filter has a resonant frequency and a *Q* defined as follows:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (21-6)$$

$$Q = \frac{R}{X_L} \quad (21-7)$$

where  $X_L$  is calculated at the resonant frequency.

For instance, the filter of Fig. 21-18a has a resonant frequency and *Q* of:

$$f_0 = \frac{1}{2\pi\sqrt{(9.55 \text{ mH})(2.65 \mu\text{F})}} = 1 \text{ kHz}$$

$$Q = \frac{600 \Omega}{2\pi(1 \text{ kHz})(9.55 \text{ mH})} = 10$$

Figure 21-18b shows the frequency response. Notice how the response peaks at 1 kHz, the resonant frequency of the filter. Notice also how the voltage gain increases 20 dB at 1 kHz. The higher *Q* is, the greater the increase in voltage gain at the resonant frequency.

The filter of Fig. 21-18c has a resonant frequency and a *Q* of:

$$f_0 = \frac{1}{2\pi\sqrt{(47.7 \text{ mH})(531 \text{ nF})}} = 1 \text{ kHz}$$

$$Q = \frac{600 \Omega}{2\pi(1 \text{ kHz})(47.7 \text{ mH})} = 2$$

In Fig. 21-18c, the inductance has been increased by a factor 5 and the capacitance has been decreased by a factor of 5 from the values of Fig. 21-18a. Because the *LC* product is the same, the resonant frequency is still 1 kHz.

On the other hand, *Q* has decreased by a factor of 5 since it is inversely proportional to inductance. Figure 21-18d shows the frequency response. Notice how the response again peaks at 1 kHz, but the increase in voltage gain is only 6 dB, a result of the lower *Q*.

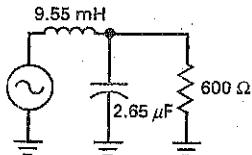
If we continue to decrease *Q*, the resonant peak will disappear. For instance, the filter of Fig. 21-18e has:

$$f_0 = \frac{1}{2\pi\sqrt{(135 \text{ mH})(187 \text{ nF})}} = 1 \text{ kHz}$$

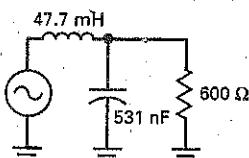
$$Q = \frac{600 \Omega}{2\pi(1 \text{ kHz})(135 \text{ mH})} = 0.707$$

Figure 21-18f shows the frequency response, which is a Butterworth response. With *Q* of 0.707, the resonant peak disappears and the passband becomes maximally flat. Any second-order filter with a *Q* of 0.707 always has a Butterworth response.

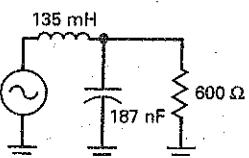
Figure 21-18 Examples.



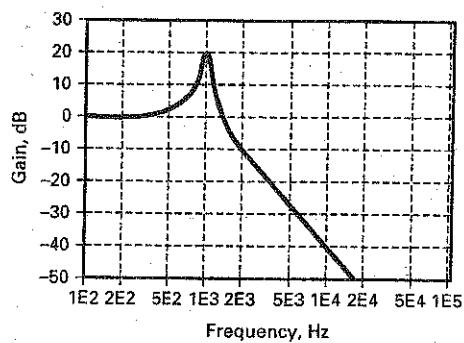
(a)



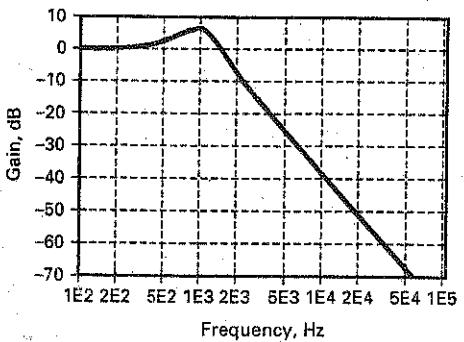
(c)



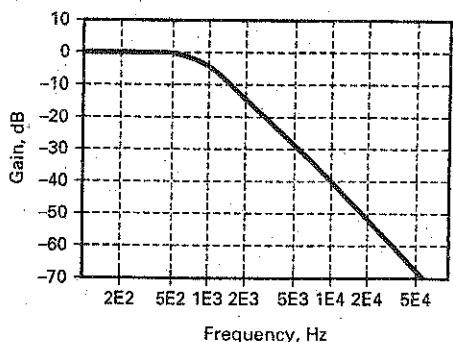
(e)



(b)



(d)



(f)

## Damping Factor

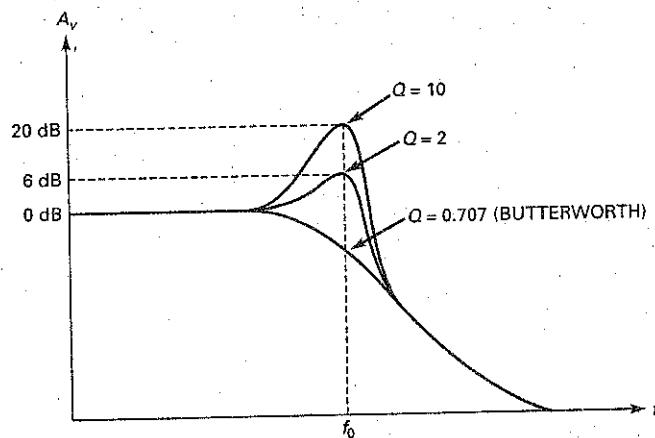
Another way of explaining the peaking action at resonance is to use the **damping factor**, defined as:

$$\alpha = \frac{1}{Q} \quad (21-8)$$

For  $Q = 10$ , the damping factor is:

$$\alpha = \frac{1}{10} = 0.1$$

Figure 21-19 Effect of  $Q$  on second-order response.



Similarly, a  $Q$  of 2 gives  $\alpha = 0.5$ , and a  $Q$  of 0.707 gives  $\alpha = 1.414$ .

Figure 21-18b has a low damping factor, only 0.1. In Fig. 21-18d, the damping factor increases to 0.5 and the resonant peak decreases. In Fig. 21-18f, the damping factor increases to 1.414 and the resonant peak disappears. As the word implies, *damping* means "reducing" or "diminishing." The higher the damping factor, the smaller the peak.

### Butterworth and Chebyshev Responses

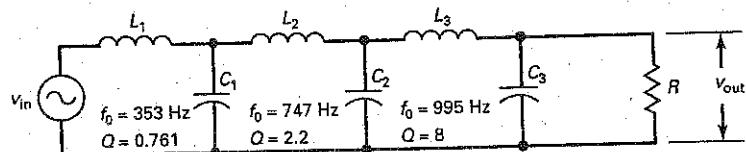
Figure 21-19 summarizes the effect of  $Q$  on a second-order filter. As indicated in Fig. 21-19, a  $Q$  of 0.707 produces the Butterworth or maximally flat response. A  $Q$  of 2 produces a ripple depth of 6 dB, and a  $Q$  of 10 produces a ripple depth of 20 dB. In terms of damping, the Butterworth response is *critically damped*, whereas the rippled responses are *underdamped*. A Bessel response (not shown) is *overdamped* because its  $Q$  equals 0.577.

### Higher-Order LC Filters

Higher-order filters are usually built by cascading second-order stages. For example, Fig. 21-20 shows a Chebyshev filter with an edge frequency of 1 kHz and a ripple depth of 1 dB. The filter consists of three second-order stages, which means that the overall filter has an order of 6. Since  $n = 6$ , the filter has three passband ripples.

Notice how each stage has its own resonant frequency and  $Q$ . The staggered resonant frequencies produce the three ripples in the passband. The staggered  $Q$ s maintain a ripple depth of 1 dB by producing peaks at frequencies at which other stages have rolled off. For instance, the second stage has a resonant frequency of 747 Hz. At this frequency, the first stage has rolled off because its cutoff frequency is 353 Hz. The second stage compensates for the roll-off in the

Figure 21-20 Staggered resonant frequencies and  $Q$ s in higher-order filter.



first stage by producing a resonant peak at 747 Hz. Similarly, the third stage has a cutoff frequency of 995 Hz. At this frequency, the first and second stages have rolled off, but the third stage compensates for their roll-offs by producing a high-Q peak at 995 Hz.

The idea of staggering the resonant frequencies and  $Q$ s of second-order stages applies to active filters as well as to passive filters. In other words, to build a high-order active filter, we can cascade second-order stages whose resonant frequencies and  $Q$ s are staggered in precisely the right way to get the desired overall response.

## 21-4 First-Order Stages

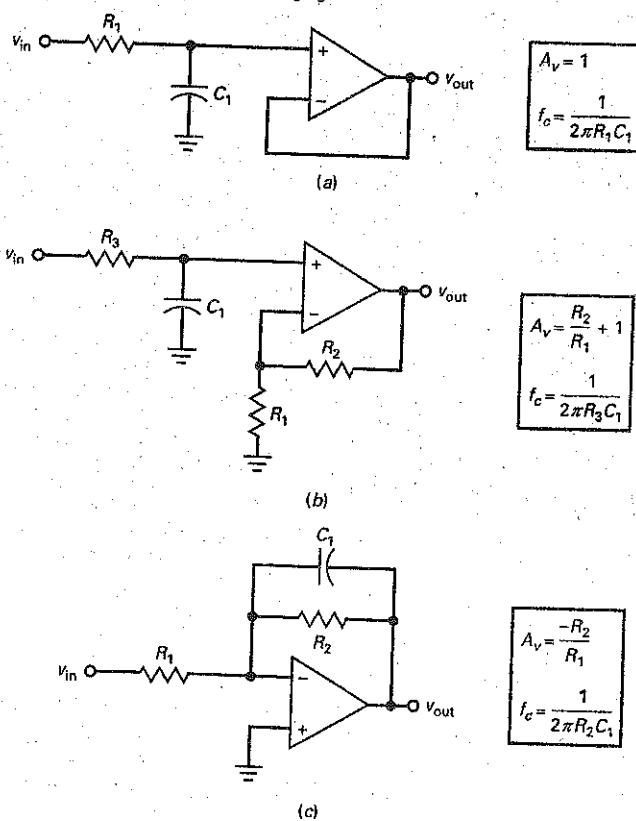
First-order or 1-pole active-filter stages have only one capacitor. Because of this, they can produce only a low-pass or a high-pass response. Bandpass and bandstop filters can be implemented only when  $n$  is greater than 1.

### Low-Pass Stage

Figure 21-21a shows the simplest way to build a first-order low-pass active filter. It is nothing more than an  $RC$  lag circuit and a voltage follower. The voltage gain is:

$$A_v = 1$$

**Figure 21-21** First-order low-pass stages: (a) Noninverting unity gain; (b) noninverting with voltage gain; (c) inverting with voltage gain.



### GOOD TO KNOW

In Fig. 21-21a, the op amp isolates the load from the  $RC$  low-pass filter at the input.

The 3-dB cutoff frequency is given by:

$$f_c = \frac{1}{2\pi R_1 C_1} \quad (21-9)$$

When the frequency increases above the cutoff frequency, the capacitive reactance decreases and reduces the noninverting input voltage. Since the  $R_1C_1$  lag circuit is outside the feedback loop, the output voltage rolls off. As the frequency approaches infinity, the capacitor becomes a short and there is zero input voltage.

Figure 21-21b shows another noninverting first-order low-pass filter. Although it has two additional resistors, it has the advantage of voltage gain. The voltage gain well below the cutoff frequency is given by:

$$A_v = \frac{R_2}{R_1} + 1 \quad (21-10)$$

The cutoff frequency is given by:

$$f_c = \frac{1}{2\pi R_3 C_1} \quad (21-11)$$

Above the cutoff frequency, the lag circuit reduces the noninverting input voltage. Since the  $R_3C_1$  lag circuit is outside the feedback loop, the output voltage rolls off at a rate of 20 dB per decade.

Figure 21-21c shows an inverting first-order low-pass filter and its equations. At low frequencies, the capacitor appears to be open and the circuit acts like an inverting amplifier with a voltage gain of:

$$A_v = -\frac{R_2}{R_1} \quad (21-12)$$

As the frequency increases, the capacitive reactance decreases and reduces the impedance of the feedback branch. This implies less voltage gain. As the frequency approaches infinity, the capacitor becomes a short and there is no voltage gain. As shown in Fig. 21-21c, the cutoff frequency is given by:

$$f_c = \frac{1}{2\pi R_2 C_1} \quad (21-13)$$

There is no other way to implement a first-order low-pass filter. In other words, the circuits shown in Fig. 21-21 are the only three configurations available for an active-filter low-pass stage.

A final point about all first-order stages. They can implement only a Butterworth response. The reason is that a first-order stage has no resonant frequency. Therefore, it cannot produce the peaking that produces a rippled passband. This means that all first-order stages are maximally flat in the passband and monotonic in the stopband, and they roll off at a rate of 20 dB per decade.

## High-Pass Stage

Figure 21-22a shows the simplest way to build a first-order high-pass active filter. The voltage gain is:

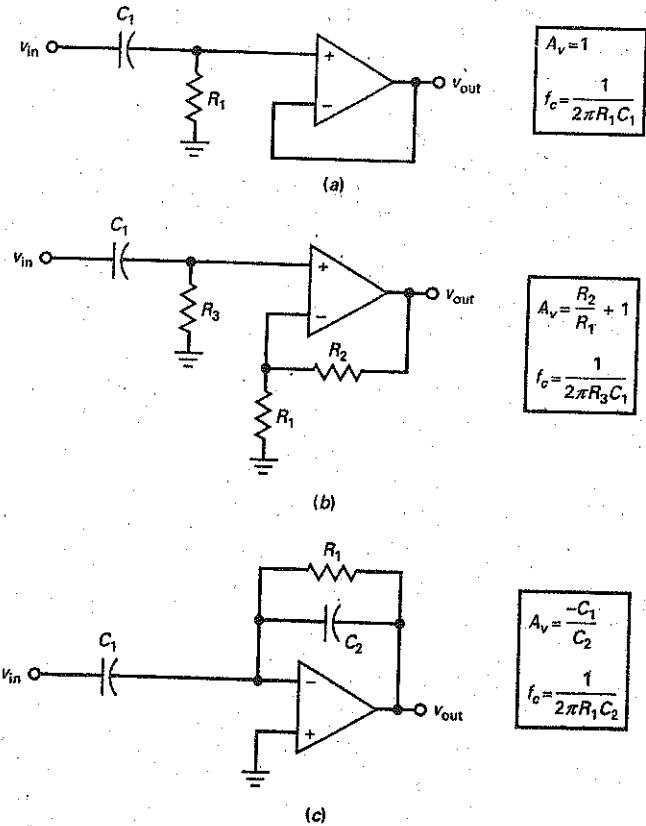
$$A_v = 1$$

The 3-dB cutoff frequency is given by:

$$f_c = \frac{1}{2\pi R_1 C_1} \quad (21-14)$$

When the frequency decreases below the cutoff frequency, the capacitive reactance increases and reduces the noninverting input voltage. Since the  $R_1C_1$  circuit is

**Figure 21-22** First-order high-pass stages: (a) Noninverting unity gain; (b) noninverting with voltage gain; (c) inverting with voltage gain.



outside the feedback loop, the output voltage rolls off. As the frequency approaches zero, the capacitor becomes an open and there is zero input voltage.

Figure 21-22b shows another noninverting first-order high-pass filter. The voltage gain well above the cutoff frequency is given by:

$$A_v = \frac{R_2}{R_1} + 1 \quad (21-15)$$

The 3-dB cutoff frequency is given by:

$$f_c = \frac{1}{2\pi R_3 C_1} \quad (21-16)$$

Well below the cutoff frequency, the  $RC$  circuit reduces the noninverting input voltage. Since the  $R_3C_1$  lag circuit is outside the feedback loop, the output voltage rolls off at a rate of 20 dB per decade.

Figure 21-22c shows another first-order high-pass filter and its equations. At high frequencies, the circuit acts like an inverting amplifier with a voltage gain of:

$$A_v = \frac{-X_{C_2}}{X_{C_1}} = \frac{-C_1}{C_2} \quad (21-17)$$

As the frequency decreases, the capacitive reactances increase and eventually reduce the input signal and the feedback. This implies less voltage gain. As the frequency approaches zero, the capacitors become open and there is no input signal. As shown in Fig. 21-22c, the 3-dB cutoff frequency is given by:

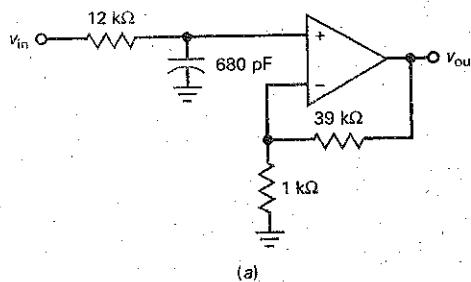
$$f_c = \frac{1}{2\pi R_1 C_2} \quad (21-18)$$

## Example 21-1

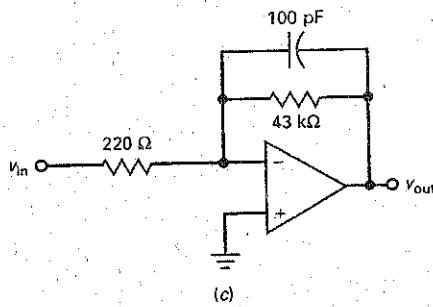
**III** **APPLICATIONS**

What is the voltage gain in Fig. 21-23a? What is the cutoff frequency? What is the frequency response?

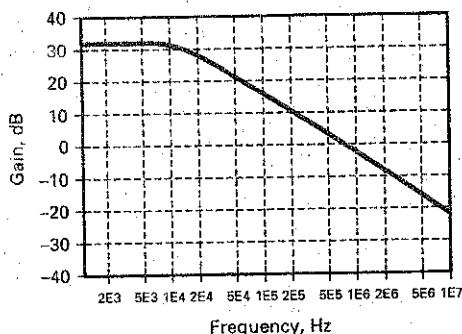
Figure 21-23 Example.



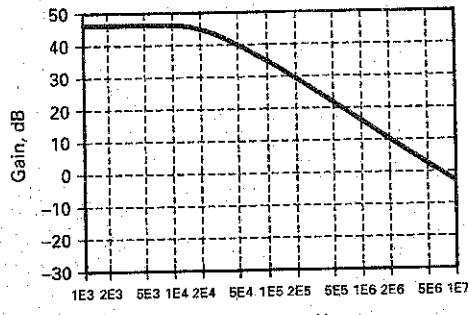
(a)



(c)



(b)



(d)

**SOLUTION** This is a noninverting first-order low-pass filter. With Eqs. (21-10) and (21-11), the voltage gain and cutoff frequencies are:

$$A_v = \frac{39 \text{ k}\Omega}{1 \text{ k}\Omega} + 1 = 40$$

$$f_c = \frac{1}{2\pi(12 \text{ k}\Omega)(680 \text{ pF})} = 19.5 \text{ kHz}$$

Figure 21-23b shows the frequency response. The voltage gain is 32 dB in the passband. The response breaks at 19.5 kHz and then rolls off at a rate of 20 dB per decade.

**PRACTICE PROBLEM 21-1** Using Fig. 21-23a, change the 12 kΩ resistor to 6.8 kΩ. Find the new cutoff frequency.

## Example 21-2

What is the voltage gain in Fig. 21-23c? What is the cutoff frequency? What is the frequency response?

**SOLUTION** This is an inverting first-order low-pass filter. With Eqs. (21-12) and (21-13), the voltage gain and cutoff frequencies are:

$$A_v = \frac{-43 \text{ k}\Omega}{220 \Omega} = -195$$

$$f_c = \frac{1}{2\pi(43 \text{ k}\Omega)(100 \text{ pF})} = 37 \text{ kHz}$$

Figure 21-23d shows the frequency response. The voltage gain is 45.8 dB in the passband. The response breaks at 37 kHz and then rolls off at a rate of 20 dB per decade.

**PRACTICE PROBLEM 21-2** In Fig. 21-23c, change the 100 pF capacitor to 220 pF. What is the new cutoff frequency?

## 21-5 VCVS Unity-Gain Second-Order Low-Pass Filters

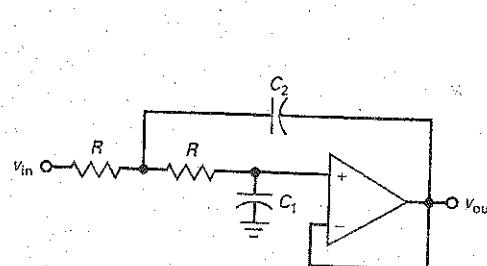
Second-order or 2-pole stages are the most common because they are easy to build and analyze. Higher-order filters are usually made by cascading second-order stages. Each second-order stage has a resonant frequency and a  $Q$  to determine how much peaking occurs.

This section discusses the **Sallen-Key low-pass filters** (named after the inventors). These filters are also called **VCVS filters** because the op amp is used as a voltage-controlled voltage source. VCVS low-pass circuits can implement three of the basic approximations: Butterworth, Chebyshev, and Bessel.

### Circuit Implementation

Figure 21-24 shows a Sallen-Key second-order low-pass filter. Notice that the two resistors have the same value, but the two capacitors are different. There is a lag

Figure 21-24 Second-order VCVS stage for Butterworth and Bessel.



$A_v = 1$
$Q = 0.5 \sqrt{\frac{C_2}{C_1}}$
$f_p = \frac{1}{2\pi R \sqrt{C_1 C_2}}$
Butterworth:
$Q = 0.707$
$K_p = 1$
Bessel:
$Q = 0.577$
$K_c = 0.786$

### GOOD TO KNOW

The study of active filters can be a bit overwhelming. Take your time when working through the examples and doing the experiments that correspond to the filters covered in this chapter.

circuit on the noninverting input, but this time there is a feedback path through a second capacitor  $C_2$ . At low frequencies, both capacitors appear to be open and the circuit has a unity gain because the op amp is connected as a voltage follower.

As the frequency increases, the impedance of  $C_1$  decreases and the noninverting input voltage decreases. At the same time, capacitor  $C_2$  is feeding back a signal that is in phase with the input signal. Since the feedback signal adds to the source signal, the feedback is *positive*. As a result, the decrease in the noninverting input voltage caused by  $C_1$  is not as large as it would be without the positive feedback.

The larger  $C_2$  is with respect to  $C_1$ , the more the positive feedback; this is equivalent to increasing the  $Q$  of the circuit. If  $C_2$  is large enough to make  $Q$  greater than 0.707, peaking appears in the frequency response.

### Pole Frequency

As shown in Fig. 21-24:

$$Q = 0.5 \sqrt{\frac{C_2}{C_1}} \quad (21-19)$$

and

$$f_p = \frac{1}{2\pi R\sqrt{C_1 C_2}} \quad (21-20)$$

The pole frequency ( $f_p$ ) is a special frequency used in the design of active filters. The mathematics behind the pole frequency is too complicated to go into here because it involves an advanced topic called the *s plane*. Advanced courses analyze and design filters using the *s plane*. (Note:  $s$  is a complex number given by  $\sigma + j\omega$ .)

For our needs, it is enough to understand how to calculate the pole frequency. In more complicated circuits, the pole frequency is given by:

$$f_p = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

In a Sallen-Key unity-gain filter,  $R_1 = R_2$  and the equation simplifies to Eq. (21-20).

### Butterworth and Bessel Responses

When analyzing a circuit like the one shown in Fig. 21-24, we start by calculating  $Q$  and  $f_p$ . If  $Q = 0.707$ , we have a Butterworth response and a  $K_c$  value of 1. If  $Q = 0.577$ , we have a Bessel response and a  $K_c$  value of 0.786. Next, we can calculate the cutoff frequency with:

$$f_c = K_c f_p \quad (21-21)$$

With Butterworth and Bessel filters, the cutoff frequency is always the frequency at which the attenuation is 3 dB.

### Peaked Response

Figure 21-25 shows how to analyze the circuit when  $Q$  is greater than 0.707. After calculating the  $Q$  and the pole frequency of the circuit, we can calculate three other frequencies with these equations:

$$f_0 = K_0 f_p \quad (21-22)$$

$$f_c = K_c f_p \quad (21-23)$$

$$f_{3dB} = K_3 f_p \quad (21-24)$$

The first of these frequencies is the resonant frequency where peaking appears. The second is the edge frequency, and the third is the 3-dB frequency.

Figure 21-25 Second-order VCVS stage for  $Q > 0.707$ .

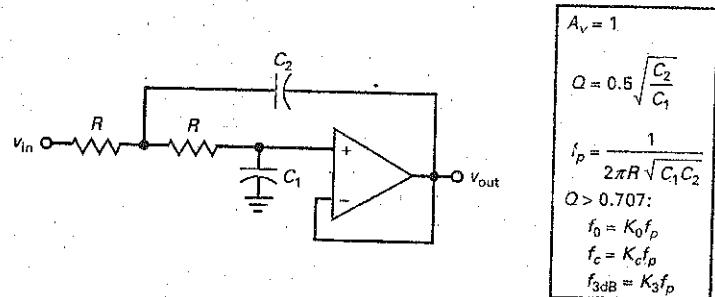
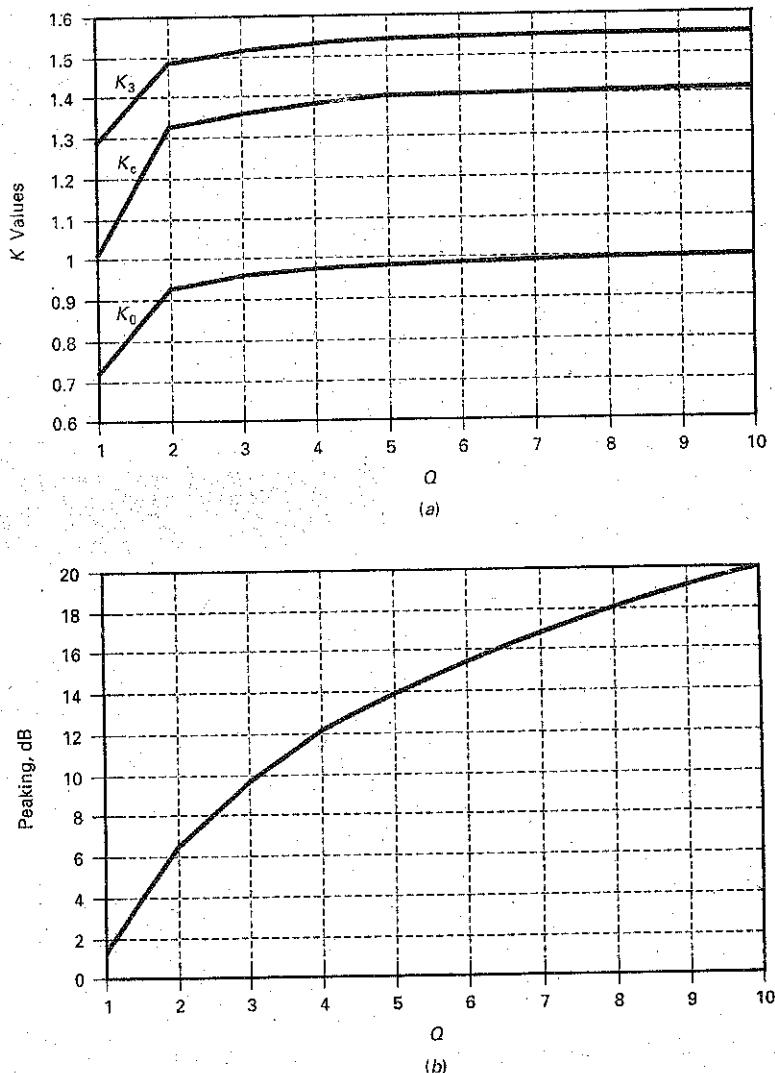


Table 21-3 shows the  $K$  and  $A_p$  values versus  $Q$ . The Bessel and Butterworth values appear first. Because these responses have no noticeable resonant frequency, the  $K_0$  and  $A_p$  values do not apply. When  $Q$  is greater than 0.707, a noticeable resonant frequency appears and all  $K$  and  $A_p$  values are present. By

Table 21-3 K Values and Ripple Depth of Second-Order Stages

$Q$	$K_0$	$K_c$	$K_3$	$A_p(\text{dB})$
0.577	—	0.786	1	—
0.707	—	1	1	—
0.75	0.333	0.471	1.057	0.054
0.8	0.467	0.661	1.115	0.213
0.9	0.620	0.874	1.206	0.688
1	0.708	1.000	1.272	1.25
2	0.935	1.322	1.485	6.3
3	0.972	1.374	1.523	9.66
4	0.984	1.391	1.537	12.1
5	0.990	1.400	1.543	14
6	0.992	1.402	1.546	15.6
7	0.994	1.404	1.548	16.9
8	0.995	1.406	1.549	18
9	0.997	1.408	1.550	19
10	0.998	1.410	1.551	20
100	1.000	1.414	1.554	40

Figure 21-26 (a)  $K$  values versus  $Q$ ; (b) peaking versus  $Q$ .



plotting the values of Table 21-3, we get Fig. 21-26a and b. We can use the table for integral values of  $Q$  and the graphs for intermediate values of  $Q$ . For instance, if we calculate a  $Q$  of 5, we can read the following approximate values from either Table 21-3 or Fig. 21-26:  $K_0 = 0.99$ ,  $K_c = 1.4$ ,  $K_3 = 1.54$ , and  $A_p = 14$  dB.

In Fig. 21-26a, notice how the  $K$  values level off as  $Q$  approaches 10. For  $Q$  greater than 10, we will use these approximations:

$$K_0 = 1 \quad (21-25)$$

$$K_c = 1.414 \quad (21-26)$$

$$K_3 = 1.55 \quad (21-27)$$

$$A_p = 20 \log Q \quad (21-28)$$

The values shown in Table 21-3 and Fig. 21-26 apply to all second-order low-pass stages.

## Gain-Bandwidth Product of Op Amps

In all our discussions about active filters, we will assume that the op amps have enough *gain-bandwidth product (GBW)* not to affect filter performance. Limited GBW increases the  $Q$  of a stage. With high cutoff frequencies, a designer must be aware of limited GBW because it may change the performance of a filter.

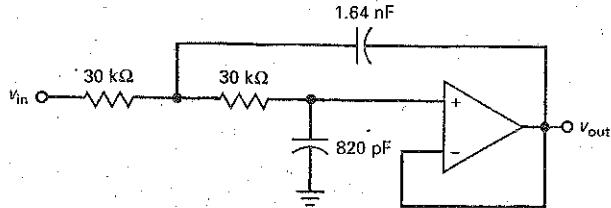
One way to correct for limited GBW is by means of **predistortion**. This refers to decreasing the design value of  $Q$  as needed to compensate for limited GBW. For instance, if a stage should have a  $Q$  of 10 and a limited GBW increases it to 11, a designer can predistort by designing the stage with a  $Q$  of 9.1. The limited GBW will increase 9.1 to 10. Designers try to avoid predistortion because low- $Q$  and high- $Q$  stages sometimes interact adversely. The best approach is to use a better op amp, one with a higher GBW (same as  $f_{\text{unity}}$ ).

## Example 21-3

Multisim

What are the pole frequency and  $Q$  of the filter shown in Fig. 21-27? What is the cutoff frequency?

Figure 21-27 Butterworth unity-gain example.



**SOLUTION** The  $Q$  and pole frequency are:

$$Q = 0.5 \sqrt{\frac{C_2}{C_1}} = 0.5 \sqrt{\frac{1.64 \text{ nF}}{820 \text{ pF}}} = 0.707$$

$$f_p = \frac{1}{2\pi R\sqrt{C_1 C_2}} = \frac{1}{2\pi(30 \text{ k}\Omega)\sqrt{(820 \text{ pF})(1.64 \text{ nF})}} = 4.58 \text{ kHz}$$

The  $Q$  value of 0.707 tells us that this is a Butterworth response, so the cutoff frequency is the same as the pole frequency:

$$f_c = f_p = 4.58 \text{ kHz}$$

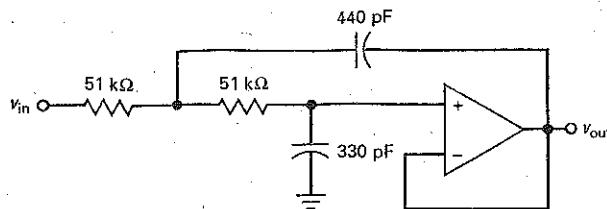
The response of the filter breaks at 4.58 kHz and rolls off at a rate of 40 dB per decade because  $n = 2$ .

**PRACTICE PROBLEM 21-3** Repeat Example 21-3 with the resistor values changed to 10 kΩ.

## Example 21-4

In Fig. 21-28, what are the pole frequency and  $Q$ ? What is the cutoff frequency?

**Figure 21-28** Bessel unity-gain example.



**SOLUTION** The  $Q$  and pole frequency are:

$$Q = 0.5 \sqrt{\frac{C_2}{C_1}} = 0.5 \sqrt{\frac{440 \text{ pF}}{330 \text{ pF}}} = 0.577$$

$$f_p = \frac{1}{2\pi R\sqrt{C_1 C_2}} = \frac{1}{2\pi(51 \text{ k}\Omega)\sqrt{(330 \text{ pF})(440 \text{ pF})}} = 8.19 \text{ kHz}$$

The  $Q$  value of 0.577 tells us that this is a Bessel response. With Eq. (21-21), the cutoff frequency is given by:

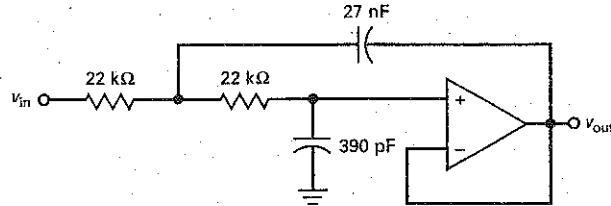
$$f_c = K_c f_p = 0.786(8.19 \text{ kHz}) = 6.44 \text{ kHz}$$

**PRACTICE PROBLEM 21-4** In Example 21-4, if the value of  $C_1$  changed to 680 pF, what value should  $C_2$  be to maintain a  $Q$  of 0.577?

### Example 21-5

What are the pole frequency and  $Q$  in Fig. 21-29? What are the cutoff and 3-dB frequencies?

**Figure 21-29** Unity-gain example with  $Q > 0.707$ .



**SOLUTION** The  $Q$  and pole frequency are:

$$Q = 0.5 \sqrt{\frac{C_2}{C_1}} = 0.5 \sqrt{\frac{27 \text{ nF}}{390 \text{ pF}}} = 4.16$$

$$f_p = \frac{1}{2\pi R\sqrt{C_1 C_2}} = \frac{1}{2\pi(22 \text{ k}\Omega)\sqrt{(390 \text{ pF})(27 \text{ nF})}} = 2.23 \text{ kHz}$$

Referring to Fig. 21-26, we can read the following approximate  $K$  and  $A_p$  values:

$$K_0 = 0.99$$

$$K_c = 1.38$$

$$K_3 = 1.54$$

$$A_p = 12.5 \text{ dB}$$

The cutoff or edge frequency is:

$$f_c = K_c f_p = 1.38(2.23 \text{ kHz}) = 3.08 \text{ kHz}$$

and the 3-dB frequency is:

$$f_{3\text{dB}} = K_3 f_p = 1.54(2.23 \text{ kHz}) = 3.43 \text{ kHz}$$

**PRACTICE PROBLEM 21-5** In Fig. 21-29, change the 27 nF capacitor to 14 nF and repeat Example 21.5.

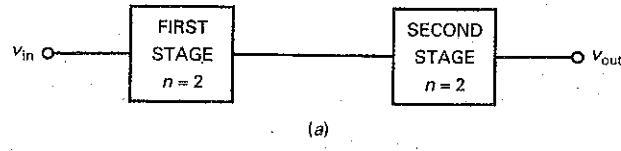
## 21-6 Higher-Order Filters

The standard approach in building higher-order filters is to cascade first- and second-order stages. When the order is even, we need to cascade only second-order stages. When the order is odd, we need to cascade second-order stages and a single first-order stage. For instance, if we want to build a sixth-order filter, we can cascade three second-order stages. If we want to build a fifth-order filter, we can cascade two second-order stages and one first-order stage.

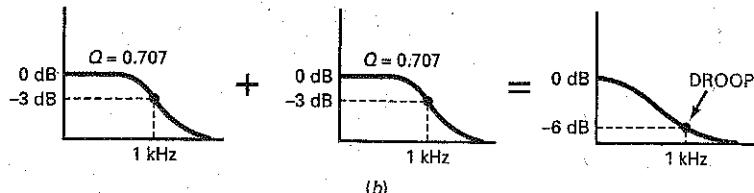
### Butterworth Filters

When filter stages are cascaded, we can add the decibel attenuation of each stage to get the total attenuation. For instance, Fig. 21-30a shows two cascaded second-order stages. If each has a  $Q$  of 0.707 and a pole frequency of 1 kHz, then each stage has a Butterworth response with an attenuation of 3 dB at 1 kHz. Although

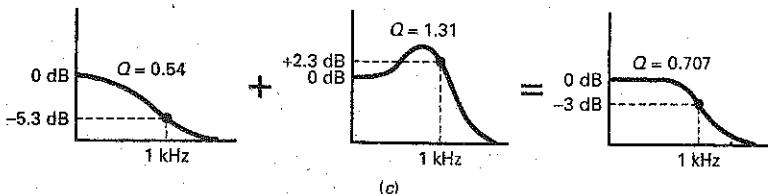
**Figure 21-30** (a) Cascading two stages; (b) equal stages produce a droop at the cutoff frequency; (c) low- $Q$  and high- $Q$  stages compensate to produce Butterworth response.



(a)



(b)



(c)

Table 21-4

Staggered Qs for Butterworth Low-Pass Filters

Order	Stage 1	Stage 2	Stage 3	Stage 4	Stage 5
2	0.707				
4	0.54	1.31			
6	0.52	1.93	0.707		
8	0.51	2.56	0.6	0.9	
10	0.51	3.2	0.56	1.1	0.707

each stage has a Butterworth response, the overall response is not a Butterworth response because it droops at the pole frequency, as shown in Fig. 21-30b. Since each stage has an attenuation of 3 dB at the cutoff frequency of 1 kHz, the overall attenuation is 6 dB at 1 kHz.

To get a Butterworth response, the pole frequencies are still 1 kHz, but the  $Q$ s of the stages have to be staggered above and below 0.707. Figure 21-30c shows how to get a Butterworth response for the overall filter. The first stage has  $Q = 0.54$ , and the second stage has  $Q = 1.31$ . The peaking in the second stage offsets the droop in the first stage to get an attenuation of 3 dB at 1 kHz. Furthermore, it can be shown that the passband response is maximally flat with these  $Q$  values.

Table 21-4 shows the staggered  $Q$  values of the stages used in higher-order Butterworth filters. All the stages have the same pole frequency, but each stage has a different  $Q$ . For instance, the fourth-order filter described by Fig. 21-30c uses  $Q$  values of 0.54 and 1.31, the same values shown in Table 21-4. To build a tenth-order Butterworth filter, we would need five stages with  $Q$  values of 0.51, 3.2, 0.56, 1.1, and 0.707.

### Bessel Filters

With higher-order Bessel filters, we need to stagger both the  $Q$ s and the pole frequencies of the stages. Table 21-5 shows the  $Q$  and  $f_p$  for each stage in a filter with a cutoff frequency of 1000 Hz. For instance, a fourth-order Bessel filter needs a

Table 21-5

Staggered Qs and Pole Frequencies for Bessel Low-Pass Filters ( $f_c = 1000$  Hz)

Order	$Q_1$	$f_{p1}$	$Q_2$	$f_{p2}$	$Q_3$	$f_{p3}$	$Q_4$	$f_{p4}$	$Q_5$	$f_{p5}$
2	0.577	1274								
4	0.52	1432	0.81	1606						
6	0.51	1607	1.02	1908	0.61	1692				
8	0.51	1781	1.23	2192	0.71	1956	0.56	1835		
10	0.50	1946	1.42	2455	0.81	2207	0.62	2066	0.54	1984

**Table 21-6**  $A_p$ ,  $Q_p$ , and  $f_p$  for Chebyshev Low-Pass Filters ( $f_c = 1000$  Hz)

Order	$A_p$ , dB	$Q_1$	$f_{p1}$	$Q_2$	$f_{p2}$	$Q_3$	$f_{p3}$	$Q_4$	$f_{p4}$
2	1	0.96	1050						
	2	1.13	907						
	3	1.3	841						
4	1	0.78	529	3.56	993				
	2	0.93	471	4.59	964				
	3	1.08	443	5.58	950				
6	1	0.76	353	8	995	2.2	747		
	2	0.9	316	10.7	983	2.84	730		
	3	1.04	298	12.8	977	3.46	722		
8	1	0.75	265	14.2	997	4.27	851	1.96	584
	2	0.89	238	18.7	990	5.58	842	2.53	572
	3	1.03	224	22.9	987	6.83	839	3.08	566

first stage with  $Q = 0.52$  and  $f_p = 1432$  Hz, and a second stage with  $Q = 0.81$  and  $f_p = 1606$  Hz.

If the frequency is different from 1000 Hz, the pole frequencies in Table 21-5 are scaled in direct proportion by a frequency scaling factor (FSF) of:

$$\text{FSF} = \frac{f_c}{1 \text{ kHz}}$$

For instance, if a sixth-order Bessel filter has a cutoff frequency of 7.5 kHz, we would multiply each pole frequency in Table 21-5 by 7.5.

### Chebyshev Filters

With Chebyshev filters, we have to stagger  $Q$  and  $f_p$ . Furthermore, we have to include the ripple depth. Table 21-6 shows the  $Q$  and  $f_p$  for each stage of a Chebyshev filter. As an example, a sixth-order Chebyshev filter with a ripple depth of 2 dB needs a first stage with  $Q = 0.9$  and  $f_p = 316$  Hz. The second stage must have  $Q = 10.7$  and  $f_p = 983$  Hz, and a third stage needs  $Q = 2.84$  and  $f_p = 730$  Hz.

### Filter Design

The foregoing discussion gives you the basic idea behind the design of higher-order filters. So far, we have discussed only the simplest circuit implementation, which is the Sallen-Key unity-gain second-order stage. By cascading Sallen-Key unity-gain stages with staggered  $Q$ s and pole frequencies, we can implement higher-order filters for the Butterworth, Bessel, and Chebyshev approximations.

The tables shown earlier indicate how the  $Q$ s and pole frequencies need to be staggered in different designs. Larger, comprehensive tables are available in

filter handbooks. The design of active filters is very complicated, especially when filters need to be designed with orders up to 20 and trade-offs are made between circuit complexity, component sensitivity, and ease of tuning.

Which brings us to an important point: All serious filter design is done on computers because the calculations are too difficult and time-consuming to attempt by hand. An active-filter computer program stores all the equations, tables, and circuits needed to implement the five approximations discussed earlier (Butterworth, Chebyshev, inverse Chebyshev, elliptic, and Bessel). The circuits used to build filters range from a simple one op-amp stage to complex five op-amp stages.

## 21-7 VCVS Equal-Component Low-Pass Filters

Figure 21-31 shows another Sallen-Key second-order low-pass filter. This time, both resistors and both capacitors have the same value. This is why the circuit is called a **Sallen-Key equal-component filter**. The circuit has a midband voltage gain of:

$$A_v = \frac{R_2}{R_1} + 1 \quad (21-29)$$

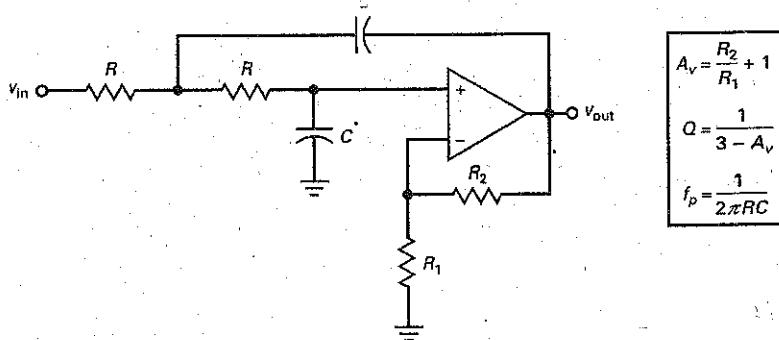
The operation of the circuit is similar to that of Sallen-Key unity-gain filter, except for the effect of the voltage gain. Since the voltage gain can produce more positive feedback through the feedback capacitor, the  $Q$  of the stage becomes a function of voltage gain and is given by:

$$Q = \frac{1}{3 - A_v} \quad (21-30)$$

Because  $A_v$  can be no smaller than unity, the minimum  $Q$  is 0.5. When  $A_v$  increases from 1 to 3,  $Q$  varies from 0.5 to infinity. Therefore, the allowable range of  $A_v$  is between 1 and 3. If we try to run the circuit with  $A_v$  greater than 3, it will break into oscillations because the positive feedback is too large. In fact, it is dangerous to use a voltage gain that even approaches 3 because component tolerance and drift may cause the voltage gain to exceed 3. A later example will bring this point out more clearly.

After we calculate  $A_v$ ,  $Q$ , and  $f_p$  with the equations shown in Fig. 21-31, the rest of the analysis is the same as before because a Butterworth filter has  $Q = 0.707$  and  $K_c = 1$ . A Bessel filter has  $Q = 0.577$  and  $K_c = 0.786$ . For other  $Q$ s, we can get the approximate  $K$  and  $A_p$  values by interpolating from Table 21-3 or by using Fig. 21-26.

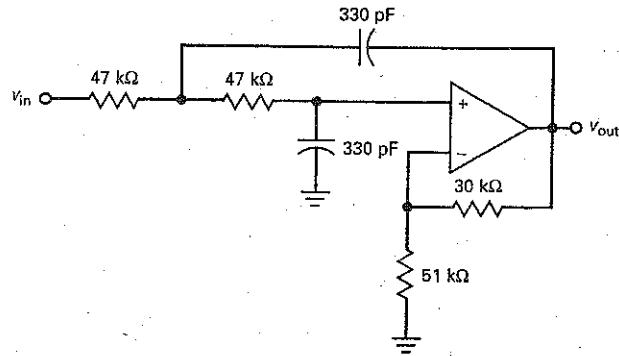
Figure 21-31 VCVS equal-component stage.



## Example 21-6

What are the pole frequency and  $Q$  of the filter shown in Fig. 21-32? What is the cutoff frequency?

Figure 21-32 Butterworth equal-component example.



**SOLUTION** The  $A_v$ ,  $Q$ , and  $f_p$  are:

$$A_v = \frac{30 \text{ k}\Omega}{51 \text{ k}\Omega} + 1 = 1.59$$

$$Q = \frac{1}{3 - A_v} = \frac{1}{3 - 1.59} = 0.709$$

$$f_p = \frac{1}{2\pi RC} = \frac{1}{2\pi(47 \text{ k}\Omega)(330 \text{ pF})} = 10.3 \text{ kHz}$$

It takes a  $Q$  of 0.77 to produce a ripple of 0.1 dB. Therefore, a  $Q$  of 0.709 produces a ripple of less than 0.003 dB. For all practical purposes, the calculated  $Q$  of 0.709 means that we have a Butterworth response to a very close approximation.

The cutoff frequency of a Butterworth filter is equal to the pole frequency of 10.3 kHz.

**PRACTICE PROBLEM 21-6** In Example 21-6, change the 47 kΩ resistors to 22 kΩ and solve for  $A_v$ ,  $Q$ , and  $f_p$ .

## Example 21-7

In Fig. 21-33, what are the pole frequency and  $Q$ ? What is the cutoff frequency?

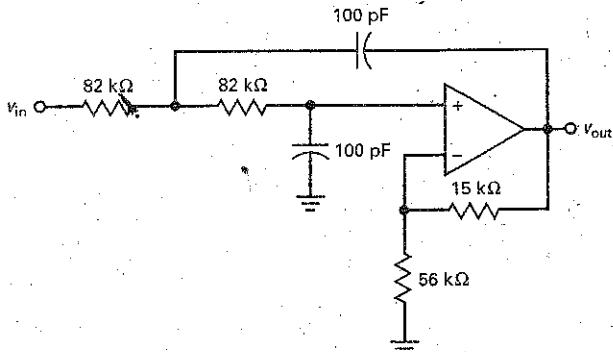
**SOLUTION** The  $A_v$ ,  $Q$ , and  $f_p$  are:

$$A_v = \frac{15 \text{ k}\Omega}{56 \text{ k}\Omega} + 1 = 1.27$$

$$Q = \frac{1}{3 - A_v} = \frac{1}{3 - 1.27} = 0.578$$

$$f_p = \frac{1}{2\pi RC} = \frac{1}{2\pi(82 \text{ k}\Omega)(100 \text{ pF})} = 19.4 \text{ kHz}$$

Figure 21-33 Bessel equal-component example.



This is the  $Q$  of a Bessel second-order response. Therefore,  $K_c = 0.786$  and the cutoff frequency is:

$$f_c = 0.786 f_p = 0.786(19.4 \text{ kHz}) = 15.2 \text{ kHz}$$

**PRACTICE PROBLEM 21-7** Repeat Example 21-7 with the capacitors equal to 330 pF and the  $R$  value set to 100 kΩ.

### Example 21-8

What are the pole frequency and  $Q$  in Fig. 21-34? What are the resonant, cutoff, and 3-dB frequencies? What is the ripple depth in decibels?

**SOLUTION** The  $A_v$ ,  $Q$ , and  $f_p$  are:

$$A_v = \frac{39 \text{ k}\Omega}{20 \text{ k}\Omega} + 1 = 2.95$$

$$Q = \frac{1}{3 - A_v} = \frac{1}{3 - 2.95} = 20$$

$$f_p = \frac{1}{2\pi RC} = \frac{1}{2\pi(56 \text{ k}\Omega)(220 \text{ pF})} = 12.9 \text{ kHz}$$

Figure 21-34 Equal-component example with  $Q > 0.707$ .

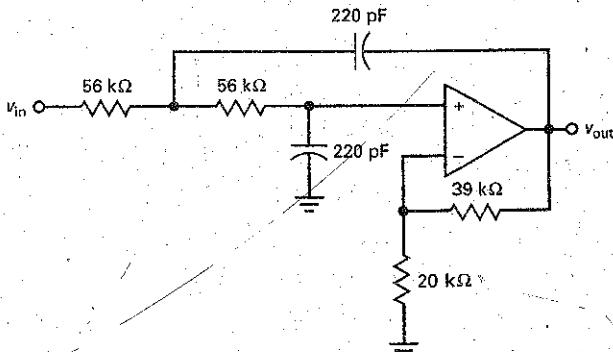


Figure 21-26 has  $Q$ s only between 1 and 10. In this case, we need to use Eqs. (21-25) to (21-28) to get the  $K$  and  $Q$  values:

$$K_0 = 1$$

$$K_c = 1.414$$

$$K_3 = 1.55$$

$$A_p = 20 \log Q = 20 \log 20 = 26 \text{ dB}$$

The resonant frequency is:

$$f_0 = K_0 f_p = 12.9 \text{ kHz}$$

The cutoff or edge frequency is:

$$f_c = K_c f_p = 1.414 (12.9 \text{ kHz}) = 18.2 \text{ kHz}$$

and the 3-dB frequency is:

$$f_{3\text{dB}} = K_3 f_p = 1.55(12.9 \text{ kHz}) = 20 \text{ kHz}$$

The circuit produces a 26-dB peak in the response at 12.9 kHz, rolls off to 0 dB at the cutoff frequency, and is down 3 dB at the 20 kHz.

A Sallen-Key circuit like this is impractical because the  $Q$  is too high. Since the voltage gain is 2.95, any error in the values of  $R_1$  and  $R_2$  can cause large increases in  $Q$ . For instance, if the tolerance of the resistors is  $\pm 1$  percent, the voltage gain can be as high as:

$$A_v = \frac{1.01(39 \text{ k}\Omega)}{0.99(20 \text{ k}\Omega)} + 1 = 2.989$$

This voltage gain produces a  $Q$  of:

$$Q = \frac{1}{3 - A_v} = \frac{1}{3 - 2.989} = 90.9$$

The  $Q$  has changed from a design value of 20 to an approximate value of 90.9, which means that the frequency response is radically different from the intended response.

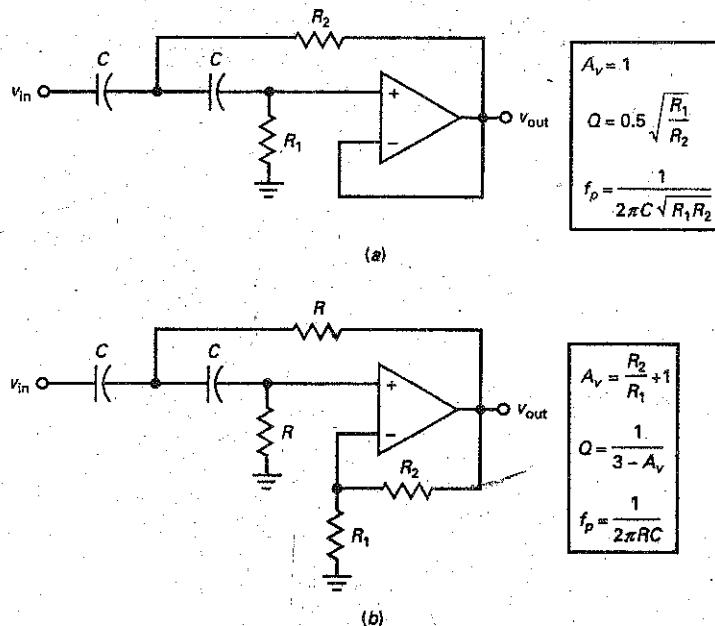
Even though the Sallen-Key equal-component filter is simple compared to other filters, it has the disadvantage of component sensitivity when high  $Q$ s are used. This is why more complicated circuits are typically used for high- $Q$  stages. The added complexity reduces the component sensitivity.

## 21-8 VCVS High-Pass Filters

Figure 21-35a shows the Sallen-Key unity-gain high-pass filter and its equations. Notice that the positions of resistors and capacitors have been reversed. Also notice that  $Q$  depends on the ratio of resistances rather than capacitances. The calculations are similar to those discussed for low-pass filters, except that we have to divide the pole frequency by the  $K$  value. To calculate the cutoff frequency of a high-pass filter, we use:

$$f_c = \frac{f_p}{K_c} \quad (21-31)$$

**Figure 21-35** Second-order VCVS high-pass stages: (a) Unity gain; (b) voltage gain greater than unity.



Similarly, we divide the pole frequency by  $K_0$  or  $K_3$  for the other frequencies. For instance, if the pole frequency is 2.5 kHz and we read  $K_c = 1.3$  in Fig. 21-26, the cutoff frequency for the high-pass filter is:

$$f_c = \frac{2.5 \text{ kHz}}{1.3} = 1.92 \text{ kHz}$$

Figure 21-35b shows the Sallen-Key equal-component high-pass filter and its equations. All the equations are the same as for a low-pass filter. The positions of the resistors and capacitors have been reversed. The following examples show how to analyze high-pass filters.

### Example 21-9

**Multisim**

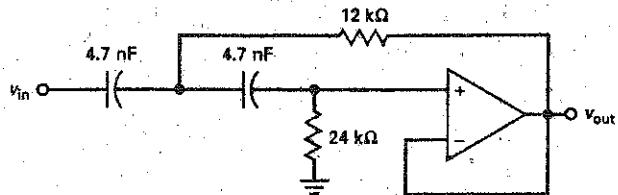
What are the pole frequency and  $Q$  of the filter shown in Fig. 21-36? What is the cutoff frequency?

**SOLUTION** The  $Q$  and pole frequency are:

$$Q = 0.5 \sqrt{\frac{R_1}{R_2}} = 0.5 \sqrt{\frac{24 \text{ k}\Omega}{12 \text{ k}\Omega}} = 0.707$$

$$f_p = \frac{1}{2\pi C \sqrt{R_1 R_2}} = \frac{1}{2\pi(4.7 \text{ nF}) \sqrt{(24 \text{ k}\Omega)(12 \text{ k}\Omega)}} = 2 \text{ kHz}$$

Figure 21-36 High-pass Butterworth example.



Since  $Q = 0.707$ , the filter has a Butterworth second-order response and:

$$f_c = f_p = 2 \text{ kHz}$$

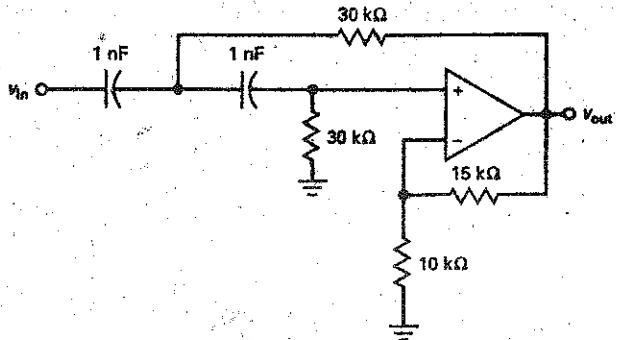
The filter has a high-pass response with a break at 2 kHz, and it rolls off at 40 dB per decade below 2 kHz.

**PRACTICE PROBLEM 21-9** In Fig. 21-36, double the two resistor values. Find the circuit's  $Q$ ,  $f_p$ , and  $f_c$  values.

## Example 21-10

What are the pole frequency and  $Q$  in Fig. 21-37? What are the resonant, cutoff, and 3-dB frequencies? What is the ripple depth or peaking in decibels?

Figure 21-37 High-pass example with  $Q > 1$ .



**SOLUTION** The  $A_v$ ,  $Q$ , and  $f_p$  are:

$$A_v = \frac{15 \text{ k}\Omega}{10 \text{ k}\Omega} + 1 = 2.5$$

$$Q = \frac{1}{3 - A_v} = \frac{1}{3 - 2.5} = 2$$

$$f_p = \frac{1}{2\pi RC} = \frac{1}{2\pi(30 \text{ k}\Omega)(1 \text{ nF})} = 5.31 \text{ kHz}$$

In Fig. 21-26, a  $Q$  of 2 gives the following approximate values:

$$K_0 = 0.94$$

$$K_c = 1.32$$

$$K_3 = 1.48$$

$$A_p = 20 \log Q = 20 \log 2 = 6.3 \text{ dB}$$

The resonant frequency is:

$$f_0 = \frac{f_p}{K_0} = \frac{5.31 \text{ kHz}}{0.94} = 5.65 \text{ kHz}$$

The cutoff frequency is:

$$f_c = \frac{f_p}{K_c} = \frac{5.31 \text{ kHz}}{1.32} = 4.02 \text{ kHz}$$

The 3-dB frequency is:

$$f_{3\text{dB}} = \frac{f_p}{K_3} = \frac{5.31 \text{ kHz}}{1.48} = 3.59 \text{ kHz}$$

The circuit produces a 6.3-dB peak in the response at 5.65 kHz, rolls off to 0 dB at the cutoff frequency of 4.02 kHz, and is down 3 dB at 3.59 kHz.

**PRACTICE PROBLEM 21-10** Repeat Example 21-10 with the 15 k $\Omega$  resistor changed to 17.5 k $\Omega$ .

## 21-9 MFB Bandpass Filters

A bandpass filter has a center frequency and a bandwidth. Recall the basic equations for a bandpass response:

$$\text{BW} = f_2 - f_1$$

$$f_0 = \sqrt{f_1 f_2}$$

$$Q = \frac{f_0}{\text{BW}}$$

When  $Q$  is less than 1, the filter has a wideband response. In this case, a bandpass filter is usually built by cascading a low-pass stage with a high-pass stage. When  $Q$  is greater than 1, the filter has a narrowband response and a different approach is used.

### Wideband Filters

Suppose we want to build a bandpass filter with a lower cutoff frequency of 300 Hz and an upper cutoff frequency of 3.3 kHz. The center frequency of the filter is:

$$f_0 = \sqrt{f_1 f_2} = \sqrt{(300 \text{ Hz})(3.3 \text{ kHz})} = 995 \text{ Hz}$$

The bandwidth is:

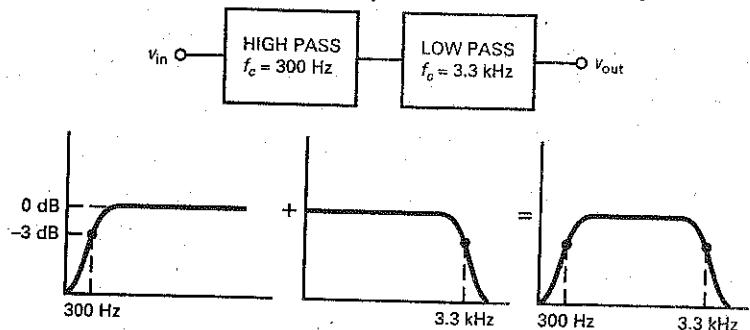
$$\text{BW} = f_2 - f_1 = 3.3 \text{ kHz} - 300 \text{ Hz} = 3 \text{ kHz}$$

$Q$  is:

$$Q = \frac{f_0}{\text{BW}} = \frac{995 \text{ Hz}}{3 \text{ kHz}} = 0.332$$

Since  $Q$  is less than 1, we can use cascaded low-pass and high-pass stages, as shown in Fig. 21-38. The high-pass filter has a cutoff frequency of 300 Hz, and the low-pass filter has a cutoff frequency of 3.3 kHz. When the two decibel responses are added, we get a bandpass response with cutoff frequencies of 300 Hz and 3.3 kHz.

Figure 21-38 Wideband filter uses cascade of low-pass and high-pass stages.



When  $Q$  is greater than 1, the cutoff frequencies are much closer than shown in Fig. 21-38. Because of this, the sum of the passband attenuations is greater than 3 dB at the cutoff frequencies. This is why we use another approach for narrowband filters.

### Narrowband Filters

When  $Q$  is greater than 1, we can use the multiple-feedback (MFB) filter shown in Fig. 21-39. First, notice that the input signal goes to the inverting input rather than the noninverting input. Second, notice that the circuit has two feedback paths, one through a capacitor and another through a resistor.

At low frequencies the capacitors appear to be open. Therefore, the input signal cannot reach the op amp, and the output is zero. At high frequencies the capacitors appear to be shorted. In this case, the voltage gain is zero because the feedback capacitor has zero impedance. Between the low and high extremes in frequency, there is a band of frequencies where the circuit acts like an inverting amplifier.

The voltage gain at the center frequency is given by:

$$A_v = \frac{-R_2}{2R_1} \quad (21-32)$$

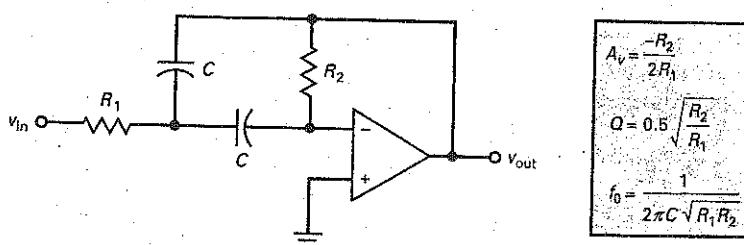
This is almost identical to the voltage gain of an inverting amplifier: except for the factor of 2 in the denominator. The  $Q$  of the circuit is given by:

$$Q = 0.5 \sqrt{\frac{R_2}{R_1}} \quad (21-33)$$

which is equivalent to:

$$Q = 0.707 \sqrt{-A_v} \quad (21-34)$$

Figure 21-39 Multiple-feedback bandpass stage.



For instance, if  $A_v = -100$ :

$$Q = 0.707 \sqrt{100} = 7.07$$

Equation (21-34) tells us that the greater the voltage gain, the higher the  $Q$ .

The center frequency is given by:

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \quad (21-35)$$

Since  $C_1 = C_2$  in Fig. 21-39, the equation simplifies to:

$$f_0 = \frac{1}{2\pi C \sqrt{R_1 R_2}} \quad (21-36)$$

### Increasing the Input Impedance

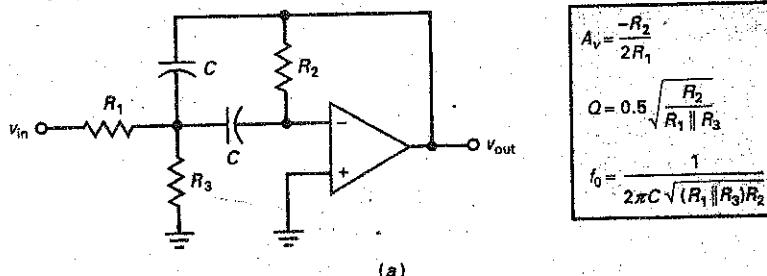
Equation (21-33) tells us that  $Q$  is proportional to the square root of  $R_2/R_1$ . To get high  $Q$ s, we need to use a high ratio of  $R_2/R_1$ . For instance, to get a  $Q$  of 5,  $R_2/R_1$  must equal 100. To avoid problems with input offset and bias current,  $R_2$  is usually kept under 100 k $\Omega$ , which means that  $R_1$  has to be less than 1 k $\Omega$ . For  $Q$ s greater than 5,  $R_1$  must be even smaller. This means that the input impedance of Fig. 21-39 may be too low at higher  $Q$ s.

Figure 21-40a shows an MFB bandpass filter that increases the input impedance. The circuit is identical to the earlier MFB circuit, except for the new resistor  $R_3$ . Notice that  $R_1$  and  $R_3$  form a voltage divider. By applying Thevenin's theorem, the circuit simplifies to Fig. 21-40b. This configuration is the same as that shown in Fig. 21-39, but some of the equations are different. To begin with, the voltage gain is still given by Eq. (21-32). But the  $Q$  and center frequency become:

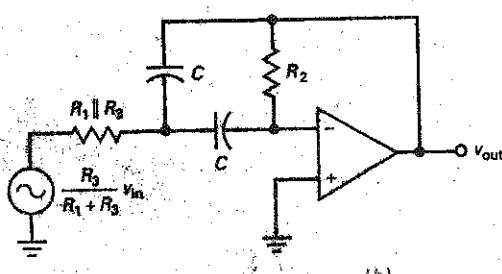
$$Q = 0.5 \sqrt{\frac{R_2}{R_1 \parallel R_3}} \quad (21-37)$$

$$f_0 = \frac{1}{2\pi C \sqrt{(R_1 \parallel R_3) R_2}} \quad (21-38)$$

Figure 21-40 Increasing input impedance of MFB stage.

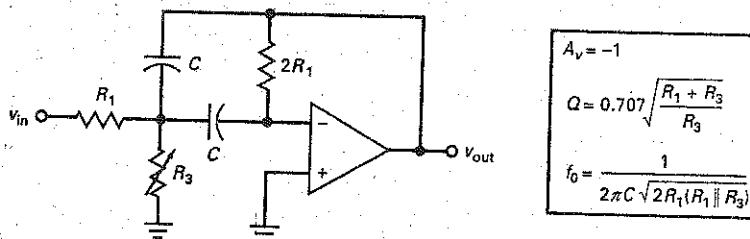


(a)



(b)

Figure 21-41 MFB stage with variable center frequency and constant bandwidth.



The circuit has the advantage of higher input impedance because  $R_1$  can be made higher for a given  $Q$ .

### Tunable Center Frequency with Constant Bandwidth

Having a voltage gain greater than 1 is not necessary in many applications because voltage gain is usually available in another stage. If unity voltage gain is acceptable, then we can use a clever circuit that varies the center frequency while holding the bandwidth constant.

Figure 21-41 shows a modified MFB circuit in which  $R_2 = 2R_1$  and  $R_3$  is variable. With this circuit, the analysis equations are:

$$A_v = -1 \quad (21-39)$$

$$Q = 0.707 \sqrt{\frac{R_1 + R_3}{R_3}} \quad (21-40)$$

$$f_0 = \frac{1}{2\pi C \sqrt{2R_1(R_1 \parallel R_3)}} \quad (21-41)$$

Since  $BW = f_0/Q$ , we can derive this equation for bandwidth:

$$BW = \frac{1}{2\pi R_1 C} \quad (21-42)$$

Equation (21-41) says that varying  $R_3$  will vary  $f_0$ , but Eq. (21-42) shows that bandwidth is independent of  $R_3$ . Therefore, we can have a constant bandwidth while varying the center frequency.

Variable resistor  $R_3$  in Fig. 21-41 is often a JFET used as a voltage-controlled resistance (discussed in Sec. 13-9). Since the gate voltage changes the resistance of the JFET, the center frequency of the circuit can be tuned electronically.

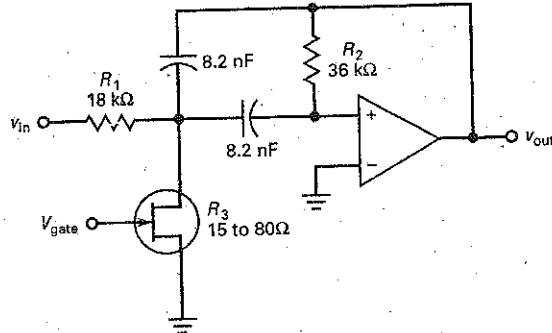
### Example 21-11

The gate voltage of Fig. 21-42 can vary the JFET resistance from 15 to 80  $\Omega$ . What is the bandwidth? What are the minimum and maximum center frequencies?

**SOLUTION** Equation (21-42) gives the bandwidth:

$$BW = \frac{1}{2\pi R_1 C} = \frac{1}{2\pi(18 \text{ k}\Omega)(8.2 \text{ nF})} = 1.08 \text{ kHz}$$

Figure 21-42 Tuning an MFB filter with a voltage-controlled resistance.



With Eq. (21-41), the minimum center frequency is:

$$f_0 = \frac{1}{2\pi C \sqrt{2R_1(R_1 \parallel R_3)}} \\ = \frac{1}{2\pi(8.2 \text{ nF})\sqrt{2(18 \text{ k}\Omega)(18 \text{ k}\Omega \parallel 80 \Omega)}} \\ = 11.4 \text{ kHz}$$

The maximum frequency is:

$$f_0 = \frac{1}{2\pi(8.2 \text{ nF})\sqrt{2(18 \text{ k}\Omega)(18 \text{ k}\Omega \parallel 15 \Omega)}} = 26.4 \text{ kHz}$$

**PRACTICE PROBLEM 21-11** Using Fig. 21-42, change  $R_1$  to 10 kΩ and repeat Example 21-11.

## 21-10 Bandstop Filters

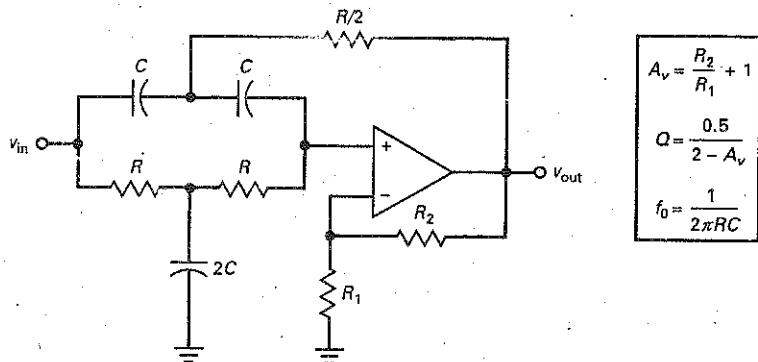
There are many circuit implementations for bandstop filters. They use from one to four op amps in each second-order stage. In many applications, a bandstop filter needs to block only a single frequency. For instance, the ac power lines may induce a hum of 60 Hz in sensitive circuits; this may interfere with a desired signal. In this case, we can use a bandstop filter to notch out the unwanted hum signal.

Figure 21-43 shows a Sallen-Key second-order notch filter and its analysis equations. At low frequencies all capacitors are open. As a result, all the input signal reaches the noninverting input. The circuit has a passband voltage gain of:

$$A_v = \frac{R_2}{R_1} + 1 \quad (21-43)$$

At very high frequencies, the capacitors are shorted. Again, all the input signal reaches the noninverting input.

Figure 21-43 Sallen-Key second-order notch filter.



Between the low and high extremes in frequency, there is a center frequency given by:

$$f_0 = \frac{1}{2\pi RC} \quad (21-44)$$

At this frequency, the feedback signal returns with the correct amplitude and phase to attenuate the signal on the noninverting input. Because of this, the output voltage drops to a very low value.

The  $Q$  of the circuit is given by:

$$Q = \frac{0.5}{2 - A_v} \quad (21-45)$$

The voltage gain of a Sallen-Key notch filter must be less than 2 to avoid oscillations. Because of the tolerance of the  $R_1$  and  $R_2$  resistors, the circuit  $Q$  should be much less than 10. At higher  $Q$ s, the tolerance of these resistors may produce a voltage gain greater than 2, which would produce oscillations.

## Example 21-12

Multisim

What are the voltage gain, center frequency, and  $Q$  for the bandstop filter shown in Fig. 21-43 if  $R = 22 \text{ k}\Omega$ ,  $C = 120 \text{ nF}$ ,  $R_1 = 13 \text{ k}\Omega$ , and  $R_2 = 10 \text{ k}\Omega$ ?

**SOLUTION** With Eqs. (21-43) to (21-45):

$$A_v = \frac{10 \text{ k}\Omega}{13 \text{ k}\Omega} + 1 = 1.77$$

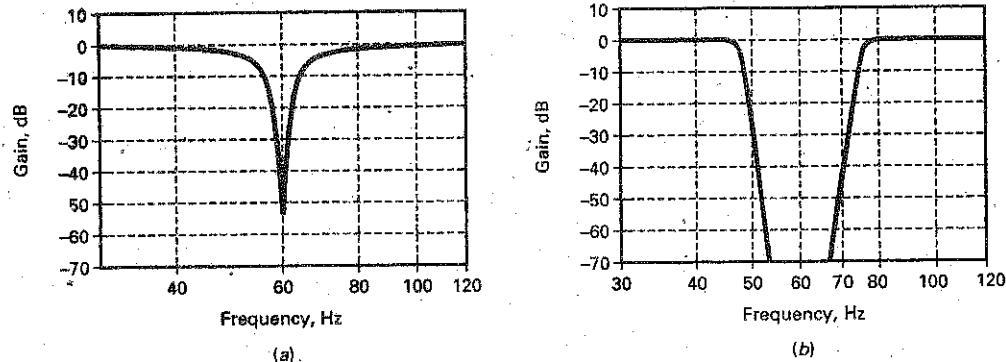
$$f_0 = \frac{1}{2\pi(22 \text{ k}\Omega)(120 \text{ nF})} = 60.3 \text{ Hz}$$

$$Q = \frac{0.5}{2 - A_v} = \frac{0.5}{2 - 1.77} = 2.17$$

Figure 21-44a shows the response. Notice how sharp the notch is for a second-order filter.

By increasing the order of the filter, we can broaden the notch. For instance, Fig. 21-44b shows the frequency response for a notch filter with  $n = 20$ . The broader notch reduces component sensitivity and guarantees that the 60-Hz hum will be heavily attenuated.

Figure 21-44 (a) Second-order notch filter at 60 Hz; (b) notch filter with  $n = 20$ .



**PRACTICE PROBLEM 21-12** In Fig. 21-43, change  $R_2$  to obtain a  $Q$  value of 3. Also, change the  $C$  value for a center frequency of 120 Hz.

## 21-11 The All-Pass Filter

Section 21-1 discussed the basic idea of the *all-pass filter*. Although the term *all-pass filter* is widely used in industry, a more descriptive name would be the *phase filter* because the filter shifts the phase of the output signal without changing the magnitude. Another descriptive title would be the *time-delay filter*, since time delay is related to a phase shift.

### First-Order All-Pass Stage

The all-pass filter has a constant voltage gain for all frequencies. This type of filter is useful when we want to produce a certain amount of phase shift for a signal without changing the amplitude.

Figure 21-45a shows a *first-order all-pass lag filter*. It is first order because it has only one capacitor. This is the phase shifter we discussed in Chap. 20. Recall that it shifts the phase of the output signal between 0 and  $-180^\circ$ . The center frequency of an all-pass filter is where the phase shift is half of maximum. For a first-order lag filter, the center frequency has a phase shift of  $-90^\circ$ .

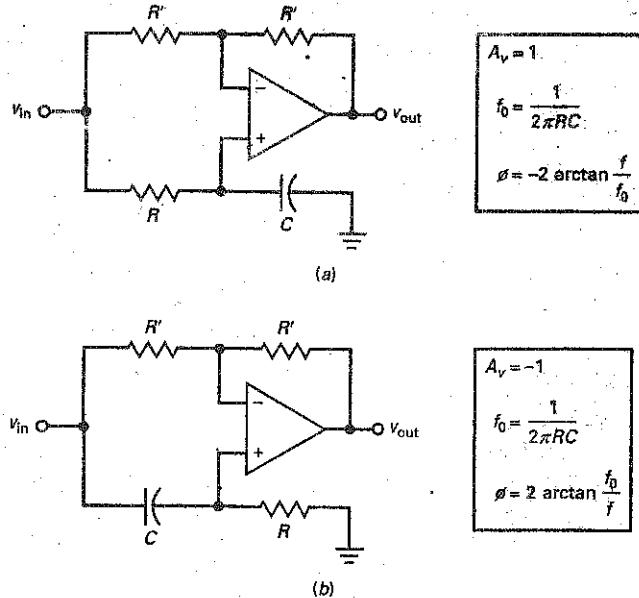
Figure 21-45b shows a *first-order all-pass lead filter*. In this case, the circuit shifts the phase of the output signal between  $180$  and  $0^\circ$ . This means that the output signal can lead the input signal by up to  $+180^\circ$ . For a first-order lead filter, the phase shift is  $+90^\circ$  at the center frequency.

### Second-Order All-Pass Filter

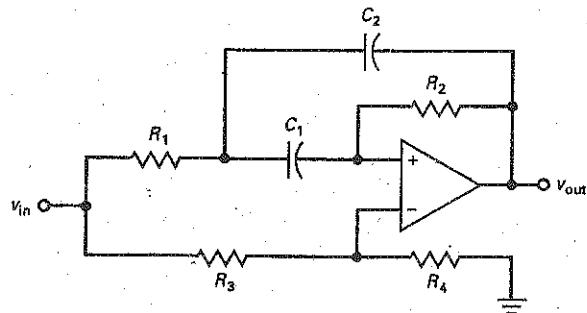
A second-order all-pass filter has at least one op amp, two capacitors, and several resistors that can shift the phase between 0 and  $\pm 360^\circ$ . Furthermore, it is possible to adjust the  $Q$  of a second-order all-pass filter to change the shape of the phase response between 0 and  $\pm 360^\circ$ . The center frequency of a second-order filter is where the phase shift equals  $\pm 180^\circ$ .

Figure 21-46 shows a *second-order MFB all-pass lag filter*. It has one op amp, four resistors, and two capacitors, which is the simplest configuration. More

**Figure 21-45** First-order all-pass stages: (a) lagging output phase; (b) leading output phase.



**Figure 21-46** Second-order all-pass stage.



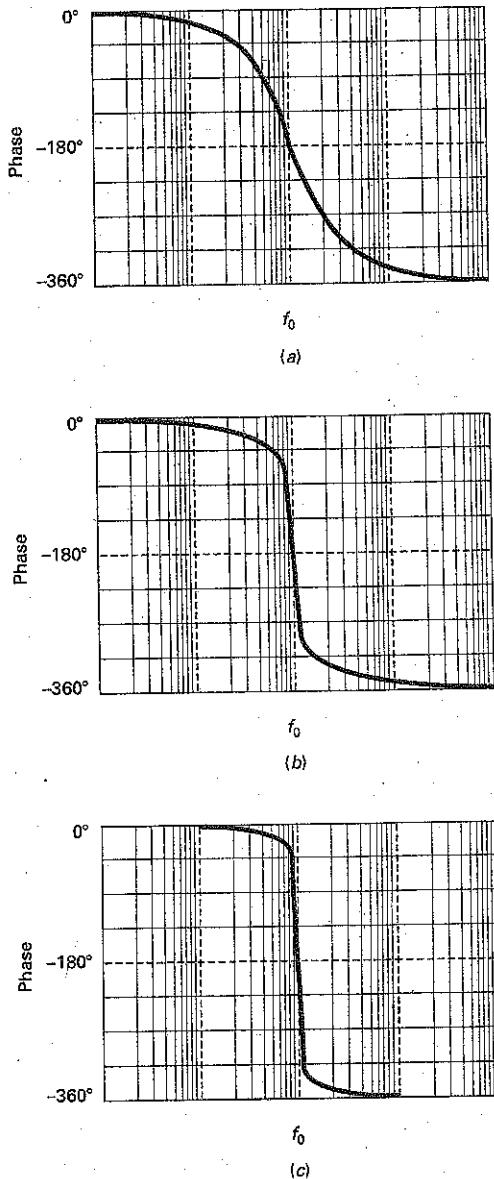
complex configurations use two or more op amps, two capacitors, and several resistors. With a second-order all-pass filter, we can set the center frequency and  $Q$  of the circuit.

Figure 21-47 shows the phase response of a second-order all-pass lag filter with  $Q = 0.707$ . Notice how the output phase increases from  $0^\circ$  to  $-360^\circ$ . By increasing the  $Q$  to 2, we can get the phase response as shown in Fig. 21-47b. The higher  $Q$  does not change the center frequency, but the phase change is faster near the center frequency. A  $Q$  of 10 produces the even steeper phase response of Fig. 21-47c.

### Linear Phase Shift

To prevent distortion of digital signals (rectangular pulses), a filter must have a linear phase shift for the fundamental and all significant harmonics. An equivalent requirement is a constant time delay for all frequencies in the passband. The

**Figure 21-47** Second-order phase responses: (a)  $Q = 0.707$ ; (b)  $Q = 2$ ; (c)  $Q = 10$ .

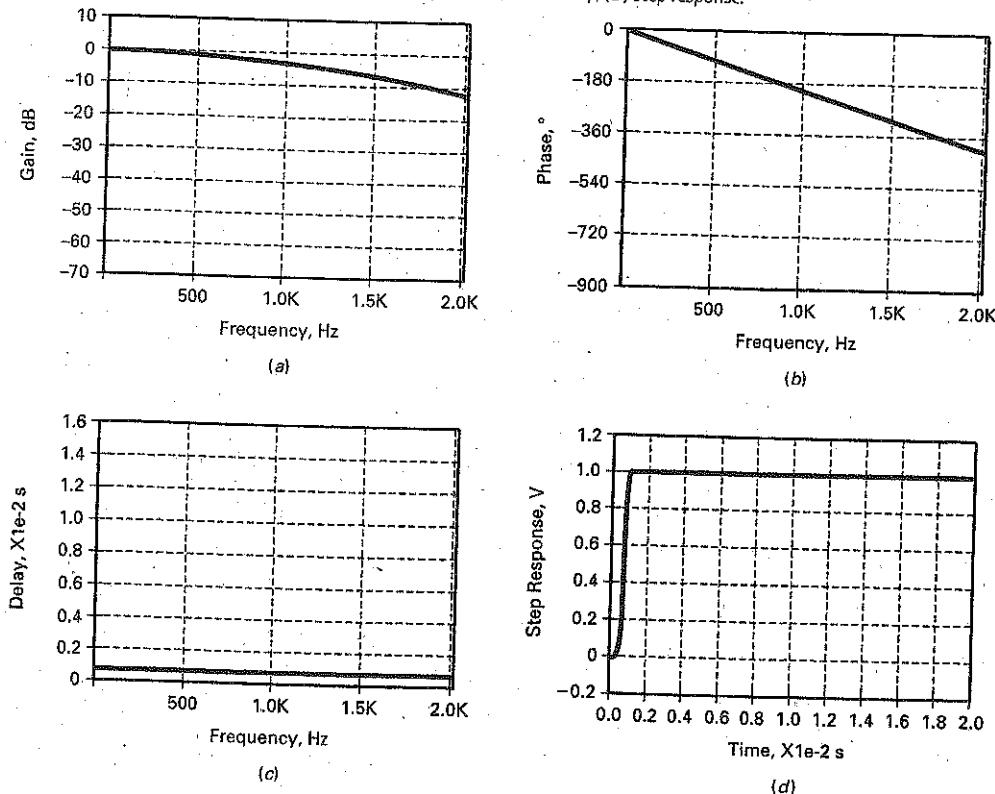


Bessel approximation produces an almost linear phase shift and constant time delay. But in some applications, the slow roll-off rate of the Bessel approximation may not be adequate. Sometimes, the only solution is to use one of the other approximations to get the required roll-off rate, and then use an all-pass filter to correct the phase shift as needed to get an overall linear phase shift.

### Bessel Responses

For instance, suppose we need a low-pass filter with  $A_p = 3$  dB,  $f_c = 1$  kHz,  $A_s = 60$  dB, and  $f_s = 2$  kHz and with a linear phase shift for all frequencies in the

Figure 21-48 Bessel responses for  $n = 10$ . (a) Gain; (b) phase; (c) time delay; (d) step response.



passband. If a tenth-order Bessel filter is used, it would produce the frequency response of Fig. 21-48a, the phase response of Fig. 21-48b, the time-delay response of Fig. 21-48c, and the step response of Fig. 21-48d.

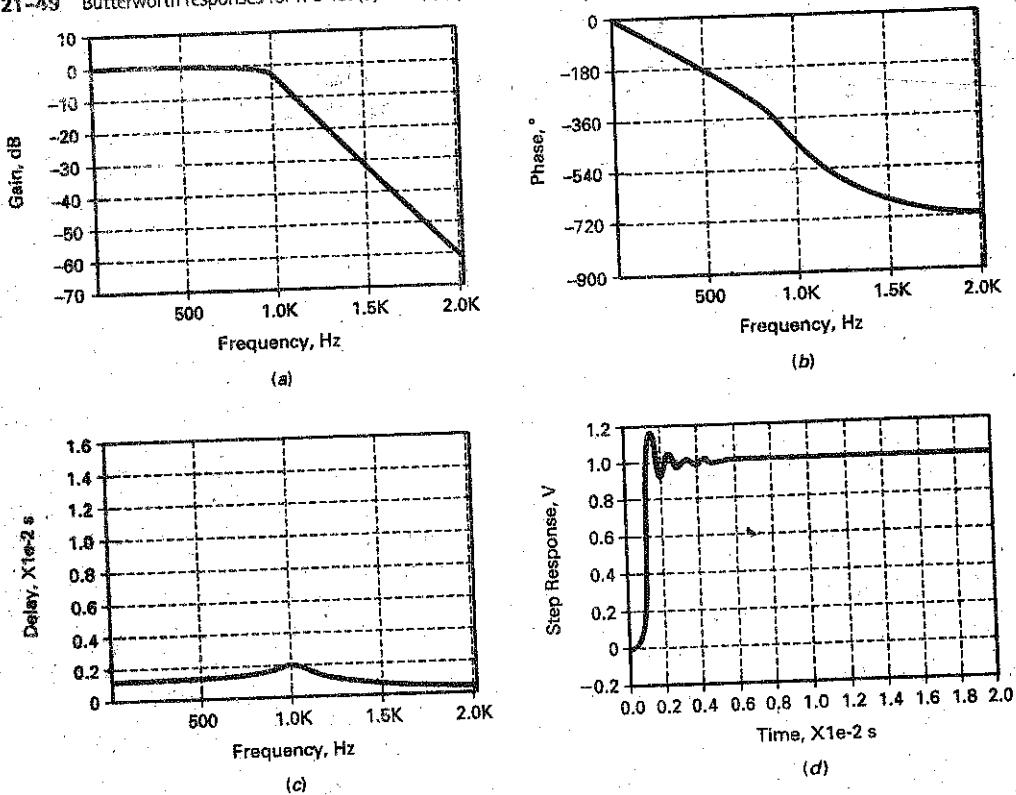
First off, notice how slow the roll-off is in Fig. 21-48a. The cutoff frequency is 1 kHz. An octave higher, the attenuation is only 12 dB, which does not meet the required specification of  $A_s = 60$  dB and  $f_s = 2$  kHz. But look at how linear the phase response of Fig. 21-48b is. This is the kind of phase response that is almost perfect for digital signals. Linear phase shift and constant time delay are synonymous. This is why the time delay is constant in Fig. 21-48c. Finally, look at how sharp the step response of Fig. 21-48d is. It may not be perfect, but it is close.

## Butterworth Responses

To meet the specifications, we can do the following: We can cascade a tenth-order Butterworth filter and an all-pass filter. The Butterworth filter will produce the required roll-off rate, and the all-pass filter will produce a phase response that complements the Butterworth phase response to get a linear phase response.

A tenth-order Butterworth filter will produce the frequency response of Fig. 21-49a, the phase response of Fig. 21-49b, the time-delay response of Fig. 21-49c, and the step response of Fig. 21-49d. As we can see, the attenuation is 60 dB at 2 kHz (Fig. 21-49a), which meets the specifications of  $A_s = 60$  dB and

Figure 21-49 Butterworth responses for  $n = 10$ : (a) Gain; (b) phase; (c) time delay; (d) step response.



$f_s = 2$  kHz. But look at how nonlinear the phase response of Fig. 21-49b is. This kind of phase response will distort digital signals. Likewise, look at the peaked time delay of Fig. 21-49c. Finally, look at the overshoot in the step response of Fig. 21-49d.

### Delay Equalizers

One of the main uses of all-pass filters is to correct the overall phase response by adding the necessary phase shift at each frequency to linearize the overall phase response. When this is done, the time delay becomes constant and the overshoot disappears. When used to compensate for the time delay of another filter, the all-pass filter is sometimes called a **delay equalizer**. A delay equalizer has a time delay that looks like an inverted image of the original time delay. For instance, to compensate for the time delay of Fig. 21-49c, the delay equalizer needs to have an upside-down version of Fig. 21-49c. Since the total time delay is the sum of the two delays, the total time delay will be flat or constant.

The problem of designing a delay equalizer is extremely complicated. Because of the difficult calculations that are required, only computers can find the component values in a reasonable amount of time. To synthesize an all-pass filter, the computer has to cascade several second-order all-pass stages and then stagger the center frequencies and  $Q$ s as needed to get the final design.

### Example 21-13

Multisim

In Fig. 21-45b,  $R = 1 \text{ k}\Omega$  and  $C = 100 \text{ nF}$ . What is the phase shift of the output voltage when  $f = 1 \text{ kHz}$ ?

**SOLUTION** Figure 21-45b gives the equation for the cutoff frequency:

$$f_0 = \frac{1}{2\pi(1 \text{ k}\Omega)(100 \text{ nF})} = 1.59 \text{ kHz}$$

The phase shift is:

$$\phi = 2 \arctan \frac{1.59 \text{ kHz}}{1 \text{ kHz}} = 116^\circ$$

## 21-12 Biquadratic and State-Variable Filters

All second-order filters discussed up to now have used only one op amp. These single op-amp stages are adequate for many applications. In the most stringent applications, more complicated second-order stages are used.

### Biquadratic Filter

Figure 21-50 shows a second-order biquadratic bandpass/lowpass filter. It has three op amps, two equal capacitors, and six resistors. Resistors  $R_2$  and  $R_1$  set the voltage gain. Resistors  $R_3$  and  $R'_3$  have the same nominal value, as do  $R_4$  and  $R'_4$ . The circuit equations are shown in Fig. 21-50.

The biquadratic filter is also referred to as a *TT (Tow-Thomas) filter*. This type of filter can be tuned by varying  $R_3$ . This has no effect on the voltage gain, which is an advantage. The biquadratic filter of Fig. 21-50 also has a low-pass output. In some applications, getting bandpass and low-pass responses simultaneously is an advantage.

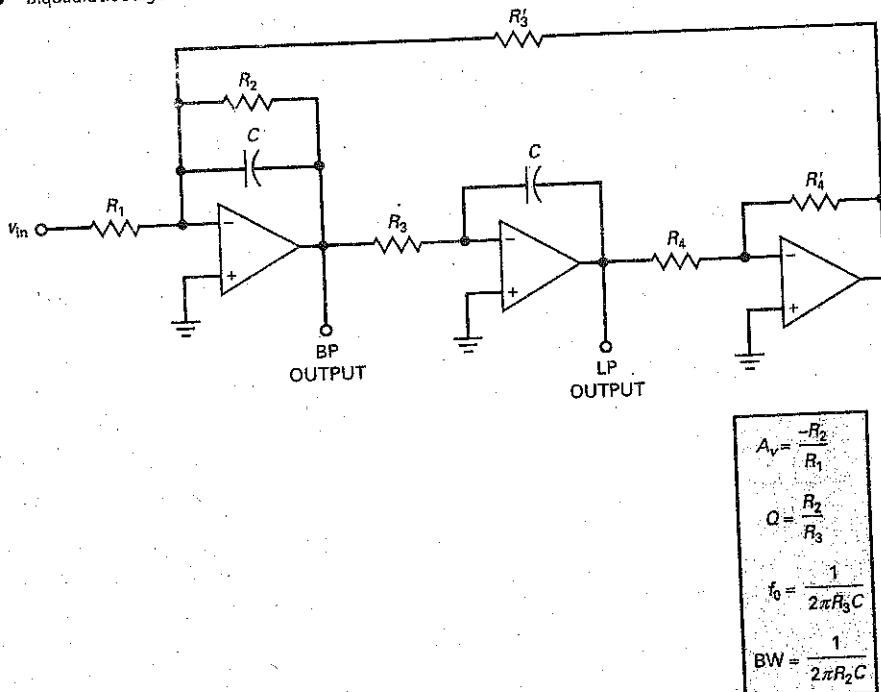
Here is another advantage of the biquadratic filter: As shown in Fig. 21-50, the bandwidth of a biquadratic filter is given by:

$$\text{BW} = \frac{1}{2\pi R_2 C}$$

With the biquadratic filter of Fig. 21-50, we can independently vary the voltage gain with  $R_1$ , the bandwidth with  $R_2$ , and the center frequency with  $R_3$ . Having voltage gain, center frequency, and bandwidth all independently tunable is a major advantage and one of the reasons for the popularity of biquadratic filters (also called *biquads*).

By adding a fourth op amp and more components, we can also build biquadratic high-pass, bandstop, and all-pass filters. When component tolerance is a problem, biquadratic filters are often used because they have less sensitivity to changes in the component values than do the Sallen-Key and MFB filters.

Figure 21-50 Biquadratic stage.



### State-Variable Filter

The state-variable filter is also called a *KHN filter* after the inventors (Kerwin, Huelsman, and Newcomb). Two configurations are available: inverting and noninverting. Figure 21-51 shows a second-order state-variable filter. It has three simultaneous outputs: low-pass, high-pass, and bandpass. This may be an advantage in some applications.

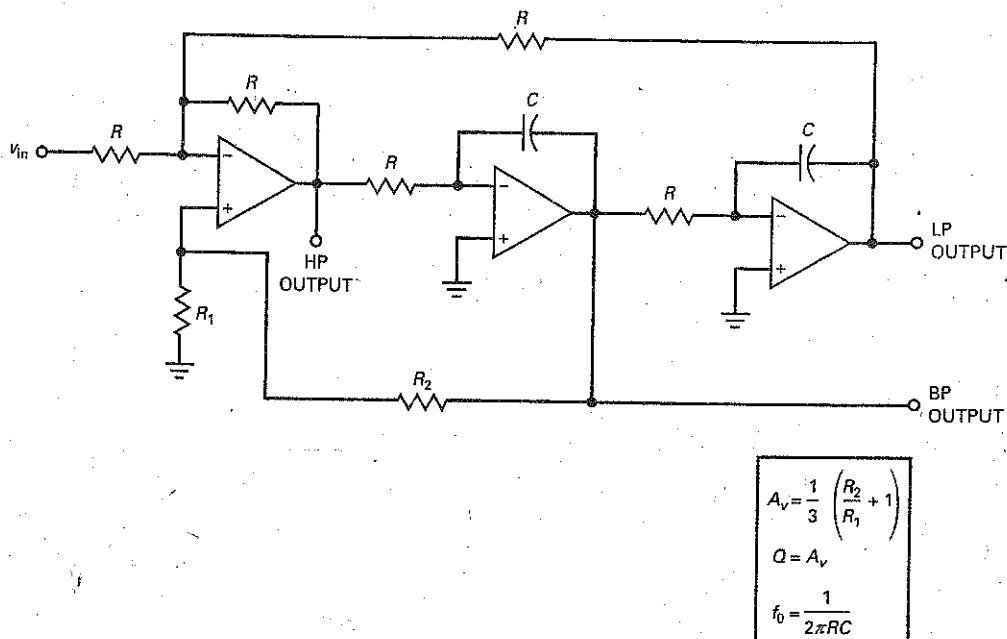
By adding a fourth op amp and a few more components, the  $Q$  of the circuit becomes independent of the voltage gain and the center frequency. This means that the  $Q$  is constant when the center frequency is varied. A constant  $Q$  means that bandwidth is a fixed percentage of the center frequency. For instance, if  $Q = 10$ , bandwidth will be 10 percent of  $f_0$ . This is desirable in some applications where the center frequency is varied.

Like the biquad, the state-variable filter uses more parts than do the VCVS and MFB filters. But the additional op amps and other components make it more suitable for higher-order filters and critical applications. Furthermore, the biquad and state-variable filters exhibit less component sensitivity, which results in a filter that is easier to produce and requires less adjustment.

### Conclusion

Summary Table 21-1 presents the four basic filter circuits used to implement the different approximations. As indicated, the Sallen-Key filters fall into the general class of VCVS filters, the multiple-feedback filters are abbreviated *MFB*, the biquadratic filters may be referred to as *TT filters*, and the state-variable filters are known as *KHN filters*. The complexity of the VCVS and MFB filters is low

Figure 21-51 State-variable stage.



Summary Table 21-1 Basic Filter Circuits

Type	Other names	Complexity	Sensitivity	Tuning	Advantages
Sallen-Key	VCVS	Low	High	Difficult	Simplicity, noninverting
Multiple-feedback	MFB	Low	High	Difficult	Simplicity, inverting
Biquadratic	TT	High	Low	Easy	Stability, extra outputs, constant BW
State-variable	KHN	High	Low	Easy	Stability, extra outputs, constant Q

because they use only one op amp, whereas the complexity of the TT and KHN filters is high because they may use three to five op amps in a second-order stage.

The VCVS and MFB filters have a high sensitivity to component tolerance, whereas the TT and KHN filters have a much lower component sensitivity. VCVS and MFB filters may be somewhat difficult to tune because of interaction between voltage gain, cutoff and center frequencies, and  $Q$ . The TT filter is easier to tune because its voltage gain, center frequency, and bandwidth are independently tunable. The KHN has independently tunable voltage gain, center frequency, and  $Q$ . Finally, the VCVS and MFB filters offer simplicity, and the TT and KHN filters offer stability and additional outputs. When the center frequency of a bandpass filter is varied, the TT filter has a constant bandwidth and the KHN filter has a constant  $Q$ .

Although any of the five basic approximations (Butterworth, Chebyshev, inverse Chebyshev, elliptic, and Bessel) can be implemented with op-amp circuits, the more complicated approximations (inverse Chebyshev and elliptic)

**Summary Table 21-2** Approximations and Circuits

Type	Passband	Stopband	Usable stages
Butterworth	Flat	Monotonic	VCVS, MFB, TT, KHN
Chebyshev	Rippled	Monotonic	VCVS, MFB, TT, KHN
Inverse Chebyshev	Flat	Rippled	KHN
Elliptic	Rippled	Rippled	KHN
Bessel	Flat	Monotonic	VCVS, MFB, TT, KHN

cannot be implemented with VCVS or MFB circuits. Summary Table 21-2 shows the five approximations and the types of stages that can be used with them. As we can see, the rippled stopband responses of the inverse Chebyshev and the elliptic approximations require a complex filter like the KHN (state-variable) for implementation.

This chapter discussed four of the most basic filter circuits, shown in Summary Table 21-1. These basic circuits are quite popular and widely used. But we should be aware of the fact that many more circuits are available in computer programs that do filter design. These include the following second-order stages: Akerberg-Mossberg, Bach, Berha-Herpy, Boctor, Diliannis-Friend, Fliege, Mikhael-Bhattacharyya, Sculley, and the twin-T. All the active-filter circuits used today have advantages and disadvantages that allow a designer to choose the best compromise for an application.

## Summary

### SEC. 21-1 IDEAL RESPONSES

There are five basic types of responses: low-pass, high-pass, bandpass, bandstop, and all-pass. The first four have a passband and a stopband. Ideally, the attenuation should be zero in the passband and infinite in the stopband with a brick wall transition.

### SEC. 21-2 APPROXIMATE RESPONSES

The passband is identified by its low attenuation and its edge frequency. The stopband is identified by its high attenuation and edge frequency. The order of a filter is the number of reactive components. With active filters, it is usually the number of capacitors. The five approximations are the Butterworth (maximally flat passband), the Chebyshev

(ripped passband), the inverse Chebyshev (flat passband and rippled stopband), the elliptic (ripped passband and stopband), and the Bessel (maximally flat time delay).

### SEC. 21-3 PASSIVE FILTERS

A low-pass LC filter has a resonant frequency  $f_0$  and a  $Q$ . The response is maximally flat when  $Q = 0.707$ . As  $Q$  increases, a peak appears in the response, centered on the resonant frequency. The Chebyshev response occurs with  $Q$  greater than 0.707, and the Bessel with  $Q = 0.577$ . The higher the  $Q$ , the faster the roll-off in the transition region.

### SEC. 21-4 FIRST-ORDER STAGES

First-order stages have a single capacitor and one or more resistors. All first-order

stages produce a Butterworth response because peaking is possible only in second-order stages. A first-order stage can produce either a low-pass or a high-pass response.

### SEC. 21-5 VCVS UNITY-GAIN SECOND-ORDER LOW-PASS FILTERS

Second-order stages are the most common stage because they are easy to implement and analyze. The  $Q$  of the stage produces different  $K$  values. The pole frequency of a low-pass stage can be multiplied by its  $K$  values to get the resonant frequency if there is a peak, a cutoff frequency, and a 3-dB frequency.

## SEC. 21-6 HIGHER-ORDER FILTERS

Higher-order filters are usually made by cascading second-order stages or a first-order stage when the total order is odd. When filter stages are cascaded, we add the decibel gains of the stages to get the total decibel gain. To get the Butterworth response for a higher-order filter, we have to stagger the  $Q$ s of the stages. To get the Chebyshev and other responses, we have to stagger the pole frequencies and the  $Q$ s.

## SEC. 21-7 VCVS EQUAL-COMPONENT LOW-PASS FILTERS

The Sallen-Key equal-component filters control the  $Q$  by setting the voltage gain. The voltage gain must be less than 3 to avoid oscillations. Higher  $Q$ s are difficult to get with this circuit because the component tolerance becomes very important in determining the voltage gain and  $Q$ .

## SEC. 21-8 VCVS HIGH-PASS FILTERS

VCVS high-pass filters have the same configuration as low-pass filters, except

that the resistors and capacitors are interchanged. Again, the  $Q$  values determine the  $K$  values. We have to divide pole frequency by the  $K$  values to get the resonant frequency, cutoff frequency, and 3-dB frequency.

## SEC. 21-9 MFB BANDPASS FILTERS

Low-pass and high-pass filters may be cascaded to get a bandpass filter, provided that  $Q$  is less than 1. When  $Q$  is greater than 1, we have a narrowband filter rather than a wideband filter.

## SEC. 21-10 BANDSTOP FILTERS

Bandstop filters can be used to notch out a specific frequency such as the 60-Hz hum induced in circuits by ac power lines. With a Sallen-Key notch filter, the voltage gain controls the  $Q$  of the circuit. The voltage gain must be less than 2 to avoid oscillations.

## SEC. 21-11 THE ALL-PASS FILTER

Somewhat of a misnomer, the all-pass filter does more than pass all frequencies

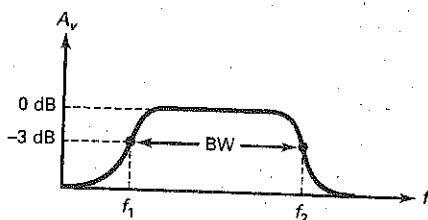
with no attenuation. This type of filter is designed to control the phase of the output signal. Especially important is the use of an all-pass filter as a phase or time-delay equalizer. With one of the other filters producing the desired frequency response and an all-pass filter producing the desired phase response, the overall filter has a linear phase response, equivalent to a maximally flat time delay.

## SEC. 21-12 BIQUADRATIC AND STATE-VARIABLE FILTERS

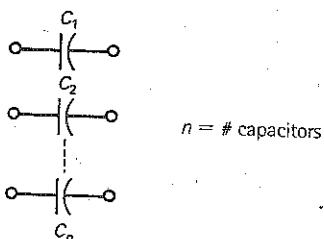
The biquadratic or TT filters use three or four op amps. Although more complex, the biquadratic filter offers lower component sensitivity and easier tuning. This type of filter also has simultaneous low-pass and bandpass outputs, or high-pass and bandstop outputs. The state-variable or KHN filters also use three or more op amps. When a fourth op amp is used, it offers easy tuning because voltage gain, center frequency, and  $Q$  are all independently tunable.

## Definitions

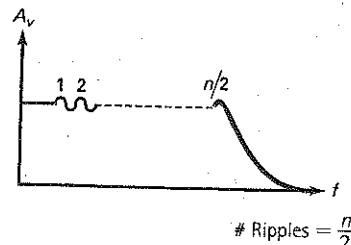
(21-1) Bandwidth:



(21-4) Order of a filter:



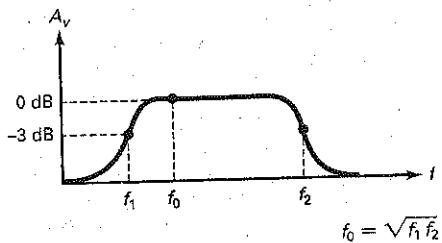
(21-5) Number of ripples:



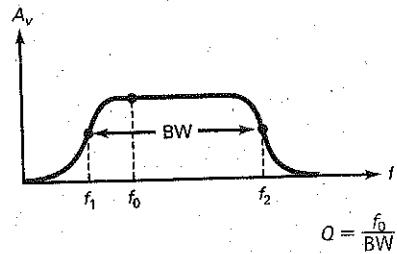
$$\# \text{ Ripples} = \frac{n}{2}$$

## Derivations

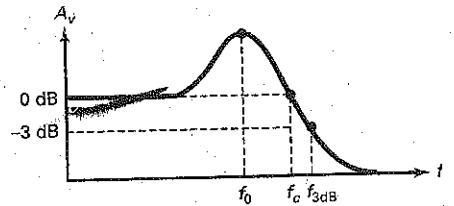
(21-2) Center frequency:



(21-3) Q of stage:



(21-2?) to (21-24) Center, cutoff, and 3-dB frequencies:



$$\begin{aligned} f_0 &= K_0 f_p \\ f_c &= K_c f_p \\ f_{3dB} &= K_3 f_p \end{aligned}$$

## Student Assignments

1. The region between the passband and the stopband is called the
  - Attenuation
  - Center
  - Transition
  - Ripple
2. The center frequency of a bandpass filter is always equal to the
  - Bandwidth
  - Geometric average of the cutoff frequencies
  - Bandwidth divided by Q
  - 3-dB frequency
3. The Q of a narrowband filter is always
  - Small
  - Equal to BW divided by  $f_0$
  - Less than 1
  - Greater than 1
4. A bandstop filter is sometimes called a
  - Snubber
  - Phase shifter
  - Notch filter
  - Time-delay circuit
5. The all-pass filter has
  - No passband
  - One stopband
  - The same gain at all frequencies
  - A fast roll-off above cutoff
6. The approximation with a maximally flat passband is the
  - Chebyshev
  - Inverse Chebyshev
  - Elliptic
  - Cauer
7. The approximation with a rippled passband is the
  - Butterworth
  - Inverse Chebyshev
  - Elliptic
  - Bessel
8. The approximation that distorts digital signals the least is the
  - Butterworth
  - Chebyshev
  - Elliptic
  - Bessel
9. If a filter has six second-order stages and one first-order stage, the order is
  - 2
  - 6
  - 7
  - 13
10. If a Butterworth filter has nine second-order stages, its roll-off rate is
  - 20 dB per decade
  - 40 dB per decade
  - 180 dB per decade
  - 360 dB per decade
11. If  $n = 10$ , the approximation with the fastest roll-off in the transition region is
  - Butterworth
  - Chebyshev
  - Inverse Chebyshev
  - Elliptic
12. The elliptic approximation has a
  - Slow roll-off rate compared to the Cauer approximation
  - Rippled stopband
  - Maximally flat passband
  - Monotonic stopband

13. Linear phase shift is equivalent to a
- $Q$  of 0.707
  - Maximally flat stopband
  - Constant time delay
  - Rippled passband
14. The filter with the slowest roll-off rate is the
- Butterworth
  - Chebyshev
  - Elliptic
  - Bessel
15. A first-order active-filter stage has
- One capacitor
  - Two op amps
  - Three resistors
  - A high  $Q$
16. A first-order stage cannot have a
- Butterworth response
  - Chebyshev response
  - Maximally flat passband
  - Roll-off rate of 20 dB per decade
17. Sallen-Key filters are also called
- VCVS filters
  - MFB filters
  - Biquadratic filters
  - State-variable filters
18. To build a tenth-order filter, we should cascade
- 10 first-order stages
  - 5 second-order stages
  - 3 third-order stages
  - 2 fourth-order stages
19. To get a Butterworth response with an eighth-order filter, the stages need to have
- Equal  $Q$ s
  - Unequal center frequencies
  - Inductors
  - Staggered  $Q$ s
20. To get a Chebyshev response with a twelfth-order filter, the stages need to have
- Equal  $Q$ s
  - Equal center frequencies
  - Staggered bandwidths
  - Staggered pole frequencies and  $Q$ s
21. The  $Q$  of a Sallen-Key equal-component second-order stage depends on the
- Voltage gain
  - Center frequency
  - Bandwidth
  - GBW of the op amp
22. With Sallen-Key high-pass filters, the pole frequency must be
- Added to the  $K$  values
  - Subtracted from the  $K$  values
  - Multiplied by the  $K$  values
  - Divided by the  $K$  values
23. If bandwidth increases,
- The center frequency decreases
  - $Q$  decreases
  - The roll-off rate increases
  - Ripples appear in the stopband
24. When  $Q$  is greater than 1, a bandpass filter should be built with
- Low-pass and high-pass stages
  - MFB stages
  - Notch stages
  - All-pass stages
25. The all-pass filter is used when
- High roll-off rates are needed
  - Phase shift is important
  - A maximally flat passband is needed
  - A rippled stopband is important
26. A second-order all-pass filter can vary the output phase from
- 90 to  $-90^\circ$
  - 0 to  $-360^\circ$
  - 0 to  $-180^\circ$
  - 0 to  $-720^\circ$
27. The all-pass filter is sometimes called a
- Tow-Thomas filter
  - Delay equalizer
  - KHN filter
  - State-variable filter
28. The biquadratic filter
- Has low component sensitivity
  - Uses three or more op amps
  - Is also called a Tow-Thomas filter
  - All of the above
29. The state-variable filter
- Has a low-pass, high-pass, and bandpass output
  - Is difficult to tune
  - Has high component sensitivity
  - Uses fewer than three op amps
30. If GBW is limited, the  $Q$  of the stage will
- Remain the same
  - Double
  - Decrease
  - Increase
31. To correct for limited GBW, a designer may use
- A constant time delay
  - Predistortion
  - Linear phase shift
  - A rippled passband

## Problems

### SEC. 21-1 IDEAL RESPONSES

- 21-1 A bandpass filter has lower and upper cutoff frequencies of 445 and 7800 Hz, respectively. What are the bandwidth, center frequency, and  $Q$ ? Is this a wideband or narrowband filter?
- 21-2 If a bandpass filter has cutoff frequencies of 20 and 22.5 kHz, what are the bandwidth, center frequency, and  $Q$ ? Is this a wideband or narrowband filter?

21-3 Identify the following filters as narrowband or wideband:

- $f_1 = 2.3$  kHz and  $f_2 = 4.5$  kHz
- $f_1 = 47$  kHz and  $f_2 = 75$  kHz
- $f_1 = 2$  Hz and  $f_2 = 5$  Hz
- $f_1 = 80$  Hz and  $f_2 = 160$  Hz

### SEC. 21-2 APPROXIMATE RESPONSES

- 21-4 An active filter contains 7 capacitors. What is the order of the filter?

- 21-5 If a Butterworth filter contains 10 capacitors, what is its roll-off rate?
- 21-6 A Chebyshev filter has 14 capacitors. How many ripples does its passband have?

### SEC. 21-3 PASSIVE FILTERS

- 21-7 The filter of Fig. 21-17 has  $L = 20 \text{ mH}$ ,  $C = 5 \mu\text{F}$ , and  $R = 600 \Omega$ . What is the resonant frequency? What is the  $Q$ ?
- 21-8 If the inductance is reduced by a factor of 2 in Prob. 21-7, what is the resonant frequency? What is the  $Q$ ?

### SEC. 21-4 FIRST-ORDER STAGES

- 21-9 In Fig. 21-21a,  $R_1 = 15 \text{ k}\Omega$  and  $C_1 = 270 \text{ nF}$ . What is the cutoff frequency?
- 21-10 **Multisim** In Fig. 21-21b,  $R_1 = 7.5 \text{ k}\Omega$ ,  $R_2 = 33 \text{ k}\Omega$ ,  $R_3 = 20 \text{ k}\Omega$ , and  $C_1 = 680 \text{ pF}$ . What is the cutoff frequency? What is the voltage gain in the passband?
- 21-11 **Multisim** In Fig. 21-21c,  $R_1 = 2.2 \text{ k}\Omega$ ,  $R_2 = 47 \text{ k}\Omega$ , and  $C_1 = 330 \text{ pF}$ . What is the cutoff frequency? What is the voltage gain in the passband?
- 21-12 In Fig. 21-22a,  $R_1 = 10 \text{ k}\Omega$  and  $C_1 = 15 \text{ nF}$ . What is the cutoff frequency?
- 21-13 In Fig. 21-22b,  $R_1 = 12 \text{ k}\Omega$ ,  $R_2 = 24 \text{ k}\Omega$ ,  $R_3 = 20 \text{ k}\Omega$ , and  $C_1 = 220 \text{ pF}$ . What is the cutoff frequency? What is the voltage gain in the passband?
- 21-14 In Fig. 21-22c,  $R_1 = 8.2 \text{ k}\Omega$ ,  $C_1 = 560 \text{ pF}$ , and  $C_2 = 680 \text{ pF}$ . What is the cutoff frequency? What is the voltage gain in the passband?

### SEC. 21-5 VCVS UNITY-GAIN SECOND-ORDER LOW-PASS FILTERS

- 21-15 **Multisim** In Fig. 21-24,  $R = 75 \text{ k}\Omega$ ,  $C_1 = 100 \text{ pF}$ , and  $C_2 = 200 \text{ pF}$ . What are the pole frequency and  $Q$ ? What are the cutoff and 3-dB frequencies?
- 21-16 In Fig. 21-25,  $R = 51 \text{ k}\Omega$ ,  $C_1 = 100 \text{ pF}$ , and  $C_2 = 680 \text{ pF}$ . What are the pole frequency and  $Q$ ? What are the cutoff and 3-dB frequencies?

### SEC. 21-7 VCVS EQUAL-COMPONENT LOW-PASS FILTERS

- 21-17 In Fig. 21-31,  $R_1 = 51 \text{ k}\Omega$ ,  $R_2 = 30 \text{ k}\Omega$ ,  $R = 33 \text{ k}\Omega$ , and  $C = 220 \text{ pF}$ . What are the pole frequency and  $Q$ ? What are the cutoff and 3-dB frequencies?
- 21-18 In Fig. 21-31,  $R_1 = 33 \text{ k}\Omega$ ,  $R_2 = 33 \text{ k}\Omega$ ,  $R = 75 \text{ k}\Omega$ , and  $C = 100 \text{ pF}$ . What are the pole frequency and  $Q$ ? What are the cutoff and 3-dB frequencies?

## Critical Thinking

- 21-31 A bandpass filter has a center frequency of 50 kHz and a  $Q$  of 20. What are the cutoff frequencies?
- 21-32 A bandpass filter has an upper cutoff frequency of 84.7 kHz and a bandwidth of 12.3 kHz. What is the lower cutoff frequency?
- 21-33 You are testing a Butterworth filter with the following specifications:  $n = 10$ ,  $A_p = 3 \text{ dB}$ , and  $f_c = 2 \text{ kHz}$ . What is the attenuation at each of the following frequencies: 4, 8, and 20 kHz?

- 21-19 In Fig. 21-31,  $R_1 = 75 \text{ k}\Omega$ ,  $R_2 = 56 \text{ k}\Omega$ ,  $R = 68 \text{ k}\Omega$ , and  $C = 120 \text{ pF}$ . What are the pole frequency and  $Q$ ? What are the cutoff and 3-dB frequencies?

### SEC. 21-8 VCVS HIGH-PASS FILTERS

- 21-20 In Fig. 21-35a,  $R_1 = 56 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$ , and  $C = 680 \text{ pF}$ . What are the pole frequency and  $Q$ ? What are the cutoff and 3-dB frequencies?

- 21-21 **Multisim** In Fig. 21-35a,  $R_1 = 91 \text{ k}\Omega$ ,  $R_2 = 15 \text{ k}\Omega$ , and  $C = 220 \text{ nF}$ . What are the pole frequency and  $Q$ ? What are the cutoff and 3-dB frequencies?

### SEC. 21-9 MFB BANDPASS FILTERS

- 21-22 In Fig. 21-39,  $R_1 = 2 \text{ k}\Omega$ ,  $R_2 = 56 \text{ k}\Omega$ , and  $C = 270 \text{ pF}$ . What are the voltage gain,  $Q$ , and center frequency?

- 21-23 In Fig. 21-40,  $R_1 = 3.6 \text{ k}\Omega$ ,  $R_2 = 7.5 \text{ k}\Omega$ ,  $R_3 = 27 \Omega$ , and  $C = 22 \text{ nF}$ . What are the voltage gain,  $Q$ , and center frequency?

- 21-24 In Fig. 21-41,  $R_1 = 28 \text{ k}\Omega$ ,  $R_3 = 1.8 \text{ k}\Omega$ , and  $C = 1.8 \text{ nF}$ . What are the voltage gain,  $Q$ , and center frequency?

### SEC. 21-10 BANDSTOP FILTERS

- 21-25 **Multisim** What are the voltage gain, center frequency, and  $Q$  for the bandstop filter shown in Fig. 21-43 if  $R = 56 \text{ k}\Omega$ ,  $C = 180 \text{ nF}$ ,  $R_1 = 20 \text{ k}\Omega$ , and  $R_2 = 10 \text{ k}\Omega$ ? What is the bandwidth?

### SEC. 21-11 THE ALL-PASS FILTER

- 21-26 In Fig. 21-45a,  $R = 3.3 \text{ k}\Omega$  and  $C = 220 \text{ nF}$ . What is the center frequency? The phase shift 1 octave above the center frequency?

- 21-27 **Multisim** In Fig. 21-45b,  $R = 47 \text{ k}\Omega$  and  $C = 6.8 \text{ nF}$ . What is the center frequency? The phase shift 1 octave below the center frequency?

### SEC. 21-12 BIQUADRATIC AND STATE-VARIABLE FILTERS

- 21-28 In Fig. 21-50,  $R_1 = 24 \text{ k}\Omega$ ,  $R_2 = 100 \text{ k}\Omega$ ,  $R_3 = 10 \text{ k}\Omega$ ,  $R_4 = 15 \text{ k}\Omega$ , and  $C = 3.3 \text{ nF}$ . What are the voltage gain,  $Q$ , center frequency, and bandwidth?

- 21-29 In Prob. 21-28,  $R_3$  is varied from  $10 \text{ k}\Omega$  to  $2 \text{ k}\Omega$ . What are the maximum center frequency and the maximum  $Q$ ? What are the minimum and maximum bandwidths?

- 21-30 In Fig. 21-51,  $R = 6.8 \text{ k}\Omega$ ,  $C = 5.6 \text{ nF}$ ,  $R_1 = 6.8 \text{ k}\Omega$ , and  $R_2 = 100 \text{ k}\Omega$ . What are the voltage gain,  $Q$ , and center frequency?

- 21-34 A Sallen-Key unity-gain low-pass filter has a cutoff frequency of 5 kHz. If  $n = 2$  and  $R = 10 \text{ k}\Omega$ , what do  $C_1$  and  $C_2$  equal for a Butterworth response?

- 21-35 A Chebyshev Sallen-Key unity-gain low-pass filter has a cutoff frequency of 7.5 kHz. The ripple depth is 12 dB. If  $n = 2$  and  $R = 25 \text{ k}\Omega$ , what do  $C_1$  and  $C_2$  equal?

## Job Interview Questions

1. Draw the four brick wall responses. Identify the passband, stopband, and cutoff frequencies of each.
2. Describe the five approximations used in filter design. Use sketches as needed to show what happens in the passbands and stopbands.
3. In digital systems, filters need a linear phase response or maximally flat time delay. What does this mean, and why is it important?
4. Tell me what you can about how a tenth-order low-pass Chebyshev filter is implemented. Your discussion should include the center frequencies and  $Q_s$  of the stages.
5. To get a fast roll-off and a linear-phase response, somebody has cascaded a Butterworth filter with an all-pass filter. Tell me what each of these filters does.
6. What are the distinguishing features of the response in the passband? In the stopband?
7. What is an all-pass filter?
8. What does the frequency response of a filter measure or indicate?
9. What is the roll-off rate (per decade and per octave) for an active filter?
10. What is an MFB filter and where is it used?
11. Which type of filter is used for delay equalization?

## Self-Test Answers

- |       |       |       |
|-------|-------|-------|
| 1. c  | 12. b | 23. b |
| 2. b  | 13. c | 24. b |
| 3. d  | 14. d | 25. b |
| 4. c  | 15. a | 26. c |
| 5. c  | 16. b | 27. b |
| 6. b  | 17. a | 28. d |
| 7. c  | 18. b | 29. a |
| 8. d  | 19. d | 30. d |
| 9. d  | 20. d | 31. b |
| 10. d | 21. a |       |
| 11. d | 22. d |       |

## Practice Problem Answers

- |   |  |  |
|---|--|--|
| 21-1 $f_c = 34.4 \text{ kHz}$   | 21-6 $A_v = 1.59; Q = 0.709; f_p = 21.9 \text{ kHz}$   | 21-11 $\text{BW} = 1.94 \text{ kHz}; f_{0(\min)} = 15 \text{ kHz}; f_{0(\max)} = 35.5 \text{ kHz}$ |
| 21-2 $f_c = 16.8 \text{ kHz}$   | 21-7 $A_v = 1.27; Q = 0.578; f_p = 4.82 \text{ kHz}; f_c = 3.79 \text{ kHz}$   | 21-12 $R_2 = 12 \text{ kHz}; C = 60 \text{ nF}$  |
| 21-3 $Q = 0.707; f_p = 13.7 \text{ kHz}; f_c = 13.7 \text{ kHz}$  | 21-9 $Q = 0.707; f_p = 998 \text{ Hz}; f_c = 998 \text{ Hz}$   |  |
| 21-4 $C_2 = 904 \text{ pF}$   | 21-10 $A_v = 2.75; Q = 4; f_p = 5.31 \text{ kHz}; K_0 = 0.98; K_C = 1.38; K_3 = 1.53; A_p = 12 \text{ dB}; f_0 = 5.42 \text{ kHz}; f_c = 3.85 \text{ kHz}; f_{3dB} = 3.47 \text{ kHz}$ |  |
| 21-5 $Q = 3; f_p = 3.1 \text{ kHz}; K_0 = 0.96; K_C = 1.35; K_3 = 1.52; A_p = 9.8 \text{ dB}; f_c = 4.19 \text{ kHz}; f_{3dB} = 4.71 \text{ kHz}$ |  |  |

chapter

# 22

# Nonlinear Op-Amp Circuit

- Monolithic op amps are inexpensive, versatile, and reliable. They can be used not only for linear circuits like voltage amplifiers, current sources, and active filters but also for nonlinear circuits such as comparators, waveshapers, and active-diode circuits. The output of a nonlinear op-amp circuit usually has a different shape from the input signal because the op amp saturates during part of the input cycle. Because of this, we have to analyze two different modes of operation to see what happens during an entire cycle.

## Objectives

After studying this chapter, you should be able to:

- Explain how a comparator works and describe the importance of the reference point.
- Discuss comparators that have positive feedback and calculate the trip points and hysteresis for these circuits.
- Identify and discuss waveform conversion circuits.
- Identify and discuss waveform generation circuits.
- Describe how several active diode circuits work.
- Explain integrators and differentiators.
- Explain the circuit operation of a Class-D amplifier.

## Chapter Outline

- 22-1 Comparators with Zero Reference
- 22-2 Comparators with Nonzero References
- 22-3 Comparators with Hysteresis
- 22-4 Window Comparator
- 22-5 The Integrator
- 22-6 Waveform Conversion
- 22-7 Waveform Generation
- 22-8 Another Triangular Generator
- 22-9 Active Diode Circuits
- 22-10 The Differentiator
- 22-11 Class-D Amplifier

## Vocabulary

active half-wave rectifier	Lissajous pattern	speed-up capacitor
active peak detector	nonlinear circuits	thermal noise
active positive clammer	open-collector comparator	threshold
active positive clipper	oscillators	transfer characteristic
Class-D amplifier	pullup resistor	trip point
comparator	pulse-width-modulated (PWM)	window comparator
differentiator	relaxation oscillator	zero-crossing detector
hysteresis	Schmitt trigger	
integrator		

## 22-1 Comparators with Zero Reference

Often we want to compare one voltage with another to see which is larger. In this situation, a **comparator** may be the perfect solution. A comparator is similar to an op amp because it has two input voltages (noninverting and inverting) and one output voltage. It differs from a linear op-amp circuit because it has a two-state output, either a low or a high voltage. Because of this, comparators are often used to interface with analog and digital circuits.

### GOOD TO KNOW

### Basic Idea

The output of the comparator in Fig. 22-1 can be characterized as *digital* in the sense that the output is always either high at  $+V_{\text{sat}}$  or low at  $-V_{\text{sat}}$ .

The simplest way to build a comparator is to connect an op amp without feedback resistors, as shown in Fig. 22-1a. Because of the high open-loop voltage gain, a positive input voltage produces positive saturation, and a negative input voltage produces negative saturation.

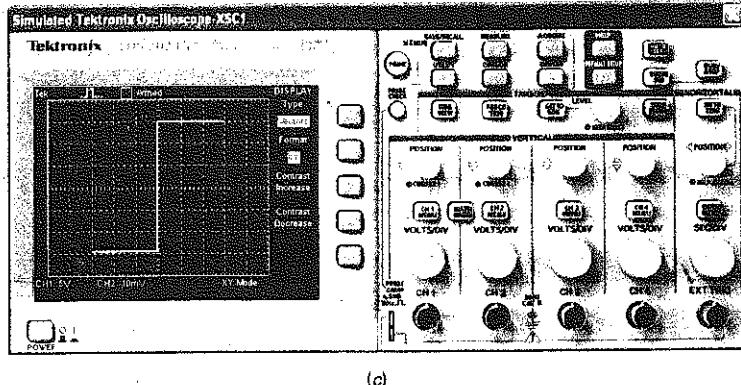
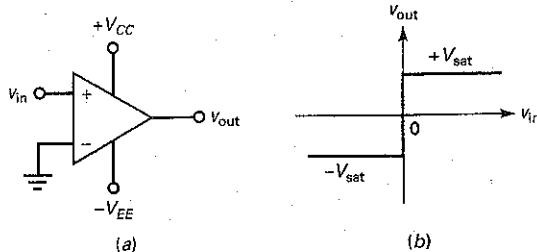
The comparator of Fig. 22-1a is called a **zero-crossing detector** because the output voltage ideally switches from low to high or vice versa whenever the input voltage crosses zero. Figure 22-1b shows the input-output response of a zero-crossing detector. The minimum input voltage that produces saturation is:

$$v_{\text{in(min)}} = \frac{\pm V_{\text{sat}}}{A_{\text{VOL}}} \quad (22-1)$$

If  $V_{\text{sat}} = 14$  V, the output swing of the comparator is from approximately  $-14$  to  $+14$  V. If the open-loop voltage gain is 100,000, the input voltage needed to produce saturation is:

$$v_{\text{in(min)}} = \frac{\pm 14 \text{ V}}{100,000} = \pm 0.14 \text{ mV}$$

Figure 22-1 (a) Comparator; (b) input/output response; (c) 741C response.



This means that an input voltage more positive than  $+0.014$  mV drives the comparator into positive saturation, and an input voltage more negative than  $-0.014$  mV drives it into negative saturation.

Input voltages used with comparators are usually much greater than  $\pm 0.014$  mV. This is why the output voltage is a two-state output, either  $+V_{\text{sat}}$  or  $-V_{\text{sat}}$ . By looking at the output voltage, we can instantly tell whether the input voltage is: greater than or less than zero.

### Lissajous Pattern

A Lissajous pattern appears on an oscilloscope when harmonically related signals are applied to the horizontal and vertical inputs. One convenient way to display the input/output response of any circuit is with a Lissajous pattern in which the two harmonically related signals are the input and output voltages of the circuit.

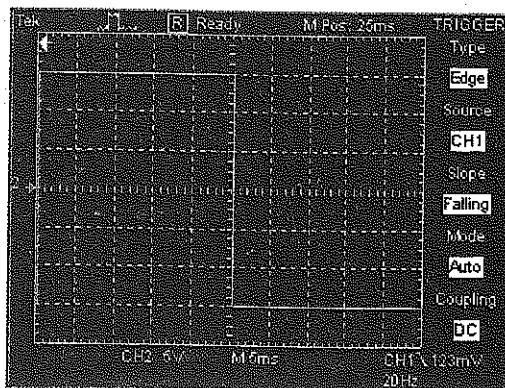
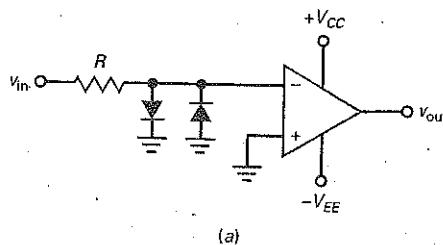
For instance, Fig. 22-1c shows the input/output response for a 741C with supplies of  $\pm 15$  V. Channel 1 (the vertical axis) has a sensitivity of 5 V/Div. As we can see, the output voltage is either  $-14$  or  $+14$  V, depending on whether the comparator is in negative or positive saturation.

Channel 2 (the horizontal axis) has sensitivity of 10 mV/Div. In Fig. 22-1c, the transition appears to be vertical. This means that the slightest positive input voltage produces positive saturation, and the slightest negative input produces negative saturation.

### Inverting Comparator

Sometimes, we may prefer to use an inverting comparator like Fig. 22-2a. The noninverting input is grounded. The input signal drives the inverting input of the comparator. In this case, a slightly positive input voltage produces a maximum

**Figure 22-2** (a) Inverting comparator with clamping diodes; (b) input/output response.



negative output, as shown in Fig. 22-2b. On the other hand, a slightly negative input voltage produces a maximum positive output.

### Diode Clamps

Section 4-10 discussed the use of *diode clamps* to protect sensitive circuits. Figure 22-2a is a practical example. Here we see two diode clamps protecting the comparator against excessively large input voltages. For instance, the LF311 is an IC comparator with an absolute maximum input rating of  $\pm 15$  V. If the input voltage exceeds these limits, the LF311 will be destroyed.

With some comparators, the maximum input voltage rating may be as little as  $\pm 5$  V, whereas with others it may be more than  $\pm 30$  V. In any case, we can protect a comparator against destructively large input voltages by using the diode clamps shown in Fig. 22-2a. These diodes have no effect on the operation of the circuit as long as the magnitude of the input voltage is less than 0.7 V. When the magnitude of the input voltage is greater than 0.7 V, one of the diodes will turn on and clamp the magnitude of the inverting input voltage to approximately 0.7 V.

Some ICs are optimized for use as comparators. These IC comparators often have diode clamps built into their input stages. When using one of these comparators, we have to add an external resistor in series with the input terminal. This series resistor will limit the internal diode currents to a safe level.

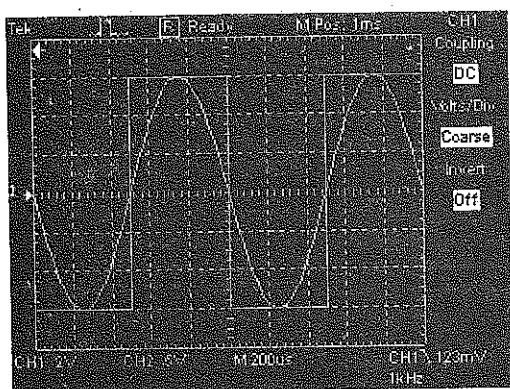
### Converting Sine Waves to Square Waves

The **trip point** (also called the **threshold** or **reference**) of a comparator is the input voltage that causes the output voltage to switch states (from low to high or from high to low). In the noninverting and inverting comparators discussed earlier, the trip point is zero because this is the value of input voltage where the output switches states. Since a zero-crossing detector has a *two-state output*, any periodic input signal that crosses zero threshold will produce a rectangular output waveform.

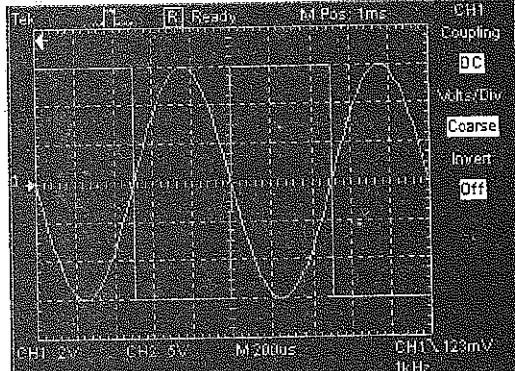
For instance, if a sine wave is the input to a noninverting comparator with a threshold of 0 V, the output will be the square wave shown in Fig. 22-3a. As we can see, the output of a zero-crossing detector switches states each time the input voltage crosses the zero threshold.

Figure 22-3b shows the input sine wave and the output square wave for an inverting comparator with a threshold of 0 V. With this zero-crossing detector, the output square wave is 180° out of phase with the input sine wave.

**Figure 22-3** Comparator converts sine waves to square waves: (a) Noninverting; (b) inverting.

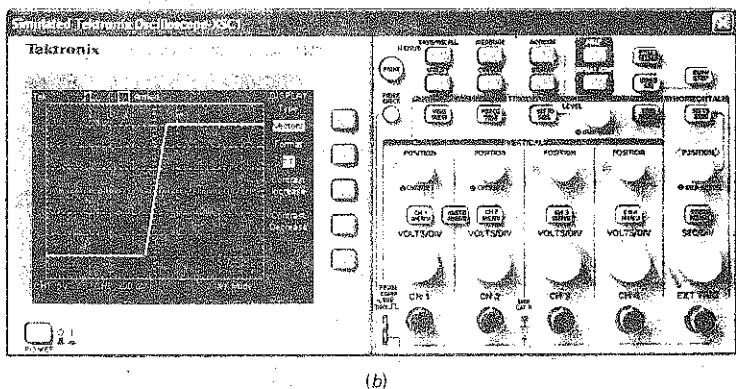
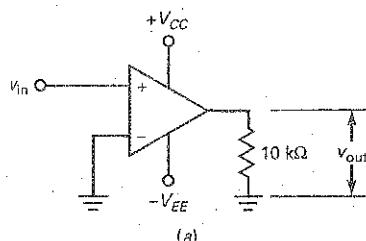


(a)



(b)

Figure 22-4 Narrow linear region of typical comparator.



## Linear Region

Figure 22-4a shows a zero-crossing detector. If this comparator had an infinite open-loop gain, the transition between negative and positive saturation would be vertical. In Fig. 22-4b, the transition appears to be vertical because the sensitivity of the 2 channel is  $10\text{ mV/Div}$ .

When the sensitivity of the 2 channel is changed to  $200\text{ }\mu\text{V/Div}$ , we can see that the transition is not vertical, as shown in Fig. 22-4b. It takes approximately  $\pm 100\text{ }\mu\text{V}$  to get positive or negative saturation. This is typical for a comparator. The narrow input region between approximately  $-100$  to  $+100\text{ }\mu\text{V}$  is called the *linear region of the comparator*. During a zero crossing, a changing input signal usually passes through the linear region so quickly that we see only a sudden jump between negative and positive saturation, or vice versa.

## Interfacing Analog and Digital Circuits

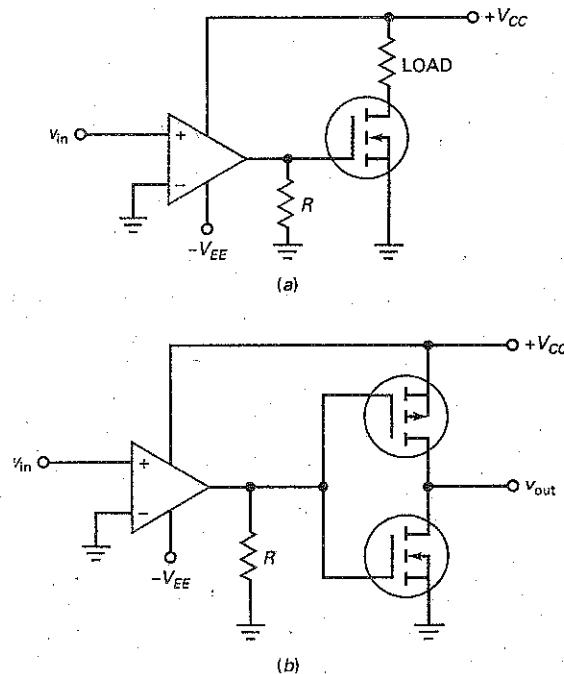
Comparators usually interface at their outputs with digital circuits such as CMOS, EMOS, or TTL (stands for *transistor-transistor logic*, a family of digital circuits).

Figure 22-5a shows how a zero-crossing detector can interface with an EMOS circuit. Whenever the input voltage is greater than zero, the output of the comparator is high. This turns on the power FET and produces a large load current.

Figure 22-5b shows a zero-crossing detector interfacing with a CMOS inverter. The idea is basically the same. A comparator input greater than zero produces a high input to the CMOS inverter.

Most EMOS devices can handle input voltages greater than  $\pm 15\text{ V}$ , and most CMOS devices can handle input voltages up to  $\pm 15\text{ V}$ . Therefore, we can interface the output of a typical comparator without any level shifting or clamping. TTL logic, on the other hand, operates with lower input voltages. Because of this,

Figure 22-5 Comparator interfaces with (a) power FET; (b) CMOS.



interfacing a comparator with TTL requires a different approach (to be discussed in the next section).

### Clamping Diodes and Compensating Resistors

When a current-limiting resistor is used with clamping diodes, a compensating resistor of equal size may be used on the other input of the comparator, as shown in Fig. 22-6. This is still a zero-crossing detector, except that it now has a compensating resistor to eliminate the effect of input bias current.

As before, the diodes are normally off and have no effect on the operation of the circuit. It is only when the input tries to exceed  $\pm 0.7$  V that one of the clamping diodes turns on and protects the comparator against excessive input voltage.

### Bounded Output

The output swing of a zero-crossing detector may be too large in some applications. If so, we can *bound the output* by using back-to-back zener diodes, as

Figure 22-6 Using a compensating resistor to minimize the effect of  $I_{in(bias)}$ .

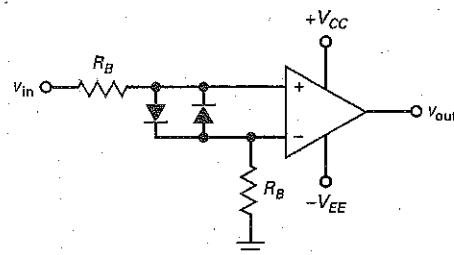
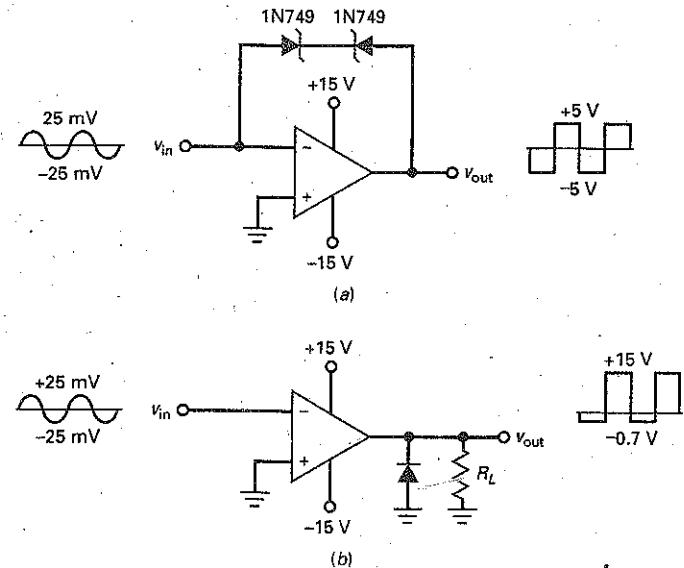


Figure 22-7 Bounded outputs: (a) Zener diodes; (b) rectifier diode.



shown in Fig. 22-7a. In this circuit, the inverting comparator has a bounded output because one of the diodes will be conducting in the forward direction and the other will be operating in the breakdown region.

For instance, a 1N749 has a zener voltage of 4.3 V. Therefore, the voltage across the two diodes will be approximately  $\pm 5\text{ V}$ . If the input voltage is a sine wave with a peak value of  $25\text{ mV}$ , then the output voltage will be an inverted square wave with a peak voltage of  $5\text{ V}$ .

Figure 22-7b shows another example of a bounded output. This time, the output diode will clip off the negative half cycles of the output voltage. Given an input sine wave with a peak of  $25\text{ mV}$ , the output is bounded between  $-0.7$  and  $+15\text{ V}$  as shown.

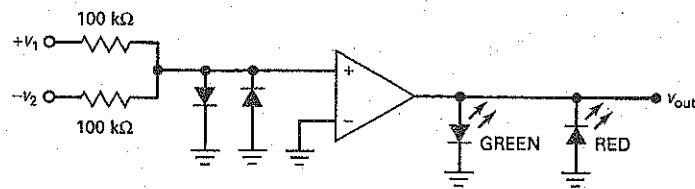
A third approach to bounding the output is to connect zener diodes across the output. For instance, if we connect the back-to-back zener diodes of Fig. 22-7a across the output, the output will be bounded at  $\pm 5\text{ V}$ .

## Example 22-1

Multisim

What does the circuit of Fig. 22-8 do?

Figure 22-8 Comparing voltages of different polarities.

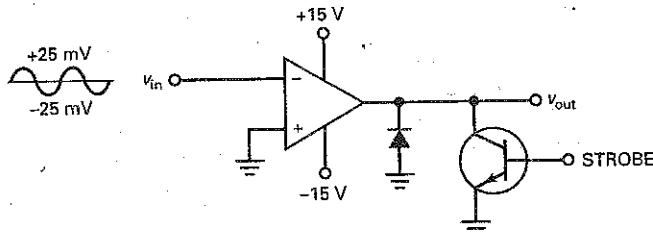


**SOLUTION** This circuit compares two voltages of opposite polarity to determine which is greater. If the magnitude of  $v_1$  is greater than the magnitude of  $v_2$ , the noninverting input is positive, the comparator output is positive, and the green LED is on. On the other hand, if the magnitude of  $v_1$  is less than the magnitude of  $v_2$ , the noninverting input is negative, the comparator output is negative, and the red LED is on.

## Example 22-2

What does the circuit of Fig. 22-9 do?

Figure 22-9 Bounded comparator with strobe.

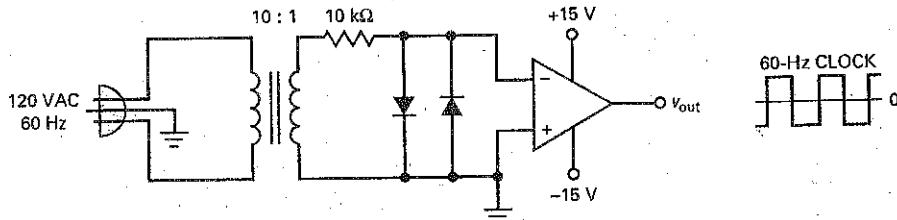


**SOLUTION** To begin with, the output diode clips off the negative half cycles. Figure 22-9 also contains a signal called a *strobe*. When the strobe is positive, the transistor saturates and pulls the output voltage down to approximately zero. When the strobe is zero, the transistor is cut off and the comparator output can swing positively. Therefore, the comparator output can swing from  $-0.7$  to  $+15$  V when the strobe is low. When the strobe is high, the output is disabled. In this circuit, the strobe is a signal used to turn the output off at certain times or under certain conditions.

## Example 22-3

What does the circuit of Fig. 22-10 do?

Figure 22-10 Generating a 60-Hz clock.



**SOLUTION** This is one way to create a *60-Hz clock*, a square-wave signal used as the basic timing mechanism for inexpensive digital clocks. The transformer steps the line voltage down to 12 V ac. The diode clamps then bound the input to  $\pm 0.7$  V. The inverting comparator produces an output square wave with a frequency of 60 Hz. The output signal is called a *clock* because its frequency can be used to get seconds, minutes, and hours.

A digital circuit called a *frequency divider* can divide the 60 Hz by 60 to get a square wave with a period of 1 s. Another divide-by-60 circuit can divide this signal to get a square wave with a period of 1 min. A final divide-by-60 circuit produces a square wave with a period of 1 hr. Using the three square waves (1 s, 1 min, 1 hr) with other digital circuits and seven-segment LED indicators, we can display the time of day numerically.

## 22-2 Comparators with Nonzero References

In some applications a threshold voltage different from zero may be preferred. By biasing either input, we can change the threshold voltage as needed.

### Moving the Trip Point

In Fig. 22-11a, a voltage divider produces the following reference voltage for the inverting input:

$$v_{\text{ref}} = \frac{R_2}{R_1 + R_2} V_{CC} \quad (22-2)$$

When  $v_{in}$  is greater than  $v_{\text{ref}}$ , the differential input voltage is positive and the output voltage is high. When  $v_{in}$  is less than  $v_{\text{ref}}$ , the differential input voltage is negative and the output voltage is low.

A bypass capacitor is typically used on the inverting input, as shown in Fig. 22-11a. This reduces the amount of power-supply ripple and other noise appearing at the inverting input. To be effective, the cutoff frequency of this bypass circuit should be much lower than the ripple frequency of the power supply. The cutoff frequency is given by:

$$f_c = \frac{1}{2\pi(R_1 \parallel R_2)C_{BY}} \quad (22-3)$$

Figure 22-11b shows the transfer characteristic (input/output response). The trip point is now equal to  $v_{\text{ref}}$ . When  $v_{in}$  is greater than  $v_{\text{ref}}$ , the output of the comparator goes into positive saturation. When  $v_{in}$  is less than  $v_{\text{ref}}$ , the output goes into negative saturation.

**Figure 22-11** (a) Positive threshold; (b) positive input/output response; (c) negative threshold; (d) negative input/output response.

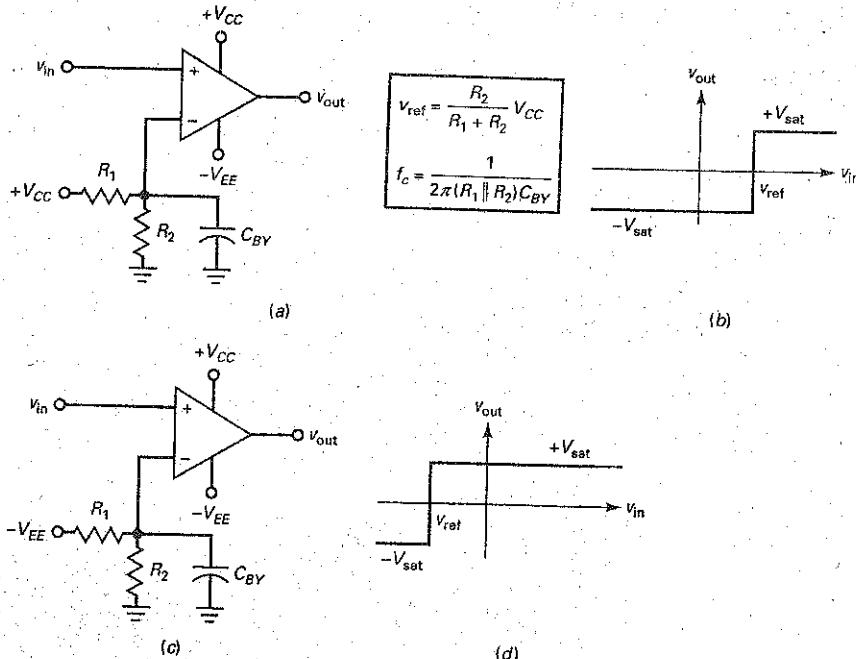
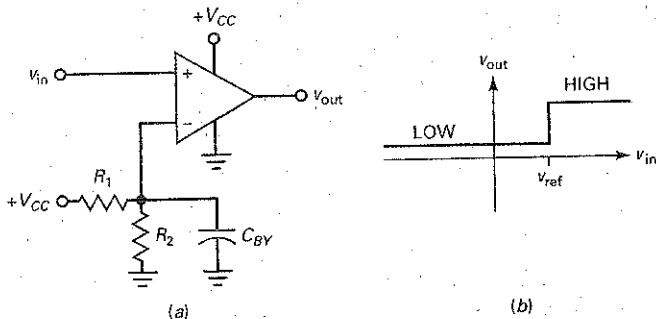


Figure 22-12 (a) Single-supply comparator; (b) input/output response.



A comparator like this is sometimes called a *limit detector* because a positive output indicates that the input voltage exceeds a specific limit. With different values of  $R_1$  and  $R_2$ , we can set the limit anywhere between 0 and  $V_{CC}$ . If a negative limit is preferred, connect  $-V_{EE}$  to the voltage divider, as shown in Fig. 22-11c. Now a negative reference voltage is applied to the inverting input. When  $v_{in}$  is more positive than  $v_{ref}$ , the differential input voltage is positive and the output is high, as shown in Fig. 22-11d. When  $v_{in}$  is more negative than  $v_{ref}$ , the output is low.

### Single-Supply Comparator

A typical op amp like the 741C can run on a single positive supply by grounding the  $-V_{EE}$  pin, as shown in Fig. 22-12a. The output voltage has only one polarity, either a low or a high positive voltage. For instance, with  $V_{CC}$  equal to  $+15$  V, the output swing is from approximately  $+1.5$  V (low state) to around  $+13.5$  V (high state).

When  $v_{in}$  is greater than  $v_{ref}$ , the output is high, as shown in Fig. 22-12b. When  $v_{in}$  is less than  $v_{ref}$ , the output is low. In either case, the output has a positive polarity. For many digital applications, this kind of positive output is preferred.

### IC Comparators

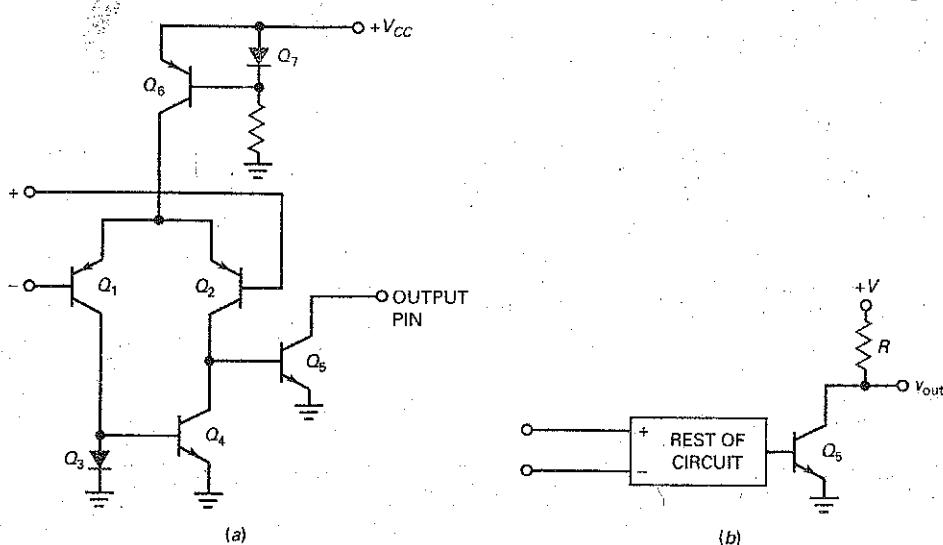
An op amp like a 741C can be used as a comparator, but it has speed limitations because of its slew rate. With a 741C, the output can change no faster than  $0.5$  V/ $\mu$ s. Because of this, a 741C takes more than  $50$   $\mu$ s to switch output states with supplies of  $\pm 15$  V. One solution to the slew-rate problem is to use a faster op amp like an LM318. Since it has a slew rate of  $70$  V/ $\mu$ s, it can switch from  $-V_{sat}$  to  $+V_{sat}$  in approximately  $0.3$   $\mu$ s.

Another solution is to eliminate the compensating capacitor found in a typical op amp. Since a comparator is always used as a nonlinear circuit, a compensating capacitor is unnecessary. A manufacturer can delete the compensating capacitor and significantly increase the slew rate. When an IC has been optimized for use as a comparator, the device is listed in a separate section of the manufacturer's data book. This is why you will find a section on op amps and another section on comparators in the typical data book.

### Open-Collector Devices

Figure 22-13a is a simplified schematic diagram for an **open-collector comparator**. Notice that it runs off a single positive supply. The input stage is a diff amp ( $Q_1$  and  $Q_2$ ). A current source  $Q_6$  supplies the tail current. The diff amp drives an active-load  $Q_4$ . The output stage is a single transistor  $Q_5$  with an open collector. This open collector allows the user to control the output swing of the comparator.

**Figure 22-13** (a) Simplified schematic diagram of IC comparator; (b) using pullup resistor with open collector output stage.



The typical op amp discussed in Chap. 18 has an output stage that can be described as an *active-pullup stage* because it contains two devices in a class B push-pull connection. With the active pullup, the upper device turns on and pulls the output up to the high output state. On the other hand, an open-collector output stage of Fig. 22-13a needs external components to be connected to it.

For the output stage to work properly, the user has to connect the open collector to an external resistor and supply voltage, as shown in Fig. 22-13b. The resistor is called a **pullup resistor** because it pulls the output voltage up to the supply voltage when  $Q_5$  is cut off. When  $Q_5$  is saturated, the output voltage is low. Since the output stage is a transistor switch, the comparator produces a two-state output.

With no compensating capacitor in the circuit, the output in Fig. 22-13a can slew very rapidly because only small stray capacitances remain in the circuit. The main limitation on the switching speed is the amount of capacitance across  $Q_5$ . This output capacitance is the sum of the internal collector capacitance and the external stray wiring capacitance.

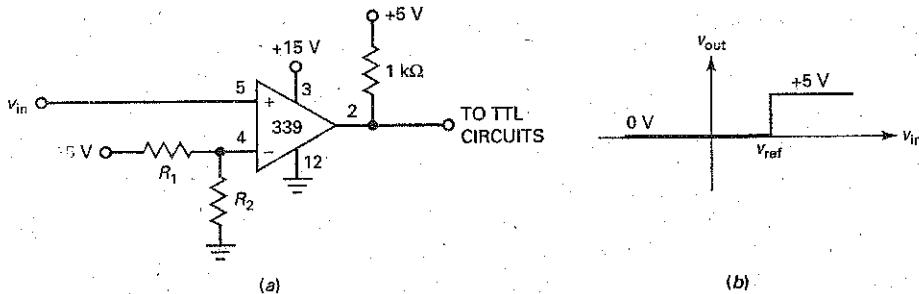
The output time constant is the product of the pullup resistance and the output capacitance. For this reason, the smaller the pullup resistance in Fig. 22-13b, the faster the output voltage can change. Typically,  $R$  is from a couple of hundred to a couple of thousand ohms.

Examples of IC comparators are the LM311, LM339, and NE529. They all have an open-collector output stage, which means that you have to connect the output pin to a pullup resistor and a positive supply voltage. Because of their high slew rates, these IC comparators can switch output states in a microsecond or less.

The LM339 is a *quad comparator*—four comparators in a single IC package. It can run off a single supply or off dual supplies. Because it is inexpensive and easy to use, the LM339 is a popular comparator for general-purpose applications.

Not all IC comparators have an open-collector output stage. Some, like the LM360, LM361, and LM760, have an active-collector output stage. The active pullup produces faster switching. These high-speed IC comparators require dual supplies.

Figure 22-14 (a) LM339 comparator; (b) input/output response.



### Driving TTL

The LM339 is an open-collector device. Figure 22-14a shows how an LM339 can be connected to interface with TTL devices. A positive supply of +15 V is used for the comparator, but the open collector of the LM339 is connected to a supply of +5 V through a pullup resistor of  $1\text{ k}\Omega$ . Because of this, the output swings between 0 and +5 V, as shown in Fig. 22-14b. This output signal is ideal for TTL devices because they are designed to work with supplies of +5 V.

### Example 22-4

MultiSim

In Fig. 22-15a, the input voltage is a sine wave with a peak value of 10 V. What is the trip point of the circuit? What is the cutoff frequency of the bypass circuit? What does the output waveform look like?

**SOLUTION** Since +15 V is applied to a 3:1 voltage divider, the reference voltage is:

$$v_{ref} = +5 \text{ V}$$

This is the trip point of the comparator. When the sine wave crosses through this level, the output voltage switches states.

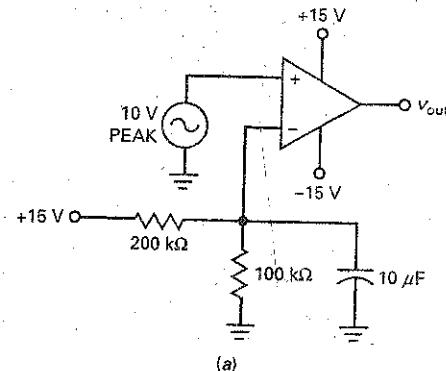
With Eq. (22-3), the cutoff frequency of the bypass circuit is:

$$\begin{aligned} f_c &= \frac{1}{2\pi(200\text{ k}\Omega \parallel 100\text{ k}\Omega)(10\text{ }\mu\text{F})} \\ &= 0.239 \text{ Hz} \end{aligned}$$

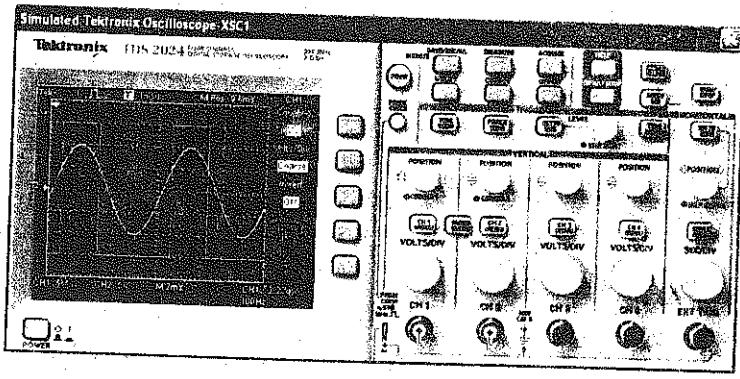
This low cutoff frequency means that any 60-Hz ripple on the reference supply voltage will be heavily attenuated.

Figure 22-15b shows the input sine wave. It has a peak value of 10 V. The rectangular output has a peak value of approximately 15 V. Notice how the output voltage switches states when the input sine wave crosses the trip point of +5 V.

Figure 22-15 Calculating duty cycle.



(a)



(b)

**PRACTICE PROBLEM 22-4** Using Fig. 22-15a, change the  $200\text{ k}\Omega$  resistor to  $100\text{ k}\Omega$  and the  $10\text{ }\mu\text{F}$  capacitor to  $4.7\text{ }\mu\text{F}$ . Solve for the circuit's trip point and cutoff frequency.

## Example 22-5

What is the duty cycle of the output waveform in Fig. 22-15b?

**SOLUTION** In Chap. 11, we defined the *duty cycle* as the pulse width divided by the period. Equation (11-22) gave this equivalent definition: Duty cycle equals the conduction angle divided by  $360^\circ$ .

In Fig. 22-15b, the sine wave has a peak value of  $10\text{ V}$ . Therefore, the input voltage is given by:

$$v_{in} = 10 \sin \theta$$

The rectangular output switches states when the input voltage crosses  $+5\text{ V}$ . At this point, the foregoing equation becomes:

$$5 = 10 \sin \theta$$

Now, we can solve for the angle  $\theta$  where switching occurs:

$$\sin \theta = 0.5$$

or

$$\theta = \arcsin 0.5 = 30^\circ \text{ and } 150^\circ$$

The first solution,  $\theta = 30^\circ$ , is where the output switches from low to high. The second solution,  $\theta = 150^\circ$ , is where the output switches from high to low. The duty cycle is:

$$D = \frac{\text{Conduction angle}}{360^\circ} = \frac{150^\circ - 30^\circ}{360^\circ} = 0.333$$

The duty cycle in Fig. 22-15b can be expressed as 33.3 percent.

## 22-3 Comparators with Hysteresis

If the input to a comparator contains a large amount of noise, the output will be erratic when  $v_{in}$  is near the trip point. One way to reduce the effect of noise is by using a comparator with positive feedback. The positive feedback produces two separate trip points that prevent a noisy input from producing false transitions.

### Noise

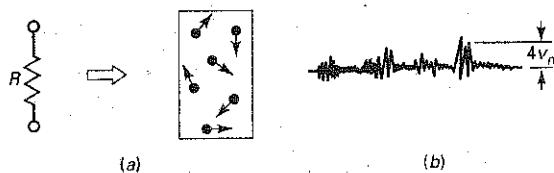
**Noise** is any kind of unwanted signal that is not derived from or harmonically related to the input signal. Electric motors, neon signs, power lines, car ignitions, lightning, and so on, produce electromagnetic fields that can induce noise voltages into electronic circuits. Power-supply ripple is also classified as noise since it is not related to the input signal. By using regulated power supplies and shielding, we usually can reduce the ripple and induced noise to an acceptable level.

**Thermal noise**, on the other hand, is caused by the random motion of free electrons inside a resistor (see Fig. 22-16a). The energy for this electron motion comes from the thermal energy of the surrounding air. The higher the ambient temperature, the more active the electrons.

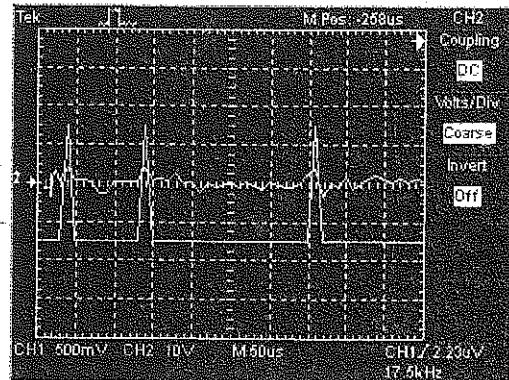
The motion of billions of free electrons inside a resistor is pure chaos. At some instants, more electrons move up than down, producing a small negative voltage across the resistor. At other instants, more electrons move down than up, producing a positive voltage. If this type of noise were amplified and viewed on an oscilloscope, it would resemble Fig. 22-16b. Like any voltage, noise has an rms or effective value. As an approximation, the highest noise peaks are about four times the rms value.

The randomness of the electron motion inside a resistor produces a distribution of noise at virtually all frequencies. The rms value of this noise increases with temperature, bandwidth, and resistance. For our purposes, we need to be aware of how noise may affect the output of a comparator.

Figure 22-16 Thermal noise: (a) Random electron motion in resistor; (b) noise on oscilloscope.



**Figure 22-17** Noise produces false triggering of comparator.



## Noise Triggering

As discussed in Sec. 22-1, the high open-loop gain of a comparator means that an input of only  $100 \mu\text{V}$  may be enough to switch the output from one state to another. If the input contains noise with a peak of  $100 \mu\text{V}$  or more, the comparator will detect the zero crossings produced by the noise.

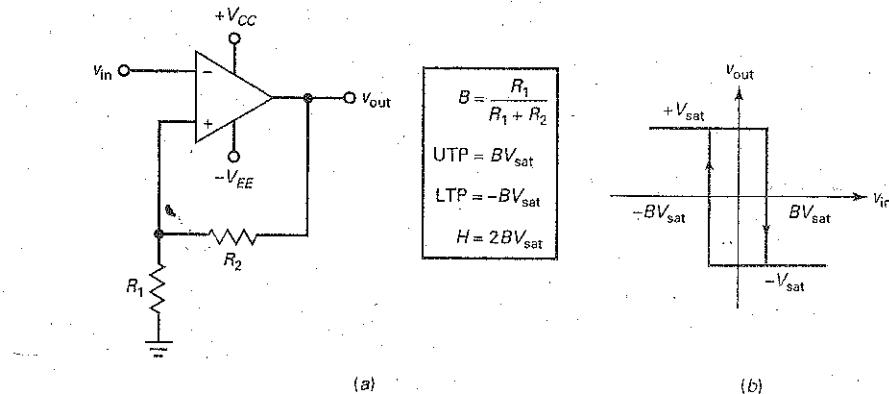
Figure 22-17 shows the output of a comparator with no input signal, except for noise. When the noise peaks are large enough, they produce unwanted changes in the comparator output. For instance, the noise peaks at A, B, and C are producing unwanted transitions from low to high. When an input signal is present, the noise is superimposed on the input signal and produces erratic triggering.

## Schmitt Trigger

The standard solution for a noisy input is to use a comparator like the one shown in Fig. 22-18a. The input voltage is applied to the inverting input. Because the feedback voltage is aiding the input voltage, the feedback is *positive*. A comparator using positive feedback like this is usually called a **Schmitt trigger**.

When the comparator is positively saturated, a positive voltage is fed back to the noninverting input. This positive feedback voltage holds the output in the high state. Similarly, when the output voltage is negatively saturated, a negative

**Figure 22-18** (a) Inverting Schmitt trigger; (b) input/output response has hysteresis.



voltage is fed back to the noninverting input, holding the output in the low state. In either case, the positive feedback reinforces the existing output state.

The feedback fraction is:

$$B = \frac{R_1}{R_1 + R_2} \quad (22-4)$$

When the output is positively saturated, the reference voltage applied to the non-inverting input is:

$$v_{\text{ref}} = +BV_{\text{sat}} \quad (22-5a)$$

When the output is negatively saturated, the reference voltage is:

$$v_{\text{ref}} = -BV_{\text{sat}} \quad (22-5b)$$

The output voltage will remain in a given state until the input voltage exceeds the reference voltage for that state. For instance, if the output is positively saturated, the reference voltage is  $+BV_{\text{sat}}$ . The input voltage must be increased to slightly more than  $+BV_{\text{sat}}$  to switch the output voltage from positive to negative, as shown in Fig. 22-18b. Once the output is in the negative state, it will remain there indefinitely until the input voltage becomes more negative than  $-BV_{\text{sat}}$ . Then, the output switches from negative to positive (Fig. 22-18b).

## Hysteresis

The unusual response of Fig. 22-18b has a useful property called hysteresis. To understand this concept, put your finger on the upper end of the graph where it says  $+V_{\text{sat}}$ . Assume that this is the current value of output voltage. Move your finger to the right along the horizontal line. Along this horizontal line, the input voltage is changing but the output voltage is still equal to  $+V_{\text{sat}}$ . When you reach the upper right corner,  $v_{\text{in}}$  equals  $+BV_{\text{sat}}$ . When  $v_{\text{in}}$  increases to slightly more than  $+BV_{\text{sat}}$ , the output voltage goes into the transition region between the high and the low states.

If you move your finger down along the vertical line, you will simulate the transition of the output voltage from high to low. When your finger is on the lower horizontal line, the output voltage is negatively saturated and equal to  $-V_{\text{sat}}$ .

To switch back to the high output state, move your finger until it reaches the lower left corner. At this point,  $v_{\text{in}}$  equals  $-BV_{\text{sat}}$ . When  $v_{\text{in}}$  becomes slightly more negative than  $-BV_{\text{sat}}$ , the output voltage goes into the transition from low to high. If you move your finger up along the vertical line, you will simulate the switching of the output voltage from low to high.

In Fig. 22-18b, the trip points are defined as the two input voltages where the output voltage changes states. The *upper trip point (UTP)* has the value:

$$\text{UTP} = BV_{\text{sat}} \quad (22-6)$$

and the *lower trip point (LTP)* has the value:

$$\text{LTP} = -BV_{\text{sat}} \quad (22-7)$$

The difference between these trip points is defined as the hysteresis (also called the *deadband*):

$$H = \text{UTP} - \text{LTP} \quad (22-8)$$

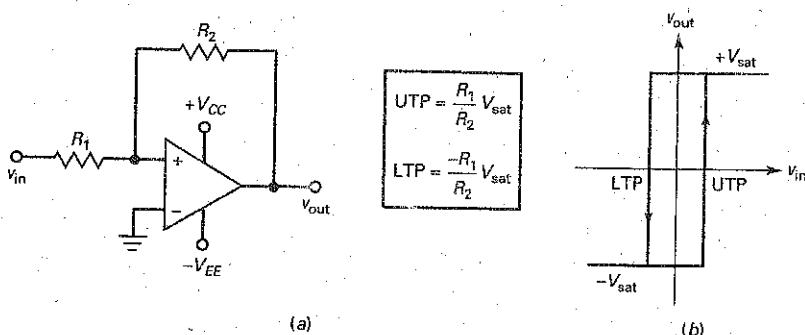
With Eqs. (22-6) and (22-7), this becomes:

$$H = BV_{\text{sat}} - (-BV_{\text{sat}})$$

which equals:

$$H = 2BV_{\text{sat}} \quad (22-9)$$

Figure 22-19 (a) Noninverting Schmitt trigger; (b) input/output response.



Positive feedback causes the hysteresis of Fig. 22-19b. If there were no positive feedback,  $B$  would equal zero and the hysteresis would disappear, because both trip points would equal zero.

Hysteresis is desirable in a Schmitt trigger because it prevents noise from causing false triggering. If the peak-to-peak noise voltage is less than the hysteresis, the noise cannot produce false triggering. For instance, if  $UTP = +1\text{ V}$  and  $LTP = -1\text{ V}$ , then  $H = 2\text{ V}$ . In this case, the Schmitt trigger is immune to false triggering as long as the peak-to-peak noise voltage is less than 2 V.

### Noninverting Circuit

Figure 22-19a shows a *noninverting Schmitt trigger*. The input/output response has a hysteresis loop, as shown in Fig. 22-19b. Here is how the circuit works: If the output is positively saturated in Fig. 22-19a, the feedback voltage to the noninverting input is positive, which reinforces the positive saturation. Similarly, if the output is negatively saturated, the feedback voltage to the noninverting input is negative, which reinforces the negative saturation.

Assume that the output is negatively saturated. The feedback voltage will hold the output in negative saturation until the input voltage becomes slightly more positive than UTP. When this happens, the output switches from negative to positive saturation. Once in positive saturation, the output stays there until the input voltage becomes slightly less than LTP. Then, the output can change back to the negative state.

The equations for the trip points of a noninverting Schmitt trigger are given by:

$$UTP = \frac{R_1}{R_2} V_{sat} \quad (22-10)$$

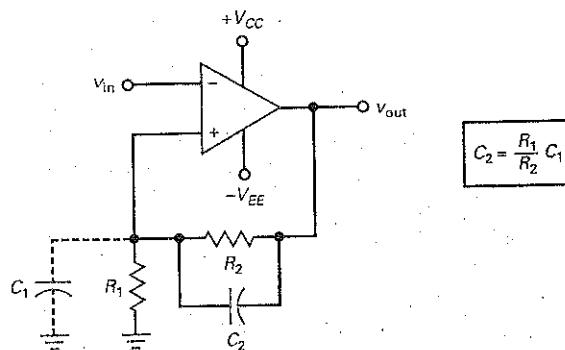
$$LTP = \frac{-R_1}{R_2} V_{sat} \quad (22-11)$$

The ratio of  $R_1$  to  $R_2$  determines how much hysteresis the Schmitt trigger has. A designer can create enough hysteresis to prevent unwanted noise triggers.

### Speed-Up Capacitor

Besides suppressing the effects of noise, positive feedback speeds up the switching of output states. When the output voltage begins to change, this change is fed back to the noninverting input and amplified, forcing the output to change faster.

Figure 22-20 Speed-up capacitor compensates for stray capacitance.



Sometimes a capacitor  $C_2$  is connected in parallel with  $R_2$ , as shown in Fig. 22-20a. Known as a **speed-up capacitor**, it helps to cancel the bypass circuit formed by the stray capacitance across  $R_1$ . This stray capacitance  $C_1$  has to be charged before the noninverting input voltage can change. The speed-up capacitor supplies this charge.

To neutralize the stray capacitance, the minimum speed-up capacitance must be at least:

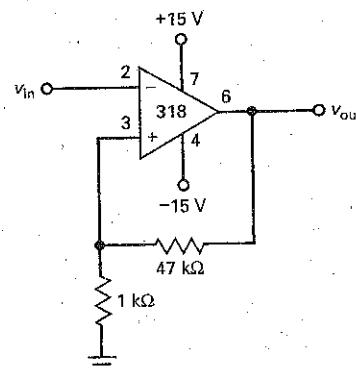
$$C_2 = \frac{R_1}{R_2} C_1 \quad (22-12)$$

As long as  $C_2$  is equal to or greater than the value given by Eq. (22-12), the output will switch states at maximum speed. Since a designer often has to estimate the stray capacitance  $C_1$ , he or she usually makes  $C_2$  at least two times larger than the value given by Eq. (22-12). In typical circuits  $C_2$  is from 10 to 100 pF.

## Example 22-6

If  $V_{sat} = 13.5$  V, what are the trip points and hysteresis in Fig. 22-21?

Figure 22-21 Example.



**SOLUTION** With Eq. (22-4), the feedback fraction is:

$$B = \frac{1\text{ k}\Omega}{48\text{ k}\Omega} = 0.0208$$

With Eqs. (22-6) and (22-7), the trip points are:

$$\text{UTP} = 0.0208(13.5\text{ V}) = 0.281\text{ V}$$

$$\text{LTP} = -0.0208(13.5\text{ V}) = -0.281\text{ V}$$

With Eq. (22-9), the hysteresis is:

$$H = 2(0.0208\text{ V})(13.5\text{ V}) = 0.562\text{ V}$$

This means that the Schmitt trigger of Fig. 22-21 can withstand a peak-to-peak noise voltage up to 0.562 V without false triggering.

**PRACTICE PROBLEM 22-6** Repeat Example 22-6 with the 47 kΩ resistor changed to 22 kΩ.

## 22-4 Window Comparator

An ordinary comparator indicates when the input voltage exceeds a certain limit or threshold. A **window comparator** (also called a *double-ended limit detector*) detects when the input voltage is between two limits called the *window*. To create a window comparator, we will use two comparators with different thresholds.

### Low Output between Limits

Figure 22-22a shows a window comparator that can produce a low output voltage when the input voltage is between a lower and an upper limit. The circuit has an

Figure 22-22 (a) Inverting window comparator; (b) output is low when input is in window.

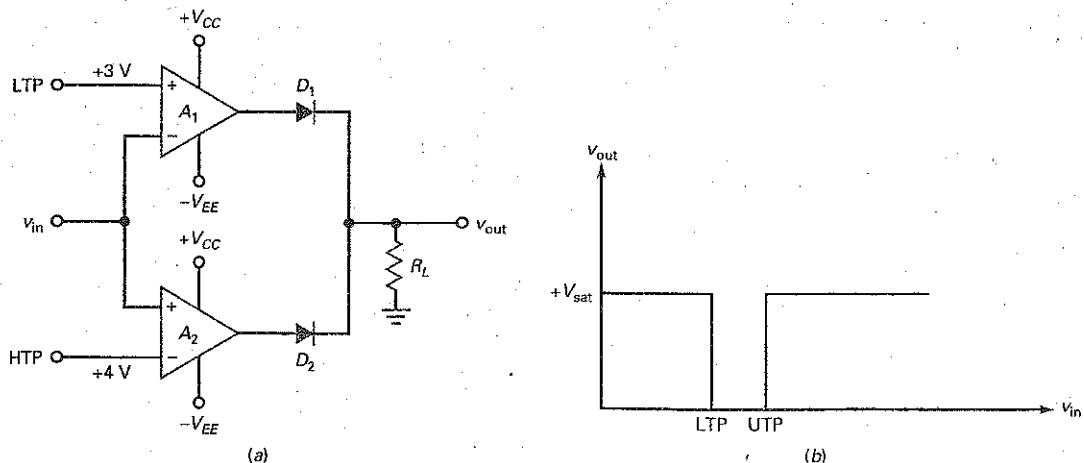
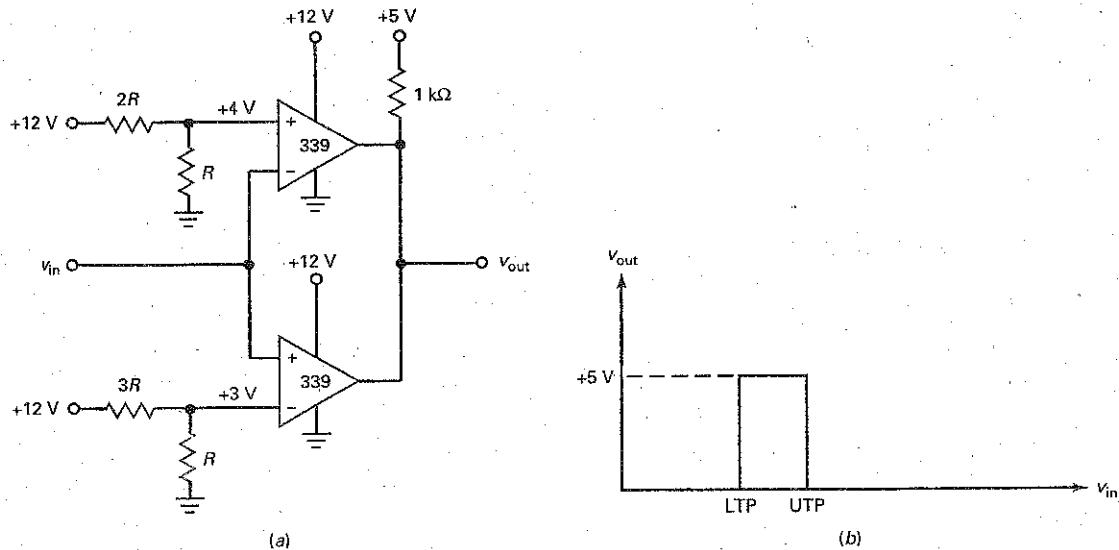


Figure 22-23 (a) Noninverting window comparator; (b) output is high when input is in window.



LTP and a UTP. The reference voltages can be derived from voltage dividers, zener diodes, or other circuits. Figure 22-22b shows the input/output response of the window comparator. When  $v_{in}$  is less than LTP or greater than UTP, the output is high. When  $v_{in}$  is between LTP and UTP, the output is low.

Here is the theory of operation: For this discussion, assume the following positive trip points: LTP = 3 V and UTP = 4 V. When  $v_{in} < 3$  V, comparator  $A_1$  has a positive output and  $A_2$  has a negative output. Diode  $D_1$  is on and  $D_2$  is off. Therefore, the output voltage is high. Similarly, when  $v_{in} > 4$  V, comparator  $A_1$  has a negative output and  $A_2$  has a positive output. Diode  $D_1$  is off,  $D_2$  is on, and the output voltage is high. When  $3 < v_{in} < 4$  V,  $A_1$  has a negative output,  $A_2$  has a negative output,  $D_1$  is off,  $D_2$  is off, and the output voltage is low.

### High Output between Limits

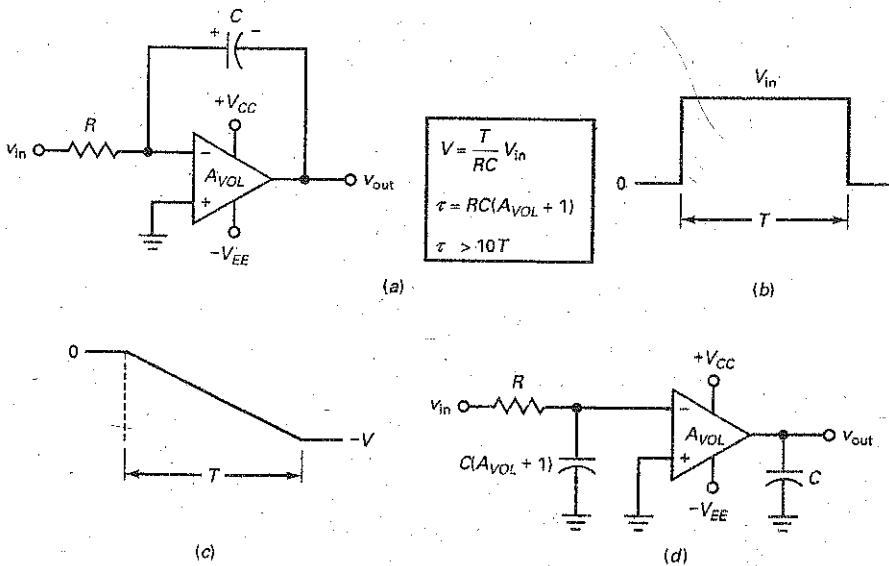
Figure 22-23a shows another window comparator. The circuit uses an LM339, which is a quad comparator that needs external pullup resistors. When used with a pullup supply of +5 V, the output can drive TTL circuits. Figure 22-23b shows the input/output response. As we can see, the output voltage is high when the input voltage is between the two limits.

For this discussion, we are assuming the same reference voltages as in the preceding example. When the input voltage is less than 3 V, the lower comparator pulls the output down to zero. When the input voltage is greater than 4 V, the upper comparator pulls the output down to zero. When  $v_{in}$  is between 3 and 4 V, the output transistor of each comparator is cut off, so the output is pulled up to +5 V.

## 22-5 The Integrator

An integrator is a circuit that performs a mathematical operation called *integration*. The most popular application of an integrator is in producing a *ramp* of output voltage, which is a linearly increasing or decreasing voltage. The integrator is sometimes called the *Miller integrator*, after the inventor.

Figure 22-24 (a) Integrator; (b) typical input pulse; (c) output ramp; (d) input Miller capacitance is very large.



### Basic Circuit

Figure 22-24a is an op-amp integrator. As you can see, the feedback component is a capacitor instead of a resistor. The usual input to an integrator is a rectangular pulse like the one shown in Fig. 22-24b. The width of this pulse is equal to  $T$ . When the pulse is low,  $v_{in} = 0$ . When the pulse is high,  $v_{in} = V_{in}$ . Visualize this pulse applied to the left end of  $R$ . Because of the virtual ground on the inverting input, a high input voltage produces an input current of:

$$I_{in} = \frac{V_{in}}{R}$$

All this input current goes into the capacitor. As a result, the capacitor charges and its voltage increases with the polarity shown in Fig. 22-24a. The virtual ground implies that the output voltage equals the voltage across the capacitor. For a positive input voltage, the output voltage will increase negatively, as shown in Fig. 22-24c.

Since a constant current is flowing into the capacitor, the charge  $Q$  increases linearly with time. This means that the capacitor voltage increases linearly, which is equivalent to a negative ramp of output voltage, as shown in Fig. 22-24c. At the end of the pulse period in Fig. 22-24b, the input voltage returns to zero and the capacitor charging stops. Because the capacitor retains its charge, the output voltage remains constant at a negative voltage of  $-V$ . The magnitude of this voltage is given by:

$$V = \frac{T}{RC} V_{in} \quad (22-13)$$

A final point: Because of the Miller effect, we can split the feedback capacitor into two equivalent capacitances, as shown in Fig. 22-24d. The closed-loop time constant  $\tau$  for the input bypass circuit is:

$$\tau = RC(A_{VOL} + 1) \quad (22-14)$$

For the integrator to work properly, the closed-loop time constant should be much greater than the width of the input pulse (at least 10 times greater). As a formula:

$$\tau > 10T \quad (22-15)$$

In the typical op-amp integrator, the closed-loop time constant is extremely long, so this condition is easily satisfied.

### Eliminating Output Offset

The circuit of Fig. 22-24a needs a slight modification to make it practical. Because a capacitor is open to dc signals, there is no negative feedback at zero frequency. Without negative feedback, the circuit treats any input offset voltage as a valid input voltage. The result is that the capacitor charges and the output goes into positive or negative saturation, where it stays indefinitely.

One way to reduce the effect of input offset voltage is to decrease the voltage gain at zero frequency by inserting a resistor in parallel with the capacitor, as shown in Fig. 22-25a. This resistor should be at least 10 times larger than the input resistor. If the added resistance equals  $10R$ , the closed-loop voltage gain is 10 and the output offset voltage is reduced to an acceptable level. When a valid input voltage is present, the additional resistor has almost no effect on the charging of a capacitor, so the output voltage is still almost a perfect ramp.

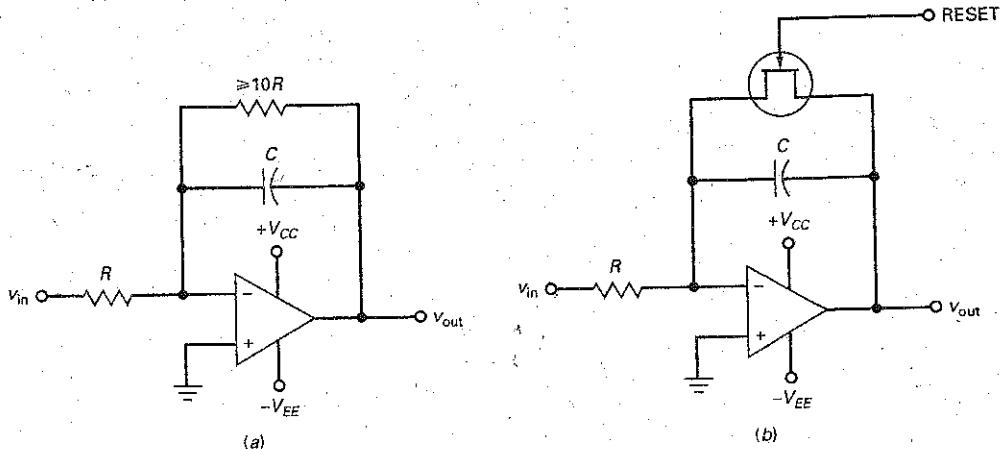
Another way to suppress the effect of input offset voltage is to use a JFET switch, as shown in Fig. 22-25b. The reset voltage on the gate of the JFET is either 0 V or  $-V_{CC}$ , which is enough to cut off the JFET. Therefore, we can set the JFET to a low resistance when the integrator is idle and to a high resistance when the integrator is active.

The JFET discharges the capacitor in preparation for the next input pulse. Just before the beginning of the next input pulse, the reset voltage is made equal to 0 V. This discharges the capacitor. At the instant the next pulse begins, the reset voltage becomes  $-V_{CC}$ , which cuts off the JFET. The integrator then produces an output voltage ramp.

### GOOD TO KNOW

The feedback resistor in Fig. 22-25 can also be split into two equivalent resistances. On the input side,  $Z_{in} = R_f/(1 + A_{vol})$ .

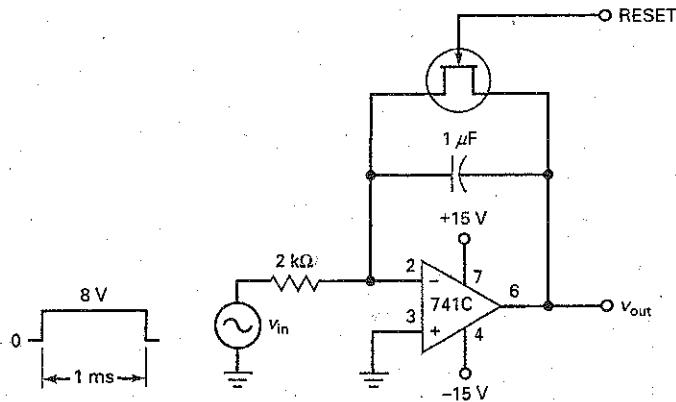
Figure 22-25 (a) Resistor across capacitor reduces output offset voltage; (b) JFET used to reset integrator.



## Example 22-7

In Fig. 22-26, what is the output voltage at the end of the input pulse? If the 741C has an open-loop voltage gain of 100,000, what is the closed-loop time constant of the integrator?

Figure 22-26 Example.



**SOLUTION** With Eq. (22-13), the magnitude of the negative output voltage at the end of the pulse is:

$$V = \frac{1 \text{ ms}}{(2 \text{ k}\Omega)(1 \mu\text{F})} (8 \text{ V}) = 4 \text{ V}$$

With Eq. (22-14), the closed-loop time constant is:

$$\tau = RC(A_{VOL} + 1) = (2 \text{ k}\Omega)(1 \mu\text{F})(100,000) = 200 \text{ s}$$

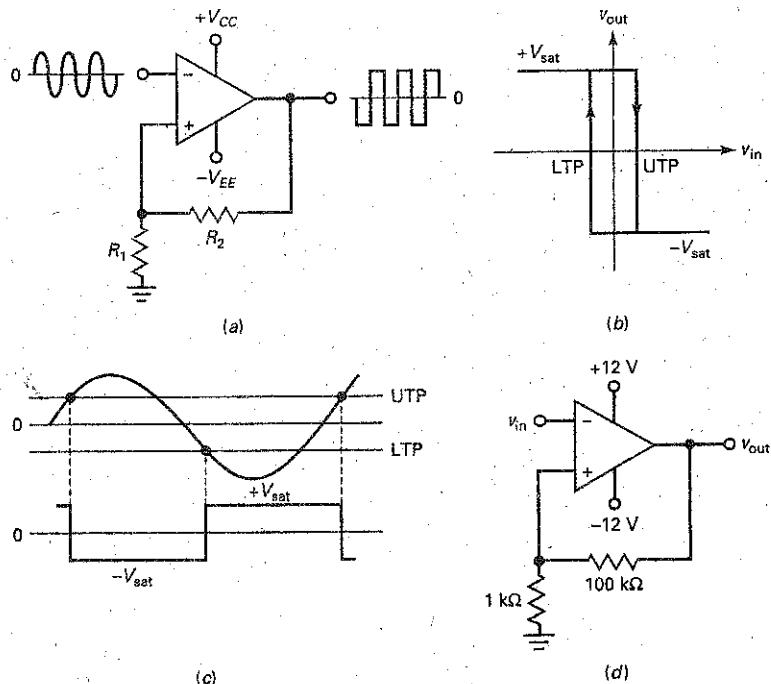
Since the pulse width of 1 ms is much smaller than the closed-loop time constant, only the earliest part of an exponential function is involved in the capacitor charging. Because the initial part of an exponential function is almost linear, the output voltage is almost a perfect ramp. Using an integrator to generate linear ramps is how the linear sweep voltages of an oscilloscope are produced.

**PRACTICE PROBLEM 22-7** Using Fig. 22-26, change the  $2 \text{ k}\Omega$  resistor to  $10 \text{ k}\Omega$  and repeat Example 22-7.

## 22-6 Waveform Conversion

With op amps we can convert sine waves to rectangular waves, rectangular waves to triangular waves, and so on. This section is about some basic circuits that convert an input waveform to an output waveform of a different shape.

Figure 22-27 Schmitt trigger always produces rectangular output.



### Sine to Rectangular

Figure 22-27a shows a Schmitt trigger, and Fig. 22-27b is the graph of output voltage versus input voltage. When the input signal is *periodic* (repeating cycles), the Schmitt trigger produces a rectangular output, as shown. This assumes that the input signal is large enough to pass through both trip points of Fig. 22-27c. When the input voltage exceeds UTP on the upward swing of the positive half cycle, the output voltage switches to  $-V_{sat}$ . One half cycle later, the input voltage becomes more negative than LTP, and the output switches back to  $+V_{sat}$ .

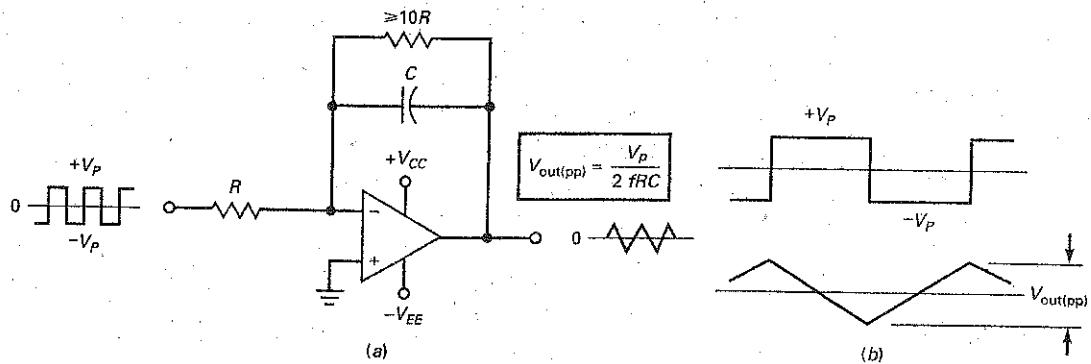
A Schmitt trigger always produces a rectangular output, regardless of the shape of the input signal. In other words, the input voltage does not have to be sinusoidal. As long as the waveform is periodic and has an amplitude large enough to pass through the trip points, we get a rectangular output from the Schmitt trigger. This rectangular wave has the same frequency as the input signal.

As an example, Fig. 22-27d shows a Schmitt trigger with trip points of approximately UTP =  $+0.1$  V and LTP =  $-0.1$  V. If the input voltage is repetitive and has a peak-to-peak value greater than 0.2 V, the output voltage is a rectangular wave with a peak-to-peak value of approximately  $2V_{sat}$ .

### Rectangular to Triangular

In Fig. 22-28a, a rectangular wave is the input to an integrator. Since the input voltage has a dc or average value of zero, the dc or average value of the output is also zero. As shown in Fig. 22-28b, the ramp is decreasing during the positive half cycle of input voltage and increasing during the negative half cycle. Therefore,

Figure 22-28 (a) Square wave into integrator produces triangular output; (b) input and output waveforms.



the output is a triangular wave with the same frequency as the input. It can be shown that the triangular output waveform has a peak-to-peak value of:

$$V_{\text{out(pp)}} = \frac{T}{2RC} V_p \quad (22-16)$$

where  $T$  is the period of the signal. An equivalent expression in terms of frequency is:

$$V_{\text{out(pp)}} = \frac{V_p}{2fRC} \quad (22-17)$$

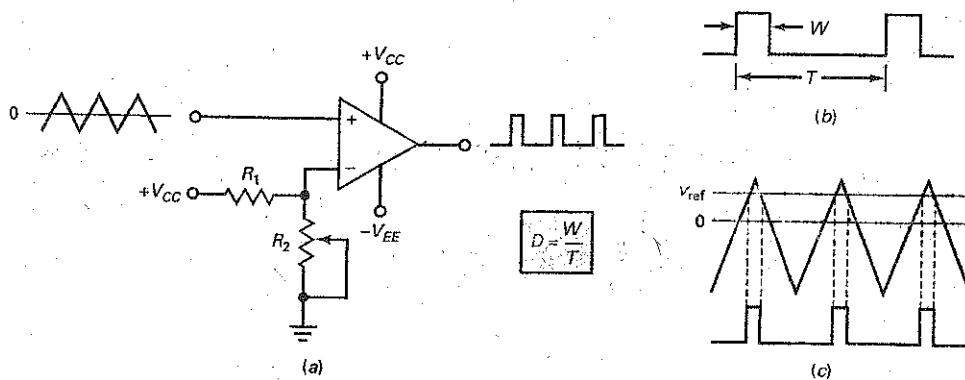
where  $V_p$  is the peak input voltage and  $f$  is the input frequency.

### Triangle to Pulse

Figure 22-29a shows a circuit that converts a triangular input to a rectangular output. By varying  $R_2$ , we can change the width of the output pulses, which is equivalent to varying the duty cycle. In Fig. 22-29b,  $W$  represents the width of the pulse and  $T$  is the period. As previously discussed, the duty cycle  $D$  is the width of the pulse divided by the period.

In some applications, we want to vary the duty cycle. The adjustable limit detector of Fig. 22-29a is ideal for this purpose. With this circuit, we can move the trip point from zero to a positive level. When the triangular input voltage exceeds

Figure 22-29 Triangular input to limit detector produces rectangular output.

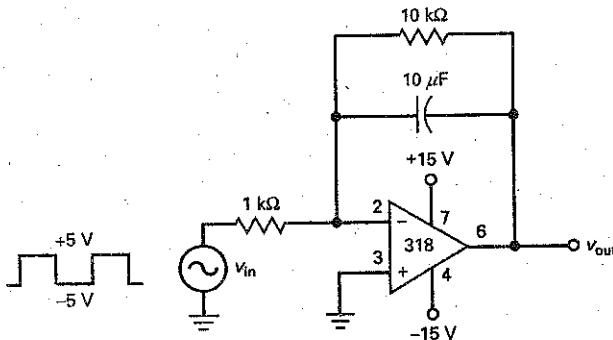


the trip point, the output is high, as shown in Fig. 22-29c. Since  $v_{ref}$  is adjustable, we can vary the width of the output pulse, which is equivalent to changing the duty cycle. With a circuit like this, we can vary the duty cycle from approximately 0 to 50 percent.

## Example 22-8

What is the output voltage in Fig. 22-30 if the input frequency is 1 kHz?

Figure 22-30 Example.



**SOLUTION** With Eq. (22-17), the output is a triangular wave with a peak-to-peak voltage of:

$$V_{out(pp)} = \frac{5 \text{ V}}{2(1 \text{ kHz})(1 \text{ k}\Omega)(10 \mu\text{F})} = 0.25 \text{ V pp}$$

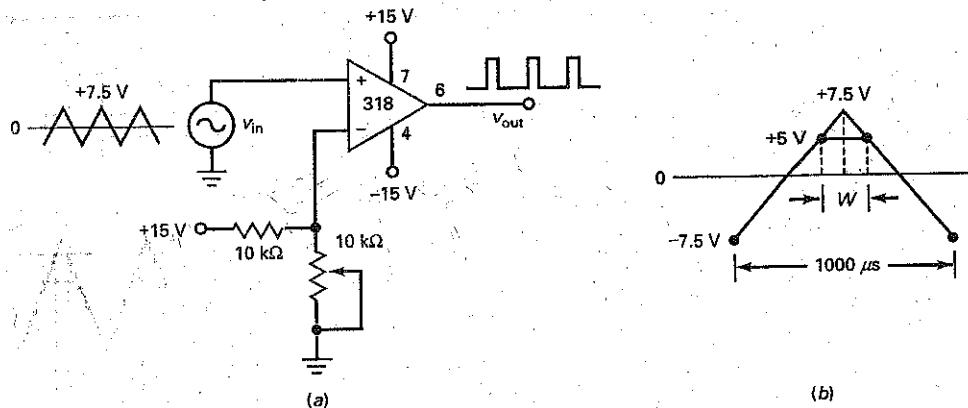
**PRACTICE PROBLEM 22-8** In Fig. 22-30, what value of capacitor is needed to produce an output voltage of 1 V pp?

## Example 22-9

MultiSim

A triangular input drives the circuit of Fig. 22-31a. The variable resistance has a maximum value of 10 kΩ. If the triangular input has a frequency of 1 kHz, what is the duty cycle when the wiper is at the middle of its range?

Figure 22-31 Example.



**SOLUTION** When the wiper is at the middle of its range, it has a resistance of  $5\text{ k}\Omega$ . This means that the reference voltage is:

$$V_{\text{ref}} = \frac{5\text{ k}\Omega}{15\text{ k}\Omega} 15\text{ V} = 5\text{ V}$$

The period of the signal is:

$$T = \frac{1}{1\text{ kHz}} = 1000\text{ }\mu\text{s}$$

Figure 22-31b shows this value. It takes  $500\text{ }\mu\text{s}$  for the input voltage to increase from  $-7.5$  to  $+7.5\text{ V}$  because this is half of the cycle. The trip point of the comparator is  $+5\text{ V}$ . This means that the output pulse has a width of  $W$ , as shown in Fig. 22-31b.

Because of the geometry of Fig. 22-31b, we can set up a proportion between voltage and time as follows:

$$\frac{W/2}{500\text{ }\mu\text{s}} = \frac{7.5\text{ V} - 5\text{ V}}{15\text{ V}}$$

Solving for  $W$  gives:

$$W = 167\text{ }\mu\text{s}$$

The duty cycle is:

$$D = \frac{167\text{ }\mu\text{s}}{1000\text{ }\mu\text{s}} = 0.167$$

In Fig. 22-31a, moving the wiper down will increase the reference voltage and decrease the output duty cycle. Moving the wiper up will decrease the reference voltage and increase the output duty cycle. For all values given in Fig. 22-31a, the duty cycle can vary from 0 to 50 percent.

**PRACTICE PROBLEM 22-9** Repeat Example 22-9 using an input frequency of 2 kHz.

## 22-7 Waveform Generation

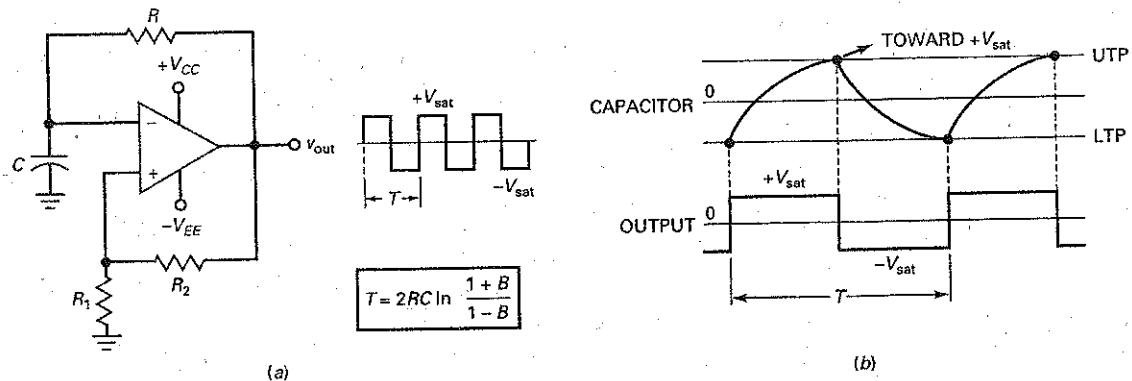
With positive feedback, we can build oscillators, circuits that generate or create an output signal with no external input signal. This section discusses some op-amp circuits that can generate nonsinusoidal signals.

### Relaxation Oscillator

In Fig. 22-32a, there is no input signal. Nevertheless, the circuit produces a rectangular output signal. This output is a square wave that swings between  $-V_{\text{sat}}$  and  $+V_{\text{sat}}$ . How is this possible? Assume that the output of Fig. 22-32a is in positive saturation. Because of feedback resistor  $R$ , the capacitor will charge exponentially toward  $+V_{\text{sat}}$ , as shown in Fig. 22-32b. But the capacitor voltage never reaches  $+V_{\text{sat}}$  because the voltage crosses the UTP. When this happens, the output square wave switches to  $-V_{\text{sat}}$ .

With the output now in negative saturation, the capacitor discharges, as shown in Fig. 22-32b. When the capacitor voltage crosses through zero, the capacitor starts charging negatively toward  $-V_{\text{sat}}$ . When the capacitor voltage crosses the LTP, the output square wave switches back to  $+V_{\text{sat}}$ . The cycle then repeats.

Figure 22-32 (a) Relaxation oscillator; (b) capacitor charging and output waveform.



Because of the continuous charging and discharging of the capacitor, the output is a rectangular wave with a duty cycle of 50 percent. By analyzing the exponential charge and discharge of the capacitor, we can derive this formula for the period of the rectangular output:

$$T = 2RC \ln \frac{1+B}{1-B} \quad (22-18)$$

where  $B$  is the feedback fraction given by:

$$B = \frac{R_1}{R_1 + R_2}$$

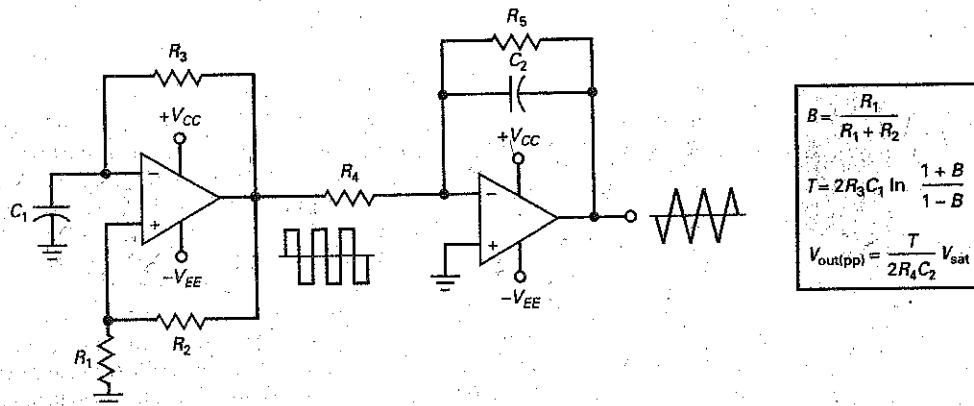
Equation (22-18) uses the *natural logarithm*, which is a logarithm to base  $e$ . A scientific calculator or table of natural logarithms must be used with this equation.

Figure 22-32a is called a **relaxation oscillator**, defined as a circuit that generates an output signal whose frequency depends on the charging of a capacitor. If we increase the  $RC$  time constant, it takes longer for the capacitor voltage to reach the trip points. Therefore, the frequency is lower. By making  $R$  adjustable, we can get a 50 : 1 tuning range.

### Generating Triangular Waves

By cascading a relaxation oscillator and an integrator, we get a circuit that produces the triangular output shown in Fig. 22-33. The rectangular wave out of the

Figure 22-33 Relaxation oscillator drives integrator to produce triangular output.



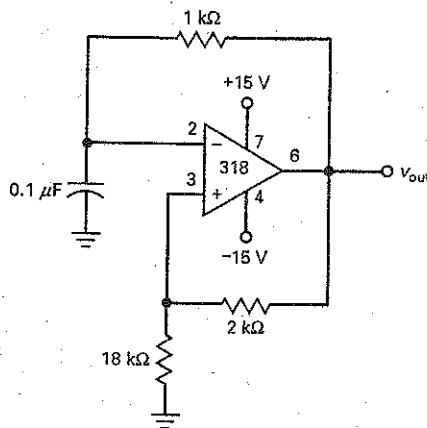
relaxation oscillator drives the integrator, which produces a triangular output waveform. The rectangular wave swings between  $+V_{\text{sat}}$  and  $-V_{\text{sat}}$ . You can calculate its period with Eq. (22-18). The triangular wave has the same period and frequency. You can calculate its peak-to-peak value with Eq. (22-16).

## Example 22-10

Multisim

What is the frequency of the output signal in Fig. 22-34?

Figure 22-34 Example.



**SOLUTION** The feedback fraction is:

$$B = \frac{18 \text{ k}\Omega}{20 \text{ k}\Omega} = 0.9$$

With Eq. (22-18):

$$T = 2RC \ln \frac{1+B}{1-B} = 2(1 \text{ k}\Omega)(0.1 \mu\text{F}) \ln \frac{1+0.9}{1-0.9} = 589 \mu\text{s}$$

The frequency is:

$$f = \frac{1}{589 \mu\text{s}} = 1.7 \text{ kHz}$$

The square-wave output voltage has a frequency of 1.7 kHz and a peak-to-peak value of  $2V_{\text{sat}}$ , approximately 27 V for the circuit of Fig. 22-34.

**PRACTICE PROBLEM 22-10** In Fig. 22-34, change the 18 kΩ resistor to 10 kΩ and calculate the new output frequency.

## Example 22-11

Multisim

The relaxation oscillator of Example 22-10 is used in Fig. 22-33 to drive the integrator. Assume that the peak voltage out of the relaxation oscillator is 13.5 V. If the integrator has  $R_4 = 10 \text{ k}\Omega$  and  $C_2 = 10 \mu\text{F}$ , what is the peak-to-peak value of the triangular output wave?

**SOLUTION** With the equations shown in Fig. 22-33, we can analyze the circuit. In Example 22-10, we calculated a feedback fraction of 0.9 and a period of  $589 \mu\text{s}$ . Now, we can calculate the peak-to-peak value of the triangular output:

$$V_{\text{out(pp)}} = \frac{589 \mu\text{s}}{2(10 \text{k}\Omega)(10 \mu\text{F})} (13.5 \text{ V}) = 39.8 \text{ mV pp}$$

The circuit generates a square wave with a peak-to-peak value of approximately 27 V and a triangular wave with a peak-to-peak value of 39.8 mV.

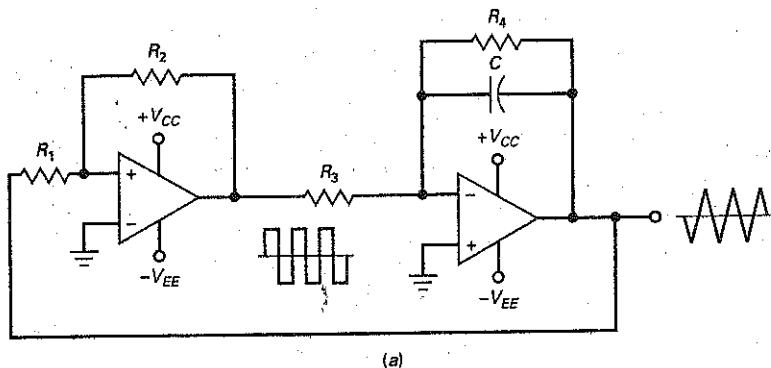
**PRACTICE PROBLEM 22-11** Repeat Example 22-11 with the  $18 \text{k}\Omega$  resistor, in Fig. 22-34, changed to  $10 \text{k}\Omega$ .

## 22-8 Another Triangular Generator

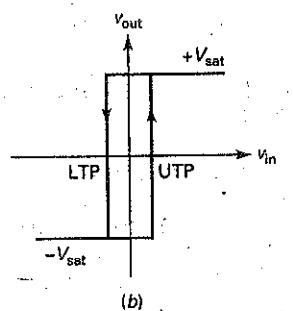
In Fig. 22-35a, the output of a noninverting Schmitt trigger is a rectangular wave that drives an integrator. The output of the integrator is a triangular wave. This triangular wave is fed back and drives the Schmitt trigger. So we have a very interesting circuit. The first stage drives the second, and the second drives the first.

Figure 22-35b is the transfer characteristic of the Schmitt trigger. When the output is low, the input must increase to the UTP to switch the output to high.

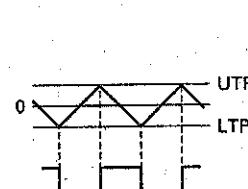
Figure 22-35 Schmitt trigger and integrator generate square wave and triangular wave.



(a)



(b)



(c)

$\text{UTP} = \frac{R_1}{R_2} V_{\text{sat}}$
$H = 2\text{UTP}$
$V_{\text{out(pp)}} = H$
$f = \frac{R_2}{4R_1 R_3 C}$

Likewise, when the output is high, the input must decrease to the LTP to switch the output to low.

When the Schmitt trigger output is low in Fig. 22-35c, the integrator produces a positive ramp, which increases until it reaches the UTP. At this point, the output of the Schmitt trigger switches to the high state and the triangular wave reverses direction. The negative ramp then decreases until it reaches the LTP, where another Schmitt output change takes place.

In Fig. 22-35c, the peak-to-peak value of the triangular wave equals the difference between the UTP and the LTP. We can derive this equation for the frequency:

$$f = \frac{R_2}{4R_1R_3C} \quad (22-19)$$

Figure 22-35 shows this equation, along with other analysis equations.

## Example 22-12

The triangular-wave generator of Fig. 22-35a has these circuit values:  $R_1 = 1\text{ k}\Omega$ ,  $R_2 = 100\text{ k}\Omega$ ,  $R_3 = 10\text{ k}\Omega$ ,  $R_4 = 100\text{ k}\Omega$ , and  $C = 10\text{ }\mu\text{F}$ . What is the peak-to-peak output if  $V_{\text{sat}} = 13\text{ V}$ ? What is the frequency of the triangular wave?

**SOLUTION** With the equations shown in Fig. 22-35, the UTP has a value of:

$$\text{UTP} = \frac{1\text{ k}\Omega}{100\text{ k}\Omega}(13\text{ V}) = 0.13\text{ V}$$

The peak-to-peak value of the triangular output equals the hysteresis:

$$V_{\text{out(pp)}} = H = 2\text{UTP} = 2(0.13\text{ V}) = 0.26\text{ V}$$

The frequency is:

$$f = \frac{100\text{ k}\Omega}{4(1\text{ k}\Omega)(10\text{ k}\Omega)(10\text{ }\mu\text{F})} = 250\text{ Hz}$$

**PRACTICE PROBLEM 22-12** Using Fig. 22-35, change  $R_1$  to  $2\text{ k}\Omega$  and  $C$  to  $1\text{ }\mu\text{F}$ . Calculate  $V_{\text{out(pp)}}$  and the output frequency.

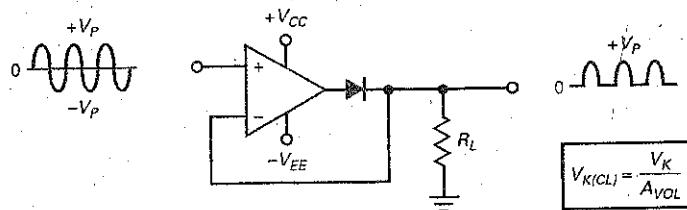
## 22-9 Active Diode Circuits

Op amps can enhance the performance of diode circuits. For one thing, an op amp with negative feedback reduces the effect of the knee voltage, allowing us to rectify, peak-detect, clip, and clamp low-level signals (those with amplitudes less than the knee voltage). And because of their buffering action, op amps can eliminate the effects of the source and load on diode circuits.

### Half-Wave Rectifier

Figure 22-36 is an active half-wave rectifier. When the input signal goes positive, the output goes positive and turns on the diode. The circuit then acts like a voltage follower, and the positive half cycle appears across the load resistor.

Figure 22-36 Active half-wave rectifier.



When the input goes negative, the op-amp output goes negative and turns off the diode. Since the diode is open, no voltage appears across the load resistor. The final output is almost a perfect half-wave signal.

There are two distinct *modes* or regions of operation. First, when the input voltage is positive, the diode is conducting and the operation is linear. In this case, the output voltage is fed back to the input, and we have negative feedback. Second, when the input voltage is negative, the diode is nonconducting and the feedback path is open. In this case, the op-amp output is isolated from the load resistor.

The high open-loop voltage gain of the op amp almost eliminates the effect of the knee voltage. For instance, if the knee voltage is 0.7 V and  $A_{VOL}$  is 100,000, the input voltage that just turns on the diode is 7  $\mu$ V.

The closed-loop knee voltage is given by:

$$V_{K(CL)} = \frac{V_K}{A_{VOL}}$$

where  $V_K = 0.7$  V for a silicon diode. Because the closed-loop knee voltage is so small, the active half-wave rectifier may be used with low-level signals in the microvolt region.

### Active Peak Detector

To peak-detect small signals, we can use an **active peak detector** like the one shown in Fig. 22-37a. Again, the closed-loop knee voltage is in the microvolt region, which means that we can peak-detect low-level signals. When the diode is on, the negative feedback produces a Thevenin output impedance that approaches zero. This means that the charging time constant is very low, so the capacitor can quickly charge to the positive peak value. When the diode is off, the capacitor has to discharge through  $R_L$ . Because the discharging time constant  $R_L C$  can be made much longer than the period of the input signal, we can get almost perfect peak detection of low-level signals.

There are two distinct regions of operation. First, when the input voltage is positive, the diode is conducting and the operation is linear. In this case, the capacitor charges to the peak of the input voltage. Second, when the input voltage is negative, the diode is nonconducting and the feedback path is open. In this case, the capacitor discharges through the load resistor. As long as the discharging time constant is much greater than the period of the input signal, the output voltage will be approximately equal to the peak value of the input voltage.

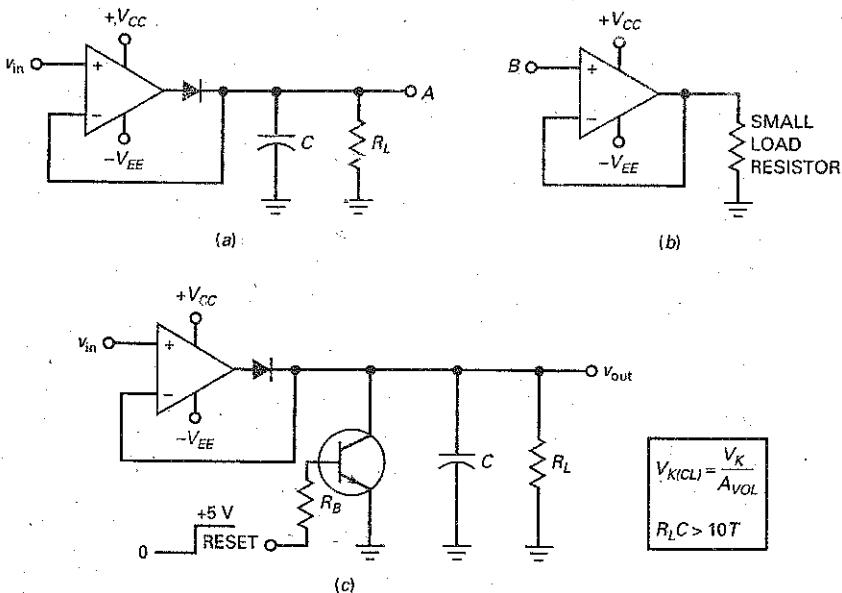
If the peak-detected signal has to drive a small load, we can avoid loading effects by using an op-amp buffer. For instance, if we connect point A of Fig. 22-37a to point B of Fig. 22-37b, the voltage follower isolates the small load resistor from the peak detector. This prevents the small load resistor from discharging the capacitor too quickly.

At a minimum, the  $R_L C$  time constant should be at least 10 times longer than the period  $T$  of the lowest input frequency. In symbols:

$$R_L C > 10T$$

(22-20)

Figure 22-37 (a) Active peak detector; (b) buffer amplifier; (c) peak detector with reset.



If this condition is satisfied, the output voltage will be within 5 percent of the peak input. For instance, if the lowest frequency is 1 kHz, the period is 1 ms. In this case, the  $R_L C$  time constant should be at least 10 ms for an error of less than 5 percent.

Often, a *reset* is included with an active peak detector, as shown in Fig. 22-37c. When the reset input is low, the transistor switch is off. This allows the circuit to work as previously described. When the reset input is high, the transistor switch is closed. This rapidly discharges the capacitor. The reason you may need a reset is because the long discharge time constant means that the capacitor will hold its charge for a long time, even though the input signal is removed. By using a high reset input, we can quickly discharge the capacitor in preparation for another input signal with a different peak value.

### Active Positive Clipper

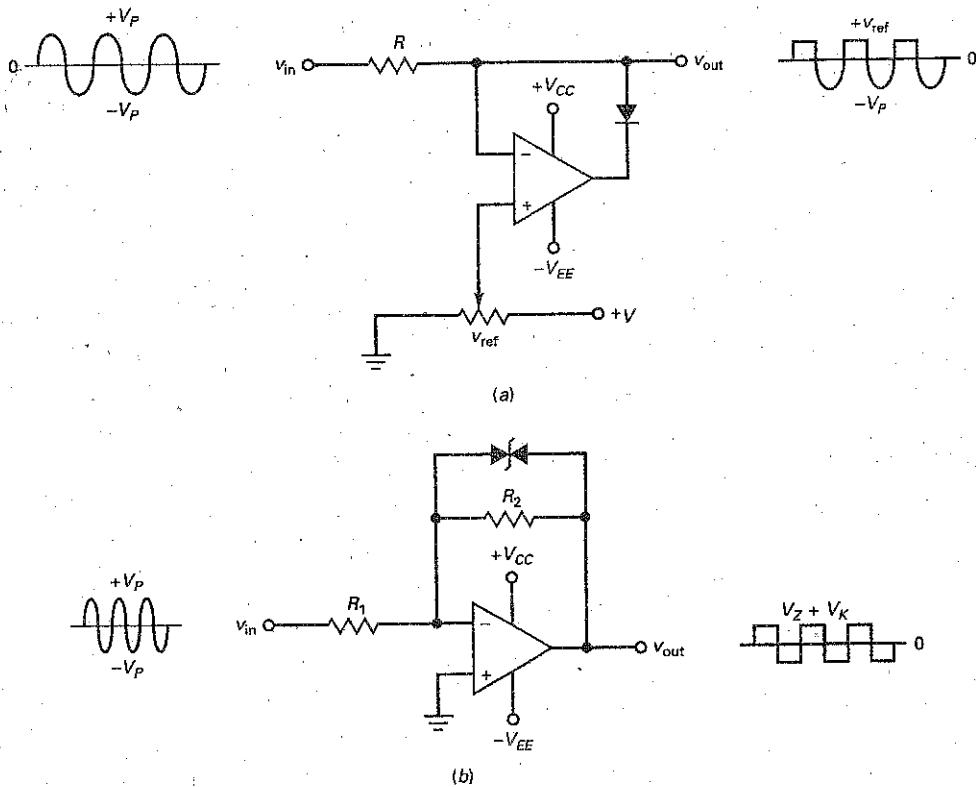
Figure 22-38a is an **active positive clipper**. With the wiper all the way to the left,  $v_{ref}$  is zero and the noninverting input is grounded. When  $v_{in}$  is positive, the op-amp output is negative and the diode is conducting. The low impedance of the diode produces heavy negative feedback because the feedback resistance approaches zero. For this condition, the output node is at virtual ground for all positive values of  $v_{in}$ .

When  $v_{in}$  goes negative, the output of the op amp is positive, which turns off the diode and opens the loop. When the loop is open, the virtual ground is lost and  $v_{out}$  equals the negative half cycle of input voltage. This is why the negative half cycle appears at the output as shown.

We can adjust the clipping level by moving the wiper to get different values of  $v_{ref}$ . In this way, we get the output waveform shown in Fig. 22-38a. The reference level can be varied between 0 and  $+V$ .

Figure 22-38b shows an active circuit that clips on both half cycles. Notice the back-to-back zener diodes in the feedback loop. Below the zener voltage, the circuit has a closed-loop gain of  $R_2/R_1$ . When the output tries to exceed the zener voltage plus one forward diode drop, the zener diode breaks down and

Figure 22-38 (a) Active positive limiter; (b) zener diodes produce rectangular wave.



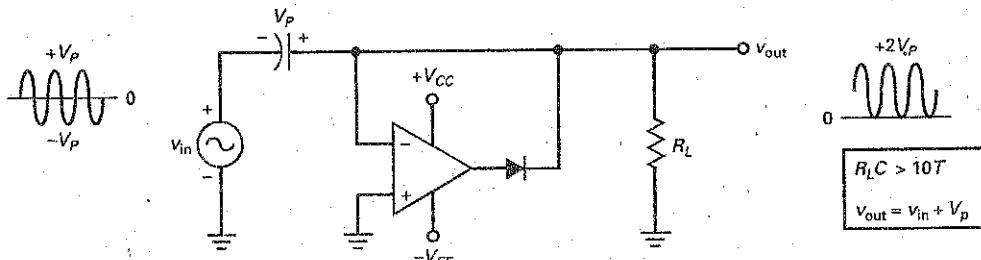
the output voltage is  $V_Z + V_K$  away from virtual ground. This is why the output is clipped as shown.

### Active Positive Clamper

Figure 22-39 is an active positive clamper. This circuit adds a dc component to the input signal. As a consequence, the output has the same size and shape as the input signal, except for the dc shift.

Here is the theory of operation: The first negative input half cycle is coupled through the uncharged capacitor and produces a positive op-amp output that

Figure 22-39 Active positive clamper.



turns on the diode. Because of the virtual ground, the capacitor charges to the peak value of the negative input half cycle with the polarity shown in Fig. 22-39. Just beyond the negative input peak, the diode turns off, the loop opens, and the virtual ground is lost. In this case, the output voltage is the sum of the input voltage and the capacitor voltage:

$$V_{\text{out}} = V_{\text{in}} + V_p \quad (22-21)$$

Since  $V_p$  is being added to a sinusoidal input voltage, the final output waveform is shifted positively through  $V_p$ , as shown in Fig. 22-39. The positively clamped waveform swings from 0 to  $+2V_p$ , which means that it has a peak-to-peak value of  $2V_p$ , the same as the input. Again, the negative feedback reduces the knee voltage by a factor of approximately  $A_{\text{VOL}}$ , which means that we can build excellent clampers for low-level inputs.

Figure 22-39 shows the op-amp output. During most of the cycle, the op amp operates in negative saturation. Right at the negative input peak, however, the op amp produces a sharp, positive-going pulse that replaces any charge lost by the clamping capacitor between negative input peaks.

## 22-10 The Differentiator

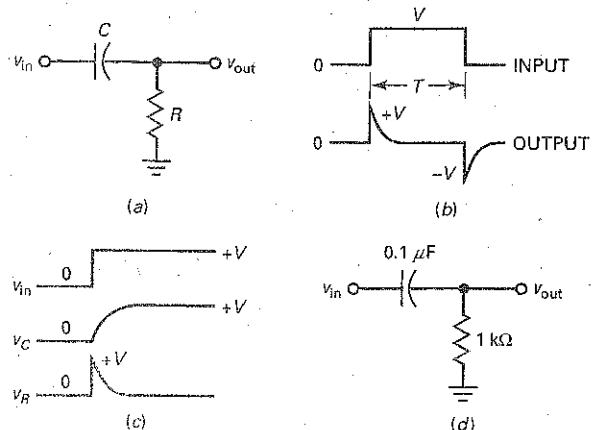
A differentiator is a circuit that performs a calculus operation called *differentiation*. It produces an output voltage proportional to the instantaneous rate of change of the input voltage. Common applications of a differentiator are to detect the leading and trailing edges of a rectangular pulse or to produce a rectangular output from a ramp input.

### RC Differentiator

An *RC* circuit like the one shown in Fig. 22-40a can be used to differentiate an input signal. The typical input signal is a rectangular pulse, as shown in Fig. 22-40b. The output of the circuit is a series of positive and negative spikes. The positive spike occurs at the same instant as the leading edge of the input, and the negative spike occurs at the same instant as the trailing edge. Spikes like these are useful signals because they indicate when the rectangular input signal starts and ends.

To understand how the *RC* differentiator works, look at Fig. 22-40c. When the input voltage changes from 0 to  $+V$ , the capacitor begins to charge

Figure 22-40 (a) *RC* differentiator; (b) rectangular input produces spiked output; (c) charging waveforms; (d) example.



exponentially, as shown. After five time constants, the capacitor voltage is within 1 percent of the final voltage. To satisfy Kirchhoff's voltage law, the voltage across the resistor of Fig. 22-40a is:

$$v_R = v_{in} - v_C$$

Since  $v_C$  is initially zero, the output voltage suddenly jumps from 0 to  $V$  and then decays exponentially, as shown in Fig. 22-40b. By a similar argument, the trailing edge of a rectangular pulse produces a negative spike. Incidentally, each spike in Fig. 22-40b has a peak value of approximately  $V$ , the size of the voltage step.

If an  $RC$  differentiator is to produce narrow spikes, the time constant should be at least 10 times smaller than the pulse width  $T$ :

$$RC < 10T$$

If the pulse width is 1 ms, the  $RC$  time constant should be less than 0.1 ms. Figure 22-40d shows an  $RC$  differentiator with a time constant of 0.1 ms. If you drive this circuit with any rectangular pulse that has  $T$  greater than 1 ms, the output is a series of sharp positive and negative voltage spikes.

### Op-Amp Differentiator

Figure 22-41a shows an op-amp differentiator. Notice the similarity to the op-amp integrator. The difference is that the resistor and capacitor are interchanged. Because of the virtual ground, the capacitor current passes through the feedback resistor, producing a voltage across this resistor. The capacitor current is given by this fundamental relation:

$$i = C \frac{dv}{dt}$$

The quantity  $dv/dt$  equals the slope of the input voltage.

One common application of the op-amp differentiator is to produce very narrow spikes, as shown in Fig. 22-41b. The advantage of an op-amp differentiator over a simple  $RC$  differentiator is that the spikes are coming from a low-impedance source, which makes driving typical load resistances easier.

### Practical Op-Amp Differentiator

The op-amp differentiator of Fig. 22-41a has a tendency to oscillate. To avoid this, a practical op-amp differentiator usually includes some resistance in series with the capacitor, as shown in Fig. 22-42. A typical value for this added resistance is between  $0.01R$  and  $0.1R$ . With this resistor, the closed-loop voltage gain is between 10 and 100. The effect is to limit the closed-loop voltage gain at higher frequencies, where the oscillation problem arises.

**Figure 22-41** (a) Op-amp differentiator; (b) rectangular input produces spiked output.

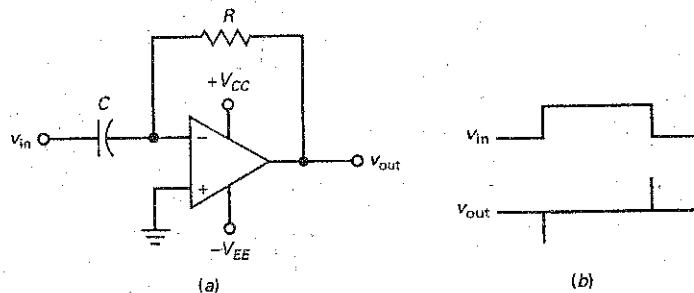
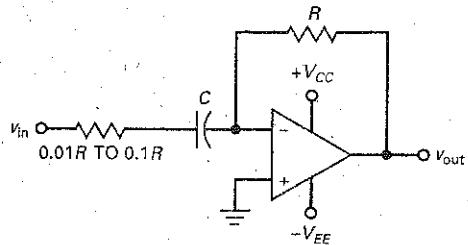


Figure 22-42 Resistance added to input to prevent oscillations.



## 22-11 Class-D Amplifier

The Class-B or Class-AB amplifier has been the main choice of many designers for audio amplifiers. This linear amplifier configuration has been able to provide the necessary conventional performance and cost requirements. Now, products such as LCD TVs, plasma TVs, and desktop PCs are driving the necessity for greater power output while maintaining or reducing the form-factor, without increasing costs. Portable powered devices, such as PDAs, cell phones, and notebook PCs, are demanding higher circuit efficiencies. Due to very high efficiency and low heat dissipation, the Class-D amplifier is now challenging the Class-AB amplifiers in many applications. The Class-D amplifier demonstrates a practical application of many of the circuits and devices we have been discussing.

Instead of being biased for linear operation, a **Class-D amplifier** uses output transistors operated as switches. This enables each transistor to either be in a cutoff or saturated mode. When in cutoff, its current is zero. When it is saturated, the voltage across it is low. In each mode, its power dissipation is very low. This concept increases the circuit efficiency, therefore, requires less power from the power supply and enables the use of smaller heat sinks for the amplifier.

A basic Class-D amplifier is shown in Fig. 22-43. The amplifier consists of a comparator op amp driving two MOSFETs operating as switches. The comparator has two input signals: one signal is the audio signal  $V_A$ , and the other input

Figure 22-43 Basic class-D amplifier.

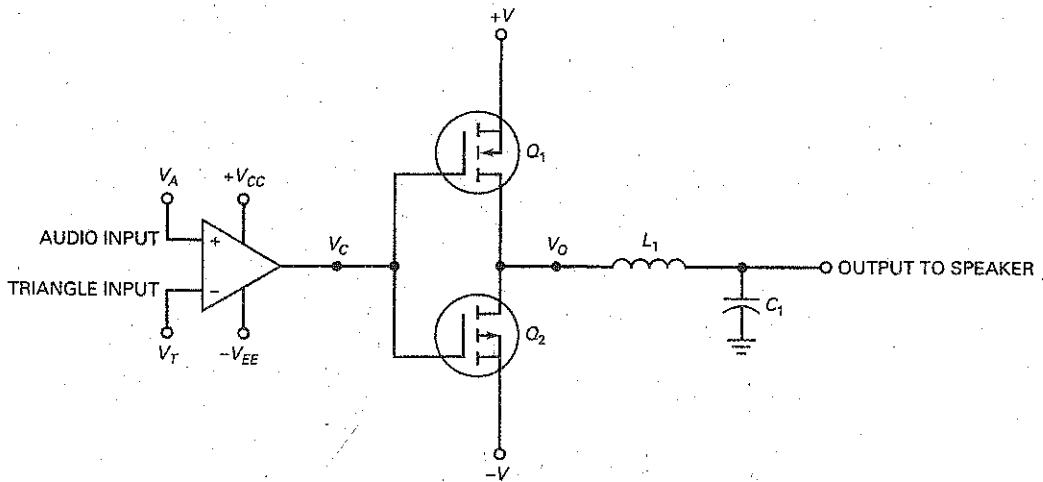
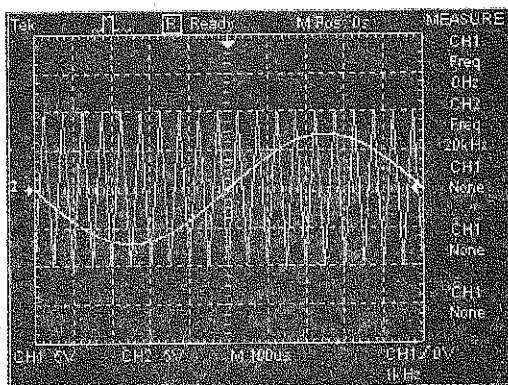


Figure 22-44 Input waveforms.



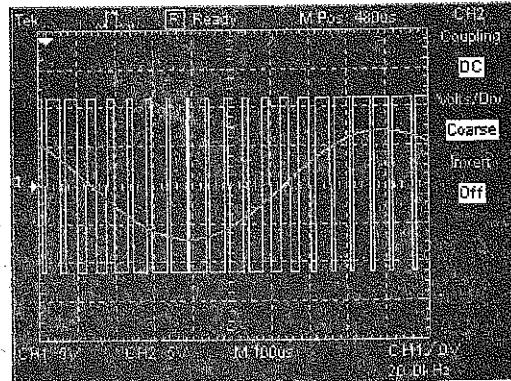
is a triangle wave  $V_T$  with a much higher frequency. The voltage value out of the comparator,  $V_C$ , will be approximately at either  $+V_{CC}$  or  $-V_{EE}$ . When  $V_A > V_T$ ,  $V_C = +V_{CC}$ . When  $V_A < V_T$ ,  $V_C = -V_{EE}$ .

The comparator's positive or negative output voltage drives two complementary common-source MOSFETs. When  $V_C$  is positive,  $Q_1$  is switched on and  $Q_2$  is off. When  $V_C$  is negative,  $Q_2$  is switched on and  $Q_1$  is off. The output voltage of each transistor will be slightly less than their  $+V$  and  $-V$  supply values.  $L_1$  and  $C_1$  act as a low-pass filter. When their values are properly chosen, this filter passes the average value of the switching transistors' output to the speaker. If the audio input signal  $V_A$  were zero,  $V_O$  would be a symmetrical square wave with an average value of zero volts.

To illustrate the operation of this circuit, examine Fig. 22-44. A 1 kHz sine wave is applied to the input at  $V_A$ , and a 20 kHz triangle wave is applied to input  $V_T$ . In practice, the triangle-wave input frequency would be many times higher than in this illustration. A frequency of 250–300 kHz is often used. The frequency should be as high as possible compared to the cutoff frequency,  $f_c$ , of  $L_1C_1$  for minimum output distortion. Also, note that the maximum voltage of  $V_A$  is at approximately 70 percent of  $V_T$ .

The resulting output  $V_O$  of the switching transistors is a **pulse-width-modulated (PWM)** waveform. The duty cycle of the waveform produces an output whose average value follows the audio input signal. This is shown in Fig. 22-45.

Figure 22-45 Output waveform following the input.



More sophisticated Class-D amplifiers use a MOSFET H-bridge circuit configuration for the switching devices and incorporate active low-pass filters. Resulting efficiencies can reach upwards from 85–90 percent, even at lower power levels. This exceeds the efficiency of the Class-AB amplifier, whose efficiency reaches a theoretical maximum of 78 percent at high-output levels and is much less efficient at lower power levels.

New generation IC Class-D amplifiers, such as the NJU8755, amplify analog input signals and produce PWM digital output signals. This provides for a fusion between digital and analog systems. The NJU8755, configured as a stereo bridge-tied load (BTL) and connected to an analog input signal, is capable of delivering 1.2 W/channel at 5 V into 8 ohms. This type of circuit also employs a standby mode designed to reduce power consumption to minimum levels during silent periods.

## Summary

### SEC. 22-1 COMPARATORS WITH ZERO REFERENCE

A comparator with a reference voltage of zero is called a zero-crossing detector. Diode clamps are often used to protect the comparator against excessively large input voltages. Comparators usually interface their outputs with digital circuits.

### SEC. 22-2 COMPARATORS WITH NONZERO REFERENCES

In some applications a threshold voltage different from zero may be preferred. Comparators with a nonzero reference voltage are sometimes called limit detectors. Although op amps may be used as comparators, IC comparators are optimized for this application by removing the internal compensating capacitor. This increases the switching speed.

### SEC. 22-3 COMPARATORS WITH HYSTERESIS

Noise is any kind of unwanted signal that is not derived from or harmonically related to the input signal. Because noise can cause false triggering of a comparator, positive feedback is used to create hysteresis. This prevents noise from producing false triggering. The positive feedback also speeds up the switching between output states.

### SEC. 22-4 WINDOW COMPARATOR

A window comparator, also called a double-ended limit detector, detects

when the input voltage is between two limits. To create the window, a window comparator uses two comparators with two different trip points.

### SEC. 22-5 THE INTEGRATOR

An integrator is useful for converting rectangular pulses into linear ramps. Because of the large input Miller capacitance, only the earliest part of an exponential charge is used. Since this early part is almost linear, the output ramps are almost perfect. Integrators are used to create the time bases of oscilloscopes.

### SEC. 22-6 WAVEFORM CONVERSION

We can use a Schmitt trigger to convert a sine wave to a rectangular wave. An integrator can convert a square wave to a triangular wave. With an adjustable resistor, we can control the duty cycle with a limit detector.

### SEC. 22-7 WAVEFORM GENERATION

With positive feedback, we can build oscillators, circuits that generate or create an output signal with no external input signal. A relaxation oscillator uses the charging of a capacitor to generate an output signal. By cascading a relaxation oscillator and an integrator, we can produce a triangular output waveform.

### SEC. 22-8 ANOTHER TRIANGULAR GENERATOR

The output of a noninverting Schmitt trigger can be used to drive an integrator. If the output of the integrator is used as the input to the Schmitt trigger, we have an oscillator that produces both square waves and triangular waves.

### SEC. 22-9 ACTIVE DIODE CIRCUITS

With op amps, we can build active half-wave rectifiers, peak detectors, clippers, and clampers. In all these circuits, the closed-loop knee voltage equals the knee voltage divided by the open-loop voltage gain. Because of this, we can process low-level signals.

### SEC. 22-10 THE DIFFERENTIATOR

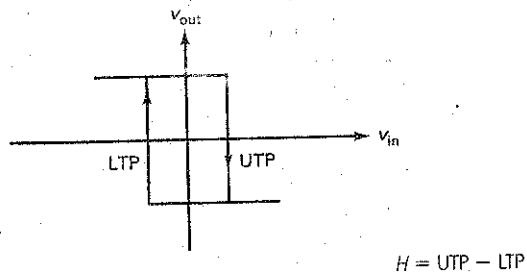
When a square wave drives an *RC* differentiator, the output is a series of narrow positive and negative voltage spikes. With an op amp, we can improve the differentiation and get a low output impedance.

### SEC. 22-11 CLASS-D AMPLIFIER

The Class-D amplifier uses output transistors operated as switches. Instead of operating in a linear region, these transistors are alternately driven into saturation and cutoff by the output signal of a comparator circuit. The Class-D amplifier is capable of very high circuit efficiencies and is gaining popularity in portable equipment needing audio amplification.

## Definitions

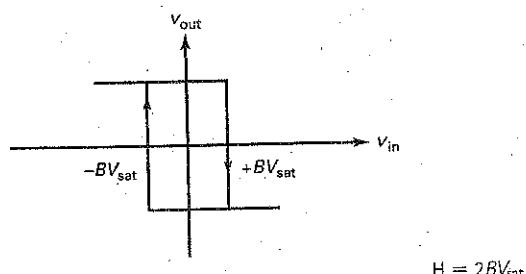
(22-8) Hysteresis:



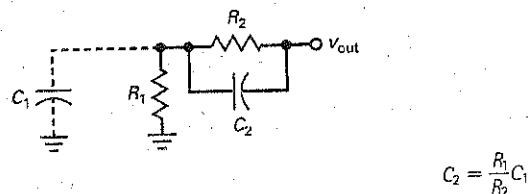
## Derivations

For all derivations not shown here, see appropriate figures in chapter.

(22-9) Hysteresis:



(22-12) Speed-up capacitance:



## Student Assignments

1. In a nonlinear op-amp circuit, the
  - a. Op amp never saturates
  - b. Feedback loop is never opened
  - c. Output shape is the same as the input shape
  - d. Op amp may saturate
2. To detect when the input is greater than a particular value, use a
  - a. Comparator
  - b. Clamper
  - c. Limiter
  - d. Relaxation oscillator
3. The voltage out of a Schmitt trigger is
  - a. A low voltage
  - b. A high voltage
  - c. Either a low or a high voltage
  - d. A sine wave
4. Hysteresis prevents false triggering associated with
  - a. A sinusoidal input
  - b. Noise voltages
  - c. Stray capacitances
  - d. Trip points
5. If the input is a rectangular pulse, the output of an integrator is a
  - a. Sine wave
  - b. Square wave
  - c. Ramp
  - d. Rectangular pulse
6. When a large sine wave drives a Schmitt trigger, the output is a
  - a. Rectangular wave
  - b. Triangular wave
  - c. Rectified sine wave
  - d. Series of ramps

7. If pulse width decreases and the period stays the same, the duty cycle
- Decreases
  - Stays the same
  - Increases
  - Is zero
8. The output of a relaxation oscillator is a
- Sine wave
  - Square wave
  - Ramp
  - Spike
9. If  $A_{vol} = 100,000$ , the closed-loop knee voltage of a silicon diode is
- $1 \mu V$
  - $3.5 \mu V$
  - $7 \mu V$
  - $14 \mu V$
10. The input to a peak detector is a triangular wave with a peak-to-peak value of 8 V and an average value of 0. The output is
- 0
  - 4 V
  - 8 V
  - 16 V
11. The input to a positive limiter is a triangular wave with a peak-to-peak value of 8 V and an average value of 0. If the reference level is 2 V, the output has a peak-to-peak value of
- 0
  - 6 V
  - 2 V
  - 8 V
12. The discharging time constant of a peak detector is 100 ms. The lowest frequency you should use is
- 10 Hz
  - 1 kHz
  - 100 Hz
  - 10 kHz
13. A comparator with a trip point of zero is sometimes called a
- Threshold detector
  - Zero-crossing detector
  - Positive limit detector
  - Half-wave detector
14. To work properly, many IC comparators need an external
- Compensating capacitor
  - Pullup resistor
  - Bypass circuit
  - Output stage
15. A Schmitt trigger uses
- Positive feedback
  - Negative feedback
  - Compensating capacitors
  - Pullup resistors
16. A Schmitt trigger
- Is a zero-crossing detector
  - Has two trip points
  - Produces triangular output waves
  - Is designed to trigger on noise voltage
17. A relaxation oscillator depends on the charging of a capacitor through a
- Resistor
  - Inductor
  - Capacitor
  - Noninverting input
18. A ramp of voltage
- Always increases
  - Is a rectangular pulse
  - Increases or decreases at a linear rate
  - Is produced by hysteresis
19. The op-amp integrator uses
- Inductors
  - The Miller effect
  - Sinusoidal inputs
  - Hysteresis
20. The trip point of a comparator is the input voltage that causes
- The circuit to oscillate
  - Peak detection of the input signal
  - The output to switch states
  - Clamping to occur
21. In an op-amp integrator, the current through the input resistor flows into the
- Inverting input
  - Noninverting input
  - Bypass capacitor
  - Feedback capacitor
22. An active half-wave rectifier has a knee voltage of
- $V_K$
  - 0.7 V
  - More than 0.7 V
  - Much less than 0.7 V
23. In an active peak detector, the discharging time constant is
- Much longer than the period
  - Much shorter than the period
  - Equal to the period
  - The same as the charging time constant
24. If the reference voltage is zero, the output of an active positive limiter is
- Positive
  - Negative
  - Either positive or negative
  - A ramp
25. The output of an active positive clamer is
- Positive
  - Negative
  - Either positive or negative
  - A ramp
26. The positive clamper adds
- A positive dc voltage to the input
  - A negative dc voltage to the input
  - An ac signal to the output
  - A trip point to the point
27. A window comparator
- Has only one usable threshold
  - Uses hysteresis to speed up response
  - Clamps the input positively
  - detects an input voltage between two limits
28. An RC differentiator circuit produces an output voltage related to the instantaneous rate of change of the input
- Current
  - Resistance
  - Voltage
  - Frequency
29. An op-amp differentiator is used to produce
- Output square waves
  - Output sine waves
  - Output voltage spikes
  - Output dc levels
30. Class-D amplifiers are very efficient because
- The output transistors are either cutoff or saturated
  - They do not require a dc voltage source
  - They use RF tuned stages
  - They conduct for 360° of the input voltage

## Problems

### SEC. 22-1 COMPARATORS WITH ZERO REFERENCE

- 22-1 In Fig. 22-1a, the comparator has an open-loop voltage gain of 106 dB. What is the input voltage that produces positive saturation if the supply voltages are  $\pm 20$  V?
- 22-2 If the input voltage is 50 V in Fig. 22-2a, what is the approximation current through the left clamping diode if  $R = 10 \text{ k}\Omega$ ?
- 22-3 In Fig. 22-7a, each zener diode is a 1N4736A. If the supply voltages are  $\pm 15$  V, what is the output voltage?
- 22-4 The dual supplies of Fig. 22-7b are reduced to  $\pm 12$  V, and the diode is reversed. What is the output voltage?
- 22-5 If the diode of Fig. 22-9 is reversed and the supplies changed to  $\pm 9$  V, what is the output when the strobe is high? When it is low?

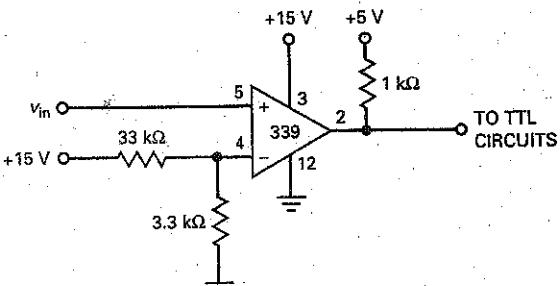
### SEC. 22-2 COMPARATORS WITH NONZERO REFERENCES

- 22-6 In Fig. 22-11a, the dual supply voltages are  $\pm 15$  V. If  $R_1 = 47 \text{ k}\Omega$  and  $R_2 = 12 \text{ k}\Omega$ , what is the reference voltage? If the bypass capacitance is  $0.5 \mu\text{F}$ , what is the cutoff frequency?
- 22-7 In Fig. 22-11c, the dual supply voltages are  $\pm 12$  V. If  $R_1 = 15 \text{ k}\Omega$  and  $R_2 = 7.5 \text{ k}\Omega$ , what is the reference voltage? If the bypass capacitance is  $1.0 \mu\text{F}$ , what is the cutoff frequency?
- 22-8 In Fig. 22-12,  $V_{cc} = 9$  V,  $R_1 = 22 \text{ k}\Omega$ , and  $R_2 = 4.7 \text{ k}\Omega$ . What is the output duty cycle if the input is a sine wave with a peak of 7.5 V?
- 22-9 In Fig. 22-46, what is the output duty cycle if the input is a sine wave with a peak of 5 V?

### SEC. 22-3 COMPARATORS WITH HYSTERESIS

- 22-10 In Fig. 22-18a,  $R_1 = 2.2 \text{ k}\Omega$ , and  $R_2 = 18 \text{ k}\Omega$ . If  $V_{sat} = 14$  V, what are the trip points? What is the hysteresis?

Figure 22-46

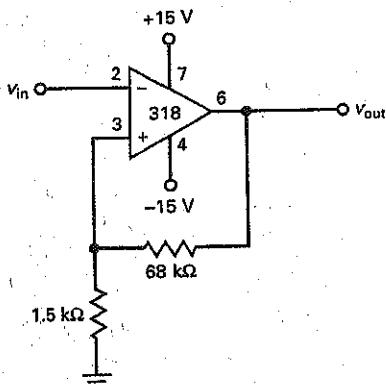


- 22-11 If  $R_1 = 1 \text{ k}\Omega$ ,  $R_2 = 20 \text{ k}\Omega$ , and  $V_{sat} = 15$  V, what is the maximum peak-to-peak noise the circuit of Fig. 22-19a can withstand without false triggering?

- 22-12 The Schmitt trigger of Fig. 22-20 has  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 18 \text{ k}\Omega$ . If the stray capacitance across  $R_1$  is  $3.0 \text{ pF}$ , what size should the speed-up capacitor be?

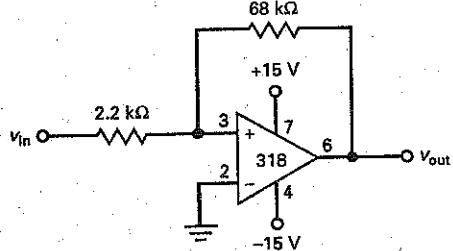
- 22-13 If  $V_{sat} = 13.5$  V in Fig. 22-47, what are the trip points and hysteresis?

Figure 22-47



- 22-14 What are the trip points and hysteresis if,  $V_{sat} = 1.4$  V in Fig. 22-48?

Figure 22-48



### SEC. 22-4 WINDOW COMPARATOR

- 22-15 In Fig. 22-22a, the LTP and UTP are changed to  $+3.5$  V and  $+4.75$  V. If  $V_{sat} = 12$  V and the input is a sine wave with a peak of 10 V, what is the output voltage waveform?

- 22-16 In Fig. 22-23a, the  $2R$  resistance is changed to  $4R$ , and the  $3R$  resistance is changed to  $6R$ . What are the new reference voltages?

### SEC. 22-5 THE INTEGRATOR

- 22-17 What is the capacitor charging current in Fig. 22-49 when the input pulse is high?
- 22-18 In Fig. 22-49, the output voltage is reset just before the pulse begins. What is the output voltage at the end of the pulse?
- 22-19 The input voltage is changed from 5 to 0.1 V in Fig. 22-49. The capacitance of Fig. 22-49 is changed to each of these values: 0.1, 1, 10, and 100  $\mu\text{F}$ . A reset is done at the beginning of the pulse. What is the output voltage at the end of the pulse for each capacitance?

### SEC. 22-6 WAVEFORM CONVERSION

- 22-20 What is the output voltage in Fig. 22-50?
- 22-21 If the capacitance is changed to 0.068  $\mu\text{F}$  in Fig. 22-50, what is the output voltage?
- 22-22 In Fig. 22-50, what happens to the output voltage if the frequency changes to 5 kHz? To 20 kHz?
- 22-23 **Multisim** What is the duty cycle in Fig. 22-51 when the wiper is at the top? What is the duty cycle when the wiper is at the bottom?
- 22-24 **Multisim** What is the duty cycle in Fig. 22-51 when the wiper is one-half of the way from the top?

Figure 22-49

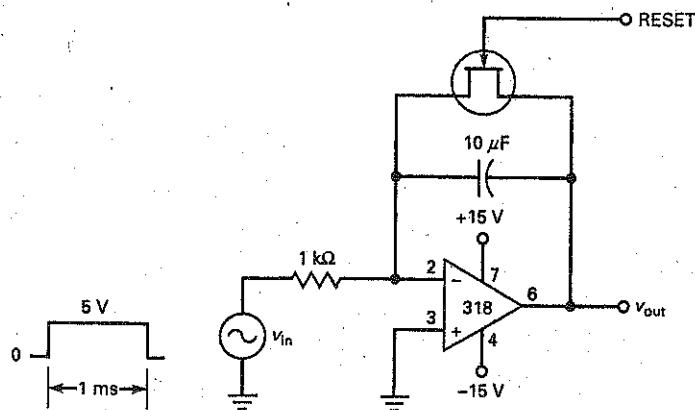


Figure 22-50

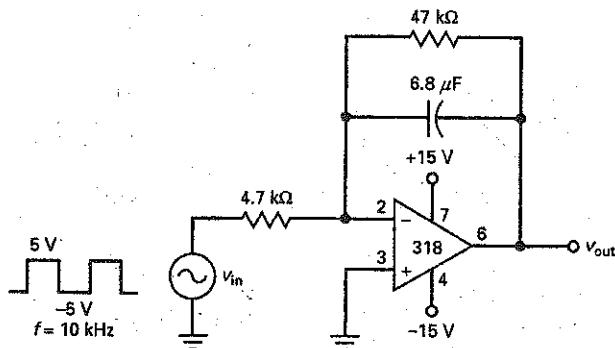
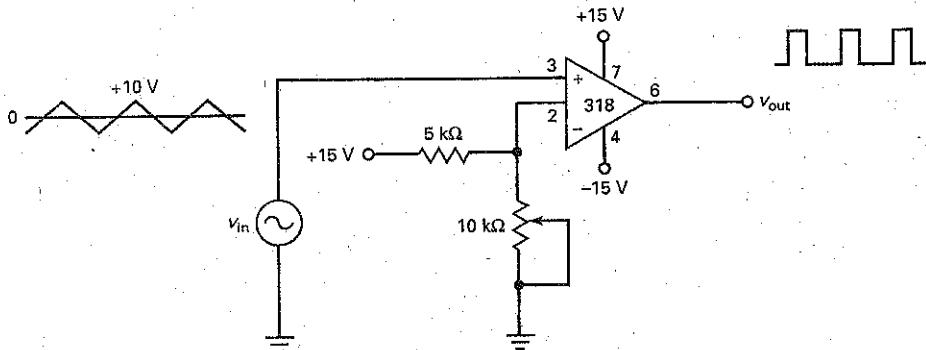


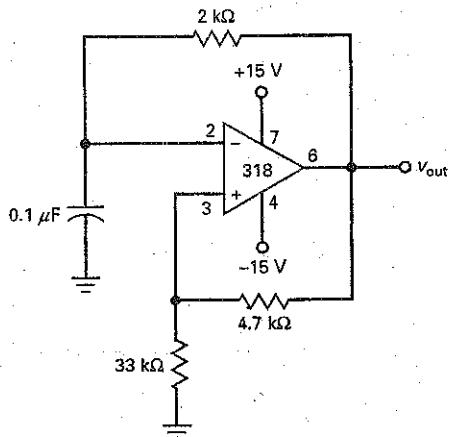
Figure 22-51



#### SEC. 22-7 WAVEFORM GENERATION

- 22-25 **MultiSim** What is the frequency of the output signal in Fig. 22-52?

Figure 22-52



- 22-26 **MultiSim** If all resistors are doubled in Fig. 22-52, what happens to the frequency?

- 22-27 The capacitor of Fig. 22-52 is changed to  $0.47 \mu\text{F}$ . What is the new frequency?

#### SEC. 22-8 ANOTHER TRIANGULAR GENERATOR

- 22-28 In Fig. 22-35a,  $R_1 = 2.2 \text{ k}\Omega$ , and  $R_2 = 22 \text{ k}\Omega$ . If  $V_{\text{sat}} = 12 \text{ V}$ , what are the trip points of the Schmitt trigger? What is the hysteresis?

- 22-29 In Fig. 22-35a,  $R_3 = 2.2 \text{ k}\Omega$ ,  $R_4 = 22 \text{ k}\Omega$ , and  $C = 4.7 \mu\text{F}$ . If the output of the Schmitt trigger is a square wave with a peak-to-peak value of  $28 \text{ V}$  and a frequency of  $5 \text{ kHz}$ , what is the peak-to-peak output of the triangular wave generator?

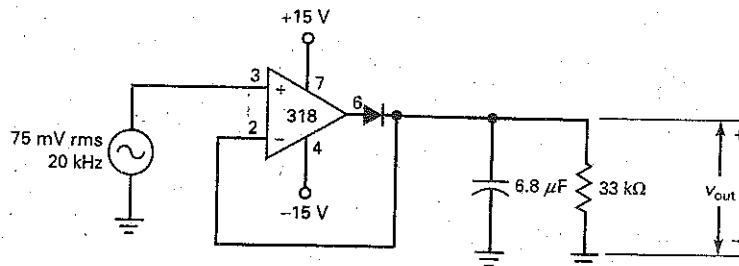
#### SEC. 22-9 ACTIVE DIODE CIRCUITS

- 22-30 In Fig. 22-36, the input sine wave has a peak of  $100 \text{ mV}$ . What is the output voltage?
- 22-31 What is the output voltage in Fig. 22-53?
- 22-32 What is the lowest recommended frequency in Fig. 22-53?
- 22-33 Suppose the diode of Fig. 22-53 is reversed. What is the output voltage?
- 22-34 The input voltage of Fig. 22-53 is changed from  $75 \text{ mV rms}$  to  $150 \text{ mV pp}$ . What is the output voltage?
- 22-35 If the peak input voltage is  $100 \text{ mV}$  in Fig. 22-39, what is the output voltage?
- 22-36 A positive clamper like Fig. 22-39 has  $R_L = 10 \text{ k}\Omega$  and  $C = 4.7 \mu\text{F}$ . What is the lowest recommended frequency for this clamper?

#### SEC. 22-10 THE DIFFERENTIATOR

- 22-37 In Fig. 22-40, the input voltage is a square wave with a frequency of  $10 \text{ kHz}$ . How many positive and negative spikes does the differentiator produce in  $1 \text{ s}$ ?
- 22-38 In Fig. 22-41, the input voltage is a square wave with a frequency of  $1 \text{ kHz}$ . What is the time between the negative and positive output spike?

Figure 22-53



## Critical Thinking

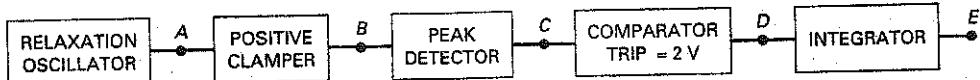
- 22-39 Suggest one or more changes in Fig. 22-46 to get a reference voltage of 1 V.
- 22-40 The stray capacitance across the output in Fig. 22-46 is 50 pF. What is the risetime of the output waveform when it switches from low to high?
- 22-41 A bypass capacitor of  $47 \mu\text{F}$  is connected across the  $3.3 \text{ k}\Omega$  of Fig. 22-46. What is the cutoff frequency of the bypass circuit? If the supply ripple is 1 V rms, what is the approximate ripple at the inverting input?
- 22-42 What is the average current through the  $1-\text{k}\Omega$  resistor of Fig. 22-14a if the input is a sine wave with a peak of 5 V? Assume  $R_1 = 33 \text{ k}\Omega$  and  $R_2 = 3.3 \text{ k}\Omega$ .
- 22-43 The resistors of Fig. 22-47 have a tolerance of  $\pm 5\%$  percent. What is the minimum hysteresis?
- 22-44 In Fig. 22-23a, the LTP and UTP are changed to  $+3.5 \text{ V}$  and  $+4.75 \text{ V}$ . If  $V_{\text{sat}} = 12 \text{ V}$  and the input is a sine wave with a peak of 10 V, what is the output duty cycle?
- 22-45 We want to produce ramp output voltages in Fig. 22-49 that swing from 0 to  $+10 \text{ V}$  with times of 0.1, 1, and 10 ms. What changes can you make in the circuit to accomplish this? (Many right answers are possible.)
- 22-46 We want the output frequency of Fig. 22-52 to be 20 kHz. Suggest some changes that will accomplish this.
- 22-47 The noise voltage at the input of Fig. 22-48 may be as large as 1 V pp. Suggest one or more changes that make the circuit immune to noise voltage.
- 22-48 Company XYZ is mass-producing relaxation oscillators. The output voltage is supposed to be at least 10 V pp. Suggest some ways to check the output of each unit to see whether it is at least 10 V pp. (There are many right answers here. See how many you can think of. You can use any device or circuit in this and earlier chapters.)
- 22-49 How can you build a circuit that turns on the lights when it gets dark and turns them off when it gets light? (Use this and earlier chapters to find as many right answers as you can think of.)
- 22-50 You have some electronics equipment that malfunctions when the line voltage is too low. Suggest one or more ways to set off an audible alarm when the line voltage is less than 105 V rms.
- 22-51 Radar waves travel at 186,000 mi/s. A transmitter on earth sends a radar wave to the moon, and an echo of this radar wave returns to earth. In Fig. 22-49,  $1 \text{ k}\Omega$  is changed to  $1 \text{ M}\Omega$ . The input rectangular pulse starts at the instant the radar wave is sent to the moon, and the pulse ends at the instant the radar wave arrives back on earth. If the output ramp has decreased from 0 to a final voltage of  $-1.23 \text{ V}$ , how far away is the moon?

## Troubleshooting

Use Fig. 22-54 for the remaining problems. Each test point, A through E, will show an oscilloscope display. Based on your knowledge of the circuits and waveforms, you are to locate the most suspicious block for further testing. Familiarize yourself with normal operation by using the OK measurements. When ready to troubleshoot, do the following problems.

- 22-52 Find Troubles 1 and 2.
- 22-53 Find Troubles 3 through 5.
- 22-54 Find Troubles 6 and 7.
- 22-55 Find Troubles 8 through 10.

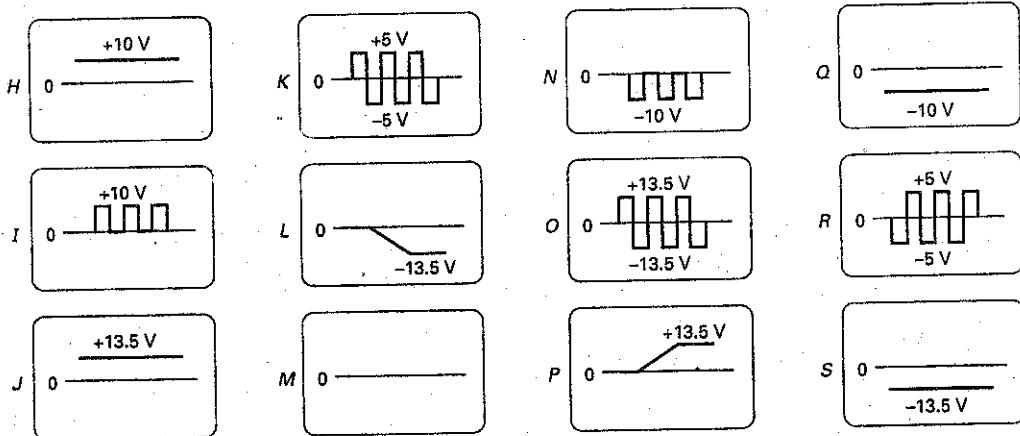
Figure 22-54



Troubleshooting

Trouble	$V_A$	$V_B$	$V_C$	$V_D$	$V_E$
OK	K	I	H	J	L
T1	K	N	M	S	P
T2	K	I	H	J	O
T3	M	M	M	S	P
T4	R	I	M	S	P
T5	K	M	M	S	P
T6	K	I	H	S	P
T7	K	I	H	J	J
T8	K	I	Q	S	P
T9	R	I	H	J	S
T10	K	I	H	M	M

WAVEFORMS



## Job Interview Questions

- Sketch a zero-crossing detector and describe its theory of operation.
- How can I prevent a noisy input from triggering a comparator? Draw a schematic diagram and some waveforms to support your discussion.
- Tell me how an integrator works by drawing a schematic diagram and some waveforms.
- You are going to mass-produce a circuit that is supposed to have a dc output voltage between 3 and 4 V. What kind of a comparator would you use? How would you connect green and red LEDs across the comparator output to indicate pass or fail?
- What does the term *bounded output* mean? How can the task be easily accomplished?

6. How does a Schmitt trigger differ from a zero-crossing detector?
7. How can we protect the input of a comparator from excessively large input voltages?
8. How does an IC comparator differ from a typical op amp?
9. If a rectangular pulse drives an integrator, what kind of output can we expect?

10. What effect does an active diode circuit have on the knee voltage?
11. What does a relaxation oscillator do? Explain the general idea of how it does this.
12. If a rectangular pulse drives a differentiator, what kind of output can we expect?

## Self-Test Answers

- |       |       |       |
|-------|-------|-------|
| 1. d  | 11. c | 21. d |
| 2. a  | 12. b | 22. d |
| 3. c  | 13. b | 23. a |
| 4. b  | 14. b | 24. b |
| 5. c  | 15. a | 25. a |
| 6. a  | 16. b | 26. a |
| 7. a  | 17. a | 27. d |
| 8. b  | 18. c | 28. b |
| 9. c  | 19. b | 29. c |
| 10. b | 20. c | 30. a |

## Practice Problem Answers

22-4  $V_{ref} = 7.5 \text{ V};$   
 $f_c = 0.508 \text{ Hz}$

22-6  $B = 0.0435;$   
 $\text{UTP} = 0.587 \text{ V};$   
 $\text{LTP} = -0.587 \text{ V};$   
 $H = 1.17 \text{ V}$

22-7  $V = 0.800 \text{ V};$   
time constant = 1000 sec.

22-8  $C = 2.5 \mu\text{F}$   
  
22-9  $W = 83.3 \mu\text{S};$   
 $D = 0.167$

22-10  $T = 479 \mu\text{S};$   
 $f = 2.1 \text{ kHz}$

22-11  $V_{out(pp)} = 32.3 \text{ mV pp}$   
  
22-12  $V_{out(pp)} = 0.52 \text{ V};$   
 $f = 2.5 \text{ kHz}$

# 23

# Oscillators

- At frequencies under 1 MHz, we can use *RC* oscillators to produce almost perfect sine waves. These low-frequency oscillators use op amps and *RC* resonant circuits to determine the frequency of oscillation.
- Above 1 MHz, *LC* oscillators are used. These high-frequency oscillators use transistors and *LC* resonant circuits. This chapter also discusses a popular chip called the 555 timer. It is used in many applications to produce time delays, voltage-controlled oscillators, and modulated output signals. The chapter also covers an important communications circuit called the phase-locked loop (PLL) and concludes with the popular XR-2206 function generator IC.

## Chapter Outline

- 23-1 Theory of Sinusoidal Oscillation
- 23-2 The Wien-Bridge Oscillator
- 23-3 Other *RC* Oscillators
- 23-4 The Colpitts Oscillator
- 23-5 Other *LC* Oscillators
- 23-6 Quartz Crystals
- 23-7 The 555 Timer
- 23-8 Astable Operation of the 555 Timer
- 23-9 555 Circuits
- 23-10 The Phase-Locked Loop
- 23-11 Function Generator ICs

## Objectives

After studying this chapter, you should be able to:

- Explain loop gain and phase and how they relate to sinusoidal oscillators.
- Describe the operation of several *RC* sinusoidal oscillators.
- Describe the operation of several *LC* sinusoidal oscillators.
- Explain how crystal-controlled oscillators work.
- Discuss the 555 timer IC, its modes of operation, and how it is used as an oscillator.
- Explain the operation of phase-locked loops.
- Describe the operation of the XR-2206 function generator IC.

## Vocabulary

Armstrong oscillator	lock range	pulse-position modulation (PPM)
astable	modulating signal	pulse-width modulation (PWM)
bistable multivibrator	monostable	quartz-crystal oscillator
capture range	mounting capacitance	resonant frequency $f_r$
carrier	multivibrator	twin-T oscillator
Clapp oscillator	natural logarithm	voltage-controlled oscillator (VCO)
Colpitts oscillator	notch filter	voltage-to-frequency converter
frequency modulation (FM)	phase detector	Wien-bridge oscillator
frequency-shift keying (FSK)	phase-locked loop (PLL)	
fundamental frequency	phase-shift oscillator	
Hartley oscillator	Pierce crystal oscillator	
lead-lag circuit	piezoelectric effect	

## 23-1 Theory of Sinusoidal Oscillation

To build a sinusoidal oscillator, we need to use an amplifier with positive feedback. The idea is to use the feedback signal in place of the input signal. If the feedback signal is large enough and has the correct phase, there will be an output signal even though there is no external input signal.

### GOOD TO KNOW

In most oscillators, the feedback voltage is a fractional part of the output voltage. When this is the case, the voltage gain  $A_v$  must be large enough to ensure that  $A_vB = 1$ . In other words, the amplifier voltage gain must at least be large enough to overcome the losses in the feedback network. However, if an emitter follower is used as the amplifier, the feedback network must provide a slight amount of gain to ensure that  $A_vB = 1$ . For example, if the voltage gain  $A_v$  of an emitter follower equals 0.9, then  $B$  must equal  $1/0.9$  or 1.11. RF communication circuits sometimes use oscillators that contain an emitter follower for the amplifier.

### Loop Gain and Phase

Figure 23-1a shows an ac voltage source driving the input terminals of an amplifier. The amplified output voltage is:

$$v_{\text{out}} = A_v(v_{\text{in}})$$

This voltage drives a feedback circuit that is usually a resonant circuit. Because of this, we get maximum feedback at one frequency. In Fig. 23-1a, the feedback voltage returning to point  $x$  is given by:

$$v_f = A_vB(v_{\text{in}})$$

where  $B$  is the feedback fraction.

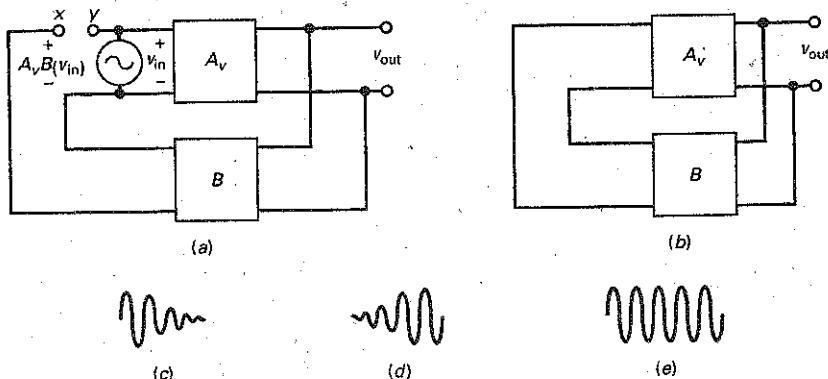
If the phase shift through the amplifier and feedback circuit is equivalent to  $0^\circ$ ,  $A_vB(v_{\text{in}})$  is in phase with  $v_{\text{in}}$ .

Suppose we connect point  $x$  to point  $y$  and simultaneously remove voltage source  $v_{\text{in}}$ . Then the feedback voltage  $A_vB(v_{\text{in}})$  drives the input of the amplifier, as shown in Fig. 23-1b.

What happens to the output voltage? If  $A_vB$  is less than 1,  $A_vB(v_{\text{in}})$  is less than  $v_{\text{in}}$  and the output signal will die out, as shown in Fig. 23-1c. However, if  $A_vB$  is greater than 1,  $A_vB(v_{\text{in}})$  is greater than  $v_{\text{in}}$  and the output voltage builds up (Fig. 23-1d). If  $A_vB$  equals 1, then  $A_vB(v_{\text{in}})$  equals  $v_{\text{in}}$  and the output voltage is a steady sine wave like the one in Fig. 23-1e. In this case, the circuit supplies its own input signal.

In any oscillator the loop gain  $A_vB$  is greater than 1 when the power is first turned on. A small starting voltage is applied to the input terminals, and the output voltage builds up, as shown in Fig. 23-1d. After the output voltage reaches a certain level,  $A_vB$  automatically decreases to 1, and the peak-to-peak output becomes constant (Fig. 23-1e).

**Figure 23-1** (a) Feedback voltage returns to point  $x$ ; (b) connecting points  $x$  and  $y$ ; (c) oscillations die out; (d) oscillations increase; (e) oscillations are fixed in amplitude.



## Starting Voltage Is Thermal Noise

Where does the starting voltage come from? As discussed in Chap. 22, every resistor contains some free electrons. Because of the ambient temperature, these free electrons move randomly in different directions and generate a noise voltage across the resistor. The motion is so random that it contains frequencies to over 1000 GHz. You can think of each resistor as a small ac voltage source producing all frequencies.

In Fig. 23-1b, here is what happens: When you first turn on the power, the only signals in the system are the noise voltages generated by the resistors. These noise voltages are amplified and appear at the output terminals. The amplified noise, which contains all frequencies, drives the resonant feedback circuit. By deliberate design, we can make the loop gain greater than 1 and the loop phase shift equal to  $0^\circ$  at the resonant frequency. Above and below the resonant frequency, the phase shift is different from  $0^\circ$ . As a result, oscillations will build up only at the resonant frequency of the feedback circuit.

## $A_vB$ Decreases to Unity

There are two ways in which  $A_vB$  can decrease to 1. Either  $A_v$  can decrease or  $B$  can decrease. In some oscillators, the signal is allowed to build up until clipping occurs because of saturation and cutoff. This is equivalent to reducing voltage gain  $A_v$ . In other oscillators, the signal builds up and causes  $B$  to decrease before clipping occurs. In either case, the product  $A_vB$  decreases until it equals 1.

Here are the key ideas behind any feedback oscillator:

1. Initially, loop gain  $A_vB$  is greater than 1 at the frequency where the loop phase shift is  $0^\circ$ .
2. After the desired output level is reached,  $A_vB$  must decrease to 1 by reducing either  $A_v$  or  $B$ .

## 23-2 The Wien-Bridge Oscillator

The Wien-bridge oscillator is the standard oscillator circuit for low to moderate frequencies, in the range of 5 Hz to about 1 MHz. It is almost always used in commercial audio generators and is usually preferred for other low-frequency applications.

### Lag Circuit

The voltage gain of the bypass circuit of Fig. 23-2a is:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{X_C}{\sqrt{R^2 + X_C^2}}$$

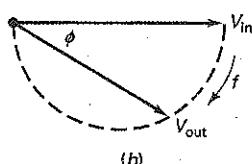
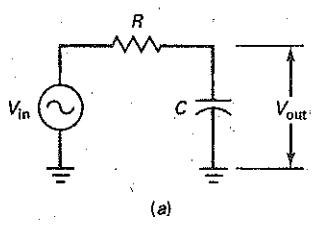
and the phase angle is:

$$\phi = -\arctan \frac{R}{X_C}$$

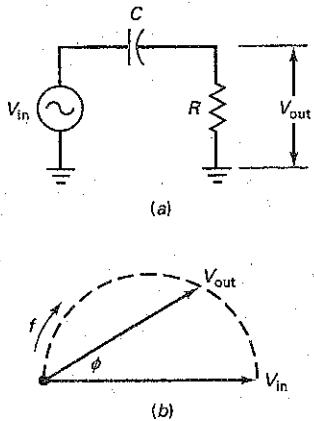
where  $\phi$  is the phase angle between the output and the input.

Notice the minus sign in this equation for phase angle. It means that the output voltage lags the input voltage, as shown in Fig. 23-2b. Because of this, a bypass circuit is also called a *lag circuit*. In Fig. 23-2b, the half circle shows the possible positions of the output phasor voltage. This implies that the output phasor can lag the input phasor by an angle between  $0^\circ$  and  $-90^\circ$ .

Figure 23-2 (a) Bypass capacitor; (b) phasor diagram.



**Figure 23-3** (a) Coupling circuit; (b) phasor diagram.



## Lead Circuit

Figure 23-3a shows a coupling circuit. The voltage gain in this circuit is:

$$\frac{V_{out}}{V_{in}} = \frac{R}{\sqrt{R^2 + X_C^2}}$$

and the phase angle is:

$$\phi = \arctan \frac{X_C}{R}$$

Notice that the phase angle is positive. It means that the output voltage leads the input voltage, as shown in Fig. 23-3b. Because of this, a coupling circuit is also called a *lead circuit*. In Fig. 23-3b, the half circle shows the possible positions of the output phasor voltage. This implies that the output phasor can lead the input phasor by an angle between  $0^\circ$  and  $+90^\circ$ .

Coupling and bypass circuits are examples of phase-shifting circuits. These circuits shift the phase of the output signal either positive (leading) or negative (lagging) with respect to the input signal. A sinusoidal oscillator always uses some kind of phase-shifting circuit to produce oscillation at one frequency.

## Lead-Lag Circuit

The Wien-bridge oscillator uses a resonant feedback circuit called a *lead-lag circuit* (Fig. 23-4). At very low frequencies, the series capacitor appears open to the input signal, and there is no output signal. At very high frequencies, the shunt capacitor looks shorted, and there is no output. In between these extremes, the output voltage reaches a maximum value (see Fig. 23-5a). The frequency where the output is maximum is the **resonant frequency**  $f_r$ . At this frequency, the feedback fraction  $B$  reaches a maximum value of  $\frac{1}{2}$ .

Figure 23-5b shows the phase angle of the output voltage versus input voltage. At very low frequencies, the phase angle is positive (leading). At very high frequencies, the phase angle is negative (lagging). At the resonant frequency, the phase shift is  $0^\circ$ . Figure 23-5c shows the phasor diagram of the input and output voltages. The tip of the phasor can lie anywhere on the dashed circle. Because of this, the phase angle may vary from  $+90^\circ$  to  $-90^\circ$ .

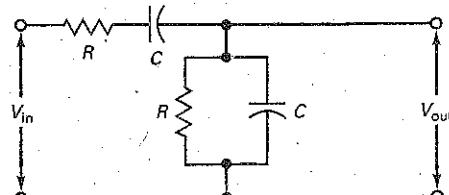
The lead-lag circuit of Fig. 23-4 acts like a resonant circuit. At the resonant frequency  $f_r$ , the feedback fraction  $B$  reaches a maximum value of  $\frac{1}{2}$ , and the phase angle equals  $0^\circ$ . Above and below the resonant frequency, the feedback fraction is less than  $\frac{1}{2}$ , and the phase angle no longer equals  $0^\circ$ .

## Formula for Resonant Frequency

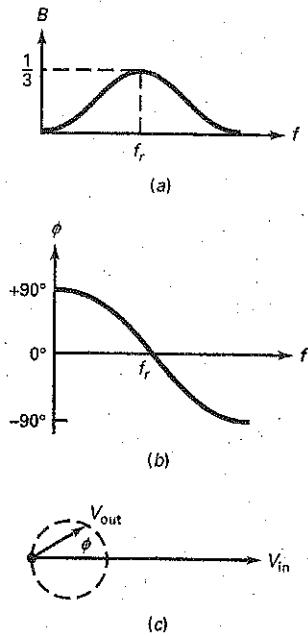
By analyzing Fig. 23-4 with complex numbers, we can derive these two equations:

$$B = \frac{1}{\sqrt{9 - (X_C/R - R/X_C)^2}} \quad (23-1)$$

**Figure 23-4** Lead-lag circuit.



**Figure 23-5** (a) Voltage gain; (b) phase response; (c) phasor diagram.



and

$$\phi = \arctan \frac{X_C/R - R/X_C}{3} \quad (23-2)$$

Graphing these equations produces Fig. 23-5a and b.

The feedback fraction given by Eq. (23-1) has a maximum value at the resonant frequency. At this frequency,  $X_C = R$ :

$$\frac{1}{2\pi f_r C} = R$$

Solving for  $f_r$  gives:

$$f_r = \frac{1}{2\pi RC} \quad (23-3)$$

### How It Works

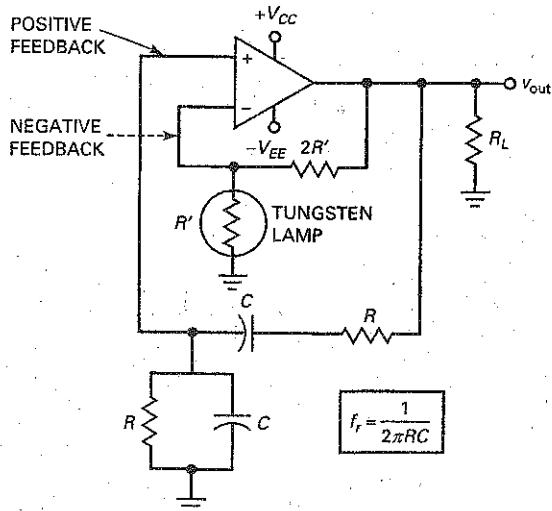
Figure 23-6a shows a Wien-bridge oscillator. It uses positive and negative feedback because there are two paths for feedback. There is a path for positive feedback from the output through the lead-lag circuit to the noninverting input. There is also a path for negative feedback from the output through the voltage divider to the inverting input.

When the circuit is initially turned on, there is more positive feedback than negative feedback. This allows the oscillations to build up, as previously described. After the output signal reaches a desired level, the negative feedback becomes large enough to reduce loop gain  $A_v B$  to 1.

Here is why  $A_v B$  decreases to 1: At power-up, the tungsten lamp has a low resistance, and the negative feedback is small. For this reason, the loop gain is greater than 1, and the oscillations can build up at the resonant frequency. As the oscillations build up, the tungsten lamp heats slightly and its resistance increases. In most circuits, the current through the lamp is not enough to make the lamp glow, but it is enough to increase the resistance.

At some high output level, the tungsten lamp has a resistance of exactly  $R'$ . At this point, the closed-loop voltage gain from the noninverting input to the

**Figure 23-6** Wien-bridge oscillator.



output decreases to:

$$A_{V(CL)} = \frac{2R'}{R'} + 1 = 3.$$

Since the lead-lag circuit has a  $B$  of  $\frac{1}{3}$ , the loop gain is:

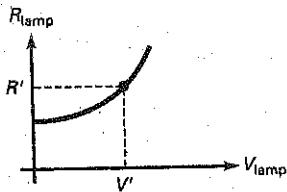
$$A_{V(CL)}B = 3(\frac{1}{3}) = 1$$

When the power is first turned on, the resistance of the tungsten lamp is less than  $R'$ . As a result, the closed-loop voltage gain from the noninverting input to the output is greater than 3 and  $A_{V(CL)}B$  is greater than 1.

As the oscillations build up, the peak-to-peak output becomes large enough to increase the resistance of the tungsten lamp. When its resistance equals  $R'$ , the loop gain  $A_{V(CL)}B$  is exactly equal to 1. At this point, the oscillations become stable, and the output voltage has a constant peak-to-peak value.

## Initial Conditions

**Figure 23-7** Resistance of tungsten lamp.



At power-up, the output voltage is zero and the resistance of the tungsten lamp is less than  $R'$ , as shown in Fig. 23-7. When the output voltage increases, the resistance of the lamp increases, as shown in the graph. When the voltage across the tungsten lamp is  $V'$ , the tungsten lamp has a resistance of  $R'$ . This means that  $A_{V(CL)}$  has a value of 3 and the loop gain is 1. When this happens, the output amplitude levels off and becomes constant.

## Notch Filter

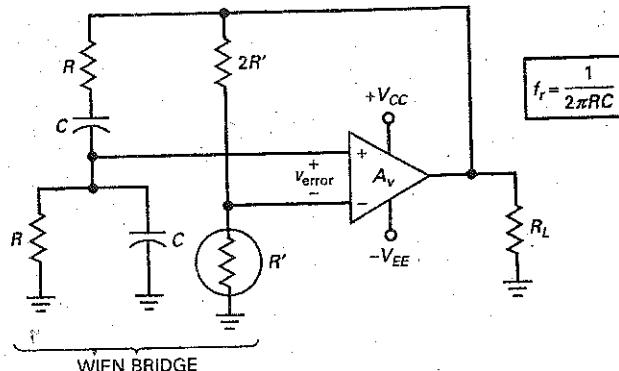
Figure 23-8 shows another way to draw the Wien-bridge oscillator. The lead-lag circuit is the left side of a bridge, and the voltage divider is the right side. This ac bridge, called a *Wien bridge*, is used in other applications besides oscillators. The *error voltage* is the output of the bridge. When the bridge approaches balance, the error voltage approaches zero.

The Wien bridge acts like a *notch filter*, a circuit with zero output at one particular frequency. For a Wien bridge, the notch frequency equals:

$$f_r = \frac{1}{2\pi RC} \quad (23-4)$$

Because the required error voltage for the op amp is so small, the Wien bridge is almost perfectly balanced, and the oscillation frequency equals  $f_r$  to a close approximation.

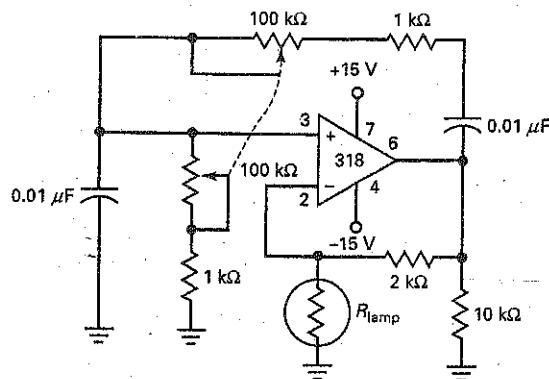
**Figure 23-8** Wien-bridge oscillator redrawn.



## Example 23-1

Calculate the minimum and maximum frequencies in Fig. 23-9. The two variable resistors are *ganged*, which means that they change together and have the same value for any wiper position.

Figure 23-9 Example.



**SOLUTION** With Eq. (23-4), the minimum frequency of oscillation is:

$$f_r = \frac{1}{2\pi(101 \text{ k}\Omega)(0.01 \mu\text{F})} = 158 \text{ Hz}$$

The maximum frequency of oscillation is:

$$f_r = \frac{1}{2\pi(1 \text{ k}\Omega)(0.01 \mu\text{F})} = 15.9 \text{ kHz}$$

**PRACTICE PROBLEM 23-1** Using Fig. 23-9, determine the variable resistor value for an output frequency of 1000 Hz.

## Example 23-2

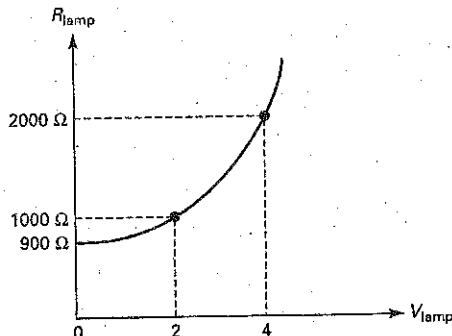
Figure 23-10 shows the lamp resistance of Fig. 23-9 versus lamp voltage. If the lamp voltage is expressed in rms volts, what is the output voltage of the oscillator?

**SOLUTION** In Fig. 23-9, the feedback resistance is 2 kΩ. Therefore, the oscillator output signal becomes constant when the lamp resistance equals 1 kΩ because this produces a closed-loop gain of 3.

In Fig. 23-10, a lamp resistance of 1 kΩ corresponds to a lamp voltage of 2 V rms. The lamp current is:

$$I_{\text{lamp}} = \frac{2 \text{ V}}{1 \text{ k}\Omega} = 2 \text{ mA}$$

**Figure 23-10** Example.



This 2 mA of current flows through the feedback resistance of 2 kΩ, which means that the output voltage of the oscillator is:

$$V_{\text{out}} = (2 \text{ mA})(1 \text{ k}\Omega + 2 \text{ k}\Omega) = 6 \text{ V rms}$$

**PRACTICE PROBLEM 23-2** Repeat Example 23-2 using a feedback resistance of 3 kΩ.

## 23-3 Other RC Oscillators

Although the Wien-bridge oscillator is the industry standard for frequencies up to 1 MHz, other RC oscillators can be used in different applications. This section discusses two other basic designs, called the **twin-T oscillator** and the **phase-shift oscillator**.

### Twin-T Filter

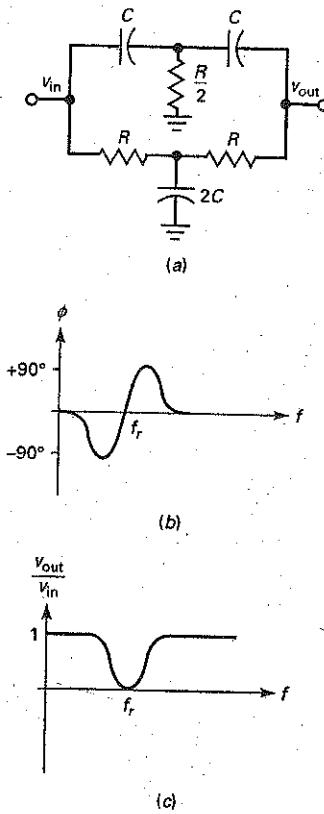
Figure 23-11a is a twin-T filter. A mathematical analysis of this circuit shows that it acts like a lead-lag circuit with a changing phase angle, as shown in Fig. 23-11b. Again, there is a frequency  $f_r$ , where the phase shift equals 0°. In Fig. 23-11c, the voltage gain equals 1 at low and high frequencies. In between, there is a frequency  $f_r$  at which the voltage gain drops to 0. The twin-T filter is another example of a notch filter because it can notch out frequencies near  $f_r$ . The equation for the resonant frequency of a twin-T filter is the same as for a Wien-bridge oscillator:

$$f_r = \frac{1}{2\pi RC}$$

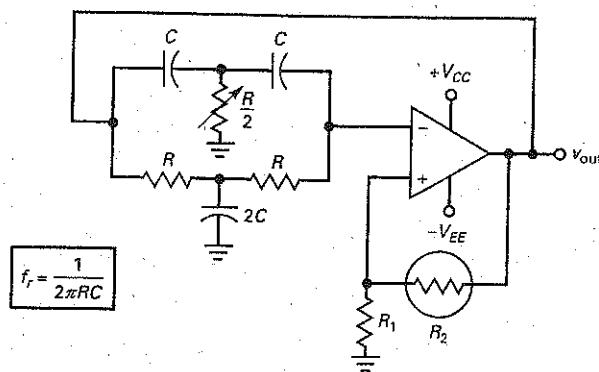
### Twin-T Oscillator

Figure 23-12 shows a twin-T oscillator. The positive feedback to the noninverting input is through a voltage divider. The negative feedback is through the twin-T filter. When power is first turned on, the lamp resistance  $R_2$  is low and the positive feedback is maximum. As the oscillations build up, the lamp resistance increases and the positive feedback decreases. As the feedback decreases, the oscillations level off and become constant. In this way, the lamp stabilizes the level of the output voltage.

**Figure 23-11** (a) Twin-T filter; (b) phase response; (c) frequency response.



**Figure 23-12** Twin-T oscillator.



In the twin-T filter, resistance \$R/2\$ is adjusted. This is necessary because the circuit oscillates at a frequency slightly different from the ideal resonant frequency. To ensure that the oscillation frequency is close to the notch frequency, the voltage divider should have \$R\_2\$ much larger than \$R\_1\$. As a guide, \$R\_2/R\_1\$ is in the range of 10 to 1000. This forces the oscillator to operate at a frequency near the notch frequency.

Although it is occasionally used, the twin-T oscillator is not a popular circuit because it works well only at one frequency. That is, unlike the Wien-bridge oscillator, it cannot be easily adjusted over a large frequency range.

### Phase-Shift Oscillator

Figure 23-13 is a phase-shift oscillator with three lead circuits in the feedback path. As you recall, a lead circuit produces a phase shift between \$0^\circ\$ and \$90^\circ\$, depending on the frequency. At some frequency, the total phase shift of the three lead circuits equals \$180^\circ\$ (approximately \$60^\circ\$ each). Some phase-shift oscillator configurations use four lead circuits to produce the required \$180^\circ\$ of phase shift. The amplifier has an additional \$180^\circ\$ of phase shift because the signal drives the inverting input. As a result, the phase shift around the loop will be \$360^\circ\$, equivalent to \$0^\circ\$. If \$A\_vB\$ is greater than 1 at this particular frequency, oscillations can start.

Figure 23-14 shows an alternative design. It uses three lag circuits. The operation is similar. The amplifier produces \$180^\circ\$ of phase shift, and the lag circuits contribute \$-180^\circ\$ at some higher frequency to get a loop phase shift of \$0^\circ\$. If \$A\_vB\$ is greater than 1 at this frequency, oscillations can start. The phase-shift oscillator is not a popular circuit. Again, the main problem with the circuit is that it cannot be easily adjusted over a large frequency range.

**Figure 23-13** Phase-shift oscillator with three lead circuits.

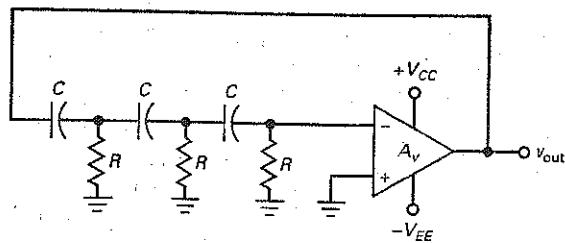
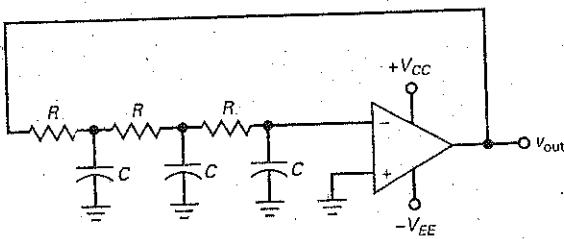


Figure 23-14 Phase-shift oscillator with three lag circuits.



## 23-4 The Colpitts Oscillator

Although it is superb at low frequencies, the Wien-bridge oscillator is not suited to high frequencies (well above 1 MHz). The main problem is the limited bandwidth ( $f_{unity}$ ) of the op amp.

### LC Oscillators

One way to produce high-frequency oscillations is with an *LC* oscillator, a circuit that can be used for frequencies between 1 and 500 MHz. This frequency range is beyond the  $f_{unity}$  of most op amps. This is why a bipolar junction transistor or an FET is typically used for the amplifier. With an amplifier and *LC* tank circuit, we can feed back a signal with the right amplitude and phase to sustain oscillations.

The analysis and the design of high-frequency oscillators are difficult. Why? Because at higher frequencies, stray capacitances and lead inductances become very important in determining the oscillation frequency, feedback fraction, output power, and other ac quantities. This is why many designers use computer approximations for an initial design and adjust the built-up oscillator as needed to get the desired performance.

### CE Connection

Figure 23-15 shows a **Colpitts oscillator**. The voltage-divider bias sets up a quiescent operating point. The RF choke has a very high inductive reactance, so it appears open to the ac signal. The circuit has a low-frequency voltage gain of  $r_c/r_e$ , where  $r_c$  is the ac collector resistance. Because the RF choke appears open to the ac signal, the ac collector resistance is primarily the ac resistance of the resonant tank circuit. This ac resistance has a maximum value at resonance.

Figure 23-15 Colpitts oscillator.

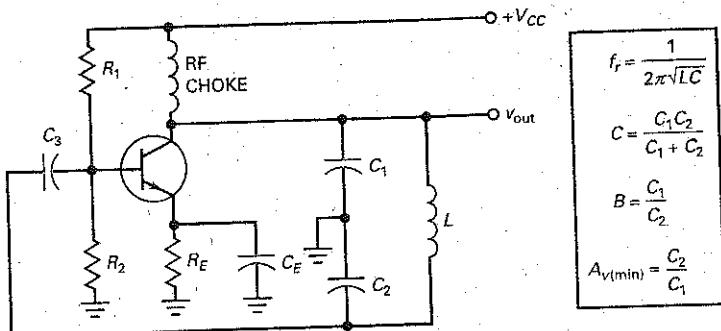
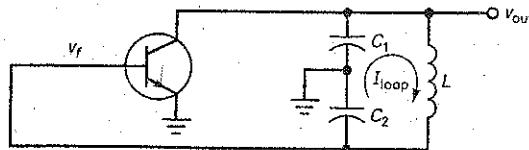


Figure 23-16 Equivalent circuit of Colpitts oscillator.



You will encounter many variations of the Colpitts oscillator. One way to recognize a Colpitts oscillator is by the capacitive voltage divider formed by  $C_1$  and  $C_2$ . It produces the feedback voltage necessary for oscillations. In other kinds of oscillators, the feedback voltage is produced by transformers, inductive voltage dividers, and so on.

### AC Equivalent Circuit

Figure 23-16 is a simplified ac equivalent circuit for the Colpitts oscillator. The circulating or loop current in the tank flows through  $C_1$  in series with  $C_2$ . Notice that  $v_{out}$  equals the ac voltage across  $C_1$ . Also, the feedback voltage  $v_f$  appears across  $C_2$ . This feedback voltage drives the base and sustains the oscillations developed across the tank circuit, provided there is enough voltage gain at the oscillation frequency. Since the emitter is at ac ground, the circuit is a CE connection.

### Resonant Frequency

Most  $LC$  oscillators use tank circuits with a  $Q$  greater than 10. Because of this, we can calculate the approximate resonant frequency as:

$$f_r = \frac{1}{2\pi\sqrt{LC}} \quad (23-5)$$

This is accurate to better than 1 percent when  $Q$  is greater than 10.

The capacitance to use in Eq. (23-5) is the equivalent capacitance through which the circulating current passes. In the Colpitts tank circuit of Fig. 23-16, the circulating current flows through  $C_1$  in series with  $C_2$ . Therefore, the equivalent capacitance is:

$$C = \frac{C_1 C_2}{C_1 + C_2} \quad (23-6)$$

For instance, if  $C_1$  and  $C_2$  are 100 pF each, you would use 50 pF in Eq. (23-5).

### Starting Condition

The required starting condition for any oscillator is  $A_v B > 1$  at the resonant frequency of the tank circuit. This is equivalent to  $A_v > 1/B$ . In Fig. 23-16, the output voltage appears across  $C_1$  and the feedback voltage appears across  $C_2$ . The feedback fraction in this type of oscillator is given by:

$$B = \frac{C_1}{C_2} \quad (23-7)$$

For the oscillator to start, the minimum voltage gain is:

$$A_{v(\min)} = \frac{C_2}{C_1} \quad (23-8)$$

What does  $A_v$  equal? This depends on the upper cutoff frequencies of the amplifier. There are base and collector bypass circuits in a bipolar amplifier. If the

### GOOD TO KNOW

In reference to Fig. 23-15, it is important to realize that the net reactance of the  $L-C_2$  branch appears inductive at the resonant frequency of the tank. Furthermore, the net inductive reactance of the  $L-C_2$  branch equals the capacitive reactance of  $C_1$ .

## GOOD TO KNOW

In Fig. 23-15, the current in the  $L-C_2$  branch lags the tank voltage by  $90^\circ$  at resonance, since the net reactance of this branch is inductive. Furthermore, since the voltage across  $C_2$  must lag its current by  $90^\circ$ , the feedback voltage must lag the tank voltage (ac collector voltage) by  $180^\circ$ . As you can see, the feedback network provides the required  $180^\circ$  phase shift of  $V_{out}$ .

cutoff frequencies of these bypass circuits are greater than the oscillation frequency,  $A_v$  is approximately equal to  $r_c/r_e'$ . If the cutoff frequencies are lower than the oscillation frequency, the voltage gain is less than  $r_c/r_e'$  and there is additional phase shift through the amplifier.

## Output Voltage

With light feedback (small  $B$ ),  $A_v$  is only slightly larger than  $1/B$ , and the operation is approximately class A. When you first turn on the power, the oscillations build up, and the signal swings over more and more of the ac load line. With this increased signal swing, the operation changes from small-signal to large-signal. When this happens, the voltage gain decreases slightly. With light feedback, the value of  $A_vB$  can decrease to 1 without excessive clipping.

With heavy feedback (large  $B$ ), the large feedback signal drives the base of Fig. 23-15 into saturation and cutoff. This charges capacitor  $C_3$ , producing negative dc clamping at the base. The negative clamping automatically adjusts the value of  $A_vB$  to 1. If the feedback is too heavy, you may lose some of the output voltage because of stray power losses.

When you build an oscillator, you can adjust the feedback to maximize the output voltage. The idea is to use enough feedback to start under all conditions (different transistors, temperature, voltage, and so on), but not so much that you lose output signal. Designing reliable high-frequency oscillators is a challenge. Most designers use computers to model high-frequency oscillators.

## Coupling to a Load

The exact frequency of oscillation depends on the  $Q$  of the circuit and is given by:

$$f_r = \frac{1}{2\pi \sqrt{LC}} \sqrt{\frac{Q^2}{Q^2 + 1}} \quad (23-9)$$

When  $Q$  is greater than 10, this equation simplifies to the ideal value given by Eq. (23-5). If  $Q$  is less than 10, the frequency is lower than the ideal value. Furthermore, a low  $Q$  may prevent the oscillator from starting because it may reduce the high-frequency voltage gain below the starting value of  $1/B$ .

Figure 23-17a shows one way to couple the oscillator signal to the load resistance. If the load resistance is large, it will load the resonant circuit only slightly and the  $Q$  will be greater than 10. But if the load resistance is small,  $Q$  drops under 10 and the oscillations may not start. One solution to a small load resistance is to use a small capacitance  $C_4$ , one whose  $X_C$  is large compared with the load resistance. This prevents excessive loading of the tank circuit.

Figure 23-17b shows link coupling, another way of coupling the signal to a small load resistance. Link coupling means using only a few turns on the secondary winding of an RF transformer. This light coupling ensures that the load resistance will not lower the  $Q$  of the tank circuit to the point at which the oscillator will not start.

Whether capacitive or link coupling is used, the loading effect is kept as small as possible. In this way, the high  $Q$  of the tank ensures an undistorted sinusoidal output with a reliable start for the oscillations.

## CB Connection

When the feedback signal in an oscillator drives the base, a large Miller capacitance appears across the input. This produces a relatively low cutoff frequency, which means that the voltage gain may be too low at the desired resonant frequency.

To get a higher cutoff frequency, the feedback signal can be applied to the emitter, as shown in Fig. 23-18. Capacitor  $C_3$  ac-grounds the base, and so the transistor acts like a common-base (CB) amplifier. A circuit like this can oscillate

Figure 23-17 (a) Capacitor coupling; (b) link coupling.

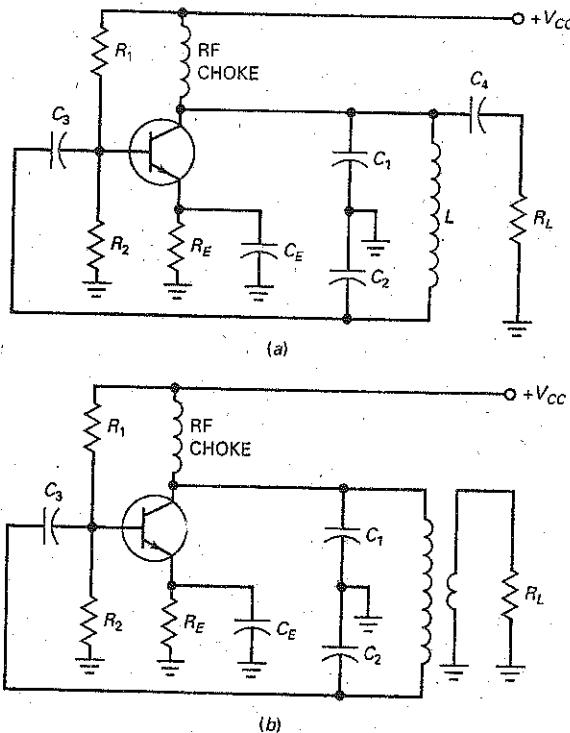
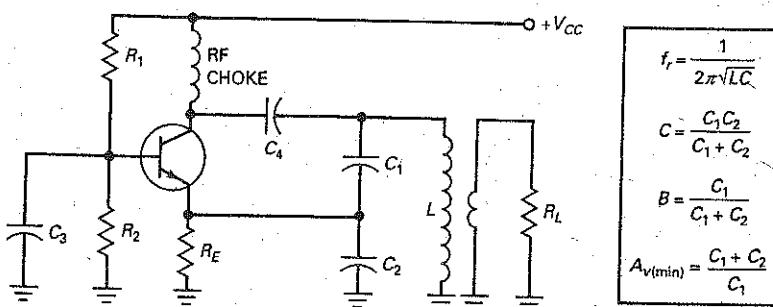


Figure 23-18 CB oscillator can oscillate at higher frequencies than CE oscillator.

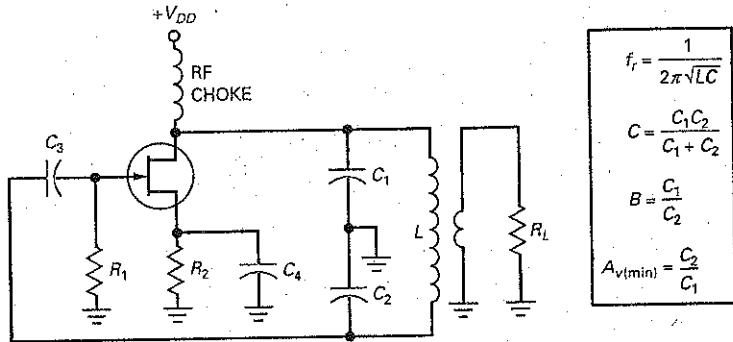


at higher frequencies because its high-frequency gain is larger than that of a CE oscillator. With link coupling on the output, the tank is lightly loaded, and the resonant frequency is given by Eq. (23-5).

The feedback fraction is slightly different in a CB oscillator. The output voltage appears across  $C_1$  and  $C_2$  in series, and the feedback voltage appears across  $C_2$ . Ideally, the feedback fraction is:

$$B = \frac{C_1}{C_1 + C_2} \quad (23-10)$$

**Figure 23-19** JFET oscillator has less loading effect on tank circuit.



For the oscillations to start,  $A_v$  must be greater than  $1/B$ . As an approximation, this means that:

$$A_{v(\min)} = \frac{C_1 + C_2}{C_1} \quad (23-11)$$

This is an approximation because it ignores the input impedance of the emitter, which is in parallel with  $C_2$ .

### FET Colpitts Oscillator

Figure 23-19 is an example of an FET Colpitts oscillator in which the feedback signal is applied to the gate. Since the gate has a high input resistance, the loading effect on the tank circuit is much less than with a bipolar junction transistor. The feedback fraction for the circuit is:

$$B = \frac{C_1}{C_2} \quad (23-12)$$

The minimum gain needed to start the FET oscillator is:

$$A_{v(\min)} = \frac{C_2}{C_1} \quad (23-13)$$

In an FET oscillator, the low-frequency voltage gain is  $g_m r_d$ . Above the cutoff frequency of the FET amplifier, the voltage gain decreases. In Eq. (23-13),  $A_{v(\min)}$  is the voltage gain at the oscillation frequency. As a rule, we try to keep the oscillation frequency lower than the cutoff frequency of the FET amplifier. Otherwise, the additional phase shift through the amplifier may prevent the oscillator from starting.

### Example 23-3

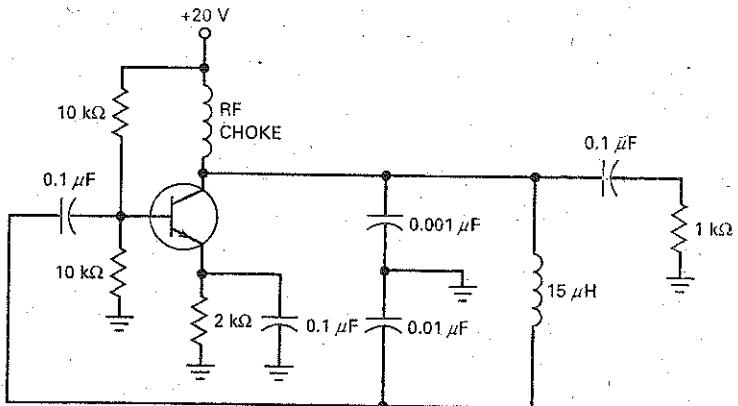
Multisim

What is the frequency of oscillation in Fig. 23-20? What is the feedback fraction? How much voltage gain does the circuit need to start oscillating?

**SOLUTION** This is a Colpitts oscillator using the CE connection of a transistor. With Eq. (23-6), the equivalent capacitance is:

$$C = \frac{(0.001 \mu\text{F})(0.01 \mu\text{F})}{0.001 \mu\text{F} + 0.01 \mu\text{F}} = 909 \text{ pF}$$

Figure 23-20 Example.



The inductance is  $15 \mu\text{H}$ . With Eq. (23-5), the frequency of oscillation is:

$$f_r = \frac{1}{2\pi \sqrt{(15 \mu\text{H})(909 \text{ pF})}} = 1.36 \text{ MHz}$$

With Eq. (23-7), the feedback fraction is:

$$B = \frac{0.001 \mu\text{F}}{0.01 \mu\text{F}} = 0.1$$

To start oscillating, the circuit needs a minimum voltage gain of:

$$A_{v(\min)} = \frac{0.01 \mu\text{F}}{0.001 \mu\text{F}} = 10$$

**PRACTICE PROBLEM 23-3** In Fig. 23-20, what is the approximate value that the  $15 \mu\text{H}$  would need to equal for an output frequency of 1 MHz?

## 23-5 Other LC Oscillators

The Colpitts oscillator is the most widely used *LC* oscillator. The capacitive voltage divider in the resonant circuit is a convenient way to develop the feedback voltage. But other kinds of oscillators can also be used.

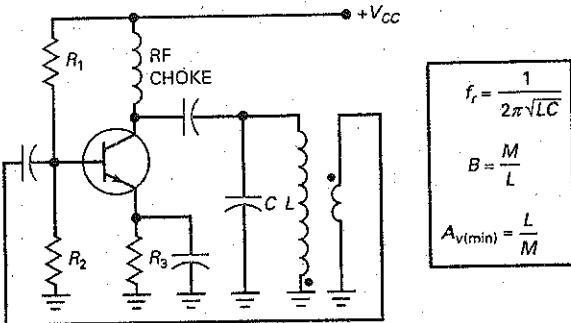
### Armstrong Oscillator

Figure 23-21 is an example of an **Armstrong oscillator**. In this circuit, the collector drives an *LC* resonant tank. The feedback signal is taken from a small secondary winding and fed back to the base. There is a phase shift of  $180^\circ$  in the transformer, which means that the phase shift around the loop is zero. If we ignore the loading effect of the base, the feedback fraction is:

$$B = \frac{M}{L} \quad (23-14)$$

where  $M$  is the mutual inductance and  $L$  is the primary inductance. For the Armstrong oscillator to start, the voltage gain must be greater than  $1/B$ .

Figure 23-21 Armstrong oscillator.



An Armstrong oscillator uses transformer coupling for the feedback signal. This is how you can recognize variations of this basic circuit. The small secondary winding is sometimes called a *tickler coil* because it feeds back the signal that sustains the oscillations. The resonant frequency is given by Eq. (23-5), using the  $L$  and  $C$  shown in Fig. 23-21. As a rule, you do not see the Armstrong oscillator used much because many designers avoid transformers whenever possible.

### Hartley Oscillator

Figure 23-22 is an example of the Hartley oscillator. When the  $LC$  tank is resonant, the circulating current flows through  $L_1$  in series with  $L_2$ . The equivalent  $L$  to use in Eq. (23-5) is:

$$L = L_1 + L_2 \quad (23-15)$$

In a Hartley oscillator, the feedback voltage is developed by the inductive voltage divider,  $L_1$  and  $L_2$ . Since the output voltage appears across  $L_1$  and the feedback voltage appears across  $L_2$ , the feedback fraction is:

$$B = \frac{L_2}{L_1} \quad (23-16)$$

As usual, this ignores the loading effects of the base. For oscillations to start, the voltage gain must be greater than  $1/B$ .

Often a Hartley oscillator uses a single tapped inductor instead of two separate inductors. Another variation sends the feedback signal to the emitter instead of to the base. Also, you may see an FET used instead of a bipolar junction transistor. The output signal can be either capacitively coupled or link-coupled.

Figure 23-22 Hartley oscillator.

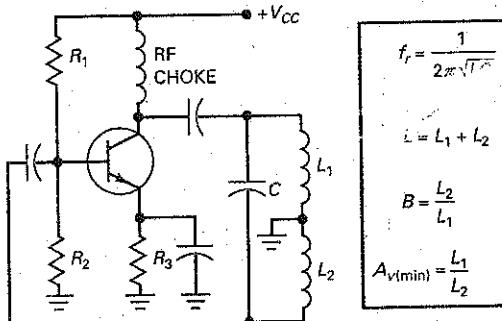
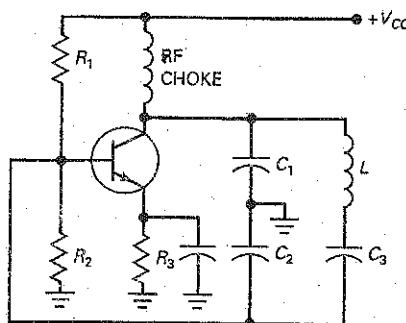


Figure 23-23 Clapp oscillator.



$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

$$C = \frac{1}{1/C_1 + 1/C_2 + 1/C_3}$$

$$B = \frac{C_1}{C_2}$$

$$A_{v(\min)} = \frac{C_2}{C_1}$$

### Clapp Oscillator

#### GOOD TO KNOW

In the Colpitts oscillator, the tank inductor is adjusted to vary the frequency of oscillation, whereas in the Hartley oscillator, the tank capacitor is adjusted to vary the frequency of oscillation.

The Clapp oscillator of Fig. 23-23 is a refinement of the Colpitts oscillator. The capacitive voltage divider produces the feedback signal as before. An additional capacitor  $C_3$  is in series with the inductor. Since the circulating tank current flows through  $C_1$ ,  $C_2$ , and  $C_3$  in series, the equivalent capacitance used to calculate the resonant frequency is:

$$C = \frac{1}{1/C_1 + 1/C_2 + 1/C_3} \quad (23-17)$$

In a Clapp oscillator,  $C_3$  is much smaller than  $C_1$  and  $C_2$ . As a result,  $C$  is approximately equal to  $C_3$ , and the resonant frequency is given by:

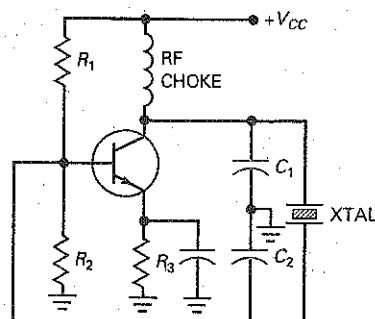
$$f_r \approx \frac{1}{2\pi\sqrt{LC_3}} \quad (23-18)$$

Why is this important? Because  $C_1$  and  $C_2$  are shunted by transistor and stray capacitances. These extra capacitances alter the values of  $C_1$  and  $C_2$  slightly. In a Colpitts oscillator, the resonant frequency therefore depends on the transistor and stray capacitances. But in a Clapp oscillator, the transistor and stray capacitances have no effect on  $C_3$ , so the oscillation frequency is more stable and accurate. This is why you occasionally see the Clapp oscillator used.

### Crystal Oscillator

When accuracy and stability of the oscillation frequency are important, a quartz-crystal oscillator is used. In Fig. 23-24, the feedback signal comes from a

Figure 23-24 Crystal oscillator.



capacitive tap. As will be discussed in the next section, the crystal (abbreviated XTAL) acts like a large inductor in series with a small capacitor (similar to the Clapp). Because of this, the resonant frequency is almost totally unaffected by transistor and stray capacitances.

### Example 23-4

III Multisim

If 50 pF is added in series with the 15- $\mu$ H inductor of Fig. 23-20, the circuit becomes a Clapp oscillator. What is the frequency of oscillation?

**SOLUTION** We can calculate the equivalent capacitance with Eq. (23-17):

$$C = \frac{1}{1/0.001 \text{ } \mu\text{F} + 1/0.01 \text{ } \mu\text{F} + 1/50 \text{ pF}} \cong 50 \text{ pF}$$

Notice how the term 1/50 pF swamps the other values because the 50 pF is much smaller than the other capacitances. The frequency of oscillation is:

$$f_r = \frac{1}{2\pi\sqrt{(15 \text{ } \mu\text{H})(50 \text{ pF})}} = 5.81 \text{ MHz}$$

**PRACTICE PROBLEM 23-4** Repeat Example 23-4 by replacing the 50 pF capacitor with a 120 pF.

## 23-6 Quartz Crystals

When the frequency of oscillation needs to be accurate and stable, a crystal oscillator is the natural choice. Electronic wristwatches and other critical timing applications use crystal oscillators because they provide an accurate clock frequency.

### Piezoelectric Effect

Some crystals found in nature exhibit the **piezoelectric effect**. When you apply an ac voltage across them, they vibrate at the frequency of the applied voltage. Conversely, if you mechanically force them to vibrate, they generate an ac voltage of the same frequency. The main substances that produce the piezoelectric effect are quartz, Rochelle salts, and tourmaline.

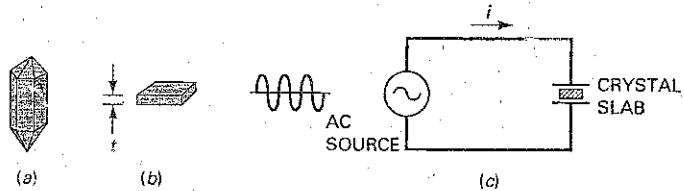
Rochelle salts have the greatest piezoelectric activity. For a given ac voltage, they vibrate more than quartz or tourmaline. Mechanically, they are the weakest because they break easily. Rochelle salts have been used to make microphones, phonograph pickups, headsets, and loudspeakers. Tourmaline shows the least piezoelectric activity but is the strongest of the three. It is also the most expensive. It is occasionally used at very high frequencies.

Quartz is a compromise between the piezoelectric activity of Rochelle salts and the strength of tourmaline. Because it is inexpensive and readily available in nature, quartz is widely used for RF oscillators and filters.

### Crystal Slab

The natural shape of a quartz crystal is a hexagonal prism with pyramids at the ends (see Fig. 23-25a). To get a usable crystal out of this, a manufacturer slices a

**Figure 23-25** (a) Natural quartz crystal; (b) slab; (c) input current is maximum at resonance.



rectangular slab out of the natural crystal. Figure 23-25b shows this slab with thickness  $t$ . The number of slabs we can get from a natural crystal depends on the size of the slabs and the angle of the cut.

For use in electronic circuits, the slab must be mounted between two metal plates, as shown in Fig. 23-25c. In this circuit the amount of crystal vibration depends on the frequency of the applied voltage. By changing the frequency, we can find resonant frequencies at which the crystal vibrations reach a maximum. Since the energy for the vibrations must be supplied by the ac source, the ac current is maximum at each resonant frequency.

### Fundamental Frequency and Overtones

Most of the time, the crystal is cut and mounted to vibrate best at one of its resonant frequencies, usually the **fundamental frequency**, or lowest frequency. Higher resonant frequencies, called *overtones*, are almost exact multiples of the fundamental frequency. As an example, a crystal with a fundamental frequency of 1 MHz has a first overtone of approximately 2 MHz, a second overtone of approximately 3 MHz, and so on.

The formula for the fundamental frequency of a crystal is:

$$f = \frac{K}{t} \quad (23-19)$$

where  $K$  is a constant and  $t$  is the thickness of the crystal. Since the fundamental frequency is inversely proportional to the thickness, there is a limit to the highest fundamental frequency. The thinner the crystal, the more fragile it becomes and the more likely it is to break when vibrating.

Quartz crystals work well up to 10 MHz on the fundamental frequency. To reach higher frequencies, we can use a crystal that vibrates on overtones. In this way, we can reach frequencies up to 100 MHz. Occasionally, the more expensive but stronger tourmaline is used at higher frequencies.

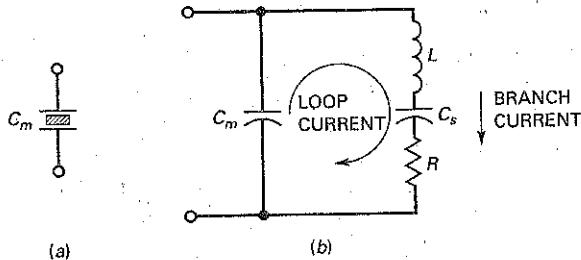
### AC Equivalent Circuit

What does the crystal look like to an ac source? When the crystal of Fig. 23-26a is not vibrating, it is equivalent to a capacitance  $C_m$  because it has two metal plates separated by a dielectric. The capacitance  $C_m$  is known as the **mounting capacitance**.

When a crystal is vibrating, it acts like a tuned circuit. Figure 23-26b shows the ac equivalent circuit of a crystal vibrating at its fundamental frequency. Typical values are  $L$  in henrys,  $C_s$  in fractions of a picofarad,  $R$  in hundreds of ohms, and  $C_m$  in picofarads. For instance, a crystal can have values such as  $L = 3 \text{ H}$ ,  $C_s = 0.05 \text{ pF}$ ,  $R = 2 \text{ k}\Omega$ , and  $C_m = 10 \text{ pF}$ .

Crystals have an incredibly high  $Q$ . For the values just given,  $Q$  is almost 4000. The  $Q$  of a crystal can easily be over 10,000. The extremely high  $Q$  of a

Figure 23-26 (a) Mounting capacitance; (b) ac equivalent circuit of vibrating crystal.



crystal means that crystal oscillators have a very stable frequency. We can understand why this is true when we examine Eq. (23-9), the exact equation for resonant frequency:

$$f_r = \frac{1}{2\pi\sqrt{LC}} \sqrt{\frac{Q^2}{Q^2 + 1}}$$

When  $Q$  approaches infinity, the resonant frequency approaches the ideal value determined by the values of  $L$  and  $C$ , which are precise in a crystal. By comparison, the  $L$  and  $C$  values of a Colpitts oscillator have large tolerances, which means that the frequency is less precise.

### Series and Parallel Resonance

The *series resonant frequency*  $f_s$  of a crystal is the resonant frequency of the  $LCR$  branch in Fig. 23-26b. At this frequency, the *branch current* reaches a maximum value because  $L$  resonates with  $C_s$ . The formula for this resonant frequency is:

$$f_s = \frac{1}{2\pi\sqrt{LC_s}} \quad (23-20)$$

The *parallel resonant frequency*  $f_p$  of the crystal is the frequency at which the circulating or loop current of Fig. 23-26b reaches a maximum value. Since this loop current must flow through the series combination of  $C_s$  and  $C_m$ , the equivalent parallel capacitance is:

$$C_p = \frac{C_m C_s}{C_m + C_s} \quad (23-21)$$

and the parallel resonant frequency is:

$$f_p = \frac{1}{2\pi\sqrt{LC_p}} \quad (23-22)$$

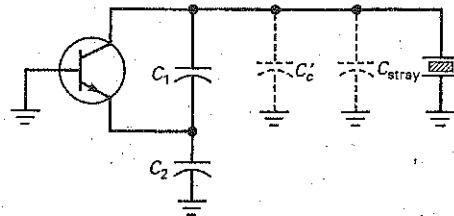
In any crystal,  $C_s$  is much smaller than  $C_m$ . Because of this,  $f_p$  is only slightly greater than  $f_s$ . When we use a crystal in an ac equivalent circuit like Fig. 23-27, the additional circuit capacitances appear in shunt with  $C_m$ . Because of this, the oscillation frequency will lie between  $f_s$  and  $f_p$ .

### Crystal Stability

The frequency of any oscillator tends to change slightly with time. This *drift* is produced by temperature, aging, and other causes. In a crystal oscillator, the frequency drift is very small, typically less than 1 part in  $10^6$  per day. Stability like this is important in electronic wristwatches because they use quartz-crystal oscillators as the basic timing device.

By putting a crystal oscillator in a temperature-controlled oven, we can get a frequency drift of less than 1 part in  $10^{10}$  per day. A clock with this drift will

**Figure 23-27** Stray capacitances are in parallel with mounting capacitance.



take 300 years to gain or lose 1 s. Stability like this is needed in frequency and time standards.

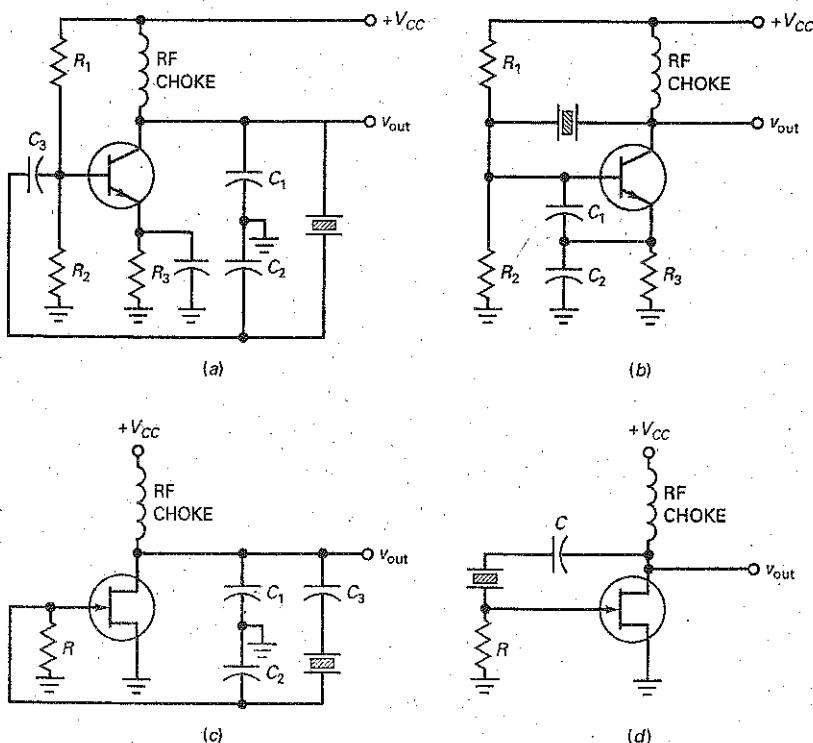
### Crystal Oscillators

Figure 23-28a shows a Colpitts crystal oscillator. The capacitive voltage divider produces the feedback voltage for the base of the transistor. The crystal acts like an inductor that resonates with  $C_1$  and  $C_2$ . The oscillation frequency is between the series and parallel resonant frequencies of the crystal.

Figure 23-28b is a variation of the Colpitts crystal oscillator. The feedback signal is applied to the emitter instead of the base. This variation allows the circuit to work at higher resonant frequencies.

Figure 23-28c is an FET Clapp oscillator. The intention is to improve the frequency stability by reducing the effect of stray capacitances. Figure 23-28d is a circuit called a Pierce crystal oscillator. Its main advantage is simplicity.

**Figure 23-28** Crystal oscillators: (a) Colpitts; (b) variation of Colpitts; (c) Clapp; (d) Pierce.



## Example 23-5

A crystal has these values:  $L = 3 \text{ H}$ ,  $C_s = 0.05 \text{ pF}$ ,  $R = 2 \text{ k}\Omega$ , and  $C_m = 10 \text{ pF}$ . What are the series and parallel resonant frequencies of the crystal?

**SOLUTION** Equation (23-20) gives the series resonant frequency:

$$f_s = \frac{1}{2\pi \sqrt{(3H)(0.05\text{pF})}} = 411 \text{ kHz}$$

Equation (23-21) gives the equivalent parallel capacitance:

$$C_p = \frac{(10 \text{ pF})(0.05 \text{ pF})}{10 \text{ pF} + 0.05 \text{ pF}} = 0.0498 \text{ pF}$$

Equation (23-22) gives the parallel resonant frequency:

$$f_p = \frac{1}{2\pi \sqrt{(3H)(0.0498 \text{ pF})}} = 412 \text{ kHz}$$

As we can see, the series and parallel resonant frequencies of the crystal are very close in value. If this crystal is used in an oscillator, the frequency of oscillation will be between 411 and 412 kHz.

**PRACTICE PROBLEM 23-5** Repeat Example 23-5 with  $C_s = 0.1 \text{ pF}$  and  $C_m = 15 \text{ pF}$ .

Summary Table 23-1 presents some of the characteristics of *RC* and *LC* oscillators.

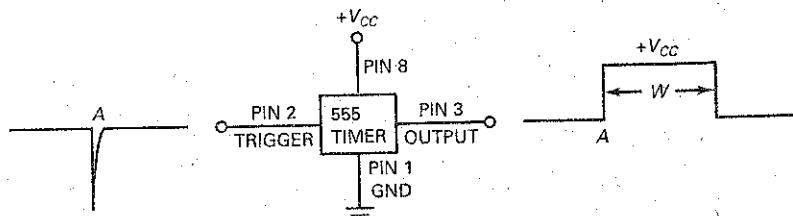
## 23-7 The 555 Timer

The NE555 (also LM555, CA555, and MC1455) is a widely used *IC timer*, a circuit that can run in either of two modes: **monostable** (one stable state) or **astable** (no stable states). In the monostable mode, it can produce accurate time delays from microseconds to hours. In the astable mode, it can produce rectangular waves with a variable duty cycle.

### Monostable Operation

Figure 23-29 illustrates monostable operation. Initially, the 555 timer has a low output voltage at which it can remain indefinitely. When the 555 timer receives a

Figure 23-29 The 555 timer used in monostable (one-shot) mode.



**Summary Table 23-1****Oscillators**

Type	Characteristics
<b>RC oscillators</b>	
Wien-bridge	<ul style="list-style-type: none"> <li>• Uses lead-lag feedback circuits</li> <li>• Needs ganged Rs for tuning</li> <li>• Low distortion output from 5 Hz to 1 MHz (limited bandwidth)</li> <li>• <math>f_r = \frac{1}{2\pi RC}</math></li> </ul>
Twin-T	<ul style="list-style-type: none"> <li>• Uses a notch filter circuit</li> <li>• Works well at one frequency</li> <li>• Difficult to adjust over a wide output frequency</li> <li>• <math>f_r = \frac{1}{2\pi RC}</math></li> </ul>
Phase-shift	<ul style="list-style-type: none"> <li>• Uses 3-4 lead or lag circuits</li> <li>• Cannot be adjusted over wide frequency range</li> </ul>
<b>LC oscillators</b>	
Colpitts	<ul style="list-style-type: none"> <li>• Uses a pair of tapped capacitors</li> <li>• <math>C = \frac{C_1 C_2}{C_1 + C_2}</math></li> <li>• <math>f_r = \frac{1}{2\pi \sqrt{LC}}</math></li> <li>• Widely used</li> </ul>
Armstrong	<ul style="list-style-type: none"> <li>• Uses a transformer for feedback</li> <li>• Not used frequently</li> <li>• <math>f_r = \frac{1}{2\pi \sqrt{LC}}</math></li> </ul>
Hartley	<ul style="list-style-type: none"> <li>• Uses a pair of tapped inductors</li> <li>• <math>L = L_1 + L_2</math></li> <li>• <math>f_r = \frac{1}{2\pi \sqrt{LC}}</math></li> </ul>
Clapp	<ul style="list-style-type: none"> <li>• Uses tapped capacitors and a capacitor in series with the inductor</li> <li>• Stable and accurate output</li> <li>• <math>C = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}}</math></li> <li>• <math>f_r = \frac{1}{2\pi \sqrt{LC}}</math></li> </ul>
Crystal	<ul style="list-style-type: none"> <li>• Uses a quartz crystal</li> <li>• Very accurate and stable</li> <li>• <math>f_p = \frac{1}{2\pi \sqrt{LC_p}}</math></li> <li>• <math>f_s = \frac{1}{2\pi \sqrt{LC_s}}</math></li> </ul>

*trigger* at point A in time, the output voltage switches from low to high, as shown. The output remains high for a while and then returns to the low state after a time delay of  $W$ . The output will remain in the low state until another trigger arrives.

A **multivibrator** is a two-state circuit that has zero, one, or two stable output states. When the 555 timer is used in the monostable mode, it is sometimes called a *monostable multivibrator* because it has only one stable state. It is stable in the low state until it receives a trigger, which causes the output to temporarily change to the high state. The high state, however, is not stable because the output returns to the low state when the pulse ends.

When operating in the monostable mode, the 555 timer is often referred to as a *one-shot multivibrator* because it produces only one output pulse for each input trigger. The duration of this output pulse can be precisely controlled with an external resistor and capacitor.

The 555 timer is an 8-pin IC. Figure 23-29 shows four of the pins. Pin 1 is connected to ground, and pin 8 is connected to the positive supply voltage. The 555 timer will work with any supply voltage between +4.5 and +18 V. The trigger goes into pin 2, and the output comes from pin 3. The other pins, which are not shown here, are connected to external components that determine the pulse width of the output.

### Astable Operation

The 555 timer can also be connected to run as an *astable multivibrator*. When used in this way, the 555 timer has no stable states, which means that it cannot remain indefinitely in either state. Stated another way, it oscillates when operated in the astable mode and it produces a rectangular output signal.

Figure 23-30 shows the 555 timer used in the astable mode. As we can see, the output is a series of rectangular pulses. Since no input trigger is needed to get an output, the 555 timer operating in the astable mode is sometimes called a *free-running multivibrator*.

### Functional Block Diagram

The schematic diagram of a 555 timer is complicated because it has about two dozen components connected as diodes, current mirrors, and transistors. Figure 23-31 shows a functional diagram of the 555 timer. This diagram captures all the key ideas we need for our discussion of the 555 timer.

As shown in Fig. 23-31, the 555 timer contains a voltage divider, two comparators, an *RS* flip-flop, and an *n-p-n* transistor. Since the voltage divider has equal resistors, the top comparator has a trip point of:

$$UTP = \frac{2V_{CC}}{3} \quad (23-23)$$

The lower comparator has a trip point of:

$$LTP = \frac{V_{CC}}{3} \quad (23-24)$$

Figure 23-30 The 555 timer used in astable (free-running) mode.

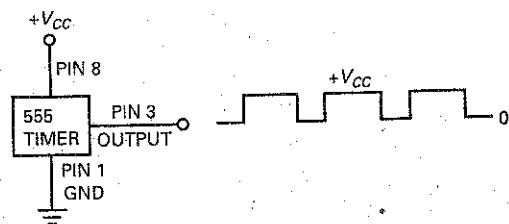
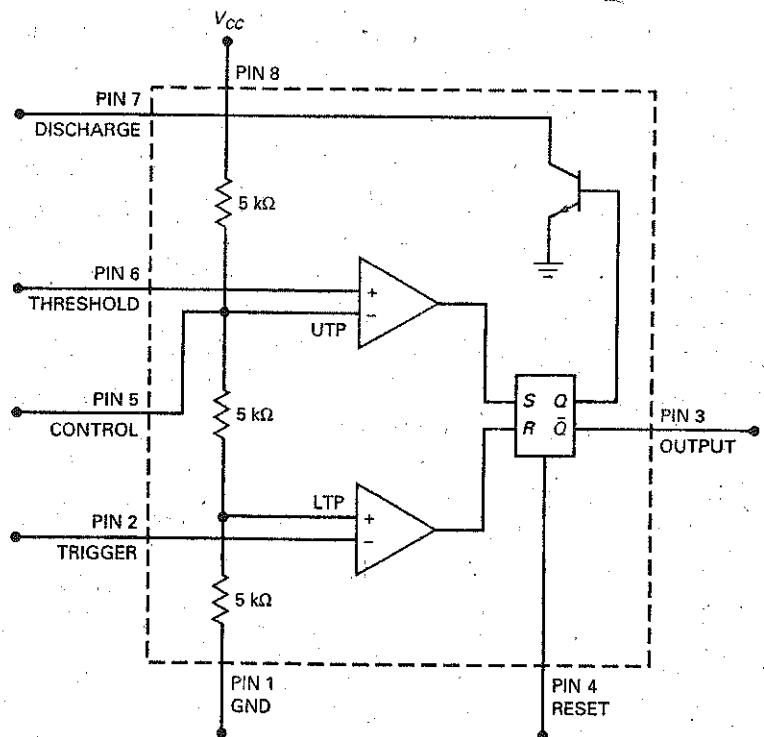


Figure 23-31 Simplified functional block diagram of a 555 timer.



In Fig. 23-31, pin 6 is connected to the upper comparator. The voltage on pin 6 is called the *threshold*. This voltage comes from external components not shown. When the *threshold voltage* is greater than the UTP, the upper comparator has a high output.

Pin 2 is connected to the lower comparator. The voltage on pin 2 is called the *trigger*. This is the trigger voltage that is used for the monostable operation of the 555 timer. When the timer is inactive, the trigger voltage is high. When the trigger voltage falls to less than the LTP, the lower comparator produces a high output.

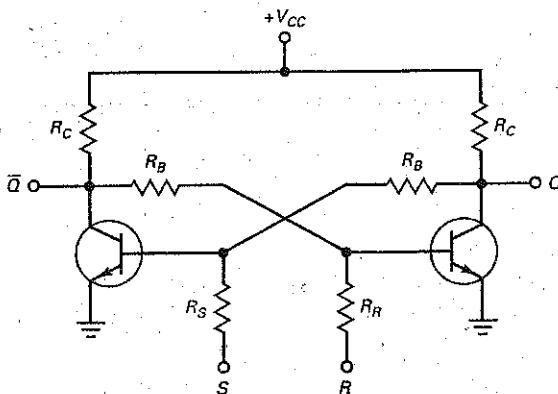
Pin 4 may be used to reset the output voltage to zero. Pin 5 may be used to control the output frequency when the 555 timer is used in the astable mode. In many applications, these two pins are made inactive as follows: Pin 4 is connected to  $+V_{CC}$ , and pin 5 is bypassed to ground through a capacitor. Later, we will discuss how pins 4 and 5 are used in some advanced circuits.

### RS Flip-Flop

Before we can understand how a 555 timer works with external components, we need to discuss the action of the block that contains,  $S$ ,  $R$ ,  $Q$ , and  $\bar{Q}$ . This block is called an *RS flip-flop*, a circuit that has two stable states.

Figure 23-32 shows one way to build an *RS flip-flop*. In a circuit like this, one of the transistors is saturated, and the other is cut off. For instance, if the right transistor is saturated, its collector voltage will be approximately zero. This means that there is no base current in the left transistor. As a result, the left transistor is cut off, producing a high collector voltage. This high collector voltage produces a large base current that keeps the right transistor in saturation.

Figure 23-32 RS flip-flop built with transistors.



The *RS* flip-flop has two outputs,  $Q$  and  $\bar{Q}$ . These are two-state outputs, either low or high voltages. Furthermore, the two outputs are always in opposite states. When  $Q$  is low,  $\bar{Q}$  is high. When  $Q$  is high,  $\bar{Q}$  is low. For this reason,  $\bar{Q}$  is called the *complement* of  $Q$ . The overbar on  $\bar{Q}$  is used to indicate that it is the complement of  $Q$ .

We can control the output states with the  $S$  and  $R$  inputs. If we apply a large positive voltage to the  $S$  input, we can drive the left transistor into saturation. This will cut off the right transistor. In this case,  $Q$  will be high and  $\bar{Q}$  will be low. The high  $S$  input can then be removed, because the saturated left transistor will keep the right transistor in cutoff.

Similarly, we can apply a large positive voltage to the  $R$  input. This will saturate the right transistor and cut off the left transistor. For this condition,  $Q$  is low and  $\bar{Q}$  is high. After this transition has occurred, the high  $R$  input can be removed because it is no longer needed.

Since the circuit is stable in either of two states, it is sometimes called a **bistable multivibrator**. A bistable multivibrator latches in either of two states. A high  $S$  input forces  $Q$  into the high state, and a high  $R$  input forces  $Q$  to return to the low state. The output  $Q$  remains in a given state until it is triggered into the opposite state.

Incidentally, the  $S$  input is sometimes called the *set input* because it sets the  $Q$  output to high. The  $R$  input is called the *reset input* because it resets the  $Q$  output to low.

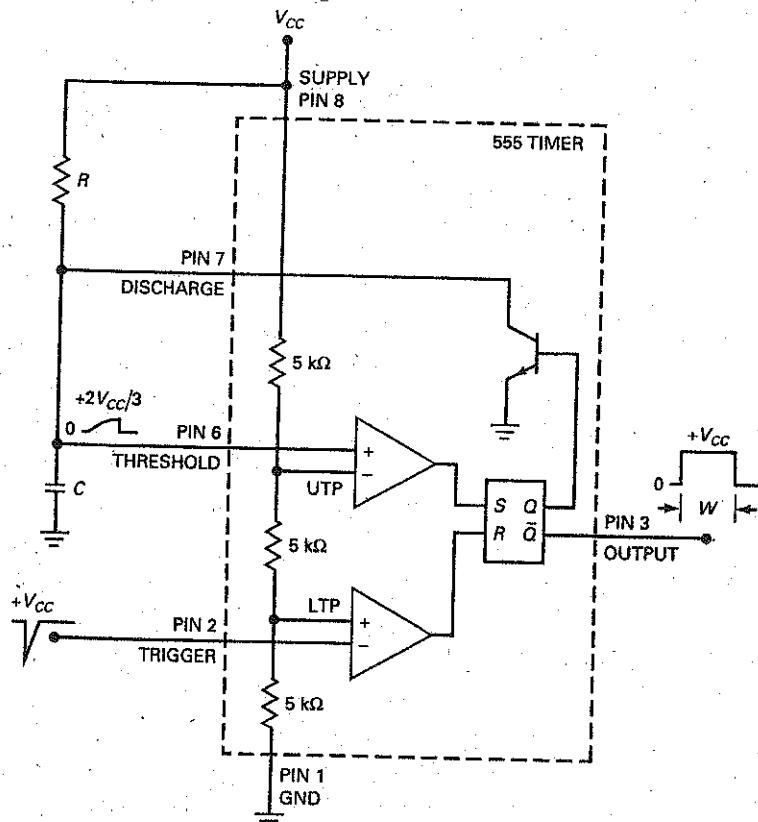
## Monostable Operation

Figure 23-33 shows the 555 timer connected for monostable operation. The circuit has an external resistor  $R$  and a capacitor  $C$ . The voltage across the capacitor is used for the threshold voltage to pin 6. When the trigger arrives at pin 2, the circuit produces a rectangular output pulse from pin 3.

Here is the theory of operation. Initially, the  $Q$  output of the *RS* flip-flop is high. This saturates the transistor and clamps the capacitor voltage at ground. The circuit will remain in this state until a trigger arrives. Because of the voltage divider, the trip points are the same as previously discussed: UTP =  $2V_{CC}/3$  and LTP =  $V_{CC}/3$ .

When the trigger input falls to slightly less than  $V_{CC}/3$ , the lower comparator resets the flip-flop. Since  $Q$  has changed to low, the transistor goes into cutoff, allowing the capacitor to charge. At this time,  $\bar{Q}$  has changed to high. The

**Figure 23-33** 555 timer connected for monostable operation.



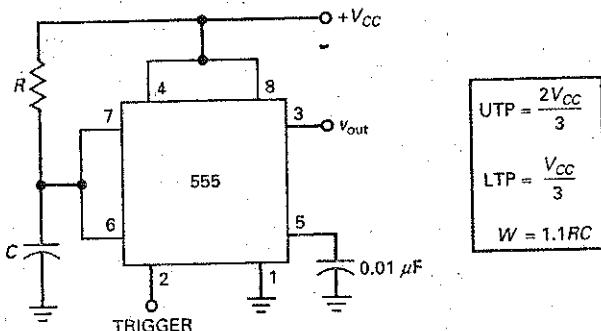
capacitor now charges exponentially as shown. When the capacitor voltage is slightly greater than  $2V_{CC}/3$ , the upper comparator sets the flip-flop. The high  $Q$  turns on the transistor, which discharges the capacitor almost instantly. At the same instant,  $\bar{Q}$  returns to the low state and the output pulse ends.  $\bar{Q}$  remains low until another input trigger arrives.

The complementary output  $\bar{Q}$  comes out of pin 3. The width of the rectangular pulse depends on how long it takes to charge the capacitor through resistance  $R$ . The longer the time constant, the longer it takes for the capacitor voltage to reach  $2V_{CC}/3$ . In one time constant, the capacitor can charge to 63.2 percent of  $V_{CC}$ . Since  $2V_{CC}/3$  is equivalent to 66.7 percent of  $V_{CC}$ , it takes slightly more than one time constant for the capacitor voltage to reach  $2V_{CC}/3$ . By solving the exponential charging equation, it is possible to derive this formula for the pulse width:

$$W = 1.1RC \quad (23-25)$$

Figure 23-34 shows the schematic diagram for the monostable 555 circuit as it usually appears. Only the pins and external components are shown. Notice that pin 4 (reset) is connected to  $+V_{CC}$ . As discussed earlier, this prevents pin 4 from having any effect on the circuit. In some applications, pin 4 may be temporarily grounded to suspend the operation. When pin 4 is taken high, the operation resumes. A later discussion will describe this type of reset in more detail.

Figure 23-34 Monostable timer circuit.



Pin 5 (control) is a special input that can be used to change the UTP, which changes the width of the pulse. Later, we will discuss *pulse-width modulation*, in which an external voltage is applied to pin 5 to change the pulse width. For now, we will bypass pin 5 to ground as shown. By ac-grounding pin 5, we prevent stray electromagnetic noise from interfering with the operation of the 555 timer.

In summary, the monostable 555 timer produces a single pulse whose width is determined by the external  $R$  and  $C$  used in Fig. 23-34. The pulse begins with the leading edge of the input trigger. A one-shot operation like this has a number of applications in digital and switching circuits.

### Example 23-6

Multisim

In Fig. 23-34,  $V_{CC} = 12$  V,  $R = 33$  kΩ, and  $C = 0.47$  μF. What is the minimum trigger voltage that produces an output pulse? What is the maximum capacitor voltage? What is the width of the output pulse?

**SOLUTION** As shown in Fig. 23-33, the lower comparator has a trip point of LTP. Therefore, the input trigger on pin 2 has to fall from  $+V_{CC}$  to slightly less than LTP. With the equations shown in Fig. 23-34:

$$LTP = \frac{12\text{ V}}{3} = 4\text{ V}$$

After a trigger arrives, the capacitor charges from 0 V to a maximum of UTP, which is:

$$UTP = \frac{2(12\text{ V})}{3} = 8\text{ V}$$

The pulse width of the one-shot output is:

$$W = 1.1(33\text{ k}\Omega)(0.47\text{ }\mu\text{F}) = 17.1\text{ ms}$$

This means that the falling edge of the output pulse occurs 17.1 ms after the trigger arrives. You can think of this 17.1 ms as a time delay, because the falling edge of the output pulse can be used to trigger some other circuit.

**PRACTICE PROBLEM 23-6** Using Fig. 23-34, change  $V_{CC}$  to 15 V,  $R$  to 100 kΩ, and repeat Example 23-6.

## Example 23-7

What is the pulse width in Fig. 23-34 if  $R = 10 \text{ M}\Omega$  and  $C = 470 \mu\text{F}$ ?

### SOLUTION

$$W = 1.1(10 \text{ M}\Omega)(470 \mu\text{F}) = 5170 \text{ s} = 86.2 \text{ min} = 1.44 \text{ hr}$$

Here we have a pulse width of more than an hour. The falling edge of the pulse occurs after a time delay of 1.44 hr.

## 23-8 Astable Operation of the 555 Timer

Generating time delays from microseconds to hours is useful in many applications. The 555 timer can also be used as an astable or free-running multivibrator. In this mode, it requires two external resistors and one capacitor to set the frequency of oscillations.

### Astable Operation

Figure 23-35 shows the 555 timer connected for astable operation. The trip points are the same as for monostable operation:

$$\text{UTP} = \frac{2V_{CC}}{3}$$

$$\text{LTP} = \frac{V_{CC}}{3}$$

When  $Q$  is low, the transistor is cut off and the capacitor is charging through a total resistance of:

$$R = R_1 + R_2$$

Because of this, the charging time constant is  $(R_1 + R_2)C$ . As the capacitor charges, the threshold voltage (pin 6) increases.

Eventually, the threshold voltage exceeds  $+2V_{CC}/3$ . Then, the upper comparator sets the flip-flop. With  $Q$  high, the transistor saturates and grounds pin 7. The capacitor now discharges through  $R_2$ . Therefore, the discharging time constant is  $R_2C$ . When the capacitor voltage drops to slightly less than  $V_{CC}/3$ , the lower comparator resets the flip-flop.

Figure 23-36 shows the waveforms. The timing capacitor has exponentially rising and falling voltages between UTP and LTP. The output is a rectangular wave that swings between 0 and  $V_{CC}$ . Since the charging time constant is longer than the discharging time constant, the output is nonsymmetrical. Depending on resistances  $R_1$  and  $R_2$ , the duty cycle is between 50 and 100 percent.

By analyzing the equations for charging and discharging, we can derive the following formulas. The pulse width is given by:

$$W = 0.693(R_1 + R_2)C \quad (23-26)$$

Figure 23-35 555 timer connected for astable operation.

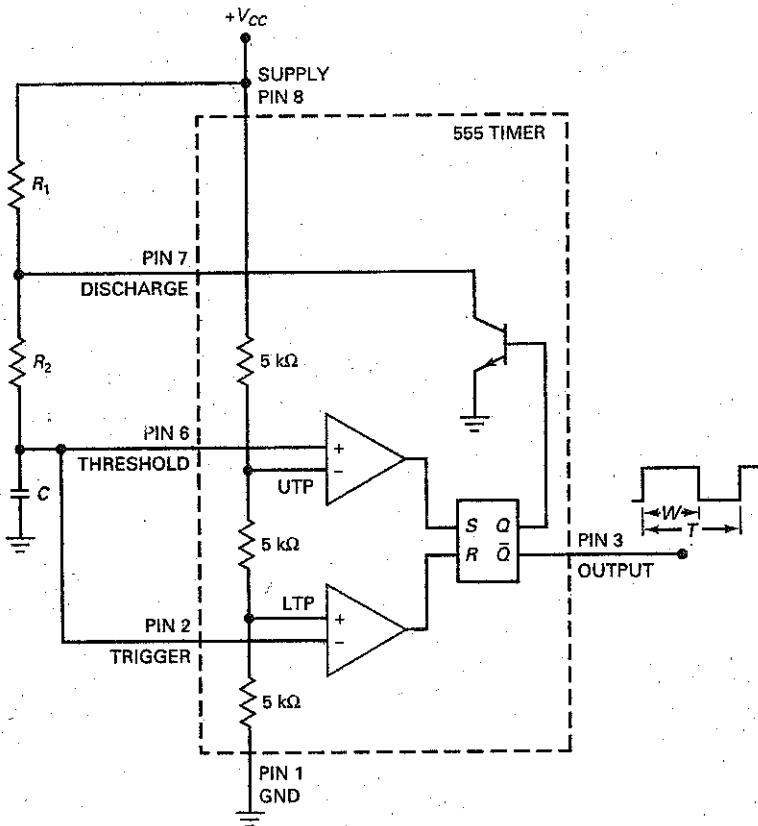
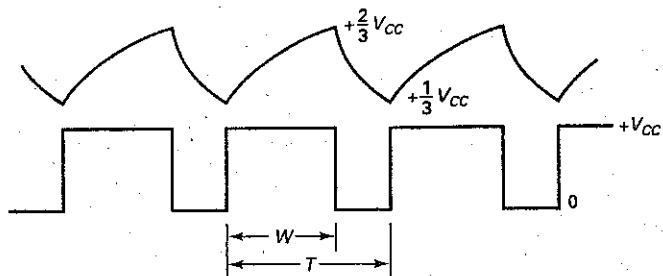


Figure 23-36 Capacitor and output waveforms for astable operation.



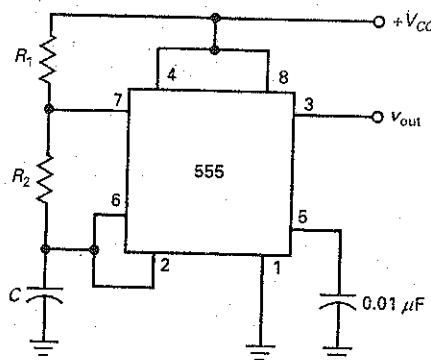
The period of the output equals:

$$T = 0.693(R_1 + 2R_2)C \quad (23-27)$$

The reciprocal of the period is the frequency:

$$f = \frac{1.44}{(R_1 + 2R_2)C} \quad (23-28)$$

Figure 23-37 Astable multivibrator.



$$W = 0.693(R_1 + R_2)C$$

$$T = 0.693(R_1 + 2R_2)C$$

$$f = \frac{1.44}{(R_1 + 2R_2)C}$$

$$D = \frac{R_1 + R_2}{R_1 + 2R_2}$$

Dividing the pulse width by the period gives the duty cycle:

$$D = \frac{R_1 + R_2}{R_1 + 2R_2} \quad (23-29)$$

When  $R_1$  is much smaller than  $R_2$ , the duty cycle approaches 50 percent. Conversely, when  $R_1$  is much greater than  $R_2$ , the duty cycle approaches 100 percent.

Figure 23-37 shows the astable 555 timer as it usually appears on a schematic diagram. Again notice how pin 4 (reset) is tied to the supply voltage and how pin 5 (control) is bypassed to ground through a  $0.01\text{-}\mu\text{F}$  capacitor.

The circuit of Fig. 23-37 can be modified to enable the duty cycle to become less than 50 percent. By placing a diode in parallel with  $R_2$  (anode connected to pin 7), the capacitor will effectively charge through  $R_1$  and the diode. The capacitor will discharge through  $R_2$ . Therefore, the duty cycle becomes:

$$D = \frac{R_1}{R_1 + R_2} \quad (23-30)$$

## VCO Operation

Figure 23-38a shows a **voltage-controlled oscillator** (VCO), another application for a 555 timer. The circuit is sometimes called a **voltage-to-frequency converter** because an input voltage can change the output frequency.

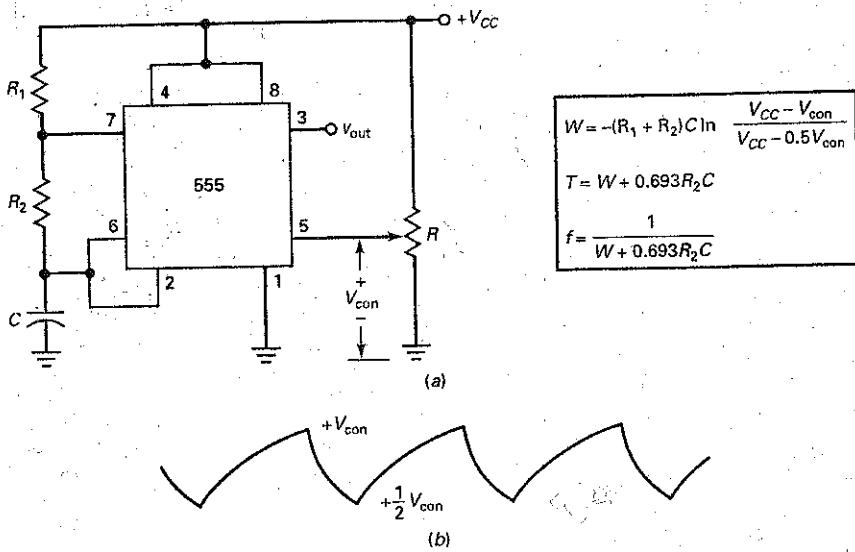
Here is how the circuit works: Recall that pin 5 connects to the inverting input of the upper comparator (Fig. 23-31). Normally, pin 5 is bypassed to ground through a capacitor, so that UTP equals  $+2V_{CC}/3$ . In Fig. 23-38a, however, the voltage from a stiff potentiometer overrides the internal voltage. In other words, UTP equals  $V_{con}$ . By adjusting the potentiometer, we can change UTP to a value between 0 and  $V_{CC}$ .

Figure 23-38b shows the voltage waveform across the timing capacitor. Notice that the waveform has a minimum value of  $+V_{con}/2$  and a maximum value of  $+V_{con}$ . If we increase  $V_{con}$ , it takes the capacitor longer to charge and discharge. Therefore, the frequency decreases. As a result, we can change the frequency of the circuit by varying the control voltage. Incidentally, the control voltage may come from a potentiometer, as shown, or it may be the output of a transistor circuit, an op amp, or some other device.

By analyzing the exponential charging and discharging of the capacitor, we can derive these equations:

$$W = -(R_1 + R_2)C \ln \frac{V_{CC} - V_{con}}{V_{CC} - 0.5V_{con}} \quad (23-31)$$

**Figure 23-38** (a) Voltage-controlled oscillator; (b) capacitor voltage waveform.



$$W = -(R_1 + R_2)C \ln \frac{V_{CC} - V_{con}}{V_{CC} - 0.5V_{con}}$$

$$T = W + 0.693R_2C$$

$$f = \frac{1}{W + 0.693R_2C}$$

To use this equation, you need to take the **natural logarithm**, which is the logarithm to the base  $e$ . If you have a scientific calculator, look for the  $\ln$  key. The period is given by:

$$T = W + 0.693R_2C \quad (23-32)$$

The frequency is given by:

$$f = \frac{1}{W + 0.693R_2C} \quad (23-33)$$

### Example 23-8

||| Multisim

The 555 timer of Fig. 23-37 has  $R_1 = 75 \text{ k}\Omega$ ,  $R_2 = 30 \text{ k}\Omega$ , and  $C = 47 \text{ nF}$ . What is frequency of the output signal? What is the duty cycle?

**SOLUTION** With the equations shown in Fig. 23-37:

$$f = \frac{1.44}{(75 \text{ k}\Omega + 60 \text{ k}\Omega)(47 \text{ nF})} = 227 \text{ Hz}$$

$$D = \frac{75 \text{ k}\Omega + 30 \text{ k}\Omega}{75 \text{ k}\Omega + 60 \text{ k}\Omega} = 0.778$$

This is equivalent to 77.8 percent.

**PRACTICE PROBLEM 23-8** Repeat Example 23-8 with both  $R_1$  and  $R_2 = 75 \text{ k}\Omega$ .

## Example 23-9

The VCO of Fig. 23-38a has the same  $R_1$ ,  $R_2$ , and  $C$  as in Example 23-8. What are the frequency and duty cycle when  $V_{con}$  is 11 V? What are the frequency and duty cycle when  $V_{con}$  is 1 V?

**SOLUTION** Using the equations of Fig. 23-38:

$$W = -(75 \text{ k}\Omega + 30 \text{ k}\Omega)(47 \text{ nF}) \ln \frac{12 \text{ V} - 11 \text{ V}}{12 \text{ V} - 5.5 \text{ V}} = 9.24 \text{ ms}$$

$$T = 9.24 \text{ ms} + 0.693(30 \text{ k}\Omega)(47 \text{ nF}) = 10.2 \text{ ms}$$

The duty cycle is:

$$D = \frac{W}{T} = \frac{9.24 \text{ ms}}{10.2 \text{ ms}} = 0.906$$

The frequency is:

$$f = \frac{1}{T} = \frac{1}{10.2 \text{ ms}} = 98 \text{ Hz}$$

When  $V_{con}$  is 1 V, the calculations give:

$$W = -(75 \text{ k}\Omega + 30 \text{ k}\Omega)(47 \text{ nF}) \ln \frac{12 \text{ V} - 1 \text{ V}}{12 \text{ V} - 0.5 \text{ V}} = 0.219 \text{ ms}$$

$$T = 0.219 \text{ ms} + 0.693(30 \text{ k}\Omega)(47 \text{ nF}) = 1.2 \text{ ms}$$

$$D = \frac{W}{T} = \frac{0.219 \text{ ms}}{1.2 \text{ ms}} = 0.183$$

$$f = \frac{1}{T} = \frac{1}{1.2 \text{ ms}} = 833 \text{ Hz}$$

**PRACTICE PROBLEM 23-9** Repeat Example 23-9 with  $V_{CC} = 15 \text{ V}$  and  $V_{con} = 10 \text{ V}$ .

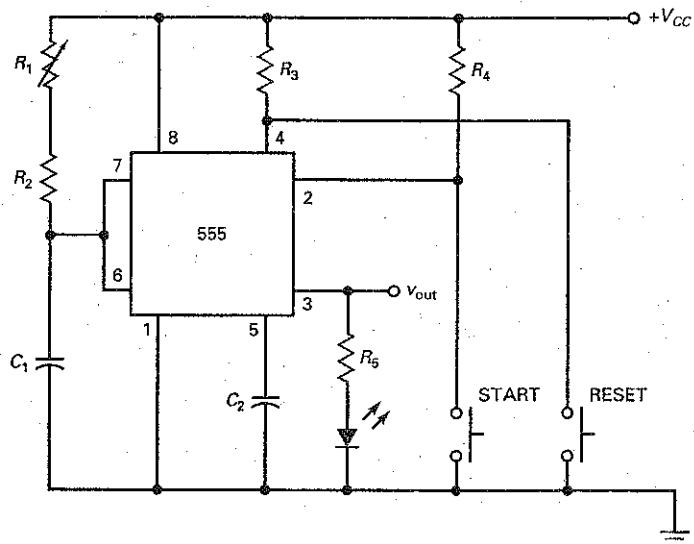
## 23-9 555 Circuits

The output stage of a 555 timer can *source* 200 mA. This means that a high output can produce up to 200 mA of load current (sourcing). Because of this, the 555 timer can drive relatively heavy loads such as relays, lamps, and loudspeakers. The output stage of a 555 timer can also *sink* 200 mA. This means that a low output can allow up to 200 mA to flow to ground (sinking). For instance, when a 555 timer drives a TTL load, the timer sources current when the output is high and it sinks current when the output is low. In this section, we discuss some applications for a 555 timer.

### Start and Reset

Figure 23-39 shows a circuit with a number of modifications from the monostable timer shown earlier. To begin with, the trigger input (pin 2) is controlled by a

**Figure 23-39** Monostable timer with adjustable pulse width and START and RESET buttons.



push-button switch (START). Since the switch is normally open, pin 2 is high and the circuit is inactive.

When somebody pushes and releases the START switch, pin 2 is temporarily pulled down to ground. Therefore, the output goes high and the LED turns on. Capacitor  $C_1$  charges positively, as previously described. The charging time constant can be varied with  $R_1$ . In this way, we can get time delays of seconds to hours. When the capacitor voltage is slightly greater than  $2V_{CC}/3$ , the circuit resets and the output goes low. When this happens, the LED turns off.

Notice the RESET switch. It can be used to reset the circuit at any time during the output pulse. Since the switch is normally open, pin 4 is high and has no effect on the operation of the timer. When the RESET switch is closed, however, pin 4 is pulled down to ground and the output is reset to zero. The RESET is included because the user may want to terminate the high output. For instance, if the output pulse width has been set to 5 min, the user can terminate the pulse prematurely by pushing the RESET.

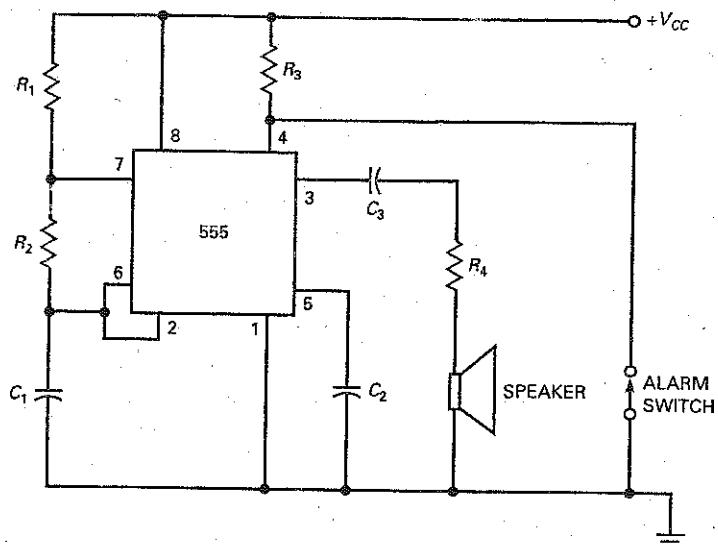
Incidentally, the output signal  $v_{out}$  can be used to drive a relay, a power FET, an IGBT, a buzzer, and so on. The LED serves as an indicator of the high output being delivered to some other circuit.

### Sirens and Alarms

Figure 23-40 shows how to use an astable 555 timer as a siren or an alarm. Normally, the ALARM switch is closed, which pulls pin 4 down to ground. In this case, the 555 timer is inactive and there is no output. When the ALARM switch is opened, however, the circuit will generate a rectangular output whose frequency is determined by  $R_1$ ,  $R_2$ , and  $C_1$ .

The output from pin 3 drives a loudspeaker through a resistance of  $R_4$ . The size of this resistance depends on the supply voltage and the impedance of the loudspeaker. The impedance of the branch with  $R_4$  and the speaker should limit the output current to 200 mA or less because this is the maximum current a 555 timer can source.

Figure 23-40 Astable 555 circuit used for siren or alarm.



The circuit of Fig. 23-40 can be modified to produce more output power for the speaker. For instance, we can use the output from pin 3 to drive a class B push-pull power amplifier, the output of which then drives the speaker.

### Pulse-Width Modulator

Figure 23-41 shows a circuit used for pulse-width modulation (PWM). The 555 timer is connected in the monostable mode. The values of  $R$ ,  $C$ , UTP, and  $V_{CC}$  determine the width of the output pulse as follows:

$$W = -RC \ln \left( 1 - \frac{UTP}{V_{CC}} \right) \quad (23-34)$$

A low-frequency signal called a **modulating signal** is capacitively coupled into pin 5. This modulating signal is voice or computer data. Since pin 5 controls the value of UTP,  $v_{mod}$  is being added to the quiescent UTP. Therefore, the instantaneous UTP is given by:

$$UTP = \frac{2V_{CC}}{3} + v_{mod} \quad (23-35)$$

For instance, if  $V_{CC} = 12$  V and the modulating signal has a peak value of 1 V, then Eq. (23-31) gives:

$$UTP_{max} = 8 \text{ V} + 1 \text{ V} = 9 \text{ V}$$

$$UTP_{min} = 8 \text{ V} - 1 \text{ V} = 7 \text{ V}$$

This means that the instantaneous UTP varies sinusoidally between 7 and 9 V.

A train of triggers called the *clock* is the input to pin 2. Each trigger produces an output pulse. Since the period of the triggers is  $T$ , the output will be a series of rectangular pulses with a period of  $T$ . The modulating signal has no effect on the period  $T$ , but it does change the width of each output pulse. At point A, the positive peak of the modulating signal, the output pulse is wide as shown. At point B, the negative peak of the modulating signal, the output pulse is narrow.

PWM is used in communications. It allows a low-frequency modulating signal (voice or data) to change the pulse width of a high-frequency signal called the **carrier**. The modulated carrier can be transmitted over copper wire, over fiber-optic cable, or through space to a receiver. The receiver recovers the modulating signal to drive a speaker (voice) or a computer (data).

### Pulse-Position Modulation

With PWM, the pulse width changes, but the period is constant because it is determined by the frequency of the input triggers. Because the period is fixed, the position of each pulse is the same, which means that the leading edge of the pulse always occurs after a fixed interval of time.

**Pulse-position modulation (PPM)** is different. With this type of modulation, the position (leading edge) of each pulse changes. With PPM, both the width and the period of pulses vary with the modulating signal.

Figure 23-42a shows a *pulse-position modulator*. It is similar to the VCO discussed earlier. Since the modulating signal is coupled into pin 5, the instantaneous UTP is given by Eq. (23-35):

$$UTP = \frac{2V_{CC}}{3} + v_{mod}$$

When the modulating signal increases, UTP increases and the pulse width increases. When the modulating signal decreases, UTP decreases and the pulse width decreases. This is why the pulse width varies as shown in Fig. 23-42b.

The pulse width and period equations are:

$$W = -(R_1 + R_2)C \ln \frac{V_{CC} - UTP}{V_{CC} - 0.5 UTP} \quad (23-36)$$

$$T = W + 0.693R_2C \quad (23-37)$$

In Eq. (23-37), the second term is the *space* between pulses:

$$\text{Space} = 0.693R_2C \quad (23-38)$$

This space is the time between the trailing edge of one pulse and the leading edge of the next pulse. Since  $V_{con}$  does not appear in Eq. (23-38), the space between pulses is constant, as shown in Fig. 23-42b.

Since the space is constant, the position of the leading edge of any pulse depends on how wide the preceding pulse is. This is why this type of modulation is called *pulse-position modulation*. Like PWM, PPM is used in communication systems to transfer voice or data.

### Ramp Generation

Charging a capacitor through a resistor produces an exponential waveform. If we use a constant current source instead of a resistor to charge a capacitor, the capacitor voltage is ramp. This is the idea behind the circuit of Fig. 23-43a. Here we have replaced the resistor of a monostable circuit with a *pnp* current source that produces a constant charging current of:

$$I_C = \frac{V_{CC} - V_E}{R_E} \quad (23-39)$$

When a trigger starts the monostable 555 timer of Fig. 23-43a, the *pnp* current source forces a constant charging current into the capacitor. Therefore, the voltage across the capacitor is a ramp, as shown in Fig. 23-43b. The slope  $S$  of the ramp is given by:

$$S = \frac{I_C}{C} \quad (23-40)$$

Since the capacitor voltage reaches a maximum value  $2V_{CC}/3$  before discharge occurs, the peak value of the ramp shown in Fig. 23-43b is:

$$V = \frac{2V_{CC}}{3} \quad (23-41)$$

and the duration  $T$  of the ramp is:

$$T = \frac{2V_{CC}}{3I} \quad (23-42)$$

## Example 23-10

A pulse-width modulator like Fig. 23-41 has  $V_{CC} = 12$  V,  $R = 9.1$  k $\Omega$ , and  $C = 0.01$   $\mu$ F. The clock has a frequency of 2.5 kHz. If a modulating signal has a peak value of 2 V, what is the period of the output pulses? What is the quiescent pulse width? What are the minimum and maximum pulse widths? What are the minimum and maximum duty cycles?

**SOLUTION** The period of the output pulses equals the period of the clock:

$$T = \frac{1}{2.5 \text{ kHz}} = 400 \mu\text{s}$$

The quiescent pulse width is:

$$W = 1.1RC = 1.1(9.1 \text{ k}\Omega)(0.01 \mu\text{F}) = 100 \mu\text{s}$$

With Eq. (23-35), calculate the minimum and maximum UTP:

$$\text{UTP}_{\min} = 8 \text{ V} - 2 \text{ V} = 6 \text{ V}$$

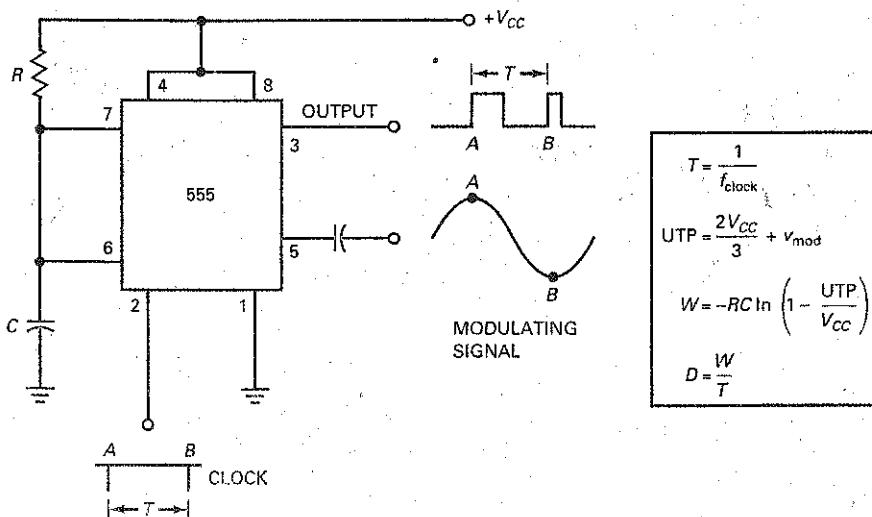
$$\text{UTP}_{\max} = 8 \text{ V} + 2 \text{ V} = 10 \text{ V}$$

Now, calculate the minimum and maximum pulse widths with Eq. (23-34):

$$W_{\min} = -(9.1 \text{ k}\Omega)(0.01 \mu\text{F}) \ln \left( 1 - \frac{6 \text{ V}}{12 \text{ V}} \right) = 63.1 \mu\text{s}$$

$$W_{\max} = -(9.1 \text{ k}\Omega)(0.01 \mu\text{F}) \ln \left( 1 - \frac{10 \text{ V}}{12 \text{ V}} \right) = 163 \mu\text{s}$$

Figure 23-41 555 timer connected as pulse-width modulator.



The minimum and maximum duty cycles are:

$$D_{\min} = \frac{63.1 \mu s}{400 \mu s} = 0.158$$

$$D_{\max} = \frac{163 \mu s}{400 \mu s} = 0.408$$

**PRACTICE PROBLEM 23-10** Following Example 23-10, change  $V_{CC}$  to 15 V. Calculate the maximum pulse width and maximum duty cycle.

## Example 23-11

A pulse-position modulator like Fig. 23-42 has  $V_{CC} = 12$  V,  $R_1 = 3.9$  k $\Omega$ ,  $R_2 = 3$  k $\Omega$ , and  $C = 0.01$   $\mu F$ . What are the quiescent width and period of the output pulses? If a modulating signal has a peak value of 1.5 V, what are the minimum and maximum pulse widths? What is the space between pulses?

**SOLUTION** With no modulating signal, the quiescent period of the output pulses is that of a 555 timer used as an astable multivibrator. With Eqs. (23-26) and (23-27), we can calculate the quiescent width and period as follows:

$$W = 0.693(3.9 \text{ k}\Omega + 3 \text{ k}\Omega)(0.01 \mu F) = 47.8 \mu s$$

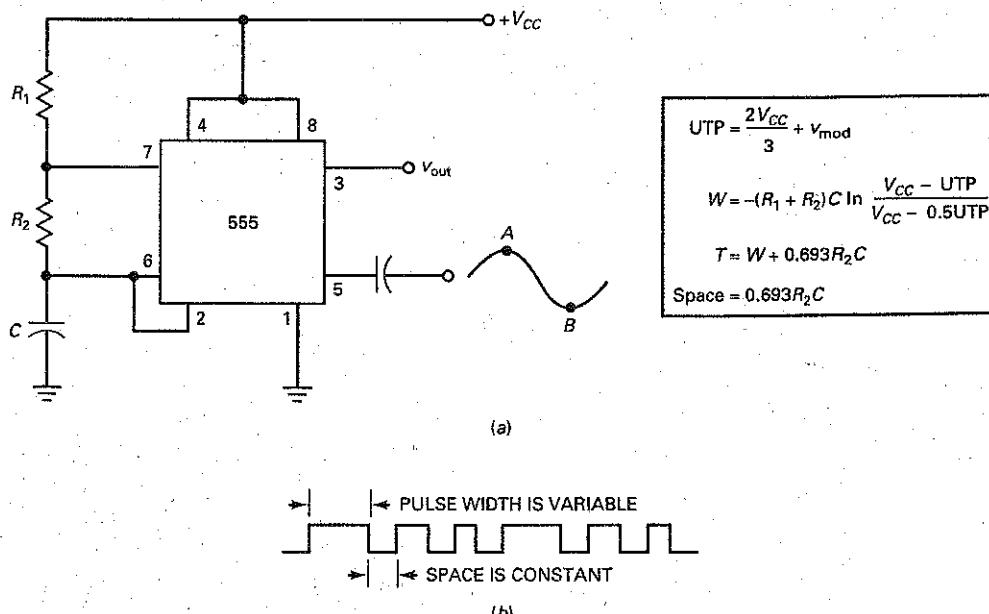
$$T = 0.693(3.9 \text{ k}\Omega + 6 \text{ k}\Omega)(0.01 \mu F) = 68.6 \mu s$$

With Eq. (23-35), calculate the minimum and maximum UTP:

$$UTP_{\min} = 8 \text{ V} - 1.5 \text{ V} = 6.5 \text{ V}$$

$$UTP_{\max} = 8 \text{ V} + 1.5 \text{ V} = 9.5 \text{ V}$$

Figure 23-42 The 555 timer connected as pulse-position modulator.



With Eq. (23-36), the minimum and maximum pulse widths are:

$$W_{\min} = -(3.9 \text{ k}\Omega + 3 \text{ k}\Omega)(0.01 \mu\text{F}) \ln \frac{12 \text{ V} - 6.5 \text{ V}}{12 \text{ V} - 3.25 \text{ V}} = 32 \mu\text{s}$$

$$W_{\max} = -(3.9 \text{ k}\Omega + 3 \text{ k}\Omega)(0.01 \mu\text{F}) \ln \frac{12 \text{ V} - 9.5 \text{ V}}{12 \text{ V} - 4.75 \text{ V}} = 73.5 \mu\text{s}$$

With Eq. (23-37), the minimum and maximum periods are:

$$T_{\min} = 32 \mu\text{s} + 0.693(3 \text{ k}\Omega)(0.01 \mu\text{F}) = 52.8 \mu\text{s}$$

$$T_{\max} = 73.5 \mu\text{s} + 0.693(3 \text{ k}\Omega)(0.01 \mu\text{F}) = 94.3 \mu\text{s}$$

The space between the trailing edge of any pulse and the leading edge of the next pulse is:

$$\text{Space} = 0.693(3 \text{ k}\Omega)(0.01 \mu\text{F}) = 20.8 \mu\text{s}$$

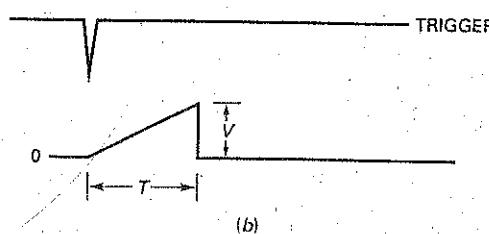
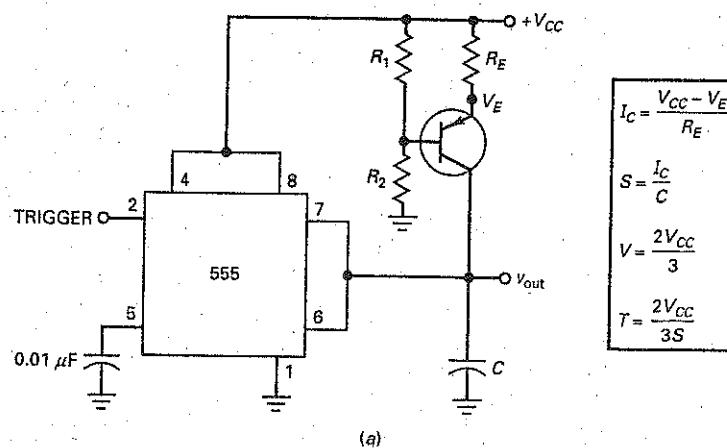
## Example 23-12

The ramp generator of Fig. 23-43 has a constant collector current of 1 mA. If  $V_{CC} = 15 \text{ V}$  and  $C = 100 \text{ nF}$ , what is the slope of the output ramp? What is its peak value? What is its duration?

**SOLUTION** The slope is

$$S = \frac{1 \text{ mA}}{100 \text{ nF}} = 10 \text{ V/ms}$$

Figure 23-43 (a) Bipolar junction transistor and 555 timer produce ramp output; (b) trigger and ramp waveforms.



The peak value is

$$V = \frac{2(15 \text{ V})}{3} = 10 \text{ V}$$

The duration of the ramp is:

$$T = \frac{2(15 \text{ V})}{3(10 \text{ V/ms})} = 1 \text{ ms}$$

**PRACTICE PROBLEM 23-12** Using Fig. 23-43, with  $V_{CC} = 12 \text{ V}$  and  $C = 0.2 \mu\text{F}$ , repeat Example 23-12.

## 23-10 The Phase-Locked Loop

A phase-locked loop (PLL) contains a phase detector, a dc amplifier, a low-pass filter, and a voltage-controlled oscillator (VCO). When a PLL has an input signal with a frequency of  $f_{in}$ , its VCO will produce an output frequency that equals  $f_{in}$ .

### Phase Detector

Figure 23-44a shows a phase detector, the first stage in a PLL. This circuit produces an output voltage proportional to the phase difference between two input signals. For instance, Fig. 23-44b shows two input signals with a phase difference of  $\Delta\phi$ . The phase detector responds to this phase difference by producing a dc output voltage, which is proportional to  $\Delta\phi$ , as shown in Fig. 23-44c.

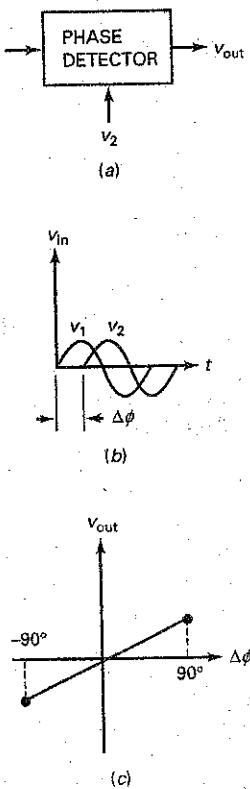
When  $v_1$  leads  $v_2$ , as shown in Fig. 23-44b,  $\Delta\phi$  is positive. If  $v_1$  were to lag  $v_2$ ,  $\Delta\phi$  would be negative. The typical phase detector produces a linear response between  $-90^\circ$  and  $+90^\circ$ , as shown in Fig. 23-44c. As we can see, the output of the phase detector is zero when  $\Delta\phi = 0^\circ$ . When  $\Delta\phi$  is between  $0^\circ$  and  $90^\circ$ , the output is a positive voltage. When  $\Delta\phi$  is between  $0^\circ$  and  $-90^\circ$ , the output is a negative voltage. The key idea here is that the phase detector produces an output voltage that is directly proportional to the phase difference between its two input signals.

### The VCO

In Fig. 23-45a, the input voltage  $v_{in}$  to the VCO determines the output frequency  $f_{out}$ . A typical VCO can be varied over a 10:1 range of frequency. Furthermore, the variation is linear as shown in Fig. 23-45b. When the input voltage to the VCO is zero, the VCO is free-running at a quiescent frequency  $f_0$ . When the input voltage is positive, the VCO frequency is greater than  $f_0$ . If the input voltage is negative, the VCO frequency is less than  $f_0$ .

### Block Diagram of a PLL

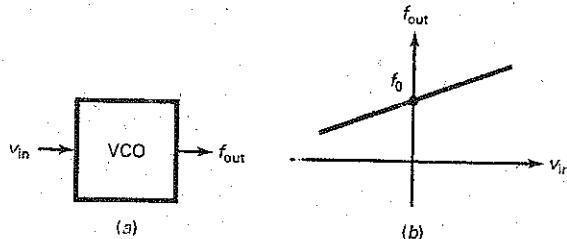
Figure 23-46 is a block diagram of a PLL. The phase detector produces a dc voltage that is proportional to the phase difference of its two input signals. The output voltage of the phase detector is usually small. This is why the second stage is a dc



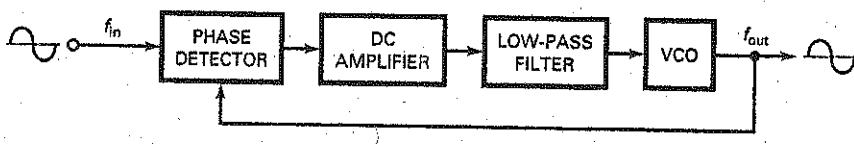
## GOOD TO KNOW

The transfer function or conversion gain  $K$  of a VCO can be expressed as the amount of frequency deviation  $\Delta f$  per unit change, or  $\Delta V$  in dc input voltage. Expressed mathematically,  $K = \Delta f/\Delta V$ , where  $K$  is the input/output transfer function specified in hertz per volt.

**Figure 23-45** (a) Input voltage controls output frequency of VCO; (b) output frequency is directly proportional to input voltage.



**Figure 23-46** Block diagram of a phase-locked loop.



amplifier. The amplified phase difference is filtered before being applied to the VCO. Notice that the VCO output is being fed back to the phase detector.

## Input Frequency Equals Free-Running Frequency

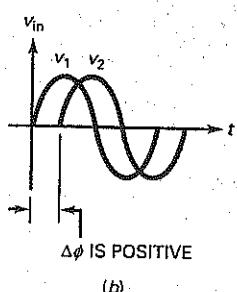
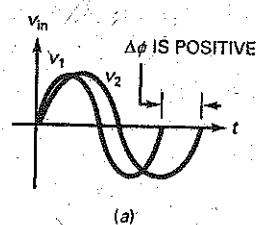
To understand PLL action, let us start with the case of input frequency equal to  $f_0$ , the free-running frequency of the VCO. In this case, the two input signals to the phase detector have the same frequency and phase. Because of this, the phase difference  $\Delta\phi$  is  $0^\circ$  and the output of the phase detector is zero. As a result, the input voltage to the VCO is zero, which means that the VCO is free-running with a frequency of  $f_0$ . As long as the frequency and phase of the input signal remain the same, the input voltage to the VCO will be zero.

## Input Frequency Differs from Free-Running Frequency

Let us assume that the input and free-running VCO frequencies are each 10 kHz. Now, suppose the input frequency increases to 11 kHz. This increase will appear to be an increase in phase because  $v_1$  leads  $v_2$  at the end of the first cycle, as shown in Fig. 23-47a. Since input signal leads the VCO signal,  $\Delta\phi$  is positive. In this case, the phase detector of Fig. 23-46 produces a positive output voltage. After being amplified and filtered, this positive voltage increases the VCO frequency.

The VCO frequency will increase until it equals 11 kHz, the frequency of the input signal. When the VCO frequency equals the input frequency, the VCO is *locked on* to the input signal. Even though each of the two input signals to the phase detector has a frequency of 11 kHz, the signals have a different phase, as shown in Fig. 23-47b. This positive phase difference produces the voltage needed to keep the VCO frequency slightly above its free-running frequency.

**Figure 23-47** (a) An increase in the frequency of  $v_1$  produces a phase difference; (b) a phase difference exists after the VCO frequency increases.



If the input frequency increases further, the VCO frequency also increases as needed to maintain the lock. For instance, if the input frequency increases to 12 kHz, the VCO frequency increases to 12 kHz. The phase difference between the two input signals will increase as needed to produce the correct control voltage for the VCO.

### Lock Range

The **lock range** of a PLL is the range of input frequencies over which the VCO can remain locked on to the input frequency. It is related to the maximum phase difference that can be detected. In our discussion, we are assuming that the phase detector can produce an output voltage for  $\Delta\phi$  between  $-90^\circ$  and  $+90^\circ$ . At these limits, the phase detector produces a maximum output voltage, either negative or positive.

If the input frequency is too low or too high, the phase difference is outside the range of  $-90^\circ$  and  $+90^\circ$ . Therefore, the phase detector cannot produce the additional voltage needed for the VCO to remain locked on. At these limits, therefore, the PLL loses its lock on the input signal.

The lock range is usually specified as a percentage of the VCO frequency. For instance, if the VCO frequency is 10 kHz and the lock range is  $\pm 20$  percent, the PLL can remain locked on any input frequency between 8 and 12 kHz.

### Capture Range

The capture range is different. Assume that the input frequency is outside the lock range. Then, the VCO is free-running at 10 kHz. Now, assume that the input frequency changes toward the VCO frequency. At some point, the PLL will be able to lock on to the input frequency. The range of input frequencies within which the PLL can reestablish the lock is called the **capture range**.

The capture range is specified as a percentage of the free-running frequency. If  $f_0 = 10$  kHz and the capture range is  $\pm 5$  percent, the PLL can lock on to an input frequency between 9.5 and 10.5 kHz. Typically, the capture range is less than the lock range because the capture range depends on the cutoff frequency of the low-pass filter. The lower the cutoff frequency, the smaller the capture range.

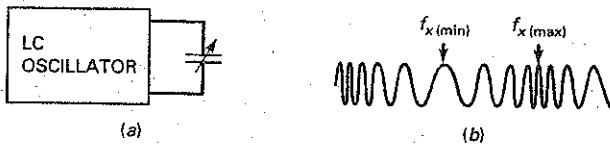
The cutoff frequency of the low-pass filter is kept low to prevent high-frequency components like noise or other unwanted signals from reaching the VCO. The lower the cutoff frequency of the filter, the cleaner the signal driving the VCO. Therefore, a designer has to trade off capture range against low-pass bandwidth to get a clean signal for the VCO.

### Applications

A PLL can be used in two fundamentally different ways. First, it can be used to lock on to the input signal. The output frequency then equals the input frequency. This has the advantage of cleaning up a noisy input signal because the low-pass filter will remove high-frequency noise and other components. Since the output signal comes from the VCO, the final output is stable and almost noise-free.

Second, a PLL can be used as an FM demodulator. The theory of **frequency modulation (FM)** is covered in communication courses, so we will discuss only the basic idea. The *LC* oscillator of Fig. 23-48a has a variable capacitance. If a modulating signal controls this capacitance, the oscillator output will be *frequency-modulated*, as shown in Fig. 23-48b. Notice how the frequency of

**Figure 23-48** (a) Variable capacitance changes resonant frequency of LC oscillator; (b) sine wave has been frequency-modulated.



this FM wave varies from a minimum to a maximum, corresponding to the minimum and maximum peaks of the modulating signal.

If the FM signal is the input to a PLL, the VCO frequency will lock on to the FM signal. Since the VCO frequency varies,  $\Delta\phi$  follows the variations in the modulating signal. Therefore, the output of the phase detector will be a low-frequency signal that is a replica of the original modulating signal. When used in this way, the PLL is being used as an *FM demodulator*, a circuit that recovers the modulating signal from the FM wave.

PLLs are available as monolithic ICs. For instance, the NE565 is a PLL that contains a phase detector, a VCO, and a dc amplifier. The user connects external components like a timing resistor and capacitor to set the free-running frequency of the VCO. Another external capacitor sets the cutoff frequency of the low-pass filter. The NE565 can be used for FM demodulation, frequency synthesis, telemetry receivers, modems, tone decoding, and so forth.

## 23-11 Function Generator ICs

Special function generator ICs have been developed that combine many of the individual circuit capabilities we have been discussing. These ICs are able to provide waveform generation including sine, square, triangle, ramp, and pulse signals. The output waveforms can be made to vary in amplitude and frequency by changing the values of external resistors and capacitors or by applying an external voltage. This external voltage enables the IC to perform useful applications such as voltage-to-frequency (V/F) conversion, AM and FM signal generation, voltage-controlled oscillation (VCO), and frequency-shift keying (FSK).

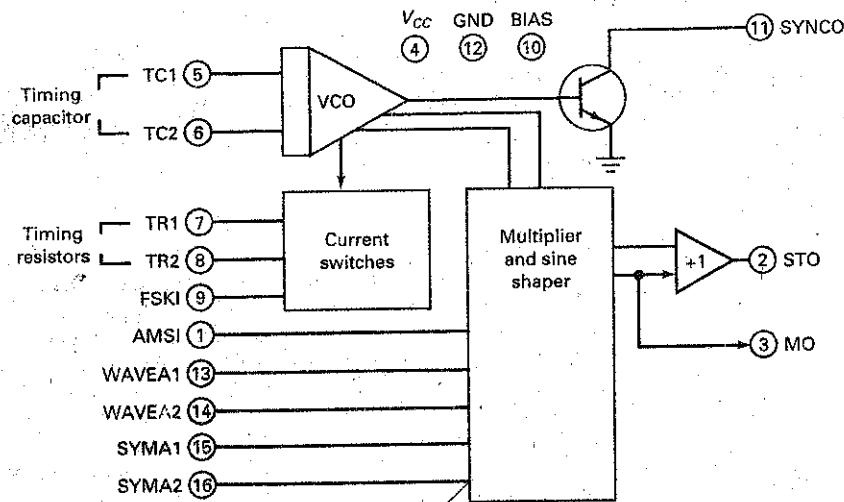
### The XR-2206

An example of a special function generator IC is the XR-2206. This monolithic IC can provide externally controlled frequencies from 0.01 Hz to more than 1.00 MHz. A block diagram of this IC is shown in Fig. 23-49. The diagram shows four main functional blocks, which include a VCO, an analog multiplier and sine-shaper, a unity gain buffer amplifier, and a set of current switches.

The output frequency of the VCO is proportional to an input current, which is determined by a set of external timing resistors. These resistors connect to pins 7 and 8, respectively, and ground. Because there are two timing pins, two discrete output frequencies can be obtained. A high or low input signal on pin 9 controls the current switches. The current switches then select which one of the timing resistors will be used. If the input signal on pin 9 alternately changes from high to low, the output frequency of the VCO will be shifted from one frequency to another. This action is referred to as **frequency-shift keying (FSK)** and is used in electronic communication applications.

The output of the VCO drives the multiplier and sine-shaper block, along with an output switching transistor. The output switching transistor is driven to

Figure 23-49 XR-2206 block diagram.



cutoff and saturation, which provides a square wave output signal at pin 11. The output of the multiplier and sine-shaper block is connected to a unity gain buffer amplifier, which determines the IC's output current capability and its output impedance. The output at pin 2 can be either a sine wave or a triangle wave.

### Sine- and Triangle-Wave Output

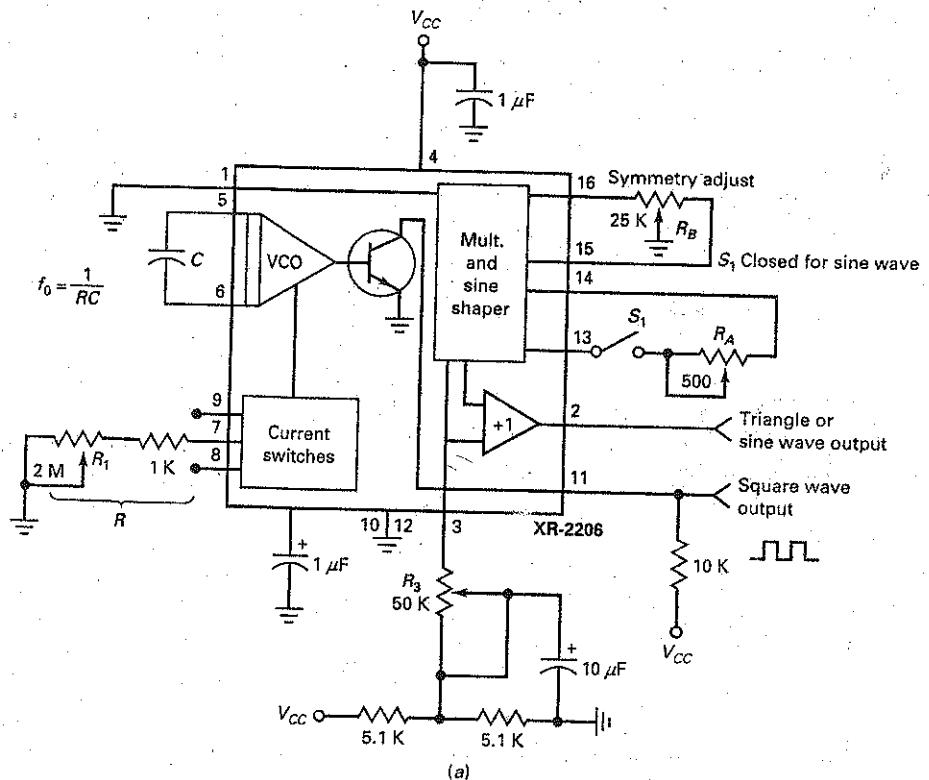
Fig. 23-50a shows the external circuit connections and components for generating sine waves or triangle waves. The frequency of oscillation  $f_0$  is determined by the timing resistor  $R$ , connected at either pin 7 or pin 8, and the external capacitor  $C$ , connected across pins 5 and 6. The value of oscillation is found by:

$$f_0 = \frac{1}{RC} \quad (23-31)$$

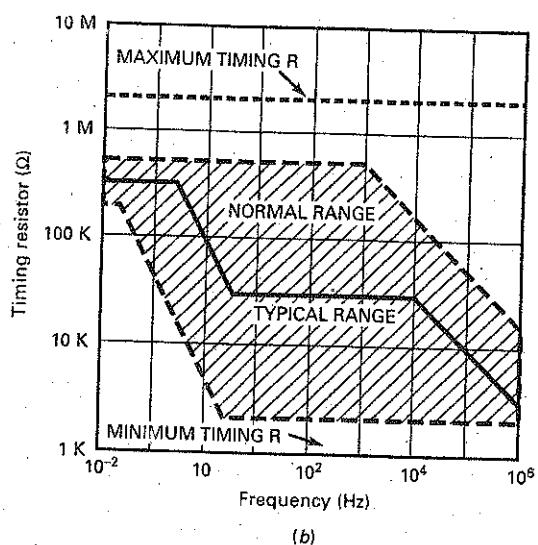
Even though  $R$  can be up to  $2 \text{ M}\Omega$ , maximum temperature stability occurs when  $4 \text{ k}\Omega < R < 200 \text{ k}\Omega$ . A graph of  $R$  versus oscillation frequency is shown in Fig. 23-50b. Also, the recommended value of  $C$  should be from  $1000 \text{ pF}$  to  $100 \mu\text{F}$ .

In Fig. 23-50a, when the switch  $S_1$  is closed, the output at pin 2 will be a sine wave. The potentiometer  $R_1$  at pin 7 provides the desired frequency tuning. Adjustable resistors  $R_A$  and  $R_B$  enable the output waveform to be modified for proper waveform symmetry and distortion levels. When  $S_1$  is open, the output at pin 2 changes from a sine wave to a triangle wave. Resistor  $R_3$ , connected at pin 3, controls the amplitude of the output waveform. As shown in Fig. 23-50c, the output amplitude is directly proportional to the value of  $R_3$ . Notice that the value of the triangle waveform is approximately double the output of a sine waveform for a given  $R_3$  setting.

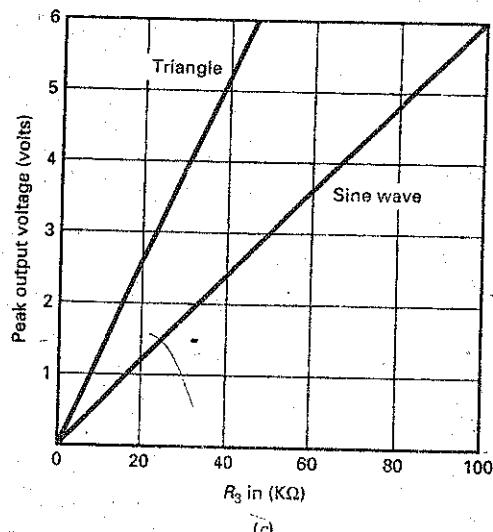
Figure 23-50 Sine-wave generation: (a) Circuit; (b) R versus oscillation frequency; (c) output amplitude.



(a)

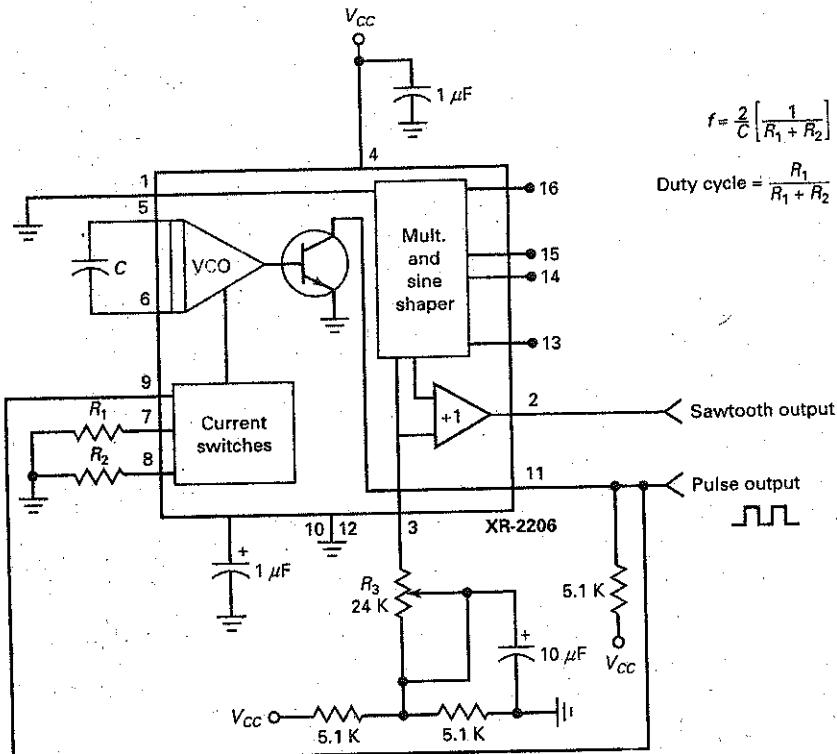


(b)



(c)

Figure 23-51 Pulse and ramp generation.



## Pulse and Ramp Generation

Fig. 23-51 shows the external connections of the circuit used to create sawtooth (ramp) and pulse outputs. Notice that the square wave output at pin 11 is shorted to the FSK terminal at pin 9. This allows the circuit to automatically frequency-shift between two separate frequencies. This frequency shift occurs when the output at pin 11 changes from a high-level output to a low-level output or from a low-level output to a high-level output. The output frequency is found by:

$$f = \frac{2}{C} \left[ \frac{1}{R_1 + R_2} \right] \quad (23-32)$$

and the circuit's duty cycle is found by:

$$D = \frac{R_1}{R_1 + R_2} \quad (23-33)$$

Fig. 23-52 shows a data sheet for the XR-2206. If operated with a single positive supply voltage, the supply can range from 10 V to 26 V. If a split- or dual-supply voltage is used, notice how the values range from  $\pm 5$  V to  $\pm 13$  V. Fig. 23-52 also shows recommended  $R$  and  $C$  values for generating maximum and minimum output frequencies. Also specified is the typical sweep range of 2000:1. As shown in the data sheet, the triangle- and sine-wave output has an output impedance value of  $600 \Omega$ . This makes the XR-2206 function generator IC well suited for many electronic communications applications.

Figure 23-52 The XR-2206 data sheet.

# XR-2206

**EXAR**

## DC ELECTRICAL CHARACTERISTICS

Test Conditions:

$V_{cc} = 12V$ ,  $T_A = 25^\circ C$ ,  $C = 0.01\mu F$ ,  $R_1 = 100k\Omega$ ,  $R_2 = 10k\Omega$ ,  $R_3 = 25k\Omega$

Unless Otherwise Specified.  $S_1$  open for triangle, closed for sine wave.

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>General Characteristics</b>								
Single Supply Voltage	10		26	10		26	V	
Split-Supply Voltage	$\pm 5$		$\pm 13$	$\pm 5$		$\pm 13$	V	
Supply Current		12	17		14	20	mA	$R_1 \geq 10k\Omega$
<b>Oscillator Section</b>								
Max. Operating Frequency	0.5	1		0.5	1		MHz	$C = 1000pF$ , $R_1 = 1k\Omega$
Lowest Practical Frequency		0.01			0.01		Hz	$C = 50\mu F$ , $R_1 = 2M\Omega$
Frequency Accuracy		$\pm 1$	$\pm 4$		$\pm 2$		% of $f_0$	$f_0 = 1/R_1C$
Temperature Stability		$\pm 10$	$\pm 50$		$\pm 20$		ppm/ $^\circ C$	$0^\circ C \leq T_A \leq 70^\circ C$
Frequency								$R_1 = R_2 = 20k\Omega$
Sine Wave Amplitude Stability <sup>2</sup>	4800			4800			ppm/ $^\circ C$	
Supply Sensitivity		0.01	0.1		0.01		%/V	$V_{LOW} = 10V$ , $V_{HIGH} = 20V$ , $R_1 = R_2 = 20k\Omega$
Sweep Range	1000:1	2000:1		2000:1				$f_L = f_H$ @ $R_1 = 1k\Omega$ $f_L = f_H$ @ $R_1 = 2M\Omega$
<b>Sweep Linearity</b>								
10:1 Sweep			2		2		%	$f_L = 1kHz$ , $f_H = 10kHz$
1000:1 Sweep		8			8		%	$f_L = 100Hz$ , $f_H = 100kHz$
FM Distortion		0.1			0.1		%	$\pm 10\%$ Deviation
<b>Recommended Timing Components</b>								
Timing Capacitor: C	0.001		100	0.001		100	$\mu F$	
Timing Resistors: $R_1$ & $R_2$	1		2000	1		2000	$k\Omega$	
<b>Triangle Sine Wave Output<sup>1</sup></b>								
Triangle Amplitude		160		160			mV/k $\Omega$	$S_1$ Open
Sine Wave Amplitude	40	60	80	60			mV/k $\Omega$	$S_1$ Closed
Max. Output Swing		6		6			Vp-p	
Output Impedance		600		600			$\Omega$	
Triangle Linearity		1		1			%	
Amplitude Stability		0.5		0.5			dB	For 1000:1 Sweep
<b>Sine Wave Distortion</b>								
Without Adjustment			2.5		2.5		%	$R_1 = 30k\Omega$
With Adjustment		0.4	1.0		0.6	1.5	%	

### Notes

<sup>1</sup> Output amplitude is directly proportional to the resistance,  $R_3$ , on Pin 3.

<sup>2</sup> For maximum amplitude stability,  $R_3$  should be a positive temperature coefficient resistor.

**Bold face** parameters are covered by production test and guaranteed over operating temperature range.

Figure 23-52 (continued).

### DC ELECTRICAL CHARACTERISTICS (CONT'D)

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>Amplitude Modulation</b>								
Input Impedance	50	100		50	100		kΩ	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
<b>Square-Wave Output</b>								
Amplitude		12			12		V <sub>p-p</sub>	Measured at Pin 11.
Rise Time		250			250		ns	C <sub>L</sub> = 10 pF
Fall Time		50			50		ns	C <sub>L</sub> = 10 pF
Saturation Voltage		0.2	0.4		0.2	0.6	V	I <sub>L</sub> = 2 mA
Leakage Current		0.1	20		0.1	100	μA	V <sub>CC</sub> = 26 V
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See section on circuit controls
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

### Example 23-13

In Fig. 23-50,  $R = 10 \text{ k}\Omega$  and  $C = 0.01 \mu\text{F}$ . With  $S_1$  closed, what are the output waveforms and output frequency at pins 2 and 11?

**SOLUTION** Because  $S_1$  is closed, the output at pin 2 will be a sine wave and the output at pin 11 will be a square wave. Both output waveforms will have the same frequency. The output frequency is found by:

$$f_0 = \frac{1}{RC} = \frac{1}{(10 \text{ k}\Omega)(0.01 \mu\text{F})} = 10 \text{ kHz}$$

**PRACTICE PROBLEM 23-13** Repeat Example 23-13 with  $R = 20 \text{ k}\Omega$ ,  $C = 0.01 \mu\text{F}$ , and  $S_1$  open.

### Example 23-14

In Fig. 23-51,  $R_1 = 1 \text{ k}\Omega$ ,  $R_2 = 2 \text{ k}\Omega$ , and  $C = 0.1 \mu\text{F}$ . Determine the square-wave output frequency and duty cycle.

**SOLUTION** Using Eq. (23-32), the frequency out at pin 11 is:

$$f = \frac{2}{0.1 \mu\text{F}} \left[ \frac{1}{1 \text{ k}\Omega + 2 \text{ k}\Omega} \right] = 6.67 \text{ kHz}$$

The duty cycle is found using Eq. (23-33) as:

$$D = \frac{1 \text{ k}\Omega}{1 \text{ k}\Omega + 2 \text{ k}\Omega} = 0.333$$

**PRACTICE PROBLEM 23-14** Repeat Example 23-14 with  $R_1$  and  $R_2 = 2 \text{ k}\Omega$  and  $C = 0.2 \mu\text{F}$ .

## Summary

### SEC. 23-1 THEORY OF SINUSOIDAL OSCILLATION

To build a sinusoidal oscillator, we need to use an amplifier with positive feedback. For the oscillator to start, the loop gain must be greater than 1 when the phase shift around the loop is  $0^\circ$ .

### SEC. 23-2 THE WIEN-BRIDGE OSCILLATOR

This is the standard oscillator for low to moderate frequencies in the range of 5 Hz to 1 MHz. It produces an almost perfect sine wave. A tungsten lamp or other nonlinear resistance is used to decrease the loop gain to 1.

### SEC. 23-3 OTHER RC OSCILLATORS

The twin-T oscillator uses an amplifier and *RC* circuits to produce the required loop gain and phase shift at the resonant frequency. It works well at one frequency but is not suitable for an adjustable frequency oscillator. The phase-shift oscillator also uses an amplifier and *RC* circuits to produce oscillations. An amplifier can act like a phase-shift oscillator because of the stray lead and lag circuits in each stage.

### SEC. 23-4 THE COLPITTS OSCILLATOR

*RC* oscillators usually do not work well above 1 MHz because of the additional phase shift inside the amplifier. This is why *LC* oscillators are preferred for frequencies between 1 and 500 MHz. This frequency range is beyond the  $f_{\text{unity}}$  of most op amps, which is why a bipolar junction transistor or FET is commonly

used for the amplifying device. The Colpitts oscillator is one of the most widely used *LC* oscillators.

### SEC. 23-5 OTHER LC OSCILLATORS

The Armstrong oscillator uses a transformer to produce the feedback signal. The Hartley oscillator uses an inductive voltage divider to produce the feedback signal. The Clapp oscillator has a small series capacitor in the inductive branch of the resonant circuit. This reduces the effect that stray capacitances have on the resonant frequency.

### SEC. 23-6 QUARTZ CRYSTALS

Some crystals exhibit the piezoelectric effect. Because of this effect, a vibrating crystal acts like an *LC* resonant circuit with an extremely high *Q*. Quartz is the most important crystal producing the piezoelectric effect. It is used in crystal oscillators, in which a precise and reliable frequency is needed.

### SEC. 23-7 THE 555 TIMER

The 555 timer contains two comparators, an *RS* flip-flop, and an *n-p-n* transistor. It has an upper and lower trip point. When used in the monostable mode, the input triggers must fall below LTP to start the action. When the capacitor voltage slightly exceeds UTP, the discharge transistor turns on to discharge the capacitor.

### SEC. 23-8 ASTABLE OPERATION OF THE 555 TIMER

When used in the astable mode, the 555 timer produces a rectangular output whose duty cycle can be set between 50

and 100 percent. The capacitor charges between  $V_{CC}/3$  and  $2V_{CC}/3$ . When a control voltage is used, it changes UTP to  $V_{con}$ . This control voltage determines the frequency.

### SEC. 23-9 555 CIRCUITS

The 555 timer can be used to create time delays, alarms, and ramp outputs. It can also be used to build a pulse-width modulator by applying a modulating signal to the control input and a train of negative-going triggers to the trigger input. The 555 timer can also be used to build a pulse-position modulator by applying a modulating signal to the control input when the timer is in the astable mode.

### SEC. 23-10 THE PHASE-LOCKED LOOP

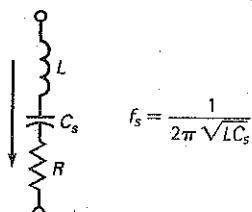
A PLL contains a phase detector, a dc amplifier, a low-pass filter, and a VCO. The phase detector produces a control voltage that is proportional to the phase difference between its two input signals. The amplified and filtered control voltage then changes the frequency of the VCO as needed to lock on to the input signal.

### SEC. 23-11 FUNCTION GENERATOR ICs

Function generator ICs have the ability to produce sine, square, triangle, pulse, and sawtooth waveforms. By connecting external resistors and capacitors, the output waveforms can be made to vary in frequency and amplitude. Special functions including AM/FM generation, voltage-to-frequency conversion, and frequency-shift keying can also be performed by these ICs.

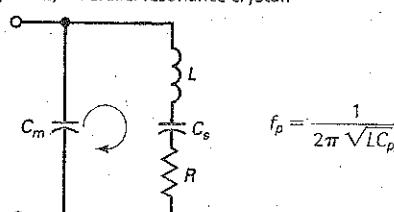
## Definitions

(23-20) Series resonance of crystal:



$$f_s = \frac{1}{2\pi\sqrt{LC_s}}$$

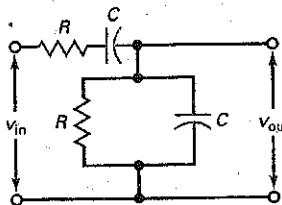
(23-22) Parallel resonance crystal:



$$f_p = \frac{1}{2\pi\sqrt{LC_p}}$$

## Derivations

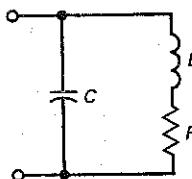
(23-1) and (23-2) Feedback factor and phase angle of lead-lag circuit:



$$B = \frac{1}{\sqrt{9 - (X_C/R - R/X_C)^2}}$$

$$\phi = \arctan \frac{X_C/R - R/X_C}{3}$$

(23-9) Exact resonant frequency:



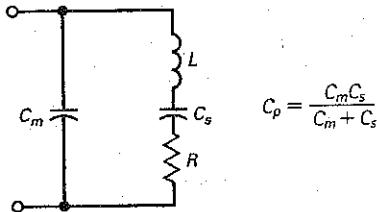
$$f_r = \frac{1}{2\pi\sqrt{LC}} \sqrt{\frac{Q^2}{Q^2 + 1}}$$

(23-19) Frequency of crystal:

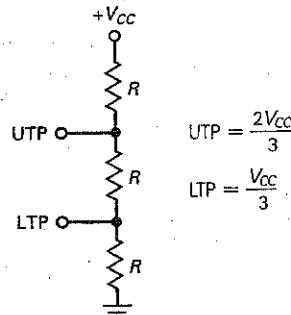


$$f = \frac{K}{t}$$

(23-21) Equivalent parallel capacitance:



(23-23) and (23-24) Trip points of 555 timer:



$$UTP = \frac{2V_{CC}}{3}$$

$$LTP = \frac{V_{CC}}{3}$$

## Student Assignments

1. An oscillator always needs an amplifier with
  - Positive feedback
  - Negative feedback
  - Both types of feedback
  - An LC tank circuit
2. The voltage that starts an oscillator is caused by
  - Ripple from the power supply
  - Noise voltage in resistors
  - The input signal from a generator
  - Positive feedback
3. The Wien-bridge oscillator is useful
  - At low frequencies
  - At high frequencies
  - With LC tank circuits
  - At small input signals
4. A lag circuit has a phase angle that is
  - Between 0 and +90°
  - Greater than 90°
  - Between 0 and -90°
  - The same as the input voltage
5. A coupling circuit is a
  - Lag circuit
  - Lead circuit
  - Lead-lag circuit
  - Resonant circuit
6. A lead circuit has a phase angle that is
  - Between 0 and +90°
  - Greater than 90°
  - Between 0 and -90°
  - The same as the input voltage
7. A Wien-bridge oscillator uses
  - Positive feedback
  - Negative feedback
  - Both types of feedback
  - An LC tank circuit
8. Initially, the loop gain of a Wien bridge is
  - 0
  - 1
  - Low
  - High
9. A Wien bridge is sometimes called a
  - Notch filter
  - Twin-T oscillator
  - Phase shifter
  - Wheatstone bridge
10. To vary the frequency of a Wien bridge, you can vary
  - One resistor
  - Three resistors
  - Two resistors
  - One capacitor

11. The phase-shift oscillator usually has
- Two lead or lag circuits
  - Three lead or lag circuits
  - A lead-lag circuit
  - A twin-T filter
12. For oscillations to start in a circuit, the loop gain must be greater than 1 when the phase shift around the loop is
- $90^\circ$
  - $270^\circ$
  - $180^\circ$
  - $360^\circ$
13. The most widely used *LC* oscillator is the
- Armstrong
  - Colpitts
  - Clapp
  - Hartley
14. Heavy feedback in an *LC* oscillator
- Prevents the circuit from starting
  - Causes saturation and cutoff
  - Produces maximum output voltage
  - Means that  $B$  is small
15. When  $Q$  decreases in a Colpitts oscillator, the frequency of oscillation
- Decreases
  - Remains the same
  - Increases
  - Becomes erratic
16. Link coupling refers to
- Capacitive coupling
  - Transformer coupling
  - Resistive coupling
  - Power coupling
17. The Hartley oscillator uses
- Negative feedback
  - Two inductors
  - A tungsten lamp
  - A tickler coil
18. To vary the frequency of an *LC* oscillator, you can vary
- One resistor
  - Two resistors
  - Three resistors
  - One capacitor
19. Of the following oscillators, the one with the most stable frequency is the
- Armstrong
  - Clapp
  - Colpitts
  - Hartley
20. The material that has the piezoelectric effect is
- Quartz
  - Rochelle salts
  - Tourmaline
  - All the above
21. Crystals have a very
- Low  $Q$
  - High  $Q$
  - Small inductance
  - Large resistance
22. The series and parallel resonant frequencies of a crystal are
- Very close together
  - Very far apart
  - Equal
  - Low frequencies
23. The kind of oscillator found in an electronic wristwatch is the
- Armstrong
  - Clapp
  - Colpitts
  - Quartz crystal
24. A monostable 555 timer has the following number of stable states:
- 0
  - 1
  - 2
  - 3
25. An astable 555 timer has the following number of stable states:
- 0
  - 1
  - 2
  - 3
26. The pulse width from a one-shot multivibrator increases when the
- Supply voltage increases
  - Timing resistor decreases
  - UTP decreases
  - Timing capacitance increases
27. The output waveform of a 555 timer is
- Sinusoidal
  - Triangular
  - Rectangular
  - Elliptical
28. The quantity that remains constant in a pulse-width modulator is
- Pulse width
  - Period
  - Duty cycle
  - Space
29. The quantity that remains constant in a pulse-position modulator is
- Pulse width
  - Period
  - Duty cycle
  - Space
30. When a PPL is locked on the input frequency, the VCO frequency
- Is less than  $f_0$
  - Is greater than  $f_0$
  - Equals  $f_0$
  - Equals  $f_0$
31. The bandwidth of the low-pass filter in a PPL determines the
- Capture range
  - Lock range
  - Free-running frequency
  - Phase difference
32. The output frequency of the XR-2206 can be varied with
- An external resistor
  - An external capacitor
  - An external voltage
  - Any of the above
33. FSK is a method of controlling the output
- Functions
  - Amplitude
  - Frequency
  - Phase

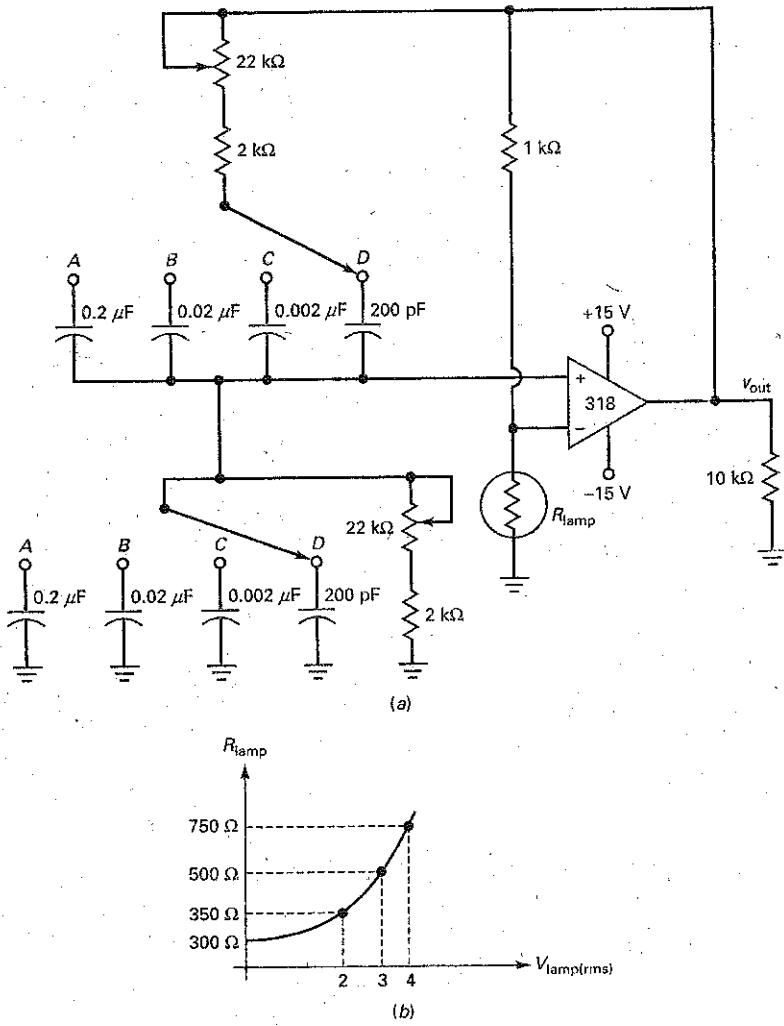
## Problems

### SEC. 23-2 THE WIEN-BRIDGE OSCILLATOR

23-1 The Wien-bridge oscillator of Fig. 23-53a uses a lamp with the characteristics of Fig. 23-53b. How much output voltage is there?

23-2 Position D in Fig. 23-53a is the highest frequency range of the oscillator. We can vary the frequency by using ganged rheostats. What are the minimum and maximum frequencies of oscillation on this range?

Figure 23-53



- 23-3 Calculate the minimum and maximum frequency of oscillation for each position of the ganged switch of Fig. 23-53a.

- 23-4 To change the output voltage of Fig. 23-53a to a value of 6 V rms, what change can you make?

- 23-5 In Fig. 23-53a, the cutoff frequency of the amplifier with negative feedback is at least 1 decade above the highest frequency of oscillation. What is the cutoff frequency?

### SEC. 23-3 OTHER RC OSCILLATORS

- 23-6 The twin-T oscillator of Fig. 23-12 has  $R = 10 \text{ k}\Omega$  and  $C = 0.01 \mu\text{F}$ . What is the frequency of oscillation?

- 23-7 If the values in Prob. 23-6 are doubled, what happens to the frequency of oscillation?

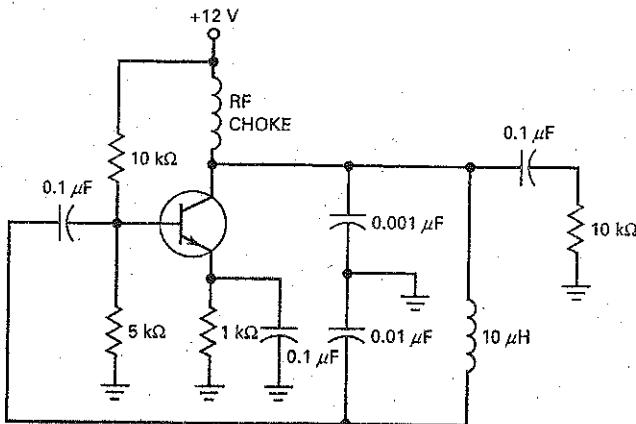
### SEC. 23-4 THE COLPITTS OSCILLATOR

- 23-8 What is the approximate value of the dc emitter current in Fig. 23-54? What is the dc voltage from the collector to the emitter?

- 23-9 What is the approximate frequency of oscillation in Fig. 23-54? The value of  $B$ ? For the oscillator to start, what is the minimum value of  $A_v$ ?

- 23-10 If the oscillator of Fig. 23-54 is redesigned to get a CB amplifier similar to the one in Fig. 23-18, what is the feedback fraction?

Figure 23-54



23-11 If the value of  $L$  is doubled in Fig. 23-54, what is the frequency of oscillation?

23-12 What can you do to the inductance of Fig. 23-54 to double the frequency of oscillation?

#### SEC. 23-5 OTHER LC OSCILLATORS

23-13 If 47 pF is connected in series with the 10 μH of Fig. 23-54, the circuit becomes a Clapp oscillator. What is the frequency of oscillation?

23-14 A Hartley oscillator like the one in Fig. 23-22 has  $L_1 = 1 \mu\text{H}$  and  $L_2 = 0.2 \mu\text{H}$ . What is the feedback fraction? The frequency of oscillation if  $C = 1000 \text{ pF}$ ? The minimum voltage gain needed to start oscillations?

23-15 An Armstrong oscillator has  $M = 0.1 \mu\text{H}$  and  $L = 3.3 \mu\text{H}$ . What is the feedback fraction? What is the minimum voltage gain needed to start the oscillations?

#### SEC. 23-6 QUARTZ CRYSTALS

23-16 A crystal has a fundamental frequency of 5 MHz. What is the approximate value of the first overtone frequency? The second overtone? The third?

23-17 A crystal has a thickness of  $t$ . If you reduce  $t$  by 1 percent, what happens to the frequency?

23-18 A crystal has these values:  $L = 1 \text{ H}$ ,  $C_s = 0.01 \text{ pF}$ ,  $R = 1 \text{ k}\Omega$ , and  $C_m = 20 \text{ pF}$ . What is the series resonant frequency? The parallel resonant frequency? The Q at each frequency?

#### SEC. 23-7 THE 555 TIMER

23-19 A 555 timer is connected for monostable operation. If  $R = 10 \text{ k}\Omega$  and  $C = 0.047 \mu\text{F}$ , what is the width of the output pulse?

23-20 In Fig. 23-34,  $V_{CC} = 10 \text{ V}$ ,  $R = 2.2 \text{ k}\Omega$ , and  $C = 0.2 \mu\text{F}$ . What is the minimum trigger voltage that produces an output pulse? What is the maximum capacitor voltage? What is the width of the output pulse?

#### SEC. 23-8 ASTABLE OPERATION OF THE 555 TIMER

23-21 An astable 555 timer has  $R_1 = 10 \text{ k}\Omega$ ,  $R_2 = 2 \text{ k}\Omega$ , and  $C = 0.0022 \mu\text{F}$ . What is the frequency?

23-22 The 555 timer of Fig. 23-37 has  $R_1 = 20 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$ , and  $C = 0.047 \mu\text{F}$ . What is the frequency of the output signal? What is the duty cycle?

#### SEC. 23-9 555 CIRCUITS

23-23 A pulse-width modulator like the one in Fig. 23-41 has  $V_{CC} = 10 \text{ V}$ ,  $R = 5.1 \text{ k}\Omega$ , and  $C = 1 \text{ nF}$ . The clock has a frequency of 10 kHz. If a modulating signal has a peak value of 1.5 V, what is the period of the output pulses? What is the quiescent pulse width? What are the minimum and maximum pulse widths? What are the minimum and maximum duty cycles?

23-24 A pulse-position modulator like the one in Fig. 23-42 has  $V_{CC} = 10 \text{ V}$ ,  $R_1 = 1.2 \text{ k}\Omega$ ,  $R_2 = 1.5 \text{ k}\Omega$ , and  $C = 4.7 \text{ nF}$ . What are the quiescent width and period of the output pulses? If the modulating signal has a peak value of 1.5 V, what are the minimum and maximum pulse widths? What is the space between pulses?

23-25 The ramp generator of Fig. 23-43 has a constant collector current of 0.5 mA. If  $V_{CC} = 10 \text{ V}$  and  $C = 47 \text{ nF}$ , what is the slope of the output ramp? What is its peak value? What is its duration?

#### SEC. 23-11 FUNCTION GENERATOR ICs

23-26 In Fig. 23-50,  $S_1$  is closed,  $R = 20 \text{ k}\Omega$ ,  $R_3 = 40 \text{ k}\Omega$ , and  $C = 0.1 \mu\text{F}$ . What is the output wave shape, frequency, and amplitude at pin 2?

23-27 In Fig. 23-50, with  $S_1$  open and  $R = 10 \text{ k}\Omega$ ,  $R_3 = 40 \text{ k}\Omega$ , and  $C = 0.01 \mu\text{F}$ , what is the output wave shape, frequency, and amplitude at pin 2?

23-28 In Fig. 23-51,  $R_1 = 2 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$ , and  $C = 0.1 \mu\text{F}$ . What is the output frequency and duty cycle at pin 11?

## Troubleshooting

- 23-29 Does the output voltage of the Wien-bridge oscillator (Fig. 23-53a) increase, decrease, or stay the same for each of these troubles?
- Lamp open
  - Lamp shorted
  - Upper potentiometer shorted
  - Supply voltages 20 percent low
  - $10\text{ k}\Omega$  open

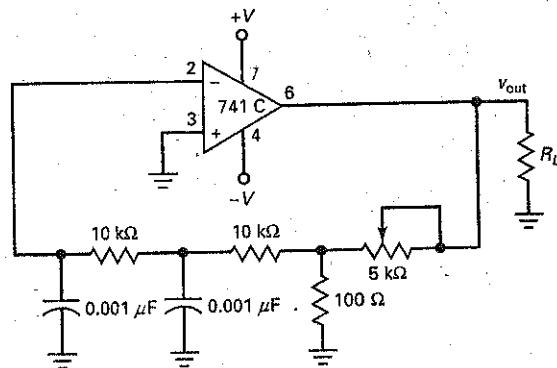
- 23-30 The Colpitts oscillator of Fig. 23-54 will not start. Name at least three possible troubles.

- 23-31 You have designed and built an amplifier. It does amplify an input signal, but the output looks fuzzy on an oscilloscope. When you touch the circuit, the fuzz disappears, leaving a perfect signal. What do you think the trouble is, and how would you try to eliminate it?

## Critical Thinking

- 23-32 Design a Wien-bridge oscillator similar to the one in Fig. 23-53a that meets these specifications: three decade frequency ranges covering 20 Hz to 20 kHz with an output voltage of 5 V rms.
- 23-33 Select a value of  $L$  in Fig. 23-54 to get an oscillation frequency of 2.5 MHz.
- 23-34 Figure 23-55 shows an op-amp phase-shift oscillator. If  $f_{2(\text{CL})} = 1\text{ kHz}$ , what is the loop phase shift at 15.9 kHz?
- 23-35 Design a 555 timer that free-runs at a frequency of 1 kHz and a duty cycle of 75 percent.

Figure 23-55



## Job Interview Questions

- How does a sinusoidal oscillator produce an output signal without an input signal?
- Which oscillator is used for many applications in the range of 5 Hz to 1 MHz? Why is the output sinusoidal rather than clipped?
- What type of oscillators are used most often for the range of 1 to 500 MHz?
- To produce oscillations of a precise and reliable frequency, what kind of oscillator is used most often?
- The 555 timer is used extensively in general applications as a timer. What is the difference between the circuit construction of a monostable and astable multivibrator?
- Draw a simple block diagram of a PLL and explain the basic idea of how it remains locked on to the incoming frequency.
- What does *pulse-width modulation* mean? What does *pulse-position modulation* mean? Illustrate your explanation by sketching waveforms.
- Assume that you are building a three-stage amplifier. When you test it, you discover that it is producing an output signal with no input signal. Explain how this is possible. What are some of the things you can do to eliminate the unwanted signal?
- How does an oscillator start if there is no input signal?

## Self-Test Answers

- |      |       |       |       |       |       |       |
|------|-------|-------|-------|-------|-------|-------|
| 1. a | 6. a  | 11. b | 16. b | 21. b | 26. d | 31. a |
| 2. b | 7. c  | 12. d | 17. b | 22. a | 27. c | 32. d |
| 3. a | 8. d  | 13. c | 18. d | 23. d | 28. b | 33. c |
| 4. c | 9. a  | 14. b | 19. b | 24. b | 29. d |       |
| 5. b | 10. b | 15. a | 20. d | 25. a | 30. d |       |

## Practice Problem Answers

⑥

23-1  $R = 14.9 \text{ k}\Omega$

23-2  $R_{\text{lamp}} = 1.5 \text{ k}\Omega$ ;  $I_{\text{lamp}} = 2 \text{ mA}$ ;  
 $V_{\text{out}} = 9 \text{ V rms}$

23-3  $L = 28 \mu\text{H}$

23-4  $C = 106 \text{ pF}$ ;  $f_r = 4 \text{ MHz}$

23-5  $f_s = 291 \text{ kHz}$ ;  $f_p = 292 \text{ kHz}$

23-6 LPT = 5 V; UTP = 10 V;  $W = 51.7 \text{ ms}$

23-8  $f = 136 \text{ Hz}$ ;  $D = 0.667$  or  $66.7\%$

23-9  $W = 3.42 \text{ ms}$ ;  $T = 4.4 \text{ ms}$ ;  
 $D = 0.778$ ;  $f = 227 \text{ Hz}$

23-10  $W_{\text{max}} = 146.5 \mu\text{s}$ ;  $D_{\text{max}} = 0.366$

23-12  $S = 5 \text{ V/ms}$ ;  $V = 8 \text{ V}$ ;  $T = 1.6 \text{ ms}$

23-13 Triangle waveform at pin 2.

Square wave at pin 11.

Both waveform frequencies are at 500 Hz

23-14  $f = 2.5 \text{ kHz}$ ;  $D = 0.5$

# 24

# Regulated Power Supplies

- With a zener diode, we can build simple voltage regulators. Now, we want to discuss the use of negative feedback to improve voltage regulation. The discussion begins with linear regulators, the kind in which the regulating device is operating in the linear region. We will discuss two types of linear regulators: the shunt type and the series type. This chapter concludes with switching regulators, the type in which the regulating device switches on and off to improve the power efficiency.

## Chapter Outline

- 24-1 Supply Characteristics
- 24-2 Shunt Regulators
- 24-3 Series Regulators
- 24-4 Monolithic Linear Regulators
- 24-5 Current Boosters
- 24-6 DC-to-DC Converters
- 24-7 Switching Regulators

## Objectives

After studying this chapter, you should be able to:

- Describe how shunt regulators work.
- Describe how series regulators work.
- Explain the operation and characteristics of IC voltage regulators.
- Explain how dc-to-dc converters work.
- State the purposes and functions of current-booster and current-limiting circuits.
- Describe the three basic topologies of switching regulators.

## Vocabulary

boost regulator	electromagnetic interference (EMI)	pass transistor
buck-boost regulator	foldback current limiting	phase splitter
buck regulator	headroom voltage	radio-frequency interference (RFI)
current booster	IC voltage regulator	short-circuit protection
current limiting	line regulation	shunt regulator
current-sensing resistor	load regulation	switching regulator
dc-to-dc converter	outboard transistor	thermal shutdown
dropout voltage		topology

## 24-1 Supply Characteristics

The quality of a power supply depends on its load regulation, line regulation, and output resistance. In this section, we will look at these characteristics because they are often used on data sheets to specify power supplies.

### Load Regulation

Figure 24-1 shows a bridge rectifier with a capacitor-input filter. Changing the load resistance will change the load voltage. If we reduce the load resistance, we get more ripple and additional voltage drop across the transformer windings and diodes. Because of this, an increase in load current always decreases the load voltage.

**Load regulation** indicates how much the load voltage changes when the load current changes. The definition for load regulation is:

$$\text{Load regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\% \quad (24-1)$$

where  $V_{NL}$  = load voltage with no load current

$V_{FL}$  = load voltage with full load current

With this definition,  $V_{NL}$  occurs when the load current is zero, and  $V_{FL}$  occurs when the load current is the maximum value for the design.

For instance, suppose that the power supply of Fig. 24-1 has these values:

$$V_{NL} = 10.6 \text{ V for } I_L = 0$$

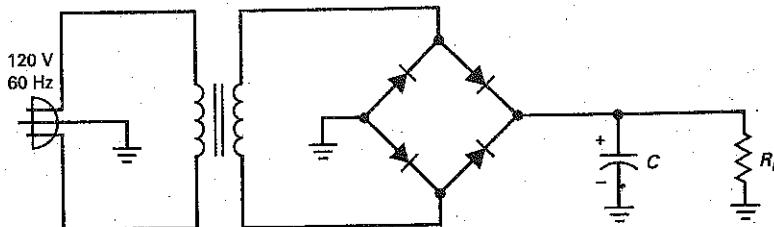
$$V_{FL} = 9.25 \text{ V for } I_L = 1 \text{ A}$$

Then, Eq. (24-1) gives:

$$\text{Load regulation} = \frac{10.6 \text{ V} - 9.25 \text{ V}}{9.25 \text{ V}} \times 100\% = 14.6\%$$

The smaller the load regulation, the better the power supply. For instance, a well-regulated power supply can have a load regulation of less than

Figure 24-1 Power supply with capacitor-input filter.



$$\text{Load regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

$V_{NL}$  = Load voltage with no load current

$V_{FL}$  = Load voltage with full load current

$$\text{Line regulation} = \frac{V_{HL} - V_{LL}}{V_{LL}} \times 100\%$$

$V_{LL}$  = Load voltage with low line voltage

$V_{HL}$  = Load voltage with high line voltage

1 percent. This means that the load voltage varies less than 1 percent over the full range of load current.

## Line Regulation

In Fig. 24-1, the input line voltage has a nominal value of 120 V. The actual voltage coming out of a power outlet may vary from 105 to 125 V rms, depending on the time of day, the locality, and other factors. Since the secondary voltage is directly proportional to the line voltage, the load voltage in Fig. 24-1 will change when line voltage changes.

Another way to specify the quality of a power supply is by its line regulation, defined as:

$$\text{Line regulation} = \frac{V_{HL} - V_{LL}}{V_{LL}} \times 100\% \quad (24-2)$$

where  $V_{HL}$  = load voltage with high line

$V_{LL}$  = load voltage with low line

For instance, suppose that the power supply of Fig. 24-1 has these measured values:

$V_{LL} = 9.2$  V for line voltage = 105 V rms

$V_{HL} = 11.2$  V for line voltage = 125 V rms

Then, Eq. (24-2) gives:

$$\text{Line regulation} = \frac{11.2 \text{ V} - 9.2 \text{ V}}{9.2 \text{ V}} \times 100\% = 21.7\%$$

As with load regulation, the smaller the line regulation, the better the power supply. For example, a well-regulated power supply can have a line regulation of less than 0.1 percent. This means that the load voltage varies less than 0.1 percent when the line voltage varies from 105 to 125 V rms.

## Output Resistance

The Thevenin or output resistance of a power supply determines the load regulation. If a power supply has a low output resistance, its load regulation will also be low. Here is one way to calculate the output resistance:

$$R_{TH} = \frac{V_{NL} - V_{FL}}{I_{FL}} \quad (24-3)$$

For example, here are the values given earlier for Fig. 24-1:

$V_{NL} = 10.6$  V for  $I_L = 0$

$V_{FL} = 9.25$  V for  $I_L = 1$  A

For this power supply, the output resistance is:

$$R_{TH} = \frac{10.6 \text{ V} - 9.25 \text{ V}}{1 \text{ A}} = 1.35 \Omega$$

Figure 24-2 shows a graph of load voltage versus load current. As we can see, the load voltage decreases when the load current increases. The change in load voltage ( $V_{NL} - V_{FL}$ ) divided by the change in current ( $I_{FL}$ ) equals the output resistance of the power supply. The output resistance is related to the slope of this graph. The more horizontal the graph, the lower the output resistance.

In Fig. 24-2, the maximum load current  $I_{FL}$  occurs when the load resistance is minimum. Because of this, an equivalent expression for load regulation is:

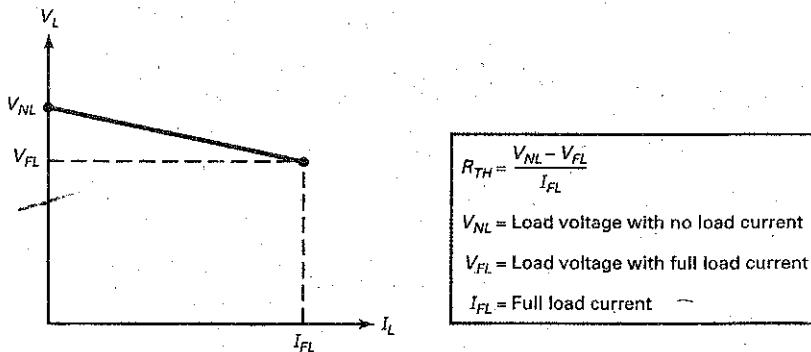
$$\text{Load regulation} = \frac{R_{TH}}{R_{L(\min)}} \times 100\% \quad (24-4)$$

## GOOD TO KNOW

Equation (24-3) can also be shown as

$$R_{TH} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times R_L$$

Figure 24-2 Graph of load voltage versus load current.



For example, if a power supply has an output resistance of  $1.5\ \Omega$  and the minimum load resistance is  $10\ \Omega$ , it has a load regulation of:

$$\text{Load regulation} = \frac{1.5\ \Omega}{10\ \Omega} \times 100\% = 15\%$$

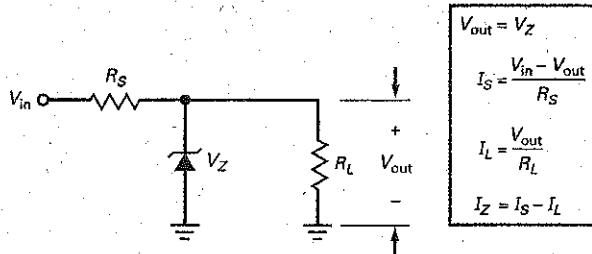
## 24-2 Shunt Regulators

The line regulation and load regulation of an unregulated power supply are too high for most applications. By using a voltage regulator between the power supply and the load, we can significantly improve the line and load regulation. A linear voltage regulator uses a device operating in the linear region to hold the load voltage constant. There are two fundamental types of linear regulators: the shunt type and the series type. With the shunt type, the regulating device is in parallel with the load.

### Zener Regulator

The simplest shunt regulator is the zener-diode circuit of Fig. 24-3. As discussed in Chap. 5, the zener diode operates in the breakdown region, producing an output voltage equal to the zener voltage. When the load current changes, the zener current increases or decreases to keep the current through  $R_S$  constant. With any shunt regulator, a change in load current is complemented by an opposing change in shunt current. If load current increases by 1 mA, the shunt current decreases by

Figure 24-3 Zener regulator is a shunt regulator.



## GOOD TO KNOW

In Fig. 24-3, it is important to remember that  $V_{out}$  changes slightly when the zener current changes. The change in  $V_{out}$  can be determined as  $\Delta V_{out} = \Delta I_Z R_Z$ , where  $R_Z$  represents the zener impedance.

1 mA. Conversely, if the load current decreases by 1 mA, the shunt current increases by 1 mA.

As shown in Fig. 24-3, the equation for the current through the series resistor is:

$$I_S = \frac{V_{in} - V_{out}}{R_S}$$

This series current equals the *input current* to the shunt regulator. When the input voltage is constant, the input current is almost constant when the load current changes. This is how you can recognize any shunt regulator. A change in load current has almost no effect on the input current.

A final point: In Fig. 24-3, the maximum load current with regulation occurs when the zener current is almost zero. Therefore, the maximum load current in Fig. 24-3 equals the input current. This is true for any shunt regulator. The maximum load current with a regulated output voltage is equal to the input current.

## Zener Voltage Plus One Diode Drop

At larger load currents, the load regulation of a zener regulator like Fig. 24-3 gets worse (increases) because the changing current through the zener resistance can change the output voltage significantly. One way to improve load regulation at larger load currents is to add a transistor to the circuit, as shown in Fig. 24-4. With this shunt regulator, the load voltage equals:

$$V_{out} = V_Z + V_{BE} \quad (24-5)$$

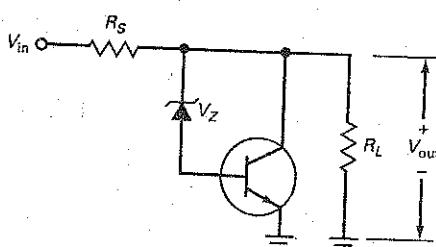
Here is how the circuit holds the output voltage constant: If the output voltage tries to increase, the increase is coupled through the zener diode to the base of the transistor. The larger base voltage produces more collector current through  $R_L$ . The larger voltage drop across  $R_L$  will offset most of the attempted increase in output voltage. The only noticeable change will be a slight increase in load voltage.

Conversely, if the output voltage tries to decrease, the voltage fed back to the base reduces the collector current and there is less voltage drop across  $R_L$ . Again, the attempted change in output voltage is offset by an opposing change in voltage across the series resistor. This time, the only noticeable change is a slight decrease in the output voltage.

## Higher Output Voltage

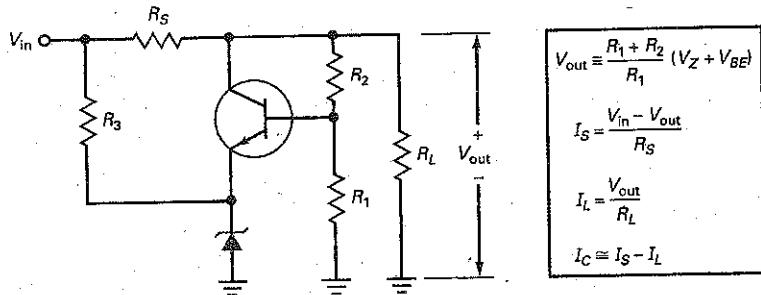
Figure 24-5 shows another shunt regulator. This circuit has the advantage of being able to use low-temperature-coefficient zener voltages (between 5 and 6 V). The regulated output voltage will have approximately the same temperature coefficient as the zener diode, but the voltage will be higher.

Figure 24-4 Improved shunt regulator.



$$\begin{aligned} V_{out} &= V_Z + V_{BE} \\ I_S &= \frac{V_{in} - V_{out}}{R_S} \\ I_L &= \frac{V_{out}}{R_L} \\ I_C &\approx I_S - I_L \end{aligned}$$

Figure 24-5 Shunt regulator with higher output.



The negative feedback is similar to that of the preceding regulator. Any attempted change in output voltage is fed back to the transistor, the output of which then almost completely offsets the attempted change in output voltage. The result is an output voltage that changes much less than it would without the negative feedback.

The base voltage is given by:

$$V_B \approx \frac{R_1}{R_1 + R_2} V_{out}$$

This is an approximation because it does not include the loading effect of the base current on the voltage divider. Usually, the base current is small enough to ignore. By solving the foregoing equation for output voltage, we get:

$$V_{out} \approx \frac{R_1 + R_2}{R_1} V_B$$

In Fig. 24-5, the base voltage is the sum of the zener voltage plus one  $V_{BE}$  drop:

$$V_B = V_Z + V_{BE}$$

Substituting this into the preceding equation gives:

$$V_{out} \approx \frac{R_1 + R_2}{R_1} (V_Z + V_{BE}) \quad (24-6)$$

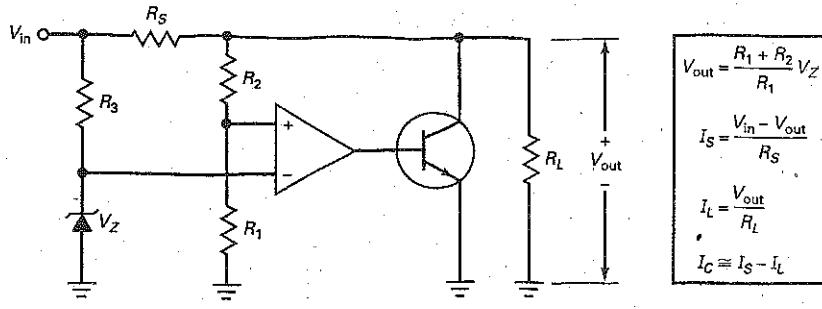
Figure 24-5 shows the equations for analyzing the circuit. The equation for collector current is an approximation because it does not include the current through the voltage divider ( $R_1$  and  $R_2$ ). To keep the efficiency of the regulator as high as possible, a designer normally makes  $R_1$  and  $R_2$  much larger than the load resistance. As a result, the current through the voltage divider is usually small enough to neglect in preliminary analysis.

The disadvantage of this regulator is that any changes in  $V_{BE}$  will translate into changes in the output voltage. Although useful in simpler applications, the circuit of Fig. 24-5 can be improved.

## Improved Regulation

One way to reduce the effect of  $V_{BE}$  on output voltage is with the shunt regulator of Fig. 24-6. The zener diode holds the inverting input of the op amp at a constant voltage. The voltage divider consisting of  $R_1$  and  $R_2$  samples the load voltage and returns a feedback voltage to the noninverting input. The output of the op amp drives the base of the shunt transistor. Because of the negative feedback, the output voltage is held almost constant in spite of line and load changes.

Figure 24-6 Shunt regulator with large negative feedback.



For instance, if the load voltage tries to increase, the feedback signal to the noninverting input increases. The output of the op amp drives the base harder and increases the collector current. The larger collector current through  $R_S$  produces a larger voltage across  $R_S$ , which offsets most of the attempted increase in load voltage. A similar correction occurs when the load voltage tries to decrease. In short, any attempted change in output voltage is offset by the negative feedback.

In Fig. 24-6, the high voltage gain of the op amp takes  $V_{BE}$  out of Eq. (24-6), (a situation similar to the one with active diode circuits discussed in Chap. 22). Because of this, the load voltage is given by:

$$V_{\text{out}} = \frac{R_1 + R_2}{R_1} V_Z \quad (24-7)$$

### Short-Circuit Protection

One advantage of shunt regulators is that they have built-in short-circuit protection. For instance, if we deliberately place a short circuit across the load terminals in Fig. 24-6, none of the components in the shunt regulator will be damaged. All that happens is that the input current increases to:

$$I_S = \frac{V_{\text{in}}}{R_S}$$

This current is not large enough to damage any of the components in a typical shunt regulator.

### Efficiency

One way to compare regulators of different designs is by using *efficiency*, defined as:

$$\text{Efficiency} = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100\% \quad (24-8)$$

where  $P_{\text{out}}$  is the load power ( $V_{\text{out}} I_L$ ) and  $P_{\text{in}}$  is the input power ( $V_{\text{in}} I_{\text{in}}$ ). The difference between  $P_{\text{in}}$  and  $P_{\text{out}}$  is  $P_{\text{reg}}$ , the power wasted in the regulator components:

$$P_{\text{reg}} = P_{\text{in}} - P_{\text{out}}$$

In the shunt regulators of Figs. 24-4 to 24-6, the power dissipation of  $R_S$  and the transistor account for most of the power wasted in the regulator.

## Example 24-1

Multisim

In Fig. 24-4,  $V_{in} = 15 \text{ V}$ ,  $R_S = 10 \Omega$ ,  $V_Z = 9.1 \text{ V}$ ,  $V_{BE} = 0.8 \text{ V}$ , and  $R_L = 40 \Omega$ . What are the values of output voltage, input current, the load current, and collector current?

**SOLUTION** With the equations of Fig. 24-4, we can calculate as follows:

$$V_{out} = V_Z + V_{BE} = 9.1 \text{ V} + 0.8 \text{ V} = 9.9 \text{ V}$$

$$I_S = \frac{V_{in} - V_{out}}{R_S} = \frac{15 \text{ V} - 9.9 \text{ V}}{10 \Omega} = 510 \text{ mA}$$

$$I_L = \frac{V_{out}}{R_L} = \frac{9.9 \text{ V}}{40 \Omega} = 248 \text{ mA}$$

$$I_C \approx I_S - I_L = 510 \text{ mA} - 248 \text{ mA} = 262 \text{ mA}$$

**PRACTICE PROBLEM 24-1** Repeat Example 24-1 with  $V_{in} = 12 \text{ V}$ ,  $V_Z = 6.8 \text{ V}$ .

## Example 24-2

The shunt regulator of Fig. 24-5 has these circuit values:  $V_{in} = 15 \text{ V}$ ,  $R_S = 10 \Omega$ ,  $V_Z = 6.2 \text{ V}$ ,  $V_{BE} = 0.81 \text{ V}$ , and  $R_L = 40 \Omega$ . If  $R_1 = 750 \Omega$  and  $R_2 = 250 \Omega$ , what are approximate values of output voltage, input current, load current, and collector current?

**SOLUTION** With the equations of Fig. 24-5:

$$\begin{aligned} V_{out} &\approx \frac{R_1 + R_2}{R_1} (V_Z + V_{BE}) \\ &= \frac{750 \Omega + 250 \Omega}{750 \Omega} (6.2 \text{ V} + 0.81 \text{ V}) = 9.35 \text{ V} \end{aligned}$$

The exact output voltage will be slightly higher than this because of the base current through  $R_2$ . The approximate currents are:

$$I_S = \frac{V_{in} - V_{out}}{R_S} = \frac{15 \text{ V} - 9.35 \text{ V}}{10 \Omega} = 565 \text{ mA}$$

$$I_L = \frac{V_{out}}{R_L} = \frac{9.35 \text{ V}}{40 \Omega} = 234 \text{ mA}$$

$$I_C \approx I_S - I_L = 565 \text{ mA} - 234 \text{ mA} = 331 \text{ mA}$$

**PRACTICE PROBLEM 24-2** With  $V_Z = 7.5 \text{ V}$ , repeat Example 24-2.

## Example 24-3

What is the approximate efficiency in the preceding example? How much power does the regulator dissipate?

**SOLUTION** The load voltage is approximately 9.35 V, and the load current is approximately 234 mA. The load power is:

$$P_{\text{out}} = V_{\text{out}} I_L = (9.35 \text{ V})(234 \text{ mA}) = 2.19 \text{ W}$$

In Fig. 24-5, the input current is:

$$I_{\text{in}} = I_S + I_3$$

In any well-designed shunt regulator,  $I_S$  is much greater than  $I_3$  to keep the efficiency high. Therefore, the input power is:

$$P_{\text{in}} = V_{\text{in}} I_{\text{in}} \approx V_{\text{in}} I_S = (15 \text{ V})(565 \text{ mA}) = 8.48 \text{ W}$$

The efficiency of the regulator is:

$$\text{Efficiency} = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100\% = \frac{2.19 \text{ W}}{8.48 \text{ W}} \times 100\% = 25.8\%$$

This efficiency is low compared to the efficiency of other regulators to be discussed (series regulators and switching regulators). Low efficiency is one of the disadvantages of a shunt regulator. Low efficiency occurs because of the power dissipation in the series resistor and the shunt transistor, which is:

$$P_{\text{reg}} = P_{\text{in}} - P_{\text{out}} \approx 8.48 \text{ W} - 2.19 \text{ W} = 6.29 \text{ W}$$

**PRACTICE PROBLEM 24-3** Repeat Example 24-3 with  $V_Z = 7.5 \text{ V}$ .

## Example 24-4

The shunt regulator of Fig. 24-6 has these circuit values:  $V_{\text{in}} = 15 \text{ V}$ ,  $R_S = 10 \Omega$ ,  $V_Z = 6.8 \text{ V}$ , and  $R_L = 40 \Omega$ . If  $R_1 = 7.5 \text{ k}\Omega$  and  $R_2 = 2.5 \text{ k}\Omega$ , what are approximate values of output voltage, the input current, the load current, and the collector current?

**SOLUTION** With the equations of Fig. 24-6:

$$V_{\text{out}} \approx \frac{R_1 + R_2}{R_1} V_Z = \frac{7.5 \text{ k}\Omega + 2.5 \text{ k}\Omega}{7.5 \text{ k}\Omega} (6.8 \text{ V}) = 9.07 \text{ V}$$

$$I_S = \frac{V_{\text{in}} - V_{\text{out}}}{R_S} = \frac{15 \text{ V} - 9.07 \text{ V}}{10 \Omega} = 593 \text{ mA}$$

$$I_L = \frac{V_{\text{out}}}{R_L} = \frac{9.07 \text{ V}}{40 \Omega} = 227 \text{ mA}$$

$$I_C \approx I_S - I_L = 593 \text{ mA} - 227 \text{ mA} = 366 \text{ mA}$$

**PRACTICE PROBLEM 24-4** Using Example 24-4, change  $V_{\text{in}}$  to 12 V and calculate the approximate transistor collector current. What is the approximate power dissipated by  $R_S$ ?

## Example 24-5

Calculate the maximum load currents for Examples 24-1, 24-2, and 24-4.

**SOLUTION** As discussed earlier, any shunt regulator has a maximum load current approximately equal to the current through  $R_S$ . Since we have already calculated  $I_S$  in Examples 24-1, 24-2, and 24-4, the maximum load currents are:

$$I_{\max} = 510 \text{ mA}$$

$$I_{\max} = 565 \text{ mA}$$

$$I_{\max} = 593 \text{ mA}$$

## Example 24-6

When the shunt regulator of Fig. 24-5 is built and tested, the following values are measured:  $V_{NL} = 9.91 \text{ V}$ ,  $V_{FL} = 9.81 \text{ V}$ ,  $V_{HL} = 9.94 \text{ V}$ , and  $V_{LL} = 9.79 \text{ V}$ . What is the load regulation? What is the line regulation?

**SOLUTION**

$$\text{Load regulation} = \frac{9.91 \text{ V} - 9.81 \text{ V}}{9.81 \text{ V}} \times 100\% = 1.02\%$$

$$\text{Line regulation} = \frac{9.94 \text{ V} - 9.79 \text{ V}}{9.79 \text{ V}} \times 100\% = 1.53\%$$

**PRACTICE PROBLEM 24-6** Repeat Example 24-6 using the following values:  $V_{NL} = 9.91 \text{ V}$ ,  $V_{FL} = 9.70 \text{ V}$ ,  $V_{HL} = 10.0 \text{ V}$ , and  $V_{LL} = 9.68 \text{ V}$ .

## 24-3 Series Regulators

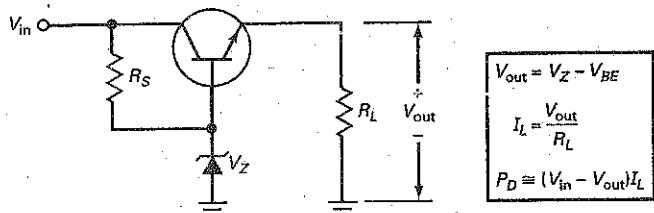
The disadvantage of a shunt regulator is its low efficiency, caused by large power losses in the series resistor and the shunt transistor. When efficiency is not important, shunt regulators may be used because they have the advantage of simplicity.

### Better Efficiency

When efficiency is important, a series regulator or a switching regulator may be used. A switching regulator is the most efficient of all voltage regulators. It has a full-load efficiency from about 75 to more than 95 percent. But a switching regulator is *noisy* because it produces **radio-frequency interference (RFI)**, caused by switching a transistor on and off at frequencies from about 10 to more than 100 kHz. Another disadvantage is that a switching regulator is the most complicated regulator to design and build.

On the other hand, the series regulator is *quiet* because its transistor always operates in the linear region. Furthermore, a series regulator is relatively simple to design and build compared to a switching regulator. Finally, a series

Figure 24-7 Zener follower is a series regulator.



regulator has full-load efficiencies from 50 to 70 percent, good enough for most applications in which the load power is less than 10 W.

Because of the foregoing reasons, the series regulator has emerged as the preferred choice for most applications when the load power is not too high. Its relative simplicity, quiet operation, and acceptable transistor power dissipation make the series regulator the natural choice for many applications. The remainder of this section discusses the series regulator.

### The Zener Follower

The simplest series regulator is the zener follower of Fig. 24-7. As discussed in Chap. 11, the zener diode operates in the breakdown region, producing a base voltage equal to the zener voltage. The transistor is connected as an emitter follower. Therefore, the load voltage equals:

$$V_{\text{out}} = V_z - V_{BE} \quad (24-9)$$

If the line voltage or load current changes, the zener voltage and base-emitter voltage will change only slightly. Because of this, the output voltage shows only small changes for large changes in line voltage or load current.

With a series regulator, the load current approximately equals the input current because the current through  $R_s$  is usually small enough to ignore in preliminary analysis. The transistor of a series regulator is called a pass transistor because all the load current passes through it.

A series regulator is more efficient than a shunt regulator because we have replaced the series resistor by the pass transistor. Now, the only significant power loss is in the transistor. Higher efficiency is one of the main reasons the series regulator is preferred to the shunt regulator when larger load currents are needed.

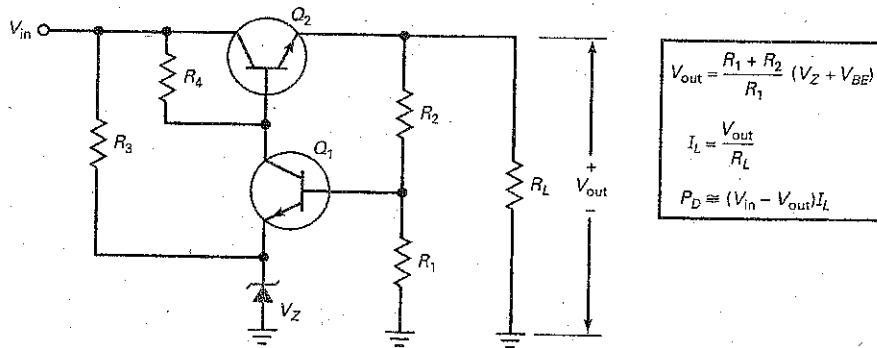
Recall that the shunt regulator has a constant input current when the load current changes. The series regulator is different because its input current is approximately equal to the load current. When the load current changes in a series regulator, the input current changes by the same amount. This is how you can recognize design variations of shunt and series regulators. In shunt regulators, the input current is constant when the load current changes, whereas in series regulators it changes when the load current changes.

### Two-Transistor Regulator

Figure 24-8 shows the two-transistor series regulator discussed in Chap. 11. If  $V_{\text{out}}$  tries to increase because of an increase in line voltage or an increase in load resistance, more voltage is fed back to the base of  $Q_1$ . This produces a larger  $Q_1$  collector current through  $R_4$  and less base voltage at  $Q_2$ . The reduced base voltage to the  $Q_2$  emitter follower almost offsets all the attempted increase in output voltage.

Similarly, if the output voltage tries to decrease because of a decrease in line voltage or a decrease in load resistance, there is less feedback voltage at the

Figure 24-8 Discrete series regulator.



base of  $Q_1$ . This produces more base voltage at  $Q_2$ , which increases the output voltage and almost completely offsets the attempted decrease in output voltage. The net effect is only a slight decrease in output voltage.

### Output Voltage

As discussed in Chap. 11, the output voltage in Fig. 24-8 is given by:

$$V_{\text{out}} = \frac{R_1 + R_2}{R_1} (V_Z + V_{BE}) \quad (24-10)$$

With a series regulator like Fig. 24-8, we can use a low zener voltage (5 to 6 V) where the temperature coefficient approaches zero. The output voltage has approximately the same temperature coefficient as the zener voltage.

### Headroom, Power Dissipation, and Efficiency

In Fig. 24-8, the headroom voltage is defined as the difference between the input and output voltage:

$$\text{Headroom voltage} = V_{\text{in}} - V_{\text{out}} \quad (24-11)$$

The current through the pass transistor of Fig. 24-8 equals:

$$I_C = I_L + I_2$$

where  $I_2$  is the current through  $R_2$ . To keep the efficiency high, a designer will make  $I_2$  much smaller than the full-load value of  $I_L$ . Therefore, we can ignore  $I_2$  at larger load currents and write:

$$I_C \approx I_L$$

At high load currents, the power dissipation in the pass transistor is given by the product of headroom voltage and load current:

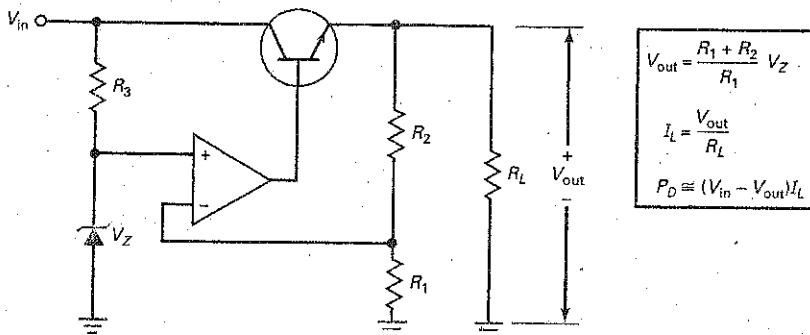
$$P_D \approx (V_{\text{in}} - V_{\text{out}}) I_L \quad (24-12)$$

The power dissipation in the pass transistor is very large in some series regulators. In this case, a large heat sink is used. Sometimes, a fan is needed to remove the excess heat inside enclosed equipment.

At full load current, most of the regulator power dissipation is in the pass transistor. Since the current in the pass transistor is approximately equal to the load current, the efficiency is given by:

$$\text{Efficiency} \approx \frac{V_{\text{out}}}{V_{\text{in}}} \times 100\% \quad (24-13)$$

**Figure 24-9** Series regulator with large negative feedback.



With this approximation, the best efficiency occurs when the output voltage is almost as large as the input voltage. It implies that the smaller the headroom voltage, the better the efficiency.

To improve the operation of the series regulator, a Darlington connection is often used for the pass transistor. This allows us to use a low-power transistor to drive a power transistor. The Darlington connection allows us to use larger values of  $R_1$  to  $R_4$  to improve the efficiency.

### Improved Regulation

Figure 24-9 shows how we can use an op amp to get better regulation. If the output voltage tries to increase, more voltage is fed back to the inverting input. This reduces the output of the op amp, the base voltage of the pass transistor, and the attempted increase in output voltage. If the output voltage tries to decrease, less voltage is fed back to the op amp, increasing the base voltage of the pass transistor, which almost completely offsets the attempted decrease in output voltage.

The derivation of output voltage is almost the same as for the regulator of Fig. 24-8, except that the high voltage gain of the op amp takes  $V_{BE}$  out of the equation. Because of this, the load voltage is given by:

$$V_{out} = \frac{R_1 + R_2}{R_1} V_Z \quad (24-14)$$

In Fig. 24-9, the op amp is being used as a noninverting amplifier with a closed-loop voltage gain of:

$$A_{v(CL)} = \frac{R_2}{R_1} + 1 \quad (24-15)$$

The input voltage being amplified is the zener voltage. This is why you sometimes see Eq. (24-14) written as:

$$V_{out} = A_{v(CL)} V_Z \quad (24-16)$$

For instance, if  $A_{v(CL)} = 2$  and  $V_Z = 5.6$  V, the output voltage will be 11.2 V.

### Current Limiting

Unlike the shunt regulator, the series regulator of Fig. 24-9 has no *short-circuit protection*. If we accidentally short the load terminals, the load current will try to approach infinity, which destroys the pass transistor. It may also destroy one or more diodes in the unregulated power supply that is driving the series regulator. To protect against an accidental short across the load, series regulators usually include some form of **current limiting**.

Figure 24-10 Series regulator with current limiting.

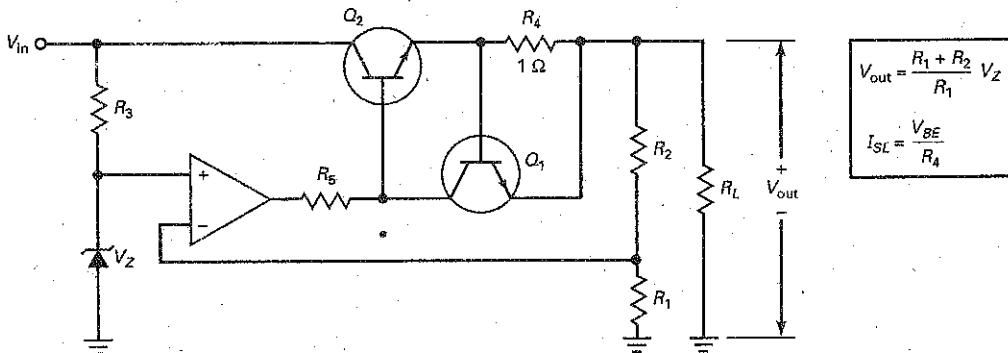


Figure 24-10 shows one way to limit the load current to safe values.  $R_4$  is a small resistor called a **current-sensing resistor**. For our discussion, we will use an  $R_4$  of 1  $\Omega$ . Since the load current has to pass through  $R_4$ , the current-sensing resistor produces the base-emitter voltage for  $Q_1$ .

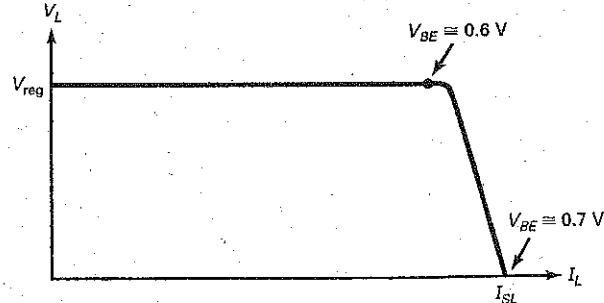
When the load current is less than 600 mA, the voltage across  $R_4$  is less than 0.6 V. In this case,  $Q_1$  is cut off and the regulator works as previously described. When the load current is between 600 and 700 mA, the voltage across  $R_4$  is between 0.6 and 0.7 V. This turns on  $Q_1$ . The collector current of  $Q_1$  flows through  $R_5$ . This decreases the base voltage to  $Q_2$ , which reduces the load voltage and the load current.

When the load is shorted,  $Q_1$  conducts heavily and brings the base voltage of  $Q_2$  down to approximately 1.4 V (two  $V_{\text{BE}}$  drops above ground). The current through the pass transistor is typically limited to 700 mA. It may be slightly more or less than this, depending on the characteristics of the two transistors.

Incidentally, resistor  $R_5$  is added to the circuit because the output impedance of the op amp is very low (75  $\Omega$  is typical). Without  $R_5$ , the current-sensing transistor does not have enough voltage gain to produce sensitive current limiting. A designer will select a value of  $R_5$  high enough to produce voltage gain in the current-sensing transistor, but not so high that it prevents the op amp from driving the pass transistor. Typical values of  $R_5$  are from a few hundred to a few thousand ohms.

Figure 24-11 summarizes the concept of current limiting. As an approximation, the graph shows 0.6 V as the voltage at which current limiting begins and 0.7 V as the voltage under shorted-load conditions. When the load current is

Figure 24-11 Graph of load voltage versus load current with simple current limiting.



## GOOD TO KNOW

In commercial regulated power supplies,  $R_4$  in Fig. 24-10 is often a variable resistor. This allows the user to set the maximum output current for a particular application.

small, the output voltage is regulated and has a value of  $V_{reg}$ . When  $I_L$  increases, the load voltage remains constant up to a  $V_{BE}$  of approximately 0.6 V. Beyond this point,  $Q_1$  turns on and current limiting sets in. Further increases in  $I_L$  decrease the load voltage, and regulation is lost. When the load is shorted, the load current is limited to a value of  $I_{SL}$ , the load current with shorted-load terminals.

When the load terminals are shorted in Fig. 24-10, the load current is given by:

$$I_{SL} = \frac{V_{BE}}{R_4} \quad (24-17)$$

where  $V_{BE}$  can be approximated as 0.7 V. For heavy load currents, the  $V_{BE}$  of the current-sensing transistor may be somewhat higher. We used an  $R_4$  of 1 Ω in our discussion. By changing the value of  $R_4$ , we can get current limiting to begin at any level. For instance, if  $R_4 = 10 \Omega$ , current limiting would start at approximately 60 mA with a shorted-load current of approximately 70 mA.

## Foldback Current Limiting

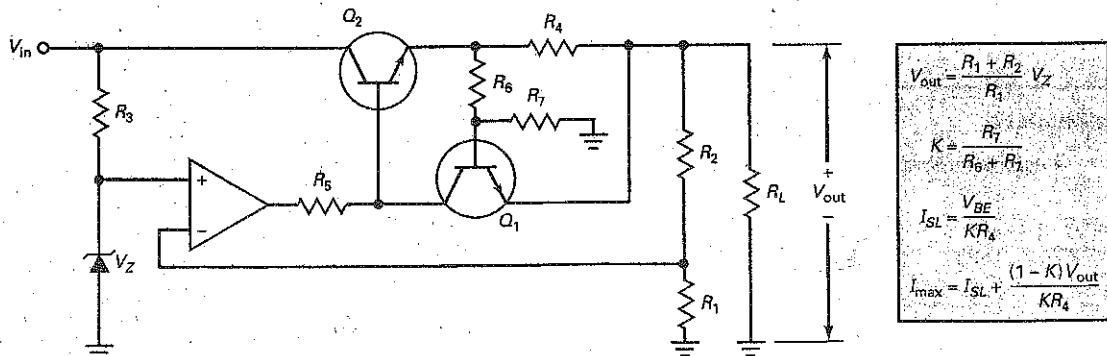
Current limiting is a big improvement because it will protect the pass transistor and rectifier diodes in case the load terminals are accidentally shorted. But it has the disadvantage of a large power dissipation in the pass transistor when the load terminals are shorted. With a short across the load, almost all the input voltage appears across the pass transistor.

To avoid excessive power dissipation in the pass transistor under shorted-load conditions, a designer can add foldback current limiting (Fig. 24-12). The voltage across the current-sensing resistor  $R_4$  is fed to a voltage divider ( $R_6$  and  $R_7$ ) whose output drives the base of  $Q_1$ . Over most of the load current range, the base voltage of  $Q_1$  is less than the emitter voltage, and  $V_{BE}$  is negative. This keeps  $Q_1$  cut off.

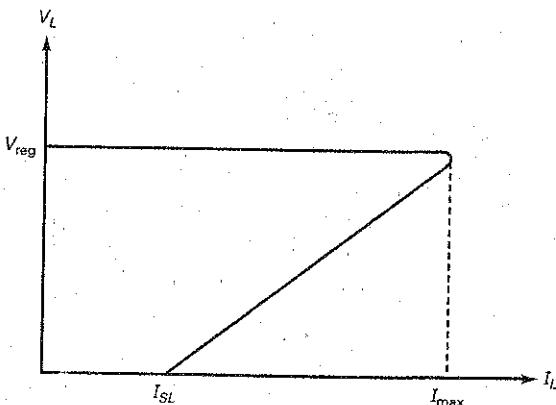
When the load current is high enough, however, the base voltage of  $Q_1$  becomes higher than the emitter voltage. When  $V_{BE}$  is between 0.6 and 0.7 V, current limiting starts. Beyond this point, further decreases in load resistance cause the current to fold back (decrease). As a result, the shorted-load current is much smaller than it would be without the foldback limiting.

Figure 24-13 shows how the output voltage varies with load current. The load voltage is constant up to a maximum value of  $I_{max}$ . At this point, current limiting starts. When the load resistance decreases further, the current folds back. When a short is across the load terminals, the load current equals  $I_{SL}$ . The main advantage of foldback current limiting is the reduced power dissipation in the pass transistor when the load terminals are accidentally shorted.

Figure 24-12 Series regulator with foldback current limiting.



**Figure 24-13** Graph of load voltage versus load current with foldback current limiting.



In Fig. 24-13, the power dissipation of the transistor under full-load conditions is:

$$P_D = (V_{\text{in}} - V_{\text{reg}})I_{\text{max}}$$

Under shorted-loaded conditions, the power dissipation is approximately:

$$P_D \approx V_{\text{in}}I_{SL}$$

Typically, a designer will use an  $I_{SL}$  that is two to three times smaller than  $I_{\text{max}}$ . By doing this, he or she can keep the power dissipation in the pass transistor down to the level it has under full-load conditions.

### Example 24-7

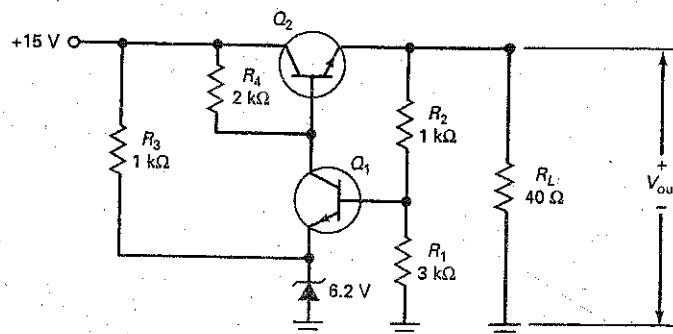
Multisim

Calculate the approximate output voltage in Fig. 24-14. What is the power dissipation in the pass transistor?

**SOLUTION** With the equations of Fig. 24-8:

$$V_{\text{out}} = \frac{3 \text{ k}\Omega + 1 \text{ k}\Omega}{3 \text{ k}\Omega} (6.2 \text{ V} + 0.7 \text{ V}) = 9.2 \text{ V}$$

**Figure 24-14** Example.



The transistor current is approximately the same as the load current:

$$I_C = \frac{9.2 \text{ V}}{40 \Omega} = 230 \text{ mA}$$

The transistor power dissipation is:

$$P_D = (15 \text{ V} - 9.2 \text{ V})(230 \text{ mA}) = 1.33 \text{ W}$$

**PRACTICE PROBLEM 24-7** In Fig. 24-14, change the input voltage to +12 V and  $V_Z$  to 5.6 V. Calculate  $V_{\text{out}}$  and  $P_D$ .

### Example 24-8

What is the approximate efficiency in Example 24-7?

**SOLUTION** The load voltage is 9.2 V, and the load current is 230 mA. The output power is:

$$P_{\text{out}} = (9.2 \text{ V})(230 \text{ mA}) = 2.12 \text{ W}$$

The input voltage is 15 V, and the input current is approximately 230 mA, the value of the load current. Therefore, the input power is:

$$P_{\text{in}} = (15 \text{ V})(230 \text{ mA}) = 3.45 \text{ W}$$

The efficiency is:

$$\text{Efficiency} = \frac{2.12 \text{ W}}{3.45 \text{ W}} \times 100\% = 61.4\%$$

We can also use Eq. (24-13) to calculate the efficiency of a series regulator:

$$\text{Efficiency} = \frac{V_{\text{out}}}{V_{\text{in}}} \times 100\% = \frac{9.2 \text{ V}}{15 \text{ V}} \times 100\% = 61.3\%$$

This is much better than 25.8 percent, the efficiency of the shunt regulator in Example 24-3. Typically, a series regulator has an efficiency about twice that of a shunt regulator.

**PRACTICE PROBLEM 24-8** Repeat Example 24-8 with  $V_{\text{in}} = +12 \text{ V}$  and  $V_Z = 5.6 \text{ V}$ .

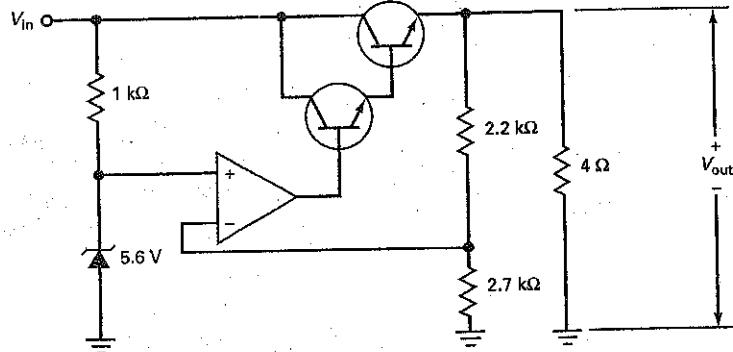
### Example 24-9

What is the approximate output voltage in Fig. 24-15? Why is a Darlington transistor used?

**SOLUTION** With the equations of Fig. 24-9:

$$V_{\text{out}} = \frac{2.7 \text{ k}\Omega + 2.2 \text{ k}\Omega}{2.7 \text{ k}\Omega} (5.6 \text{ V}) = 10.2 \text{ V}$$

**Figure 24-15** Series regulator with Darlington transistor.



The load current is:

$$I_L = \frac{10.2 \text{ V}}{4 \Omega} = 2.55 \text{ A}$$

If an ordinary transistor with a current gain of 100 were used for the pass transistor, the required base current would be:

$$I_B = \frac{2.55 \text{ A}}{100} = 25.5 \text{ mA}$$

This is too much output current for a typical op amp. If a Darlington transistor is used, the base current of the pass transistor is reduced to a much lower value. For instance, a Darlington transistor with a current gain of 1000 would require a base current of only 2.55 mA.

**PRACTICE PROBLEM 24-9** In Fig. 24-15, determine the output voltage if the zener voltage is changed to 6.2 V.

### Example 24-10

When the series regulator of Fig. 24-15 is built and tested, the following values are measured:  $V_{NL} = 10.16 \text{ V}$ ,  $V_{FL} = 10.15 \text{ V}$ ,  $V_{HL} = 10.16 \text{ V}$ , and  $V_{LL} = 10.07 \text{ V}$ . What is the load regulation? What is the line regulation?

#### SOLUTION

$$\text{Load regulation} = \frac{10.16 \text{ V} - 10.15 \text{ V}}{10.15 \text{ V}} \times 100\% = 0.0985\%$$

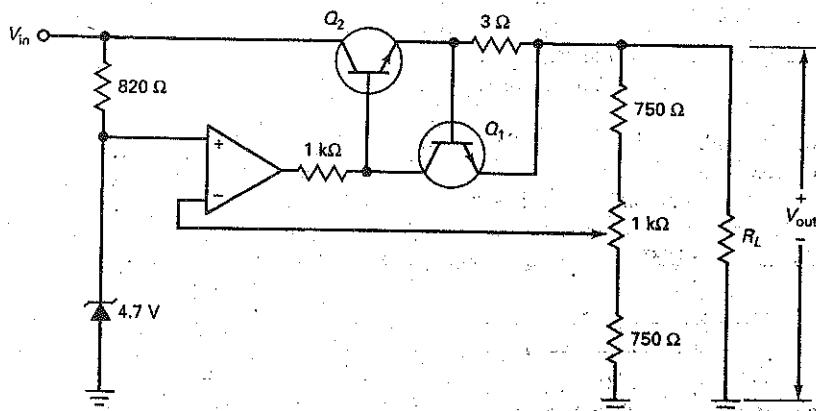
$$\text{Line regulation} = \frac{10.16 \text{ V} - 10.07 \text{ V}}{10.07 \text{ V}} \times 100\% = 0.894\%$$

This example shows how effective negative feedback is in reducing the effects of line and load changes. In both cases, the change in the regulated output voltage is less than 1 percent.

## Example 24-11

In Fig. 24-16,  $V_{in}$  can vary from 17.5 to 22.5 V. What is the maximum zener current? What are the minimum and maximum regulated output voltages? If the regulated output voltage is 12.5 V, what is the load resistance where current limiting starts? What is the approximate shorted-load current?

Figure 24-16 Example.



**SOLUTION** The maximum zener current occurs when the input voltage is 22.5 V:

$$I_Z = \frac{22.5 \text{ V} - 4.7 \text{ V}}{820 \Omega} = 21.7 \text{ mA}$$

The minimum regulated output voltage occurs when the wiper of the 1-kΩ potentiometer is all the way up. In this case,  $R_1 = 1750 \Omega$ ,  $R_2 = 750 \Omega$ , and the output voltage is:

$$V_{out} = \frac{1750 \Omega + 750 \Omega}{1750 \Omega} (4.7 \text{ V}) = 6.71 \text{ V}$$

The maximum regulated output voltage occurs when the wiper of the 1-kΩ potentiometer is all the way down. In this case,  $R_1 = 750 \Omega$ , and  $R_2 = 1750 \Omega$ , and the output voltage is:

$$V_{out} = \frac{750 \Omega + 1750 \Omega}{750 \Omega} (4.7 \text{ V}) = 15.7 \text{ V}$$

Current limiting starts when the voltage across the current-limiting resistor is approximately 0.6 V. In this case, the load current is:

$$I_L = \frac{0.6 \text{ V}}{3 \Omega} = 200 \text{ mA}$$

With an output voltage of 12.5 V, the load resistance where current limiting starts is approximately:

$$R_L = \frac{12.5 \text{ V}}{200 \text{ mA}} = 62.5 \Omega$$

With a short across the load terminals, the voltage across the current-sensing resistor is approximately 0.7 V, and the shorted-load current is:

$$I_{SL} = \frac{0.7 \text{ V}}{3 \Omega} = 233 \text{ mA}$$

**PRACTICE PROBLEM 24-11** Repeat Example 24-11 using a 3.9 V zener and a 2 Ω current-sensing resistor.

## 24-4 Monolithic Linear Regulators

There is a wide variety of linear IC voltage regulators with pin counts from 3 to 14. All are series regulators because the series regulator is more efficient than the shunt regulator. Some IC regulators are used in special applications in which external resistors can set the current limiting, the output voltage, and so on. By far, the most widely used IC regulators are those with only three pins: one for the unregulated input voltage, one for the regulated output voltage, and one for ground.

Available in plastic or metal packages, the three-terminal regulators have become extremely popular because they are inexpensive and easy to use. Aside from two optional bypass capacitors, three-terminal IC voltage regulators require no external components.

### Basic Types of IC Regulators

Most IC voltage regulators have one of these types of output voltage: fixed positive, fixed negative, or adjustable. IC regulators with fixed positive or negative outputs are factory-trimmed to get different fixed voltages with magnitudes from about 5 to 24 V. IC regulators with an adjustable output can vary the regulated output voltage from less than 2 to more than 40 V.

IC regulators are also classified as standard, low-power, and low dropout. Standard IC regulators are designed for straightforward and noncritical applications. With heat sinks, a standard IC regulator can have a load current of more than 1 A.

If load currents up to 100 mA are adequate, *low-power IC regulators* are available in TO-92 packages, the same size used for small-signal transistors like the 2N3904. Since these regulators do not require heat sinking, they are convenient and easy to use.

The **dropout voltage** of an IC regulator is defined as the minimum headroom voltage needed for regulation. For instance, standard IC regulators have a dropout voltage of 2 to 3 V. This means that the input voltage has to be at least 2 to 3 V greater than the regulated output voltage for the chip to regulate to specifications. In applications in which 2 to 3 V of headroom is not available, *low dropout IC regulators* can be used. These regulators have typical dropout voltages of 0.15 V for a load current of 100 mA and 0.7 V for a load current of 1 A.

### On-Card Regulation versus Single-Point Regulation

With *single-point regulation*, we need to build a power supply with a large voltage regulator and then distribute the regulated voltage to all the different *cards* (printed-circuit boards) in the system. This creates problems. To begin with, the single regulator has to provide a large load current equal to the sum of all the card currents. Second, noise or other **electromagnetic interference (EMI)** can be induced on the connecting wires between the regulated power supply and the cards.

Because IC regulators are inexpensive, electronic systems that have many cards often use *on-card regulation*. This means that each card has its own three-terminal regulator to supply the voltage used by the components on that card. By using on-card regulation, we can deliver an unregulated voltage from a power supply to each card and have a local IC regulator take care of regulating the voltage for its card. This eliminates the problems of the large load current and noise pickup associated with single-point regulation.

### Load and Line Regulation Redefined

Up to now, we have used the original definitions for load and line regulation. Manufacturers of fixed IC regulators prefer to specify the change in load voltage

for a range of load and line conditions. Here are definitions for load and line regulation used on the data sheets of fixed regulators:

Load regulation =  $\Delta V_{out}$  for a range of load current

Line regulation =  $\Delta V_{out}$  for a range of input voltage

For instance, the LM7815 is an IC regulator that produces a fixed positive output voltage of 15 V. The data sheet lists the typical load and line regulation as follows:

Load regulation = 12 mV for  $I_L = 5 \text{ mA}$  to  $1.5 \text{ A}$

Line regulation = 4 mV for  $V_{in} = 17.5 \text{ V}$  to  $30 \text{ V}$

The load regulation will depend on the conditions of measurement. The foregoing load regulation is for  $T_J = 25^\circ\text{C}$  and  $V_{in} = 23 \text{ V}$ . Similarly, the foregoing line regulation is for  $T_J = 25^\circ\text{C}$  and  $I_L = 500 \text{ mA}$ . In each case, the junction temperature of the device is  $25^\circ\text{C}$ .

## The LM7800 Series

The LM78XX series (where XX = 05, 06, 08, 10, 12, 15, 18, or 24) is typical of the three-terminal voltage regulators. The 7805 produces an output of +5 V, the 7806 produces +6 V, the 7808 produces +8 V, and so on, up to the 7824, which produces an output of +24 V.

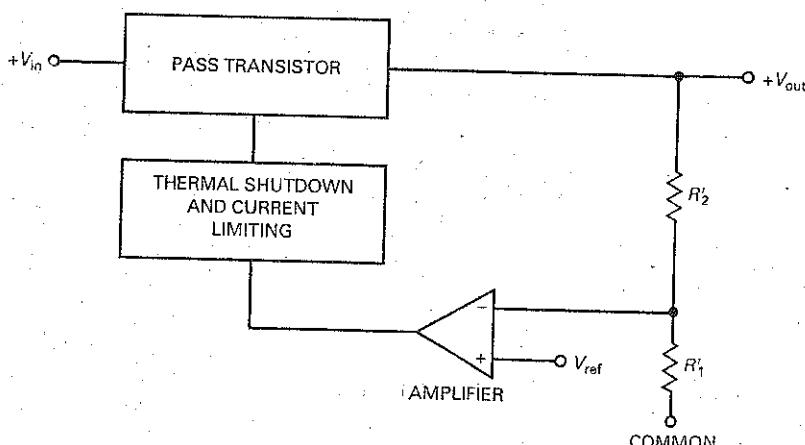
Figure 24-17 shows the functional block diagram for the 78XX series. A built-in reference voltage  $V_{ref}$  drives the noninverting input of an amplifier. The voltage regulation is similar to our earlier discussion. A voltage divider consisting of  $R'_1$  and  $R'_2$  samples the output voltage and returns a feedback voltage to the inverting input of a high-gain amplifier. The output voltage is given by:

$$V_{out} = \frac{R'_1 + R'_2}{R'_1} V_{ref}$$

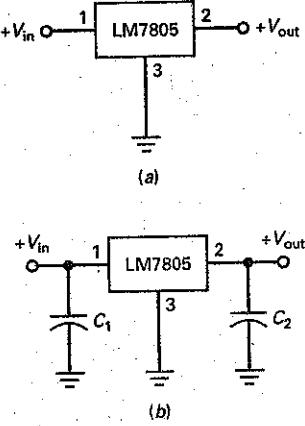
In this equation, the reference voltage is equivalent to the zener voltage in our earlier discussions. The primes attached to  $R'_1$  and  $R'_2$  indicate that these resistors are inside the IC itself, rather than being external resistors. These resistors are factory-trimmed to get the different output voltages (5 to 24 V) in the 78XX series. The tolerance of the output voltage is  $\pm 4$  percent.

The LM78XX includes a pass transistor that can handle 1 A of load current, provided that adequate heat sinking is used. Also included are thermal shutdown and current limiting. Thermal shutdown means that the chip will shut

Figure 24-17: Functional block diagram of three-terminal IC regulator.



**Figure 24-18** (a) Using a 7805 for voltage regulation; (b) input capacitor prevents oscillations and output capacitor improves frequency response.



itself off when the internal temperature becomes too high, around 175°C. This is a precaution against excessive power dissipation, which depends on the ambient temperature, type of heat sinking, and other variables. Because of thermal shutdown and current limiting, devices in the 78XX series are almost indestructible.

## Fixed Regulator

Figure 24-18a shows an LM7805 connected as a fixed voltage regulator. Pin 1 is the input, pin 2 is the output, and pin 3 is ground. The LM7805 has an output voltage of +5 V and a maximum load current over 1 A. The typical load regulation is 10 mV for a load current between 5 mA and 1.5 A. The typical line regulation is 3 mV for an input voltage of 7 to 25 V. It also has a ripple rejection of 80 dB, which means that it will reduce the input ripple by a factor of 10,000. With an output resistance of approximately  $0.01 \Omega$ , the LM7805 is a very stiff voltage source to all loads within its current rating.

When an IC is more than 6 in from the filter capacitor of the unregulated power supply, the inductance of the connecting wire may produce oscillations inside the IC. This is why manufacturers recommend using a bypass capacitor  $C_1$  on pin 1 (Fig. 24-18b). To improve the transient response of the regulated output voltage, a bypass capacitor  $C_2$  is sometimes used on pin 2. Typical values for either bypass capacitor are from 0.1 to  $1 \mu\text{F}$ . The data sheet of the 78XX series suggests  $0.22 \mu\text{F}$  for the input capacitor and  $0.1 \mu\text{F}$  for the output capacitor.

Any regulator in the 78XX series has a dropout voltage of 2 to 3 V, depending on the output voltage. This means that the input voltage must be at least 2 to 3 V greater than the output voltage. Otherwise, the chip stops regulating. Also, there is a maximum input voltage because of excessive power dissipation. For instance, the LM7805 will regulate over an input range of approximately 8 to 20 V. The data sheet for the 78XX series gives the minimum and maximum input voltages for the other preset output voltages.

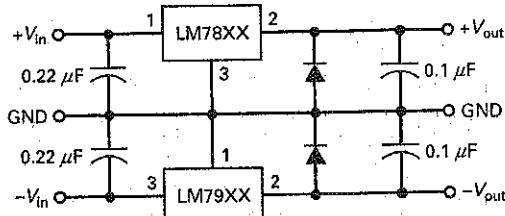
## The LM79XX Series

The LM79XX series is a group of negative voltage regulators with preset voltages of -5, -6, -8, -10, -12, -15, -18, or -24 V. For instance, an LM7905 produces a regulated output voltage of -5 V. At the other extreme, an LM7924 produces an output of -24 V. With the LM79XX series, the load-current capability is over 1 A with adequate heat sinking. The LM79XX series is similar to the 78XX series and includes current limiting, thermal shutdown, and excellent ripple rejection.

## Regulated Dual Supplies

By combining an LM78XX and an LM79XX, as shown in Fig. 24-19, we can regulate the output of a dual supply. The LM78XX regulates the positive output, and the LM79XX handles the negative output. The input capacitors prevent oscillations,

**Figure 24-19** Using the LM78XX and LM79XX for dual outputs.



and the output capacitors improve transient response. The manufacturer's data sheet recommends the addition of two diodes to ensure that both regulators can turn on under all operating conditions.

An alternative solution for dual supplies is to use a dual-tracking regulator. This is an IC that contains a positive and a negative regulator in a single IC package. When adjustable, this type of IC can vary the dual supplies with a single variable resistor.

## Adjustable Regulators

A number of IC regulators (LM317, LM337, LM338, and LM350) are adjustable. These have maximum load currents from 1.5 to 5 A. For instance, the LM317 is a three-terminal positive voltage regulator that can supply 1.5 A of load current over an adjustable output range of 1.25 to 37 V. The ripple rejection is 80 dB. This means that the input ripple is 10,000 smaller at the output of the IC regulator.

Again, manufacturers redefine the load and line regulation to suit the characteristics of the IC regulator. Here are definitions for load and line regulation used on the data sheets of adjustable regulators:

Load regulation = Percent change in  $V_{out}$  for a range in load current

Line regulation = Percent change in  $V_{out}$  per volt of input change

For instance, the data sheet of an LM317 lists these typical load and line regulations:

Load regulation = 0.3% for  $I_L$  = 10 mA to 1.5 A

Line regulation = 0.02% per volt

Since the output voltage is adjustable between 1.25 and 37 V, it makes sense to specify the load regulation as a percent. For instance, if the regulated voltage is adjusted to 10 V, the foregoing load regulation means that the output voltage will remain within 0.3 percent of 10 V (or 30 mV) when the load current changes from 10 mA to 1.5 A.

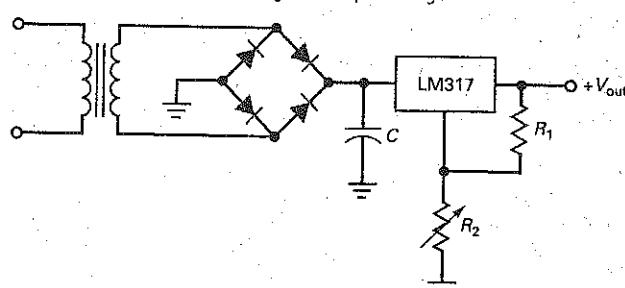
The line regulation is 0.02 percent per volt. This means that the output voltage changes only 0.02 percent for each volt of input change. If the regulated output is set at 10 V and the input voltage increases by 3 V, the output voltage will increase by 0.06 percent, equivalent to 60 mV.

Figure 24-20 shows an unregulated supply driving an LM317 circuit. The data sheet of an LM317 gives this formula for output voltage:

$$V_{out} = \frac{R_1 + R_2}{R_1} V_{ref} + I_{ADJ} R_2 \quad (24-18)$$

In this equation,  $V_{ref}$  has a value of 1.25 V and  $I_{ADJ}$  has a typical value of 50  $\mu$ A. In Fig. 24-20,  $I_{ADJ}$  is the current flowing through the middle pin (the one between the input and the output pins). Because this current can change with temperature, load current, and other factors, a designer usually makes the first term in Eq. (24-18)

Figure 24-20 Using an LM317 to regulate output voltage.



## GOOD TO KNOW

In Fig. 24-20, the value of the filter capacitor  $C$  has to be large enough to ensure that  $V_{in}$  remains at least 2 or 3 V higher than  $V_{out}$  when  $V_{out}$  and  $I_L$  are both at their maximum values. This means that  $C$  has to be a very large filter capacitor.

much greater than the second. This is why we can use the following equation for all preliminary analyses of an LM317:

$$V_{\text{out}} \approx \frac{R_1 + R_2}{R_1} (1.25 \text{ V}) \quad (24-19)$$

### Ripple Rejection

The ripple rejection of an IC voltage regulator is high, from about 65 to 80 dB. This is a tremendous advantage because it means that we do not have to use bulky *LC* filters in the power supply to minimize the ripple. All we need is a capacitor-input filter that reduces the peak-to-peak ripple to about 10 percent of the unregulated voltage out of the power supply.

For instance, the LM7805 has a typical ripple rejection of 80 dB. If a bridge rectifier and a capacitor-input filter produce an unregulated output voltage of 10 V with a peak-to-peak ripple of 1 V, we can use an LM7805 to produce a regulated output voltage of 5 V with a peak-to-peak ripple of only 0.1 mV. Eliminating bulky *LC* filters in an unregulated power supply is a bonus that comes with IC voltage regulators.

### Regulator Table

Table 24-1 lists some widely used IC regulators. The first group, the LM78XX series, is for fixed positive output voltages from 5 to 24 V. With heat sinking, these

**Table 24-1** Typical Parameters of Popular IC Voltage Regulators at 25°C

Number	$V_{\text{out}}$ , V	$I_{\text{max}}$ , A	Load Reg., mV	Line Reg., mV	Rip Rej., dB	Dropout, V	$R_{\text{out}}$ , mΩ	$I_{SL}$ , A
LM7805	5	1.5	10	3	80	2	8	2.1
LM7806	6	1.5	12	5	75	2	9	0.55
LM7808	8	1.5	12	6	72	2	16	0.45
LM7812	12	1.5	12	4	72	2	18	1.5
LM7815	15	1.5	12	4	70	2	19	1.2
LM7818	18	1.5	12	15	69	2	22	0.20
LM7824	24	1.5	12	18	66	2	28	0.15
LM78L05	5	100 mA	20	18	80	1.7	190	0.14
LM78L12	12	100 mA	30	30	80	1.7	190	0.14
LM2931	3 to 24	100 mA	14	4	80	0.3	200	0.14
LM7905	-5	1.5	10	3	80	2	8	2.1
LM7912	-12	1.5	12	4	72	2	18	1.5
LM7915	-15	1.5	12	4	70	2	19	1.2
LM317	1.2 to 37	1.5	0.3%	0.02%/V	80	2	10	2.2
LM337	-1.2 to -37	1.5	0.3%	0.01%/V	77	2	10	2.2
LM338	1.2 to 32	5	0.3%	0.02%/V	75	2.7	5	8

regulators can produce a load current up to 1.5 A. Load regulation is between 10 and 12 mV. Line regulation is between 3 and 18 mV. Ripple rejection is best at the lowest voltage (80 dB) and worst at the high voltage (66 dB). The dropout voltage is 2 V for the entire series. Output resistance increases from 8 to 28 mΩ between the lowest and highest output voltage.

The LM78L05 and LM78L12 are low-power versions of their standard counterparts, the LM7805 and LM7812. These *low-power IC regulators* are available in TO-92 packages, which do not require heat sinking. As shown in Table 24-1, the LM78L05 and LM78L12 can produce load currents up to 100 mA.

The LM2931 is included as an example of a low-dropout regulator. This adjustable regulator can produce output voltages between 3 and 24 V with a load current up to 100 mA. Notice that the dropout voltage is only 0.3 V, which means that the input voltage need be only 0.3 V greater than the regulated output voltage.

The LM7905, LM7912, and LM7915 are widely used negative regulators. Their parameters are similar to those of their LM78XX counterparts. The LM317 and LM337 are adjustable positive and negative regulators that can deliver load currents up to 1.5 A. Finally, the LM338 is an adjustable positive regulator that can produce a load voltage between 1.2 and 32 V with a load current up to 5 A.

All the regulators listed in Table 24-1 have *thermal shutdown*. This means that the regulator will cut off the pass transistor and shut down the operation if the chip temperature becomes too high. When the device cools off, it will attempt to restart. If whatever caused the excessive temperature has been removed, the regulator will function normally. If not, it will shut down again. Thermal shutdown is an advantage that monolithic regulators offer for safe operation.

## Example 24-12

Multisim

What is the load current in Fig. 24-21? What is the output ripple?

**SOLUTION** The LM7812 produces a regulated output voltage of +12 V. Therefore, the load current is:

$$I_L = \frac{12 \text{ V}}{100 \Omega} = 120 \text{ mA}$$

We can calculate the peak-to-peak input ripple with the equation given in Chap. 4:

$$V_R = \frac{I_L}{fC} = \frac{120 \text{ mA}}{(120 \text{ Hz})(1000 \mu\text{F})} = 1 \text{ V}$$

Figure 24-21 Example.

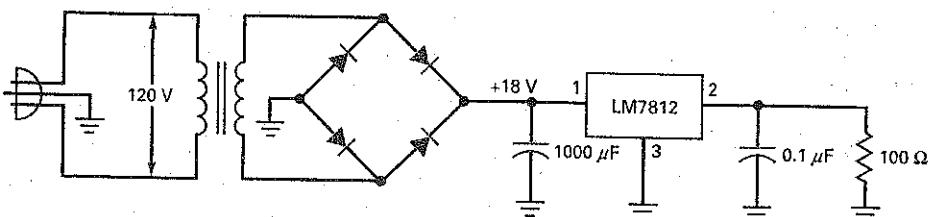


Table 24-1 shows a typical ripple rejection of 72 dB for the LM7812. If we convert 72 dB mentally (60 dB + 12 dB), we get approximately 4000. With a scientific calculator, the exact ripple rejection is:

$$RR = \text{antilog } \frac{72 \text{ dB}}{20} = 3981$$

The peak-to-peak output ripple is approximately:

$$V_R = \frac{1 \text{ V}}{4000} = 0.25 \text{ mV}$$

**PRACTICE PROBLEM 24-12** Repeat Example 24-12 using an LM7815 voltage regulator and a 2000  $\mu\text{F}$  capacitor.

### Example 24-13

If  $R_1 = 2 \text{ k}\Omega$  and  $R_2 = 22 \text{ k}\Omega$  in Fig. 24-20, what is the output voltage? If  $R_2$  is increased to  $46 \text{ k}\Omega$ , what is the output voltage?

**SOLUTION** With Eq. (24-19):

$$V_{\text{out}} = \frac{2 \text{ k}\Omega + 22 \text{ k}\Omega}{2 \text{ k}\Omega} (1.25 \text{ V}) = 15 \text{ V}$$

When  $R_2$  is increased to  $46 \text{ k}\Omega$ , the output voltage increases to:

$$V_{\text{out}} = \frac{2 \text{ k}\Omega + 46 \text{ k}\Omega}{2 \text{ k}\Omega} (1.25 \text{ V}) = 30 \text{ V}$$

**PRACTICE PROBLEM 24-13** In Fig. 24-20, what is the output voltage if  $R_1 = 330 \Omega$  and  $R_2 = 2 \text{ k}\Omega$ ?

### Example 24-14

The LM7805 can regulate to specifications with an input voltage between 7.5 and 20 V. What is the maximum efficiency? What is the minimum efficiency?

**SOLUTION** The LM7805 produces an output of 5 V. With Eq. (24-13), the maximum efficiency is:

$$\text{Efficiency} \approx \frac{V_{\text{out}}}{V_{\text{in}}} \times 100\% = \frac{5 \text{ V}}{7.5 \text{ V}} \times 100\% = 67\%$$

This high efficiency is possible only because the headroom voltage is approaching the dropout voltage.

On the other hand, the minimum efficiency occurs when the input voltage is maximum. For this condition, the headroom voltage is maximum and the power dissipation in the pass transistor is maximum. The minimum efficiency is:

$$\text{Efficiency} \approx \frac{5 \text{ V}}{20 \text{ V}} \times 100\% = 25\%$$

Since the unregulated input voltage is usually somewhere between the extremes in input voltage, the efficiency we can expect with an LM7805 is in the range of 40 to 50 percent.

## 24-5 Current Boosters

Even though the 78XX regulators of Table 24-1 have a maximum load current of 1.5 A, the data sheet shows many parameters measured at 1 A. For instance, a load current of 1 A is used for measuring line regulation, ripple rejection, and output resistance. For this reason, we will establish 1 A as a practical limit on the load current when using a 78XX device.

### The Outboard Transistor

One way to get more load current is to use a **current booster**. The idea is similar to what we did to boost the output current of an op amp. Recall that we used the op amp to supply the base current for an external transistor, which produced a much larger output current.

Figure 24-22 shows how we can use an external transistor to boost the output current. The external transistor, called an **outboard transistor**, is a power transistor.  $R_1$  is a current-sensing resistor of  $0.7\ \Omega$ . Notice that we are using  $0.7\ \Omega$  instead of  $0.6\ \Omega$ . We are using  $0.7\ \Omega$  because a power transistor needs more base voltage than does a small-signal transistor (used in the previous discussion).

When the current is less than 1 A, the voltage across the current-sensing resistor is less than 0.7 V and the transistor is off. When the load current is greater than 1 A, the transistor turns on and supplies almost all the load current above 1 A. Here is why: When the load current increases, the current through the 78XX increases slightly. This produces more voltage across the current-sensing resistor, which makes the outboard transistor conduct more heavily.

Each time we increase the load current, the current through the 78XX device increases slightly, producing more voltage across the current-sensing resistor. In this way, the outboard transistor produces the bulk of any increase in load current above 1 A, with only a small increase in the current through the 78XX.

For large load currents, the base current in the outboard transistor becomes large. The 78XX chip has to supply this base current in addition to its share of load current. When the large base current becomes a problem, a designer may use a Darlington connection for the outboard transistor. In this case, the current-sensing voltage is approximately 1.4 V, which means that  $R_1$  should be increased to approximately  $1.4\ \Omega$ .

### Short-Circuit Protection

Figure 24-23 shows how to add short-circuit protection to the circuit. We are using two current-sensing resistors, one to drive the outboard transistor  $Q_2$  and a second to turn on  $Q_1$  for short-circuit protection. For this discussion, 1 A is where  $Q_2$  conducts, and 10 A is where  $Q_1$  provides short-circuit protection.

Figure 24-22 Outboard transistor increases load current.

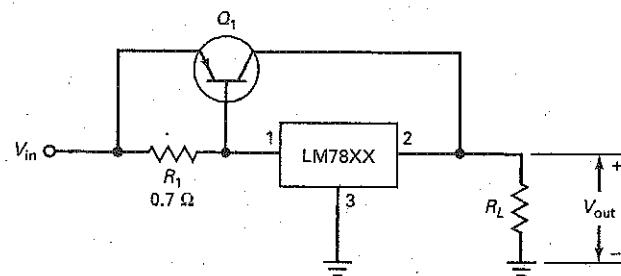
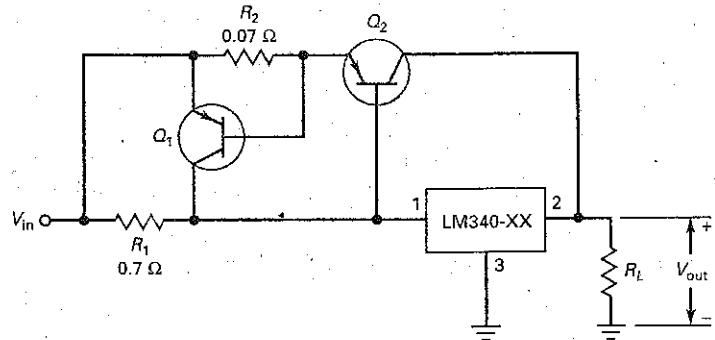


Figure 24-23 Outboard transistor with current limiting.



Here is how the circuit works: When the load current is greater than 1 A, the voltage across  $R_1$  is greater than 0.7 V. This turns on the outboard transistor  $Q_2$ , which supplies all the load current above 1 A. The outboard current has to pass through  $R_2$ . Since  $R_2$  is only 0.07 Ω, the voltage across it is less than 0.7 V as long as the outboard current is less than 10 A.

When the outboard current is 10 A, the voltage across  $R_2$  is:

$$V_2 = (10 \text{ A})(0.07 \Omega) = 0.7 \text{ V}$$

This means that the current-limiting transistor  $Q_1$  is on the verge of turning on. When the outboard current is greater than 10 A,  $Q_1$  conducts heavily. Since the collector current of  $Q_1$  passes through the 78XX, the device overheats and produces thermal shutdown.

A final point: Using an outboard transistor does not improve the efficiency of a series regulator. With typical headroom voltages, the efficiency is around 40 to 50 percent. To get higher efficiency with large headroom voltages, we have to use a fundamentally different approach to voltage regulation.

## 24-6 DC-to-DC Converters

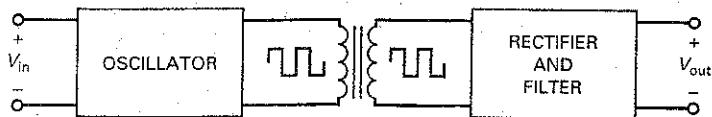
Sometimes we want to convert a dc voltage of one value to a dc voltage of another value. For instance, if we have a system with a positive supply of +5 V, we can use a **dc-to-dc converter** to convert this +5 V to an output of +15 V. Then we would have two supply voltages for our system: +5 and +15 V.

DC-to-dc converters are very efficient. Because they switch transistors on and off, transistor power dissipation is greatly reduced. Typical efficiencies are from 65 to 85 percent. This section discusses unregulated dc-to-dc converters. The next section is about regulated dc-to-dc converters that use pulse-width modulation. These dc-to-dc converters are usually called **switching regulators**.

### Basic Idea

In a typical unregulated dc-to-dc converter, the input dc voltage is applied to a square-wave oscillator. The peak-to-peak value of the square wave is proportional to the input voltage. The square wave is used to drive the primary winding of a transformer, as shown in Fig. 24-24. The higher the frequency, the smaller the transformer and filter components. If the frequency is too high, however, it is difficult to produce a square wave with vertical transitions. Usually, the frequency of the square wave is between 10 and 100 kHz.

**Figure 24-24** Functional block diagram of an unregulated dc-to-dc converter.



To improve the efficiency, a special kind of transformer is used in more expensive dc-to-dc converters. The transformer has a toroidal core with a rectangular hysteresis loop. This produces a secondary voltage that is a square wave. The secondary voltage can then be rectified and filtered to get a dc output voltage. By selecting a different turns ratio, we can step the secondary voltage up or down. This way, we can build dc-to-dc converters that step the dc input voltage either up or down.

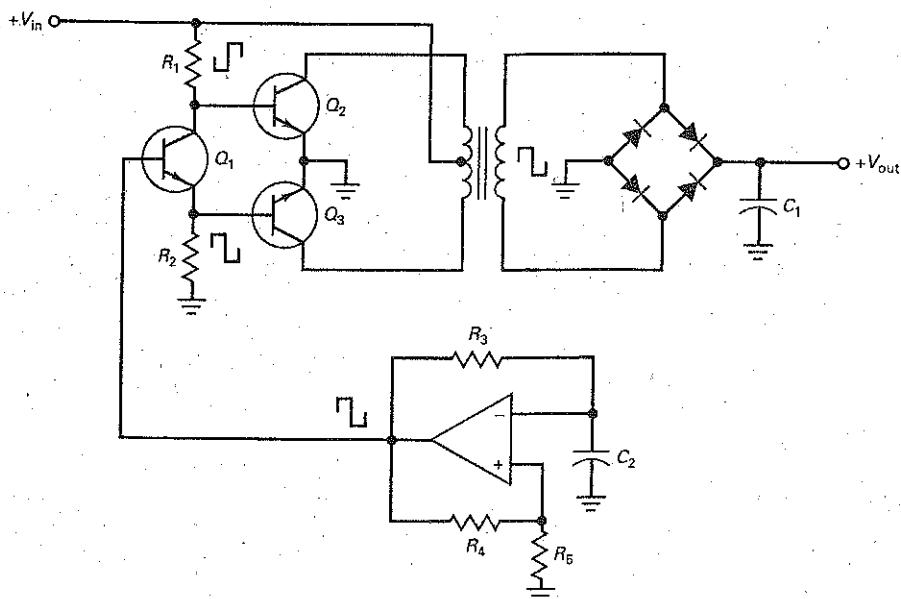
One common dc-to-dc conversion is +5 to  $\pm 15$  V. In digital systems, +5 V is a standard supply voltage for most ICs. But linear ICs, like op amps, may require  $\pm 15$  V. In a case like this, you may find a low-power dc-to-dc converter converting an input +5 V dc to dual outputs of  $\pm 15$  V dc.

### One Possible Design

There are many ways to design a dc-to-dc converter, depending on whether bipolar junction or power FETs are used, the switching frequency, whether the input voltage is stepped up or down, and so on. Figure 24-25 shows a design example that uses bipolar junction power transistors. Here is how it works: A relaxation oscillator produces a square wave whose frequency is set by  $R_3$  and  $C_2$ . This frequency is in the kilohertz range; a value like 20 kHz would be typical.

The square wave drives a phase splitter  $Q_1$ , a circuit that produces two equal-magnitude and out-of-phase square waves. These square waves are the

**Figure 24-25** An unregulated dc-to-dc converter.



input to class B push-pull switching transistors  $Q_2$  and  $Q_3$ . Transistor  $Q_2$  conducts during one half cycle, and  $Q_3$  during the other half cycle. The primary current in the transformer is a square wave. This induces a square wave across the secondary winding, as previously described.

The square wave of voltage out of the secondary winding drives a bridge rectifier and a capacitor-input filter. Because the signal is a rectified square wave in kilohertz, it is easy to filter. The final output is a dc voltage at some level different from the input.

### Commercial DC-to-DC Converters

In Fig. 24-25, notice that the output of the dc-to-dc converter is unregulated. This is typical of inexpensive dc-to-dc converters. Unregulated dc-to-dc converters are commercially available with efficiencies of about 65 to more than 85 percent. For instance, inexpensive dc-to-dc converters are available for converting +5 to  $\pm 12$  V at 375 mA, +5 to +9 V dc at 200 mA, +12 to  $\pm 5$  V at 250 mA, and so on. All of these converters require a fixed input voltage because they do not include voltage regulation. Also, they use switching frequencies between 10 and 100 kHz. Because of this, they include RFI shielding. Some of the units have an MTBF of 200,000 hr. (Note: MTBF stands for "mean time between failure.")

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## 24-7 Switching Regulators

A *switching regulator* falls into the general class of dc-to-dc converters because it will convert a dc input voltage to another dc output voltage, either lower or higher. But the switching regulator also includes voltage regulation, typically pulse-width modulation controlling the on-off time of the transistor. By changing the duty cycle, a switching regulator can hold the output voltage constant under varying line and load conditions.

### The Pass Transistor

In a series regulator the power dissipation of the pass transistor approximately equals the headroom voltage times the load current:

$$P_D = (V_{in} - V_{out})I_L$$

If the headroom voltage equals the output voltage, the efficiency is approximately 50 percent. For instance, if 10 V is the input to a 7805, the load voltage is 5 V and the efficiency is around 50 percent.

Three-terminal series regulators are very popular because they are easy to use and fill most of our needs when the load power is less than about 10 W. When the load power is 10 W and the efficiency is 50 percent, the power dissipation of the pass transistor is also 10 W. This represents a lot of wasted power, as well as heat created inside the equipment. Around load powers of 10 W, heat sinks get very bulky and the temperature of enclosed equipment may rise to objectionable levels.

### Switching the Pass Transistor On and Off

The ultimate solution to the problem of low efficiency and high equipment temperature is the switching regulator, briefly described earlier. With this type of regulator, the pass transistor is switched between cutoff and saturation. When the transistor is cut off, the power dissipation is virtually zero. When the transistor is saturated, the power dissipation is still very low because  $V_{CE(sat)}$  is much less than the headroom voltage in a series regulator. As mentioned earlier, switching regulators can have efficiencies from about 75 to more than 95 percent. Because of the high efficiency and small size, switching regulators have become widely used.

**Table 24-2 | Switching-Regulator Topologies**

Topology	Step	Choke	Transformer	Diodes	Transistors	Power, W	Complexity
Buck	Down	Yes	No	1	1	0-150	Low
Boost	Up	Yes	No	1	1	0-150	Low
Buck-boost	Both	Yes	No	1	1	0-150	Low
Flyback	Both	No	Yes	1	1	0-150	Medium
Half-forward	Both	Yes	Yes	1	1	0-150	Medium
Push-pull	Both	Yes	Yes	2	2	100-1000	High
Half bridge	Both	Yes	Yes	4	2	100-500	High
Full bridge	Both	Yes	Yes	4	4	400-2000	Very high

## Topologies

Topology is a term often used in switching-regulator literature. It is the design technique or fundamental layout of a circuit. Many topologies have evolved for switching regulators because some are better suited to an application than others.

Table 24-2 shows the topologies used for switching regulators. The first three are the most basic. They use the fewest number of parts and can deliver load power up to about 150 W. Because their complexity is low, they are widely used, especially with IC switching regulators.

When transformer isolation is preferred, the flyback and the half-forward topologies can be used for load power up to 150 W. When the load power is from 150 to 2000 W, the push-pull, half bridge, and full bridge topologies are used. Since the last three topologies use more components, the circuit complexity is high.

## Buck Regulator

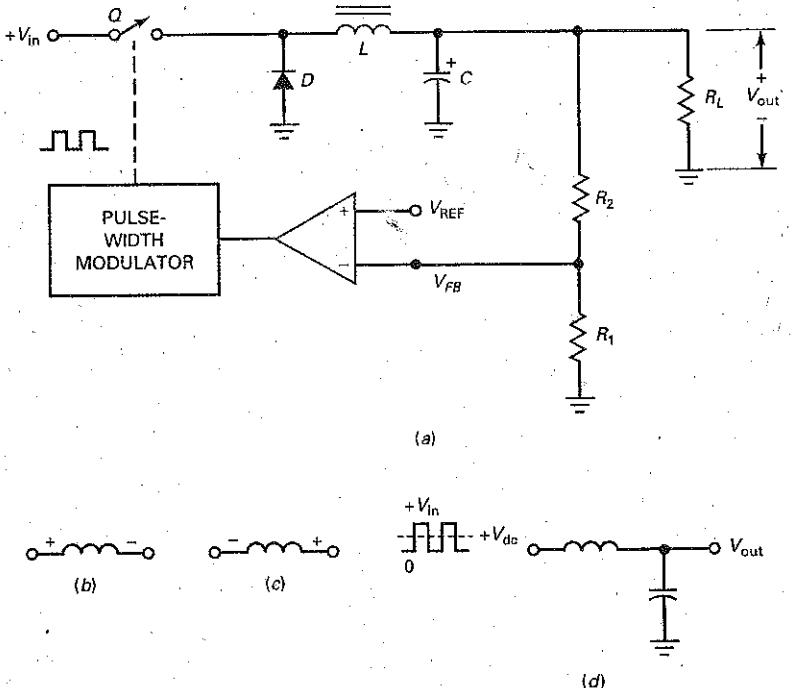
Figure 24-26a shows a **buck regulator**, the most basic topology for switching regulators. A buck regulator always steps the voltage down. A transistor, either a bipolar junction or a power FET, is used as the switching device. A rectangular signal out of the pulse-width modulator closes and opens the switch. A comparator controls the duty cycle of the pulses. For instance, the pulse-width modulator may be a one-shot multivibrator with a comparator driving the control input. As discussed in Chap. 23 with a monostable 555 timer, an increase in control voltage increases the duty cycle.

When the pulse is high, the switch is closed. This reverse-biases the diode, so that all the input current flows through the inductor. This current creates a magnetic field around the inductor. The amount of stored energy in the magnetic field is given by:

$$\text{Energy} = 0.5Li^2 \quad (24-20)$$

The current through the inductor also charges the capacitor and supplies current to the load. While the switch is closed, the voltage across the inductor has the plus-minus polarity shown in Fig. 24-26b. As the current through the inductor increases, more energy is stored in the magnetic field.

**Figure 24-26** (a) Buck regulator; (b) polarity with closed switch; (c) polarity with open switch; (d) choke-input filter passes dc value to output.



When the pulse goes low, the switch opens. At this instant, the magnetic field around the inductor starts collapsing and induces a reverse voltage across the inductor, as shown in Fig. 24-26c. This reverse voltage is called the *inductive kick*. Because of the inductive kick, the diode is forward biased and the current through the inductor continues to flow in the same direction. At this time, the inductor is returning its stored energy to the circuit. In other words, the inductor acts like a source and continues supplying current for the load.

Current flows through the inductor until the inductor returns all its energy to the circuit (discontinuous mode) or until the switch closes again (continuous mode), whichever comes first. In either case, the capacitor will also source load current during part of the time that the switch is open. This way, the ripple across the load is minimized.

The switch is being continuously closed and opened. The frequency of this switching can be from 10 to more than 100 kHz. (Some IC regulators switch at more than 1 MHz.) The current through the inductor is always in the same direction, passing through either the switch or the diode at different times in the cycle.

With a stiff input voltage and an ideal diode, a rectangular voltage waveform appears at the input to the *choke-input filter* (see Fig. 24-26d). If you recall from Chap. 4, the output of a choke-input filter equals the dc or average value of the input to the filter. The average value is related to the duty cycle and is given by:

$$V_{out} = DV_{in} \quad (24-21)$$

The larger the duty cycle, the larger the dc output voltage.

When the power is first turned on, there is no output voltage and no feedback voltage from the \$R\_1-R\_2\$ voltage divider. Therefore, the comparator output is very large and the duty cycle approaches 100 percent. As the output voltage builds

up, however, the feedback voltage  $V_{FB}$  reduces the comparator output, which reduces the duty cycle. At some point, the output voltage reaches an equilibrium value at which the feedback voltage produces a duty cycle that gives the same output voltage.

Because of the high gain of the comparator, the virtual short between the input terminals of the comparator means that:

$$V_{FB} \approx V_{REF}$$

From this, we can derive this expression for the output voltage:

$$V_{out} = \frac{R_1 + R_2}{R_1} V_{REF} \quad (24-22)$$

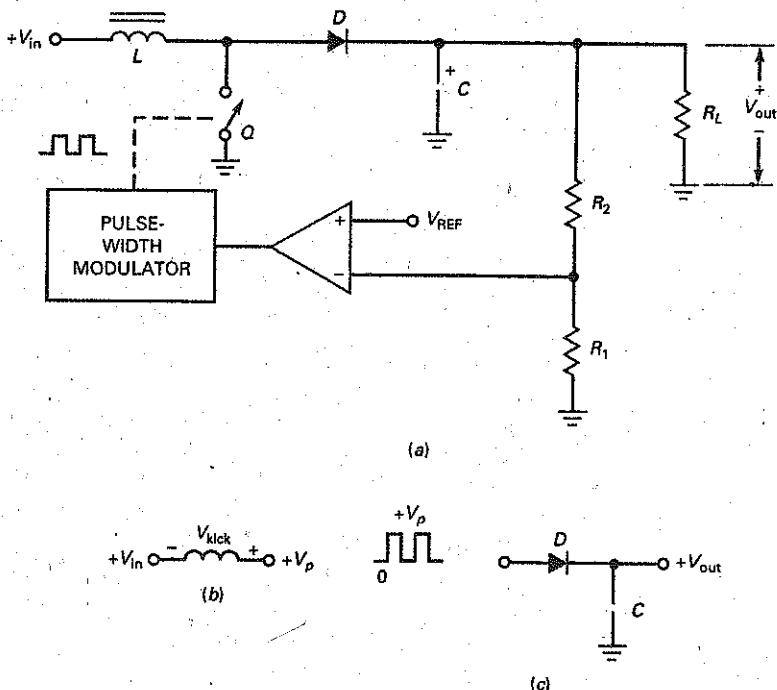
After equilibrium sets in, any attempted change in the output voltage, whether caused by line or load changes, will be almost entirely offset by the negative feedback. For instance, if the output voltage tries to increase, the feedback voltage reduces the comparator output. This reduces the duty cycle and the output voltage. The net effect is only a slight increase in output voltage, much less than without the negative feedback.

Similarly, if the output voltage tries to decrease because of a line or load change, the feedback voltage is smaller and the comparator output is larger. This increases the duty cycle and produces a larger output voltage that offsets almost all the attempted decrease in output voltage.

## Boost Regulator

Figure 24-27a shows a boost regulator, another basic topology for switching regulators. A boost regulator always steps the voltage up. The theory of operation is

**Figure 24-27** (a) Boost regulator; (b) kick voltage adds to input when switch is open; (c) capacitor-input filter produces output voltage equal to peak input.



similar to that for a buck regulator in some ways but very different in others. For instance, when the pulse is high, the switch is closed and energy is stored in the magnetic field, as previously described.

When the pulse goes low, the switch opens. Again, the magnetic field around the inductor collapses and induces a reverse voltage across the inductor, as shown in Fig. 24-27b. Notice that the input voltage now adds to the inductive kick. This means that the peak voltage on the right end of the inductor is:

$$V_p = V_{in} + V_{kick} \quad (24-23)$$

The inductive kick depends on how much energy is stored in the magnetic field. Stated another way,  $V_{kick}$  is proportional to the duty cycle.

With a stiff input voltage, a rectangular voltage waveform appears at the input to the *capacitor-input filter* of Fig. 24-27c. Therefore, the regulated output voltage approximately equals the peak voltage given by Eq. (24-23). Because  $V_{kick}$  is always greater than zero,  $V_p$  is always greater than  $V_{in}$ . This is why a boost regulator always steps up the voltage up.

Aside from using a capacitor-input filter rather than a choke-input filter, the regulation with boost topology is similar to that with buck topology. Because of the high gain of the comparator, the feedback almost equals the reference voltage. Therefore, the regulated output voltage is still given by Eq. (24-23). If the output voltage tries to increase, there is less feedback voltage, less comparator output, a smaller duty cycle, and less inductive kick. This reduces the peak voltage, which offsets the attempted increase in output voltage. If the output voltage tries to decrease, the smaller feedback voltage results in a larger peak voltage, which offsets the attempted decrease in output voltage.

### Buck-Boost Regulator

Figure 24-28a shows a **buck-boost regulator**, the third most basic topology for switching regulators. A buck-boost regulator always produces a negative output voltage when driven by a positive input voltage. When the PWM output is high, the switch is closed and energy is stored in the magnetic field. At this time, the voltage across the inductor equals  $V_{in}$ , with the polarity shown in Fig. 24-28b.

When the pulse goes low, the switch opens. Again, the magnetic field around the inductor collapses and induces a kick voltage across the inductor, as shown in Fig. 24-28c. The kick voltage is proportional to the energy stored in the magnetic field, which is controlled by the duty cycle. If the duty cycle is low, the kick voltage approaches zero. If the duty cycle is high, the kick voltage can be greater than  $V_{in}$ , depending on how much energy is stored in the magnetic field.

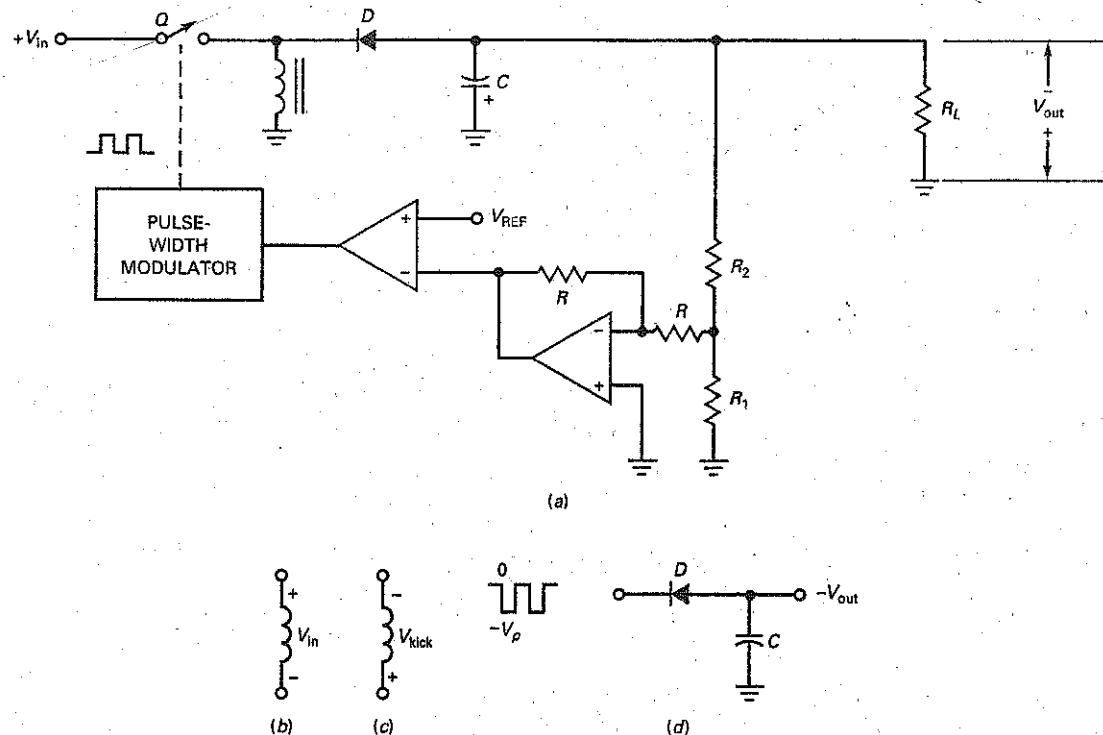
In Fig. 24-28d, the magnitude of the peak voltage may be less than or greater than the input voltage. The diode and the capacitor-input filter then produce an output voltage equal to  $-V_p$ . Since the magnitude of this output voltage can be less than or greater than the input voltage, the topology is called *buck-boost*.

An inverting amplifier is used in Fig. 24-28a to invert the feedback voltage before it reaches the inverting input of the comparator. The voltage regulation then works as previously described. Attempted increases in output voltage reduce the duty cycle, which reduces the peak voltage. Attempted decreases in output voltage increase the duty cycle. Either way, the negative feedback holds the output voltage almost constant.

### Monolithic Buck Regulators

Some IC switching regulators have only five external pins. For instance, the LT1074 is a monolithic bipolar switching regulator that uses buck topology. It contains most of the components discussed earlier, such as a reference voltage of 2.21 V, a switching device, an internal oscillator, a pulse-width modulator, and a

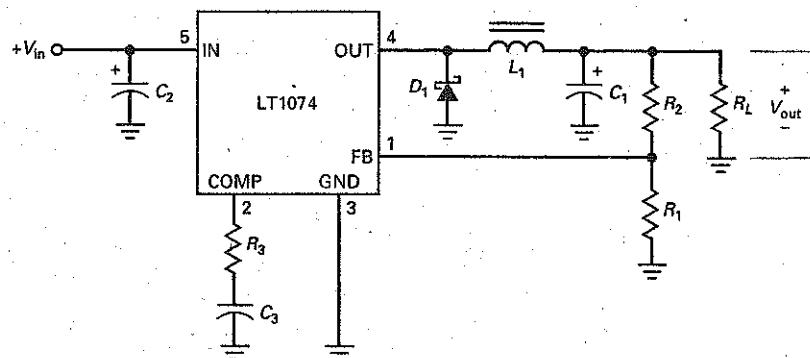
**Figure 24-28** (a) Buck-boost regulator; (b) polarity with closed switch; (c) polarity with open switch; (d) capacitor-input filter produces output equal to negative peak.



comparator. It runs at a switching frequency of 100 kHz, can handle input voltages from +8 to +40 V dc, and has efficiency of 75 to 90 percent for load currents from 1 to 5 A.

Figure 24-29 shows an LT1074 connected as a buck regulator. Pin 1 (FB) is for the feedback voltage. Pin 2 (COMP) is for frequency compensation to prevent oscillations at higher frequencies. Pin 3 (GND) is ground. Pin 4 (OUT) is the switched output of the internal switching device. Pin 5 (IN) is for the dc input voltage.

**Figure 24-29** Buck regulator using LT1074.



$D_1$ ,  $L_1$ ,  $C_1$ ,  $R_1$ , and  $R_2$  serve the same functions as described in the earlier discussion of a buck regulator. But notice the use of a Schottky diode to improve the efficiency of the regulator. Because the Schottky diode has a lower knee voltage, it wastes less power. The data sheet of an LT1074 recommends adding a capacitor  $C_2$  from 200 to 470  $\mu\text{F}$  across the input for line filtering. Also recommended are a resistor  $R_3$  of 2.7  $\text{k}\Omega$  and a capacitor  $C_3$  of 0.01  $\mu\text{F}$  to stabilize the feedback loop (prevent oscillations).

The LT1074 is widely used. A look at Fig. 24-29 tells us why. The circuit is incredibly simple, considering that it is a switching regulator, one of the most difficult of all circuits to design and build in discrete form. Fortunately, the IC designers have done all the hard work because the LT1074 includes everything except the components that cannot be integrated (choke and filter capacitors) and those left for the user to select ( $R_1$  and  $R_2$ ). By selecting values for  $R_1$  and  $R_2$ , we can get regulated output voltage from about 2.5 to 38 V. Since the reference voltage of an LT1074 is 2.21 V, the output voltage is given by:

$$V_{\text{out}} = \frac{R_1 + R_2}{R_1} (2.21 \text{ V}) \quad (24-24)$$

The headroom voltage should be at least 2 V because the internal switching device consists of a *pnp* transistor driving an *npn* Darlington. The overall switch drop can be as high as 2 V with high currents.

## Monolithic Boost Regulators

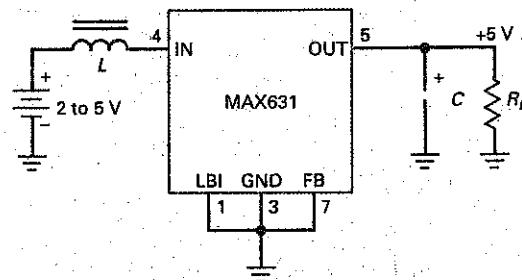
The MAX631 is a monolithic CMOS switching regulator that uses boost topology to produce a regulated output. This low-power IC switching regulator has a switching frequency of 50 kHz, an input voltage of 2 to 5 V, and an efficiency of about 80 percent. The MAX631 is the ultimate in simplicity because it requires only two external components.

For instance, Fig. 24-30 shows a MAX631 connected as a boost regulator, producing a fixed output voltage of +5 V with an input voltage of +2 to +5 V. The input voltage often comes from a battery because one of the applications for these IC regulators is in portable instruments. The data sheet recommends an inductor of 330  $\mu\text{H}$  and a capacitor of 100  $\mu\text{F}$ .

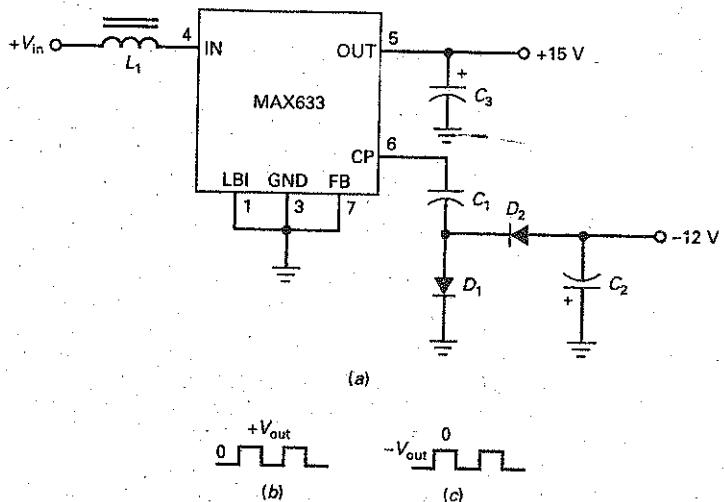
The MAX631 is an 8-pin device whose unused pins are either grounded or left unconnected. In Fig. 24-30, pin 1 (LBI) can be used for low-battery detection. When grounded, it has no effect. Although typically used as a fixed output regulator, the MAX631 can use an external voltage divider to provide a feedback voltage to pin 7 (FB). When pin 7 is grounded as shown, the output voltage is the factory preset value of +5 V.

Besides the MAX631, there is the MAX632, which produces an output of +12 V, and the MAX633, which produces an output of +15 V. The MAX631 to MAX633 regulators include pin 6, called the *charge pump*, which is a

Figure 24-30 Boost regulator using MAX631.



**Figure 24-31** (a) Using charge pump of MAX633 to produce negative output voltage; (b) output of pin 6 drives negative clamper; (c) input to negative peak detector.



low-impedance buffer that produces a rectangular output signal. This signal swings from 0 to  $V_{out}$  at the oscillator frequency and can be negatively clamped and peak-detected to get a negative output voltage.

For instance, Fig. 24-31a shows how a MAX633 uses its charge pump to get an output of approximately  $-12$  V.  $C_1$  and  $D_1$  are a negative clamper.  $D_2$  and  $C_2$  are a negative peak detector. Here is how the charge pump works: Figure 24-31b shows the ideal voltage waveform coming out of pin 6. Because of the negative clamper, the ideal voltage waveform across  $D_1$  is the negatively clamped waveform of Fig. 24-31c. This waveform drives the negative peak detector to produce an output of approximately  $-12$  V at  $20$  mA. The magnitude of this voltage is approximately  $3$  V less than the output voltage because of the two diode drops ( $D_1$  and  $D_2$ ) and the drop across the output impedance of the buffer (around  $30\ \Omega$ ).

If we use a battery to supply the input voltage to a linear regulator, the output voltage is always smaller. Boost regulators not only have better efficiency than linear regulators, they also can step up the voltage in a battery-powered system. This is very important and explains why monolithic boost regulators are so widely used. The availability of low-cost rechargeable batteries has made the monolithic boost regulator a standard choice for battery-powered systems.

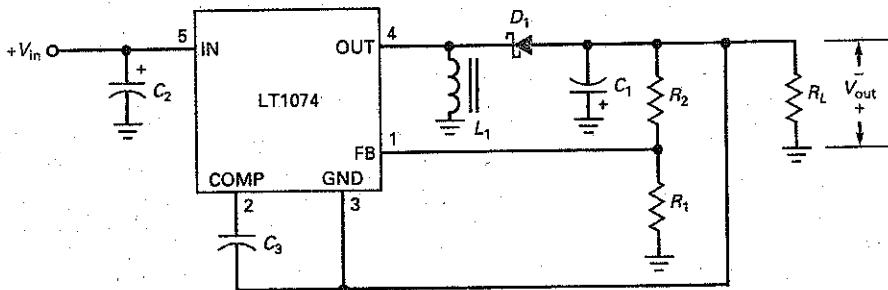
The MAX631 to MAX633 devices have an internal reference voltage of  $1.31$  V. When these switching regulators are used with an external voltage divider, the following equation gives the regulated output voltage:

$$V_{out} = \frac{R_1 + R_2}{R_1} (1.31\text{ V}) \quad (24-25)$$

### Monolithic Buck-Boost Regulators

The internal design of the LT1074 can support a buck-boost external connection. Figure 24-32 shows the LT1074 connected as a buck-boost regulator. Again, we are using a Schottky diode to improve the efficiency. As previously discussed, energy is stored in the inductor's magnetic field when the internal switch is closed. When the switch opens, the magnetic field collapses and forward biases the diode. The negative kick voltage across the inductor is peak-detected by the capacitor-input filter to produce  $-V_{out}$ .

**Figure 24-32** Using the LT1074 as buck-boost regulator.



In the earlier discussion of buck-boost topology (Fig. 24-28a), we used an inverting amplifier to get a positive feedback voltage because the output sample from the voltage divider was negative. The internal design of the LT1074 takes care of this problem. The data sheet recommends returning the GND pin to the negative output voltage, as shown in Fig. 24-32. This produces the correct error voltage to the comparator that controls the pulse-width modulator.

### Example 24-15

In the buck regulator of Fig. 24-29,  $R_1 = 2.21 \text{ k}\Omega$  and  $R_2 = 2.8 \text{ k}\Omega$ . What is the output voltage? What is the minimum input voltage that can be used with the output voltage?

**SOLUTION** With Eq. (24-24), we can calculate:

$$V_{\text{out}} = \frac{R_1 + R_2}{R_1} V_{\text{REF}} = \frac{2.21 \text{ k}\Omega + 2.8 \text{ k}\Omega}{2.21 \text{ k}\Omega} (2.21 \text{ V}) = 5.01 \text{ V}$$

Because of the drop across the switching device of an LT1074, the input voltage has to be at least 2 V greater than the output of 5 V, which means minimum input voltage of 7 V. A more comfortable headroom will use an input voltage of 8 V.

**PRACTICE PROBLEM 24-15** Repeat Example 24-15, change  $R_2$  to  $5.6 \text{ k}\Omega$  and calculate the new output voltage. With  $R_1 = 2.2 \text{ k}\Omega$ , what value of  $R_2$  is needed to produce an output of 10 V?

### Example 24-16

In the buck-boost regulator of Fig. 24-32,  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 5.79 \text{ k}\Omega$ . What is the output voltage?

**SOLUTION** With Eq. (24-24), we can calculate:

$$V_{\text{out}} = \frac{R_1 + R_2}{R_1} V_{\text{REF}} = \frac{1 \text{ k}\Omega + 5.79 \text{ k}\Omega}{1 \text{ k}\Omega} (2.21 \text{ V}) = 15 \text{ V}$$

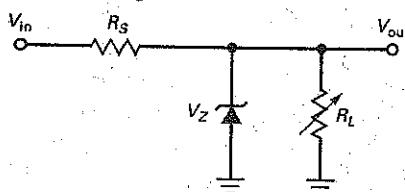
**PRACTICE PROBLEM 24-16** Using Fig. 24-32, what is the output voltage if  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 4.7 \text{ k}\Omega$ ?

Summary Table 24-1 shows a variety of voltage regulators and lists some of their characteristics.

**Summary Table 24-1** | **Voltage Regulators**

**Type**

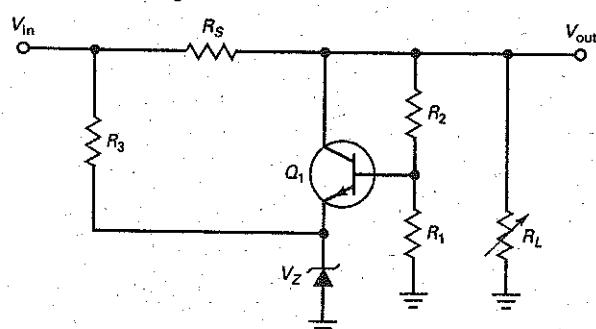
**Zener shunt regulator**



**Characteristics**

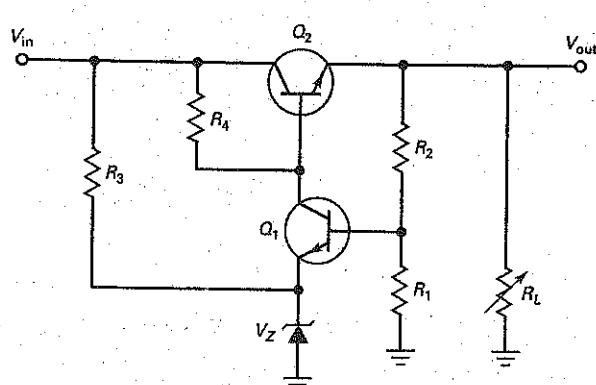
- $V_{out} = V_Z$
- Simple to build
- $\Delta V_{out} = \Delta I_Z R_Z$

**Transistor shunt regulator**



- $V_{out} = \frac{R_1 + R_2}{R_1} (V_Z + V_{BE})$
- Improved regulation
- Built-in short-circuit protection
- Low efficiency

**Transistor series regulator**

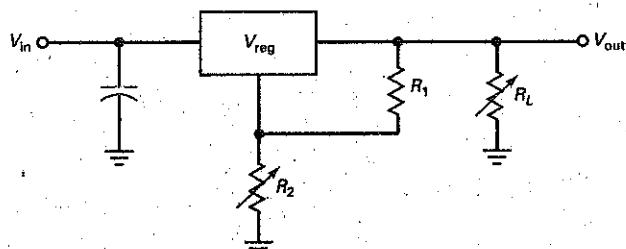
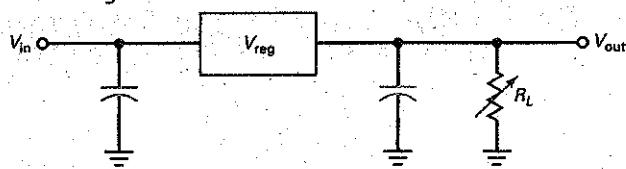


- $V_{out} = \frac{R_1 + R_2}{R_1} (V_Z + V_{BE})$
- Improved efficiency over shunt regulator
- $Q_2 P_D \approx (V_{in} - V_{out}) I_L$
- Needs added short-circuit protection

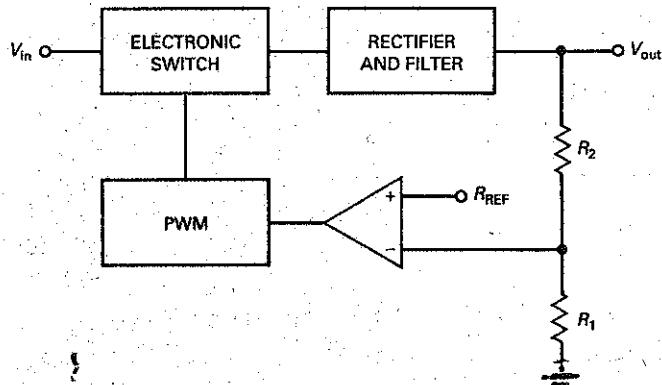
**Summary Table 24-1** (continued)

**Type**

**IC linear regulator**



**IC switching regulator**



**Characteristics**

- Easy to use
- Fixed or adjustable outputs
- $V_{out} = V_{reg}$  or  $\frac{R_1 + R_2}{R_1} (V_{ref})$
- Essentially a series regulator
- Good ripple rejection
- Built-in short-circuit and temperature protection possible

- Uses pulse-wide modulation
- High efficiencies
- Steps up or down input voltage
- May require complex circuitry
- Somewhat noisy
- Popular in computer and consumer electronics

## Summary

### SEC. 24-1 SUPPLY CHARACTERISTICS

Load regulation indicates how much the output voltage changes when the load current changes. Line regulation indicates how much the load voltage changes when the line voltage changes. The output resistance determines the load regulation.

### SEC. 24-2 SHUNT REGULATORS

The zener regulator is the simplest example of a shunt regulator. By adding transistors and an op amp, we can build a shunt regulator that has excellent line and load regulation. The main disadvantage of a shunt regulator is its low efficiency, caused by power losses in the series resistor and shunt transistor.

### SEC. 24-3 SERIES REGULATORS

By using a pass transistor instead of a series resistor, we can build series regulators with higher efficiencies than shunt regulators. The zener follower is the simplest example of a series regulator. By adding transistors and an op amp, we can build series regulators with excellent line and load regulation, plus current limiting.

## SEC. 24-4 MONOLITHIC LINEAR REGULATORS

IC voltage regulators have one of the following voltages: fixed positive, fixed negative, or adjustable. IC regulators are also classified as standard, low-power, and low-dropout. The LM78XX series is a standard line of fixed regulators with output voltages from 5 to 24 V.

## SEC. 24-5 CURRENT BOOSTERS

To increase the regulated load current of an IC regulator such as a 78XX device, we can use an outboard transistor to carry most of the current above 1 A. By adding another transistor, we can have short-circuit protection.

## SEC. 24-6 DC-TO-DC CONVERTERS

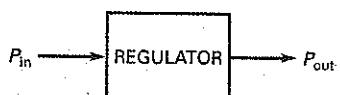
When we want to convert an input dc voltage to an output dc voltage of another value, a dc-to-dc converter is useful. Unregulated dc-to-dc converters have an oscillator whose output voltage is proportional to the input voltage. Typically, a push-pull arrangement of transistors and a transformer can step this voltage up or down. Then, it is rectified and filtered to get an output voltage different from the input voltage.

## SEC. 24-7 SWITCHING REGULATORS

A switching regulator is a dc-to-dc converter that uses pulse-width modulation to regulate the output voltage. By switching the pass transistor on and off, the switching regulator can attain efficiencies from 70 to 95 percent. The basic topologies are the buck (step-down), boost (step-up), and buck-boost (inverting). This type of regulator is very popular in computer and portable electronic systems.

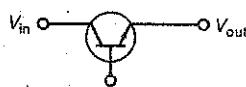
## Definitions

(24-8) Efficiency:



$$\text{Efficiency} = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100\%$$

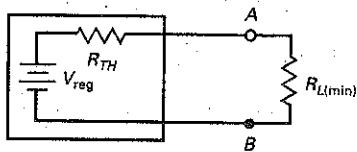
(24-11) Headroom:



$$\text{Headroom voltage} = V_{\text{in}} - V_{\text{out}}$$

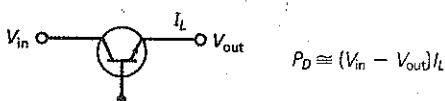
## Derivations

(24-4) Load regulation:



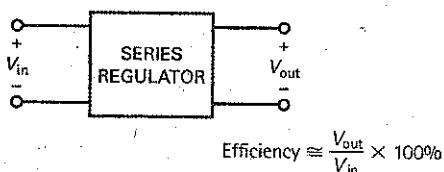
$$\text{Load regulation} = \frac{R_{TH}}{R_{L(\min)}} \times 100\%$$

(24-12) Pass dissipation:



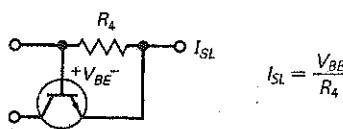
$$P_D \approx (V_{\text{in}} - V_{\text{out}})I_L$$

(24-13) Efficiency:



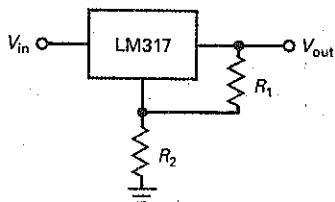
$$\text{Efficiency} \approx \frac{V_{\text{out}}}{V_{\text{in}}} \times 100\%$$

(24-17) Shorted-load current:



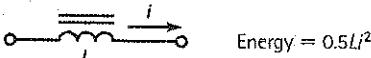
$$I_{SL} = \frac{V_{BE}}{R_4}$$

(24-19) LM317 output voltage:



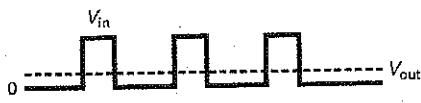
$$V_{\text{out}} = \frac{R_1 + R_2}{R_1} (1.25 \text{ V})$$

(24-20) Stored energy in magnetic field:

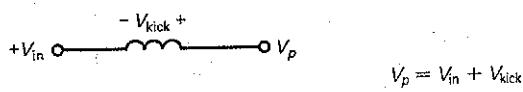


$$\text{Energy} = 0.5LI^2$$

(24-21) Average value of input to filter

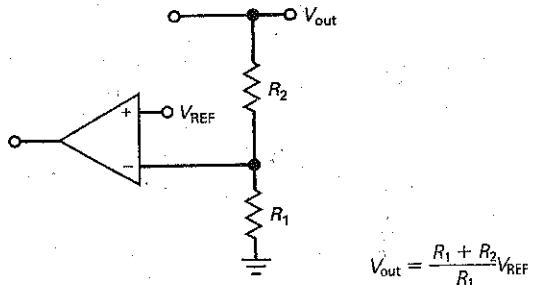


(24-23) Boost peak voltage:



$$V_p = V_{in} + V_{kick}$$

(24-22) Output of switching regulator:



$$V_{out} = \frac{R_1 + R_2}{R_1} V_{REF}$$

## Student Assignments

1. Voltage regulators normally use
  - a. Negative feedback
  - b. Positive feedback
  - c. No feedback
  - d. Phase limiting
2. During regulation, the power dissipation of the pass transistor equals the collector-emitter voltage times the
  - a. Base current
  - b. Load current
  - c. Zener current
  - d. Foldback current
3. Without current limiting, a shorted load will probably
  - a. Produce zero load current
  - b. Destroy diodes and transistors
  - c. Have a load voltage equal to the zener voltage
  - d. Have too little load current
4. A current-sensing resistor is usually
  - a. Zero      c. Large
  - b. Small     d. Open
5. Simple current limiting produces too much heat in the
  - a. Zener diode
  - b. Load resistor
  - c. Pass transistor
  - d. Ambient air
6. With foldback current limiting, the load voltage approaches zero and the load current approaches
  - a. A small value
  - b. Infinity
  - c. The zener current
  - d. A destructive level
7. A capacitor may be needed in a discrete voltage regulator to prevent
  - a. Negative feedback
  - b. Excessive load current
  - c. Oscillations
  - d. Current sensing
8. If the output of a voltage regulator varies from 15 to 14.7 V between the minimum and maximum load current, the load regulation is
  - a. 0
  - b. 1 percent
  - c. 2 percent
  - d. 5 percent
9. If the output of a voltage regulator varies from 20 to 19.8 V when the line voltage varies over its specified range, the source regulation is
  - a. 0            c. 2 percent
  - b. 1 percent    d. 5 percent
10. The output impedance of a voltage regulator is
  - a. Very small
  - b. Very large
  - c. Equal to the load voltage divided by the load current
  - d. Equal to the input voltage divided by the output current
11. Compared to the ripple into a voltage regulator, the ripple out of a voltage regulator is
  - a. Equal in value
  - b. Much larger
  - c. Much smaller
  - d. Impossible to determine
12. A voltage regulator has a ripple rejection of -60 dB. If the input ripple is 1 V, the output ripple is
  - a. -60 mV
  - b. 1 mV
  - c. 10 mV
  - d. 1000 V
13. Thermal shutdown occurs in an IC regulator if
  - a. Power dissipation is too low
  - b. Internal temperature is too high
  - c. Current through the device is too low
  - d. Any of the above occur

- 14.** If a linear three-terminal IC regulator is more than a few inches from the filter capacitor, you may get oscillations inside the IC unless you use
- Current limiting
  - A bypass capacitor on the input pin
  - A coupling capacitor on the output pin
  - A regulated input voltage
- 15.** The 78XX series of voltage regulators produces an output voltage that is
- Positive
  - Negative
  - Either positive or negative
  - Unregulated
- 16.** The LM7812 produces a regulated output voltage of
- 3 V
  - 12 V
  - 4 V
  - 78 V
- 17.** A current booster is a transistor in
- Series with the IC regulator
  - Parallel with the IC regulator
  - Either series or parallel
  - Shunt with the load
- 18.** To turn on a current booster, we can drive its base-emitter terminals with the voltage across
- A load resistor
  - A zener impedance
  - Another transistor
  - A current-sensing resistor
- 19.** A phase splitter produces two output voltages that are
- Equal in phase
  - Unequal in amplitude
  - Opposite in phase
  - Very small
- 20.** A series regulator is an example of a
- Linear regulator
  - Switching regulator
  - Shunt regulator
  - DC-to-dc converter
- 21.** To get more output voltage from a buck switching regulator, you have to
- Decrease the duty cycle
  - Decrease the input voltage
  - Increase the duty cycle
  - Increase the switching frequency
- 22.** An increase of line voltage into a power supply usually produces
- A decrease in load resistance
  - An increase in load voltage
  - A decrease in efficiency
  - Less power dissipation in the rectifier diodes
- 23.** A power supply with low output impedance has low
- Load regulation
  - Current limiting
  - Line regulation
  - Efficiency
- 24.** A zener-diode regulator is a
- Shunt regulator
  - Series regulator
  - Switching regulator
  - Zener follower
- 25.** The input current to a shunt regulator is
- Variable
  - Constant
  - Equal to load current
  - Used to store energy in a magnetic field
- 26.** An advantage of shunt regulation is
- Built-in short-circuit protection
  - Low power dissipation in the pass transistor
  - High efficiency
  - Little wasted power
- 27.** The efficiency of a voltage regulator is high when
- Input power is low
  - Output power is high
  - Little power is wasted
  - Input power is high
- 28.** A shunt regulator is inefficient because
- It wastes power
  - It uses a series resistor and a shunt transistor
  - The ratio of output to input power is low
  - All of the above
- 29.** A switching regulator is considered
- Quiet
  - Noisy
  - Inefficient
  - Linear
- 30.** The zener follower is an example of a
- Boost regulator
  - Buck regulator
  - Shunt regulator
  - Series regulator
- 31.** A series regulator is more efficient than a shunt regulator because
- It has a series resistor
  - It can boost the voltage
  - The pass transistor replaces the series resistor
  - It switches the pass transistor on and off
- 32.** The efficiency of a linear regulator is high when the
- Headroom voltage is low
  - Pass transistor has a high power dissipation
  - Zener voltage is low
  - Output voltage is low
- 33.** If the load is shorted, the pass transistor has the least power dissipation when the regulator has
- Foldback limiting
  - Low efficiency
  - Buck topology
  - A high zener voltage
- 34.** The dropout voltage of standard monolithic linear regulators is closest to
- 0.3 V
  - 0.7 V
  - 2 V
  - 3.1 V
- 35.** In a buck regulator, the output voltage is filtered with a
- Choke-input filter
  - Capacitor-input filter
  - Diode
  - Voltage divider
- 36.** The regulator with the highest efficiency is the
- Shunt regulator
  - Series regulator
  - Switching regulator
  - DC-to-dc converter
- 37.** In a boost regulator, the output voltage is filtered with a
- Choke-input filter
  - Capacitor-input filter
  - Diode
  - Voltage divider
- 38.** The buck-boost regulator is also
- A step-down regulator
  - A step-up regulator
  - An inverting regulator
  - All of the above

## Problems

### SEC. 24-1 SUPPLY CHARACTERISTICS

- 24-1 A power supply has  $V_{NL} = 15 \text{ V}$  and  $V_{RL} = 14.5 \text{ V}$ . What is the load regulation?
- 24-2 A power supply has  $V_{NL} = 20 \text{ V}$  and  $V_{RL} = 19 \text{ V}$ . What is the line regulation?
- 24-3 If line voltage changes from 108 to 135 V and load voltage changes from 12 to 12.3 V, what is the line regulation?
- 24-4 A power supply has an output resistance of  $2 \Omega$ . If the minimum load resistance is  $50 \Omega$ , what is the load regulation?

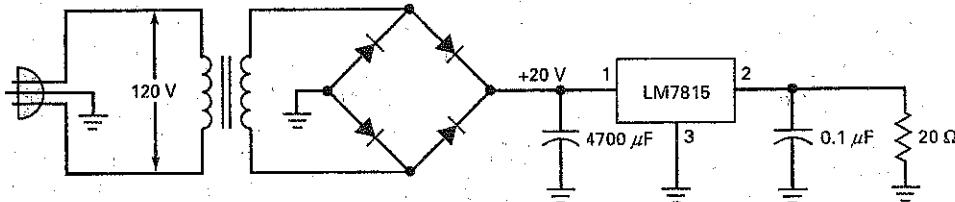
### SEC. 24-2 SHUNT REGULATORS

- 24-5 In Fig. 24-4,  $V_{in} = 25 \text{ V}$ ,  $R_S = 22 \Omega$ ,  $V_Z = 18 \text{ V}$ ,  $V_{BE} = 0.75 \text{ V}$ , and  $R_L = 100 \Omega$ . What are the values of output voltage, the input current, the load current, and the collector current?
- 24-6 The shunt regulator of Fig. 24-5 has these circuit values:  $V_{in} = 25 \text{ V}$ ,  $R_S = 15 \Omega$ ,  $V_Z = 5.6 \text{ V}$ ,  $V_{BE} = 0.77 \text{ V}$ , and  $R_L = 80 \Omega$ . If  $R_1 = 330 \Omega$  and  $R_2 = 680 \Omega$ , what are the approximate values of output voltage, the input current, the load current, and the collector current?
- 24-7 The shunt regulator of Fig. 24-6 has these circuit values:  $V_{in} = 25 \text{ V}$ ,  $R_S = 8.2 \Omega$ ,  $V_Z = 5.6 \text{ V}$ , and  $R_L = 50 \Omega$ . If  $R_1 = 2.7 \text{ k}\Omega$  and  $R_2 = 6.2 \text{ k}\Omega$ , what are the approximate values of output voltage, the input current, the load current, and the collector current?

### SEC. 24-3 SERIES REGULATORS

- 24-8 In Fig. 24-8,  $V_{in} = 20 \text{ V}$ ,  $V_Z = 4.7 \text{ V}$ ,  $R_1 = 2.2 \text{ k}\Omega$ ,  $R_2 = 4.7 \text{ k}\Omega$ ,  $R_3 = 1.5 \text{ k}\Omega$ ,  $R_4 = 2.7 \text{ k}\Omega$ , and  $R_L = 50 \Omega$ . What is the output voltage? What is the power dissipation in the pass transistor?
- 24-9 What is the approximate efficiency in Prob. 24-8?
- 24-10 In Fig. 24-15, the zener voltage is changed to 6.2 V. What is the approximate output voltage?
- 24-11 In Fig. 24-16,  $V_{in}$  can vary from 20 to 30 V. What is the maximum zener current?

Figure 24-33 Example.



### Critical Thinking

- 24-24 Figure 24-34 shows an LM317 regulator with electronic shutdown. When the shutdown voltage is zero, the transistor is cut off and has no effect on the operation. But when the shutdown voltage is approximately 5 V, the transistor saturates. What is the adjustable range of output voltage when the shutdown voltage is zero?

- 24-12 If the 1-kΩ potentiometer of Fig. 24-16 is changed to 1.5 kΩ, what are the minimum and maximum regulated output voltages?

- 24-13 If the regulated output voltage is 8 V in Fig. 24-16, what is the load resistance where current limiting starts? What is the approximate shorted-load current?

### SEC. 24-4 MONOLITHIC LINEAR REGULATORS

- 24-14 What is the load current in Fig. 24-33? The headroom voltage? The power dissipation of the LM7815?
- 24-15 What is the output ripple in Fig. 24-33?
- 24-16 If  $R_1 = 2.7 \text{ k}\Omega$  and  $R_2 = 20 \text{ k}\Omega$  in Fig. 24-20, what is the output voltage?
- 24-17 The LM7815 is used with an input voltage that can vary from 18 to 25 V. What is the maximum efficiency? The minimum efficiency?

### SEC. 24-6 DC-TO-DC CONVERTERS

- 24-18 A dc-to-dc converter has an input voltage of 5 V and an output voltage of 12 V. If the input current is 1 A and the output current is 0.25 A, what is the efficiency of the dc-to-dc converter?
- 24-19 A dc-to-dc converter has an input voltage of 12 V and an output voltage of 5 V. If the input current is 2 A and the efficiency is 80 percent, what is the output current?

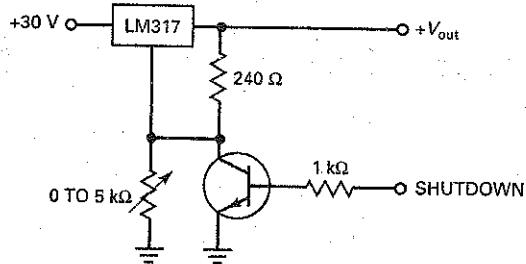
### SEC. 24-7 SWITCHING REGULATORS

- 24-20 A buck regulator has  $V_{REF} = 2.5 \text{ V}$ ,  $R_1 = 1.5 \text{ k}\Omega$ , and  $R_2 = 10 \text{ k}\Omega$ . What is the output voltage?
- 24-21 If the duty cycle is 30 percent and the peak value of the pulses to the choke-input filter is 20 V, what is the regulated output voltage?
- 24-22 A boost regulator has  $V_{REF} = 1.25 \text{ V}$ ,  $R_1 = 1.2 \text{ k}\Omega$ , and  $R_2 = 15 \text{ k}\Omega$ . What is the output voltage?
- 24-23 A buck-boost regulator has  $V_{REF} = 2.1 \text{ V}$ ,  $R_1 = 2.1 \text{ k}\Omega$ , and  $R_2 = 12 \text{ k}\Omega$ . What is the output voltage?

What does the output voltage equal when the shutdown voltage is 5 V?

- 24-25 The transistor of Fig. 24-34 is cut off. To get an output voltage of 18 V, what value should the adjustable resistor have?

Figure 24-34



- 24-26 When a bridge rectifier and a capacitor-input filter drive a voltage regulator, the capacitor voltage during discharge is almost a perfect ramp. Why do we get a ramp instead of the usual exponential wave?
- 24-27 If the load regulation is 5 percent and the no-load voltage is 12.5 V, what is the full-load voltage?

## Troubleshooting

Use Fig. 24-35 for the remaining problems. In this set of problems, you are troubleshooting a switching regulator. Before you start, look at the OK row in the troubleshooting table to see the normal waveforms with their correct peak voltages. In this exercise, most of the troubles are IC failures rather than resistor failures. When an IC fails, anything can happen. Pins may be internally open, shorted, and so on. No matter what the trouble is inside the IC, the most common symptom is a *stuck output*. This refers to the output voltage being stuck at either positive or negative saturation. If the input signals are OK, an IC with a stuck output has to be replaced. The following problems will give you a chance to work with outputs that are stuck at either +13.5 or -13.5 V.

- 24-28 If the line regulation is 3 percent and the low-line voltage is 16 V, what is the high-line voltage?
- 24-29 A power supply has a load regulation of 1 percent and a minimum load resistance of  $10 \Omega$ . What is the output resistance of the power supply?
- 24-30 The shunt regulator of Fig. 24-6 has an input voltage of 35 V, a collector current of 60 mA, a load current of 140 mA. If the series resistance is  $100 \Omega$ , what is the load resistance?
- 24-31 In Fig. 24-10, we want current limiting to start at approximately 250 mA. What value should we use for  $R_4$ ?
- 24-32 Figure 24-12 has an output voltage of 10 V. If  $V_{BE} = 0.7$  V for the current-limiting transistor, what are the values of shorted-load current and the maximum load current? Use  $K = 0.7$  and  $R_4 = 1 \Omega$ .
- 24-33 In Fig. 24-35,  $R_5 = 7.5 \text{ k}\Omega$ ,  $R_6 = 1 \text{ k}\Omega$ ,  $R_7 = 9 \text{ k}\Omega$ , and  $C_3 = 0.001 \mu\text{F}$ . What is the switching frequency of the buck regulator?
- 24-34 In Fig. 24-16, the wiper is at the middle of its range. What is the output voltage?

Figure 24-35

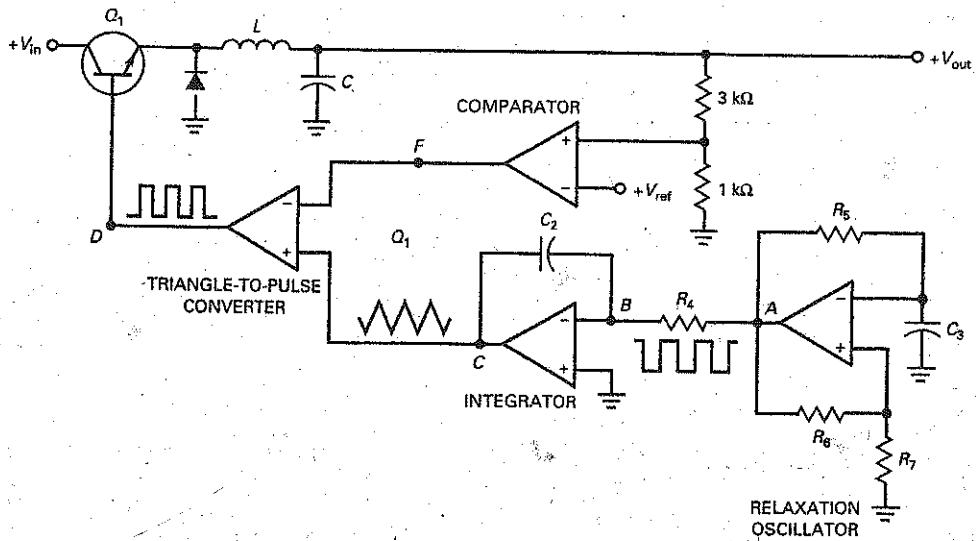
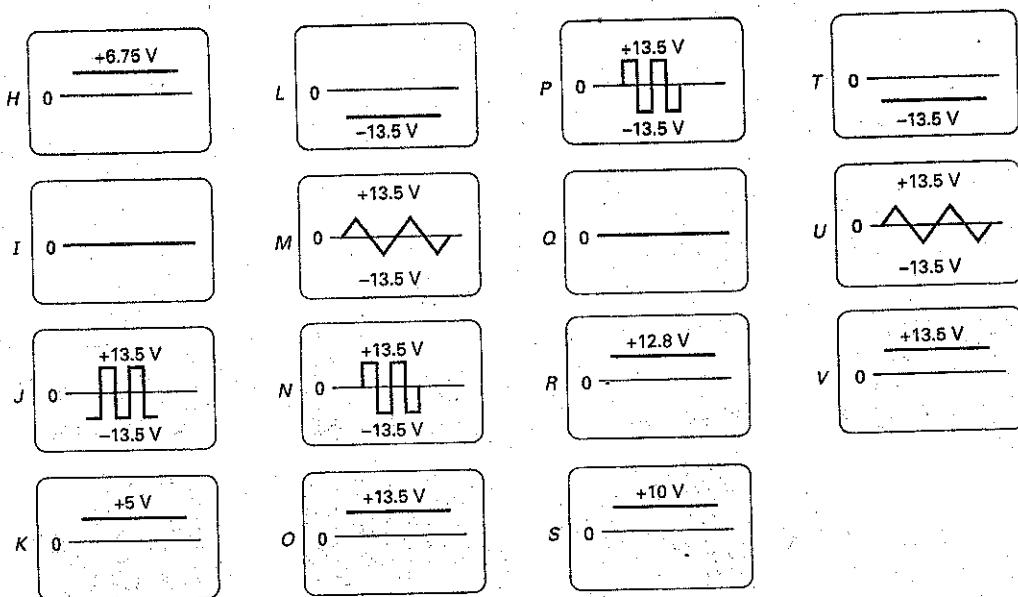


Figure 24-35 (continued)

Troubleshooting

Trouble	$V_A$	$V_B$	$V_C$	$V_D$	$V_E$	$V_F$
OK	N	I	M	J	K	H
T1	P	I	U	T	I	L
T2	T	L	V	O	R	O
T3	N	Q	M	V	I	T
T4	P	N	L	T	Q	L
T5	P	V	L	T	I	L
T6	N	Q	M	O	R	T
T7	P	I	U	I	Q	L
T8	P	I	U	L	Q	V
T9	N	Q	M	O	R	V

Waveforms



## Job Interview Questions

1. Draw any shunt regulator and tell me how it works.
2. Draw any series regulator and tell me how it works.
3. Explain why the efficiency of a series regulator is better than that of a shunt regulator.
4. What are the three basic types of switching regulators? Which one steps the voltage up? Which one produces a

negative output from a positive input? Which one steps the voltage down?

5. In a series regulator, what does *headroom voltage* mean? How is the efficiency related to headroom voltage?
6. What is the difference between the LM7806 and the LM7912?

- Explain what line and load regulation mean. Should they be high or low if you want a quality power supply?
- How is the Thevenin or output resistance of a power supply related to the load regulation? For a quality power supply, should the output resistance be high or low?
- What is the difference between simple current limiting and foldback current limiting?
- What does *thermal shutdown* mean?
- The manufacturer of a three-terminal regulator recommends using a bypass capacitor on the input if the IC is more than 6 in from the unregulated power supply. What is the purpose of this capacitor?
- What is the typical dropout voltage for the LM78XX series? What does it mean?

## Self-Test Answers

- |       |       |       |
|-------|-------|-------|
| 1. a  | 14. b | 27. c |
| 2. b  | 15. a | 28. d |
| 3. b  | 16. c | 29. b |
| 4. b  | 17. b | 30. d |
| 5. c  | 18. d | 31. c |
| 6. a  | 19. c | 32. a |
| 7. c  | 20. a | 33. a |
| 8. c  | 21. c | 34. c |
| 9. b  | 22. b | 35. a |
| 10. a | 23. a | 36. c |
| 11. c | 24. a | 37. b |
| 12. b | 25. b | 38. d |
| 13. b | 26. a |       |

## Practice Problem Answers

- |  |  |  |
|--|--|--|
| <b>24-1</b> $V_{out} = 7.6 \text{ V}$ ;<br>$I_S = 440 \text{ mA}$ ;<br>$I_L = 190 \text{ mA}$ ;<br>$I_C = 250 \text{ mA}$  | <b>24-6</b> Load regulation = 2.16%;<br>Line regulation = 3.31%  | <b>24-12</b> $I_L = 150 \text{ mA}$ ;<br>$V_R = 198 \mu\text{V}$         |
| <b>24-2</b> $V_{out} = 11.1 \text{ V}$ ;<br>$I_S = 392 \text{ mA}$ ;<br>$I_L = 277 \text{ mA}$ ;<br>$I_C = 115 \text{ mA}$ | <b>24-7</b> $V_{out} = 8.4 \text{ V}$ ;<br>$P_D = 756 \text{ mW}$  | <b>24-13</b> $V_{out} = 7.58 \text{ V}$                                  |
| <b>24-3</b> $P_{out} = 3.07 \text{ W}$ ;<br>$P_n = 5.88 \text{ W}$ ;<br>% Eff. = 52.2%                                     | <b>24-8</b> Efficiency = 70%   | <b>24-15</b> $V_{out} = 7.81 \text{ V}$ ;<br>$R_2 = 7.8 \text{ k}\Omega$ |
| <b>24-4</b> $I_C = 66 \text{ mA}$ ;<br>$P_D = 858 \text{ mW}$  | <b>24-9</b> $V_{out} = 11.25 \text{ V}$  | <b>24-16</b> $V_{out} = 7.47 \text{ V}$                                  |
|  | <b>24-11</b> $I_Z = 22.7 \text{ mA}$ ;<br>$V_{out(min)} = 5.57 \text{ V}$ ;<br>$V_{out(max)} = 13 \text{ V}$ ;<br>$R_L = 41.7 \Omega$ ;<br>$I_{SL} = 350 \text{ mA}$ |  |

# Appendix A

## Data Sheets

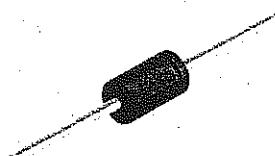
- 1N4001 to 1N4007 (rectifier diodes)**
- 1N957B Series (zener diodes)**
- 1N4728A Series (zener diodes)**
- 2N3903, 2N3904 (general purpose silicon transistors: npn)**
- 2N3906 (general purpose silicon transistors: pnp)**
- TIP 100/101/102 (silicon Darlington transistor)**
- MPF102 (JFET n-channel RF amplifier)**
- 2N7000 (MOSFET n-channel enhancement mode)**
- 2N6504 (silicon controlled rectifiers)**
- FKPF8N80 (triode thyristor)**
- FGL60N100BNTD (NPT-Trench IGBT)**
- LM741 (general purpose operational amplifier)**
- LM118/218/318 (precision high-speed operational amplifiers)**
- LM555 (timer)**
- XR-2206 (function generator IC)**
- LM78XX Series (three terminal voltage regulators)**

**FAIRCHILD**  
SEMICONDUCTOR®

## 1N4001 - 1N4007

### Features

- Low forward voltage drop.
- High surge current capability.



DO-41

COLOR BAND DENOTES CATHODE

### General Purpose Rectifiers

#### Absolute Maximum Ratings\*

 $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Value							Units
		4001	4002	4003	4004	4005	4006	4007	
$V_{RRM}$	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current, .375 " lead length @ $T_A = 75^\circ\text{C}$				1.0				A
$I_{FSM}$	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave				30				A
$T_{stg}$	Storage Temperature Range				-55 to +175				$^\circ\text{C}$
$T_J$	Operating Junction Temperature				-55 to +175				$^\circ\text{C}$

\*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

### Thermal Characteristics

Symbol	Parameter	Value							Units
$P_D$	Power Dissipation	3.0							W
$R_{JA}$	Thermal Resistance, Junction to Ambient	50							$^\circ\text{C}/\text{W}$

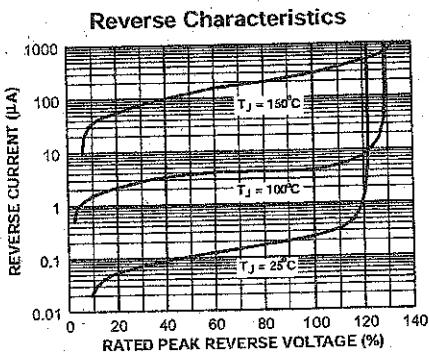
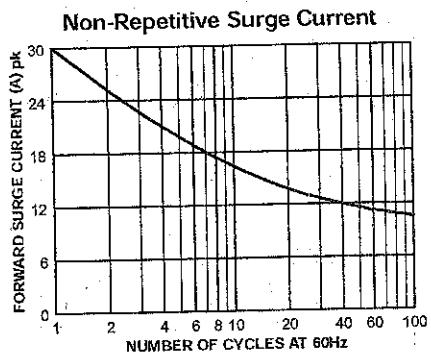
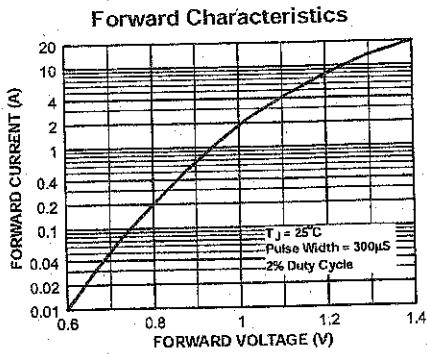
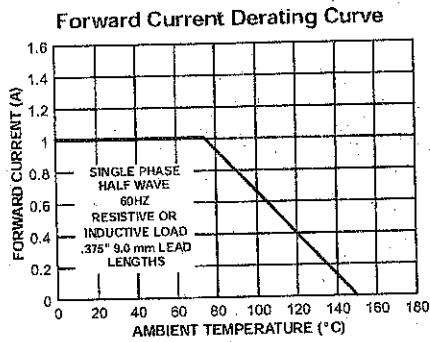
### Electrical Characteristics

 $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Device							Units
		4001	4002	4003	4004	4005	4006	4007	
$V_F$	Forward Voltage @ 1.0 A				1.1				V
$I_{rr}$	Maximum Full Load Reverse Current, Full Cycle $T_A = 75^\circ\text{C}$				30				$\mu\text{A}$
$I_R$	Reverse Current @ rated $V_R$ $T_A = 25^\circ\text{C}$ $T_A = 100^\circ\text{C}$				5.0				$\mu\text{A}$
$C_T$	Total Capacitance $V_R = 4.0 \text{ V}, f = 1.0 \text{ MHz}$				500				$\mu\text{A}$
					15				pF

## General Purpose Rectifiers (continued)

### Typical Characteristics



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## Zeners 1N957B - 1N991B

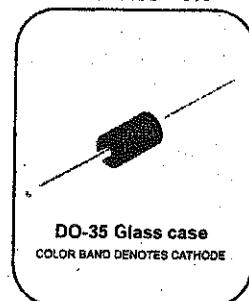
### Absolute Maximum Ratings \*

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Value	Units
$P_D$	Power Dissipation @ $T_L \leq 75^\circ\text{C}$ , Lead Length = 3/8"	500	mW
	Derate above $75^\circ\text{C}$	4.0	mW/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-65 to +200	$^\circ\text{C}$

\* These ratings are limiting values above which the serviceability of the diode may be impaired.

Tolerance = 5%



### Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Device	V <sub>Z</sub> (Volts) (Note 1)				Z <sub>Z</sub> ( $\Omega$ ) (Note 2)		I <sub>R</sub> @ V <sub>R</sub>		I <sub>ZM</sub> (mA) (Note 3)	
	Min.	Typ.	Max.	@ I <sub>Z</sub> (mA)	Z <sub>Z</sub> @ I <sub>Z</sub>	Z <sub>ZK</sub> @ I <sub>ZK</sub> $\Omega$	mA	μA	Volts	
1N957B	6.46	6.8	7.14	18.5	4.5	700	1.0	150	5.2	47
1N958B	7.125	7.5	7.875	16.5	5.5	700	0.5	75	5.7	42
1N959B	7.79	8.2	8.61	15	6.5	700	0.5	50	6.2	38
1N960B	8.645	9.1	9.555	14	7.5	700	0.5	25	6.9	35
1N961B	9.5	10	10.5	12.5	8.5	700	0.25	10	7.6	32
1N962B	10.45	11	11.55	11.5	9.5	700	0.25	5	8.4	28
1N963B	11.4	12	12.6	10.5	11.5	700	0.25	5	9.1	26
1N964B	12.35	13	13.65	9.5	13	700	0.25	5	9.9	24
1N965B	14.25	15	15.75	8.5	16	700	0.25	5	11.4	21
1N966B	15.2	16	16.8	7.8	17	700	0.25	5	12.2	19
1N967B	17.1	18	18.9	7.0	21	750	0.25	5	13.7	17
1N968B	19	20	21	6.2	25	750	0.25	5	15.2	15
1N969B	20.9	22	23.1	5.6	29	750	0.25	5	16.7	14
1N970B	22.8	24	25.2	5.2	33	750	0.25	5	18.2	13
1N971B	25.652	27	28.35	4.6	41	750	0.25	5	20.6	11
1N972B	8.5	30	31.5	4.2	49	1000	0.25	5	22.8	10
1N973B	31.35	33	34.65	3.8	58	1000	0.25	5	25.1	9.2
1N974B	34.2	36	37.8	3.4	70	1000	0.25	5	27.4	8.5
1N975B	37.05	39	40.95	3.2	80	1000	0.25	5	29.7	7.8
1N976B	40.85	43	45.15	3.0	93	1500	0.25	5	32.7	7.0
1N977B	44.65	47	49.35	2.7	105	1500	0.25	5	35.8	6.4
1N978B	48.45	51	53.55	2.5	125	1500	0.25	5	38.8	5.9
1N979B	53.2	56	58.8	2.2	150	2000	0.25	5	42.6	5.4
1N980B	58.9	62	65.1	2.0	185	2000	0.25	5	47.1	4.9
1N981B	64.6	68	71.4	1.8	230	2000	0.25	5	51.7	4.5

## Zeners 1N957B - 1N991B

**Electrical Characteristics (Continued)**  $T_A=25^\circ\text{C}$  unless otherwise noted

Device	V <sub>Z</sub> (Volts) (Note 1)				Z <sub>Z</sub> ( $\Omega$ ) (Note 2)		I <sub>R</sub> @ V <sub>R</sub>		I <sub>ZM</sub> (mA) (Note 3)	
	Min.	Typ.	Max.	@ I <sub>Z</sub>	Z <sub>Z</sub> @ I <sub>Z</sub>	Z <sub>ZK</sub> @ I <sub>ZK</sub>		$\mu\text{A}$	Volts	
						$\Omega$	mA			
1N982B	71.25	75	78.75	1.7	270	2000	0.25	5	56.0	4.1
1N983B	77.9	82	86.1	1.5	330	3000	0.25	5	62.2	3.7
1N984B	86.45	91	95.55	1.4	400	3000	0.25	5	69.2	3.3
1N985B	95	100	105	1.3	500	3000	0.25	5	76.0	3.0
1N986B	104.5	110	115.5	1.1	750	4000	0.25	5	83.6	2.7
1N987B	114	120	126	1.0	900	4500	0.25	5	91.2	2.5
1N988B	123.5	130	136.5	0.95	1100	5000	0.25	5	98.8	2.3
1N989B	142.5	150	157.5	0.85	1500	6000	0.25	5	114	2.0
1N990B	152	160	168	0.80	1700	6500	0.25	5	121.6	1.9
1N991B	171	180	189	0.68	2200	7100	0.25	5	136.8	1.7

Notes:

1. Zener Voltage (V<sub>Z</sub>) Measurement  
Nominal zener voltage is measured with the device junction in the thermal equilibrium at the lead temperature (T<sub>L</sub>) at 30°C ± 1°C and 3/8" lead length.
2. Zener Impedance (Z<sub>Z</sub>) Derivation  
Z<sub>Z</sub> and Z<sub>ZK</sub> are measured by dividing the ac voltage drop across the device by the ac current applied. The specified limits are for I<sub>Z(zo)</sub> = 0.1 I<sub>Z(dc)</sub> with the ac frequency = 60Hz.
3. Maximum Zener Current Ratings (I<sub>ZM</sub>)  
The maximum current handling capability on a worst case basis is limited by the actual zener voltage at the operation point and the power derating curve.

# 1N4728A - 1N4764A

## Zeners



DO-41 Glass-case  
COLOR BAND DENOTES CATHODE

### Absolute Maximum Ratings \* $T_a = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
$P_D$	Power Dissipation @ $T_L \leq 50^\circ\text{C}$ , Lead Length = 3/8"	1.0	W
	Derate above $50^\circ\text{C}$	6.67	mW/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-65 to +200	$^\circ\text{C}$

\* These ratings are limiting values above which the serviceability of the diode may be impaired.

### Electrical Characteristics $T_a = 25^\circ\text{C}$ unless otherwise noted

Device	V <sub>Z</sub> (V) @ I <sub>Z</sub> (Note 1)			Test Current I <sub>Z</sub> (mA)	Max. Zener Impedance			Leakage Current	
	Min.	Typ.	Max.		Z <sub>Z</sub> @ I <sub>Z</sub> ( $\Omega$ )	Z <sub>ZK</sub> @ I <sub>ZK</sub> ( $\Omega$ )	I <sub>ZK</sub> (mA)	I <sub>R</sub> ( $\mu\text{A}$ )	V <sub>R</sub> (V)
1N4728A	3.315	3.3	3.465	76	10	400	1	100	1
1N4729A	3.42	3.6	3.78	69	10	400	1	100	1
1N4730A	3.705	3.9	4.095	64	9	400	1	50	1
1N4731A	4.085	4.3	4.515	58	9	400	1	10	1
1N4732A	4.465	4.7	4.935	53	8	500	1	10	1
1N4733A	4.845	5.1	5.355	49	7	550	1	10	1
1N4734A	5.32	5.6	5.88	45	5	600	1	10	2
1N4735A	5.89	6.2	6.51	41	2	700	1	10	3
1N4736A	6.46	6.8	7.14	37	3.5	700	1	10	4
1N4737A	7.125	7.5	7.875	34	4	700	0.5	10	5
1N4738A	7.79	8.2	8.61	31	4.5	700	0.5	10	6
1N4739A	8.645	9.1	9.555	28	5	700	0.5	10	7
1N4740A	9.5	10	10.5	25	7	700	0.25	10	7.6
1N4741A	10.45	11	11.55	23	8	700	0.25	5	8.4
1N4742A	11.4	12	12.6	21	9	700	0.25	5	9.1
1N4743A	12.35	13	13.65	19	10	700	0.25	5	9.9
1N4744A	14.25	15	15.75	17	14	700	0.25	5	11.4
1N4745A	15.2	16	16.8	15.5	16	700	0.25	5	12.2
1N4746A	17.1	18	18.9	14	20	750	0.25	5	13.7
1N4747A	19	20	21	12.5	22	750	0.25	5	15.2

**Electrical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Device	V <sub>Z</sub> (V) @ I <sub>Z</sub> (Note 1)			Test Current I <sub>Z</sub> (mA)	Max. Zener Impedance			Leakage Current	
	Min.	Typ.	Max.		Z <sub>Z</sub> @ I <sub>Z</sub> (Ω)	Z <sub>ZK</sub> @ I <sub>ZK</sub> (Ω)	I <sub>ZK</sub> (mA)	I <sub>R</sub> (μA)	V <sub>R</sub> (V)
1N4748A	20.9	22	23.1	11.5	23	750	0.25	5	16.7
1N4749A	22.8	24	25.2	10.5	25	750	0.25	5	18.2
1N4750A	25.65	27	28.35	9.5	35	750	0.25	5	20.6
1N4751A	28.5	30	31.5	8.5	40	1000	0.25	5	22.8
1N4752A	31.35	33	34.65	7.5	45	1000	0.25	5	25.1
1N4753A	34.2	36	37.8	7	50	1000	0.25	5	27.4
1N4754A	37.05	39	40.95	6.5	60	1000	0.25	5	29.7
1N4755A	40.85	43	45.15	6	70	1500	0.25	5	32.7
1N4756A	44.85	47	49.35	5.5	80	1500	0.25	5	35.8
1N4757A	48.45	51	53.65	5	95	1500	0.25	5	38.8
1N4758A	53.2	56	58.8	4.5	110	2000	0.25	5	42.6
1N4759A	58.9	62	65.1	4	125	2000	0.25	5	47.1
1N4760A	64.6	68	71.4	3.7	150	2000	0.25	5	51.7
1N4761A	71.25	75	78.75	3.3	175	2000	0.25	5	56
1N4762A	77.9	82	86.1	3	200	3000	0.25	5	62.2
1N4763A	86.45	91	95.55	2.8	250	3000	0.25	5	69.2
1N4764A	95	100	105	2.5	350	3000	0.25	5	76

## Notes:

1. Zener Voltage (V<sub>Z</sub>)  
The zener voltage is measured with the device junction in the thermal equilibrium at the lead temperature ( $T_L$ ) at  $30^\circ\text{C} \pm 1^\circ\text{C}$  and 3/8" lead length.

# 2N3903, 2N3904

2N3903 is a Preferred Device

## General Purpose Transistors

### NPN Silicon

#### Features

- Pb-Free Packages are Available\*

#### MAXIMUM RATINGS

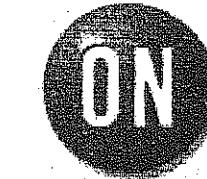
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	40	Vdc
Collector-Base Voltage	$V_{CBO}$	60	Vdc
Emitter-Base Voltage	$V_{EBO}$	6.0	Vdc
Collector Current - Continuous	$I_C$	200	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	625 5.0	mW mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.5 12	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{Stg}$	-55 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

#### THERMAL CHARACTERISTICS (Note 1)

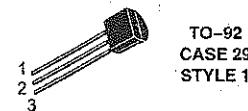
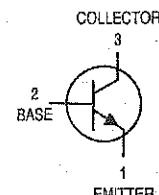
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\thetaJA}$	200	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case	$R_{\thetaJC}$	83.3	$^\circ\text{C}/\text{W}$

1. Indicates Data in addition to JEDEC Requirements.

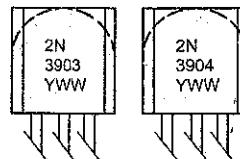


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#### MARKING DIAGRAMS



Y = Year  
WW = Work Week

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERMM/D.

## 2N3903, 2N3904

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Breakdown Voltage (Note 2) ( $I_C = 1.0 \text{ mA DC}, I_B = 0$ )	$V_{(\text{BR})\text{CEO}}$	40	—	Vdc
Collector-Base Breakdown Voltage ( $I_C = 10 \mu\text{A DC}, I_E = 0$ )	$V_{(\text{BR})\text{CBO}}$	60	—	Vdc
Emitter-Base Breakdown Voltage ( $I_E = 10 \mu\text{A DC}, I_C = 0$ )	$V_{(\text{BR})\text{EBO}}$	6.0	—	Vdc
Base Cutoff Current ( $V_{CE} = 30 \text{ Vdc}, V_{EB} = 3.0 \text{ Vdc}$ )	$I_{BL}$	—	50	nA DC
Collector Cutoff Current ( $V_{CE} = 30 \text{ Vdc}, V_{EB} = 3.0 \text{ Vdc}$ )	$I_{CEX}$	—	50	nA DC
<b>ON CHARACTERISTICS</b>				
DC Current Gain (Note 2) ( $I_C = 0.1 \text{ mA DC}, V_{CE} = 1.0 \text{ Vdc}$ )	$h_{FE}$ 2N3903 2N3904	20 40	—	—
( $I_C = 1.0 \text{ mA DC}, V_{CE} = 1.0 \text{ Vdc}$ )	$h_{FE}$ 2N3903 2N3904	35 70	—	—
( $I_C = 10 \text{ mA DC}, V_{CE} = 1.0 \text{ Vdc}$ )	$h_{FE}$ 2N3903 2N3904	50 100	150 300	—
( $I_C = 50 \text{ mA DC}, V_{CE} = 1.0 \text{ Vdc}$ )	$h_{FE}$ 2N3903 2N3904	30 60	—	—
( $I_C = 100 \text{ mA DC}, V_{CE} = 1.0 \text{ Vdc}$ )	$h_{FE}$ 2N3903 2N3904	15 30	—	—
Collector-Emitter Saturation Voltage (Note 2) ( $I_C = 10 \text{ mA DC}, I_B = 1.0 \text{ mA DC}$ ) ( $I_C = 50 \text{ mA DC}, I_B = 5.0 \text{ mA DC}$ )	$V_{CE(\text{sat})}$	— —	0.2 0.3	Vdc
Base-Emitter Saturation Voltage (Note 2) ( $I_C = 10 \text{ mA DC}, I_B = 1.0 \text{ mA DC}$ ) ( $I_C = 50 \text{ mA DC}, I_B = 5.0 \text{ mA DC}$ )	$V_{BE(\text{sat})}$	0.65 —	0.85 0.95	Vdc
<b>SMALL-SIGNAL CHARACTERISTICS</b>				
Current-Gain-Bandwidth Product ( $I_C = 10 \text{ mA DC}, V_{CE} = 20 \text{ Vdc}, f = 100 \text{ MHz}$ )	$f_T$ 2N3903 2N3904	250 300	—	MHz
Output Capacitance ( $V_{CB} = 5.0 \text{ Vdc}, I_E = 0, f = 1.0 \text{ MHz}$ )	$C_{o\text{bo}}$	—	4.0	pF
Input Capacitance ( $V_{EB} = 0.5 \text{ Vdc}, I_C = 0, f = 1.0 \text{ MHz}$ )	$C_{i\text{bo}}$	—	8.0	pF
Input Impedance ( $I_C = 1.0 \text{ mA DC}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}$ )	$h_{ie}$ 2N3903 2N3904	1.0 1.0	8.0 10	kΩ
Voltage Feedback Ratio ( $I_C = 1.0 \text{ mA DC}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}$ )	$h_{re}$ 2N3903 2N3904	0.1 0.5	5.0 8.0	$\times 10^{-4}$
Small-Signal Current Gain ( $I_C = 1.0 \text{ mA DC}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}$ )	$h_{fe}$ 2N3903 2N3904	50 100	200 400	—
Output Admittance ( $I_C = 1.0 \text{ mA DC}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}$ )	$h_{oe}$	1.0	40	μmhos
Noise Figure ( $I_C = 100 \mu\text{A DC}, V_{CE} = 5.0 \text{ Vdc}, R_S = 1.0 \text{ k}\Omega, f = 1.0 \text{ kHz}$ )	NF 2N3903 2N3904	— —	6.0 5.0	dB
<b>SWITCHING CHARACTERISTICS</b>				
Delay Time	$t_d$	—	35	ns
Rise Time	$t_r$	—	35	ns
Storage Time	$t_s$ 2N3903 2N3904	— —	175 200	ns
Fall Time	$t_f$	—	50	ns

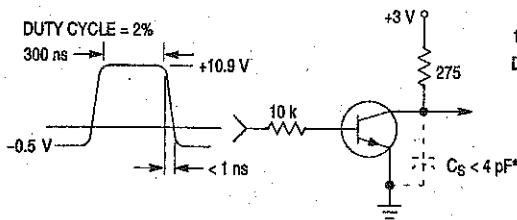
2. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ ; Duty Cycle  $\leq 2\%$ .

## 2N3903, 2N3904

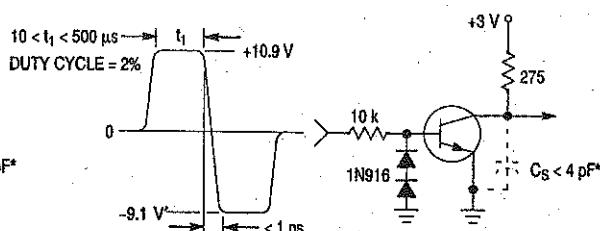
### ORDERING INFORMATION

Device	Package	Shipping†
2N3903	TO-92	5,000 Units / Box
2N3903RLRM	TO-92	2,000 / Ammo Pack
2N3904	TO-92	5,000 Units / Box
2N3904G	TO-92 (Pb-Free)	5,000 Units / Box
2N3904RLRA	TO-92	2,000 / Tape & Reel
2N3904RLRAG	TO-92 (Pb-Free)	2,000 / Tape & Reel
2N3904RLRE	TO-92	2,000 / Tape & Reel
2N3904RLRM	TO-92	2,000 / Ammo Pack
2N3904RLRMG	TO-92 (Pb-Free)	2,000 / Ammo Pack
2N3904RLRP	TO-92	2,000 / Ammo Pack
2N3904RLRPG	TO-92 (Pb-Free)	2,000 / Ammo Pack
2N3904RL1	TO-92	2,000 / Tape & Reel
2N3904ZL1	TO-92	2,000 / Ammo Pack

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



**Figure 1. Delay and Rise Time  
Equivalent Test Circuit**



**Figure 2. Storage and Fall Time  
Equivalent Test Circuit**

# 2N3903, 2N3904

## TYPICAL TRANSIENT CHARACTERISTICS

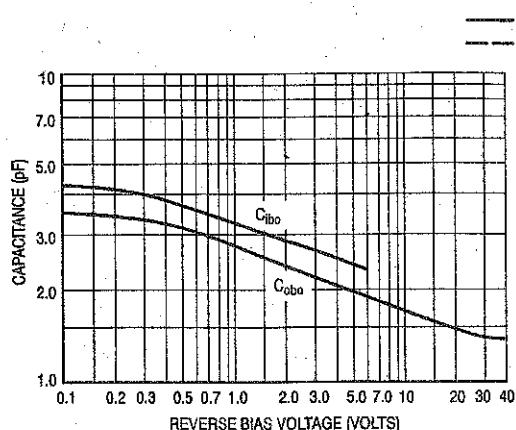


Figure 3. Capacitance

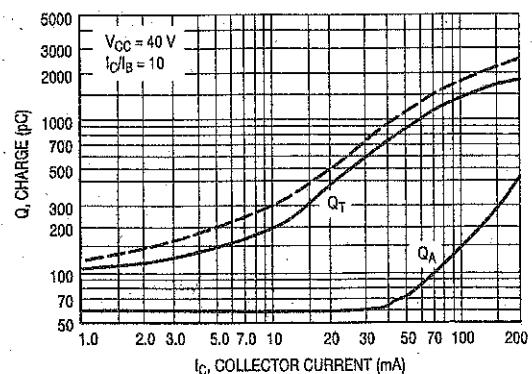


Figure 4. Charge Data

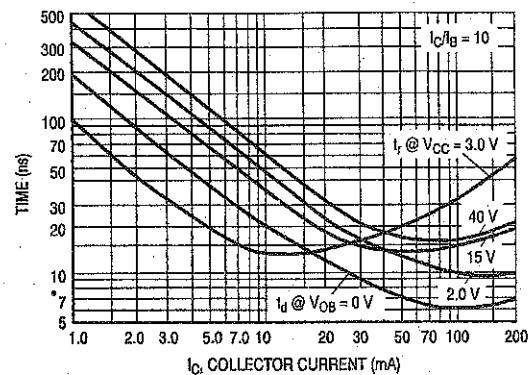


Figure 5. Turn-On Time

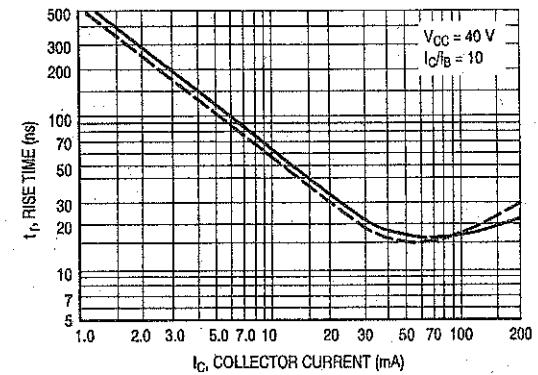


Figure 6. Rise Time

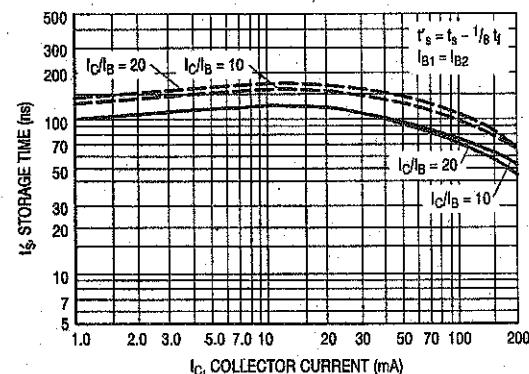


Figure 7. Storage Time

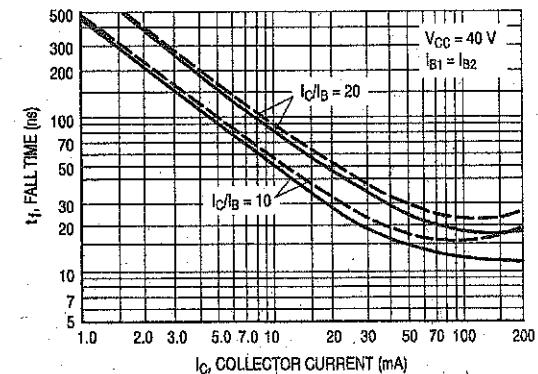


Figure 8. Fall Time

## 2N3903, 2N3904

### TYPICAL AUDIO SMALL-SIGNAL CHARACTERISTICS NOISE FIGURE VARIATIONS

( $V_{CE} = 5.0$  Vdc,  $T_A = 25^\circ\text{C}$ , Bandwidth = 1.0 Hz)

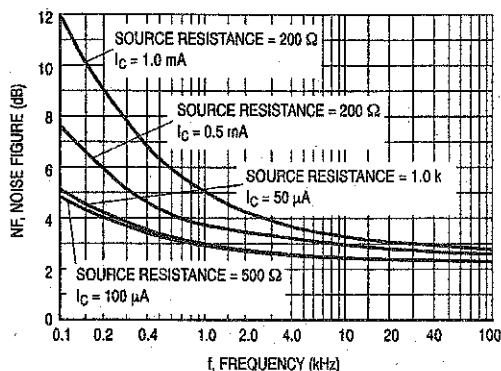


Figure 9.

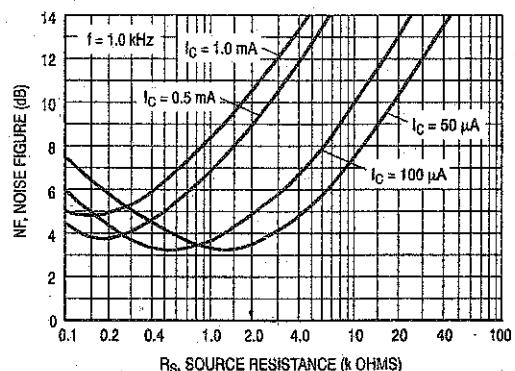


Figure 10.

### $h$ PARAMETERS

( $V_{CE} = 10$  Vdc,  $f = 1.0$  kHz,  $T_A = 25^\circ\text{C}$ )

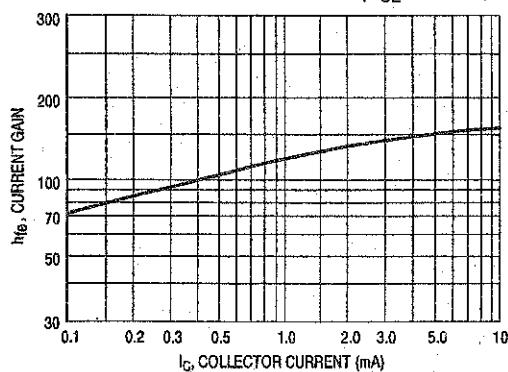


Figure 11. Current Gain

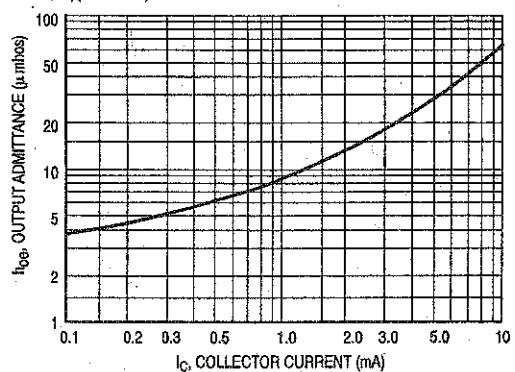


Figure 12. Output Admittance

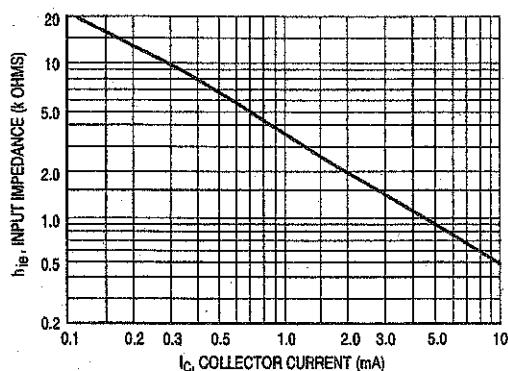


Figure 13. Input Impedance

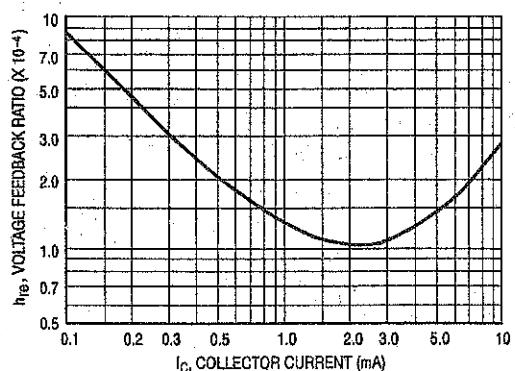


Figure 14. Voltage Feedback Ratio

## 2N3903, 2N3904

### TYPICAL STATIC CHARACTERISTICS

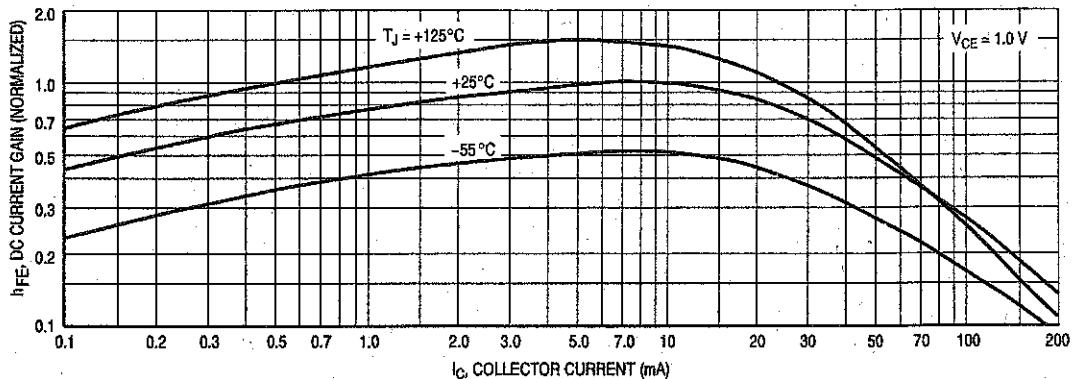


Figure 15. DC Current Gain

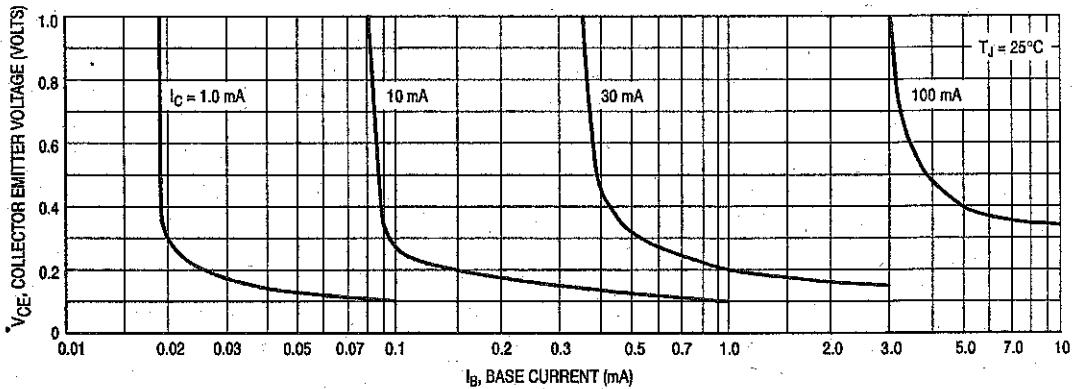


Figure 16. Collector Saturation Region

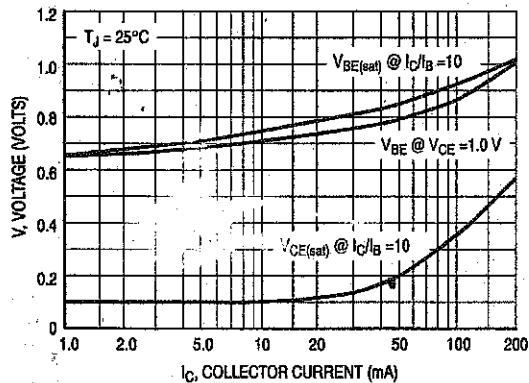


Figure 17. "ON" Voltages

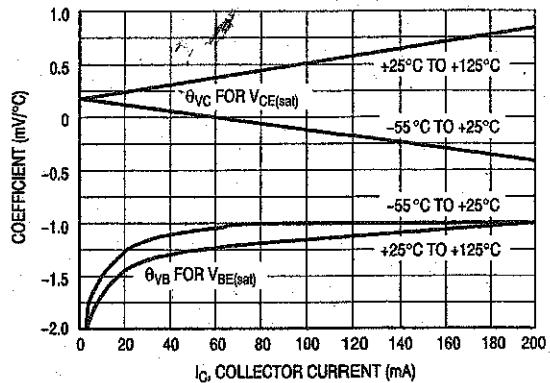


Figure 18. Temperature Coefficients

# 2N3906

Preferred Device

## General Purpose Transistors

### PNP Silicon

#### Features

- Pb-Free Packages are Available\*

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector - Emitter Voltage	V <sub>CEO</sub>	40	Vdc
Collector - Base Voltage	V <sub>CBO</sub>	40	Vdc
Emitter - Base Voltage	V <sub>EBO</sub>	-5.0	Vdc
Collector Current - Continuous	I <sub>C</sub>	200	mAdc
Total Device Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	625 5.0	mW mW/°C
Total Power Dissipation @ T <sub>A</sub> = 60°C	P <sub>D</sub>	250	mW
Total Device Dissipation* @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C

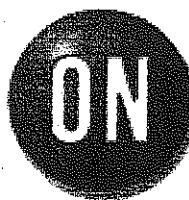
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

#### THERMAL CHARACTERISTICS (Note 1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	200	°C/W
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	83.3	°C/W

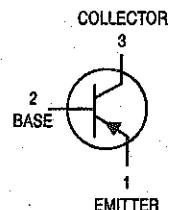
1. Indicates Data in addition to JEDEC Requirements.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

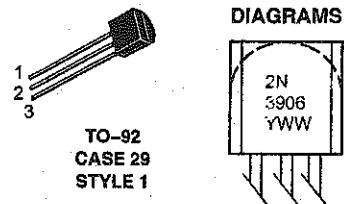


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#### MARKING DIAGRAMS



Y = Year  
WW = Work Week

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

## 2N3906

ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Breakdown Voltage (Note 2) ( $I_C = 1.0 \text{ mA DC}, I_B = 0$ )	$V_{(\text{BR})\text{CEO}}$	40	—	Vdc
Collector-Base Breakdown Voltage ( $I_C = 10 \mu\text{A DC}, I_E = 0$ )	$V_{(\text{BR})\text{CBO}}$	40	—	Vdc
Emitter-Base Breakdown Voltage ( $I_E = 10 \mu\text{A DC}, I_C = 0$ )	$V_{(\text{BR})\text{EBO}}$	5.0	—	Vdc
Base Cutoff Current ( $V_{CE} = 30 \text{ Vdc}, V_{EB} = 3.0 \text{ Vdc}$ )	$I_{BL}$	—	50	nAdc
Collector Cutoff Current ( $V_{CE} = 30 \text{ Vdc}, V_{EB} = 3.0 \text{ Vdc}$ )	$I_{CEX}$	—	50	nAdc

ON CHARACTERISTICS (Note 2)

DC Current Gain ( $I_C = 0.1 \text{ mA DC}, V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 1.0 \text{ mA DC}, V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 10 \text{ mA DC}, V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 50 \text{ mA DC}, V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 100 \text{ mA DC}, V_{CE} = 1.0 \text{ Vdc}$ )	$h_{FE}$	60 80 100 60 30	— — 300 — —	—
Collector-Emitter Saturation Voltage ( $I_C = 10 \text{ mA DC}, I_B = 1.0 \text{ mA DC}$ ) ( $I_C = 50 \text{ mA DC}, I_B = 5.0 \text{ mA DC}$ )	$V_{CE(\text{sat})}$	— —	0.25 0.4	Vdc
Base-Emitter Saturation Voltage ( $I_C = 10 \text{ mA DC}, I_B = 1.0 \text{ mA DC}$ ) ( $I_C = 50 \text{ mA DC}, I_B = 5.0 \text{ mA DC}$ )	$V_{BE(\text{sat})}$	0.65 —	0.85 0.95	Vdc

### SMALL-SIGNAL CHARACTERISTICS

Current-Gain - Bandwidth Product ( $I_C = 10 \text{ mA DC}, V_{CE} = 20 \text{ Vdc}, f = 100 \text{ MHz}$ )	$f_T$	250	—	MHz
Output Capacitance ( $V_{CB} = 5.0 \text{ Vdc}, I_E = 0, f = 1.0 \text{ MHz}$ )	$C_{cbo}$	—	4.5	pF
Input Capacitance ( $V_{EB} = 0.5 \text{ Vdc}, I_C = 0, f = 1.0 \text{ MHz}$ )	$C_{ibo}$	—	10	pF
Input Impedance ( $I_C = 1.0 \text{ mA DC}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}$ )	$h_{ie}$	2.0	12	k $\Omega$
Voltage Feedback Ratio ( $I_C = 1.0 \text{ mA DC}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}$ )	$h_{re}$	0.1	10	$\times 10^{-4}$
Small-Signal Current Gain ( $I_C = 1.0 \text{ mA DC}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}$ )	$h_{fe}$	100	400	—
Output Admittance ( $I_C = 1.0 \text{ mA DC}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}$ )	$h_{oe}$	3.0	60	$\mu\text{mhos}$
Noise Figure ( $I_C = 100 \mu\text{A DC}, V_{CE} = 5.0 \text{ Vdc}, R_S = 1.0 \text{ k}\Omega, f = 1.0 \text{ kHz}$ )	NF	—	4.0	dB

### SWITCHING CHARACTERISTICS

Delay Time	( $V_{CC} = 3.0 \text{ Vdc}, V_{BE} = 0.5 \text{ Vdc}, I_C = 10 \text{ mA DC}, I_{B1} = 1.0 \text{ mA DC}$ )	$t_d$	—	35	ns
Rise Time	( $V_{CC} = 3.0 \text{ Vdc}, I_C = 10 \text{ mA DC}, I_{B1} = 1.0 \text{ mA DC}$ )	$t_r$	—	35	ns
Storage Time	( $V_{CC} = 3.0 \text{ Vdc}, I_C = 10 \text{ mA DC}, I_{B1} = I_{B2} = 1.0 \text{ mA DC}$ )	$t_s$	—	225	ns
Fall Time	( $V_{CC} = 3.0 \text{ Vdc}, I_C = 10 \text{ mA DC}, I_{B1} = I_{B2} = 1.0 \text{ mA DC}$ )	$t_f$	—	75	ns

2. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ ; Duty Cycle  $\leq 2\%$ .

### ORDERING INFORMATION

Device	Package	Shipping†
2N3906	TO-92	5,000 Units / Box
2N3906G	TO-92 (Pb-Free)	5,000 Units / Box
2N3906RL1	TO-92	5,000 Units / Box
2N3906RLRA	TO-92	2,000 / Tape & Reel
2N3906RLRAG	TO-92 (Pb-Free)	2,000 / Tape & Reel
2N3906RLRM	TO-92	2,000 / Ammo Pack
2N3906RLRMG	TO-92 (Pb-Free)	2,000 / Ammo Pack
2N3906RLRP	TO-92	2,000 / Tape & Reel
2N3906ZL1	TO-92	2,000 / Ammo Pack

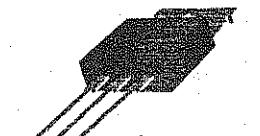
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**FAIRCHILD**  
SEMICONDUCTOR®

## TIP100/101/102

### Monolithic Construction With Built In Base-Emitter Shunt Resistors

- High DC Current Gain :  $h_{FE}=1000$  @  $V_{CE}=4V$ ,  $I_C=3A$  (Min.)
- Collector-Emitter Sustaining Voltage
- Low Collector-Emitter Saturation Voltage
- Industrial Use
- Complementary to TIP105/106/107

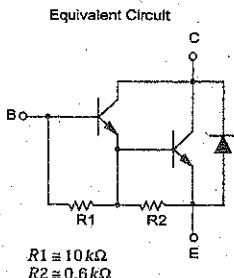


1. Base 2. Collector 3. Emitter

### NPN Epitaxial Silicon Darlington Transistor

#### Absolute Maximum Ratings $T_C=25^\circ C$ unless otherwise noted

Symbol	Parameter	Value	Units
$V_{CBO}$	Collector-Base Voltage : TIP100	60	V
	: TIP101	80	V
	: TIP102	100	V
$V_{CEO}$	Collector-Emitter Voltage : TIP100	60	V
	: TIP101	80	V
	: TIP102	100	V
$V_{EBO}$	Emitter-Base Voltage	5	V
$I_C$	Collector Current (DC)	8	A
$I_{CP}$	Collector Current (Pulse)	15	A
$I_B$	Base Current (DC)	1	A
$P_C$	Collector Dissipation ( $T_a=25^\circ C$ )	2	W
	Collector Dissipation ( $T_c=25^\circ C$ )	80	W
$T_J$	Junction Temperature	150	°C
$T_{STG}$	Storage Temperature	-65 ~ 150	°C



$R1 \approx 10\text{ k}\Omega$   
 $R2 \approx 0.6\text{ k}\Omega$

#### Electrical Characteristics $T_C=25^\circ C$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage : TIP100	$I_C = 30\text{ mA}$ , $I_B = 0$	60		V
	: TIP101		80		V
	: TIP102		100		V
$I_{CEO}$	Collector Cut-off Current : TIP100	$V_{CE} = 30\text{ V}$ , $I_E = 0$		50	$\mu\text{A}$
	: TIP101	$V_{CE} = 40\text{ V}$ , $I_E = 0$		50	$\mu\text{A}$
	: TIP102	$V_{CE} = 50\text{ V}$ , $I_E = 0$		50	$\mu\text{A}$
$I_{CBO}$	Collector Cut-off Current : TIP100	$V_{CE} = 60\text{ V}$ , $I_E = 0$		50	$\mu\text{A}$
	: TIP101	$V_{CE} = 80\text{ V}$ , $I_E = 0$		50	$\mu\text{A}$
	: TIP102	$V_{CE} = 100\text{ V}$ , $I_E = 0$		50	$\mu\text{A}$
$I_{EBO}$	Emitter Cut-off Current	$V_{EB} = 5\text{ V}$ , $I_C = 0$		2	mA
$h_{FE}$	DC Current Gain	$V_{CE} = 4\text{ V}$ , $I_C = 3\text{ A}$	1000	20000	
		$V_{CE} = 4\text{ V}$ , $I_C = 8\text{ A}$	200		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 3\text{ A}$ , $I_E = 6\text{ mA}$		2	V
		$I_C = 8\text{ A}$ , $I_E = 80\text{ mA}$		2.5	V
$V_{BE(on)}$	Base-Emitter ON Voltage	$V_{CE} = 4\text{ V}$ , $I_C = 8\text{ A}$		2.8	V
$C_{ob}$	Output Capacitance	$V_{CB} = 10\text{ V}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$		200	pF

## Typical Characteristics

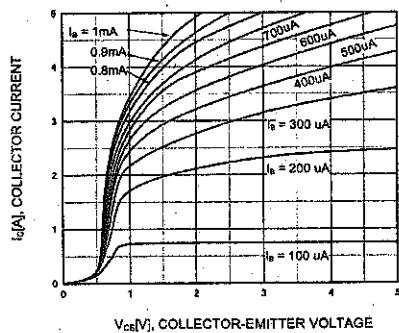


Figure 1. Static Characteristic

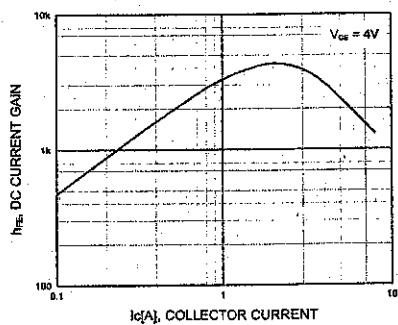


Figure 2. DC current Gain

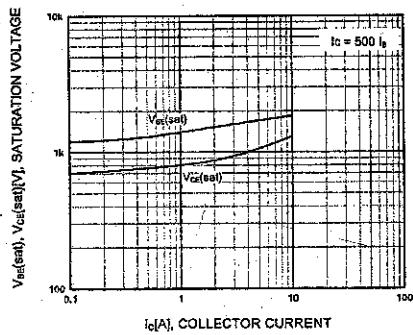
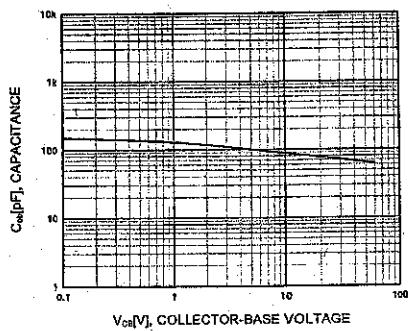
Figure 3. Collector-Emitter Saturation Voltage  
Base-Emitter Saturation Voltage

Figure 4. Collector Output Capacitance

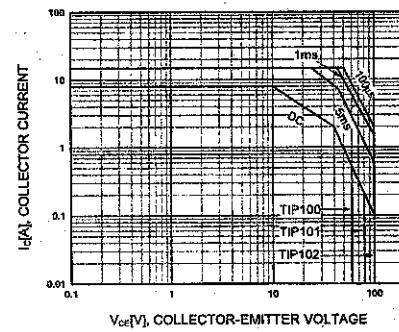


Figure 5. Safe Operating Area

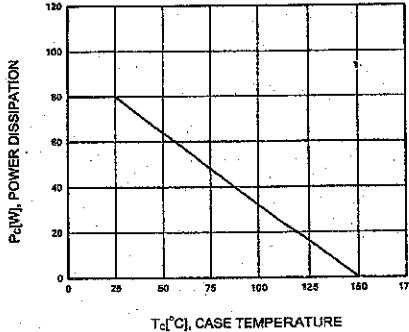


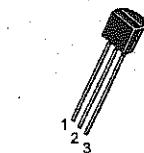
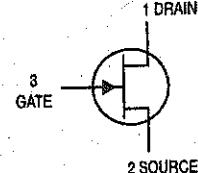
Figure 6. Power Derating

## JFET VHF Amplifier

### N-Channel – Depletion

**MPF102****MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain–Source Voltage	V <sub>DS</sub>	25	Vdc
Drain–Gate Voltage	V <sub>DG</sub>	25	Vdc
Gate–Source Voltage	V <sub>GS</sub>	-25	Vdc
Gate Current	I <sub>G</sub>	10	mAdc
Total Device Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	350 2.8	mW mW/°C
Junction Temperature Range	T <sub>J</sub>	125	°C
Storage Temperature Range	T <sub>Stg</sub>	-65 to +150	°C

CASE 28-11, STYLE 5  
TO-92 (TO-226AA)**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)**

Characteristic	Symbol	Min	Max	Unit
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**OFF CHARACTERISTICS**

Gate–Source Breakdown Voltage (I <sub>G</sub> = -10 μAdc, V <sub>DS</sub> = 0)	V <sub>(BR)GSS</sub>	-25	—	Vdc
Gate Reverse Current (V <sub>GS</sub> = -15 Vdc, V <sub>DS</sub> = 0) (V <sub>GS</sub> = -15 Vdc, V <sub>DS</sub> = 0, T <sub>A</sub> = 100°C)	I <sub>GSS</sub>	— —	-2.0 -2.0	nAdc μAdc
Gate–Source Cutoff Voltage (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 2.0 nAdc)	V <sub>GS(off)</sub>	—	-8.0	Vdc
Gate–Source Voltage (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 0.2 mAdc)	V <sub>GS</sub>	-0.5	-7.5	Vdc

**ON CHARACTERISTICS**

Zero–Gate–Voltage Drain Current <sup>(1)</sup> (V <sub>DS</sub> = 15 Vdc, V <sub>GS</sub> = 0 Vdc)	I <sub>DSS</sub>	2.0	20	mAdc
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**SMALL-SIGNAL CHARACTERISTICS**

Forward Transfer Admittance <sup>(1)</sup> (V <sub>DS</sub> = 15 Vdc, V <sub>GS</sub> = 0, f = 1.0 kHz) (V <sub>DS</sub> = 15 Vdc, V <sub>GS</sub> = 0, f = 100 MHz)	y <sub>fs</sub>	2000 1600	7500	μmhos
Input Admittance (V <sub>DS</sub> = 15 Vdc, V <sub>GS</sub> = 0, f = 100 MHz)	Re(y <sub>is</sub> )	--	800	μmhos
Output Conductance (V <sub>DS</sub> = 15 Vdc, V <sub>GS</sub> = 0, f = 100 MHz)	Re(y <sub>os</sub> )	--	200	μmhos
Input Capacitance (V <sub>DS</sub> = 15 Vdc, V <sub>GS</sub> = 0, f = 1.0 MHz)	C <sub>iss</sub>	--	7.0	pF
Reverse Transfer Capacitance (V <sub>DS</sub> = 15 Vdc, V <sub>GS</sub> = 0, f = 1.0 MHz)	C <sub>rss</sub>	--	3.0	pF

1. Pulse Test; Pulse Width ≤ 630 ns, Duty Cycle ≤ 10%.

# MPF102

## COMMON SOURCE CHARACTERISTICS

### \* ADMITTANCE PARAMETERS

$(V_{DS} = 15 \text{ Vdc}, T_{\text{channel}} = 25^\circ\text{C})$

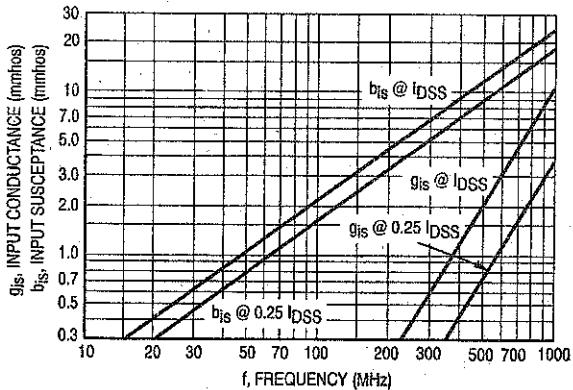


Figure 1. Input Admittance ( $y_{is}$ )

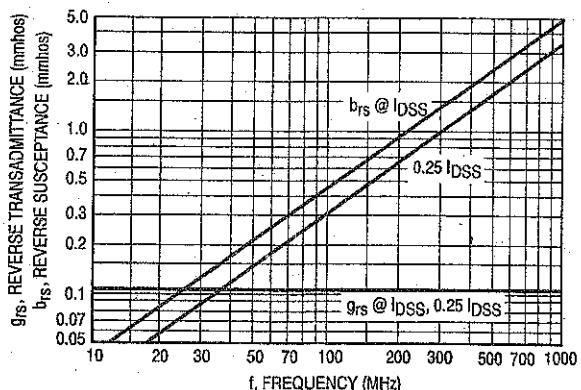


Figure 2. Reverse Transfer Admittance ( $y_{rs}$ )

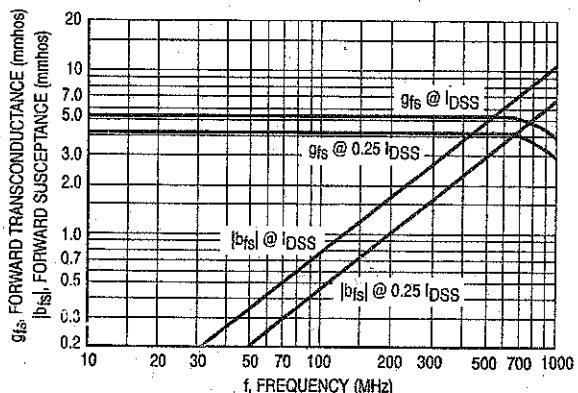


Figure 3. Forward Transadmittance ( $y_{tf}$ )

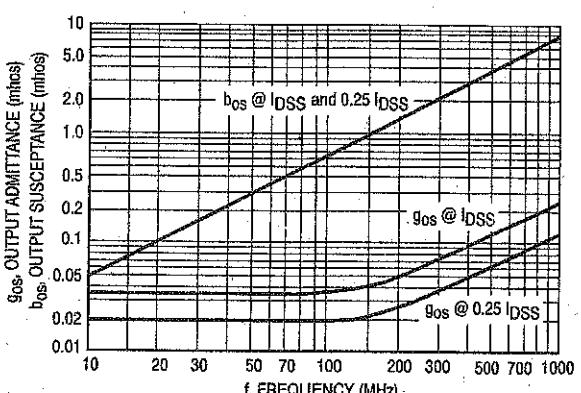


Figure 4. Output Admittance ( $y_{os}$ )

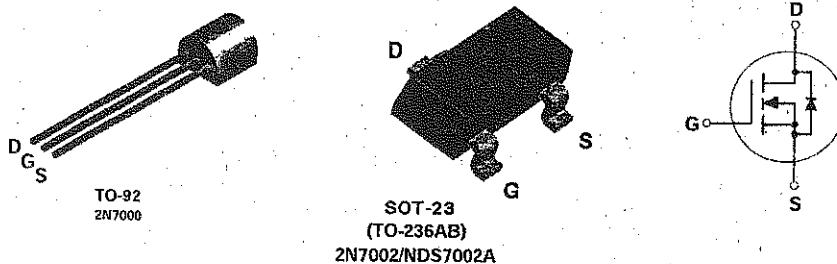
## 2N7000 / 2N7002 / NDS7002A N-Channel Enhancement Mode Field Effect Transistor

### General Description

These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 400mA DC and can deliver pulsed currents up to 2A. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

### Features

- High density cell design for low  $R_{DS(on)}$ .
- Voltage controlled small signal switch.
- Rugged and reliable.
- High saturation current capability.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	2N7000	2N7002	NDS7002A	Units
$V_{DSS}$	Drain-Source Voltage		60		V
$V_{DGR}$	Drain-Gate Voltage ( $R_{GS} \leq 1 \text{ M}\Omega$ )		60		V
$V_{GS}$	Gate-Source Voltage - Continuous - Non Repetitive ( $t_p < 50\mu\text{s}$ )		$\pm 20$	$\pm 40$	V
$I_D$	Maximum Drain Current - Continuous	200	115	280	mA
	- Pulsed	.500	800	1500	
$P_D$	Maximum Power Dissipation	400	200	300	mW
	Derated above $25^\circ\text{C}$	3.2	1.6	2.4	mW/ $^\circ\text{C}$
$T_J, T_{STO}$	Operating and Storage Temperature Range	-55 to 150		-65 to 150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300			$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{QJA}$	Thermal Resistance, Junction-to-Ambient	312.5	625	417	$^\circ\text{C/W}$
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**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \mu\text{A}$	All	60			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$	2N7000			'1	$\mu\text{A}$
		$T_J = 125^\circ\text{C}$				1	mA
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$	2N7002 NDS7002A			1	$\mu\text{A}$
$I_{GSSF}$	Gate - Body-Leakage, Forward	$T_J = 125^\circ\text{C}$				0.5	mA
		$V_{GS} = 15 \text{ V}, V_{DS} = 0 \text{ V}$	2N7000			10	nA
		$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	2N7002 NDS7002A			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -15 \text{ V}, V_{DS} = 0 \text{ V}$	2N7000			-10	nA
		$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$	2N7002 NDS7002A			-100	nA
<b>ON CHARACTERISTICS</b> (Note 1)							
$V_{GS(H)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1 \text{ mA}$	2N7000	0.8	2.1	3	V
		$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2N7002 NDS7002A	1	2.1	2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$	2N7000		1.2	5	$\Omega$
		$T_J = 125^\circ\text{C}$			1.9	9	
		$V_{GS} = 4.5 \text{ V}, I_D = 75 \text{ mA}$			1.8	5.3	
		$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$	2N7002		1.2	7.5	
		$T_J = 100^\circ\text{C}$			1.7	13.5	
		$V_{GS} = 5.0 \text{ V}, I_D = 50 \text{ mA}$			1.7	7.5	
		$T_J = 100^\circ\text{C}$			2.4	13.5	
		$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$	NDS7002A		1.2	2	
		$T_J = 125^\circ\text{C}$			2	3.5	
		$V_{GS} = 5.0 \text{ V}, I_D = 50 \text{ mA}$			1.7	3	
		$T_J = 125^\circ\text{C}$			2.8	5	
$V_{DS(ON)}$	Drain-Source On-Voltage	$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$	2N7000		0.6	2.5	$\text{V}$
		$V_{GS} = 4.5 \text{ V}, I_D = 75 \text{ mA}$			0.14	0.4	
		$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$	2N7002		0.6	3.75	
		$V_{GS} = 5.0 \text{ V}, I_D = 50 \text{ mA}$			0.09	1.5	
		$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$	NDS7002A		0.6	1	
		$V_{GS} = 5.0 \text{ V}, I_D = 50 \text{ mA}$			0.09	0.15	

2N7000, SAM Rev. A1

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
<b>ON CHARACTERISTICS Continued (Note 1)</b>							
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5 \text{ V}$ , $V_{DS} = 10 \text{ V}$	2N7000	75	600		mA
		$V_{GS} = 10 \text{ V}$ , $V_{DS} \geq 2 V_{DS(on)}$	2N7002	500	2700		
		$V_{GS} = 10 \text{ V}$ , $V_{DS} \geq 2 V_{DS(on)}$	NDS7002A	.500	2700		
$g_{FS}$	Forward Transconductance	$V_{DS} = 10 \text{ V}$ , $I_D = 200 \text{ mA}$	2N7000	100	320		mS
		$V_{DS} \geq 2 V_{DS(on)}$ , $I_D = 200 \text{ mA}$	2N7002	80	320		
		$V_{DS} \geq 2 V_{DS(on)}$ , $I_D = 200 \text{ mA}$	NDS7002A	80	320		
<b>DYNAMIC CHARACTERISTICS</b>							
$C_{iss}$	Input Capacitance	$V_{DS} = 25 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1.0 \text{ MHz}$	All		20	50	pF
$C_{oss}$	Output Capacitance		All		11	25	pF
$C_{ras}$	Reverse Transfer Capacitance		All		4	5	pF
$t_{on}$	Turn-On Time	$V_{DD} = 15 \text{ V}$ , $R_L = 25 \Omega$ , $I_D = 500 \text{ mA}$ , $V_{GS} = 10 \text{ V}$ , $R_{GEN} = 25 \Omega$	2N7000			10	ns
		$V_{DD} = 30 \text{ V}$ , $R_L = 150 \Omega$ , $I_D = 200 \text{ mA}$ , $V_{GS} = 10 \text{ V}$ , $R_{GEN} = 25 \Omega$	2N7002			20	ns
$t_{off}$	Turn-Off Time	$V_{DD} = 15 \text{ V}$ , $R_L = 25 \Omega$ , $I_D = 500 \text{ mA}$ , $V_{GS} = 10 \text{ V}$ , $R_{GEN} = 25 \Omega$	2N7000			10	ns
		$V_{DD} = 30 \text{ V}$ , $R_L = 150 \Omega$ , $I_D = 200 \text{ mA}$ , $V_{GS} = 10 \text{ V}$ , $R_{GEN} = 25 \Omega$	2N7002			20	ns
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>							
$I_s$	Maximum Continuous Drain-Source Diode Forward Current	$V_{GS} = 0 \text{ V}$ , $I_s = 115 \text{ mA}$ (Note 1)	2N7002			115	mA
			NDS7002A			280	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	$V_{GS} = 0 \text{ V}$ , $I_s = 400 \text{ mA}$ (Note 1)	2N7002			0.8	A
			NDS7002A			1.5	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$ , $I_s = 115 \text{ mA}$ (Note 1)	2N7002		0.88	1.5	V
		$V_{GS} = 0 \text{ V}$ , $I_s = 400 \text{ mA}$ (Note 1)	NDS7002A		0.88	1.2	

Note:

1. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

2N7000 / 2N7002 / NDS7002A

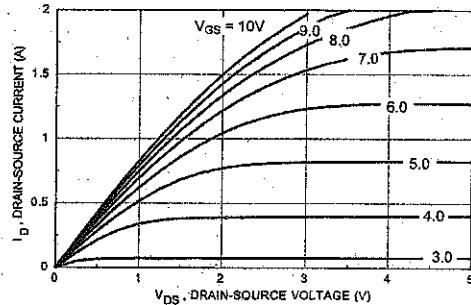


Figure 1. On-Region Characteristics

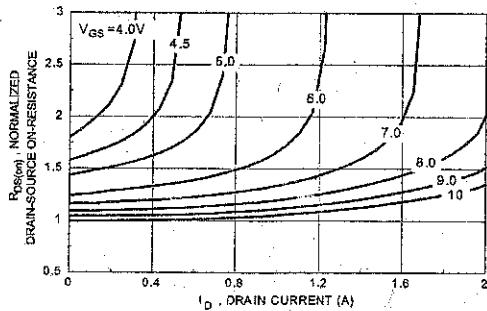


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

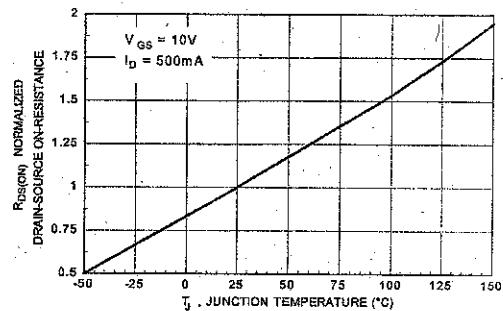


Figure 3. On-Resistance Variation with Temperature

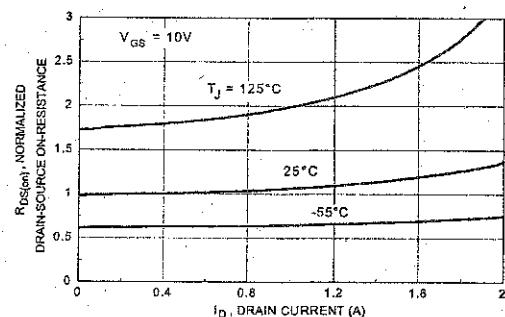


Figure 4. On-Resistance Variation with Drain Current and Temperature

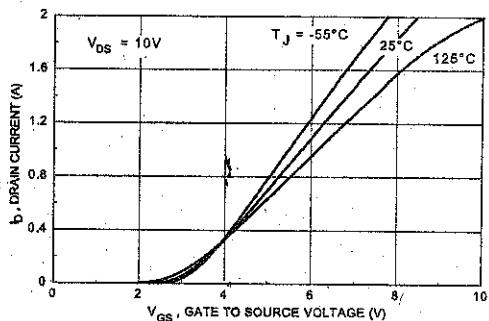


Figure 5. Transfer Characteristics

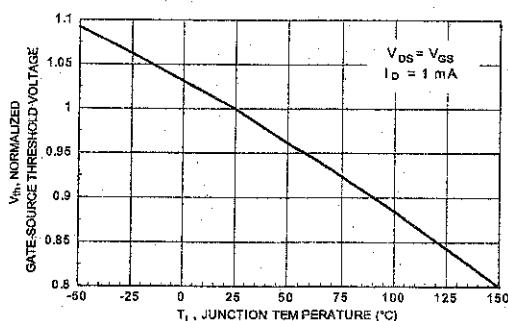


Figure 6. Gate Threshold Variation with Temperature

### Typical Electrical Characteristics (continued)

2N7000 / 2N7002 / NDS7002A

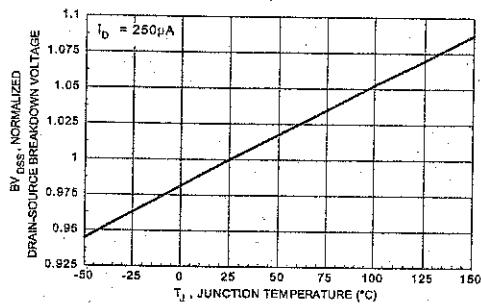


Figure 7. Breakdown Voltage Variation with Temperature

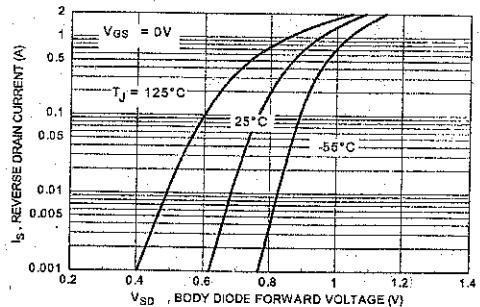


Figure 8. Body Diode Forward Voltage Variation with Temperature

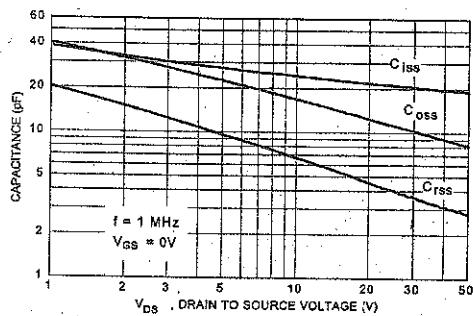


Figure 9. Capacitance Characteristics

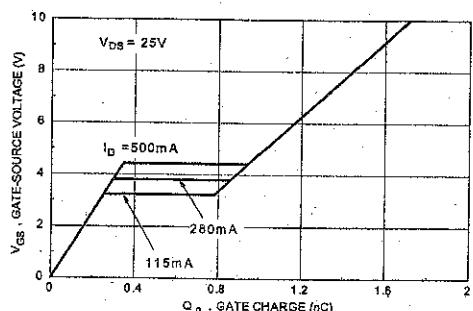


Figure 10. Gate Charge Characteristics

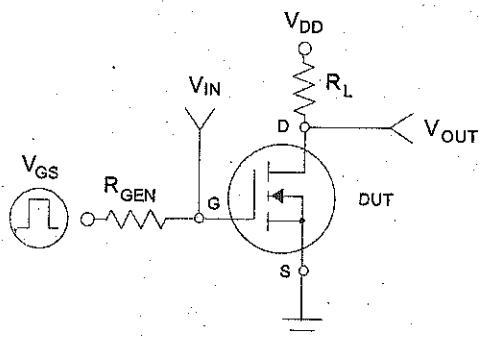


Figure 11.

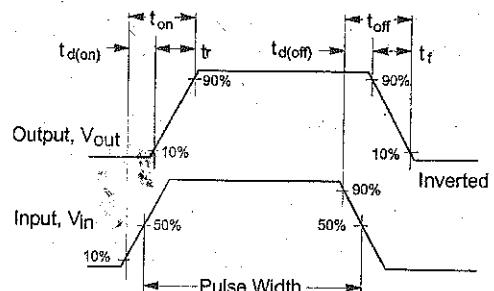


Figure 12. Switching Waveforms

# 2N6504 Series

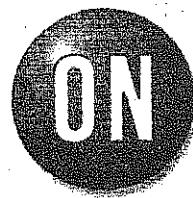
Preferred Device

## Silicon Controlled Rectifiers Reverse Blocking Thyristors

Designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supply crowbar circuits.

### Features

- Glass Passivated Junctions with Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Constructed for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts
- 300 A Surge Current Capability
- Pb-Free Packages are Available\*



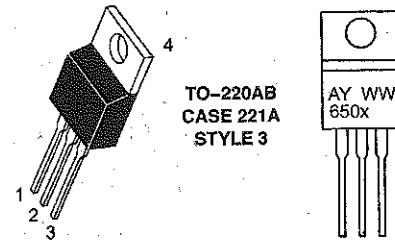
ON Semiconductor®

<http://onsemi.com>

SCRs  
25 AMPERES RMS  
50 thru 800 VOLTS



MARKING  
DIAGRAM



x = 4, 5, 7, 8 or 9  
A = Assembly Location  
Y = Year  
WW = Work Week

PIN ASSIGNMENT	
1	Cathode
2	Anode
3	Gate
4	Anode

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## 2N6504 Series

**MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)**

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (Note 1) (Gate Open, Sine Wave 50 to 60 Hz, T <sub>J</sub> = 25 to 125°C)	V <sub>DRM</sub> , V <sub>RRM</sub>		V
2N6504		50	
2N6505		100	
2N6507		400	
2N6508		600	
2N6509		800	
On-State Current RMS (180° Conduction Angles; T <sub>C</sub> = 85°C)	I <sub>T(RMS)</sub>	25	A
Average On-State Current (180° Conduction Angles; T <sub>C</sub> = 85°C)	I <sub>T(AV)</sub>	16	A
Peak Non-repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, T <sub>J</sub> = 100°C)	I <sub>TSM</sub>	250	A
Forward Peak Gate Power (Pulse Width ≤ 1.0 μs, T <sub>C</sub> = 85°C)	P <sub>GM</sub>	20	W
Forward Average Gate Power (t = 8.3 ms, T <sub>C</sub> = 85°C)	P <sub>G(AV)</sub>	0.5	W
Forward Peak Gate Current (Pulse Width ≤ 1.0 μs, T <sub>C</sub> = 85°C)	I <sub>GM</sub>	2.0	A
Operating Junction Temperature Range	T <sub>J</sub>	-40 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-40 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. V<sub>DRM</sub> and V<sub>RRM</sub> for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	1.5	°C/W
*Maximum Lead Temperature for Soldering Purposes 1/8 in from Case for 10 Seconds	T <sub>L</sub>	260	°C

**ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted.)**

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

*Peak Repetitive Forward or Reverse Blocking Current (V <sub>AK</sub> = Rated V <sub>DRM</sub> or V <sub>RRM</sub> ; Gate Open)	I <sub>DRM</sub> , I <sub>RRM</sub>	-	-	10	μA
T <sub>J</sub> = 25°C T <sub>J</sub> = 125°C		-	-	2.0	mA

### ON CHARACTERISTICS

*Forward On-State Voltage (Note 2) (I <sub>TM</sub> = 50 A)	V <sub>TM</sub>	-	-	1.8	V
*Gate Trigger Current (Continuous dc) (V <sub>AK</sub> = 12 Vdc, R <sub>L</sub> = 100 Ω)	I <sub>GT</sub>	-	9.0	30	mA
T <sub>C</sub> = 25°C T <sub>C</sub> = -40°C		-	-	75	
*Gate Trigger Voltage (Continuous dc) (V <sub>AK</sub> = 12 Vdc, R <sub>L</sub> = 100 Ω, T <sub>C</sub> = -40°C)	V <sub>GT</sub>	-	1.0	1.5	V
Gate Non-Trigger Voltage (V <sub>AK</sub> = 12 Vdc, R <sub>L</sub> = 100 Ω, T <sub>J</sub> = 125°C)	V <sub>GD</sub>	0.2	-	-	V
*Holding Current (V <sub>AK</sub> = 12 Vdc, Initiating Current = 200 mA, Gate Open) T <sub>C</sub> = -40°C	I <sub>H</sub>	-	18	40	mA
		-	-	80	
*Turn-On Time (I <sub>TM</sub> = 25 A, I <sub>GT</sub> = 50 mAdc)	t <sub>gt</sub>	-	1.5	2.0	μs
Turn-Off Time (V <sub>DRM</sub> = rated voltage) (I <sub>TM</sub> = 25 A, I <sub>R</sub> = 25 A) (I <sub>TM</sub> = 25 A, I <sub>R</sub> = 25 A, T <sub>J</sub> = 125°C)	t <sub>q</sub>	-	15	-	μs
		-	35	-	

### DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage (Gate Open, Rated V <sub>DRM</sub> , Exponential Waveform)	dv/dt	-	50	-	V/μs
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\*Indicates JEDEC Registered Data.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

## 2N6504 Series

### Voltage Current Characteristic of SCR

Symbol	Parameter
$V_{DRM}$	Peak Repetitive Off State Forward Voltage
$I_{DRM}$	Peak Forward Blocking Current
$V_{RRM}$	Peak Repetitive Off State Reverse Voltage
$I_{RRM}$	Peak Reverse Blocking Current
$V_{TM}$	Peak On State Voltage
$I_H$	Holding Current

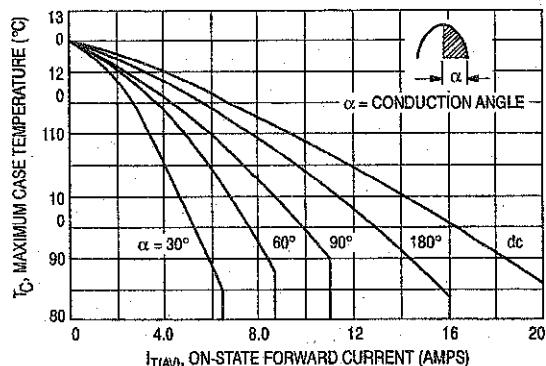
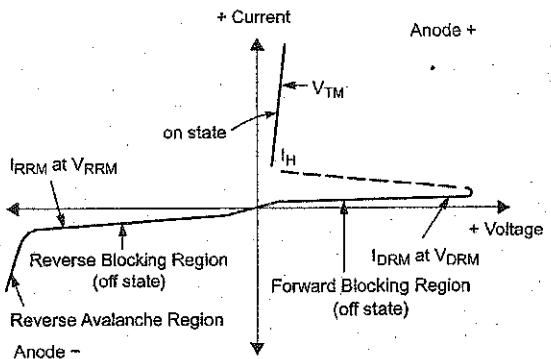


Figure 1. Average Current Derating

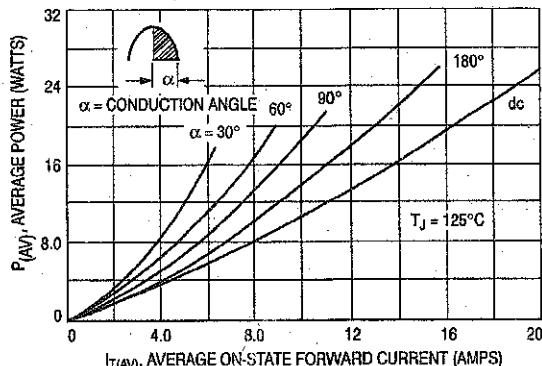


Figure 2. Maximum On-State Power Dissipation

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
2N6404	TO-220AB	
2N6405	TO-220AB	
2N6405T	TO-220AB	
2N6407	TO-220AB	
2N6407T	TO-220AB	
2N6407TG	TO-220AB (Pb-Free)	
2N6408	TO-220AB	
2N6408G	TO-220AB (Pb-Free)	
2N6409	TO-220AB	
2N6409G	TO-220AB (Pb-Free)	
2N6409T	TO-220AB	500 Units / Box

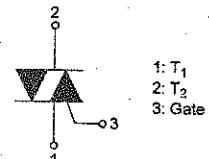
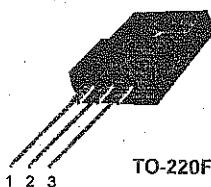
<sup>†</sup>For information on tape and reel specification, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**FAIRCHILD**  
SEMICONDUCTOR®

## FKPF8N80

### Application Explanation

- Switching mode power supply, light dimmer, electric flasher unit, hair drier
- TV sets, stereo, refrigerator, washing machine
- Electric blanket, solenoid driver, small motor control
- Photo copier, electric tool



### Bi-Directional Triode Thyristor Planar Silicon

Absolute Maximum Ratings  $T_C=25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Rating	Units
$V_{DRM}$	Repetitive Peak Off-State Voltage (Note 1)	800	V

Symbol	Parameter	Conditions	Rating	Units
$I_T$ (RMS)	RMS On-State Current	Commercial frequency, sine full wave 360° conduction, $T_C=91^\circ\text{C}$	8	A
$I_{TSM}$	Surge On-State Current	Sinewave 1 full cycle, peak value, non-repetitive	80	A
$I^2t$	$I^2t$ for Fusing	Value corresponding to 1 cycle of halfwave, surge on-state current, $t_p=10\text{ms}$	32	$\text{A}^2\text{s}$
$dI/dt$	Critical Rate of Rise of On-State Current	$I_G = 2x I_{GT}, t_r \leq 100\text{ns}$	50	$\text{A}/\mu\text{s}$
$P_{GM}$	Peak Gate Power Dissipation		5	W
$P_G$ (AV)	Average Gate Power Dissipation		0.5	W
$V_{GM}$	Peak Gate Voltage		10	V
$I_{GM}$	Peak Gate Current		2	A
$T_J$	Junction Temperature		-40 ~ 125	$^\circ\text{C}$
$T_{STG}$	Storage Temperature		-40 ~ 125	$^\circ\text{C}$
$V_{iso}$	Isolation Voltage	$T_a=25^\circ\text{C}, \text{AC } 1 \text{ minute}, T_1, T_2, G \text{ terminal to case}$	1500	V

### Thermal Characteristic

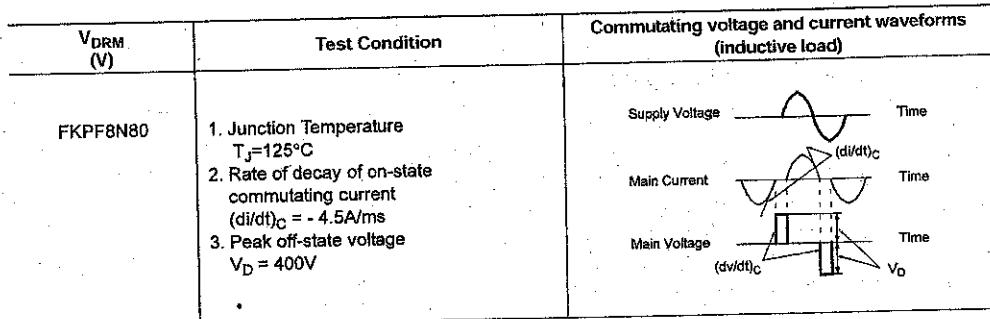
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$R_{th}(J-C)$	Thermal Resistance	Junction to case (Note 4)	-	-	3.6	$^\circ\text{C}/\text{W}$

**Electrical Characteristics**  $T_C=25^\circ\text{C}$  unless otherwise noted

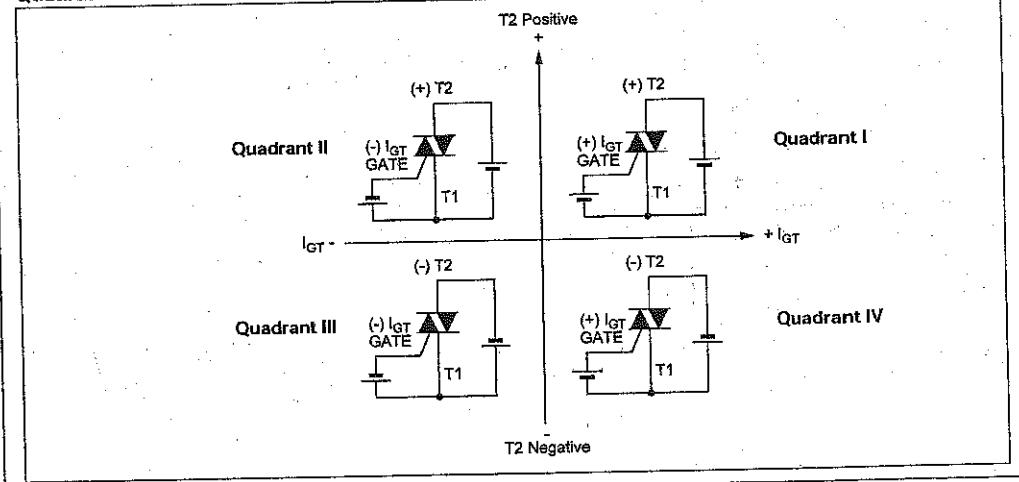
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$I_{DRM}$	Repetitive Peak Off-State Current	$V_{DRM}$ applied	-	-	20	$\mu\text{A}$
$V_{TM}$	On-State Voltage	$T_J=25^\circ\text{C}, I_{TM}=12\text{A}$ Instantaneous measurement	-	-	1.5	V
$V_{GT}$	Gate Trigger Voltage (Note 2)	I	T2(+), Gate (+)	-	-	1.5 V
		II	$V_D=12\text{V}, R_L=20\Omega$ T2(+), Gate (-)	-	-	1.5 V
		III	T2(-), Gate (-)	-	-	1.5 V
$I_{GT}$	Gate Trigger Current (Note 2)	I	T2(+), Gate (+)	-	-	30 mA
		II	$V_D=12\text{V}, R_L=20\Omega$ T2(+), Gate (-)	-	-	30 mA
		III	T2(-), Gate (-)	-	-	30 mA
$V_{GD}$	Gate Non-Trigger Voltage	$T_J=125^\circ\text{C}, V_D=1/2V_{DRM}$	0.2	-	-	V
$I_H$	Holding Current	$V_D=12\text{V}, I_{TM}=1\text{A}$	-	-	50	mA
$I_L$	Latching Current	I, III	$V_D=12\text{V}, I_G = 1.2I_{GT}$	-	-	50 mA
		II	-	-	70	mA
$dv/dt$	Critical Rate of Rise of Off-State Voltage	$V_{DRM}$ = Rated, $T_J = 125^\circ\text{C}$ , Exponential Rise	-	300	-	$\text{V}/\mu\text{s}$
$(dv/dt)_C$	Critical-Rate of Rise of Off-State Commutating Voltage (Note 3)	-	10	-	-	$\text{V}/\mu\text{s}$

## Notes:

1. Gate Open
2. Measurement using the gate trigger characteristics measurement circuit
3. The critical-rate of rise of the off-state commutating voltage is shown in the table below
4. The contact thermal resistance  $R_{TH(\text{C})}$  in case of greasing is  $0.5^\circ\text{C}/\text{W}$



## Quadrant Definitions for a Triac



## FGL60N100BNTD

### NPT-Trench IGBT

#### General Description

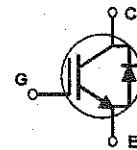
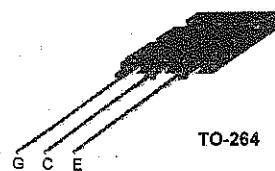
Trench insulated gate bipolar transistors (IGBTs) with NPT technology show outstanding performance in conduction and switching characteristics as well as enhanced avalanche ruggedness. These devices are well suited for Induction Heating (I-H) applications

#### Features

- High Speed Switching
- Low Saturation Voltage :  $V_{CE(sat)} = 2.5 \text{ V} @ I_C = 60\text{A}$
- High Input Impedance
- Built-in Fast Recovery Diode

#### Application

Micro-Wave Oven, I-H Cooker, I-H Jar, Induction Heater, Home Appliance



#### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Description	FGL60N100BNTD	Units
$V_{CES}$	Collector-Emitter Voltage	1000	V
$V_{GES}$	Gate-Emitter Voltage	$\pm 25$	V
$I_C$	Collector Current <small>@ <math>T_C = 25^\circ\text{C}</math></small>	60	A
	Collector Current <small>@ <math>T_C = 100^\circ\text{C}</math></small>	42	A
$I_{CM(1)}$	Pulsed Collector Current	120	A
$I_F$	Diode Continuous Forward Current <small>@ <math>T_C = 100^\circ\text{C}</math></small>	15	A
$P_D$	Maximum Power Dissipation <small>@ <math>T_C = 25^\circ\text{C}</math></small>	180	W
	Maximum Power Dissipation <small>@ <math>T_C = 100^\circ\text{C}</math></small>	72	W
$T_J$	Operating Junction Temperature	-55 to +150	$^\circ\text{C}$
$T_{stg}$	Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temp. for soldering Purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Notes :

(1) Repetitive rating : Pulse width limited by max. junction temperature

#### Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}(\text{IGBT})$	Thermal Resistance, Junction-to-Case	--	0.69	$^\circ\text{C}/\text{W}$
$R_{\theta JC}(\text{DIODE})$	Thermal Resistance, Junction-to-Case	--	2.08	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	25	$^\circ\text{C}/\text{W}$

**Electrical Characteristics of IGBT** $T_C = 25^\circ C$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
<b>Off Characteristics</b>						
$BV_{CES}$	Collector Emitter Breakdown Voltage	$V_{GE} = 0V, I_C = 1mA$	1000	—	—	V
$I_{CES}$	Collector Cut-Off Current	$V_{CE} = 1000V, V_{GE} = 0V$	—	—	1.0	mA
$I_{GES}$	G-E Leakage Current	$V_{GE} = \pm 25, V_{CE} = 0V$	—	—	$\pm 500$	nA
<b>On Characteristics</b>						
$V_{GE(th)}$	G-E Threshold Voltage	$I_C = 60mA, V_{CE} = V_{GE}$	4.0	5.0	7.0	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage	$I_C = 10A, V_{GE} = 15V$	—	1.5	1.8	V
		$I_C = 60A, V_{GE} = 15V$	—	2.5	2.9	V
<b>Dynamic Characteristics</b>						
$C_{ies}$	Input Capacitance	$V_{CE}=10V, V_{GE} = 0V,$ $f = 1MHz$	—	6000	—	pF
$C_{oes}$	Output Capacitance		—	260	—	pF
$C_{res}$	Reverse Transfer Capacitance		—	200	—	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{CC} = 600V, I_C = 60A,$ $R_G = 51\Omega, V_{GE}=15V,$ Resistive Load, $T_C = 25^\circ C$	—	140	—	ns
$t_r$	Rise Time		—	320	—	ns
$t_{d(off)}$	Turn-Off Delay Time		—	630	—	ns
$t_f$	Fall Time		—	130	250	ns
$Q_g$	Total Gate Charge	$V_{CE} = 600V, I_C = 60A,$ $V_{GE} = 15V, T_C = 25^\circ C$	—	275	350	nC
$Q_{ge}$	Gate-Emitter Charge		—	45	—	nC
$Q_{gc}$	Gate-Collector Charge		—	95	—	nC

**Electrical Characteristics of DIODE**  $T_C = 25^\circ C$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{FM}$	Diode Forward Voltage	$I_F = 15A$	—	1.2	1.7	V
		$I_F = 60A$	—	1.8	2.1	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 60A, dI/dt = 20A/\mu s$	—	1.2	1.5	us
$I_R$	Instantaneous Reverse Current	$VRM = 1000V$	—	0.05	2	$\mu A$

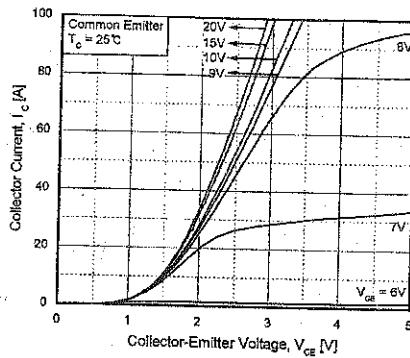


Fig 1. Typical Output Characteristics

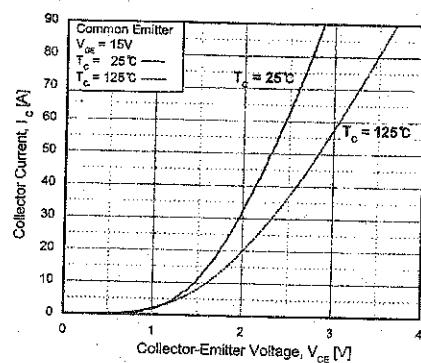


Fig 2. Typical Saturation Voltage Characteristics

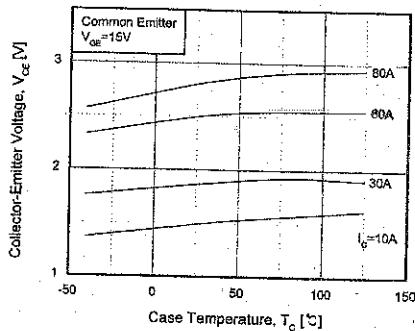
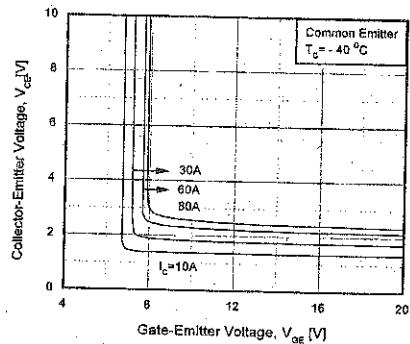
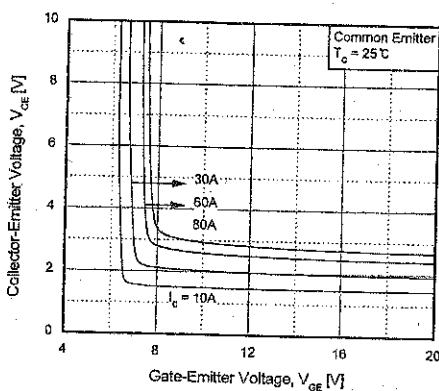
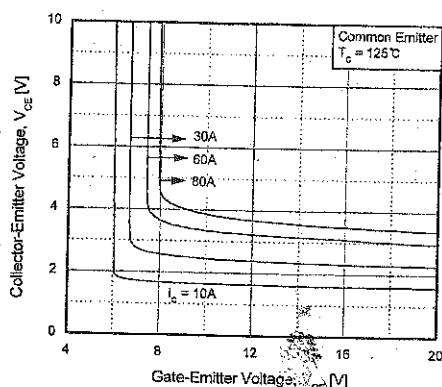
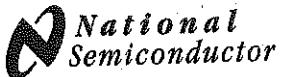


Fig 3. Saturation Voltage vs. Case Temperature at Varient Current Level

Fig 4. Saturation Voltage vs.  $V_{GE}$ Fig 5. Saturation Voltage vs.  $V_{GE}$ Fig 6. Saturation Voltage vs.  $V_{GE}$



August 2000

## LM741 Operational Amplifier

### General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and

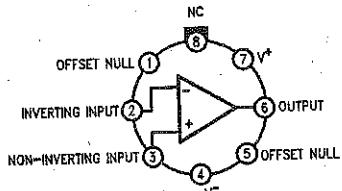
output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0°C to +70°C temperature range, instead of -55°C to +125°C.

### Features

### Connection Diagrams

Metal Can Package

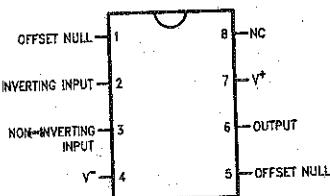


00934102

Note 1: LM741H is available per JM38510/10101

Order Number LM741H, LM741H/883 (Note 1),  
LM741AH/883 or LM741CH  
See NS Package Number H08C

Dual-In-Line or S.O. Package



00934103

Order Number LM741J, LM741J/883, LM741CN  
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak

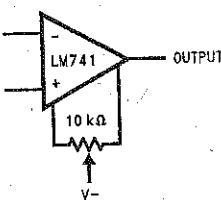


00934108

Order Number LM741W/883  
See NS Package Number W10A

### Typical Application

Offset Nulling Circuit



00934107

**Absolute Maximum Ratings** (Note 2)

If Military/Aerospace specified devices are required,  
please contact the National Semiconductor Sales Office/  
Distributors for availability and specifications.

(Note 7)

	LM741A	LM741	LM741C
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V
Input Voltage (Note 4)	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Operating Temperature Range	-55°C to +125°C	-55°C to +125°C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Junction Temperature	150°C	150°C	100°C
Soldering Information			
N-Package (10 seconds)	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C
M-Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.			
ESD Tolerance (Note 8)	400V	400V	400V

**Electrical Characteristics** (Note 5)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25^\circ\text{C}$						1.0	5.0			mV mV
	$R_S \leq 10 \text{ k}\Omega$		0.8	3.0					2.0	6.0	
Average Input Offset Voltage Drift	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$										mV mV/°C
	$R_S \leq 50\Omega$				4.0			6.0			
Input Offset Voltage Adjustment Range	$R_S \leq 10 \text{ k}\Omega$									7.5	mV
Input Offset Current	$T_A = 25^\circ\text{C}, V_S = \pm 20\text{V}$	±10				±15			±15		nA
	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$										
Average Input Offset Current Drift	$T_A = 25^\circ\text{C}$		3.0	30		20	200		20	200	nA/°C
	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$				70		85	500		300	
Input Bias Current	$T_A = 25^\circ\text{C}$				0.5						nA
	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$										
Input Resistance	$T_A = 25^\circ\text{C}, V_S = \pm 20\text{V}$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}, V_S = \pm 20\text{V}$	0.5									
Input Voltage Range	$T_A = 25^\circ\text{C}$							±12	±13		V
	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$				±12	±13					

## Electrical Characteristics (Note 5) (Continued)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$T_A = 25^\circ\text{C}$ , $R_L \geq 2 \text{ k}\Omega$ $V_S = \pm 20\text{V}$ , $V_O = \pm 15\text{V}$ $V_S = \pm 15\text{V}$ , $V_O = \pm 10\text{V}$	50			50	200		20	200		V/mV V/mV
	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$ , $R_L \geq 2 \text{ k}\Omega$ , $V_S = \pm 20\text{V}$ , $V_O = \pm 15\text{V}$ $V_S = \pm 15\text{V}$ , $V_O = \pm 10\text{V}$ $V_S = \pm 5\text{V}$ , $V_O = \pm 2\text{V}$	32			25			15			V/mV V/mV V/mV
		10									
Output Voltage Swing	$V_S = \pm 20\text{V}$ $R_L \geq 10 \text{ k}\Omega$ $R_L \geq 2 \text{ k}\Omega$	$\pm 16$									V V
	$V_S = \pm 15\text{V}$ $R_L \geq 10 \text{ k}\Omega$ $R_L \geq 2 \text{ k}\Omega$				$\pm 12$	$\pm 14$		$\pm 12$	$\pm 14$		V V
					$\pm 10$	$\pm 13$		$\pm 10$	$\pm 13$		
Output Short Circuit Current	$T_A = 25^\circ\text{C}$ $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	10	25	35		25			25		mA mA
		10		40							
Common-Mode Rejection Ratio	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$ $R_S \leq 1^{\text{st}} \text{ k}\Omega$ , $V_{CM} = \pm 12\text{V}$ $R_S \leq 50\Omega$ , $V_{CM} = \pm 12\text{V}$				70	90		70	90		dB dB
Supply Voltage Rejection Ratio	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$ , $V_S = \pm 20\text{V}$ to $V_S = \pm 5\text{V}$ $R_S \leq 50\Omega$ $R_S \leq 10 \text{ k}\Omega$	86	96		77	96		77	96		dB dB
Transient Response	$T_A = 25^\circ\text{C}$ , Unity Gain										
Rise Time		0.25	0.8		0.3			0.3			μs
Overshoot		6.0	20		5			5			%
Bandwidth (Note 6)	$T_A = 25^\circ\text{C}$	0.437	1.5								MHz
Slew Rate	$T_A = 25^\circ\text{C}$ , Unity Gain	0.3	0.7		0.5			0.5			V/μs
Supply Current	$T_A = 25^\circ\text{C}$				1.7	2.8		1.7	2.8		mA
Power Consumption	$T_A = 25^\circ\text{C}$ $V_S = \pm 20\text{V}$ $V_S = \pm 15\text{V}$		80	150				50	85		mW mW
LM741A	$V_S = \pm 20\text{V}$ $T_A = T_{A\text{MIN}}$ $T_A = T_{A\text{MAX}}$			165							mW
				135							mW
LM741	$V_S = \pm 15\text{V}$ $T_A = T_{A\text{MIN}}$ $T_A = T_{A\text{MAX}}$				60	100		45	75		mW mW

Note 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

## Electrical Characteristics (Note 5) (Continued)

Note 3: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and  $T_j$  max. (listed under "Absolute Maximum Ratings").  $T_j = T_A + (\theta_{JA} P_D)$ .

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
$\theta_{JA}$ (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
$\theta_{JC}$ (Junction to Case)	N/A	N/A	25°C/W	N/A

Note 4: For supply voltages less than  $\pm 15V$ , the absolute maximum input voltage is equal to the supply voltage.

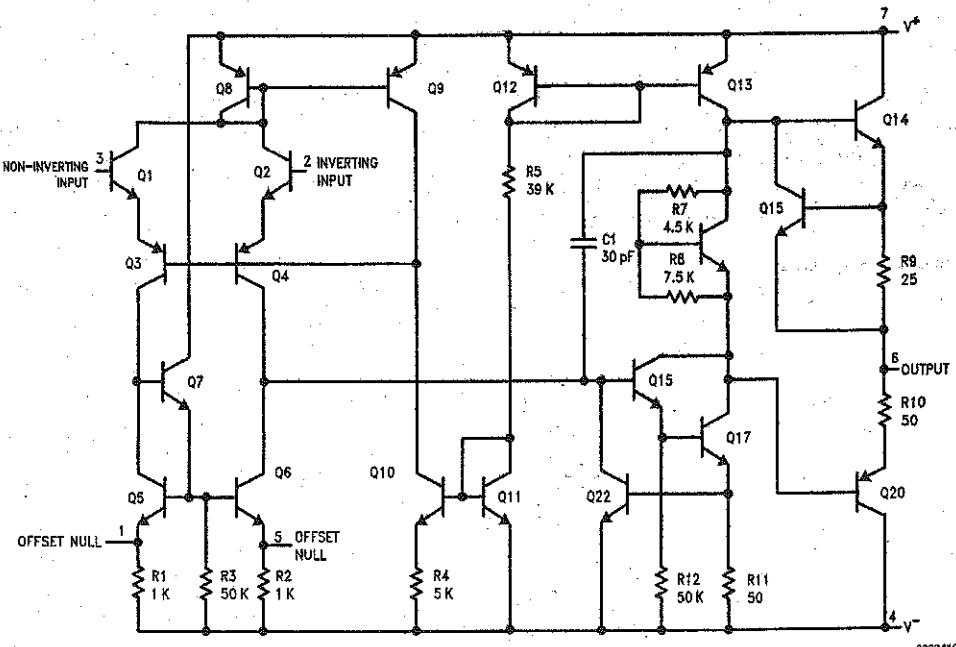
Note 5: Unless otherwise specified, these specifications apply for  $V_S = \pm 15V$ ,  $-55^\circ C \leq T_A \leq +125^\circ C$  (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to  $0^\circ C \leq T_A \leq +70^\circ C$ .

Note 6: Calculated value from:  $BW$  (MHz) =  $0.35/Rise\ Time(\mu s)$ .

Note 7: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

## Schematic Diagram



## LM118/LM218/LM318 Operational Amplifiers

### General Description

The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/ $\mu$ s and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1  $\mu$ s.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters,

sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

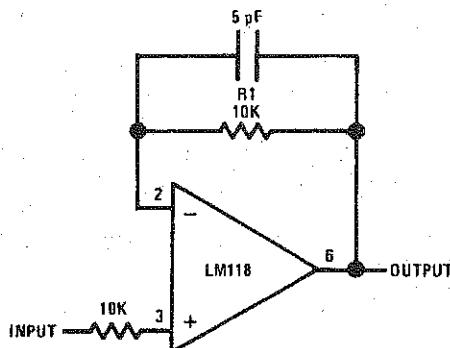
The LM218 is identical to the LM118 except that the LM218 has its performance specified over a -25°C to +85°C temperature range. The LM318 is specified from 0°C to +70°C.

### Features

- 15 MHz small signal bandwidth
- Guaranteed 50V/ $\mu$ s slew rate
- Maximum bias current of 250 nA
- Operates from supplies of  $\pm$ 5V to  $\pm$ 20V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

### Fast Voltage Follower

(Note 1)



00776613

Note 1: Do not hard-wire as voltage follower ( $R_1 \geq 5 \text{ k}\Omega$ )

**Absolute Maximum Ratings** (Note 7)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	$\pm 20V$
Power Dissipation (Note 2)	500 mW
Differential Input Current (Note 3)	$\pm 10 \text{ mA}$
Input Voltage (Note 4)	$\pm 15V$
Output Short-Circuit Duration	Continuous
Operating Temperature Range LM118	-55°C to +125°C
LM218	-25°C to +85°C
LM318	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

## Lead Temperature (Soldering, 10 sec.)

Hermetic Package	300°C
Plastic Package	260°C
Soldering Information	
Dual-In-Line Package	260°C
Soldering (10 sec.)	
Small Outline Package	215°C
Vapor Phase (60 sec.)	220°C
Infrared (15 sec.)	

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 8) 2000V

**Electrical Characteristics** (Note 5)

Parameter	Conditions	LM118/LM218			LM318			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25^\circ\text{C}$		2	4		4	10	mV
Input Offset Current	$T_A = 25^\circ\text{C}$		6	50		30	200	nA
Input Bias Current	$T_A = 25^\circ\text{C}$		120	250		150	500	nA
Input Resistance	$T_A = 25^\circ\text{C}$	1	3		0.5	3		MΩ
Supply Current	$T_A = 25^\circ\text{C}$		5	8		5	10	mA
Large Signal Voltage Gain	$T_A = 25^\circ\text{C}, V_S = \pm 15V, V_{OUT} = \pm 10V, R_L \geq 2 \text{ k}\Omega$	50	200		25	200		V/mV
Slew Rate	$T_A = 25^\circ\text{C}, V_S = \pm 15V, A_V = 1$ (Note 6)	50	70		50	70		V/μs
Small Signal Bandwidth	$T_A = 25^\circ\text{C}, V_S = \pm 15V$		15			15		MHz
Input Offset Voltage				6			15	mV
Input Offset Current				100			300	nA
Input Bias Current				500			750	nA
Supply Current	$T_A = 125^\circ\text{C}$		4.5	7				mA
Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V$ $R_L \geq 2 \text{ k}\Omega$	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V, R_L = 2 \text{ k}\Omega$	$\pm 12$	$\pm 13$		$\pm 12$	$\pm 13$		V
Input Voltage Range	$V_S = \pm 15V$	$\pm 11.5$			$\pm 11.5$			V
Common-Mode Rejection Ratio		80	100		70	100		dB
Supply Voltage Rejection Ratio		70	80		65	80		dB

Note 2: The maximum junction temperature of the LM118 is 150°C, the LM218 is 110°C, and the LM318 is 110°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 4: For supply voltages less than  $\pm 15V$ , the absolute maximum input voltage is equal to the supply voltage.

Note 5: These specifications apply for  $\pm 5V \leq V_S \leq \pm 20V$  and  $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$  (LM118),  $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$  (LM218), and  $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$  (LM318). Also, power supplies must be bypassed with 0.1 μF disc capacitors.

Note 6: Slew rate is tested with  $V_S = \pm 15V$ . The LM118 is in a unity-gain non-inverting configuration.  $V_{IN}$  is stepped from -7.5V to +7.5V and vice versa. The slew rates between -5.0V and +5.0V and vice versa are tested and guaranteed to exceed 50V/μs.

Note 7: Refer to RETS118X for LM118H and LM118J military specifications.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

## LM555 Timer

### General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

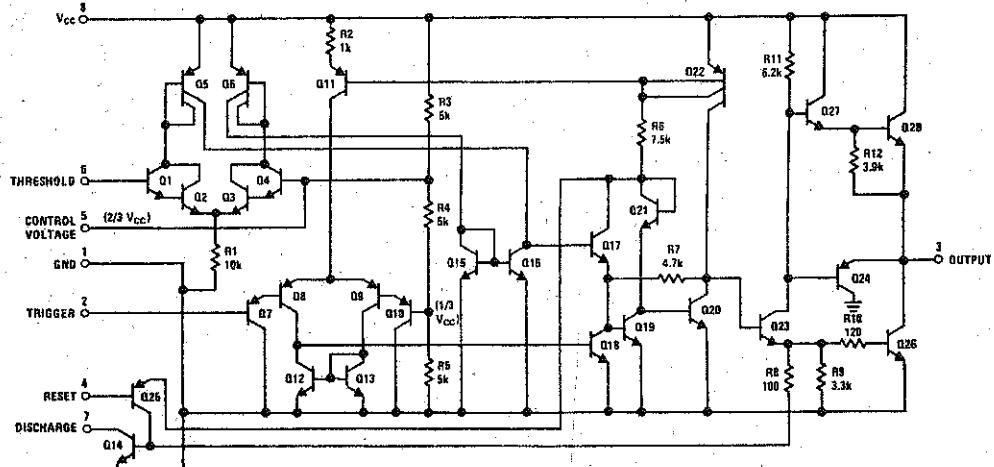
### Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

### Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

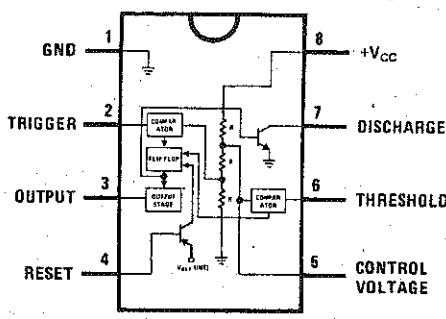
### Schematic Diagram



DS007851-1

## Connection Diagram

Dual-In-Line, Small Outline  
and Molded Mini Small Outline Packages



Top View

## Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

**Absolute Maximum Ratings** (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

**Soldering Information**

Dual-In-Line Package	260°C
Soldering (10 Seconds)	
Small Outline Packages (SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

**Electrical Characteristics** (Notes 1, 2)

( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = +5\text{V}$  to  $+15\text{V}$ , unless otherwise specified)

Parameter	Conditions	Limits			Units	
		LM555C				
		Min	Typ	Max		
Supply Voltage		4.5		16	V	
Supply Current	$V_{CC} = 5\text{V}$ , $R_L = \infty$ $V_{CC} = 15\text{V}$ , $R_L = \infty$ (Low State) (Note 4)		3 10	6 15	mA	
Timing Error, Monostable						
Initial Accuracy			1		%	
Drift with Temperature	$R_A = 1\text{k}$ to $100\text{k}\Omega$ , $C = 0.1\mu\text{F}$ , (Note 5)		50		ppm/ $^\circ\text{C}$	
Accuracy over Temperature			1.5		%	
Drift with Supply			0.1		%/V	
Timing Error, Astable						
Initial Accuracy			2.25		%	
Drift with Temperature	$R_A, R_B = 1\text{k}$ to $100\text{k}\Omega$ , $C = 0.1\mu\text{F}$ , (Note 5)		150		ppm/ $^\circ\text{C}$	
Accuracy over Temperature			3.0		%	
Drift with Supply			0.30		%/V	
Threshold Voltage			0.667		$\times V_{CC}$	
Trigger Voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$		5 1.67		V	
Trigger Current			0.5	0.9	$\mu\text{A}$	
Reset Voltage		0.4	0.5	1	V	
Reset Current			0.1	0.4	mA	
Threshold Current	(Note 6)		0.1	0.25	$\mu\text{A}$	
Control Voltage Level	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	9 2.6	10 3.33	11 4	V	
Pin 7 Leakage Output High			1	100	nA	
Pin 7 Sat (Note 7)	$V_{CC} = 15\text{V}$ , $I_7 = 15\text{mA}$ $V_{CC} = 4.5\text{V}$ , $I_7 = 4.5\text{mA}$		180 80		mV	
Output Low					mV	

## Electrical Characteristics (Notes 1, 2) (Continued)

( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = +5\text{V}$  to  $+15\text{V}$ , unless otherwise specified)

Parameter	Conditions	Limits			Units	
		LM555C				
		Min	Typ	Max		
Output Voltage Drop (Low)	$V_{CC} = 15\text{V}$ $I_{SINK} = 10\text{mA}$ $I_{SINK} = 50\text{mA}$ $I_{SINK} = 100\text{mA}$ $I_{SINK} = 200\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SINK} = 8\text{mA}$ $I_{SINK} = 5\text{mA}$		0.1 0.4 2 2.5 0.25	0.25 0.75 2.5 0.35	V V V V V	
Output Voltage Drop (High)	$I_{SOURCE} = 200\text{mA}$ , $V_{CC} = 15\text{V}$ $I_{SOURCE} = 100\text{mA}$ , $V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	12.75 2.75	12.5 18.3 3.3		V V V	
Rise Time of Output			100		ns	
Fall Time of Output			100		ns	

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above  $25^\circ\text{C}$  based on a  $+150^\circ\text{C}$  maximum junction temperature and a thermal resistance of  $106^\circ\text{C}/\text{W}$  (DIP),  $170^\circ\text{C}/\text{W}$  (SO-8), and  $204^\circ\text{C}/\text{W}$  (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at  $V_{CC} = 5\text{V}$ .

Note 5: Tested at  $V_{CC} = 5\text{V}$  and  $V_{CC} = 15\text{V}$ .

Note 6: This will determine the maximum value of  $R_A + R_B$  for 15V operation. The maximum total ( $R_A + R_B$ ) is  $20\text{M}\Omega$ .

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM655J versions for specifications.



*...the analog plus company*™

# XR-2206

Monolithic  
Function Generator

June 1997-3

## ATURES

- Low-Sine Wave Distortion, 0.5%, Typical
- Excellent Temperature Stability, 20ppm/°C, Typ.
- Wide Sweep Range, 2000:1, Typical
- Low-Supply Sensitivity, 0.01%V, Typ.
- Linear Amplitude Modulation
- TTL Compatible FSK Controls
- Wide Supply Range, 10V to 26V
- Adjustable Duty Cycle, 1% TO 99%

## APPLICATIONS

- Waveform Generation
- Sweep Generation
- AM/FM Generation
- V/F Conversion
- FSK Generation
- Phase-Locked Loops (VCO)

## GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high stability and accuracy. The output waveforms can be high amplitude and frequency modulated by an external voltage. Frequency of operation can be selected internally over a range of 0.01Hz to more than 1MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.

## DERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2206M	16 Lead 300 Mil CDIP	-55°C to +125°C
XR-2206P	16 Lead 300 Mil PDIP	-40°C to +85°C
XR-2206CP	16 Lead 300 Mil PDIP	0°C to +70°C
XR-2206D	16 Lead 300 Mil JEDEC SOIC	0°C to +70°C

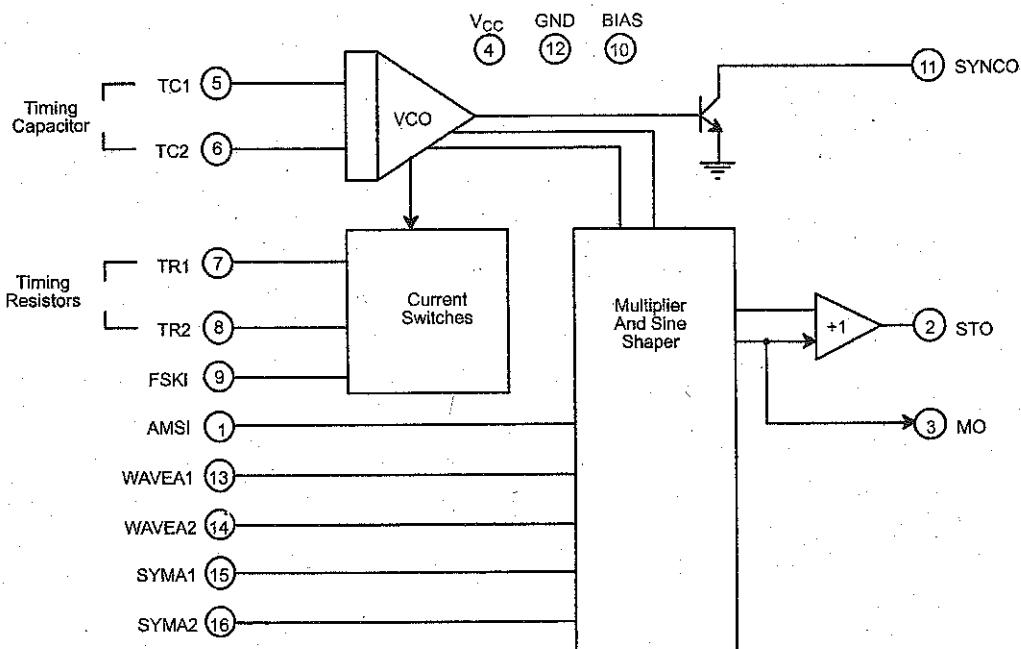
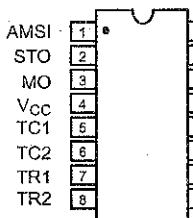
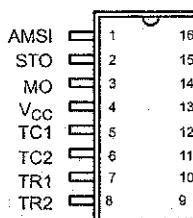


Figure 1. XR-2206 Block Diagram



16 Lead PDIP, CDIP (0.300")



16 Lead SOIC (Jedec, 0.300")

**PIN DESCRIPTION**

Pin #	Symbol	Type	Description
1	AMSI	I	Amplitude Modulating Signal Input.
2	STO	O	Sine or Triangle Wave Output.
3	MO	O	Multiplier Output.
4	V <sub>CC</sub>		Positive Power Supply.
5	TC1	I	Timing Capacitor Input.
6	TC2	I	Timing Capacitor Input.
7	TR1	O	Timing Resistor 1 Output.
8	TR2	O	Timing Resistor 2 Output.
9	FSKI	I	Frequency Shift Keying Input.
10	BIAS	O	Internal Voltage Reference.
11	SYNC0	O	Sync Output. This output is a open collector and needs a pull up resistor to V <sub>CC</sub> . Ground pin.
12	GND		
13	WAVEA1	I	Wave Form Adjust Input 1.
14	WAVEA2	I	Wave Form Adjust Input 2.
15	SYMA1	I	Wave Symetry Adjust 1.
16	SYMA2	I	Wave Symetry Adjust 2.

# XR-2206

**EXAR**

## DC ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of *Figure 2*  $V_{CC} = 12V$ ,  $T_A = 25^\circ C$ ,  $C = 0.01\mu F$ ,  $R_1 = 100k\Omega$ ,  $R_2 = 10k\Omega$ ,  $R_3 = 25k\Omega$  Unless Otherwise Specified.  $S_1$  open for triangle, closed for sine wave.

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>General Characteristics</b>								
Single Supply Voltage	10 <b>±5</b>		26 <b>±13</b>	10 <b>±5</b>		26 <b>±13</b>	V	
Split-Supply Voltage		12		17		14	V	
Supply Current						20	mA	$R_1 \geq 10k\Omega$
<b>Oscillator Section</b>								
Max. Operating Frequency	0.5	1		0.5	1		MHz	$C = 1000pF$ , $R_1 = 1k\Omega$
Lowest Practical Frequency		0.01			0.01		Hz	$C = 50\mu F$ , $R_1 = 2M\Omega$
Frequency Accuracy		<b>±1</b>	<b>±4</b>		<b>±2</b>		% of $f_o$	$f_o = 1/R_1C$
Temperature Stability		<b>±10</b>	<b>±50</b>		<b>±20</b>		ppm/°C	$0^\circ C \leq T_A \leq 70^\circ C$
Frequency								$R_1 = R_2 = 20k\Omega$
Sine Wave Amplitude Stability <sup>2</sup>		4800			4800		ppm/°C	
Supply Sensitivity		0.01	<b>0.1</b>		0.01		%/V	$V_{LOW} = 10V$ , $V_{HIGH} = 20V$ , $R_1 = R_2 = 20k\Omega$
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	$f_H @ R_1 = 1k\Omega$
							$f_L @ R_1 = 2M\Omega$	
<b>Sweep Linearity</b>								
10:1 Sweep		2			2		%	$f_L = 1kHz$ , $f_H = 10kHz$
1000:1 Sweep		8			8		%	$f_L = 100Hz$ , $f_H = 100kHz$
FM Distortion		0.1			0.1		%	±10% Deviation
<b>Recommended Timing Components</b>								
Timing Capacitor: C	<b>0.001</b>		100	0.001		100	$\mu F$	<i>Figure 5</i>
Timing Resistors: $R_1$ & $R_2$	<b>1</b>		2000	1		2000	$k\Omega$	
<b>Triangle Sine Wave Output<sup>1</sup></b>								
Triangle Amplitude		160			160		$mV/k\Omega$	<i>Figure 2</i> , $S_1$ Open
Sine Wave Amplitude	<b>40</b>	60	80		60		$mV/k\Omega$	<i>Figure 2</i> , $S_1$ Closed
Max. Output Swing		6			6		Vp-p	
Output Impedance		600			600		$\Omega$	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
<b>Sine Wave Distortion</b>								
Without Adjustment		2.5			2.5		%	$R_1 = 30k\Omega$
With Adjustment		0.4	<b>1.0</b>		0.5	1.5	%	See <i>Figure 7</i> and <i>Figure 8</i>

### Notes

<sup>1</sup> Output amplitude is directly proportional to the resistance,  $R_3$ , on Pin 3. See *Figure 3*.

<sup>2</sup> For maximum amplitude stability,  $R_3$  should be a positive temperature coefficient resistor.

**Bold face** parameters are covered by production test and guaranteed over operating temperature range.



XR-2206

## DC ELECTRICAL CHARACTERISTICS (CONT'D)

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>Amplitude Modulation</b>								
Input Impedance	50	100		50	100		kΩ	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
<b>Square-Wave Output</b>								
Amplitude		12			12		Vp-p	Measured at Pin 11.
Rise Time		250			250		ns	$C_L = 10\text{pF}$
Fall Time		50			50		ns	$C_L = 10\text{pF}$
Saturation Voltage		0.2	0.4		0.2	0.6	V	$I_L = 2\text{mA}$
Leakage Current		0.1	20		0.1	100	μA	$V_{CC} = 26\text{V}$
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See section on circuit control
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

**Notes**

<sup>1</sup> Output amplitude is directly proportional to the resistance,  $R_3$ , on Pin 3. See Figure 3.

<sup>2</sup> For maximum amplitude stability,  $R_3$  should be a positive temperature coefficient resistor.

**Bold face parameters** are covered by production test and guaranteed over operating temperature range.

Specifications are subject to change without notice

**ABSOLUTE MAXIMUM RATINGS**

Power Supply .....	26V	Total Timing Current .....	6mA
Power Dissipation .....	750mW	Storage Temperature .....	-65°C to +150°
Derate Above 25°C .....	5mW/°C		

**SYSTEM DESCRIPTION**

The XR-2206 is comprised of four functional blocks; a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches.

The VCO produces an output frequency proportional to an input current, which is set by a resistor from the timing

terminals to ground. With two timing pins, two discrete output frequencies can be independently produced FSK generation applications by using the FSK or control pin. This input controls the current switches which select one of the timing resistor currents, and routes the VCO.

# XR-2206

**EXAR**

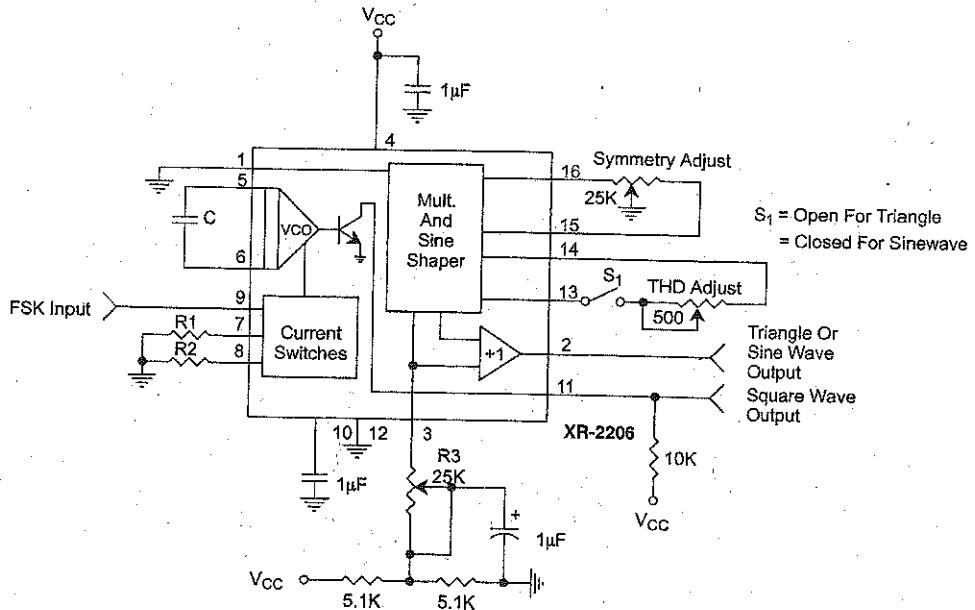


Figure 2. Basic Test Circuit

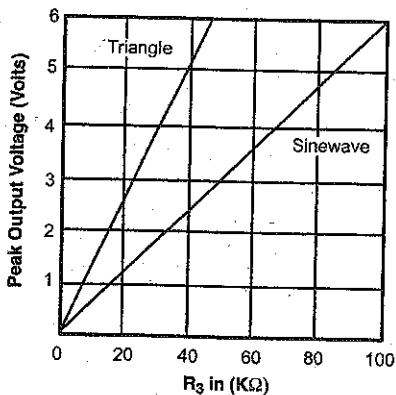


Figure 3. Output Amplitude as a Function of the Resistor, R<sub>3</sub>, at Pin 3

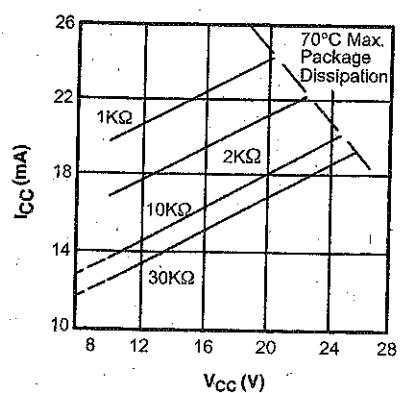
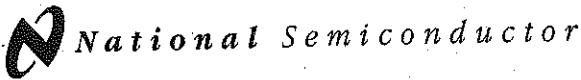


Figure 4. Supply Current vs Supply Voltage, Timing, R

May 2000



## LM78XX Series Voltage Regulators

### General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the out-

put, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

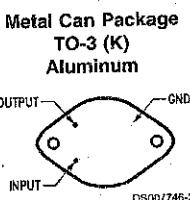
### Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

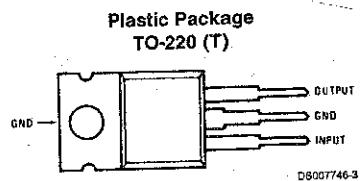
### Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

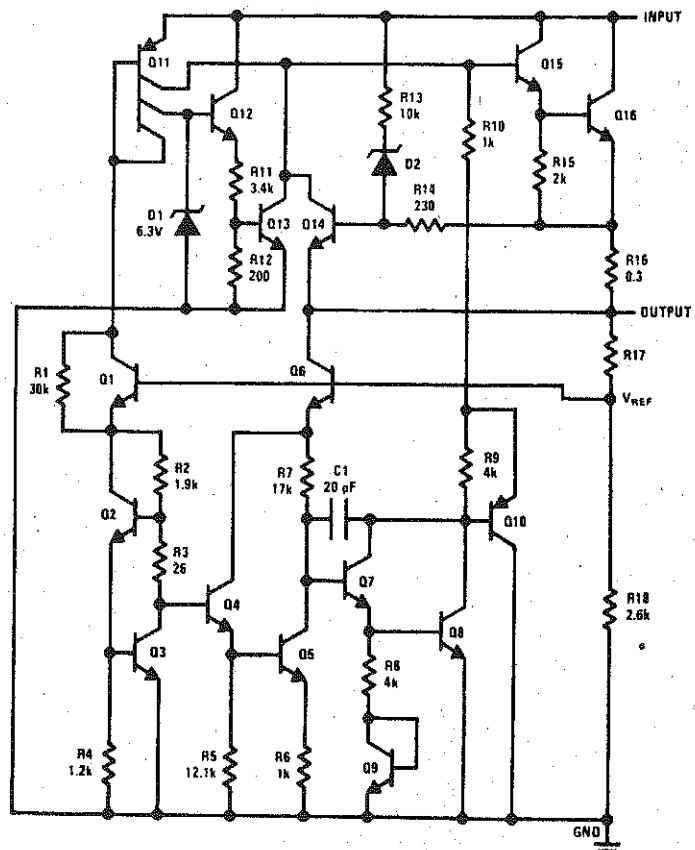
### Connection Diagrams



Bottom View  
Order Number LM7805CK,  
LM7812CK or LM7815CK  
See NS Package Number KC02A



Top View  
Order Number LM7805CT,  
LM7812CT or LM7815CT  
See NS Package Number T03B

**Schematic**

DS007748-1

**Absolute Maximum Ratings** (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage ( $V_O = 5V, 12V$ and $15V$ )	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range ( $T_A$ )	0°C to +70°C

## Maximum Junction Temperature

(K Package)	150°C
(L Package)	150°C

Storage Temperature Range -65°C to +150°C

Lead Temperature (Soldering, 10 sec.)	-65°C to +150°C
TO-3 Package K	300°C
TO-220 Package T	230°C

**Electrical Characteristics LM78XXC** (Note 2)0°C ≤  $T_J$  ≤ 125°C unless otherwise noted.

Symbol	Parameter	Output Voltage			5V			12V			15V			Units
		Input Voltage (unless otherwise noted)			10V			19V			23V			
$V_O$	Output Voltage	$T_J = 25^\circ C$ , $5 \text{ mA} \leq I_O \leq 1 \text{ A}$			4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		$P_D \leq 15W$ , $5 \text{ mA} \leq I_O \leq 1 \text{ A}$			4.75		5.25	11.4		12.6	14.25		15.75	V
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$						(14.5 ≤ $V_{IN}$ ≤ 27)			(17.5 ≤ $V_{IN}$ ≤ 30)			V
$\Delta V_O$	Line Regulation	$I_O = 500 \text{ mA}$	$T_J = 25^\circ C$		3	50		4	120		4	150		mV
			$\Delta V_{IN}$				(7 ≤ $V_{IN}$ ≤ 25)		(14.5 ≤ $V_{IN}$ ≤ 30)		(17.5 ≤ $V_{IN}$ ≤ 30)			V
		$I_O \leq 1 \text{ A}$	$0^\circ C \leq T_J \leq +125^\circ C$			50		120		150				mV
			$\Delta V_{IN}$			(8 ≤ $V_{IN}$ ≤ 20)		(15 ≤ $V_{IN}$ ≤ 27)		(18.5 ≤ $V_{IN}$ ≤ 30)				V
$\Delta V_O$	Load Regulation	$T_J = 25^\circ C$	$5 \text{ mA} \leq I_O \leq 1.5 \text{ A}$		10	50		12	120		12	150		mV
			$250 \text{ mA} \leq I_O \leq 750 \text{ mA}$			25		60			75			mV
		$5 \text{ mA} \leq I_O \leq 1 \text{ A}$ , $0^\circ C \leq T_J \leq +125^\circ C$				50		120		150				mV
$I_Q$	Quiescent Current	$I_O \leq 1 \text{ A}$	$T_J = 25^\circ C$		8			8			8			mA
			$0^\circ C \leq T_J \leq +125^\circ C$		8.5			8.5			8.5			mA
$\Delta I_Q$	Quiescent Current Change	$5 \text{ mA} \leq I_O \leq 1 \text{ A}$			0.5			0.5			0.5			mA
			$T_J = 25^\circ C$ , $I_O \leq 1 \text{ A}$			1.0		1.0			1.0			mA
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$				(7.5 ≤ $V_{IN}$ ≤ 20)		(14.8 ≤ $V_{IN}$ ≤ 27)		(17.9 ≤ $V_{IN}$ ≤ 30)				V
$V_N$	Output Noise Voltage	$T_A = 25^\circ C$ , $10 \text{ Hz} \leq f \leq 100 \text{ kHz}$			40			75			90			µV
			$I_O \leq 1 \text{ A}$ , $T_J = 25^\circ C$		62	80		55	72		54	70		dB
		$f = 120 \text{ Hz}$	$I_O \leq 500 \text{ mA}$		62			55			54			dB
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	$0^\circ C \leq T_J \leq +125^\circ C$												V
			$V_{MIN} \leq V_{IN} \leq V_{MAX}$			(8 ≤ $V_{IN}$ ≤ 18)		(15 ≤ $V_{IN}$ ≤ 25)		(18.5 ≤ $V_{IN}$ ≤ 28.5)				V
$R_O$	Dropout Voltage	$T_J = 25^\circ C$ , $I_{OUT} = 1 \text{ A}$			2.0			2.0			2.0			V
		$f = 1 \text{ kHz}$			8			18			19			mA

## Electrical Characteristics LM78XXC (Note 2) (Continued)

$0^\circ\text{C} \leq T_j \leq 125^\circ\text{C}$  unless otherwise noted.

Output Voltage			5V			12V			15V			Units
Input Voltage (unless otherwise noted)			10V			19V			23V			
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Short-Circuit Current	$T_j = 25^\circ\text{C}$		2.1			1.5			1.2		A
	Peak Output Current	$T_j = 25^\circ\text{C}$		2.4			2.4			2.4		A
	Average TC of $V_{\text{OUT}}$	$0^\circ\text{C} \leq T_j \leq +125^\circ\text{C}$ , $I_o = 5 \text{ mA}$		0.6			1.5			1.8		mV/°C
$V_{\text{IN}}$	Input Voltage Required to Maintain Line Regulation	$T_j = 25^\circ\text{C}$ , $I_o \leq 1\text{A}$		7.5			14.6			17.7		V

Note 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

Note 2: All characteristics are measured with capacitor across the input of 0.22 µF, and a capacitor across the output of 0.1µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ( $t_w \leq 10 \text{ ms}$ , duty cycle  $\leq 5\%$ ). Output voltage changes due to changes in internal temperature must be taken into account separately.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. For guaranteed specifications and the test conditions, see Electrical Characteristics.

# Appendix B

## Mathematical Derivations

This appendix contains a few selected derivations. More derivations are available at the Web site that supports this book: [www.malvino.com](http://www.malvino.com).

### Proof of Eq. (9-10)

The starting point for this derivation is the rectangular *pn* junction equation derived by Shockley:

$$I = I_s(e^{Vq/kT} - 1) \quad (\text{B-1})$$

where  $I$  = total diode current

$I_s$  = reverse saturation current

$V$  = total voltage across the depletion layer

$q$  = charge on an electron

$k$  = Boltzmann's constant

$T$  = absolute temperature, °C + 273

Equation (B-1) does *not* include the bulk resistance on either side of the junction. For this reason, the equation applies to the total diode only when the voltage across the bulk resistance is negligible.

At room temperature,  $q/kT$  equals approximately 40, and Eq. (B-1) becomes:

$$I = I_s(e^{40V} - 1) \quad (\text{B-2})$$

(Some books are 39V, but this is a small difference.) To get  $r'_e$ , we differentiate  $I$  with respect to  $V$ :

$$\frac{dI}{dV} = 40I_s e^{40V}$$

Using Eq. (B-2), we can rewrite this as:

$$\frac{dI}{dV} = 40(I + I_s)$$

Taking the reciprocal gives  $r'_e$ :

$$r'_e = \frac{dV}{dI} = \frac{1}{40(I + I_s)} = \frac{25 \text{ mV}}{I + I_s} \quad (\text{B-3})$$

Equation (B-3) includes the effect of reverse saturation current. In a practical linear amplifier,  $I$  is much greater than  $I_s$  (otherwise, the bias is unstable). For this reason, the practical value of  $r'_e$  is

$$r'_e = \frac{25 \text{ mV}}{I}$$

Since we are talking about the emitter depletion layer, we add the superscript  $E$  to get

$$r'_e = \frac{25 \text{ mV}}{I_E}$$

## Proof of Eq. (12-27)

In Fig. 12-18a, the instantaneous power dissipation during the *on* time of the transistor is

$$p = V_{CE}I_C \\ = V_{CEQ}(1 - \sin \theta)I_{C(sat)} \sin \theta$$

This is for the half-cycle when the transistor is conducting; during the *off* half-cycle,  $p = 0$  ideally.

The average power dissipation equals:

$$P_{av} = \frac{\text{area}}{\text{period}} = \frac{1}{2\pi} \int_0^\pi V_{CEQ}(1 - \sin \theta)I_{C(sat)} \sin \theta d\theta$$

After evaluating the definite integral over the half-cycle limits of 0 to  $\pi$ , and dividing by the period  $2\pi$ , we have the average power over the *entire cycle* for one transistor:

$$P_{av} = \frac{1}{2\pi} V_{CEQ} I_{C(sat)} \left[ -\cos \theta - \frac{\theta}{2} \right]_0^\pi \\ = 0.068 V_{CEQ} I_{C(sat)} \quad (B-4)$$

This is power dissipation in each transistor over the entire cycle, assuming 100 percent swing over the ac load line.

If the signal does not swing over the entire load line, the instantaneous power equals

$$p = V_{CE}I_C = V_{CEQ}(1 - k \sin \theta)I_{C(sat)}k \sin \theta$$

where  $k$  is a constant between 0 and 1;  $k$  represents the fraction of the load line being used. After integrating:

$$P_{av} = \frac{1}{2\pi} \int_0^\pi p d\theta$$

you get:

$$P_{av} = \frac{V_{CEQ} I_{C(sat)}}{2\pi} \left( 2k - \frac{\pi k^2}{2} \right) \quad (B-5)$$

Since  $P_{av}$  is a function of  $k$ , we can differentiate and set  $dP_{av}/dk$  equal to zero to find the maximizing value of  $k$ :

$$\frac{dP_{av}}{dk} = \frac{V_{CEQ} I_{C(sat)}}{2\pi} (2 - k\pi) = 0$$

Solving for  $k$  gives:

$$k = \frac{2}{\pi} = 0.636$$

With this value of  $k$ , Eq. (B-5) reduces to

$$P_{av} = 0.107 V_{CEQ} I_{C(sat)} \approx 0.1 V_{CEQ} I_{C(sat)}$$

Since  $I_{C(sat)} = V_{CEQ}/R_L$  and  $V_{CEQ} = MPP/2$ , the foregoing equation can be written as

$$P_{D(\max)} = \frac{MPP^2}{40R_L}$$

## Proof of Eqs. (13-15) and (13-16)

Start with the transconductance equation:

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2 \quad (\text{B-6})$$

The derivative of this is:

$$\frac{dI_D}{dV_{GS}} = g_m = 2I_{DSS} \left[ 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right] \left[ -\frac{1}{V_{GS(\text{off})}} \right]$$

or

$$g_m = -\frac{2I_{DSS}}{V_{GS(\text{off})}} \left[ 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right] \quad (\text{B-7})$$

When  $V_{GS} = 0$ , we get:

$$g_{m0} = -\frac{2I_{DSS}}{V_{GS(\text{off})}} \quad (\text{B-8})$$

or by rearranging:

$$V_{GS(\text{off})} = -\frac{2I_{DSS}}{g_{m0}}$$

This proves Eq. (13-15). By substituting the left member of Eq. (B-8) into Eq. (B-7):

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]$$

This is the proof of Eq. (13-16).

## Proof of Eq. (18-2)

The equation of a sinusoidal voltage is:

$$v = V_P \sin \omega t$$

The derivative with respect to time is:

$$\frac{dv}{dt} = \omega V_P \cos \omega t$$

The maximum rate of change occurs for  $t = 0$ . Furthermore, as the frequency increases, we reach the point at which the maximum rate of change just equals the slew rate. At this critical point:

$$S_R = \left( \frac{dv}{dt} \right)_{\max} = \omega_{\max} V_P = 2\pi f_{\max} V_P$$

Solving for  $f_{\max}$  in terms of  $S_R$ , we get:

$$f_{\max} = \frac{S_R}{2\pi V_P}$$

## Proof of Eq. (19-10)

Here is the derivation for closed-loop output impedance. Begin with:

$$A_{v(CL)} = \frac{A_{VOL}}{1 + A_{VOL}B}$$

Substitute:

$$A_v = A_u \frac{R_L}{r_{out} = R_L}$$

where  $A_v$  is the loaded gain ( $R_L$  connected) and  $A_u$  is the unloaded gain ( $R_L$  disconnected). After substitution for  $A_v$ , the closed-loop gain simplifies to:

$$A_{v(CL)} = \frac{A_u}{1 + A_u B + r_{out}/R_L}$$

When:

$$1 + A_u B = \frac{r_{out}}{R_L}$$

$A_{v(CL)}$  will drop in half, implying that the load resistance matches the Thevenin output resistance of the feedback amplifier. Solving for  $R_L$  gives:

$$R_L = \frac{r_{out}}{1 + A_u B}$$

This is the value of load resistance that forces the closed-loop voltage gain to drop in half, equivalent to saying it equals the closed-loop output impedance:

$$r_{out(CL)} = \frac{r_{out}}{1 + A_u B}$$

In any practical feedback amplifier,  $r_{out}$  is much smaller than  $R_L$ , so that  $A_{VOL}$  approximately equals  $A_u$ . This is why you almost always see the following expression for output impedance:

$$r_{out(CL)} = \frac{r_{out}}{1 + A_{VOL} B}$$

where  $r_{out(CL)}$  = closed-loop output impedance

$r_{out}$  = open-loop output impedance

$A_{VOL} B$  = open-loop gain

### Proof of Eq. (19-23)

Because of the virtual ground in Fig. 19-12, essentially all of the input current flows through  $R_1$ . Summing voltages around the circuit gives:

$$-v_{error} + i_{in}R_2 - (i_{out} - i_{in})R_1 = 0 \quad (B-9)$$

With the following substitutions:

$$v_{error} = \frac{v_{out}}{A_{VOL}}$$

and

$$v_{out} = i_{out}R_L + (i_{out} - i_{in})R_1$$

Eq. (B-9) can be rearranged as:

$$\frac{i_{out}}{i_{in}} = \frac{A_{VOL}R_2 + (1 + A_{VOL})R_1}{R_L + (1 + A_{VOL})R_1}$$

Since  $A$  is usually much greater than 1, this reduces to:

$$\frac{i_{out}}{i_{in}} = \frac{A_{VOL}(R_1 + R_2)}{R_L + A_{VOL}R_1}$$

Furthermore,  $AR_2$  is usually much greater than  $R_L$ , and the foregoing simplifies to

$$\frac{i_{\text{out}}}{i_{\text{in}}} = \frac{R_2}{R_1} + 1$$

### Proof of Eq. (22-17)

The change in capacitor voltage is given by:

$$\Delta V = \frac{IT}{C} \quad (\text{B-10})$$

In the positive half-cycle of input voltage (Fig. 22-28a), the capacitor charging current is ideally:

$$I = \frac{V_p}{R}$$

Since  $T$  is the rundown time of the output ramp, it represents half of the output period. If  $f$  is the frequency of the input square wave, then  $T = 1/2f$ . Substituting for  $I$  and  $T$  in Eq. (B-10) gives:

$$\Delta V = \frac{V_p}{2fRC}$$

The input voltage has a peak value of  $V_p$ , while the output voltage has a peak-to-peak value of  $\Delta V$ . Therefore, the equation can be written as

$$v_{\text{out(p-p)}} = \frac{V_p}{2fRC}$$

### Proof of Eq. (22-18)

The UTP has a value of  $+BV_{\text{sat}}$  and the LTP a value of  $-BV_{\text{sat}}$ . Start with the basic switching equation that applies to any  $RC$  circuit:

$$v = v_i + (v_f - v_i)(1 - e^{-t/RC}) \quad (\text{B-11})$$

where  $v$  = instantaneous capacitor voltage

$v_i$  = initial capacitor voltage

$v_f$  = target capacitor voltage

$t$  = charging time

$RC$  = time constant

In Fig. 22-32b, the capacitor charge starts with an initial value of  $-BV_{\text{sat}}$  and ends with a value of  $+BV_{\text{sat}}$ . The target voltage for the capacitor voltage is  $+V_{\text{sat}}$  and the capacitor charging time is half a period,  $T/2$ . Substitute into Eq. (B-11) to get:

$$BV_{\text{sat}} = -BV_{\text{sat}} + (V_{\text{sat}} + BV_{\text{sat}})(1 - e^{-T/2RC})$$

This simplifies to:

$$\frac{2B}{1+B} = 1 - e^{-T/2RC}$$

By rearranging and taking the antilog, the foregoing becomes:

$$T = 2RC \ln \frac{1+B}{1-B}$$

### Proof of Eq. (23-25)

Start with Eq. (B-11), the switching equation for any  $RC$  circuit. In Fig. 23-33, the initial capacitor voltage is zero, the target capacitor voltage is  $+V_{CC}$ , and the final capacitor voltage is  $+2V_{CC}/3$ . Substitute into Eq. (B-11) to get:

$$\frac{2V_{CC}}{3} = V_{CC}(1 - e^{-W/RC})$$

This simplifies to:

$$e^{-W/RC} = \frac{1}{3}$$

Solving for  $W$  gives

$$W = 1.0986RC \approx 1.1RC$$

### Proof of Eqs. (23-28) and (23-29)

In Fig. 23-36, the capacitor upward charge takes time  $W$ . The capacitor voltage starts at  $+V_{CC}/3$  and ends at  $+2V_{CC}/3$  with a target voltage of  $+V_{CC}$ . Substitute into Eq. (B-11) to get:

$$\frac{2V_{CC}}{3} = \frac{V_{CC}}{3} + \left( V_{CC} - \frac{V_{CC}}{3} \right) (1 - e^{-W/RC})$$

This simplifies to:

$$e^{-W/RC} = 0.5$$

or

$$W = 0.693RC = 0.693(R_1 + R_2)C$$

The discharge equation is similar, except that  $R_2$  is used instead of  $R_1 + R_2$ . In Fig. 23-36, the discharge time is  $T - W$ , which leads to:

$$T - W = 0.693R_2C$$

Therefore, the period is:

$$T = 0.693(R_1 + R_2)C + 0.693R_2C$$

and the duty cycle is:

$$D = \frac{0.693(R_1 + R_2)C}{0.693(R_1 + R_2)C + 0.693R_2C} \times 100\%$$

or

$$D = \frac{R_1 + R_2}{R_1 + 2R_2} \times 100\%$$

To get the frequency, take the reciprocal of the period  $T$ :

$$f = \frac{1}{T} = \frac{1}{0.693(R_1 + R_2)C + 0.693R_2C}$$

or

$$f = \frac{1.44}{(R_1 + 2R_2)C}$$

# Appendix C

## Introduction

In an effort to help the reader understand the concepts presented in this textbook, key examples and problems will be presented through the use of computer simulation using MultiSim. MultiSim is an interactive circuit simulation package that allows the student to view their circuit in schematic form while measuring the different parameters of the circuit. The ability to create a schematic quickly and then analyze the circuit through simulation makes MultiSim a wonderful tool to help students understand the concepts covered in the study of electronics.

This primer will introduce the reader to the features of MultiSim that directly relate to the study of DC, AC, and semiconductor electronics. The topics covered are:

- Work Area
- Opening a File
- Running a Simulation
- Saving a File
- Components
- Sources
- Measurement Equipment
- Circuit Examples

## Work Area

The power of this software lies in its simplicity. With just a few steps, a circuit can be either retrieved from disk or drawn from scratch and simulated. The main screen, as shown in Figure C-1, is divided into three areas: The drop down menu, the tool bars, and the work area.

The drop down menu gives the user access to all the functions of the program. Initially, the user will only utilize a few of the different menu selections. Each of the drop down menu main topics can be accessed by either a mouse click or by pressing the <alt> key and the underlined letter. For example, to access the File menu simply press <ALT><F> at the same time. The File menu will drop down as shown in Figure C-2.

Initially, there are only two selections from the drop down menu that need be mastered: Opening a file and saving a file. The rest of the menu options can be explored as time permits.

The tool bars beneath the drop down menu provide access to all of the menu selections. Typically, a user will access them through the tool bars instead of the drop down menus. The most important icon in the assorted tool bars is the on-off switch. The on-off switch starts and stops the simulation. The push button next to the on-off switch will pause the simulation. Pressing the Pause button while the simulation is running allows the viewing of a waveform or meter reading without the display changing.

Figure C-1 Main Screen

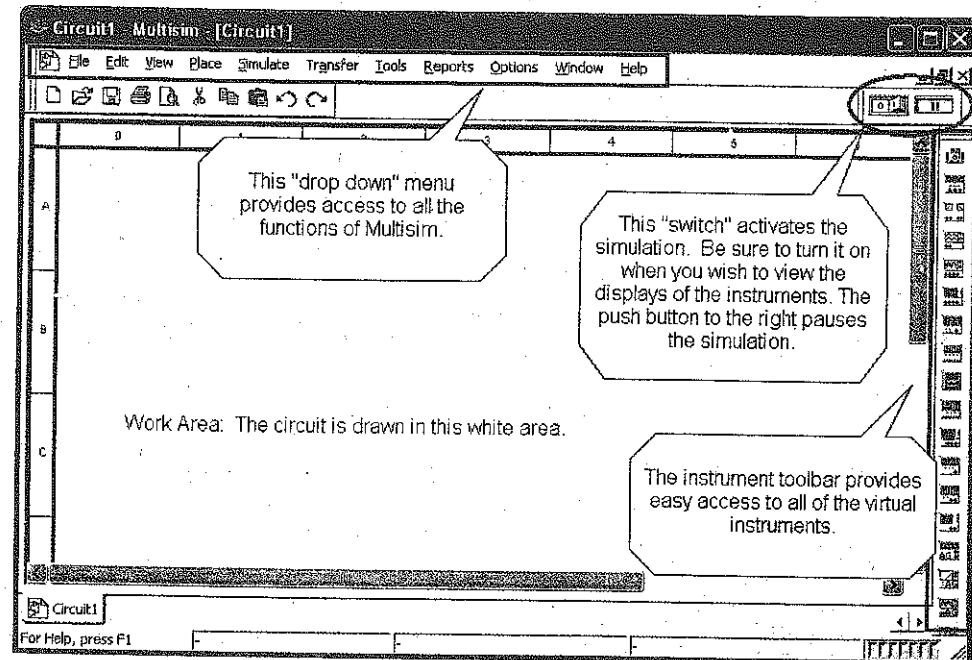
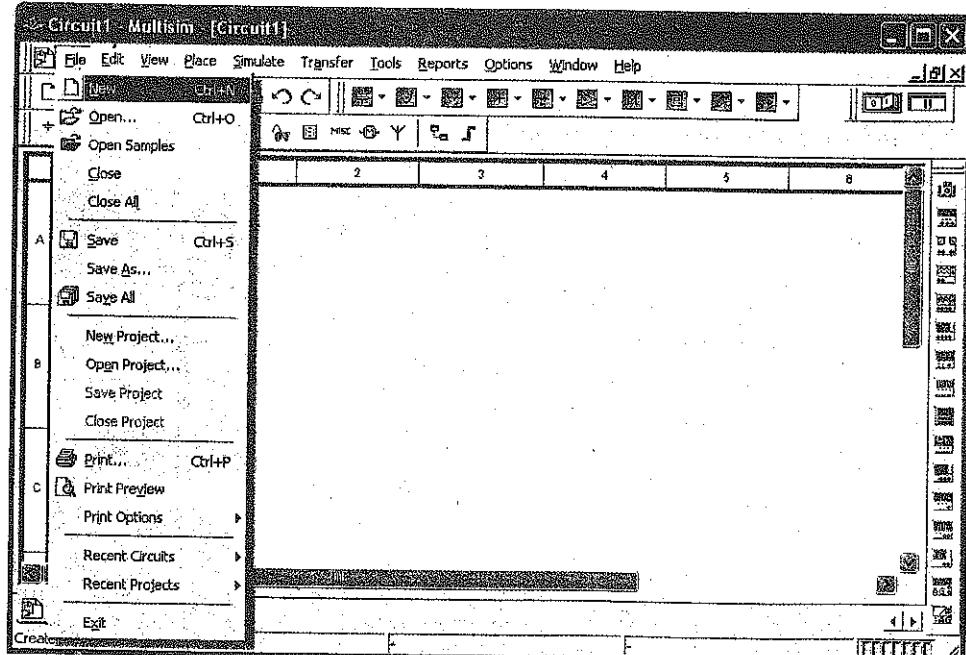


Figure C-2 File Drop Down Menu



## Opening a File

The circuits referenced in this textbook are included on a compact disk located in the back of this textbook. The files are divided into folders, one for each chapter. The name of the file provides a wealth of information to the user.

**Example:** A typical file name would be "Ch 4 Problems 4-11." This first part of the file name tells the user that the file is located in the folder labeled "Chapter 4." The second part of the file name tells the user that it is question 11 out of the Problems section at the end of chapter 4.

Figure C-3 Opening a File

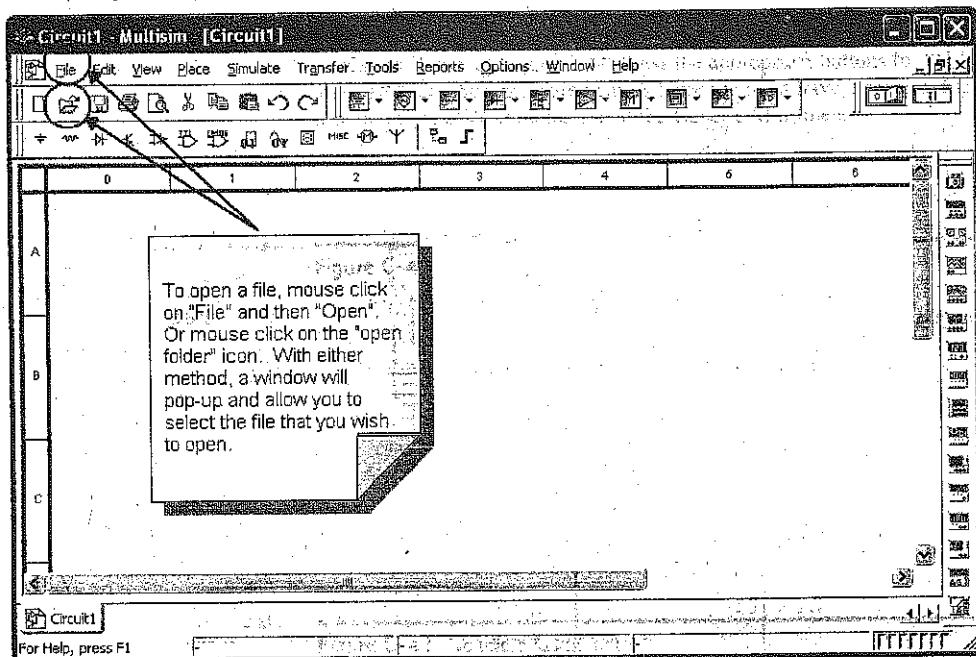
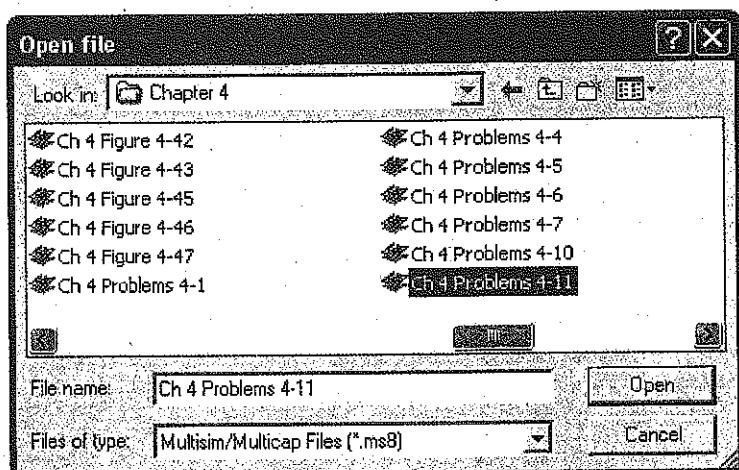


Figure C-4 Open file Dialog Box



To open a file, either mouse click on the word "File" located on the drop down menu bar and then mouse click on the Open command or mouse click on the open folder icon located on the tool bar as shown in Figure C-3. Both methods will cause the Open File dialog box shown in Figure C-4 to pop open. Navigate to the appropriate chapter folder and retrieve the file needed.

## Running a Simulation

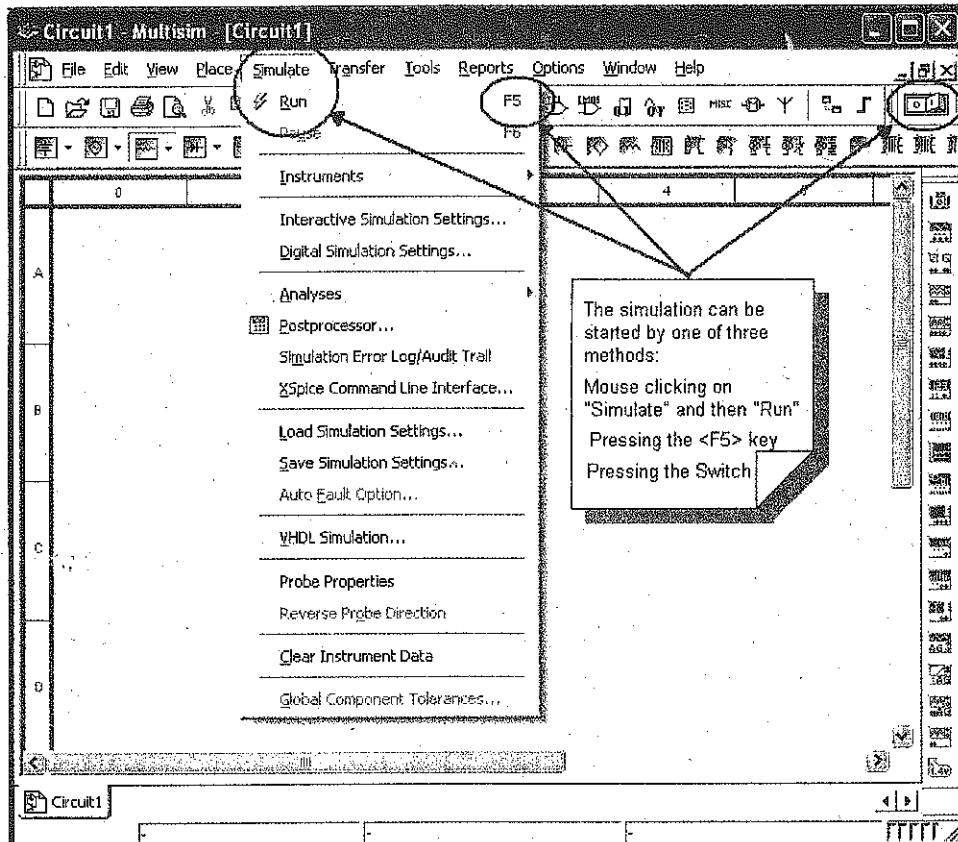
The MultiSim files developed for this textbook present the circuit in a standard format. The instrumentation is typically connected to the appropriate places within the circuit. If the instrument's display is not visible, double mouse click on the instrument icon and the display will pop up. There is a help screen referred to as the "Description Box" with helpful information relating to the circuit and the instruments within the circuit. This Description Box is opened by pressing <Control>+<D> while in MultiSim.

The simulation can be started three ways:

- Selecting "Simulate" from the drop down menu and then selecting "Run"
- Pressing the <F5> key
- Pressing the toggle switch with a mouse click

All three of these ways are illustrated in Figure C-5.

**Figure C-5** Starting the Simulation



## Saving a File

If the file has been modified, it needs to be saved under a new file name. As shown in Figure C-6, select "File" with a mouse click located on the drop down menu bar. Then select "Save As" from the drop down menu. This will cause the "Save As" dialog box to open. Give the file a new name and "Press" the save button with a mouse click. The process is demonstrated in Figure C-7.

Figure C-6 "Save As . ." Screen

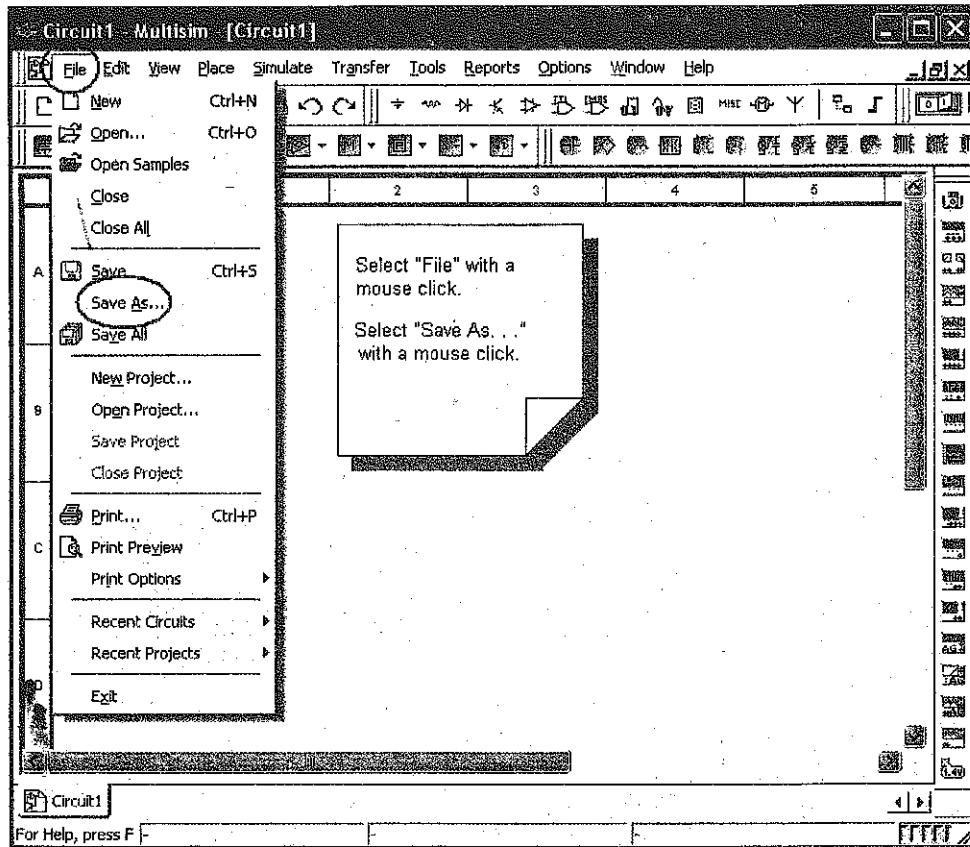
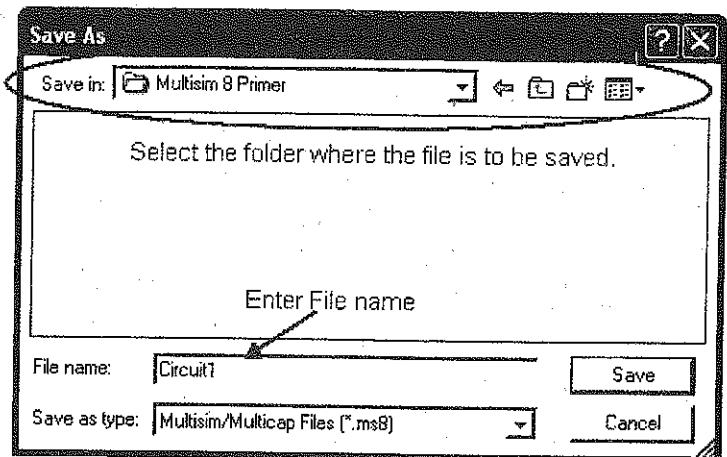


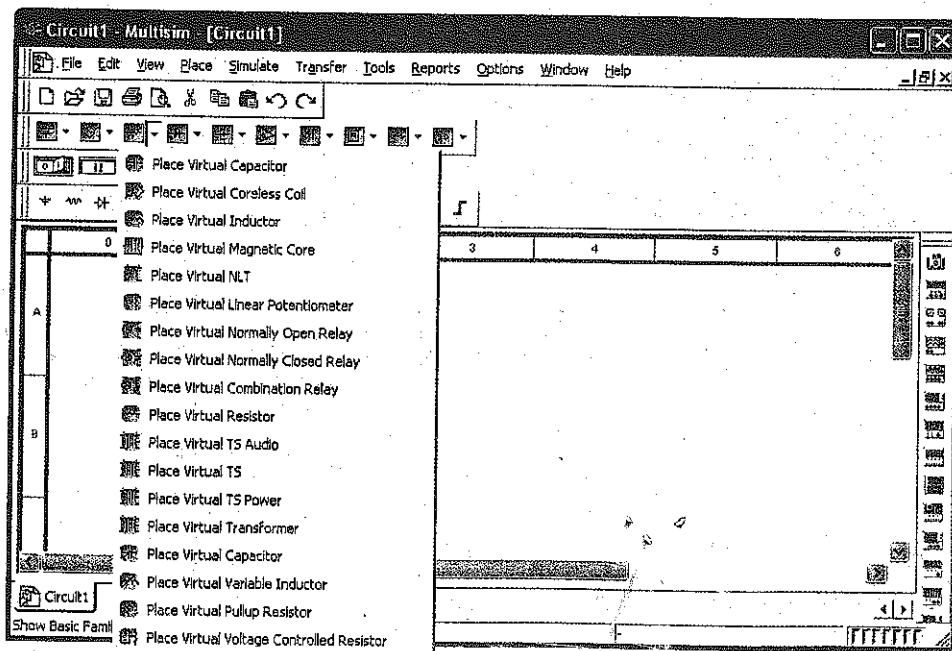
Figure C-7 "Save As . . ." Dialog Box



## Components

There are two kinds of component models used in MultiSim: Those modeled after actual components and those modeled after "ideal" components. Those modeled after ideal components are referred to as "virtual" components. There is a broad selection of virtual components available, as shown in Figure C-8.

Figure C-8 Virtual Component List



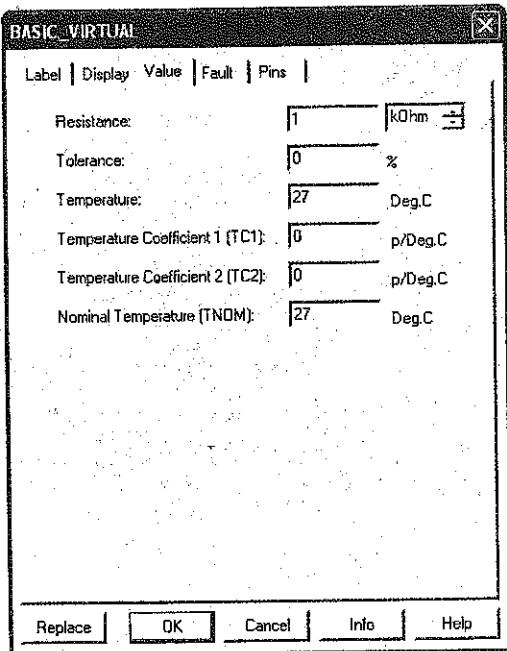
The difference between the two types of components resides in their rated values. The virtual components can have any of their parameters varied, whereas those modeled after actual components are limited to real world values. For example, a virtual resistor can have any value resistance and percent tolerance as shown in Figure C-9.

The models of the actual resistors are limited to standard values with either a 1% or 5% tolerance. The same is true for all other components modeled after real components, as shown in Figure C-10. This is especially important when the semiconductor devices are used in a simulation. Each of the models of actual semiconductors will function in accordance with their data sheets. These components will be listed by their actual device number as identified by the manufacturers. For example, a common diode is the 1N4001. This diode, along with many others, can be found in the semiconductor library of actual components. The parameters of the actual components libraries can also be modified, but that requires an extensive understanding of component modeling and is beyond the scope of this primer.

If actual components are selected for a circuit to be simulated, the measured value may differ slightly from the calculated values as the software will utilize the tolerances to vary the results. If precise results are required, the virtual components can be set to specific values with a zero percent tolerance.

Two of the components require interaction with the user. The switch is probably the most commonly used of these two devices. The movement of the switch is triggered by pressing the key associated with each switch as shown in Figure C-11. The key is selected while in the switch configuration screen, Figure C-12. If two switches are assigned the same key, they both will move when the key is pressed.

**Figure C-9** Configuration Screen for a Virtual Resistor



**Figure C-10** Component Listing for Resistors

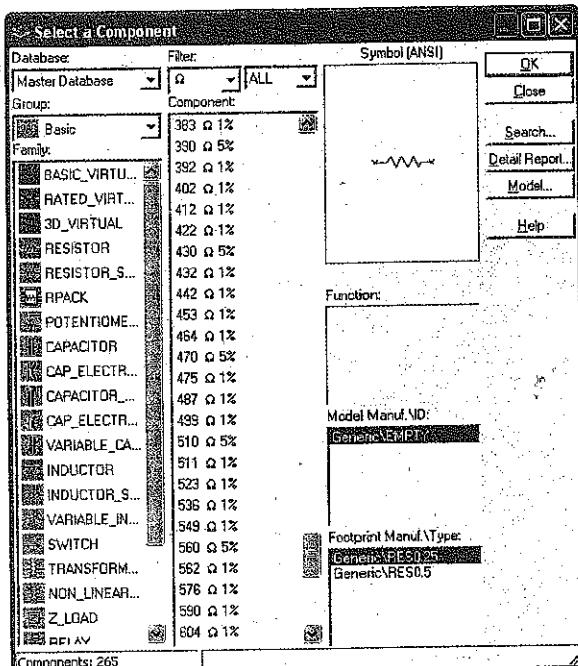


Figure C-11 Switches

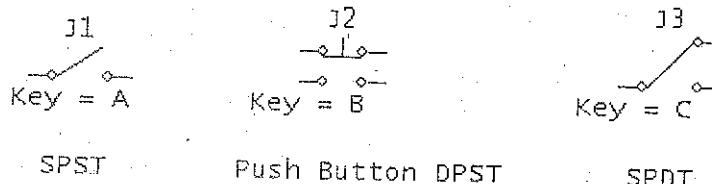
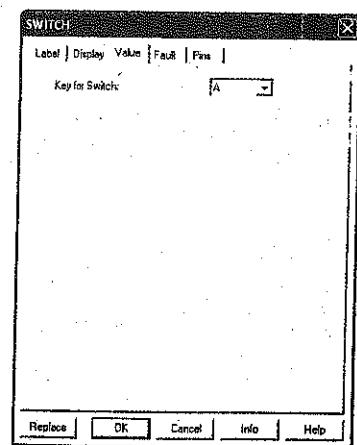


Figure C-12 Switch Configuration Screen



The second component that requires interaction with the user is the potentiometer. The potentiometer will vary its resistance in predetermined steps with each key press. The pressing of the associated letter on the keyboard will increase the resistance and the pressing of the <shift> key and the letter will decrease the resistance. As shown in Figure C-13, the percent of the total resistance is displayed next to the potentiometer. The incremental increase or decrease of resistance is set by the user in the configuration screen. The associated key is also set in the configuration screen as shown in Figure C-14.

Figure C-13 Potentiometer

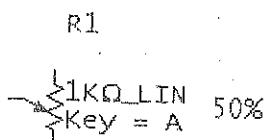
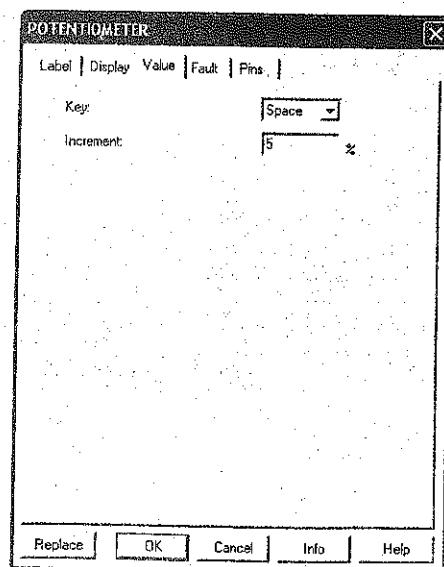
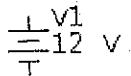


Figure C-14 Potentiometer Configuration Screen



## Sources

Figure C-15 DC Source as a Battery



In the study of DC and AC electronics, the majority of the circuits include either a voltage or current source. There are two main types of voltage sources: DC and AC sources. The DC source can be represented two ways: As a battery in Figure C-15 and as a voltage supply.

The voltage rating is fully adjustable. The default value is 12 VDC. If the component is double clicked, the configuration screen shown in Figure C-16 will pop up and the voltage value can be changed.

The voltage supplies are used in semiconductor circuits to represent either a positive or negative voltage supply. Figure C-17 contains the V<sub>CC</sub> voltage supply used in transistor circuits. FET circuits will utilize the V<sub>DD</sub> voltage supply as illustrated in Figure C-18.

Figure C-19 depicts the +V<sub>CC</sub> and the -V<sub>EE</sub> voltage sources. These sources are found in operational amplifier circuits. Operational amplifiers typically have two voltage supplies: a negative (V<sub>EE</sub>) and a positive (V<sub>CC</sub>) voltage supply, Figure C-20.

Figure C-16 Configuration Screen for the DC Source

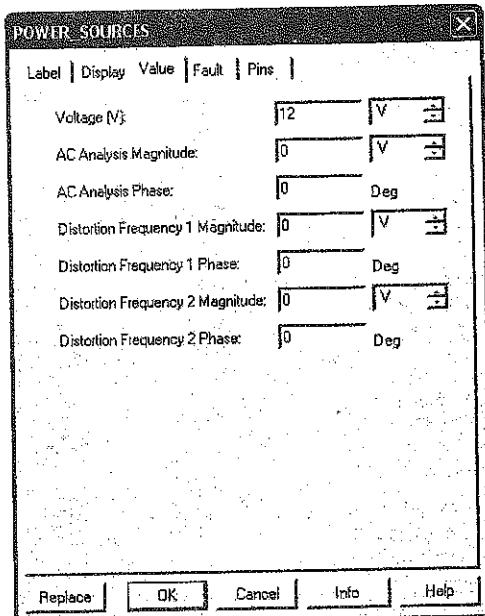


Figure C-17 V<sub>CC</sub> Voltage Source

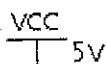


Figure C-18 V<sub>DD</sub> Voltage Source

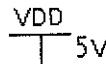
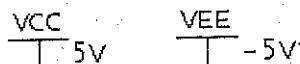
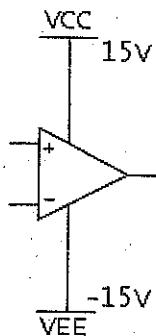


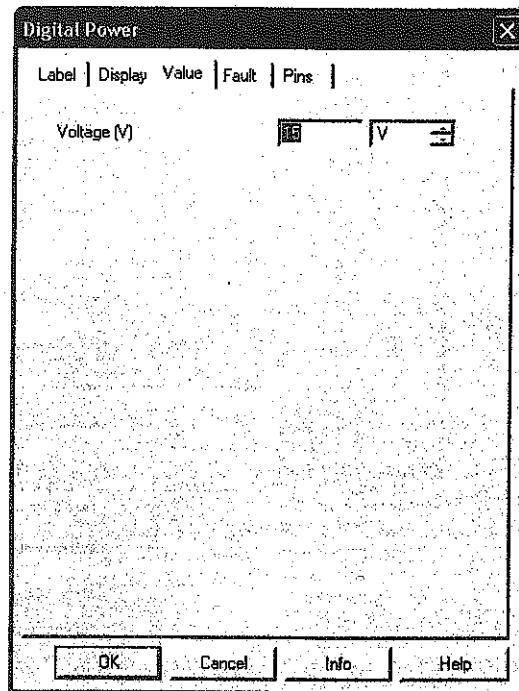
Figure C-19 V<sub>CC</sub> and V<sub>EE</sub> Voltage Sources



**Figure C-20**  $V_{CC}$  and  $V_{EE}$  Op Amp Example



**Figure C-21**  $V_{CC}$  Configuration Screen



The voltage rating is fully adjustable for all three voltage sources. The default value is +5 VDC for  $V_{CC}$  and  $V_{DD}$ . The default value for  $V_{EE}$  is -5 VDC. If the component is double clicked, the configuration screen shown in Figure C-21 will pop up and the voltage value can be changed.

The AC source can be represented as either a schematic symbol or it can take the form of a function generator. The schematic symbol as shown in Figure C-22 will include information about the AC source. This information will include the device reference number,  $V_{RMS}$  value, frequency, and phase shift. These values are fully adjustable. The default values are shown in Figure C-23. If the component is double clicked, the configuration screen will pop up and the value can be changed.

**Figure C-22** AC Source

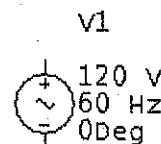
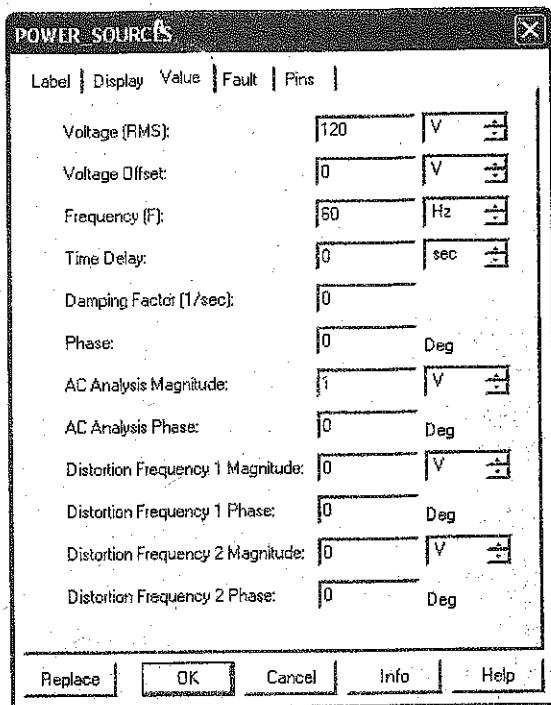


Figure C-23 Configuration Screen for an AC Source

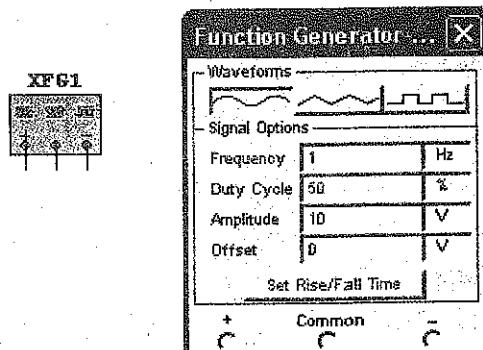


MultiSim provides two function generators: The generic model and the Agilent model. The Agilent model 33120A has the same functionality as the actual Agilent function generator.

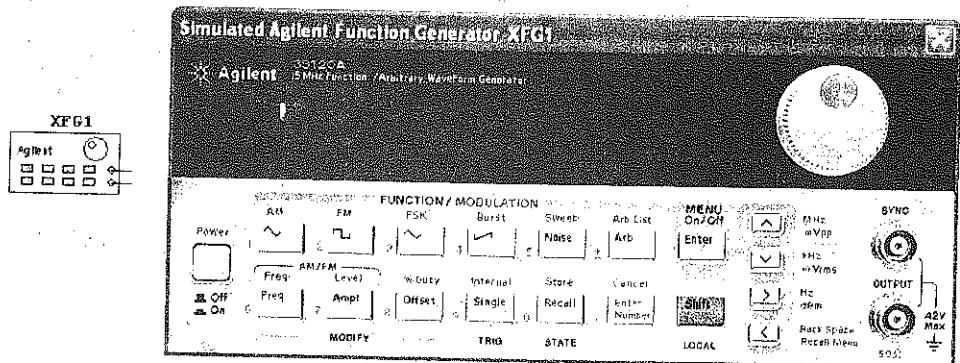
The generic function generator icon is shown in Figure C-24, along with the configuration screen. The configuration screen is displayed when the function generator icon is double clicked. The generic function generator can produce three types of waveforms: Sinusoidal wave, triangular wave, and a square wave. The frequency, duty cycle, amplitude, and DC offset are all fully adjustable.

The Agilent function generator is controlled via the front panel as shown in Figure C-25. The buttons are “pushed” by a mouse click. The dial can be turned by dragging the mouse over it or by placing the cursor over it and spinning the wheel on the mouse. The latter is by far the preferred method.

Figure C-24 Generic Function Generator and Configuration Screen



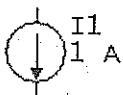
**Figure C-25** Agilent Function Generator



There are two types of current sources: DC and AC sources. The DC current source is represented as a circle with a downward pointing arrow in it. The arrow in Figure C-26 represents the direction of current flow. The arrow can be pointed downward for conventional current flow. Electron current flow can be simulated by rotating the symbol 180° and the arrow will point upwards.

The current rating is fully adjustable. The default value is 1 A. If the component is double clicked, the configuration screen in Figure C-27 will pop up and the current value can be changed.

**Figure C-26** DC Current Source



**Figure C-27** DC Current Source Configuration Screen

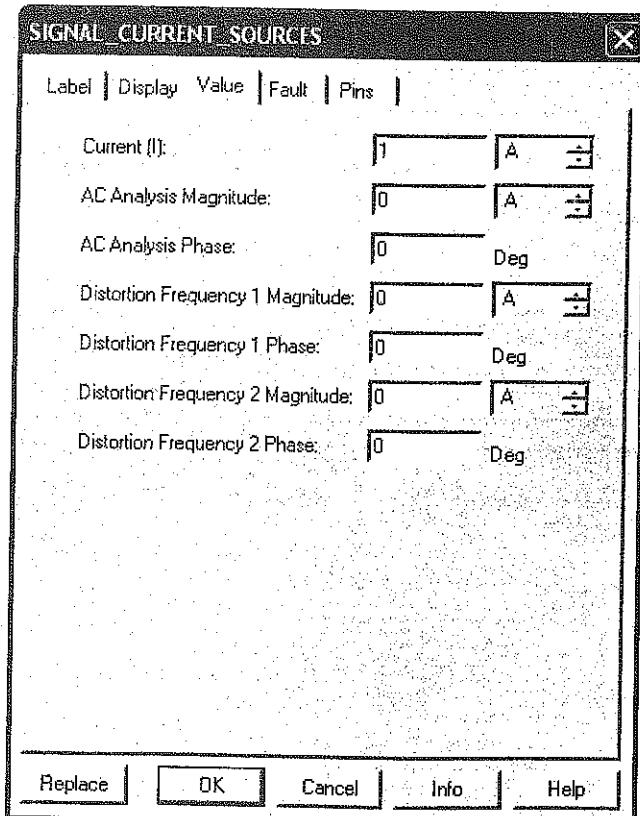


Figure C-28 AC Current Source

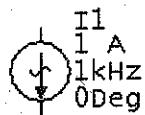
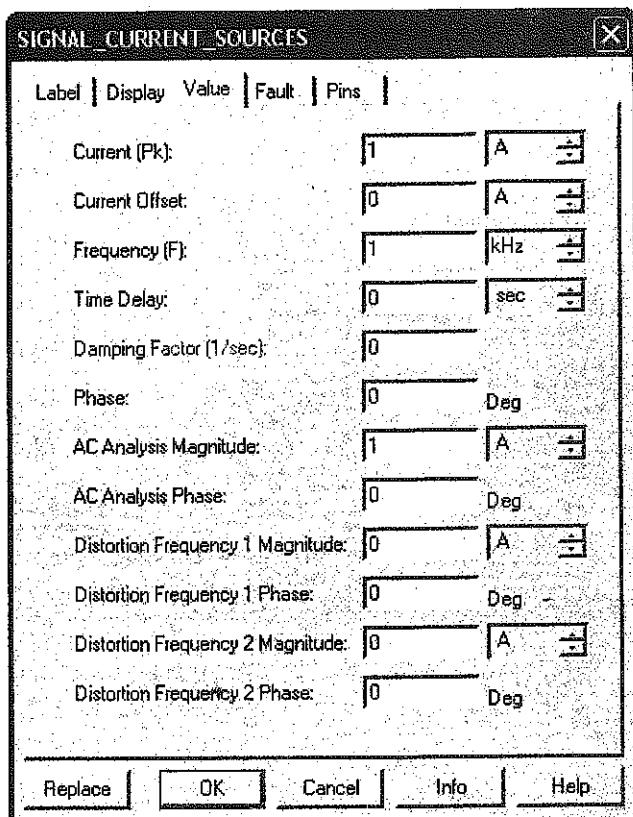


Figure C-29 AC Current Source Configuration Screen



The AC current source is represented as a circle with a downward pointing arrow. There is a sine wave across the arrow. The schematic symbol in Figure C-28 will include information about the AC current source. This information will include the device reference number,  $I_{peak}$  value, frequency, and phase shift. These values are fully adjustable. The default values are shown in Figure C-29. If the component is double clicked, the configuration screen will pop up and the values can be changed.

MultiSim requires a ground to be present in the circuit in order for the simulation to function properly. The circuit must contain a ground and all instrumentation must have a ground connection. The schematic symbol for ground is shown in Figure C-30.

Figure C-30 Ground



## Measurement Equipment

MultiSim provides a wide assortment of measurement equipment. In the study of DC, AC and semiconductor electronics, the three main pieces of measurement equipment are the digital Multimeter, the oscilloscope, and the Bode Plotter. The first two pieces of equipment are found in test labs across the world. The Bode Plotter is a fictitious device that automates the task of plotting output voltage versus frequency. This is usually done by taking many measurements and plotting the results in a spreadsheet. The Bode Plotter performs this task for you.

## Multimeters

There are two Multimeters to choose from: The Generic Multimeter and the Agilent Multimeter. The Generic Multimeter will measure current, voltage, resistance, and decibels. The meter can be used for both DC and AC measurements. The different functions of the meter are selected by mouse clicking on the icon to the left in Figure C-31. The mouse click will cause the Multimeter display to pop up. The different functions on the display can be selected "pushing" the different buttons via a mouse click.

The Agilent Multimeter icon and meter display are shown in Figure C-32. The display is brought up by mouse clicking on the Agilent Multimeter icon. This Multimeter has the same functionality as the actual Agilent Multimeter. The different functions are accessed by "pushing" the buttons. This is accomplished by mouse clicking on the button. The input jacks on the right side of the meter display correspond to the five inputs on the icon. If something is connected to the icon, the associated jacks on the display will have a white "X" in them to show a connection.

Figure C-31 Generic Multimeter icon and Configuration Screen

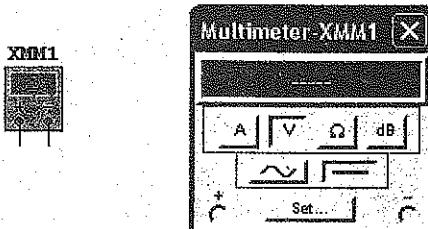
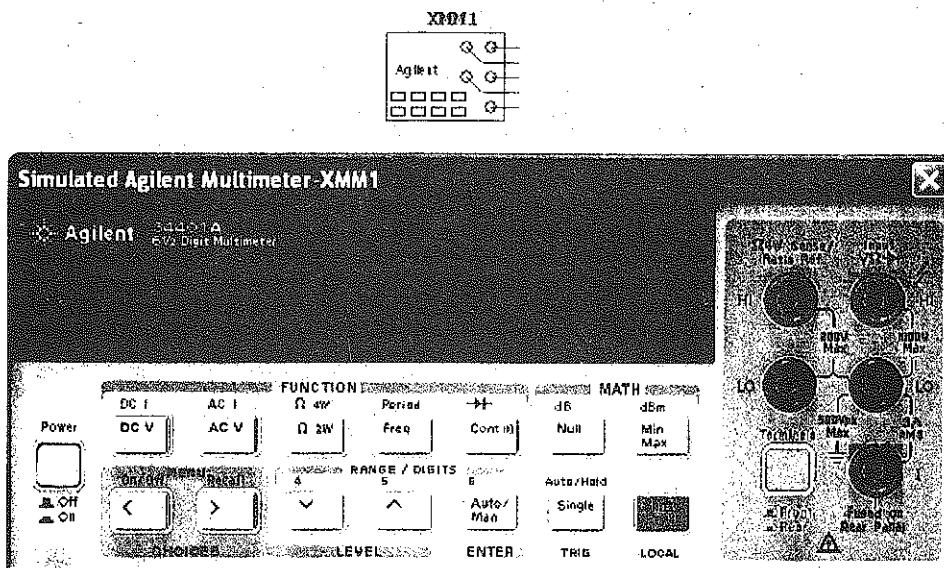


Figure C-32 Agilent Multimeter Icon and Meter Display.



## Oscilloscopes

There are three oscilloscopes to choose from: The Generic oscilloscope and the Agilent oscilloscope, and the Tektronix oscilloscope. The Generic oscilloscope shown in Figure C-33 is a dual channel oscilloscope. The oscilloscope display is brought up by mouse clicking on the oscilloscope icon. The settings can be changed by clicking in each box and bringing up the scroll arrows.

The Agilent oscilloscope icon in Figure C-34 has all of the functionality of the Model 54622D two channel oscilloscope. The Agilent oscilloscope is controlled via the front panel as shown in Figure C-35. The buttons are "pushed" by a mouse click. The dials can be turned by dragging the mouse over it or by placing the cursor over it and spinning the wheel on the mouse. The latter is by far the preferred method.

Figure C-33 Generic Oscilloscope Icon and Oscilloscope Display

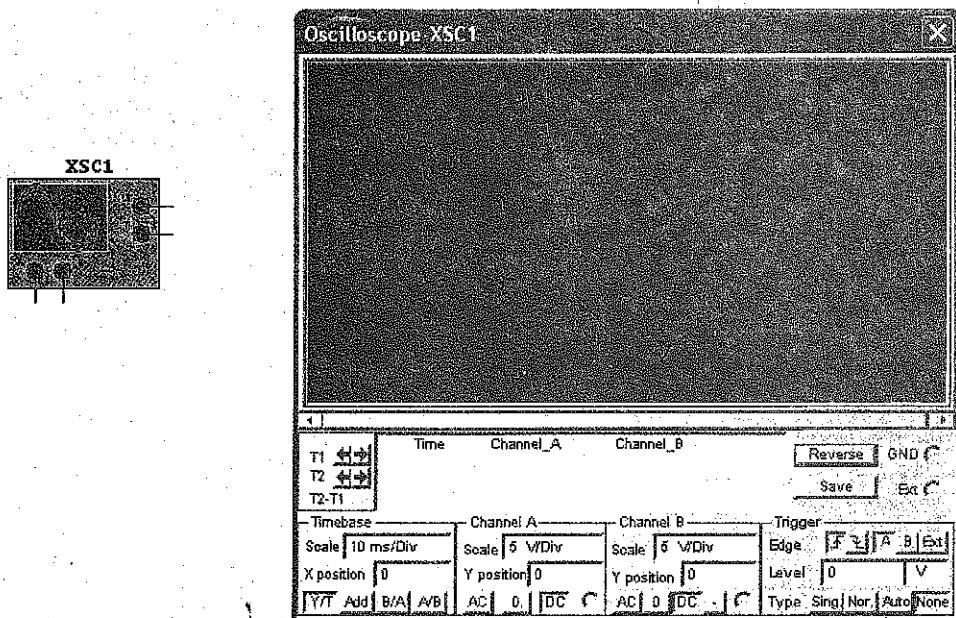


Figure C-34 Agilent Oscilloscope Icon

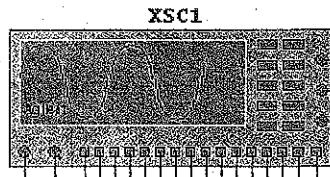


Figure C-35 Agilent Oscilloscope Display

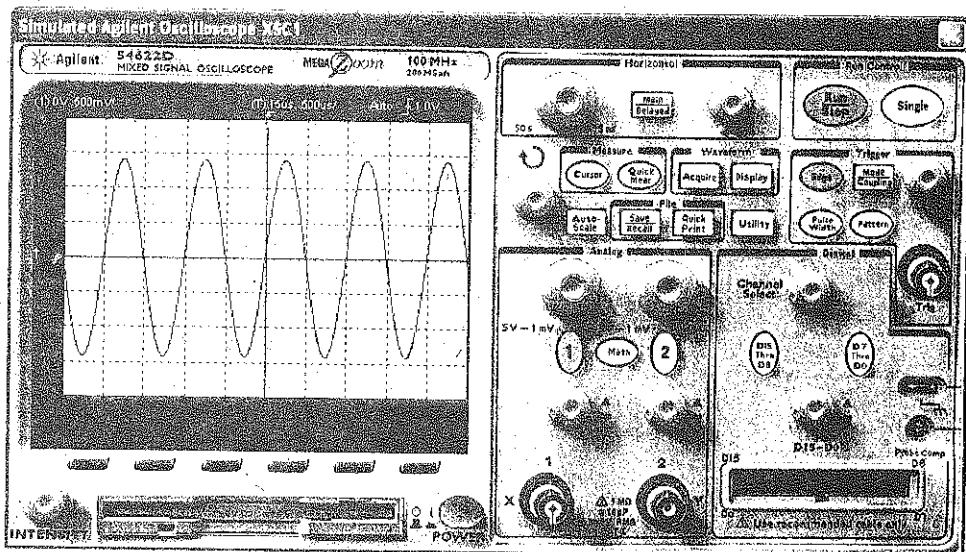
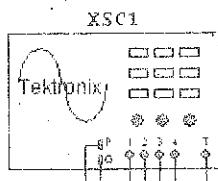
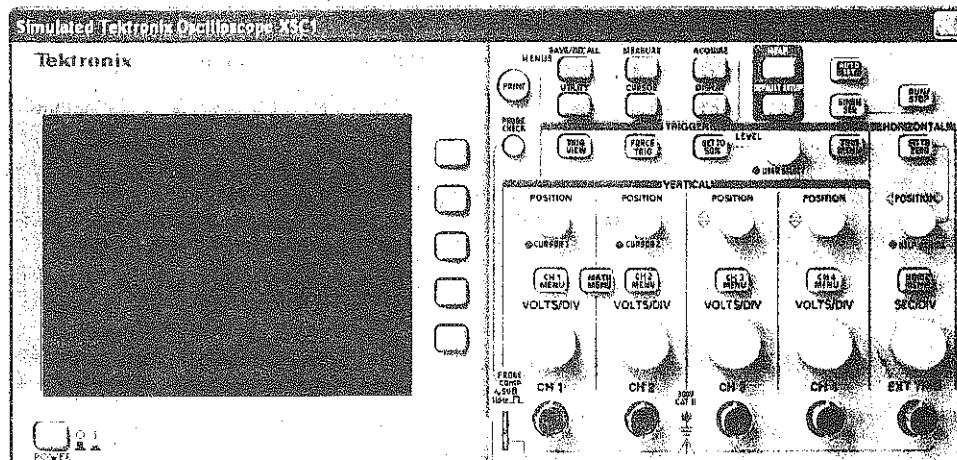


Figure C-36 Tektronix Oscilloscope Icon



The Tektronix oscilloscope icon shown in Figure C-36 has all of the functionality of the Model TDS2024 four channel Digital Storage oscilloscope. The color of the four channels is the same as the channel selection buttons on the display: Yellow, blue, purple, and green for channels one through four respectively. The Tektronix oscilloscope is controlled via the front panel as seen in Figure C-37. The buttons are “pushed” by a mouse click. The dials can be turned by dragging the mouse over it or by placing the cursor over it and spinning the wheel on the mouse. The latter is by far the preferred method.

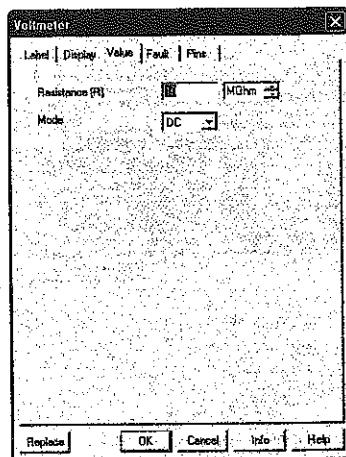
Figure C-37 Tektronix Oscilloscope Display



**Figure C-38** Voltage and Current Meters



**Figure C-39** Voltmeter Configuration Screen



### Voltage and Current Meters

When voltage or current need to be measured, MultiSim provides very simple voltmeters and ammeters as shown in Figure C-38. These meters can be placed throughout the circuit. The meters can be rotated to match the polarity needs of the circuit. The default is "DC." If the meters are to be used for AC measurement, then the configuration screen shown in Figure C-39 must be opened and that parameter changed to reflect AC measurement. To open the configuration screen, double click on the meter.

### Bode Plotter

The Bode Plotter is used to view the frequency response of a circuit. In the actual lab setting, the circuit would be operated at a base frequency and the output of the circuit measured. The frequency would be incremented by a fixed amount and the measurement repeated. After operating the circuit at a sufficient number of incremental frequencies, the data would be graphed, with independent variable "frequency" on the X axis and dependant variable "amplitude" on the Y axis. This process can be very time consuming. MultiSim provides a simpler method of determining the frequency response of a circuit through the use of the virtual Bode Plotter.

In Figure C-40, the positive terminal of the input is connected to the applied signal source. The positive terminal of the output is connected to the output voltage of the circuit. The other two terminals are connected to ground. The value of the AC source does not matter; the AC source just needs to be in the circuit. The Bode Plotter will provide the input signal.

Figure C-40 Bode Plotter

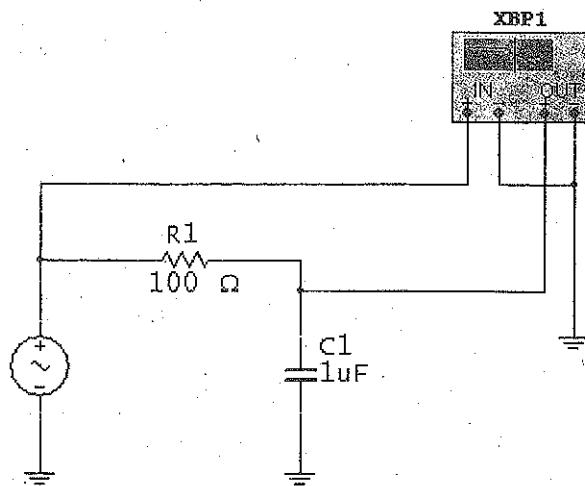
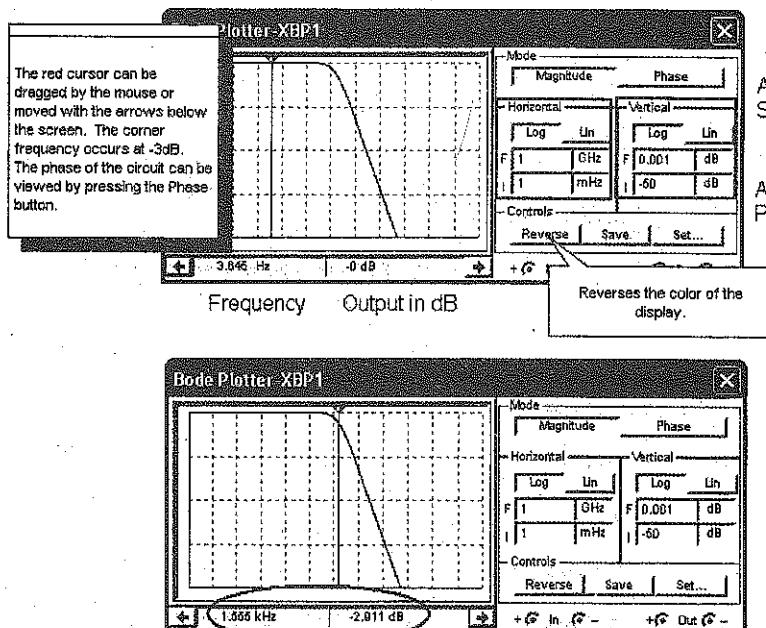


Figure C-41 Bode Plotter Display



## Circuit Examples

### Example 1 Voltage Measurement Using a Voltmeter in a Series DC Circuit

A voltmeter in Figure C-42 is placed in parallel with the resistor to measure the voltage across it. The default is set for "DC" measurement. If AC is required, double click on the meter to bring up the configuration screen. All circuits must have a ground. Figure C-43 contains a *Quick Hint* on the use of the Voltmeter.

### Example 2 Voltage Measurement Using a Generic Multimeter in a Series DC Circuit

A generic Multimeter is placed in parallel with the resistor to measure the voltage across it. Be sure to double click the generic Multimeter icon to bring up meter display as shown in Figure C-44. Press the appropriate buttons for "Voltage" and then "DC" or "AC" measurement. All circuits must have a ground. Figure C-45 contains a *Quick Hint* on the use of the Generic Multimeter.

Figure C-42 DC Voltage Measurement with a Voltmeter

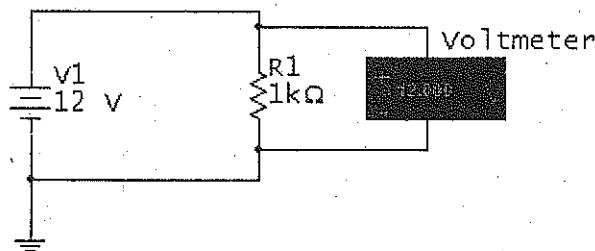
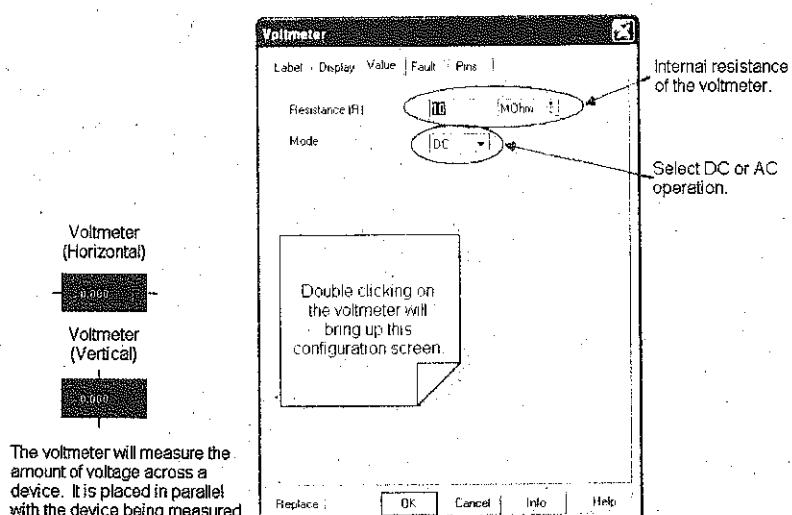
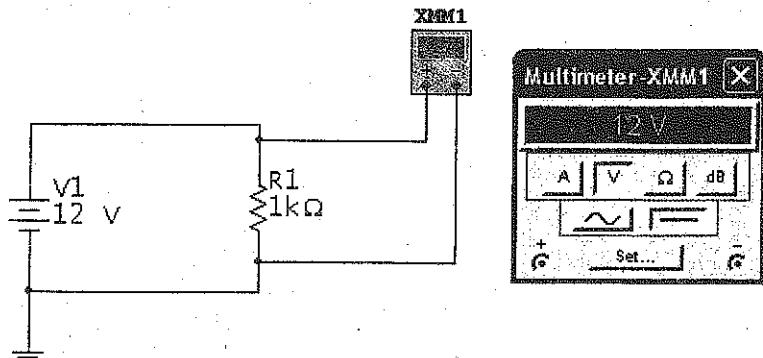


Figure C-43 Voltmeter Quick Hint



**Figure C-44** DC Voltage measurement with a Generic Multimeter

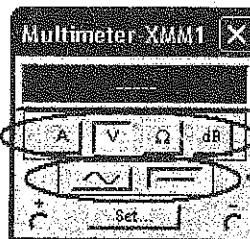


**Figure C-45** Generic Multimeter Quick Hint

#### Generic Multimeter Icon



Double clicking on the Multimeter brings up this display.



These buttons select Current, Voltage, Resistance, or Decibel measurement.

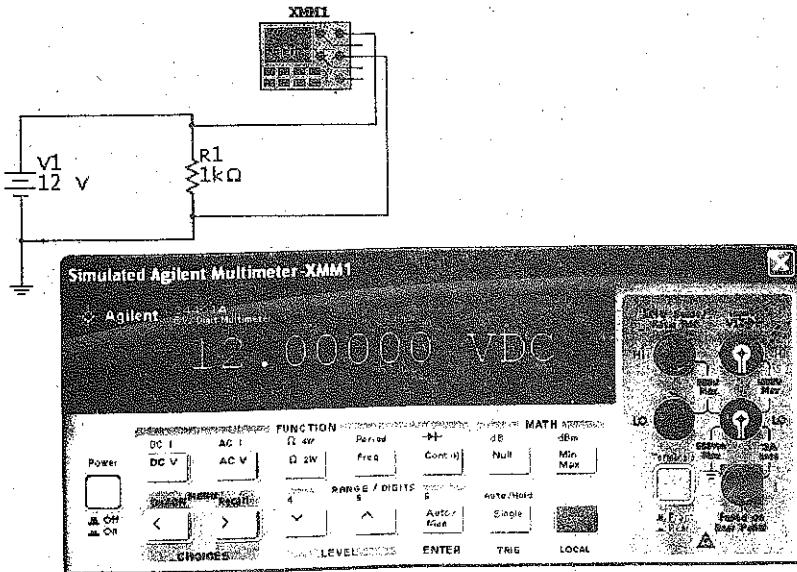
These two buttons select AC or DC measurement.

Simply mouse click on the appropriate buttons to set up the multimeter for the type of measurement you wish to make.

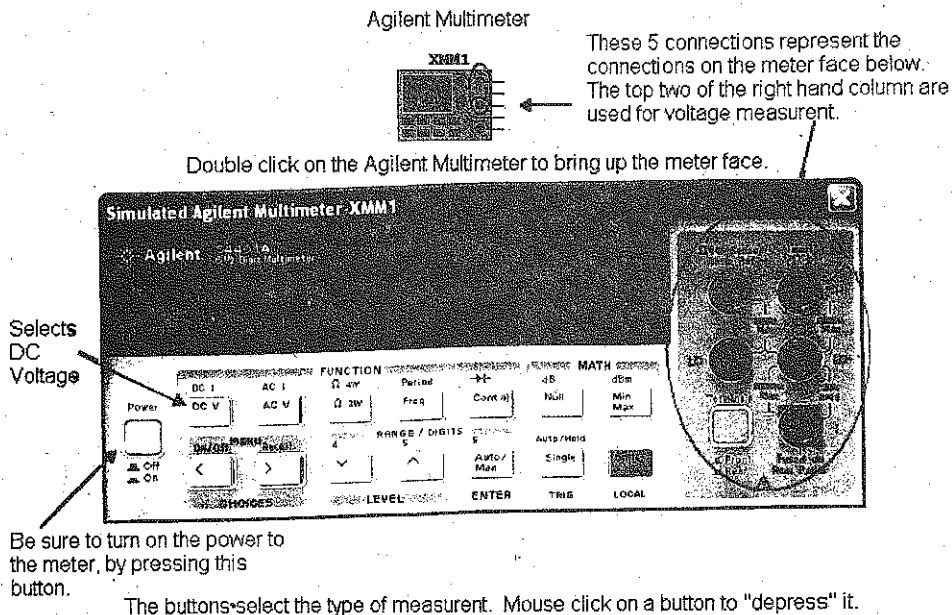
#### Example 3 Voltage Measurement Using an Agilent Multimeter in a Series DC Circuit

In Figure C-46, an Agilent Multimeter is placed in parallel with the resistor to measure the voltage across it. Be sure to double click the Agilent Multimeter icon to bring up the meter display. Press the appropriate buttons for "Voltage" and then "DC" or "AC" measurement. All circuits must have a ground. Note the two white circles and black x's on the right side of the display to indicate a connection to the meter. Note: This instrument requires that its power button be pressed to "turn on" the meter. Figure C-47 contains a *Quick Hint* on the use of the Agilent Multimeter.

**Figure C-46** DC Voltage measurement with an Agilent Multimeter



**Figure C-47** Agilent Multimeter Quick Hint



#### Example 4 Current Measurement Using an Ammeter in a Series DC Circuit

In Figure C-48, an ammeter is placed in series with the resistor and DC source to measure the current flowing through the circuit. The default is set for "DC" measurement. If AC is required, double click on the meter to bring up the configuration screen. All circuits must have a ground. Figure C-49 contains a *Quick Hint* on the use of the ammeter.

Figure C-48 DC Current measurement with an Ammeter

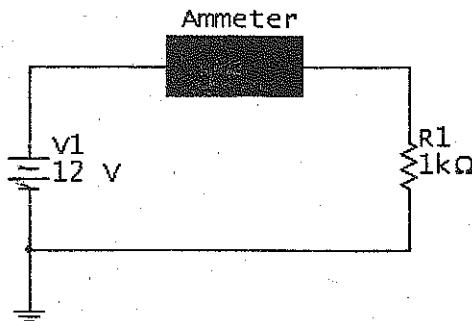
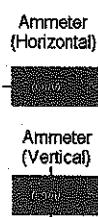
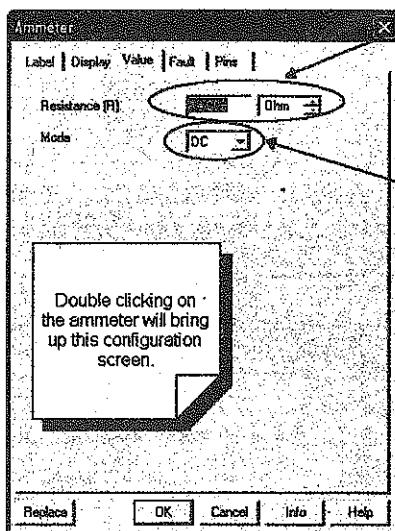


Figure C-49 Ammeter Quick Hint



The ammeter will measure the amount of current flowing through it. The meter will display the appropriate prefix, if needed. (m = milli, n = nano, p = pico)

The ammeter is placed in series.



### Example 5 Current Measurement Using a Generic Multimeter in a Series DC Circuit

In Figure C-50, a Generic Multimeter is placed in series with the resistor and DC source to measure the current flowing through the circuit. Be sure to double click the generic Multimeter icon to bring up the meter display. The current function is selected by clicking on the "A" on the meter display. Since the source is DC, the DC function of the meter is also selected, as indicated by the depressed button. All circuits must have a ground. Figure C-51 contains a *Quick Hint* on the use of the Generic Multimeter.

Figure C-50 DC Current measurement with a Generic Multimeter

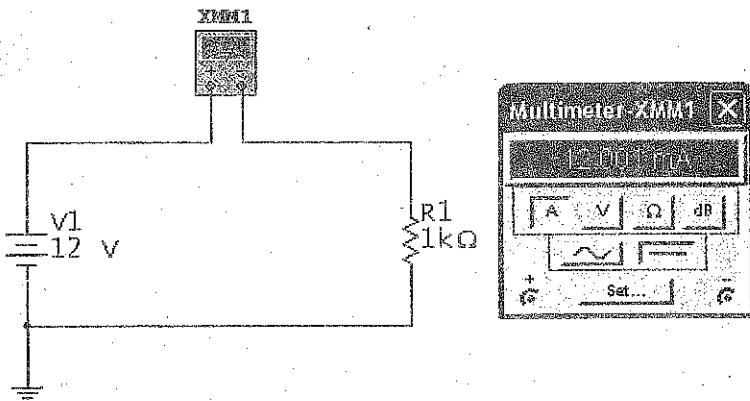
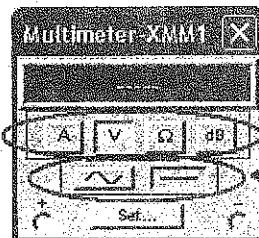


Figure C-51 Generic Multimeter Quick Hint

#### Generic Multimeter Icon



Double clicking on the Multimeter brings up this display.



These buttons select Current, Voltage, Resistance, or Decibel measurement.

These two buttons select AC or DC measurement.

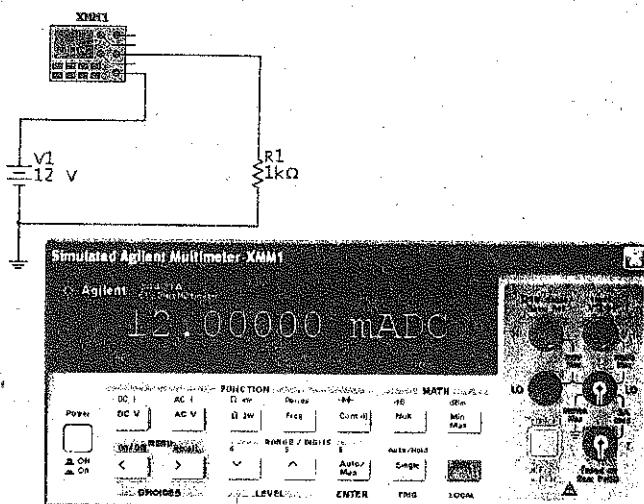
Simply mouse click on the appropriate buttons to set up the multimeter for the type of measurement you wish to make.

### Example 6 Current Measurement Using an Agilent Multimeter in a Series DC Circuit

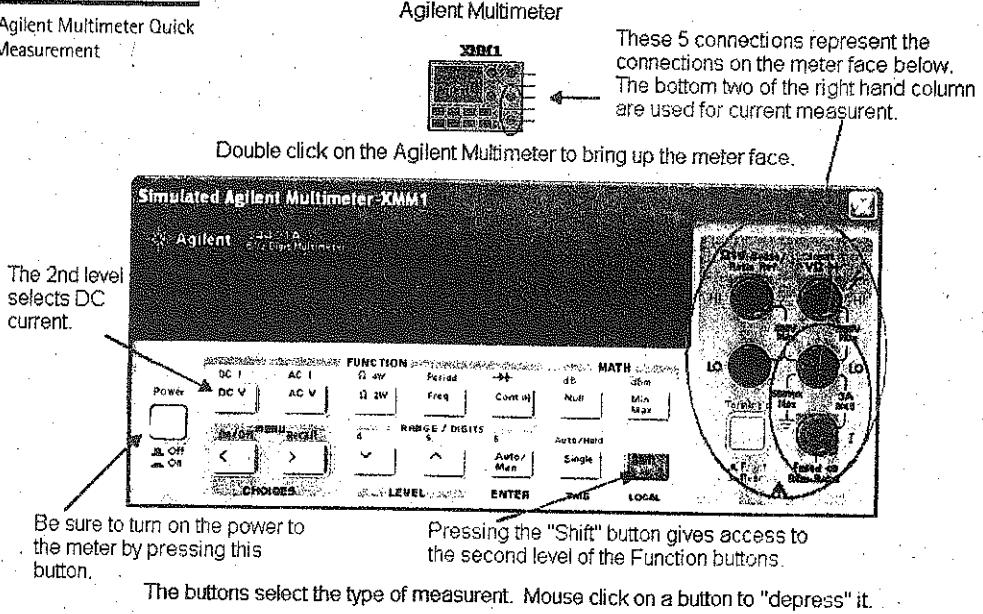
In Figure C-52, an Agilent Multimeter is placed in series with the resistor and source to measure the current flowing through the circuit. Be sure to double click the Agilent Multimeter icon to bring up the meter display. Selection of DC current measurement is the second function of the DC voltage measurement button. Be sure to press the "shift" button to access the second function of the voltage button. Note the two white circles and black x's on the right side of the display to indicate a connection to the meter. All circuits must have a ground.

This instrument requires that its power button be pressed to "turn on" the meter. Figure C-53 contains a *Quick Hint* on the use of the Agilent Multimeter for current measurement.

**Figure C-52** DC Current measurement with an Agilent Multimeter



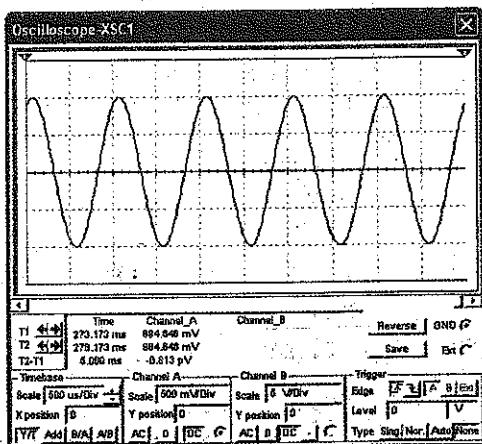
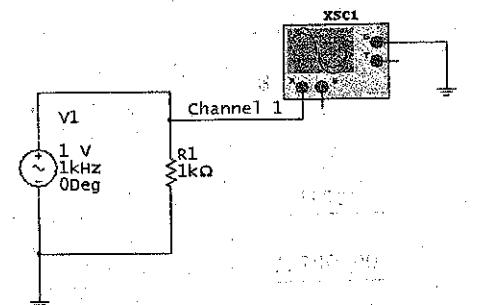
**Figure C-53** Agilent Multimeter Quick Hint for Current Measurement



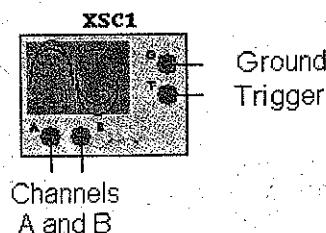
### Example 7 Voltage Measurement Using a Generic Oscilloscope in a Series AC Circuit

In Figure C-54, channel 1 of the Generic oscilloscope is connected to the positive side of the resistor. The ground connection of the scope and the circuit must be grounded. The oscilloscope will use this ground as a reference point. This Generic oscilloscope's operation follows that of an actual oscilloscope. The settings can be changed by clicking in each box and bringing up the scroll arrows. Adjust the volts per division on the channel under measurement until the amplitude of the waveform fills the majority of the screen. Adjust the Time-base such that a complete cycle or two are displayed. Figures C-55, C-56 and C-57 contain *Quick Hint* on the use of the Generic oscilloscopé.

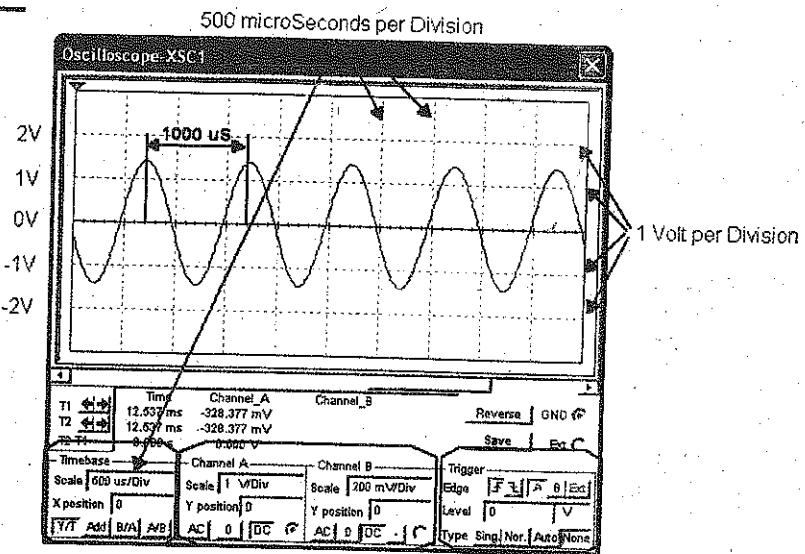
**Figure C-54** Voltage Measurement with a Generic Oscilloscope



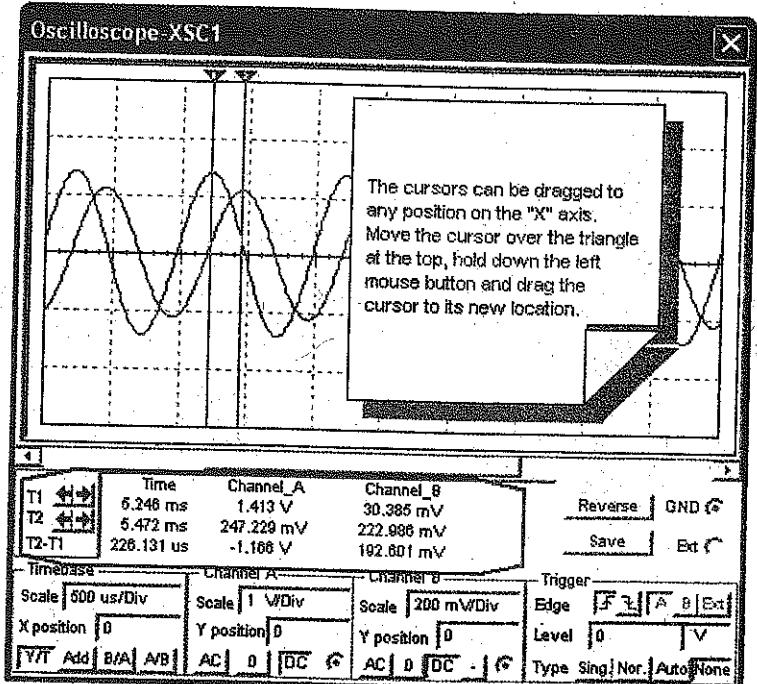
**Figure C-55** Generic Oscilloscope Icon Quick Hint



**Figure C-56** Generic Oscilloscope  
Quick Hint



**Figure C-57** Generic Oscilloscope  
Quick Hint



Time Channel\_A Channel\_B  
6.246 ms 1.413 V 30.385 mV  
5.472 ms 247.220 mV 222.986 mV  
226.131 us -1.166 V 192.801 mV

### Example 8 Voltage Measurement Using the Agilent Oscilloscope in a Series AC Circuit

In Figure C-58, channel 1 of the Agilent oscilloscope is connected to the positive side of the resistor. The ground connection of the scope and the circuit must be grounded. The oscilloscope will use this ground as a reference point. This Agilent oscilloscope's operation follows that of a 2-channel, +16 logic channel, 100-MHz bandwidth Agilent Model 54622D Oscilloscope. The oscilloscope display as shown in Figure C-59, is brought up by mouse clicking on the oscilloscope icon.

Figure C-58 Voltage Measurement with an Agilent Oscilloscope

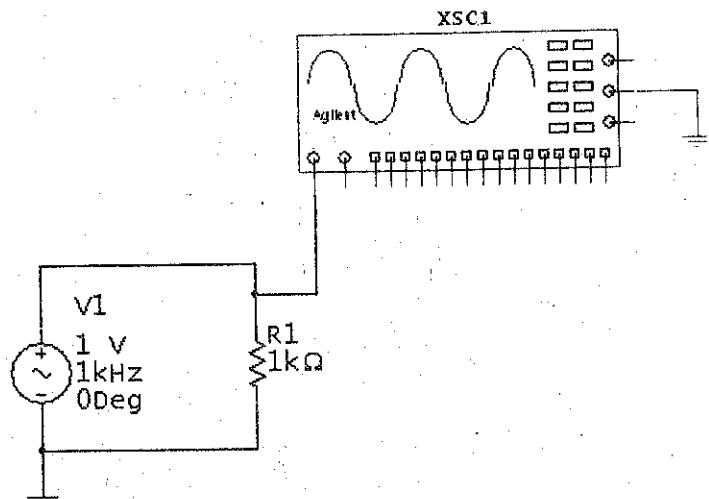
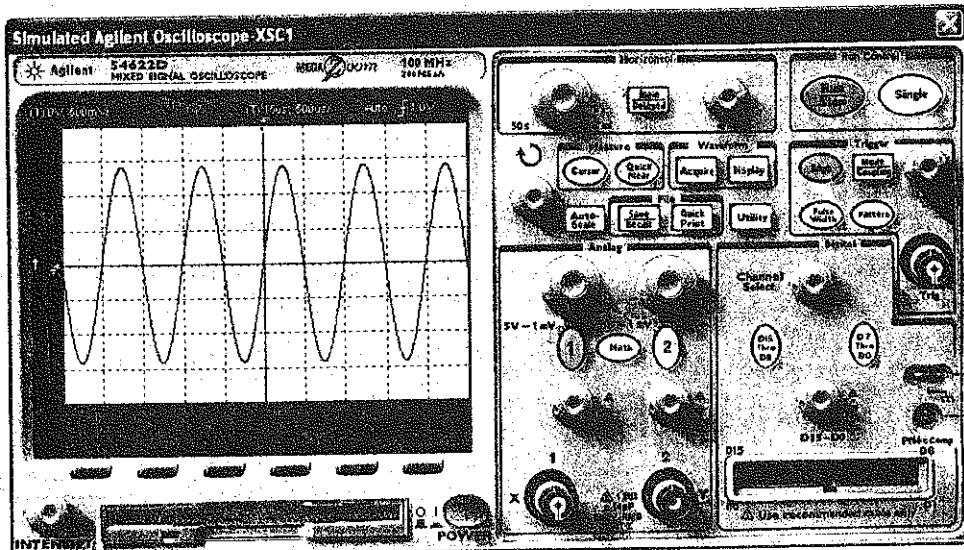
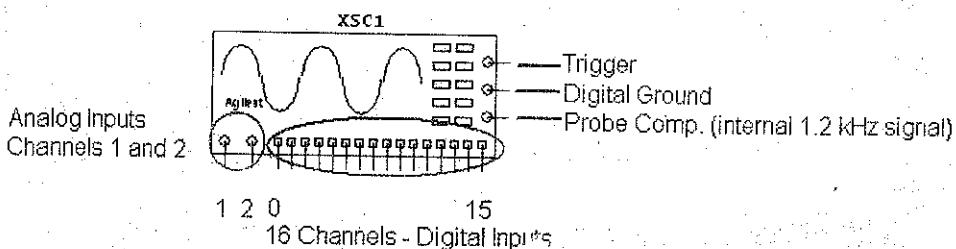


Figure C-59 Agilent Oscilloscope Display



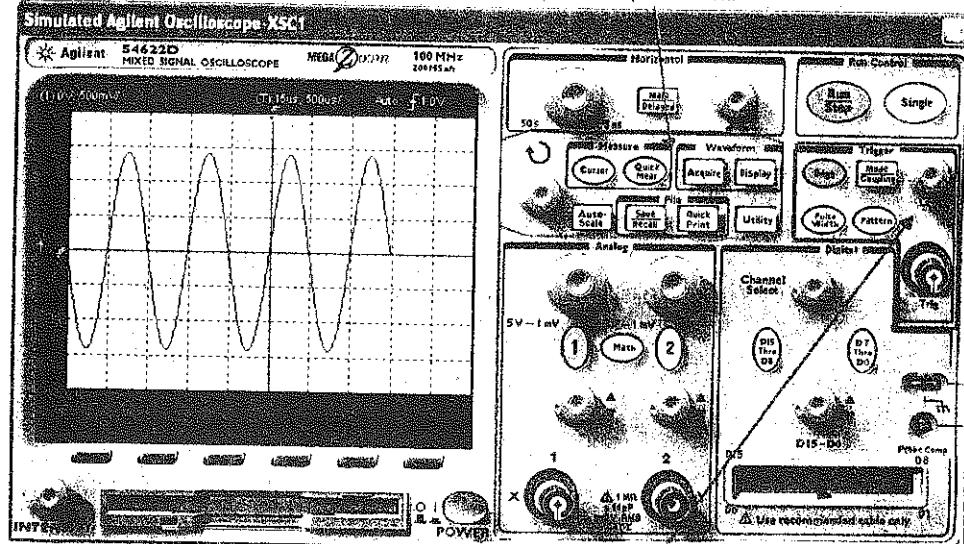
The settings can be changed by placing the mouse over the dials and spinning the mouse wheel or by "pressing" the buttons with a mouse click. Adjust the volts per division on the channel under measurement until the amplitude of the waveform fills the majority of the screen. Adjust the Time-base in the Horizontal section such that a complete cycle or two are displayed. This instrument requires that its power button be pressed to "turn on" the oscilloscope. Figures C-60, C-61, and C-62 contain *Quick Hints* on the use of the Agilent oscilloscope.

**Figure C-60** Agilent Oscilloscope Icon Quick Hint



**Figure C-61** Agilent Oscilloscope Quick Hint

The Horizontal section controls the units for the "X" axis. The "X" axis represents time and the units are seconds per division.

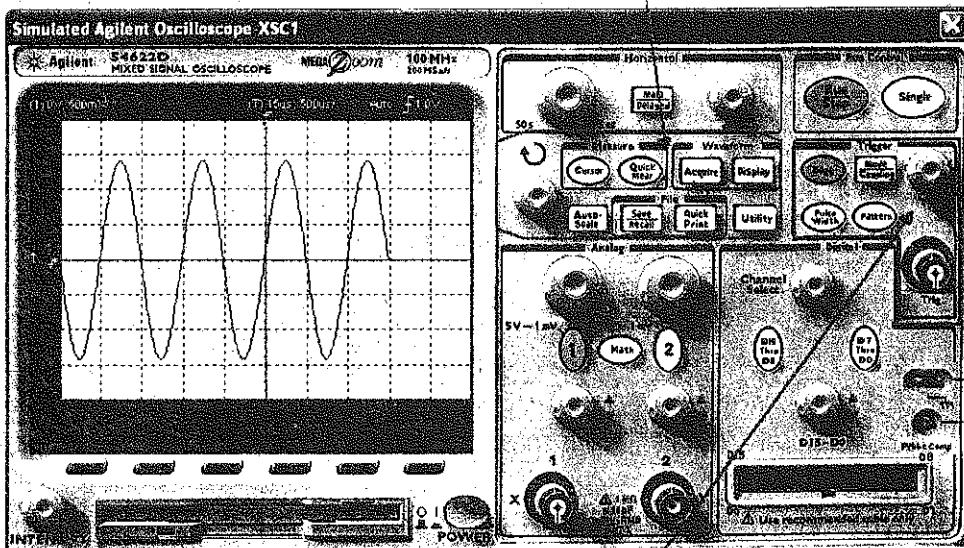


Channel "1" and "2" control the units for the "Y" axis. The "Y" axis represents Voltage and the units are Volts per division.

16 Channel Digital Logic Input

**Figure C-62** Agilent Oscilloscope Quick Hint

The Measure section includes cursor operation.  
The Waveform section allows for waveform storage.  
The File section saves, recalls, and prints.

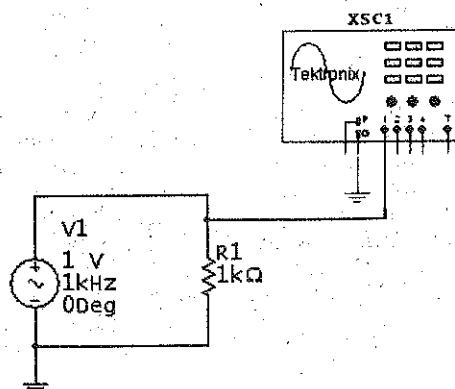


The Trigger controls when the oscilloscope starts to display the waveform. It can display it on the rising edge or the falling edge. The voltage level at which the oscilloscope is triggered is also selected here.

### Example 9 Frequency and Voltage Measurement Using the Tektronix Oscilloscope in a Series AC Circuit

In Figure C-63, channel 1 of the Tektronix oscilloscope is connected to the positive side of the resistor. The ground connection of the scope and the circuit must be grounded. The oscilloscope will use this ground as a reference point. The Tektronix oscilloscope has all of the functionality of the Model TDS2024 four channel Digital Storage oscilloscope. The oscilloscope display is brought up by mouse

**Figure C-63** Voltage and Frequency measurement with a Tektronix Oscilloscope



clicking on the oscilloscope icon. The settings can be changed by placing the mouse over the dials and spinning the mouse wheel or by "pressing" the buttons with a mouse click. Adjust the volts per division on the channel under measurement until the amplitude of the waveform fills the majority of the screen. Adjust the Time-base in the Horizontal section such that a complete cycle or two of the waveform is displayed. This instrument requires that its power button be pressed to "turn on" the oscilloscope. The voltage and frequency can be measured by the user or by using the "Measure" function of the oscilloscope.

Using volts per division and the seconds per division settings, the amplitude and frequency of the waveform in Figure C-64 can be determined. The amplitude of the waveform is two divisions above zero volts. (The yellow arrow points to the zero reference point.) The volts per division setting are set to 500 mV per division.

$$V_P = 2 \text{ divisions} \times \frac{500 \text{ mV}}{\text{division}}$$

$$V_P = 1 \text{ V}$$

$$V_{PP} = 4 \text{ divisions} \times \frac{500 \text{ mV}}{\text{division}}$$

$$V_{PP} = 2 \text{ V}$$

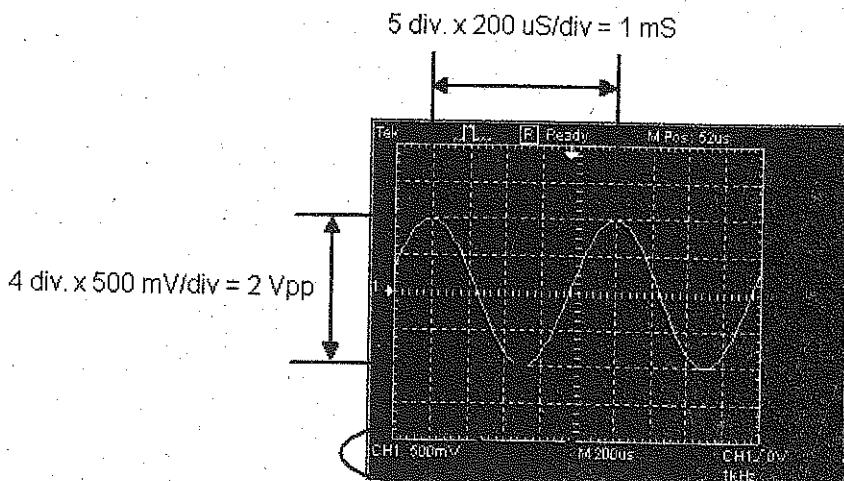
The period of the waveform is measured to be 1 mS. Since frequency is the reciprocal of the period, the frequency can be calculated.

$$F = \frac{1}{T}$$

$$F = \frac{1}{1 \text{ mS}}$$

$$F = 1 \text{ kHz}$$

**Figure C-64** Measurement of the Period of the Waveform



The oscilloscope displays the volts per division for each channel.

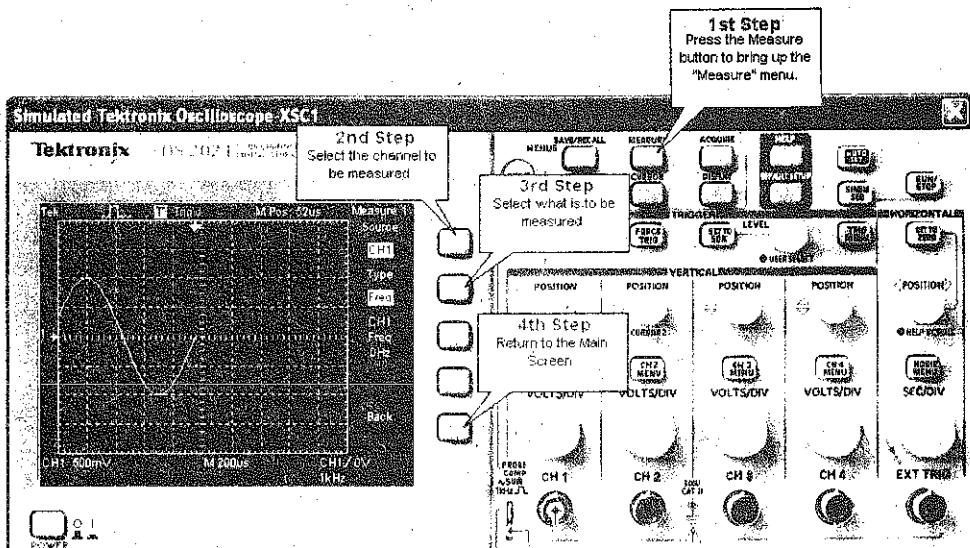
The oscilloscope displays the Time-base in seconds per division and calculates the frequency.

The Tektronix oscilloscope can also perform the voltage and frequency measurements automatically through the use of the "Measure" function. The four steps and the resulting display are shown in Figures C-65 and C-66. To set up the oscilloscope to measure these values automatically:

1. Press the Measure button.
2. Select the channel to be measured.
3. Select what is to be measured: Vpp, Frequency, etc.
4. Return to the Main Screen.
5. Repeat for other channels and or values.

Figures C-67, C-68 and C-69 contain *Quick Hint* on the use of the Tektronix oscilloscope.

**Figure C-65** Tektronix Oscilloscope Measurement Function Set-up



**Figure C-66** Tektronix Oscilloscope Measurement Display

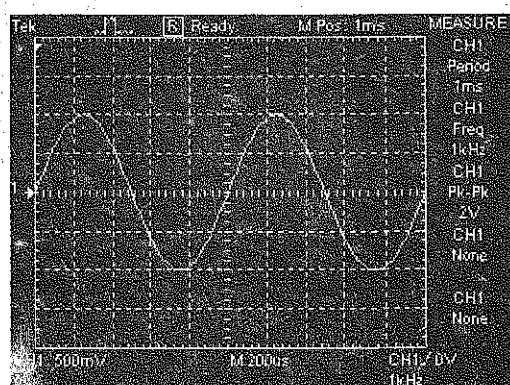


Figure C-67 Tektronix Oscilloscope Icon Quick Hint

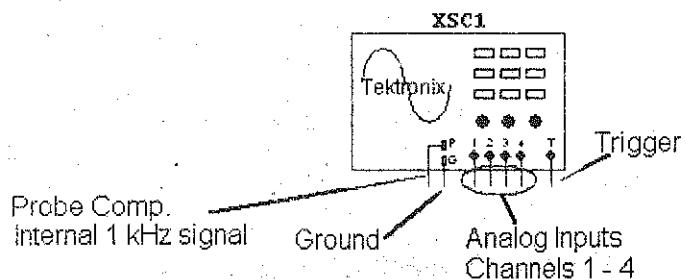
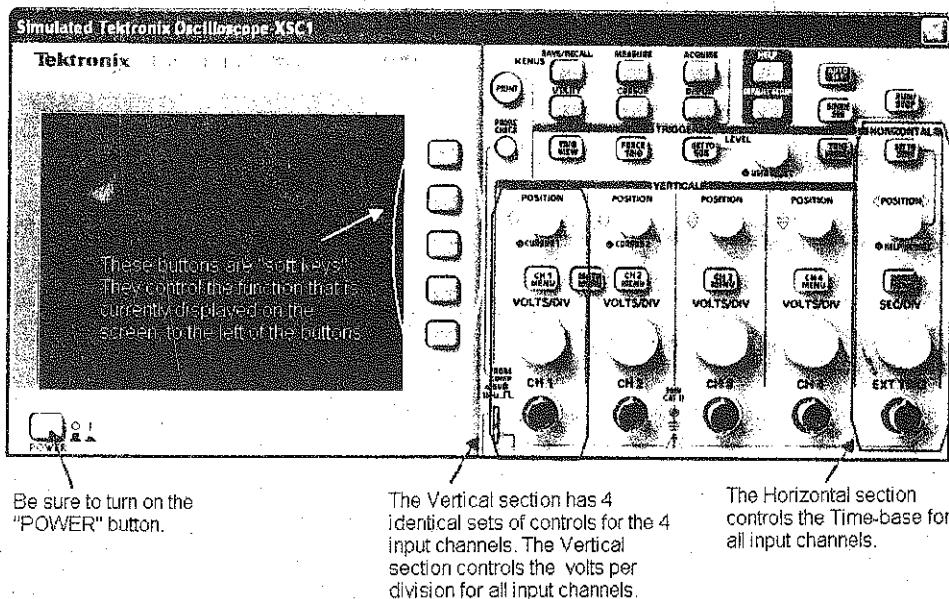
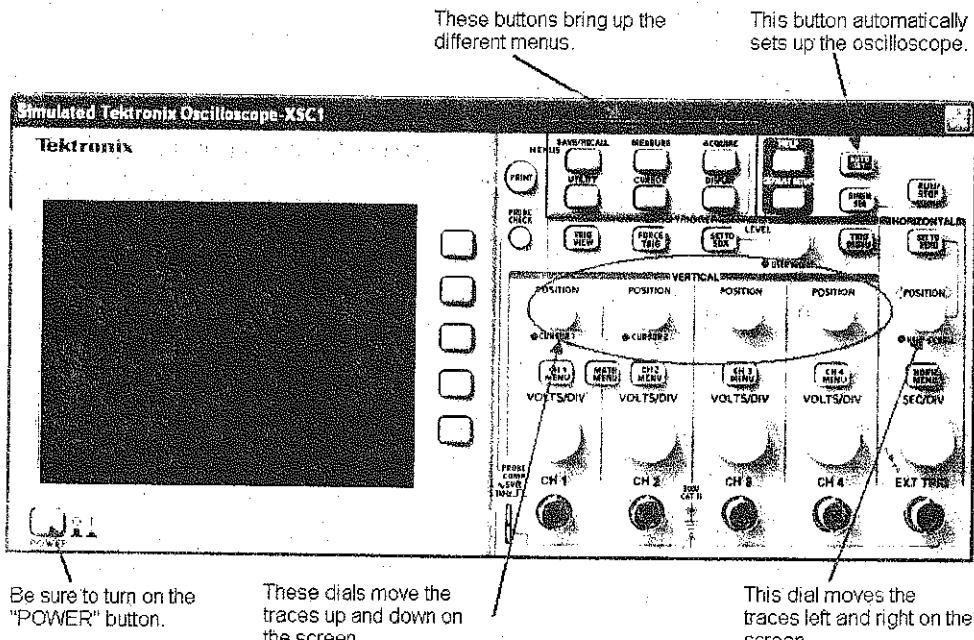


Figure C-68 Tektronix Oscilloscope Quick Hint

**Hint:** The buttons are "pressed" by a mouse click. The dials can be turned by dragging them with the cursor or by placing the cursor over the dials and spinning the mouse wheel.



**Figure C-69** Tektronix Oscilloscope Quick Hint



## Conclusion

The ability to create a schematic quickly and then analyze the circuit through simulation makes MultiSim a wonderful tool to help students understand the concepts covered in the study of DC, AC, and semiconductor electronics.

This primer introduced the reader to the features of MultiSim that directly relate to the topics covered in this textbook. The features covered in this appendix will help the student to utilize the compact disk included with this textbook to its fullest extent.

# Appendix D

## Thevenizing the R/2R D/A Converter

With the switches  $D_0 - D_4$  connected as in Fig. D-1a the binary input is  $D_0 = 1$ ,  $D_1 = 0$ ,  $D_2 = 0$ , and  $D_3 = 0$ . First, Thevenize the circuit from point A, looking toward  $D_0$ . When doing so,  $R_5$  ( $20\text{ k}\Omega$ ) becomes in parallel with  $R_1$  ( $20\text{ k}\Omega$ ) and the equivalent equals  $10\text{ k}\Omega$ . The Thevenized voltage at point A is one-half of  $V_{ref}$  and is equal to  $+2.5\text{ V}$ . This equivalent is shown in Fig. D-1b.

Next, Thevenize Fig. D-1b from point B. Notice how  $R_{TH}$  ( $10\text{ k}\Omega$ ) is in series with  $R_6$  ( $10\text{ k}\Omega$ ). This  $20\text{ k}\Omega$  value is in parallel with  $R_2$  ( $20\text{ k}\Omega$ ) and again gives us  $10\text{ k}\Omega$ . The Thevenized voltage seen from point B is again reduced by half to  $1.25\text{ V}$ . This equivalent is shown in Fig. D-1c.

Now, Thevenize Fig. D-1c from point C. Again,  $R_{TH}$  ( $10\text{ k}\Omega$ ) is in series with  $R_7$  ( $10\text{ k}\Omega$ ) and this  $20\text{ k}\Omega$  value becomes in parallel with  $R_3$  ( $20\text{ k}\Omega$ ).  $V_{TH}$  is equal to  $0.625\text{ V}$ . Notice how the  $V_{TH}$  values have been cut in half at each step. The Thevenin equivalent has been reduced to that of Fig. D-1d.

In Fig. D-1d, the op amp's inverting input and the top of  $R_4$  ( $20\text{ k}\Omega$ ) is at a virtual ground. The voltage is equal to zero volts at this point. This places the entire  $0.625\text{ V}$  of  $V_{TH}$  across  $R_{TH}$  and  $R_8$  ( $10\text{ k}\Omega$ ). This results in an input current  $I_{in}$  of:

$$I_{in} = \frac{0.625\text{ V}}{20\text{ k}\Omega} = 31.25\text{ }\mu\text{A}$$

Again, because of the virtual ground, this input current is forced to flow through  $R_f$  ( $20\text{ k}\Omega$ ) and produces an output voltage of:

$$V_{out} = -(I_{in} R_f) = -(31.25\text{ }\mu\text{A})(20\text{ k}\Omega) = -0.625\text{ V}$$

This output voltage is the smallest output increment above  $0\text{ V}$  and is referred to as the circuit's output resolution.

Figure D-1 (a) Original circuit; (b) Thevenized at point A; (c) Thevenized at point B; (d) Thevenized at point C.

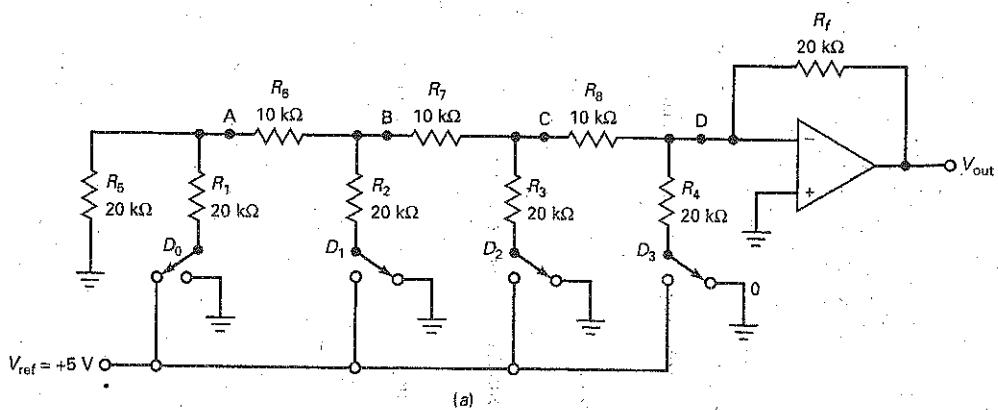
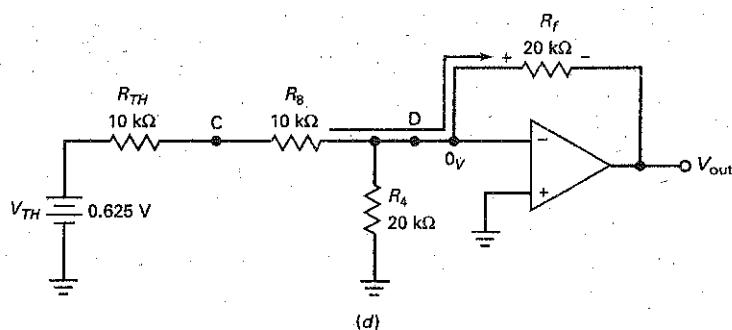
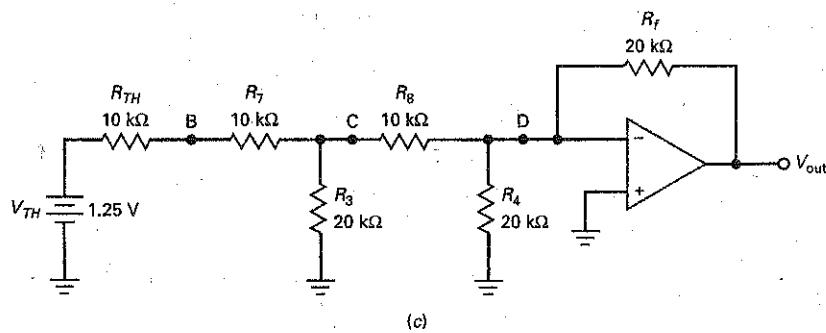
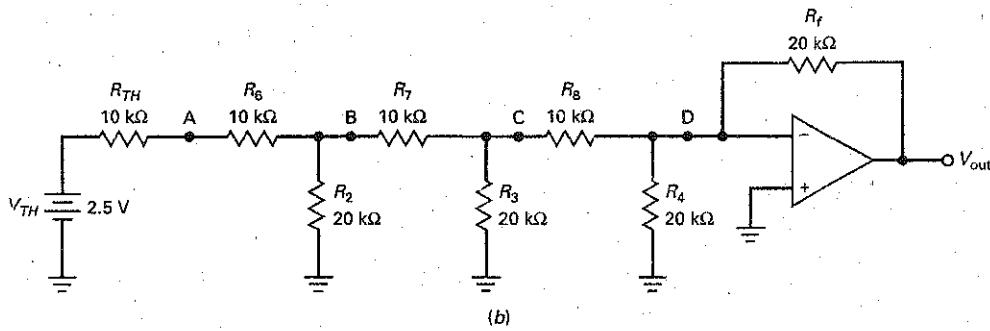


Figure D-1 (continued)



# Appendix E

## Summary Table Listing

- 1-1 Thevenin and Norton Values
- 2-1 Diode Bias
- 3-1 Diode Approximations
- 4-1 Unfiltered Rectifiers
- 4-2 Capacitor-Input Filtered Rectifiers
- 4-3 Power Supply Block Diagram
- 4-4 Typical Troubles for Capacitor-Input Filtered Bridge Rectifiers
- 6-1 Transistor Circuit Approximations
- 7-1 Base Bias vs. Emitter Bias
- 8-1 Main Bias Circuits (BJTs)
- 9-1 VDB AC and DC Equivalents
- 11-1 Common Amplifier Configurations
- 12-1 Amplifier Classes
- 13-1 JFET Biasing
- 13-2 JFET Amplifiers
- 13-3 FET Applications
- 14-1 MOSFET Amplifiers
- 16-1 Amplifier Frequency Analysis
- 18-1 Basic Op Amp Configurations
- 19-1 Four Types of Negative Feedback
- 21-1 Filter Approximations
- 21-2 Basic Filter Circuits
- 23-1 Oscillators
- 24-1 Voltage Regulators

# Glossary

## A

**absolute value** The value of an expression without regard for its sign. Sometimes called the *magnitude*. Given +5 and -5, the absolute value is 5.

**acceptor** A trivalent atom, one that has three valence electrons. Each trivalent atom produces one hole in a silicon crystal.

**ac collector resistance** The total ac load resistance found at the circuit's collector. This is often the parallel combination of  $R_C$  and  $R_L$ . This value is important when determining the voltage gain of a common-base or common-emitter amplifier.

**ac compliance** A large-signal amplifier with its  $Q$  point at the middle of the ac load line allowing a maximum peak-to-peak unclipped output.

**ac current gain** With a transistor, the ratio of ac collector current to ac base current.

**ac cutoff** The lower end of the ac load line. At this point, the transistor goes into cutoff and clips the ac signal.

**ac emitter feedback** The ac signal developed across an unbypassed emitter resistance  $r'_E$ .

**ac emitter resistance** The ac base-emitter voltage divided by the ac emitter current. This value is normally listed as  $r'_E$  and can be calculated by  $r'_E = \frac{25 \text{ mV}}{I_E}$ . This value is important when determining the input impedance and gain of a JFET amplifier.

**ac equivalent circuit** All that remains when you reduce the dc sources to zero and short all capacitors.

**ac ground** A node that is bypassed to ground through a capacitor. Such a node will show no ac voltage when it is probed by an oscilloscope, but it will indicate a dc voltage when it is measured with a voltmeter.

**ac load line** The locus of instantaneous operating points when an ac signal is driving the transistor. This load line is different from the dc load line whenever the ac load resistance is different from the dc load resistance.

**ac resistance** The resistance of a device to a small ac signal. The ratio of a voltage change to a current change. The key idea here is changes about an operating point.

**ac saturation** The upper end of the ac load line. At this point, the transistor goes into saturation and clips the ac signal.

**ac short** A coupling capacitor or bypass capacitor can be treated as an ac short if its

capacitive reactance  $X_C$  is less than 1/10 of the resistance  $R$ . This can be stated mathematically as  $X_C < 0.1R$ .

**active current gain** The current gain in the active region of a transistor. That is what you usually find on a data sheet and what most people mean when they talk about current gain. (See *saturated current gain*.)

**active filter** In the good old days, filters were made out of passive components like inductors and capacitors. Some filters are still made this way. The problem is that at low frequencies, inductors become very large in passive filter designs. Op amps give another way to build filters and eliminate the problem of bulky inductors at low frequencies. Any filter using an op amp is called an active filter.

**active half-wave rectifier** An op amp circuit with the ability to rectify signals with input voltages less than 0.7 V. This circuit makes use of the very large open-loop gain of an op amp and is also known as a precision rectifier.

**active loading** This refers to using a bipolar or MOS transistor as a resistor. It's done to save space or to get resistances that are difficult with passive resistors.

**active-load resistor** A FET with its gate connected to the drain. The resulting two-terminal device is equivalent to a resistor.

**active peak detector** An op amp circuit used to detect low-level signals.

**active positive clumper** An op amp circuit used to add a positive dc component to an input signal.

**active positive clipper** An adjustable op amp circuit used to precisely control the level of positive output voltage.

**active region** Sometimes called the *linear region*. It refers to that part of the collector curve that is approximately horizontal. A transistor operates in the active region when it is used as an amplifier. In the active region, the emitter diode is forward-biased, the collector diode is reverse-biased, the collector current almost equals the emitter current, and the base current is much smaller than either the emitter or collector current.

**all-pass filter** A specialized filter having the ideal ability to pass all frequencies between zero and infinity. This filter is also called a *phase filter* because of its ability to shift the phase of the output signal without changing the magnitude.

**ambient temperature** The temperature of the immediate surrounding air around a device.

**amplifier** A circuit that can increase the peak-to-peak voltage, current, or power of a signal.

**amplitude** The size of a signal, usually its peak value.

**analog** The branch of electronics dealing with infinitely varying quantities. Often referred to as *linear electronics*.

**analogy** A likeness in some ways between dissimilar things that are otherwise unlike. The analogy between bipolar transistors and JFETs is an example. Because the devices are similar, many of the equations for them are identical except for a change of subscripts.

**anode** The element of an electronic device that receives the flow of electron current.

**approximation** A way to retain your sanity with semiconductor devices. Exact answers are tedious and time-consuming and almost never justified in the real world of electronics. On the other hand, approximations give us quick answers, usually adequate for the job at hand.

**Armstrong oscillator** A circuit distinguished by its use of transformer coupling for the feedback signal.

**astable** A digital switching circuit with no stable states. This circuit is also referred to as a *free-running circuit*.

**attenuation** A reduction in signal intensity, normally expressed in decibels. The signal reduction value is compared to the signal level at the midband of the filter.

Mathematically, it is expressed as  

$$\text{attenuation} = \frac{V_{\text{out}}}{V_{\text{out(mid)}}}$$
 and decibel

attenuation =  $20 \log \text{attenuation}$ .

**audio amplifier** Any amplifier designed for the audio range of frequencies, 20 Hz to 20 kHz.

**automatic gain control (AGC)** A circuit designed to correct the gain of an amplifier according to the amplitude of the incoming signal.

**avalanche effect** A phenomenon that occurs for large reverse voltages across a *pn* junction. The free electrons are accelerated to such high speeds that they can dislodge valence electrons. When this happens, the valence electrons become free electrons that dislodge other valence electrons.

**averager** An op amp circuit constructed to provide an output voltage equal to the average of all input voltages.

## B

**back diode** A diode with properties that enable it to conduct better in the reverse direction than in the forward direction. Commonly used in the rectification of weak signals.

**bandpass filter** A filter capable of passing a range of input frequencies with minimum attenuation while blocking all frequencies below and above the lower and upper cutoff frequencies  $f_1$  and  $f_2$ .

**bandstop filter** A filter capable of rejecting a range of input frequencies while effectively passing all frequencies below and above the cutoff frequencies  $f_1$  and  $f_2$ . This filter is also referred to as a notch filter.

**bandwidth** The difference between the two dominant critical frequencies of an amplifier. If the amplifier has no lower critical frequency, the bandwidth equals the upper critical frequency.

**barrier potential** The voltage across the depletion layer. This voltage is built into the *pn* junction because it is the difference of potential between the ions on both sides of the junction. It equals approximately 0.7 V for a silicon diode.

**base** The middle part of a transistor. It is thin and lightly doped. This permits electrons from the emitter to pass through it to the collector.

**base bias** The worst way to bias a transistor for use in the active region. This type of bias sets up a fixed value of base current.

**Bessel filter** Filter providing the desired frequency response but with a constant time delay in the passband.

**BJFET op amp** An IC op amp that combines FETs and bipolar transistors, usually with FET source followers at the front end of the device, followed by bipolar stages of gain.

**bipolar junction transistor (BJT)** A transistor where both free electrons and holes are necessary for normal operation.

**biquadratic filter** An active filter, also known as a *TT (Tow-Thomas) filter*, with the ability to independently tune its voltage gain, center frequency, and bandwidth using separate resistors.

**Bode plot** A graph showing the gain or phase performance of an electronic circuit at various frequencies.

**boost regulator** The basic topology for a switching regulator circuit in which the output voltage is higher than the input voltage.

**bootstrapping** A "following" function in which the inverting input voltage immediately increases or decreases the same amount as the noninverting input voltage initiates.

**breakdown region** For a diode or transistor, it is the region where either avalanche or the zener effect occurs. With the exception of the zener diode, operation in the breakdown region is to be avoided under all circumstances because it usually destroys the device.

**breakdown voltage** The maximum reverse voltage a diode can withstand before avalanche or the zener effect occurs.

**breakover** When a transistor breaks down, the voltage across it remains high. But with a thyristor, breakdown turns into saturation. In other words, breakover refers to the way a thyristor breaks down and then immediately goes into saturation.

**bridge rectifier** The most common type of rectifier circuit. It has four diodes, two of which are conducting at the same time. For a given transformer, it produces the largest dc output voltage with the smallest ripple.

**buck-boost regulator** The basic topology for a switching regulator circuit in which a positive input voltage produces a negative output voltage.

**buck regulator** The basic topology for a switching regulator circuit in which the output voltage is lower than the input voltage.

**buffer** A unity gain amplifier (voltage follower) having a high input impedance and a low output impedance used primarily to provide isolation between two parts of a circuit.

**buffer amplifier** This is an amplifier that you use to isolate two other circuits when one is overloading the other. A buffer amplifier usually has a very high input impedance, a very low output impedance, and a voltage gain of 1. These qualities mean that the buffer amplifier will transmit the output of the first circuit to the second circuit without changing the signal.

**bulk resistance** The ohmic resistance of the semiconductor material.

**Butterworth filter** This is a filter designed to produce as flat a response as possible up to the cutoff frequency. In other words, the output voltage remains constant almost all the way to the cutoff frequency. Then it decreases at  $20n$  dB per decade, where  $n$  is the number of poles in the filter.

**bypass capacitor** A capacitor used to ground a node.

## C

**capacitive coupling** The use of a capacitor to pass the ac signal from one stage to another while blocking the dc component of the waveform.

**capacitor input filter** Nothing more than a capacitor across the load resistor. This type of passive filter is the most common.

**capture range** The range of input frequencies in which a phase-locked-loop (PLL) circuit can lock on to the input signal.

**carrier** The high-frequency output signal of a transmitter that is caused to vary in amplitude, frequency, or phase by a modulating signal.

**cascaded stages** Connecting two or more stages so that the output of one stage is the input to the next.

**case temperature** This is the temperature of the transistor case or package. When you pick up a transistor, you are in contact with the

case. If the case is warm, you are feeling the case temperature.

**cathode** The element of an electronic device that provides the flow of electron current.

**CB amplifier** An amplifier configuration in which the input signal is fed into the emitter terminal and the output signal is taken from the collector terminal.

**CC amplifier** An amplifier configuration in which the input signal is fed into the base terminal and the output signal is taken from the emitter terminal. Also called *emitter follower*.

**CE amplifier** The most widely applied amplifier configuration, in which the input signal is fed into the base terminal and the output signal is taken from the collector circuit.

**channel** The *n*-type or *p*-type semiconductor material that provides the main current path between the source and drain of a field effect transistor.

**Chebyshev filter** A filter with extremely good selectivity. The attenuation rate is much higher than that of Butterworth filters. The main problem with this filter is the ripple in the passband.

**chip** This has two meanings. First, an IC manufacturer produces hundreds of circuits on a large wafer of semiconductor material. Then the wafer is cut into individual chips, each containing one monolithic circuit. In this case, no leads have been connected to the chip. The chip is still an isolated piece of semiconductor material. Second, after the chip has been put inside a package and external leads have been connected to it, you have a finished IC. This finished IC is also referred to as a *chip*. For instance, we can call a 741C a chip.

**chopper** A JFET circuit that uses either a shunt or a series switch to convert a dc input voltage to a square-wave output.

**clamper** A circuit for adding a dc component to an ac signal. Also known as a *dc restorer*.

**Clapp oscillator** A series-tuned Colpitts configuration noted for its good frequency stability.

**class A operation** This means the transistor is conducting throughout the ac cycle without going into saturation or cutoff.

**class AB operation** A power amplifier biased so that each transistor conducts slightly more than  $180^\circ$  of the input signal to reduce crossover distortion.

**class B operation** Biasing of a transistor in such a way that it conducts for only half of the ac cycle.

**class C operation** Biasing a transistor amplifier so that collector current flows for less than  $180^\circ$  of the ac input cycle.

**class-D amplifier** An amplifier configuration where the output transistors are driven to saturation and cutoff. The two-state output waveform varies its duty cycle based on an input signal level and is essentially pulse width modulated. This results in very low power dissipation by the output transistors and high efficiencies.

**clipper** A circuit that removes some part of a signal. Clipping may be undesirable in a linear amplifier or desirable in a circuit such as a limiter.

**closed-loop quantity** The value of any quantity such as the voltage gain, input impedance, and output impedance that is changed by negative feedback.

**closed-loop voltage gain** Designated as  $A_{V(CL)}$  or  $A_{CL}$ , this specification designates the voltage gain of an op amp with a feedback path between the output and input.

**CMOS inverter** A circuit with complementary MOS transistors. The input voltage is either low or high, and the output voltage is either high or low.

**cold-solder joint** A poor solder connection resulting from insufficient heat applied during the soldering process. The cold-solder joint may act as an intermittent connection or as no connection at all.

**collector** The largest part of a transistor. It is called the collector because it collects or gathers the carriers sent into the base by the emitter.

**collector cutoff current** The small collector current that exists when the base current is zero in a *CE* connection. Ideally, there should be no collector current. But there is because of the minority carriers and the surface leakage current of the collector diode.

**collector diode** The diode formed by the base and collector of a transistor.

**collector-feedback bias** An attempt to stabilize the *Q* point of a transistor circuit by connecting a resistor between the collector and base leads.

**Colepits oscillator** One of the most widely used *LC* oscillators. It consists of a bipolar transistor or FET and an *LC* resonant circuit. You can recognize it because it has two capacitors in the tank circuit. They act as a capacitive voltage divider that produces the feedback voltage.

**common-anode** A circuit configuration in a seven-segment indicator where each of the anodes are tied together and connected to a common positive dc supply.

**common base (CB)** An amplifier configuration in which the input signal is fed into the emitter terminal and the output signal is taken from the collector terminal.

**common-cathode** A circuit configuration in a seven-segment indicator where all of the cathodes are tied together and connected to a common negative dc supply.

**common-collector amplifier** This is an amplifier whose collector is at ac ground. The signal goes into the base and comes out of the emitter.

**common-emitter circuit** A transistor circuit where the emitter is common or grounded.

**common-mode rejection ratio (CMRR)** The ratio of differential gain to common-mode gain in an amplifier. It is a measure of the ability to reject a common-mode signal and is usually expressed in decibels.

**common-mode signal** A signal that is applied with equal strength to both inputs of a diff-amp or an op amp.

**common-source (CS) amplifier** A JFET amplifier in which the signal is coupled directly into the gate and all of the ac input voltage appears between the gate and the source, producing an amplified and inverted ac output voltage.

**comparator** A circuit or device that detects when the input voltage is greater than a predetermined limit. The output is either a low or a high voltage. The predetermined limit is called the *trip point*.

**compensating capacitor** A capacitor inside an op amp that prevents oscillations. Also, any capacitor that stabilizes an amplifier with a negative-feedback path. Without this capacitor, the amplifier will oscillate. The compensating capacitor produces a low critical frequency and decreases the voltage gain at a rate of 20 dB per decade above the midband. At the unity-gain frequency, the phase shift is in the vicinity of 270°. When the phase shift reaches 360°, the voltage gain is less than 1 and oscillations are impossible.

**compensating diodes** These are the diodes used in a class B push-pull emitter follower. These diodes have current-voltage curves that match those of the emitter diodes. Because of this, the diodes compensate for changes in temperature.

**complementary Darlington** A Darlington connection composed of *npn* and *pnp* transistors.

**complementary MOS (CMOS)** A method of reducing the current drain of a digital circuit by combining *n*-channel and *p*-channel MOSFETs.

**conduction angle** The angle or number of electrical degrees between the start and end of conduction for a thyristor with an ac waveform applied.

**conduction band** An energy band in a semiconductor in which electrons are free to move. This energy band is one level higher than the valence band.

**correction factor** A number used to describe how much one quantity differs from another. This value can be useful when comparing the emitter current to the collector current and determining the percent error that could result.

**coupling capacitor** A capacitor used to transmit an ac signal from one node to another.

**coupling circuit** A circuit that couples a signal from a generator to a load. The capacitor is in series with the Thevenin resistance of the generator and the load resistance.

**covalent bond** The shared electrons between the silicon atoms in a crystal represent covalent bonds because the adjacent silicon atoms pull on the shared electrons, just as two tug-of-war teams pull on a rope.

**critical frequency** Also known as the *cutoff frequency*, *break frequency*, *corner frequency*, etc. This is the frequency where the total

resistance of an *RC* circuit equals the total capacitive reactance.

**crossover distortion** The output distortion of a class B emitter follower amplifier resulting from biasing the transistors at cutoff. This distortion occurs during the period when one transistor cuts off and the other transistor comes on. This distortion can be reduced by biasing the transistors slightly above cutoff or class AB.

**crowbar** The metaphor used to describe the action of an SCR when it is used to protect a load against supply overvoltage.

**crystal** The geometric structure that occurs when silicon atoms combine. Each silicon atom has four neighbors, and this results in a special shape called a *crystal*.

**current amplifier** An amplifier configuration in which an input current produces a higher output current. An op amp ICIS circuit has the characteristics of a very low input impedance and high output impedance.

**current booster** A device, usually a transistor, that increases the maximum allowable load current of an op-amp circuit.

**current-controlled current source (ICIS)** A type of negative feedback amplifier in which the input current is amplified to get a larger output current, ideal because of stabilized current gain, zero input impedance, and infinite output impedance.

**current-controlled voltage source (ICVS)** Sometimes called a *transresistance amplifier*, this type of negative feedback amplifier has the input current controlling the output voltage.

**current drain** The total dc current  $I_{dc}$  supplied to an amplifier by the dc voltage source. This current is the combination of the biasing current and the collector current through the transistor.

**current feedback** This is a type of feedback where the feedback signal is proportional to the output current.

**current gain** Abbreviated as  $A_i$ , this value represents the ratio of output current divided by the input current.

**current limiting** Electronically reducing the supply voltage so that the current does not exceed a predetermined limit. This is necessary to protect the diodes and transistors, which usually blow out faster than the fuse under shorted-load conditions.

**current mirror** A circuit that acts as a current source whose value is a reflection of current through a biasing resistor and a diode.

**current-regulator diode** A special type of diode that holds the current constant through it with changing voltage applied.

**current-sensing resistor** A small resistor value, placed in series with a pass transistor, used to control the maximum output current of a series voltage regulator. This resistor develops a voltage drop proportional to the load current. If the load current becomes excessive, the voltage drop will turn on an active device that will limit the output current.

**current source** Ideally, this is an energy source that produces a constant current through a load resistance of any value. To a second approximation, it includes a very high resistance in parallel with the energy source.

**current-source bias** An FET biasing method using a bipolar junction transistor, configured as a constant current source, to control the drain current.

**current-to-voltage converter** A circuit that takes an input current value and develops a corresponding output voltage. In op amp circuits, this is also known as a transresistance amplifier or ICVS circuit.

**curve tracer** An electronic device for drawing characteristic curves on a cathode-ray tube.

**cutoff frequency** Identical to the critical frequency. The name *cutoff* is preferred when you are discussing filters because that's what most people use.

**cutoff point** Approximately the same as the lower end of the load line. The exact cutoff point occurs where base current equals zero. At this point, there is a small collector leakage current, which means the cutoff point is slightly above the lower end of the dc load line.

**cutoff region** The region where the base current is zero in a *CE* connection. In this region, the emitter and collector diodes are nonconducting. The only collector current is the very small current produced by minority carriers and surface leakage current.

## D

**damping factor** The ability of a filter to reduce resonant peaks at its output. The damping factor  $\alpha$  is inversely proportional to the circuit's  $Q$ .

**Darlington connection** The connection of two transistors producing an overall current gain equal to the product of the individual current gains. This transistor connection can have a very high input impedance and can produce large output currents.

**Darlington pair** Two transistors connected in a Darlington configuration. The pair can consist of individual transistors or a Darlington pair inside a single case.

**Darlington transistor** Two transistors connected to get a very high value of  $\beta$ . The emitter of the first transistor drives the base of the second transistor.

**dc alpha ( $\alpha_{dd}$ )** The dc collector current divided by the dc emitter current.

**dc amplifier** An amplifier that is capable of amplifying signals at very low frequencies, including dc. This amplifier is also known as a direct coupled amplifier.

**dc beta ( $\beta_{dd}$ )** The ratio of the dc collector current to the dc base current.

**dc equivalent circuit** What remains after you open all capacitors.

**dc return** This refers to a path for direct current. Many transistor circuits won't work unless a

dc path exists between all three terminals and ground. A diff amp and an op amp are examples of devices that must have dc return paths from their input pins to ground.

**dc-to-ac converter** A circuit having the ability to convert dc current, generally from a battery, into ac current. This circuitry is also known as an inverter and is the basis for an *uninterruptible power supply*.

**dc-to-dc converter** A circuit that converts dc voltage of one value to dc voltage at another value. Usually, the dc input voltage is chopped up or changed to a rectangular voltage. This is then stepped up or down as needed, rectified, and filtered to get the output dc voltage.

**dc value** The same as the average value. For a time-varying signal, the dc value equals the average value of all the points on the waveform. A dc voltmeter reads the average value of a time-varying voltage.

**decade** A factor of 10. Often used with frequency ratios of 10, as in a decade of frequency referring to a 10:1 change in frequency.

**decibel power gain** The ratio of output power to input power. Mathematically defined as

$$A_{P(dB)} = 10 \log \frac{P_{out}}{P_{in}}$$

**decibel voltage gain** This is a defined voltage gain given by 20 times the logarithm of the ordinary voltage gain.

**defining formula** A formula or an equation used to define or give the mathematical meaning of a new quantity. Before the defining formula is used for the first time, the quantity does not appear in any other formula.

**definition** A formula invented for a new concept based on scientific observation.

**delay equalizer** An all-pass active filter used to compensate for the time delay of another filter.

**depletion layer** The region at the junction of *p*- and *n*-type semiconductors. Because of diffusion, free electrons and holes recombine at the junction. This creates pairs of oppositely charged ions on each side of the junction. This region is depleted of free electrons and holes.

**depletion-mode MOSFET** A FET with an insulated gate that relies on the action of a depletion layer to control the drain current.

**derating factor** A value that tells you how much to reduce the power rating for each degree above the reference temperature given on the data sheet.

**derivation** A formula produced with mathematics from other formulas.

**derived formula** A formula or an equation that is a mathematical rearrangement of one or more existing equations.

**diac** A silicon bilateral device used to gate other devices such as triacs.

**diff amp** A two-transistor circuit whose ac output is an amplified version of the ac input signal between the two bases.

**differential input** The difference between the two input signals at the noninverting and inverting input terminals of a diff amp.

**differential input voltage** The desired input voltage of a differential amplifier as opposed to the common-mode input voltage.

**differential output** The output voltage value of a differential amplifier equaling the difference between the two collectors.

**differential voltage gain** The amount of amplification for the desired input signal of a differential amplifier as opposed to the common-mode input voltage.

**differentiator** An electronic circuit, either active or passive, whose output is proportional to the time rate of change of its input signal. This circuit has the ability to perform a calculus operation called differentiation.

**digital** A signal level that is found in two distinct states. Digital content is useful in the storage, processing, and transmission of information.

**digital-to-analog (D/A) converter** A circuit or device used to convert a digital signal into its two input terminals.

**diode** A *pn* crystal. A device that conducts easily when forward-biased and poorly when reverse-biased.

**direct coupling** Using a direct wire connection instead of a coupling capacitor between stages. For this to succeed, the designer has to make sure the dc voltages of the two points being connected are approximately equal before the direct connection is made.

**discrete circuit** A circuit whose components, such as resistors, transistors, etc., are soldered or otherwise connected mechanically.

**distortion** An undesirable change in the shape or phase of a waveform or signal. When this happens in an amplifier, the output waveform is not a true replica of the input waveform.

**dominant capacitors** The capacitors that are the main factors in determining a circuit's low- and high-frequency cutoff points.

**donor** A pentavalent atom, one that has five valence electrons. Each pentavalent atom produces one free electron in a silicon crystal.

**doping** Adding an impurity element to an intrinsic semiconductor to change its conductivity. Pentavalent or donor impurities increase the number of free electrons, and trivalent or acceptor impurities increase the number of holes.

**drain** The terminal of a field effect transistor that corresponds to the collector of a bipolar junction transistor.

**drain-feedback bias** An FET biasing method where a resistor is connected between the drain and gate leads of the transistor. An increase or decrease in drain current results in a corresponding decrease or increase in drain voltage. This voltage is feedback to the gate that stabilizes the transistor's *Q* point.

**driver stage** An amplifier designed to provide the proper input signal level to a power amplifier.

**dropout voltage** The minimum headroom voltage needed for proper regulation of an IC voltage regulator.

**duality principle** For any theorem in electrical circuit analysis, there is a dual (opposite) theorem in which one replaces the original quantities with dual quantities. This principle can be applied to Thevenin's and Norton's theorems.

**duty cycle** The width of a pulse divided by the period between pulses. Usually, you multiply by 100 percent to get the answer as a percentage.

## E

**Ebers-Moll model** An early ac model of a transistor also known as the *T model*.

**edge frequency** The highest frequency in the passband of a low-pass filter. Because it is on the edge of the passband, it is also referred to as the cutoff frequency. The attenuation value at the edge frequency can be specified to be less than 3 dB.

**efficiency** The ac load power divided by the dc power supplied to the circuit multiplied by 100 percent.

**electromagnetic interference (EMI)** A form of interference resulting from the radiation of high-frequency energy.

**elliptical approximation** An active filter with a very steep roll-off in the transition region, but produces ripples in the passband and stopband.

**emitter** The part of a transistor that is the source of carriers. For *npn* transistors, the emitter sends free electrons into the base. For *pnp* transistors, the emitter sends holes into the base.

**emitter bias** The best way to bias a transistor for operation in the active region. The key idea is to set up a fixed value of the emitter current.

**emitter diode** The diode formed by the emitter and base of a transistor.

**emitter-feedback bias** Stabilizing the *Q* point of a base-bias circuit by adding an emitter resistor. The emitter resistor provides negative feedback.

**emitter follower** Identical to a *CC amplifier*. The name *emitter follower* caught on because it better describes the action. The ac emitter voltage follows the ac base voltage.

**enhancement-mode MOSFET** A FET with an insulated gate that relies on an inversion layer to control its conductivity.

**epitaxial layer** A thin, deposited crystal layer that forms a portion of the electrical structure of certain semiconductors and integrated circuits.

**error voltage** The voltage between the two input terminals of an op amp. It is identical to the differential input voltage of the op amp.

**experimental formula** A formula or an equation discovered through experiment or observation. It represents an existing law in nature.

**extrinsic** Refers to a doped semiconductor.

## F

**feedback attenuation factor** An indication of how much the output voltage is attenuated before the feedback signal reaches the input.

**feedback capacitor** A capacitor located between the input and output terminals of an amplifier. This capacitor feeds a portion of the output signal back to the input and impacts the voltage gain and frequency response of the amplifier.

**feedback fraction** *B* The feedback voltage divided by the output voltage in a VCVS or noninverting amplifier configuration. This value is also known as the feedback attenuation factor *B*.

**feedback resistor** A resistor placed in a circuit for the purpose of developing a negative feedback signal across it. This resistor is used to control the gain and stability of an amplifier.

**FET Colpitts oscillator** An FET oscillator in which the feedback signal is applied to the gate.

**field effect** The control of the depletion layer width existing between the gate and channel of a field effect transistor. The width of this field controls the amount of drain current.

**field-effect transistor** A transistor that depends on the action of an electric field to control its conductivity.

**filter** An electronic network designed to either pass or reject a range of band of frequencies. **firing angle** The electrical degree point or angle at which a thyristor fires and begins to conduct with an ac input waveform applied.

**firm voltage divider** A voltage divider whose loaded output voltage is within 10 percent of its unloaded output voltage.

**first-order response** The frequency response of a passive or active filter that has a 20 dB per decade roll-off.

**555 timer** A widely used circuit that can run in either of two modes: monostable and astable. In monostable, it can produce accurate time delays, and in astable it can produce rectangular waves with a variable duty cycle.

**flag** A voltage that indicates an event has taken place. Typically, a low voltage means the event has not occurred, while a high voltage means that it has. The output of a comparator is an example of a flag.

**floating load** This is a load that has nonzero node voltages on each end. You can spot it on a schematic diagram by the fact that neither end of the load is grounded.

**FM demodulator** A phase-locked loop (PLL) used as a circuit that recovers the modulating signal from the FM wave.

**foldback current limiting** Simple current limiting allows the load current to reach a maximum value while the load voltage is reduced to zero. Foldback current limiting takes this one step further. It allows the current to reach a maximum value. Then further decreases in the load resistance reduce both the load current and the load voltage.

The main advantage of foldback limiting is less power dissipation in the pass transistor under shorted-load conditions.

**formula** A rule that relates quantities. The rule may be an equation, equality, or other mathematical description.

**forward bias** Applying an external voltage to overcome the barrier potential.

**four-layer diode** A semiconductor component consisting of an interconnected four-layer *pnnp* structure. This diode allows current to flow through it in only one direction when a specific breakdown voltage is reached. Once on, it will remain on until the current through it falls below its holding current *I<sub>H</sub>* value.

**free electron** One that is loosely held by an atom. Also known as a *conduction-band electron* because it travels in a large orbit, equivalent to a high energy level.

**frequency modulation (FM)** A basic electronic communication technique in which an input intelligence signal (modulating signal) causes the output (carrier signal) to vary in frequency.

**frequency response** The graph of voltage gain versus frequency for an amplifier.

**frequency scaling factor (FSF)** The formula used to scale pole frequencies in direct proportion; cutoff frequency divided by 1 kHz.

**frequency-shift keying** A modulation technique, used in the transmission of binary data, in which an input signal causes the output signal to vary in one of two distinct output frequencies.

**full-wave rectifier** A rectifier with a center-tapped secondary winding and two diodes that act as back-to-back half-wave rectifiers. One diode supplies one-half of the output, and the other diode supplies the other half. The output is a full-wave rectified voltage.

**fundamental frequency** The lowest frequency that a crystal can effectively vibrate and produce an output. This frequency is dependent on the crystal's material constant *K* and its thickness *t* where  $f = \frac{K}{t}$ .

## G

**gain-bandwidth product (GBP)** The high frequency at which the gain of an amplifier is 0 dB (unity).

**gate** The terminal of a field-effect transistor that controls drain current. Also, the terminal of a thyristor used to turn on the device.

**gate-bias** A simplified method of biasing an FET by connecting a voltage source, through a source resistor, to the gate lead.

This biasing method is not suitable for active-region biasing due to the large spread of FET parameters. This biasing method is most applicable for biasing the FET in the ohmic region.

**gate-source cutoff voltage** The voltage between the gate and the source that reduces the drain current of a depletion-mode device to approximately zero.

**gate trigger current**  $I_{GTR}$  The minimum gate current specified to turn on an SCR.

**geometric average** The center frequency  $f_0$  of a bandpass filter found mathematically by  $f_0 = \sqrt{f_1 f_2}$ .

**germanium** One of the first semiconductor materials to be used. Like silicon, it has four valence electrons.

**go/no-go test** A test or measurement where the readings are distinctly different, really high or really low.

**ground loop** If you use more than one ground point in a multistage amplifier, the resistance between the ground points will produce small unwanted feedback voltages. This is a ground loop. It can cause unwanted oscillations in some amplifiers.

**guard driving** Minimizing the effects of cable leakage current and cable capacitance by actively bootstrapping the shield to the common-mode potential.

## H

***h* parameters** An early mathematical method for representing transistor action. Still used on data sheets.

**half-power frequencies** The frequencies at which the load power is reduced to half of its maximum value. This is also referred to as cutoff frequencies because the voltage gain equals 0.707 of the maximum value at this point.

**half-wave rectifier** A rectifier with only one diode in series with the load resistor. The output is a half-wave rectified voltage.

**hard saturation** Operating a transistor at the upper end of the load line with a base current that is one-tenth of the collector current. The reason for the overkill is to make sure the transistor remains saturated under all operating conditions, temperature conditions, transistor replacement, etc.

**harmonic distortion** A form of distortion caused by a signal passing through or being amplified by a nonlinear system resulting in an output signal containing multiples of the fundamental frequency.

**harmonics** A sine wave whose frequency is some integer multiple of a fundamental sine wave.

**Hartley oscillator** A circuit distinguished by its inductively tapped tank circuit.

**headroom voltage** The difference between the input and output voltage of a transistor series voltage regulator or a three-terminal IC voltage regulator.

**heat sink** A mass of metal attached to the case of a transistor to allow the heat to escape more easily.

**high-frequency border** The frequency above which a capacitor acts as an ac short. Also, the frequency where the reactance is one-tenth of the total series resistance.

**high-pass filter** A filter capable of blocking a range of frequencies from zero to a specified

cutoff frequency  $f_c$  and passing all frequencies above the cutoff frequency.

**holding current** The minimum current through a thyristor that can keep it latched in the conducting stage.

**hole** A vacancy in the valence orbit. For instance, each atom of a silicon crystal normally has eight electrons in the valence orbit. Heat energy may dislodge one of the valence electrons, producing a hole.

**hybrid IC** A high-power integrated circuit consisting of two or more monolithic ICs in one package or the combination of thin- and thick-film circuits. Hybrid ICs are often used in high-power audio-amplifier applications.

**hysteresis** The difference between the two trip points of a Schmitt trigger. When used elsewhere, hysteresis refers to the difference between the two trip points on the transfer characteristic.

**insulated-gate bipolar transistor (IGBT)** A hybrid semiconductor device constructed with FET characteristics on the input side and FET characteristics on the output side. This device is primarily used in high-power switching control applications.

**insulated-gate FET (IGFET)** Another name for MOSFET, which has a gate that is insulated from the channel, producing a smaller gate current than in a JFET.

**integrated circuit** A device that contains its own transistors, resistors, and diodes. A complete IC using these microscopic components can be produced in the space occupied by a discrete transistor.

**integrator** A circuit that performs the mathematical operation of integration. One popular application is generating ramps from rectangular pulses. This is how the time base is generated in oscilloscopes.

**interface** An electronic component or circuit that enables one type of device or circuit to communicate with or control another device or circuit.

**internal capacitance** The internal capacitance values between the  $pn$  junctions of a transistor. These values can normally be neglected under low-frequency conditions, but will provide bypass paths and loss of voltage gain for an ac signal at high frequencies.

**intrinsic** Refers to a pure semiconductor. A crystal that has nothing but silicon atoms is pure or intrinsic.

**inverse Chebyshev approximation** An active filter capable of producing a flat bassband response and a fast roll-off. It has the disadvantage of producing ripples in the stopband.

**inverting input** The input to a diff amp or an op amp that produces an inverted output.

**inverting voltage amplifier** As the name implies, the amplified output voltage is inverted with respect to the input voltage.

## J

**junction** The border where  $p$ - and  $n$ -type semiconductors meet. Unusual things happen at a  $pn$  junction such as the depletion layer, the barrier potential, etc.

**junction temperature** The temperature found inside a semiconductor at the  $pn$  junction. This temperature is normally higher than the ambient temperature due to electron-hole pair recombination.

**junction transistor** A transistor having three alternate sections of  $p$ -type and  $n$ -type materials. These sections are in either a  $p-n-p$  or  $n-p-n$  arrangement.

## K

**knee voltage** The point or area on a graph of diode current versus voltage where the forward current suddenly increases. It is approximately equal to the barrier potential of the diode.

**L**  
**lag circuit** Another name for a bypass circuit. The word *lag* refers to the angle of the output phasor voltage, which is negative with respect to angle of the input phase voltage. The phase angle may vary from 0 to  $-90^\circ$  (lagging).

**large signal operation** An amplifier in which the ac input peak-to-peak signal causes the transistor to use all or most of its ac load line.

**laser diode** A semiconductor laser device with the acronym for light amplification by stimulated emission of radiation. This active electron device converts input power into a very narrow, intense beam of coherent visible or infrared light.

**laser trimming** Obtaining very precise resistor values by burning off resistance areas on a semiconductor chip using a laser.

**latch** Two transistors connected with positive feedback to simulate the action of a thyristor.

**law** A summary of a relationship that exists in nature and can be verified with an experiment.

**lead circuit** Another name for a coupling circuit. The word *lead* refers to the angle of the output phasor voltage, which is positive with respect to angle of the input phase voltage. The phase angle may vary from 0 to  $+90^\circ$  (leading).

**lead-lag circuit** A circuit that combines a coupling and a bypass circuit. The angle of the output phasor voltage may be positive or negative with respect to the input phasor voltage. The phase angle may vary from  $-90^\circ$  (lagging) to  $+90^\circ$  (leading).

**leakage current** Often used for the total reverse current of a diode. It includes thermally produced current as well as the surface leakage current.

**leakage region** The graphed region on a reverse-biased zener diode between zero current and breakdown.

**LED driver** A circuit that can produce enough current through a LED to get light.

**lifetime** The average amount of time between the creation and recombination of a free electron and a hole.

**light-emitting diode** A diode that radiates colored light such as red, green, yellow, etc., or invisible light such as infrared.

**linear** Usually refers to the graph of current versus voltage for a resistor.

**linear op-amp circuit** This is a circuit where the op amp never saturates under normal operating conditions. This implies that the amplified output has the same shape as the input.

**linear phase shift** The response of a filter circuit where the phase shift increases linearly with frequency. One such filter is a Bessel filter.

**linear regulator** The series regulator is an example of a linear regulator. The thing that makes a linear regulator is the fact that the

pass transistor operates in the active or linear region. Another example of a linear regulator is the shunt regulator. In this type of regulator, a transistor is shunted across the load. Again, the transistor operates in the active region, so the regulator is classified as a linear regulator.

**line regulation** A power supply specification indicating how much the output voltage will change for a given input line voltage variation.

**line voltage** The voltage from the power line. It has a nominal value of 115 V rms. In some places, it may be as low as 105 or as high as 125 V rms.

**Lissajous pattern** The pattern appearing on an oscilloscope when harmonically related signals are applied to the horizontal and vertical inputs.

**load line** A tool used to find the exact value of diode current and voltage.

**load power** The ac power in the load resistor.

**load regulation** The change in the regulated load voltage when the load current changes from its minimum to its maximum specified value.

**lock range** The range of input frequencies over which a voltage-controlled-oscillator (VCO) can remain locked on to the input frequency. The lock range is normally specified as a percentage of the VCO frequency.

**logarithmic scale** A scale where various points are plotted according to the logarithm of the number with which the point is labeled. This scale compresses very large values and allows the plotting of data over many decades.

**loop gain** The product of the differential voltage gain *A* and the feedback fraction *B*. The value of this product is usually very large. If you pick any point in an amplifier with a feedback path, the voltage gain starting from this point and going around the loop is the loop gain. The loop gain is usually made up of two parts: the gain of the amplifier (greater than 1) and the gain of the feedback circuit (less than 1). The product of these two gains is the loop gain.

**low-current drop-out** The switching of a semiconductor latching circuit from on to off as a result of the latching current dropping low enough to bring the transistors out of saturation.

**lower trip point (LTP)** One of the two input voltages at which the output voltage changes states.  $LTP = -BV_{sat}$ .

**low-pass filter** A filter capable of passing a range of frequencies from zero to a specified cutoff frequency  $f_c$ .

**LSI** Large-scale integration. Integrated circuits with more than 100 integrated components.

## M

**majority carrier** Carriers are either free electrons or holes. If the free electrons outnumber the holes, the electrons are the majority carriers. If the holes outnumber the free electrons, the holes are the majority carriers.

**maximum forward current** The maximum amount of current that a forward-biased diode can withstand before burning out or being seriously degraded.

**measured voltage gain** The voltage gain that you calculate from the measured values of input and output voltage.

**metal-oxide semiconductor FET (MOSFET)**

Often used in switching amplifier applications, this transistor provides extremely low power dissipation even with high currents.

**midband** We have defined this as  $10f_1$  to  $0.1f_2$ . In this range of frequencies, the voltage gain is within 0.5 percent of the maximum voltage gain.

**Miller's theorem** It says a feedback capacitor is equivalent to two new capacitances, one across the input and the other across the output. The most significant thing is that the input capacitance is equal to the feedback capacitance times the voltage gain of an amplifier. This assumes an inverting amplifier.

**minority carrier** The carriers that are in the minority. (See the definition of *majority carrier*.)

**mixer** An op-amp circuit that can have a different voltage gain for each of several input signals. The total output signal is a superposition of the input signals.

**modulating signal** The low-frequency or intelligence input signal (usually voice or data) used to control the amplitude, frequency, phase, or other condition of an output signal.

**monolithic IC** An integrated circuit that is entirely on a single chip.

**monostable** A digital switching circuit with one stable state. This circuit is also referred to as a *one-shot* and is used in timing circuits.

**monotonic** A description of a filter which has no ripples in the stopband.

**motorboating** A low-pitched putt-putt sound that comes out of a loudspeaker. It indicates that an amplifier is oscillating at a low frequency. The cause is usually the power supply having too large a Thevenin impedance.

**mounting capacitance** The equivalent capacitance  $C_m$  of a crystal when it is not vibrating. Due to its physical construction, the crystal is essentially two metal plates separated by a dielectric.

**MPP value** Also called the *output voltage swing*. This is the maximum unclipped peak-to-peak output of an amplifier. With an op amp, the MPP value is ideally equal to the difference of the two supply voltages.

**MSI** Medium-scale integration. Circuits with 10 to 100 integrated components.

**multiple feedback (MFB)** An active filter design using more than one feedback path. The feedback paths generally are applied to the op amp's inverting input through a separate resistor and capacitor.

**multiplexing** A technique that allows more than one signal to be transmitted concurrently over a single medium.

**multistage amplifier** An amplifier configuration that consists of two or more individual stages of amplification cascaded together. The output of the first stage drives the input of the second stage. The output of the second stage can be used as the input to the third stage.

**multivibrator** A circuit with positive feedback and two active devices, designed so that one device conducts while the other cuts off. There are three types: a free-running multivibrator, a flip-flop, and a one-shot. The free-running or astable multivibrator produces a rectangular output, similar to a relaxation oscillator.

## N

**n-type semiconductor** A semiconductor where there are more free electrons than holes.

**narrowband amplifier** An amplifier constructed to operate over a small frequency range. This type of amplifier is often used in RF communications circuits.

**narrowband filter** A bandpass filter with a  $Q$  greater than 1 and effectively passes a small range of frequencies.

**natural logarithm** The logarithm of a number to the base  $e$ . Natural logarithms can be used when analyzing the charging and discharging of capacitors.

**negative feedback** Feeding a signal back to the input of an amplifier that is proportional to the output signal. The returning signal has a phase that opposes the input signal.

**negative resistance** The property of an electronic component where an increase in forward voltage produces a decrease in forward current over part of its V/I characteristic curve.

**noninverting input** The input to a diff amp or an op amp that produces an in-phase output.

**nonlinear circuit** An amplifier circuit where part of the input signal drives the amplifier into saturation or cutoff. The resulting output waveform has a different shape than the input waveform.

**nonlinear device** A device that has a graph of current versus voltage that is not a straight line. A device that cannot be treated as an ordinary resistor.

**normalized variable** A variable that has been divided by another variable with the same units or dimensions.

**Norton's theorem** Derived from the duality principle, the Norton theorem states that the load voltage equals the Norton current times the Norton resistance in parallel with the load resistance.

**notch filter** A filter that blocks a signal with at most one frequency.

**nulling circuit** An external op amp circuit used to reduce the effect of input offset current and input offset voltage. This circuit is used when the output error cannot be ignored.

## O

**octave** A factor of 2. Often used with frequency ratios of 2, as in an octave of frequency referring to a 2:1 change in frequency.

**ohmic region** The part of the drain curves that starts at the origin and ends at the proportional pinchoff voltage.

**op amp** A high-gain dc amplifier that provides usable voltage gain for frequencies from 0 to over 1 MHz.

**open** Refers to a component or connecting wire that has an open circuit, equivalent to a high resistance approaching infinity.

**open-collector comparator** An op amp comparator circuit that requires the use of an external *pullup* resistor. An open-collector configuration enables higher output switching speeds and allows for the interfacing of circuits with different voltage levels.

**open device** A device that has infinite resistance resulting in zero current flow through it.

**open-loop bandwidth** The frequency response of an op amp without a feedback path between the output and input. The cutoff frequency  $f_{2(OL)}$  is normally very low due to the internal compensating capacitor.

**open-loop voltage gain** Designated as  $A_{VOL}$  or  $A_{OL}$ , this specification designates the maximum voltage gain of an op amp without feedback.

**optimum Q point** The point where the ac load line has equal maximum signal swings on both half-cycles.

**optocoupler** A combination of a LED and a photodiode. An input signal to the LED is converted to varying light which is detected by the photodiode. The advantage is very high isolation resistance between the input and output.

**optoelectronics** A technology that combines optics and electronics, including many devices based on the action of a *pn* junction. Examples of optoelectronic devices are LEDs, photodiodes, and optocouplers.

**order of a filter** A basic description of the effectiveness of a filter. Generally, the higher the order of a filter, the closer it will be to achieving an ideal response. The order of a passive filter depends on the number of inductors and capacitors. The order of an active filter is determined by the number of RC circuits or poles it has.

**oscillations** The death of an amplifier. When an amplifier has positive feedback, it may break into oscillations, which is unwanted high-frequency signal. This signal is unrelated to the amplified input signal. Because of this, oscillations interfere with the desired signal. Oscillations make an amplifier useless. This is why a compensating capacitor is used with an op amp; it prevents the oscillations from occurring.

**outboard transistor** A transistor placed in parallel with a regulating circuit to increase the amount of load current that the overall circuit can regulate. The outboard transistor kicks in at a predetermined current level and

supplies the extra current needed by the load.

**output error voltage** The output voltage from an op amp circuit when the input voltage is zero. This value should ideally be zero.

**output impedance** Another term used for the Thevenin impedance of an amplifier. It means the amplifier has been Thevenized, so that the load sees only a single resistance in series with a Thevenin generator. This single resistance is the Thevenin or output impedance.

**output offset voltage** Any deviation or difference of the output voltage from the ideal output voltage.

**output transducer** A device that converts an electrical quantity into a nonelectrical quantity such as temperature, sound, pressure, or light.

**overloading** Using a load resistance so small that it decreases the voltage gain of an amplifier by a noticeable amount. In terms of the Thevenin theorem, overloading occurs when the load resistance is small compared to the Thevenin resistance.

## P

**parasitic oscillations** Oscillations of a very high frequency that cause all sorts of strange things to happen. Circuits act erratically, oscillators may produce more than one output frequency, op amps will have unaccountable offsets, supply voltage will have unexplainable ripples, video displays will contain snow, etc.

**passband** The range of frequencies that can be effectively passed with minimum attenuation.

**passive filter** A filter built using resistors, capacitors, and inductors without using amplification devices.

**pass transistor** The main current-carrying transistor found in a discrete series voltage regulator. This transistor is in effect in series with the load. Therefore, it must pass the entire load current.

**peak detector** The same as a rectifier with a capacitor input filter. Ideally, the capacitor charges to the peak of the input voltage. This peak voltage is then used for the output voltage of the peak detector, which is why the circuit is called a peak detector.

**peak inverse voltage** The maximum reverse voltage across a diode in a rectifier circuit.

**peak value** The largest instantaneous value of a time-varying voltage.

**periodic** An adjective that describes a waveform that repeats the same basic shape for cycle after cycle.

**phase detector** The circuit in a phase-locked-loop (PLL) that produces an output voltage proportional to the phase difference between two input signals.

**phase-locked loop** An electronic circuit that uses feedback and a phase comparator to control frequency or speed.

**phase shift** The difference in phase angle between phasor voltages at points A and B. For an oscillator, the phase shift around the amplifier and feedback loop at the resonant frequency must equal 360°, equivalent to 0°, for the oscillator to work.

**phase splitter** A circuit that produces two voltages of the same amplitude but opposite phase. It is useful for driving class B push-pull amplifiers. If you will visualize a swamped CE amplifier with a voltage gain of 1, then you will have a phase splitter because the ac voltages across the collector and emitter resistances are equal in magnitude and opposite in phase.

**photodiode** A reverse-biased diode that is sensitive to incoming light. The stronger the light, the larger the reverse minority-carrier current.

**phototransistor** A transistor with a collector junction that is exposed to light, producing more sensitivity to light than a photodiode does.

**Pierce crystal oscillator** A popular oscillator configuration that uses field-effect transistors, favored because of its simplicity.

**piezoelectric effect** Vibration that occurs when a crystal is excited by an ac signal across its plates.

**II model** An ac model of a transistor shaped like the Greek symbol II.

**pinchoff voltage** The border between the ohmic region and the current-source region of a depletion-mode device when the gate voltage is zero.

**PIN diode** A diode consisting of an intrinsic semiconductor material placed between n-type and p-type materials. When reverse biased, the PIN diode acts like a fixed capacitor and a current-controlled resistance when reverse biased.

**pn junction** The border between p-type and n-type semiconductors.

**pnp transistor** A semiconductor sandwich. It contains an n region between two p regions.

**pole frequency** A special frequency used in the calculations of higher-order active filters.

**poles** The number of RC circuits in an active filter. The number of poles in an active filter determines the order and response of the filter.

**positive clumper** A circuit that produces a positive dc shift of a signal by moving all the input signal upward until the negative peaks are at zero and the positive peaks are at  $2V_p$ .

**positive feedback** Feedback where the returning signal aids or increases the effect of the input voltage.

**positive limiter** A circuit that clips off the positive parts of the input signal.

**power amplifier** A large-signal amplifier designed to produce from a few hundred milliwatts up to several hundred watts of output power.

**power bandwidth** The highest frequency that an op amp can handle without distorting the

output signal. The power bandwidth is inversely proportional to the peak value.

**power dissipation** The product of voltage and current in a resistor or other nonreactive device. Rate at which heat is produced within a device.

**power FET** An E-MOSFET designed to handle the necessary current levels for controlling motors, lamps, and switching power supplies as compared to a low-power E-MOSFET used in digital circuits.

**power gain** The ratio of output power to input power.

**power rating** The maximum power that can be dissipated in a component or device that is operated according to a manufacturer's specifications.

**power supply** The section of an electronic system that converts the incoming ac line voltage to dc voltage. This section also provides for the necessary filtering and voltage regulation requirements of the system.

**power-supply rejection ratio (PSRR)** PSRR equals the change in the input offset voltage divided by the change in the supply voltages.

**power transistor** A transistor that can dissipate more than 0.5 W. Power transistors are physically larger than small-signal transistors.

**preamp** An amplifier designed to operate with low-level signals applied. Its main functions are to provide the necessary input impedance values and to produce the output signal value required by the next amplifier stage.

**predicted voltage gain** The voltage gain you calculate from the circuit values on a schematic diagram. For a CE stage, it equals the ac collector resistance divided by the ac resistance of the emitter diode.

**predistortion** Decreasing the design value of Q to compensate for op amp bandwidth limitations.

**preregulator** The first of two zener diodes used to drive a zener regulator circuit configuration. The preregulator provides the proper dc input to the regulator.

**programmable unijunction transistor (PUT)**

A semiconductor device with switching characteristics similar to a UJT, except its intrinsic standoff ratio can be determined (programmed) by external circuitry.

**proportional pinchoff voltage** The border between the ohmic region and the current-source region for any gate voltage.

**prototype** A basic circuit that a designer can modify to get more advanced circuits.

**p-type semiconductor** A semiconductor where there are more holes than free electrons.

**pullup resistor** A resistor that the user has to add to an IC device to make it work properly. One end of the pullup resistor is connected to the device, and the other end is connected to the positive supply voltage.

**pulse-position modulation** A procedure in which the pulse change position according to the amplitude of the analog signal.

**pulse-width modulation** Controlling the width of rectangular waves for the purpose of adding intelligence or to control the average dc value.

**push-pull connection** Use of two transistors in a connection that makes one of them conduct for half a cycle while the other is turned off. In this way, one of the transistors amplifies the first half-cycle, and the other amplifies the second half-cycle.

## Q

**quartz-crystal oscillator** A very stable and accurate oscillator circuit that uses the piezoelectric effect of a quartz crystal to establish its oscillator frequency.

**quiescent point (Q point)** The operating point found by plotting the collector current and voltage.

## R

**r' parameters** One way to characterize a transistor. This model uses quantities like  $\beta$  and  $r'_d$ .

**radio-frequency (RF) amplifier** Also known as a preselector, this amplifier provides some initial gain and selectivity.

**radio-frequency interference (RFI)** Interference from high-frequency electromagnetic waves emanating from electronic devices.

**rail-to-rail op amp** An op amp whose output voltage can swing all the way to the positive and negative supply voltages. In most op amps, the output swing is limited to 1–2 V less than either supply voltage.

**RC differentiator** An RC circuit used to differentiate an input signal of a rectangular pulse into a series of positive and negative spikes.

**recombination** The merging of a free electron and a hole.

**rectifiers** Circuits within a power supply that allow current to flow in only one direction. These circuits convert an ac input waveform to a pulsating dc output waveform.

**rectifier diode** A diode optimized for its ability to convert ac to dc.

**reductio ad absurdum** A trick used when a device may be operating as a current source or as a resistor. You assume a current source and proceed with the calculations. If any contradictory answers turn up, you know your original assumption was wrong. Then you can change to the resistor model and finish off the calculations. Reductio ad absurdum usually works whenever you have a two-state system and don't know which state it is in.

**reference voltage** Usually, a very precise and stable voltage derived from a zener diode with a breakdown voltage between 5 to 6 V. In this range, the temperature coefficient of the zener diode is approximately zero, which means its zener voltage is stable over a large temperature range.

**relaxation oscillator** A circuit that creates or generates an ac output signal without an ac

**input signal.** This type of oscillator depends on the charging and discharging of a capacitor through a resistor.

**resonant frequency** The frequency of a lead-lag circuit or the frequency of an *LC* tank circuit where the voltage gain and phase shift are suitable for oscillations.

**reverse-bias** Applying an external voltage across a diode to aid the barrier potential. The result is almost zero current. The only exception is when you can exceed the breakdown voltage. If the reverse voltage is large enough, it can produce breakdown through either avalanche or the zener effect.

**reverse saturation current** The same as the minority-carrier current in a diode. This current exists in the reverse direction.

**ripple** With a capacitor input filter, this is the fluctuation in load voltage caused by the charging and discharging of the capacitor.

**ripple rejection** Used with voltage regulators. It tells you how well the voltage regulator rejects or attenuates the input ripple. Data sheets usually list it in decibels, where each 20 dB represents a factor-of-10 decrease in ripple.

**risetime** The time it takes for a waveform to increase from 10 percent to 90 percent of its maximum value. Abbreviated  $T_R$ , risetime can be applied to frequency response using the equation  $f_2 = \frac{0.35}{T_R}$ .

**rms value** Used with time-varying signals. Also known as the *effective value* and the *heating value*. This is the equivalent value of a dc source that would produce the same amount of heat or power over one complete cycle of the time-varying signal.

**RS flip-flop** An electronic circuit with two states. Also known as a *multivibrator*. May be free-running (as in an oscillator) or may exhibit one or two stable states.

**R/2R ladder** A digital-to-analog converter circuit using two basic resistor values arranged in a ladder configuration to reduce resistor value count, improve the accuracy of conversion, and minimize loading effects.

## S

**safety factor** The leeway between the actual operating current, voltage, etc. and the maximum rating specified on a data sheet.

**Sallen-Key equal-component filter** A VCVS active filter designed using two equal resistor values and two equal capacitor values. The  $Q$  of the circuit is effected by the circuit's voltage gain and is determined by  $Q = \frac{1}{3 - A_v}$ .

**Sallen-Key low-pass filter** An active filter circuit configuration using an op amp connected as a voltage-controlled voltage source (VCVS). This filter has the ability to implement basic Butterworth, Chebyshev, and Bessel low-pass approximations.

**Sallen-Key second-order notch filter** A VCVS active bandstop filter with the capability of

achieving very steep roll-offs. The circuit's  $Q$  is dependent on the voltage gain and is found by  $Q = \frac{0.5}{2 - A_v}$ .

**saturation current** The current in a reverse-biased diode caused by thermally produced minority carriers.

**saturated current gain** The current gain of a transistor in the saturation region. This value is less than the active current gain. For soft saturation, the current gain is slightly less than the active current gain. For hard saturation, the current gain is approximately 10.

**saturation point** Approximately the same as the upper end of the load line. The exact location of the saturation point is slightly lower because the collector-emitter voltage is not quite zero.

**saturation region** The part of the collector curves that starts at the origin and slopes upward to the right until it reaches the beginning of the active or horizontal region. When a transistor operates in the saturation region, the collector-emitter voltage is typically only a few tenths of a volt.

**sawtooth generator** A circuit capable of producing a waveform characterized by a slow, linear rise time and a virtually instantaneous fall time.

**Schmitt trigger** A comparator with hysteresis. It has two trip points. This makes it immune to noise voltages, provided their peak-to-peak values are less than the hysteresis.

**Schockley diode** Another name for a *four-layer diode*, *pnpn diode*, and *silicon unilateral switch (SUS)* as named by its inventor.

**Schottky diode** A special-purpose diode with no depletion layer, extremely short reverse recovery time, and the ability to rectify high-frequency signals.

**second approximation** An approximation that adds a few more features to the ideal approximation. For a diode or transistor, this approximation includes the barrier potential in the model of the device. For silicon diodes or transistors, this means 0.7 V is included in the analysis.

**self-bias** The bias you get with a JFET because of the voltage produced across the source resistor.

**semiconductor** A broad category of materials having four valence electrons and electrical properties between those of conductors and insulators.

**series regulator** This is the most common type of linear regulator. It uses a transistor in series with the load. The regulation works because a control voltage to the base of the transistor changes its current and voltage as needed to keep the load voltage almost constant.

**series switch** A type of JFET analog switch where the JFET is in series with the load resistor.

**seven-segment display** A display containing seven rectangular LEDs.

**short** One of the common troubles that may occur. A short occurs when an extremely small resistance is approaching zero.

Because of this, the voltage across a short approaches zero, but the current may be very large. A component may be internally shorted, or it may be externally shorted by a solder splash or miswire.

**short-circuit output current** The maximum output current that an op amp can produce for a load resistor of zero.

**short-circuit protection** A feature of most modern power supplies. It usually means the power supply has some form of electronic current limiting that prevents excessive load currents under shorted-load conditions.

**shorted device** A device that has zero ohms of resistance resulting in zero voltage dropped across it.

**shunt regulator** A voltage regulating circuit in which the regulating device is placed in parallel with the load. This could be a simple zener diode, zener/transistor, or zener/transistor/op amp combination configuration.

**shunt switch** A type of JFET analog switch where the JFET is in shunt with the load resistor.

**sign changer** An op amp circuit that can be adjusted for a voltage gain from -1 to 1. Mathematically expressed as  $-1 < A_v < 1$ .

**silicon** The most widely used semiconductor material. It has 14 protons and 14 electrons in orbit. An isolated silicon atom has four electrons in the valence orbit. A silicon atom that is part of a crystal has eight electrons in the valence orbit because the four neighbors share one of the electrons.

**silicon controlled rectifier** A thyristor with three external leads called the *anode*, *cathode*, and *gate*. The gate can turn the SCR on, but not off. Once the SCR is on, you have to reduce the current to less than the holding current to shut off the SCR.

**silicon unilateral switch (SUS)** Another name for a *Schockley diode*. This device lets current flow in only one direction.

**single-ended** The output voltage of a differential amplifier taken from one of the collectors in respect to ground.

**sink** If you visualize water disappearing down a kitchen sink, you will have the general idea of what engineers or technicians mean when they talk about a current sink. It is the point that allows current to flow into ground or out of ground.

**slew rate** The maximum rate that the output voltage of an op amp can change. It causes distortion for high-frequency large-signal operation.

**small-signal amplifier** This type of amplifier is used at the front end of receivers because the signal coming in is very weak. (The peak-to-peak emitter current is less than 10 percent of the dc emitter current.)

**small-signal operation** This refers to an input voltage that produces only small fluctuations

- in the current and voltage.** Our rule for small-signal transistor operation is a peak-to-peak emitter current less than 10 percent of the dc emitter value.
- small-signal transistor** A transistor that can dissipate 0.5 W or less.
- soft saturation** Operation of the transistor at the upper end of the load line with just enough base current to produce saturation.
- solder bridge** An undesirable splash of solder connecting two conducting lines or circuit paths.
- source** The terminal of a field effect transistor comparable to the emitter of a bipolar junction transistor.
- source follower** The leading JFET amplifier. You see it used more than any other JFET amplifier.
- source regulation** The change in the regulated output voltage when the input or source voltage changes from its minimum to its maximum specified voltage.
- speed-up capacitor** A capacitor used to increase the switching speed of a circuit.
- squench circuit** A special circuit used in communications systems where the output signal is automatically quieted with the absence of an input signal.
- SSI** Small-scale integration. Refers to integrated circuits with 10 or fewer integrated components.
- stage** A functional part in which a circuit containing one or more active devices can be divided.
- state-variable filter** A tunable active filter that maintains a constant  $Q$  when the center frequency is varied.
- stepdown transformer** A transformer with more primary turns than secondary turns. This results in less secondary voltage than primary voltage.
- step-recovery diode** A diode having the properties of reverse snap-off due to lighter doping density near its junction. This diode is often used in frequency multiplier applications.
- stiff current source** A current source whose internal resistance is at least 100 times larger than the load resistance.
- stiff voltage divider** A voltage divider whose loaded output voltage is within 1 percent of its unloaded output voltage.
- stiff voltage source** A voltage source whose internal resistance is at least 100 times smaller than the load resistance.
- stopband** The range of frequencies that is effectively blocked or not allowed to pass from into to output.
- stray wiring capacitance** The unwanted capacitance between connecting wires and ground.
- substrate** A region in a depletion mode MOS-FET located opposite from the gate, forming a channel through which electrons flowing from source to drain must pass.
- summer** An op-amp circuit whose output voltage is the sum of the two or more input voltages.
- superposition** When you have several sources, you can determine the effect produced by each source acting alone and then add the individual effects, to get the total effect of all sources acting simultaneously.
- surface-leakage current** A reverse current that flows along the surface of a diode. It increases when you increase the reverse voltage.
- surface-mount transistors** A transistor package style that enables it to be soldered to the circuit board on the component side instead of using through-hole technology. Surface-mount technology (SMT) allows for densely populated circuit boards.
- surge current** The large initial current that flows through the diodes of a rectifier. It is the direct result of charging the filter capacitor, which initially is uncharged.
- swamped amplifier** A CE stage with a feedback resistor in the emitter circuit. This feedback resistor is much larger than the ac resistance of the emitter diode.
- swamp out** The use of a resistor or other component to nullify the effect of another circuit component. An unbypassed emitter resistor is commonly used to negate the effects of a transistor's  $r'_e$  value.
- switching circuit** A circuit that operates a transistor in either the saturation or cutoff regions. Two distinct operating regions enable the device to be used in digital and computer circuits along with output power control applications.
- switching regulator** A linear regulator uses a transistor that operates in the linear region. A switching regulator uses a transistor that switches between saturation and cutoff. Because of this, the transistor operates in the active region only during the short time that it is switching states. This implies that power dissipation of the pass transistor is much smaller than in a linear regulator.
- T**
- tail current** The current through the common emitter resistor  $R_E$  of a differential amplifier. When the transistors are perfectly matched, the individual emitter currents will be equal and can be found by  $I_E = \frac{I_T}{2}$ .
- temperature coefficient** The rate of change of a quantity with respect to the temperature.
- theorem** A derivation, in a statement form, that can be proved mathematically.
- thermal energy** Random kinetic energy possessed by semiconductor materials at a finite temperature.
- thermal noise** Noise generated by the random motion of free electrons inside a resistor or other component. This is also called Johnson noise.
- thermal resistance** A heat transfer characteristic quantity used by designers to determine semiconductor case temperatures and heat sink requirements.
- thermal runaway** As a transistor heats, its junction temperature increases. This increases the collector current, which forces the junction temperature to increase further, producing more collector current, etc., until the transistor is destroyed.
- thermal shutdown** A feature found in modern three-terminal IC regulators. When the regulator exceeds a safe operating temperature, the pass transistor is cut off and the output voltage goes to zero. When the device cools, the pass transistor is again turned on. If the original cause of the excessive temperature is still present, the device again shuts off. If the cause has been removed, the device works normally. This feature makes the regulator almost indestructible.
- theristor** A device whose resistance experiences large changes with temperature.
- Thevenin's theorem** A fundamental theorem that says any circuit driving a load can be converted to a single generator and series resistance.
- third approximation** An accurate approximation of a diode or transistor. Used for designs that need to take into account as many details as possible.
- threshold** The trip point or input voltage value of a comparator that causes the output voltage to change states.
- threshold voltage** The voltage that turns on an enhancement-mode MOSFET. At this voltage, an inversion layer connects the source to the drain.
- thyristor** A four-layer semiconductor device that acts as a latch.
- T model** An ac model of a transistor looking like a T on its side. The emitter diode acts like an ac resistance and the collector diode acts like a current source.
- topology** A term used to describe the technique or fundamental layout of a switching-regulator circuit. Common switching-regulator topologies are the buck regulator, boost regulator, and buck-boost regulator.
- total voltage gain** The overall voltage gain of an amplifier determined by the product of the individual stage gains. Mathematically found by  $A_v = (A_{v1})(A_{v2})(A_{v3})$ .
- transconductance** The ratio of ac output current to ac input voltage. A measure of how effectively the input voltage controls the output current.
- transconductance amplifier** An amplifier with the transfer characteristic where an input voltage controls an output current. This is also known as a voltage-to-current converter or VCIS circuit.
- transconductance curve** A graph displaying the relationship of  $I_D$  versus  $V_{GS}$  for a field effect transistor. This graph demonstrates the nonlinear characteristic of a FET and how it follows a square-law equation.
- transfer characteristic** The input/output response of a circuit. The transfer characteristic demonstrates the effectiveness of how the input controls the output.

**transfer function** The inputs and outputs of an op-amp circuit may be voltages, currents, or a combination of the two. When you use complex numbers for the input and output quantities, the ratio of output to input becomes a function of the frequency. The name for the ratio is the transfer function.

**transformer coupling** The use of a transformer to pass the ac signal from one stage to another while blocking the dc component of the waveform. The transformer also has the ability to match impedances between stages.

**transition** The roll-off region of a filter's frequency response between its cutoff frequency  $f_c$  and the beginning of the stopband  $f_s$ .

**transresistance amplifier** An amplifier with the transfer characteristic where an input current controls an output voltage. This is also known as a current-to-voltage converter or ICVS circuit.

**triac** A thyristor that can conduct in both directions. Because of this, it is useful for controlling alternating current. It is equivalent to two SCRs in parallel with opposite polarities.

**trial and error** Suppose you have a problem involving two simultaneous equations. Instead of solving this in the usual left-brain mathematical way, you can guess an answer and then calculate all the unknowns. One of the calculated unknowns is the very answer that you guessed. You compare the calculated and guessed answers to see how different they are. Then you guess another answer that will close the gap between the guessed and calculated answers. After several trials, the gap becomes small enough that you have an approximate answer.

**trigger** A sharp pulse of voltage and current that is used to turn on a thyristor or other switching device.

**trigger current** The minimum current needed to turn on a thyristor.

**trigger voltage** The minimum voltage needed to turn on a thyristor.

**trip point** The value of the input voltage that switches the output of a comparator or Schmitt trigger.

**troubleshooting** A method of determining a circuit fault using an acquired knowledge of electronics theory and electronics measurement equipment.

**tuned RF amplifier** A type of narrowband amplifier normally using high-Q resonant tank circuits.

**tunnel diode** A diode having the properties of negative resistance. This diode has a voltage breakdown that occurs at 0 V. Used in high-frequency oscillator circuits.

**twin-T oscillator** An oscillator that receives the positive feedback to the noninverting input through a voltage divider and the negative feedback through the twin-T filter.

**two-stage feedback** A circuit configuration where a portion of the second stage's output

signal is feedback into the first stage for controlling the overall gain and stability.

**two-state output** This is the output voltage from a digital or switching circuit. It is referred to as two-state because the output has only two stable states: low and high. The region between the low and high voltages is unstable because the circuit cannot have any value in this range except temporarily when switching between states.

**two-supply emitter bias (TSEB)** A power supply that produces both positive and negative supply voltages.

## U

**ultra-large-scale integration (ULSI)** The placing of more than 1 million components on a single chip.

**unidirectional load current** Current that flows through a load in only one direction as the result of a half- or full-wave rectifier.

**unijunction transistor** Abbreviated UJT, this low-power thyristor is useful in electronic timing, waveshaping, and control applications.

**uninterruptible power supply (UPS)** A device containing a battery and a dc-to-ac converter to be used during a power failure.

**unity-gain frequency** The frequency where the voltage gain of an op amp is 1. It indicates the highest usable frequency. It is important because it equals the gain-bandwidth product.

**universal curve** A solution in the form of a graph that solves a problem for a whole class of circuits. The universal curve for self-biased JFETs is an example. In this universal curve  $I_D/I_{DSS}$  is graphed for  $R_D/R_S$ .

**unwanted bypass circuit** A circuit that appears in the base or collector sides of a transistor because of internal transistor capacitances and stray wiring capacitances.

**up-down analysis** A method of analyzing an electronic circuit using independent and dependent variables. When an independent variable (such as a voltage source) is increased or decreased, the resulting dependent variable (resistor voltage drop or current) change is predicted.

**upper trip point (UTP)** One of the two input voltages in which the output voltage changes states.  $UTP = BV_{sat}$ .

**upside-down pnp bias** When you have a positive power supply and a pnp transistor, it is customary to draw the transistor upside-down. This is especially helpful when the circuit uses both npn and pnp transistors.

## V

**varactor** A diode optimized for a reverse capacitance. The larger the reverse voltage, the smaller the capacitance.

**varistor** A device that acts like two back-to-back zener diodes. Used across the primary

winding of a power transformer to prevent line spikes from entering the equipment.

**very-large-scale integration (VLSI)** The placing of thousands or hundreds of thousands of components on a single chip. **vertical MOS (VMOS)** A power MOSFET with a V-shaped groove channel geometry enabling the transistor to handle high currents and block high voltages.

**virtual ground** A type of ground that appears at the inverting input of an op amp that uses negative feedback. It's called virtual ground because it has some of, but not all, the effects of a mechanical ground. Specifically, it is ground for voltage but not for current. A node that is a virtual ground has 0 V with respect to ground, but the node has no path for current to ground.

**virtual short** Ideally, because of the large internal voltage gain and extremely high-input impedance of the op amp, the voltage across the inputs,  $v_1 - v_2$ , is zero and  $I_m$  is zero for both inputs. A virtual short is a short for voltage, but an open for current. Therefore, an op amp circuit can be analyzed on the input side as having a virtual short between its noninverting and inverting inputs.

**voltage amplifier** An amplifier that has its circuit values selected to produce a maximum voltage gain.

**voltage-controlled current source (VCIS)**

Sometimes called a *transconductance amplifier*, this type of negative feedback amplifier has input current controlling output voltage.

**voltage-controlled device** A device like a JFET or MOSFET whose output is controlled by an input voltage.

**voltage-controlled oscillator (VCO)** An oscillator circuit in which the output frequency is a function of a dc control voltage; also called a *voltage-to-frequency converter*.

**voltage-controlled voltage source (VCVS)** The ideal op amp, having infinite voltage gain, infinite unity-gain frequency, infinite input impedance, and infinite CMRR, as well as zero output resistance, zero bias, and zero offsets.

**voltage-divider bias (VDB)** A biasing circuit in which the base circuit contains a voltage divider that appears stiff to the input resistance of the base.

**voltage feedback** This is a type of feedback where the feedback signal is proportional to the output voltage.

**voltage follower** An op-amp circuit that uses noninverting voltage feedback. The circuit has a very high input impedance, a very low output impedance, and a voltage gain of 1. It is ideal for use as a buffer amplifier.

**voltage gain** This is defined as the output voltage divided by the input voltage. Its value indicates how much the signal is amplified.

**voltage multiplier** Direct current power-supply circuit used to provide transformerless step-up of ac line voltage.

**voltage reference** A circuit that produces an extremely accurate and stable output voltage. This circuit is often packaged as a special-function IC.

**voltage regulator** A device or circuit that holds the load voltage almost constant, even though the load current and source voltage are changing. Ideally, a voltage regulator is a stiff voltage source with an output or Thevenin resistance that approaches zero.

**voltage source** Ideally, an energy source that provides a constant load voltage for any value of the load resistance. To a second approximation, it includes a small internal resistance in series with the source.

**voltage step** A sudden input voltage change or transition applied to an amplifier. The output response will depend on the amplifier's rate of output voltage change per unit time, also known as its slew rate.

**voltage-to-current converter** A circuit that is equivalent to a controlled current source. The input voltage controls the current. The current is then constant and independent of the load resistance.

**voltage-to-frequency converter** A circuit with the ability for an input voltage to control an output frequency. This circuit is also known as a *voltage-controlled oscillator*.

## W

**wafer** A thin slice of a crystal used as a chassis for integrated components.

**wideband amplifier** An amplifier constructed to operate over a large frequency range. This type of amplifier is generally untuned using resistive loads.

**wideband filter** A bandpass filter with a  $Q$  less than 1 and effectively passes a large range of frequencies.

**Wien-bridge oscillator** An *RC* oscillator consisting of an amplifier and a Wien bridge. This is the most widely used low-frequency oscillator. It is ideal for generating frequencies from 5 Hz to 1 MHz.

**window comparator** A circuit used to detect when the input voltage is between two preset limits.

## Z

**zener diode** A diode designed to operate in reverse breakdown with a very stable voltage drop.

**zener effect** Sometimes called *high-field emission*, this occurs when the intensity of the electric field becomes high enough to dislodge valence electrons in a reverse-biased diode.

**zener follower** A circuit consisting of a zener regulator and an emitter follower. The transistor allows the zener to handle much less current as compared to an ordinary zener regulator. This circuit also has a low output impedance characteristic.

**zener regulator** A circuit consisting of a power supply or dc input voltage connected to a series resistor and a zener diode. The output voltage of this circuit is less than the output of the power supply. This circuit is also known as a zener voltage regulator.

**zener resistance** The bulk resistance of a zener diode. It is very small compared to the current-limiting resistance in series with the zener diode.

**zener voltage** The breakdown voltage of a zener diode. This is the approximate voltage out of a zener voltage regulator.

**zero-crossing detector** A comparator circuit where an input voltage is compared to a zero-volt reference voltage.

# Answers

## Odd-Numbered Problems

### CHAPTER 1

- 1-1.  $R_L \geq 10 \Omega$   
1-3.  $R_L \geq 5 \text{ k}\Omega$   
1-5. 0.1 V  
1-7.  $R_L \leq 100 \text{ k}\Omega$   
1-9. 1  $\text{k}\Omega$   
1-11. 4.80 mA and not stiff  
1-13. 6 mA, 4 mA, 3 mA, 2.4 mA,  
2 mA, 1.7 mA, 1.5 mA  
1-15.  $V_{TH}$  is unchanged, and  $R_{TH}$   
doubles  
1-17.  $R_{TH} = 10 \text{ k}\Omega$ ;  $V_{TH} = 100 \text{ V}$   
1-19. Shorted  
1-21. The battery or interconnecting  
wiring  
1-23. 0.08  $\Omega$   
1-25. Disconnect the resistor and  
measure the voltage.  
1-27. Thevenin's theorem makes it  
much easier to solve problems  
for which there could be  
many values of a resistor.  
1-29.  $R_S > 100 \text{ k}\Omega$ . Use a 100 V  
battery in series with 100  $\text{k}\Omega$ .  
1-31.  $R_1 = 30 \text{ k}\Omega$ ,  $R_2 = 15 \text{ k}\Omega$   
1-33. First, measure the voltage  
across the terminals—this is  
the Thevenin voltage. Next,  
connect a resistor across the  
terminals. Next, measure the  
voltage across the resistor.  
Then, calculate the current  
through the load resistor.  
Then, subtract the load  
voltage from the Thevenin  
voltage. Then, divide the  
difference voltage by the  
current. The result is the  
Thevenin resistance.  
1-35. Trouble 1:  $R_1$  shorted;  
Trouble 2:  $R_1$  open or  $R_2$   
shorted; Trouble 3:  $R_1$  open or  
 $R_2$  shorted; Trouble 4:  $R_3$   
open; Trouble 5:  $R_3$  shorted;  
Trouble 6:  $R_2$  open or open at  
point C; Trouble 7:  $R_4$  open or

open at point D; Trouble 8:  $R_2$   
open or open at point C;  
Trouble 9: open at point E;  
Trouble 10:  $R_4$  shorted;  
Trouble 11:  $R_4$  open or open  
at point D

### CHAPTER 2

- 2-1. —2  
2-3. a. Semiconductor;  
b. conductor;  
c. semiconductor;  
d. conductor  
2-5. a. 5 mA; b. 5 mA; c. 5 mA  
2-7. Minimum = 0.60 V,  
maximum = 0.75 V  
2-9. 0.53  $\mu\text{A}$ ; 4.47  $\mu\text{A}$

### CHAPTER 3

- 3-1. 27.3 mA  
3-3. 400 mA  
3-5. 10 mA  
3-7. 12.8 mA  
3-9. 19.3 mA, 19.3 V, 372 mW,  
13.5 mW, 386 mW  
3-11. 24 mA, 11.3 V, 272 mW,  
16.8 mW, 289 mW  
3-13. 0 mA, 12 V  
3-15. 9.65 mA  
3-17. 12 mA  
3-19. Open  
3-21. The diode is shorted or the  
resistor is open.  
3-23. The  $<2.0 \text{ V}$  reverse diode  
reading indicates a leaky diode.  
3-25. Cathode, toward  
3-27. 1N914: forward  $R = 100 \Omega$ ,  
reverse  $R = 800 \text{ M}\Omega$ ;  
1N4001: forward  $R = 1.1 \Omega$ ,  
reverse  $R = 5 \text{ M}\Omega$ ; 1N1185:  
forward  $R = 0.095 \Omega$ , reverse  
 $R = 21.7 \text{ k}\Omega$   
3-29. 23  $\text{k}\Omega$   
3-31. 4.47  $\mu\text{A}$   
3-33. During normal operation, the  
15-V power supply is

supplying power to the load.  
The left diode is forward-biased,  
allowing the 15-V power supply  
to supply current to the load. The right  
diode is reverse-biased  
because 15 V is applied to the  
cathode and only 12 V is  
applied to the anode; this  
blocks the 12-V battery. Once  
the 15-V power supply is lost,  
the right diode is no longer  
reverse-biased and the 12-V  
battery can supply current to  
the load. The left diode will  
become reverse-biased,  
preventing any current from  
going into the 15-V power  
supply.

- 3-35. The source voltage does not  
change, but all other variables  
decrease.  
3-37.  $V_A$ ,  $V_B$ ,  $V_C$ ,  $I_1$ ,  $I_2$ ,  $P_1$ ,  $P_2$ ; since  
 $R$  is so large it has no effect  
on the voltage divider;  
therefore the variables  
associated with the voltage  
divider do not change.

### CHAPTER 4

- 4-1. 70.7 V, 22.5 V, 22.5 V  
4-3. 70.0 V, 22.3 V, 22.3 V  
4-5. 20 Vac, 28.3 Vpk  
4-7. 21.21 V, 6.74 V  
4-9. 15 Vac, 21.2 Vpk, 15 Vac  
4-11. 11.42 V, 7.26 V  
4-13. 19.81 V, 12.60 V  
4-15. 0.5 V  
4-17. 21.2 V, 752 mV  
4-19. The ripple value will  
double.  
4-21. 18.85 V, 334 mV  
4-23. 18.85 V  
4-25. 17.8 V; 17.8 V; no; higher  
4-27. a. 2.12 mA; b. 2.76 mA  
4-29. 11.99 V

- 4-31.** The capacitor will be destroyed.  
**4-33.** 0.7 V, -50 V  
**4-35.** 1.4 V, -1.4 V  
**4-37.** 2.62 V  
**4-39.** 0.7 V, -89.7 V  
**4-41.** 3393.6 V  
**4-43.** 4746.4 V  
**4-45.** 10.6 V, -10.6 V  
**4-47.** Find the sum of each voltage value in  $i^2$  steps, then divide the total voltage by 180.  
**4-49.** Approximately 0 V. Each capacitor will charge up to an equal voltage but opposite polarity.

## CHAPTER 5

- 5-1.** 19.2 mA  
**5-3.** 53.2 mA  
**5-5.**  $I_S = 19.2 \text{ mA}$ ,  $I_L = 10 \text{ mA}$ ,  $I_Z = 9.2 \text{ mA}$   
**5-7.** 43.2 mA  
**5-9.**  $V_L = 12 \text{ V}$ ,  $I_Z = 12.2 \text{ mA}$   
**5-11.** 15.05 V to 15.16 V  
**5-13.** Yes,  $167 \Omega$   
**5-15.**  $784 \Omega$   
**5-17.** 0.1 W  
**5-19.** 14.25 V, 15.75 V  
**5-21.** a. 0 V; b. 18.3 V; c. 0 V; d. 0 V  
**5-23.** A short across  $R_S$   
**5-25.** 5.91 mA  
**5-27.** 13 mA  
**5-29.** 15.13 V  
**5-31.** Zener voltage is 6.8 V and  $R_S$  is less than  $440 \Omega$ .  
**5-33.** 24.8 mA  
**5-35.** 7.98 V  
**5-37.** Trouble 5: Open at A; Trouble 6: Open at  $R_L$ ; Trouble 7: Open at E; Trouble 8: Zener is shorted.

## CHAPTER 6

- 6-1.** 0.05 mA  
**6-3.** 4.5 mA  
**6-5.**  $19.8 \mu\text{A}$   
**6-7.**  $20.8 \mu\text{A}$   
**6-9.** 350 mW  
**6-11.** Ideal: 12.3 V, 27.9 mW  
 Second: 12.7 V, 24.7 mW  
**6-13.** -55 to +150°C  
**6-15.** Possibly destroyed  
**6-17.** a. Increase; b. increase;  
 c. increase; d. decrease;  
 e. increase; f. decrease

- 6-19.** 165.67  
**6-21.**  $560 \text{ k}\Omega$   
**6-23.** 5.64 mA  
**6-25.** An increase in  $V_{BB}$  causes the base current to increase, and since the transistor is controlled by base current, all other dependent variables increase except  $V_{CE}$ , which decreases because the transistor is further into conduction.  
**6-27.**  $I_C$ ,  $I_B$ , and all power dissipations decreased. The power dissipations decreased because of the drop in current ( $P = IV$ ). The base current decreased because the voltage drop across it did not change and the resistance increased ( $I = V/R$ ). The collector current decreased because the base current decreased ( $I_C = I_B\beta_{dc}$ ).  
**6-29.** The only variable that decreases is  $V_C$ . With an increase in  $\beta_{dc}$ , the same base current will cause a greater collector current, which will create a greater voltage drop across the collector resistor. This leaves less voltage to drop across the transistor.
- CHAPTER 7**
- 7-1.** 30  
**7-3.** 6.06 mA, 20 V  
**7-5.** The left side of the load line would move down and the right side would remain at the same point.  
**7-7.** 10.64 mA, 5 V  
**7-9.** The left side of the load line will decrease by half, and the right will not move.  
**7-11.** Minimum: 10.79 V; maximum: 19.23 V  
**7-13.** 4.55 V  
**7-15.** Minimum: 3.95 V; maximum: 5.38 V  
**7-17.** a. Not in saturation; b. not in saturation; c. in saturation; d. not in saturation  
**7-19.** 4.99995 V, 0.2 V  
**7-21.** 13.2 V  
**7-23.** 3.43 V
- 7-25.** 8.34 V  
**7-27.** 11 mA, 3 V  
**7-29.**  $I_B$  will increase;  $I_C$  will decrease;  $V_C$  will increase.  
**7-31.**  $I_B$  will not change;  $I_C$  will not change; more voltage at  $V_C$   
**7-33.**  $I_E$  will decrease;  $I_C$  will decrease;  $V_C$  will increase  
**7-35.**  $I_E$  will not change;  $I_C$  will not change; more voltage at  $V_C$   
**7-37.**  $V_{BB}$ ,  $V_{CC}$   
**7-39.**  $R_C$  could be shorted; the transistor could be open collector-emitter;  $R_B$  could be open, keeping the transistor in cutoff;  $R_E$  could be open; open in the base circuit; open in the emitter circuit  
**7-41.** Shorted transistor collector-emitter, since the emitter voltage should be 1.1 V; open collector resistor; loss of  $V_{CC}$   
**7-43.** Hand-selecting the components for mass production is not very efficient; instead try using feedback to make the gain independent of the  $\beta_{dc}$  of the transistor.  
**7-45.** 4.94 V  
**7-47.** 7.2  $\mu\text{A}$   
**7-49.** 22.6 mA  
**7-51.** 1.13 V  
**7-53.** Approximately 0.7 V  
**7-55.**  $2 \text{ k}\Omega$   
**7-57.**  $V_B$ ,  $V_E$ ,  $I_E$ ,  $I_C$ ,  $I_B$ , and  $P_E$  show no change. Since the base voltage did not change,  $V_B$  and  $V_E$  will not change. Since these voltages do not change, all the currents do not change.
- CHAPTER 8**
- 8-1.** 3.81 V, 11.28 V  
**8-3.** 1.63 V, 5.21 V  
**8-5.** 4.12 V, 6.14 V  
**8-7.** 3.81 mA, 7.47 V  
**8-9.** 31.96  $\mu\text{A}$ , 3.58 V  
**8-11.** 27.08  $\mu\text{A}$ , 37.36  $\mu\text{A}$   
**8-13.** 1.13 mA, 6.69 V  
**8-15.** 6.13 V, 7.19 V  
**8-17.** a. Decreases; b. increases; c. decreases; d. increases; e. increases; f. remains the same

- 8-19.** a. 0 V; b. 7.83 V; c. 0 V;  
 d. 10 V; e. 0 V  
**8-21.** -4.94 V  
**8-23.** -6.04 V, -1.1 V  
**8-25.** The transistor will be destroyed.  
**8-27.** Short  $R_1$ , increase the power supply value.  
**8-29.** 9.0 V, 8.97 V, 8.43 V  
**8-31.** 8.8 V  
**8-33.** 27.5 mA  
**8-35.**  $R_1$  shorted  
**8-37.** Trouble 3:  $R_C$  is shorted; trouble 4: transistor terminals are shorted together  
**8-39.** Trouble 7: open  $R_E$ ; trouble 8:  $R_2$  is shorted  
**8-41.** Trouble 11: power supply is not working; trouble 12: emitter-base diode of the transistor is open

### CHAPTER 9

- 9-1.** 3.39 Hz  
**9-3.** 1.59 Hz  
**9-5.** 4.0 Hz  
**9-7.** 18.8 Hz  
**9-9.** 0.426 mA  
**9-11.** 150  
**9-13.** 40  $\mu$ A  
**9-15.** 11.7  $\Omega$   
**9-17.** 2.34 k $\Omega$   
**9-19.** Base: 207  $\Omega$ , collector: 1.02 k $\Omega$   
**9-21.** Min  $h_{fe}$  = 50; max  $h_{fe}$  = 200; current is 1 mA; temperature is 25° C.  
**9-23.** The capacitor has a certain amount of leakage current that will flow through the resistor and create a voltage drop across the resistor.  
**9-25.** 9.09 Hz  
**9-27.** 5.68 k $\Omega$ , 2.27 k $\Omega$   
**9-29.** 2700  $\mu$ F

### CHAPTER 10

- 10-1.** 234 mV  
**10-3.** 212 mV  
**10-5.** 39.6 mV  
**10-7.** 0.625 mV, 21.6 mV, 2.53 V  
**10-9.** 3.71 V  
**10-11.** 713 mV  
**10-13.** 14.7  
**10-15.** 12.5 k $\Omega$

- 10-17.** Since there is a voltage at the second stage input, the cause is most likely in the second stage. Some of the possible causes are open transistor, open emitter resistor, open collector resistor, open output coupling capacitor.  
**10-19.** 72.6 mV  
**10-21.** 3.6 k $\Omega$   
**10-23.** Trouble 5:  $C_2$  open; trouble 6: open  $R_2$ ; trouble 7: open bypass capacitor  $C_3$ ; trouble 8: collector resistor is open

### CHAPTER 11

- 11-1.** 154 k $\Omega$ , 1.09 k $\Omega$   
**11-3.** 0.995, 0.951 V  
**11-5.** 2.18 k $\Omega$ , 0.956 V  
**11-7.** 0.558 V  
**11-9.** 3.9  $\Omega$   
**11-11.** 351  
**11-13.** It remains at approximately 351.  
**11-15.** 1.6 M $\Omega$   
**11-17.** 100 k $\Omega$   
**11-19.** 6.8 V, 7.5 mA  
**11-21.** 16.4 V  
**11-23.** 650  $\mu$ A  
**11-25.** 37.8  $\Omega$ , 3.3 k $\Omega$   
**11-27.** 63.8 mV  
**11-29.**  $V_B$  = 4.48 V,  $V_E$  = 3.78 V,  $V_C$  = 11.22 V,  $I_E$  = 3.78 mA,  $I_C$  = 3.78 mA,  $I_B$  = 25.2  $\mu$ A  
**11-31.** With the control voltage at 0 V, the output is 1.79 V. With the control voltage at 5 V, the output is 0 V.  
**11-33.** 21.5 W, the transistor will be destroyed.  
**11-35.** 2  $\Omega$   
**11-37.** 0 V  
**11-39.** T4: open  $C_3$ ; T5: open between B and C; T6: open  $C_2$ ; T7: open  $Q_2$ .

### CHAPTER 12

- 12-1.** 680  $\Omega$ , 1.76 mA  
**12-3.** 10.62 V  
**12-5.** 10.62 V  
**12-7.** 50  $\Omega$ , 277 mA  
**12-9.** 100  $\Omega$   
**12-11.** 500  
**12-13.** 15.84 mA  
**12-15.** 2.2 percent

- 12-17.** 237 mA  
**12-19.** 3.3 percent  
**12-21.** 1.1 A  
**12-23.** 34 Vpp  
**12-25.** 7.03 W  
**12-27.** 31.5 percent  
**12-29.** 1.13 W  
**12-31.** 9.36  
**12-33.** 1679  
**12-35.** 10.73 MHz  
**12-37.** 15.92 MHz  
**12-39.** 31.25 mW  
**12-41.** 15 mW  
**12-43.** 85.84 kHz  
**12-45.** 250 mW  
**12-47.** 72.3 W  
**12-49.** Electrically, it would be safe to touch, but it may be hot and cause a burn.  
**12-51.** No, the collector could have an inductive load.  
**12-53.** Increase, increase, decrease, increase, no change  
**12-55.** Decrease, increase, decrease, increase, no change  
**12-57.** Increase, no change, no change, no change, increase  
**12-59.** Decrease, increase, no change, increase, decrease

### CHAPTER 13

- 13-1.** 15 G $\Omega$   
**13-3.** 20 mA, -4 V, 500  $\Omega$   
**13-5.** 500  $\Omega$ , 1.1 k $\Omega$   
**13-7.** -2 V, 2.5 mA  
**13-9.** 1.5 mA, 0.849 V  
**13-11.** 0.198 V  
**13-13.** 20.45 V  
**13-15.** 14.58 V  
**13-17.** 7.43 V, 1.01 mA  
**13-19.** -1.18 V, 11 V  
**13-21.** -2.5 V, 0.55 mA  
**13-23.** -1.5 V, 1.5 mA  
**13-25.** -5 V, 3200  $\mu$ S  
**13-27.** 3 mA, 3000  $\mu$ S  
**13-29.** 7.09 mV  
**13-31.** 3.06 mV  
**13-33.** 0 mVpp, 24.55 mVpp,  $\infty$   
**13-35.** 8 mA, 18 mA  
**13-37.** 8.4 V, 16.2 mV  
**13-39.** 2.94 mA, 0.59 V, 16 mA, 30 V  
**13-41.** Open  $R_1$   
**13-43.** Open  $R_D$   
**13-45.** Open G-S  
**13-47.** Open  $C_2$

**CHAPTER 14**

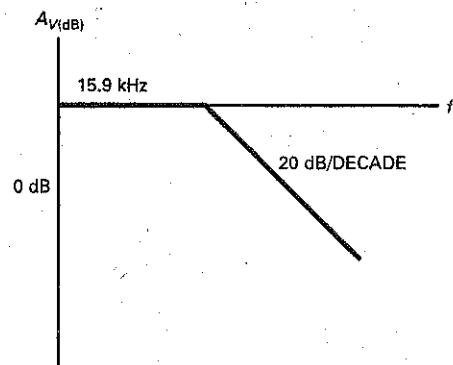
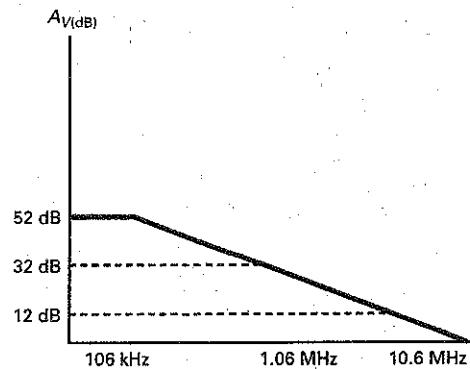
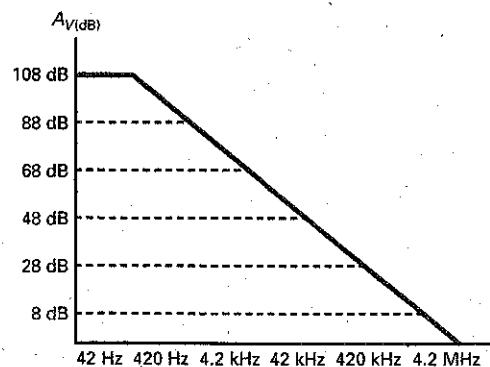
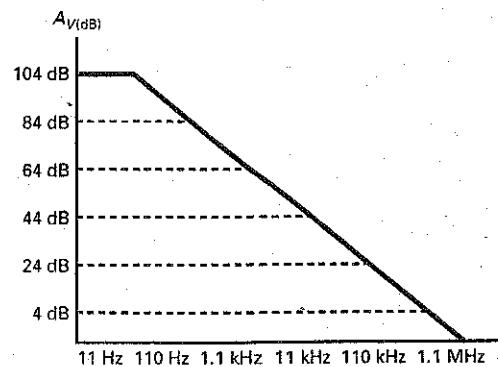
- 14-1. 2.25 mA, 1 mA, 250  $\mu$ A  
 14-3. 3 mA, 333  $\mu$ A  
 14-5. 381  $\Omega$ , 1.52, 152 mV  
 14-7. 1 M $\Omega$   
 14-9. a. 0.05 V; b. 0.1 V; c. 0.2 V;  
 d. 0.4 V  
 14-11. 0.23 V  
 14-13. 0.57 V  
 14-15. 19.5 mA, 10 A  
 14-17. 12 V, 0.43 V  
 14-19. A square-wave +12 V to  
 0.43 V  
 14-21. 12 V, 0.012 V  
 14-23. 1.2 mA  
 14-25. 1.51 A  
 14-27. 30.5 W  
 14-29. 0 A, 0.6 A  
 14-31. 20 S, 2.83 A  
 14-33. 24 mS, 3.14, 157 mV  
 14-35. 187.5 mS, 8.9, 446 mV

- CHAPTER 14**

- 14-37. 1.81 W  
 14-39. 10.5  $\mu$ A  
 14-41. 3 V  
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 15-1. 4.7 V  
 15-3. 0.1 msec, 10 kHz  
 15-5. 12 V, 0.6 ms  
 15-7. 7.3 V  
 15-9. 34.5 V, 1.17 V  
 15-11. 11.9 ms, 611  $\Omega$   
 15-13. +10°, +83.7°  
 15-15. 10.8 V  
 15-17. 12.8 V  
 15-19. 22.5 V  
 15-21. 30.5 V  
 15-23. 10 V  
 15-25. 10 V  
 15-27. 980 Hz, 50 kHz  
 15-29. T1: DE open; T2: no supply  
 voltage; T3: transformer;  
 T4: fuse is open.

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- 16-1. 196, 316  
 16-3. 19.9, 9.98, 4, 2  
 16-5. -3.98, -6.99, -10, -13  
 16-7. -3.98, -13.98, -23.98  
 16-9. 46 dB, 40 dB  
 16-11. 31.6, 398  
 16-13. 50.1  
 16-15. 41 dB, 23 dB, 18 dB  
 16-17. 100 mW  
 16-19. 14 dBm, 19.7 dBm, 36.9 dBm  
 16-21. 2  
 16-23. See Figure 1.  
 16-25. See Figure 2.  
 16-27. See Figure 3.  
 16-29. See Figure 4.  
 16-31. 1.4 MHz  
 16-33. 222 Hz  
 16-35. 284 Hz  
 16-37. 5 pF, 25 pF, 15 pF  
 16-39. gate: 30.3 MHz;  
 drain: 8.61 MHz

**Figure 1****Figure 2****Figure 3****Figure 4**

- 16-41. 40 dB  
16-43. 0.44  $\mu$ S

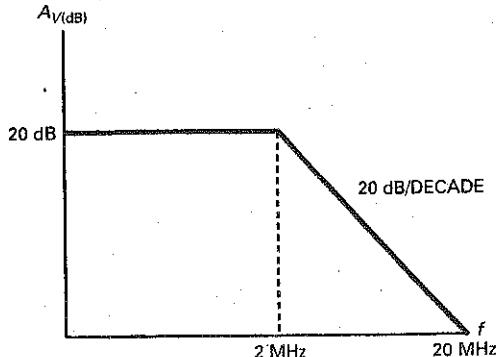
#### CHAPTER 17

- 17-1. 55.6  $\mu$ A, 27.8  $\mu$ A, 10 V  
17-3. 60  $\mu$ A, 30  $\mu$ A, 6 V (right), 12 V (left)  
17-5. 518 mV, 125 k $\Omega$   
17-7. -207 mV, 125 k $\Omega$   
17-9. 4 V, 1.75 V  
17-11. 286 mV, 2.5 mV  
17-13. 45.4 dB  
17-15. 237 mV  
17-17. Output will be high; needs a current path to ground for both bases.  
17-19. C  
17-21. 0 V  
17-23. 2 M $\Omega$   
17-25. 10.7  $\Omega$ , 187  
17-27.  $I_{B1}$ : increase, no change, increase, increase, no change;  $I_{B2}$ : no change, increase, increase, increase, no change  
17-29. Increase, increase, no change, no change, increase

#### CHAPTER 18

- 18-1. 170  $\mu$ V  
18-3. 19,900, 2000, 200  
18-5. 1.59 MHz  
18-7. 10, 2 MHz, 250 mVpp, 49 mVpp; See Figure 5.  
18-9. 40 mV  
18-11. 22 mV  
18-13. 50 mVpp, 1 MHz  
18-15. 1 to 51, 392 kHz to 20 MHz  
18-17. 188 mV/ $\mu$ s, 376 mV/ $\mu$ s  
18-19. 38 dB, 21 V, 1000

Figure 5



- 18-21. 214, 82, 177  
18-23. 41, 1  
18-25. 1, 1 MHz, 1, 500 kHz  
18-27. Go to positive or negative saturation.  
18-29. 2.55 Vpp  
18-31.  $I_{B1}$ : increase, no change, increase, increase, no change, no change; for  $I_{B2}$ : no change, increase, increase, no change, no change  
18-33. No change, no change, no change, no change, no change, increase

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- 19-1. 0.038, 26.32, 0.10 percent, 26.29  
19-3. 0.065, 15.47  
19-5. 470 M $\Omega$   
19-7. 0.0038 percent  
19-9. -0.660 Vpk  
19-11. 185 mA<sub>rms</sub>, 34.2 mW  
19-13. 106 mA<sub>rms</sub>, 11.2 mW  
19-15. 834 mA<sub>pp</sub>, 174 mW  
19-17. 2 kHz  
19-19. 15 MHz  
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19-25. 510 mV, 30 mV, 15 mV  
19-27. 110 mV, 14 mV, 11 mV  
19-29. 200 mV  
19-31. 2 k $\Omega$   
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19-35. T1: open between C and D; T2: shorted  $R_2$ ; T3: shorted  $R_4$   
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#### CHAPTER 20

- 20-1. 2, 10  
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20-5. 42, 71.4 kHz, 79.6 Hz  
20-7. 510 mV  
20-9. 4.4 mV, 72.4 mV  
20-11. 0, -10  
20-13. 15, -15  
20-15. -20,  $\pm 0.004$   
20-17. No  
20-19. -200 mV, 10,000  
20-21. 1 V  
20-23. 19.3 mV  
20-25. -3.125 V  
20-27. -3.98 V  
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20-37. -0.018, -0.99  
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20-43. 1 mA  
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#### CHAPTER 21

- 21-1. 7.36 kHz, 1.86 kHz, 0.25, wideband  
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b. narrowband; c. narrowband;  
d. narrowband  
21-5. 200 dB/decade, 60 dB/octave  
21-7. 503 Hz, 9.5  
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21-11. -21.4, 10.3 kHz  
21-13. 3, 36.2 kHz  
21-15. 15 kHz, 0.707, 15 kHz  
21-17. 21.9 kHz, 0.707, 21.9 kHz  
21-19. 19.5 kHz, 12.89 kHz,  
21.74 kHz, 0.8  
21-21. 19.6 Hz, 1.23, 18.5 Hz,  
18.5 Hz, 14.8 Hz  
21-23. -1.04, 8.39, 16.2 kHz  
21-25. 1.5, 1, 15.8 Hz, 15.8 Hz  
21-27. 127°  
21-29. 24.1 kHz, 50, 482 Hz  
(max and min)  
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21-33. 60 dB, 120 dB, 200 dB  
21-35. 148 pF, 9.47 nF

#### CHAPTER 22

- 22-1. 100  $\mu$ V  
22-3.  $\pm 7.5$  V

- 22-5. Zero, between 0.7 V and -9 V  
 22-7. -4 V, 31.8 Hz  
 22-9. 40.6 percent  
 22-11. 1.5 V  
 22-13. 0.292 V, -0.292 V, 0.584 V  
 22-15. Output voltage is low when the input voltage is between 3.5 and 4.75 V.  
 22-17. 5 mA  
 22-19. 1 V, 0.1 V, 10 mV, 1.0 mV  
 22-21. 0.782 V<sub>pp</sub> triangular waveform  
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 22-25. 923 Hz  
 22-27. 196 Hz  
 22-29. 135 mV<sub>pp</sub>  
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 22-51. 228,780 mi  
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 23-29. Shorted inductor, open inductor, shorted capacitors, open capacitors, open in the feedback path, loss of the power supply  
 23-31. One of many possible designs is  $C = 0.22 \mu\text{F}$ ,  $0.022 \mu\text{F}$ , and  $0.0022 \mu\text{F}$ . Change the 2 kΩ

in Fig. 23-53 to 3.3 kΩ and use a 50 kΩ potentiometer. Use a 1 kΩ potentiometer in place of the 1 kΩ in series with the lamp. Adjust 1 kΩ to get an output of 5 V<sub>rms</sub>.

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**CHAPTER 24**

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