	6502 / 65c02 / 6280 / 65816 Cheatsheet	Implied	Relative	Accumulator	Immediate #nn	Zero Page \$nn	Zero Page,X \$nn,X	Zero PG,Y \$nn,Y	Absolute \$0100	Absolute,X \$0100.X	Absolute,Y \$0100,Y	Abs,X Indir	Indirect (\$nnnn)	(Indirect,X) (\$nn,X)	(Indirect),Y (\$nn),Y		Absolute Long	Abs Indir Long	Direct Pg Indirect		Abs Long,X	(Long Indirect),Y	Stack Relative Sss.S	SR Indirect Indexed
		no params	jr	works on A	&nn	(&00nn)	(&00nn+X)	\$nn, Y (&00nn+Y)	(&0100)	(&0100+X)	(&0100+Y)	(\$nnnn,X) ((&nnnn+X))	((&nnnn))	((&00nn+X))	((&00nn)+Y)		\$100000 (\$100000)	[\$1000] ((\$1000))	(\$nn) (\$dpnn)	(\$nn) (\$dpdpnn)	(&010000+X)	((&dpdpnn)+Y)	(\$ss+8)	(\$ss,S),Y ((\$ss,S)+Y)
	Add with Carry Logical AND				\$69 2 2 \$29 2 2	\$65 2 3 \$25 2 3	\$75 2 4 \$35 2 4		\$6D 3 4 \$2D 3 4	\$7D 3 4/5 \$3D 3 4/5			\$72 3 \$32 3	\$61 2 6 \$21 2 6	\$71 2 5/6 \$31 2 5/6	Ovf7 2 +- 7	\$6F 3 4 \$2F 4 5		\$72 2 5 \$32 2 5		\$7F 4 5 \$3F 4 5		\$63 2 4 \$23 2 4	
ASL	Arithmetic Shift Left			\$0A 1 2		\$06 2 5	\$1626		\$0E 3 6	\$1E 3 7						7 Z 7							-	
	Branch if Carry Clear C=1 (Aka BLT) Branch if Carry Set C=0 (Aka BGE)		\$90 2 2/3/4 \$B0 2 2/3/4																					
BEQ	Branch if Equal to Zero (Z = 1 JP Z,)		\$F0 2 2/3/4																					
	Bit Test (And A with mem loc) Branch if Minus (S = 1)		\$30 2 2/3/4		\$89 2	\$24 2 3	\$34 2		\$2C 3 4	\$3C 3						- z 6 7								
BNE	Branch if Not Equal to Zero (Z = 0 JP NZ,)		\$D0 2 2/3/4																					
	Branch if Plus (S = 0) Break	\$00 1 7	\$10 2 2/3/4													=1								
BVC	Branch if Overflow Clear		\$50 2 2/3/4																					
BVS CLC	Branch if Overflow Set Clear Carry Flag		\$70 2 2/3/4													=0								
CLD	Clear Decimal Mode	\$D8 1 2														=0								
CLI	Clear Interrupt Mask (EI) Clear Overflow Flag	\$58 1 2 \$B8 1 2														=0								
CMP	Compare Accumulator to Memory				\$C9 2 2		\$D5 2 4		\$CD 3 4	\$DD 3 4/5	\$D9 3 4/5		\$D2 3	\$C1 2 6	\$D1 2 5/6	> = 7	\$CF 4 5		\$D2 2 5	\$C7 2 6	\$DF 4 5	\$D7 2 6	\$C3 2 4	\$D327
CPX CPY	Compare with Index Register X Compare with Index Register Y				\$E0 2 2 \$C0 2 2				\$EC 3 4 \$CC 3 4							> = 7								
DEC	Decrement (Aka DEA)			\$3A		\$C6 2 5	\$D6 2 6		\$CE 3 6	\$DE 3 7						- z 7								
DEX DEY	Decrement Index Register X Decrement Index Register Y	\$CA 1 2 \$88 1 2														- z 7								
EOR	Logical Exclusive-OR (XOR)	***			\$49 2 2	\$45 2 3	\$55 2 4		\$4D 3 4	\$5D 3 4/5	\$59 3/4/5		\$523	\$41 2 6	\$51 2 5/6	- z 7	\$4F 4 5		\$52 2 5	\$47 2 6	\$5F 4 5	\$57 2 6	\$43 2 4	\$53 2 7
INC	Increment (Aka INA) Increment Index Register X	\$E8 1 2		\$1A		\$E6 2 5	\$F6 2 6		\$EE 3 6	\$FE 3 7						- z 7 - z 7								
INY	Increment Index Register Y	\$C8 1 2														- z 7								
JMP JSR	Jump to New Location (or JML for long) Jump to Subroutine (or JSL for long)								\$4C 3 3 \$20 3 6	\$FC 3 8		\$7C 3	\$6C 3 5				\$5C 4 4 \$22 4 8	\$DC 3 6						
LDA	Load Accumulator				\$A9 2 2		\$B5 2 4		\$AD 3 4	\$BD 3 4/5			\$B2 3	\$A1 2 6	\$B1 2 5	- z 7	\$AF 4 5		\$B2 2 5	\$A7 2 6	\$BF 4 5	\$B7 2 6	\$A3 2 4	#B3 2 7
LDX LDY	Load Index Register X Load Index Register Y				\$A222 \$A022	\$A623 \$A423	\$B4 2 4	\$B6 2 4	\$AE 3 4 \$AC 3 4	\$BC 3 4/5	\$BE 3 4/5					- z 7								
LSR	Logical Shift Right (BitShift Right topbit 0)			\$4A 1 2	w.10 Z Z	\$46 2 5	\$56 2 6		\$4E 3 6	\$5E 3 7						- z 7								
NOP ORA	No Operation Logical (Inclusive) OR	\$EA 12			\$09 2 2	\$05 2 3	\$1524		\$0D 3 4	\$1D 3 4/5	\$10.3 4/5		\$123	\$0126	\$11 2 5/6	7	S0F 4 5		\$1225	\$07 2 6	\$1F 4 5	\$07 2 6	\$03.2.4	\$1327
PHA	Push Accumulator onto Stack (PUSH A)	\$48 1 3			ψυσ 2 2	ψυυ Δ 3	ψ10 2 4		ψUD 3 4	ψ10 3 4/5	9100410		9123	90120	ψ11∠ 3/0		9∪F 4 0		ψ1220	901 2 0	\$1F 4 0	φυι 20	903 Z 4	ψ10 2 1
	Push Processor Status (PUSH F) Pull Accumulator from Stack (POP A)	\$08 1 3 \$68 1 4																						
PLP	Pull Accumulator from Stack (POP A) Pull Processor Status (POP F)	\$68 1 4 \$28 1 4														- z 7								
ROL ROR	Rotate Left through Carry (RLCA) Rotate Right through Carry			\$2A 1 2 \$6A 1 2		\$26 2 5 \$66 2 5	\$36 2 6 \$76 2 6		\$2E 3 6 \$6E 3 6	\$3E 3 7 \$7E 3 7						old7 z 7								
	Rotate Right through Carry Return from Interrupt (RETI)	\$40 1 6		эUA 12		φυ0 ∠ 5	φι026		φυ⊑ 3 b	φ1 ⊑ 3 /						old0 z 7								
RTS	Return from Subroutine (RET) (or RTL for long)	\$60 1 6 \$6B 1 6																						
SBC	Subtract with Carry Set Carry (SCF)	\$38 1 2			\$E9 2 2	\$E5 2 3			\$ED 3 4	\$FD 3 4/5	\$F9 3 4/5		\$F23	\$E1 2 6	\$F1 2 5/6	Ovf7 z 7	\$EF 4 5		\$F2 2 5	\$E7 2 6	\$FF 4 5	\$F7 2 6	\$E3 2 4	\$F3 2 7
SED	Set Carry (3CF) Set Decimal Flag	\$F8 1 2														1								
	Set Interrupt Mask (Disable Interrupts) Store Accumulator	\$78 1 2				\$8523	\$9524		\$8D 3 4	\$9D 3 5	\$9935		\$923	\$8126	\$9126	1	\$8F 4 5		\$92 2 5	\$87 2 6	\$9F 4 5	\$97 2 6	602.0.4	\$93 \$2 7
STX	Store Index Register X					\$86 2 3	\$95 2 4	\$96 2 4		\$90.35	\$99.3.5		\$92.3	\$6126	\$9120		\$0F 4 5		\$92.25	\$67.20	\$9F 4 5	\$97.20	\$63 2 4	\$93 \$2 7
STY	Store Index Register Y Transfer Accumulator to Index Register X	\$AA 1 2				\$84 2 3	\$94 2 4		\$8C 3 4							7								
TAY	Transfer Accumulator to Index Register X Transfer Accumulator to Index Register Y	\$A8 1 2														- z 7								
TSX TXA	Transfer Stack Pointer to X (LD X,SP) Transfer Index Register X to Accumulator	\$BA 1 2 \$8A 1 2														- z 7								
TXS	Transfer X to Stack Pointer (LD SP,X)	\$9A 1 2														- 2 7								
TYA	Transfer Index Register Y to Accumulator	\$98 1 2	\$80.2													- z 7								
BRA	Branch Relative Always (JR) (BRL for long) Coprocessor Enable	\$02 2 7	\$82 3 4													ID								
MVN	Block Move Next (LDIR) MVN M,N A bytes from MX->NY (Alters DBR)	\$UZ Z T			\$54 3 ?																			
MVP	Block Move Previous (LDDR) MVP M,N A bytes from MX→NY (Alters DBR)				\$443?																			
PEA PEI	Push Effective Absolute address Push Effective Indirect Address							\$F4 3 5											an 4 a a					
PER	Push effective PC Relative Indirect Address		\$62 3 6																\$D4 2 6					
PHB PHD	Push 8 bit Data Bank Reg (DBR) Push 16bit Direct Page Register	\$8B 1 3 \$0B 1 4																						
PHK	Push 8 bit Program Bank Register (PBR)	\$4B 1 3																						
PHX PHY	Push X Push Y	\$DA 1 \$5A 1																						
PLB	Pull 8 bit Data Bank Reg (DBR)	\$AB 1 4														- z 7								
PLD PLX	Pull 16bit Direct Page Register Pull X	\$2B 1 5 \$FA 1														- z 7								
PLY	Pull Y	\$7A 1														- z 7								
REP SEP	Reset Status Bits Set Status Bit				\$C223 \$E223											,,,,,,,,								
STP	Stop processor until next RST	\$DB 1																						
STZ TCD	Store Zero to address Transer Accumulator to the Direct page register (aka TAD)	\$5B 1 2				\$64 2	\$74.2		\$9C 3	\$9E 3						- 2 7								
TDC	Transfer Direct Page register to the Accumulator (aka TDA)	\$7B 1 2														- z 7								
TCS TRB	Transfer Accumulator to SP (aka TAS) Test and Reset Bits with A	\$1B 1 2				\$14.2			\$1C 3							- z 7								
TSB	Test and Set Bits with A					\$04.2			\$0C 3							- z								
TSC	Transfer SP to Accumulator (aka TSA) Transfer X to Y	\$3B 1 2 \$9B 1 2														- z 7								
TYX	Transfer Y to X	\$BB 1 2														- z 7								
WAI WDM	Wait until any interrupt Reseverd for future use!	\$CB 1 \$42 2																						
XBA	Exchange A and B (aka SWA)	\$EB 1 3														- z 7								
XCE BBR	Exchange Carry (C) and Emu bits (E) Branch if bit n is Reset (also some 65c02)	\$FB 1 2				\$0f-\$7F 2										Еив								
BBS	Branch if bit n is Reset (also some 65c02)					\$8f-\$FF 2										D								
	Branch to subroutine (Call Relative) Clear X	\$44 2 8 \$82 1 2																						
CLY	Clear Y	\$C2 1 2																						
CSH	Change Speed High (7.16 MHz) Change Speed Low (1.78 MHz)	\$D4 1 3 \$54 1 3																						
RMB	Reset Memory Bit n (also some 65c02)					\$07-\$77																		
SAX	Swap A and X Swap A and Y	\$22 1 3 \$42 1 3																						
SET	Set T flag	\$4213 \$F412																						
SMB ST0	Set Memory Bit n (also some 65c02)					\$87-\$F7																		
ST1	ST0 - Store (HuC6270) VDC No. 0 ST1 - Store (HuC6270) VDC No. 1				\$03 2 5 \$13 2 5																			
ST2	ST2 - Store (HuC6270) VDC No. 2	600.4.0			\$23 2 5																			
SXY TAI	Swap X and Y registers Transfer Alternate Increment	\$02 1 3			\$F3 7 17+																			
TAM TIA	Tranfer Accumulator to MPR				\$53 2 5																			
TII	Transfer Increment Alternate Transfer Increment Increment				\$E3 7 17+ \$73 7 17+																			
TIN TMA	Transfer Increment				SD3 7 17+																			
TST	Tranfer MPR to Accumulator Test Bits at n2 witn n1				\$43 2 4	\$83 3 7	\$A3 3 7	\$93 4 8	\$B3 4 8															
	http://www.LearnAsm.net	>=6502	65C02, 658	316, 6280	65C02,					65816	65816		16 bit in	n 65816 M	=0 / X=0									