

digital

LOGIC HANDBOOK

Modules



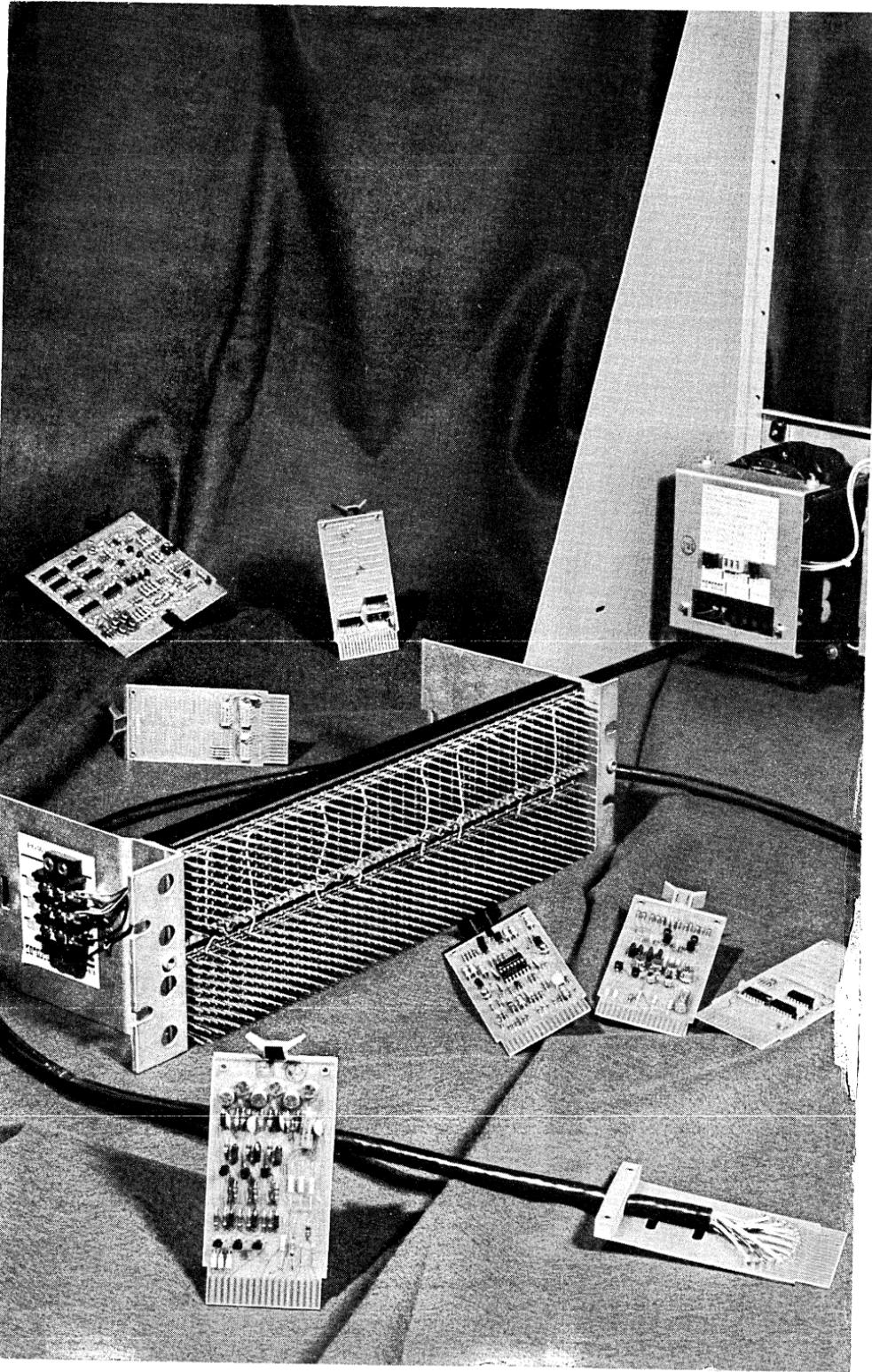
Hardware



Applications



Positive Logic Edition



THE
digital
LOGIC HANDBOOK
FLIP CHIP™ MODULES
1969 EDITION

POSITIVE LOGIC EDITION

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Maynard, Massachusetts**

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M SERIES

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K SERIES

A SERIES

POWER SUPPLIES

PART II HARDWARE

HARDWARE

ACCESSORIES

M SERIES

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FOREWORD

This fifth edition of the Logic Handbook is your guide to the most extensive array of logic capabilities, hardware and applications information ever offered by Digital Equipment Corporation. Here you will find a wealth of useful information on the latest techniques and products available for implementing your electronic logic designs for instrumentation computer interfacing, data gathering, or control. The handbook is a basic reference for anyone involved in specifying, designing, manufacturing or using solid state logic.

The Products

Two of our major module lines are featured in this edition: M Series TTL integrated circuit modules and K Series low-speed noise-immune logic. The M Series line has now been expanded to over 60 modules. In addition to a comprehensive array of basic logic and functional modules, the general-purpose M Series line now offers seven new computer interfacing modules to augment its already broad interfacing capabilities. The K Series product offering has also been expanded, and now comprises nearly 60 modules, all compatible with M Series. Complementing its basic logic, expanded K Series offers specialized functional modules such as sensor converters, communications interfaces, 120 V ac interfaces, drivers for solenoids and motors, and logic level converters for tying either high-speed or noise-sensitive logic to other devices.

Fifteen A Series analog/digital modules are also described, including seven functionally complete digital-to-analog converter modules.

As the cost of the logic itself decreases, it becomes increasingly important that efficient, reliable and inexpensive hardware be available to keep total system costs down. DIGITAL provides this hardware. Now, from a few to thousands of modules can be connected, wired, mounted, power and enclosed efficiently with the lowest cost per function in the industry.

DIGITAL's complete line of power and hardware accessories provides everything needed to put your designs into action, from connector blocks to mounting cabinets. Seven power supplies, six connector block variations, ten mounting panels, twelve blank module configurations and five types of connector cards are among the well over 100 different hardware and accessory items described in this edition of the Logic Handbook.

Over 35 applications notes and dozens of useful design notes have been included to help you easily design custom systems, making this one of the most informative electronic handbooks available. The application information is accessible through subject index in the back or by using the thumb index on page iii.

The Company

In a little over ten years, Digital has become a major force in the electronics industry. The company has grown from three employees and 8,500 square feet of production floor space in a converted woolen mill in Maynard, Massachusetts, to an international corporation employing more than 3,000 people with over one million square feet of floor space in a dozen buildings around the world. From its beginnings as a manufacturer of digital modules, the company has now grown to the point where it is the world's largest manufacturing supplier of logic modules and the fourth largest computer manufacturer in the industry.

DIGITAL's rise as a leader in the electronics industry began in 1957 with the introduction of the company's line of electronic circuit modules. These solid state modules were used to build and test other manufacturers' computers. A year later, DIGITAL introduced its first computer, the PDP-1. The PDP-1 heralded a new concept for the industry—the small, on-line computer. And the PDP-1 was inexpensive—it sold for \$120,000 while competitive machines with similar capabilities were selling at over \$1 million. But the PDP-1 was more than a data processor; more than just a tool to manipulate data. It was a system that could be connected to all types of instrumentation and equipment for on-line, real-time monitoring, control and analysis. It was a system with which people and machines could interact.

Also, in 1958, DIGITAL introduced the Systems Module, a high-quality, low cost solid state digital logic circuit on a single printed circuit card. Today, electronic modules, like the ones DIGITAL introduced, are used in most electronic equipment, from computers to television sets.

In 1965, DIGITAL announced the first of the FLIP CHIP modules lines. These highly reliable modules include cards for internal computer logic, interfacing, control and analog-to-digital conversion.

About a year ago, DIGITAL announced the newest additions to the FLIP-CHIP family: M Series high-speed integrated circuit modules and K Series noise-immune modules.

This year, DIGITAL introduced the PDP-1's grandson, the PDP-8/L. It is a small computer with far greater capabilities than the PDP-1 and a price tag of only \$8,500.

DIGITAL produces almost two million modules a year, making it the world's largest manufacturing supplier of logic modules. DIGITAL sales engineers in over 50 offices around the world and our applications engineering staff at the home office are ready to help you with your more difficult or complex applications. They are all listed on the inside back cover. Give us a call.

March, 1969

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WARRANTY

WARRANTY 1. B, R, W, M, K, AND A MODULES — All B, R, W, M, K, and A modules shown in Catalogs C-105, or C-110 as revised from time to time, are warranted against defects in workmanship and material under normal use and service for a period of ten years from date of shipment providing parts are available. DEC will repair or replace any B, R, W, M, K, or A modules found to be defective in workmanship or material within ten years of shipment for a handling charge of \$5.00 or 10% of list price per unit, whichever is higher. Handling charges will be applicable from one year after delivery.

WARRANTY 2. SYSTEM MODULES, LABORATORY MODULES, HIGH CURRENT PULSE EQUIPMENT, G, S, H, NON-CATALOG FLIP-CHIP MODULES AND ACCESSORIES — All items referenced are warranted against defects in workmanship and material under normal use service for a period of one year from date of shipment. DEC will repair or replace any of the above items found to be defective in workmanship or material within one year of shipment. Handling charges will be applicable from one year after delivery with handling charges varying depending on the complexity of the circuit.

The Module Warranty outside the continental U.S.A. is limited to repair of the module and excludes shipping, customer's clearance or any other charges.

Modules must be returned prepaid to DEC. Transportation charges covering the return of the repaired modules shall be paid by DEC. DEC will select the carrier, but by so doing will not thereby assume any liability in connection with the shipment nor shall the carrier be in any way construed to be the agent of DEC. Please ship all units to:

**Digital Equipment Corporation
Module Marketing Services
Repair Division
146 Main Street
Maynard, Mass. 01754**

No module will be accepted for credit or exchange without the prior written approval of DEC, plus proper Return Authorization Number (RA#).

All shipments are F.O.B. Maynard, Massachusetts, and prices do not include state or local taxes.
Prices and specifications are subject to change without notice.

QUANTITY DISCOUNTS

\$5,000 — 3%; \$10,000 — 5%; \$20,000 — 10%; \$40,000 — 15%;

\$70,000 — 18%; \$100,000 — 20%; \$250,000 — 22%; \$500,000 — 25%

Discounts apply to any combination of FLIP CHIP Modules

PART I
M
SERIES

INTRODUCTION

The development of monolithic integrated circuits has had an impact on the design of digital module systems. Advantages of small size and high operating speeds made these circuits initially attractive. However, a lower price/performance ratio compared to hybrid or discrete component modules offset the advantages. Recently, significant price reductions in both TTL (transistor-transistor logic) and DTL (diode-transistor logic) integrated circuits indicated a re-evaluation was needed.

DIGITAL EQUIPMENT CORPORATION undertook a study of both types of logic, their performance in large and small systems, and their ease of use in system design. The result of this study is the M Series Integrated Circuit FLIP CHIP™ Module.

M Series modules contain high speed TTL logic in both general purpose and functional logic arrays. TTL was chosen for its high speed, capacitance drive capability, high noise immunity and choice of logical elements. High performance integrated circuit modules are now available at approximately one half the price of their discrete or hybrid counterparts.

In addition to the reduced cost of integrated circuits, Digital's advanced manufacturing methods and computer controlled module testing have resulted in considerable production cost savings, reflected in the low price of all M Series Modules.

GENERAL CHARACTERISTICS

M Series high-speed, monolithic integrated circuit logic modules employ TTL (transistor-transistor logic) integrated circuits which provide high speed, high fan out, large capacitance drive capability and excellent noise margins. The M Series includes a full digital system complement of basic modules which are designed with sufficient margin for reliable system operation at frequencies up to 6 MHz. Specific modules may be operated at frequencies up to 10 MHz. The integrated circuits are dual in-line packages.

The M Series printed circuit boards are identical in size to the standard FLIP CHIP™ modules. The printed circuit board material is double-sided providing 36-pins in a single height module. Mounting panels (H910 and H911) and 36-pin sockets (H803 and H808) are available for use with M Series modules. Additional information concerning applicable hardware may be found in the Power Supply & Hardware and Accessories section of this handbook.

M Series modules are compatible with Digital's K Series and, through the use of level converters, are compatible with all of Digital's other standard negative voltage logic FLIP CHIP™ modules.

OPERATING CHARACTERISTICS

Power Supply Voltage: 5 volts \pm 5%

Operating Temperature Range: 0° to 70°C

Speed: M Series integrated circuit modules are rated for operation in a system environment at frequencies up to 6 MHz. Specific modules may be operated at higher frequencies as indicated by the individual module specifications.

Noise Immunity: Typical DC noise margin is 1 volt at either the logic 1 or the logic 0 level. Worst case noise margin is 400 millivolts at either level when full fan-out is employed. Reduced fanout will generally enhance the noise margin.

Logic Levels: Logic levels, unless otherwise specified, are as follows:

	Outputs	Inputs
Logic 1 or High (H)	> +2.4 volts	< +2.0 volts
Logic 0 or Low (L)	< +0.4 volts	> +0.8 volts

The above is consistent with the loading specifications for M Series modules.

Input and Output Loading: The input loading and output drive capability of M Series modules are specified in terms of a specific number of unit loads. Typically the input loading is one unit, however certain modules may contain inputs which will present greater than one unit load. The typical M Series module output will supply 10 unit loads of input loading. However, certain module outputs will deviate from a 10 unit load capability and provide more or less drive. Always refer to the individual module specifications to ascertain actual loading figures.

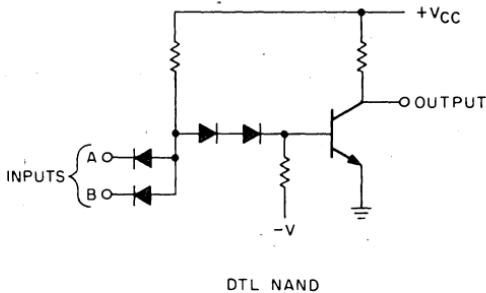
Unit Load: In the logic 0 state, one unit load requires that the driver be able to sink 1.6 millamps (maximum) from the load's input circuit while maintaining an output voltage of equal to or less than +0.4 volts. In the logic 1

state, one unit load requires that the driver supply a leakage current 40 microamps (maximum) while maintaining an output voltage of equal to or greater than +2.4 volts.

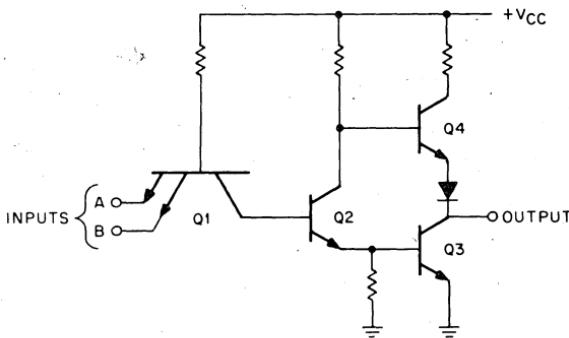
TIMING: M Series pulse sources provide sufficient pulse duration to trigger any M Series flip-flop operating within maximum propagation delay specifications. Detailed timing information appears later in this section and in the module specifications.

TTL NAND GATE

The basic gate of the M Series is a TTL NAND gate. Operation of the TTL gate is similar in many respects to the familiar DTL (diode-transistor logic) NAND gate. The two circuits are compared in Figure 1.



DTL NAND



TTL NAND

Figure 1. Schematic Comparison of DTL and TTL NAND gates

Both approaches provide the NAND function, in which the output, C, is low when both inputs (A and B) are high.

Logic Levels: Operating from a power supply voltage of +5 vdc $\pm 5\%$, the TTL NAND gate develops the following nominal logic levels at the loading extremes:

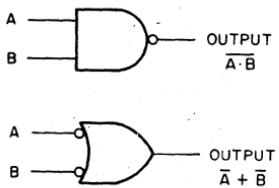
Logic Level	Voltage, No Load	Voltage, Full Load
1 (High) (H)	+3.6	+2.4
0 (Low) (L)	0.1	+0.4

Circuit Operation: The input element of the TTL gate is a multiple-emitter transistor which performs the same basic function as the input diodes of the DTL gate. When both inputs are high, the collector of transistor Q1 is high, turning on the phase-splitter, Q2. The phase-splitter turns on output switching transistor Q3, which permits the flow of load current. During the power driving state, the output is clamped near ground potential. Transistor Q4 is turned off during this state and is effectively out of the circuit.

When either of the inputs returns to the low level, the collector of the input transistor goes low, turning off the phase-splitter. The output transistor Q3, is turned off, ending the load current drain, and transistor Q4 is turned on to return the output line rapidly toward Vcc. Leakage current through the emitter of the driven gate is supplied by Q4 during the off state.

Output recovery time is speeded by the "totem pole" output circuit, which provides a practical output impedance of about 100 ohms compared to the typical DTL "pullup" resistor of 4 to 6 K ohms. This feature significantly reduces noise pickup through capacitive or inductive coupling.

NAND Logic Symbol: Logic symbology used to describe M Series modules is based on widely accepted standards. Logic symbols and a truth table for the NAND gate are shown in Figure 2.



A	B	OUTPUT
L	L	H
L	H	H
H	L	H
H	H	L

Figure 2. NAND Gate Logic Symbol and Truth Table

The first symbol is visually more effective in applications where two high inputs are ANDed to produce a low output. The second symbol better represents an application where low inputs are ORed to produce a high output.

TTL AND/NOR GATE

With a few modifications, the basic TTL NAND gate can perform an AND/NOR function useful in exclusive OR, coincidence, line selection and NOR gating operations. The modified circuit is shown in simplified form in Figure 3.

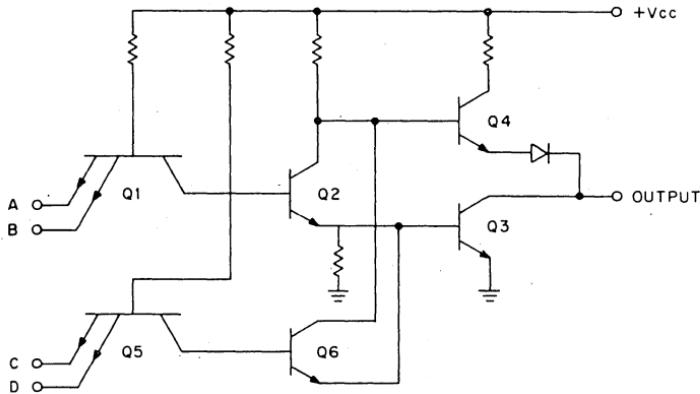


Figure 3. TTL AND/NOR Gate Simplified Schematic

Circuit Operation: The basic elements of the TTL NAND gate are used without modification. The phase-splitter (Q2) is paralleled with an identical transistor (Q6), also controlled by multiple-emitter input transistor which receives two additional inputs, C and D. When either of the input pairs are high, the phase inverter operates to switch the output voltage low. Circuit performance is essentially identical to the TTL NAND circuit.

AND/NOR Logic Symbol: The logic symbols for the AND/NOR gate are shown and defined in Figure 4.

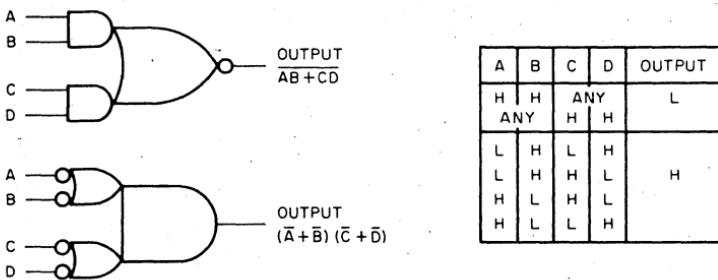
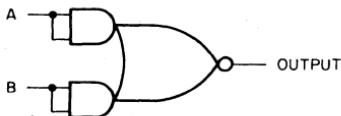
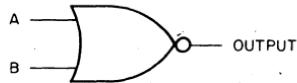


Figure 4. AND/NOR Gate Logic Symbols and Truth Table

NOR Configuration: The AND/NOR gate can perform a straight NOR function if the AND gate inputs are tied together as shown in Figure 5:



AND/NOR INPUTS TIED

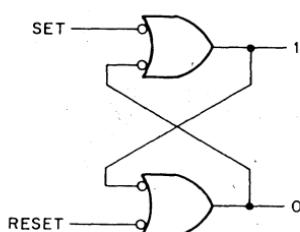


RESULTING NOR SYMBOL

Figure 5. NOR Connection of AND/NOR Gate

NAND GATE FLIP-FLOPS

RS Flip-Flop: A basic Reset/Set flip-flop can be constructed by connecting two NAND gates as shown in Figure 6.



PREVIOUS STATE		INPUT CONDITION		RESULT	
1	0	SET	RESET	1	0
L	H	L	H	H	L
H	L	H	L	L	H
L	H	H	H	NO CHANGE	
H	L	H	H	NO CHANGE	
H	L	L	H	NO CHANGE	
L	H	H	L	NO CHANGE	
L	H	L	L	H	H*
H	L	L	L	H	H*

Ambiguous state: In practice the input that stays low longest will assume control.

Figure 6. RESET/SET NAND Gate Flip-Flop

CLOCKED NAND GATE FLIP-FLOPS

The Reset-Set flip-flop can be clock-synchronized by the addition of a two-input NAND gate to both the set and the reset inputs. (See Figure 7.) One of the inputs of each NAND is tied to a common clock or trigger line.

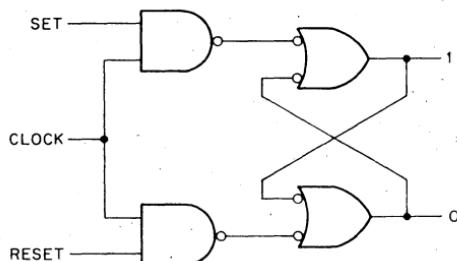


Figure 7. Clocked NAND Gate Flip-Flop

A change of state is inhibited until a positive clock pulse is applied. The ambiguous case will result if both the set and reset inputs are high when the clock pulse occurs.

M SERIES GENERAL-PURPOSE FLIP-FLOPS

Two types of general-purpose flip-flops are available in the M Series, both of which have built-in protection against the ambiguous state characteristic of NAND gate flip-flops.

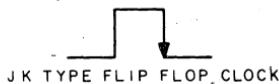
FLIP-FLOP CLOCK INPUT SYMBOLS

The D type flip-flop is a true leading (positive going voltage) edge triggered flip-flop and the D input is locked out until the clock input returns to low. The symbol to indicate this function will be as follows;



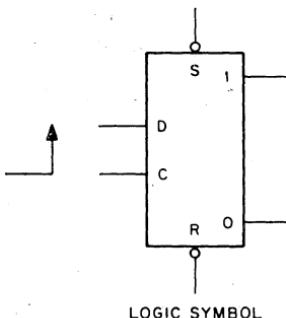
D TYPE FLIP FLOP CLOCK

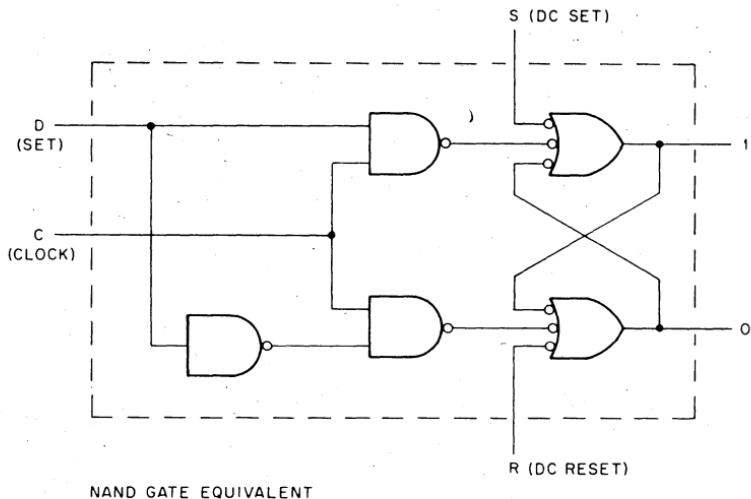
The operation of the J-K type flip-flop is to transfer the information present at the J and K inputs just prior to and during the clock pulse to the master flip-flop when the threshold is passed on the leading (positive going voltage) edge of the clock pulse. The information stored in the master flip-flop is transferred to the slave flip-flop, and consequentially to the outputs, when the threshold is passed on the trailing (negative going voltage) edge of the clock pulse. The symbol to indicate this function will be as follows;



J K TYPE FLIP FLOP CLOCK

D Type Flip-Flop: The first of these is the D type flip-flop shown in Figure 8. In this element, a single-ended data input (D) is connected directly to the set gate input. An inverter is provided between the input line (D) and the reset input. This ensures that the set and reset levels cannot be high at the same time.





SIMPLIFIED NAND GATE EQUIVALENT

Figure 8. D Type General Purpose Flip-Flop

The flip-flop proper employs three-input NAND gates to provide for dc set and reset inputs.

D type flip-flops are especially suited to buffer register, shift register and binary ripple counter applications. Note that D type devices trigger on the leading (or positive going) edge of the clock pulse. Once the clock has passed threshold, changes on the D input will not affect the state of the flip-flop due to a lockout circuit (not shown).

A characteristic of the D type flip-flop which is not illustrated in the NAND gate equivalent circuit is the fact that the D input is locked out after the clock input threshold voltage on the leading (positive going voltage) edge of the clock has been passed. The D input is not unlocked until the clock input threshold voltage of the trailing (negative going voltage) edge has been passed.

"MASTER-SLAVE J-K FLIP-FLOP"

The two unique features of a J-K flip-flop are: A) a clock pulse will not cause any transition in the flip-flop if neither the J nor the K inputs are enabled during the clock pulse, and B) if both the J and the K inputs are enabled during the clock pulse, the flip-flop will complement (change states). There is no indeterminate condition in the operation of a J-K flip-flop.

A word of caution is in order concerning the clock input. The J and K inputs must not be allowed to change states when the clock line is high, the output will complement on the negative going voltage transition of the clock. It is for this reason that the clock line must be kept low until it is desired to transfer information into the flip-flop and no change in the states of the J and K inputs should be allowed when the clock line is high.

The J-K flip-flops used are master-slave devices which transfer information to the outputs on the trailing (negative going voltage) edge of the clock pulse. The J-K flip-flop consists of two flip-flop circuits, a master flip-flop and a slave flip-flop. The information which is present at the J and K inputs when the leading edge threshold is passed and during the clock high will be passed to the master flip-flop (The J and K inputs must not change after the leading edge threshold has been passed). At the end of the clock pulse when the threshold of the clock is passed during the trailing (negative going voltage) edge, the information present in the master flip-flop is passed to the slave flip-flop. If the J input is enabled and the K input is disabled prior to and during the clock pulse, the flip-flop will go to the "1" condition when the trailing edge of the clock occurs. If the K input is enabled and the J input is disabled prior to and during the clock pulse, the flip-flop will go to the "0" condition when the trailing edge of the clock pulse occurs. If both the J and K inputs are enabled prior to and during the clock pulse, the flip-flop will complement when the trailing edge of the clock pulse occurs. If both the J and K inputs are disabled prior to and during the clock pulse, the flip-flop will remain in whatever condition existed prior to the clock pulse when the trailing edge of the clock pulse occurs.

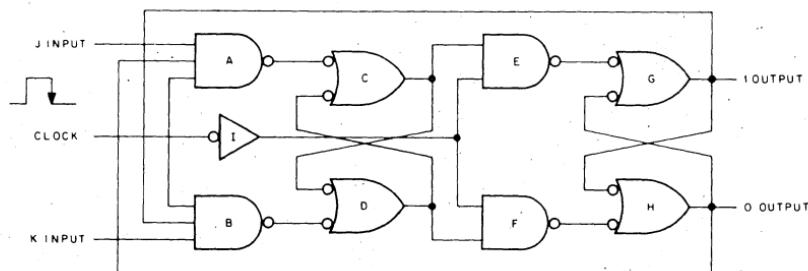


Figure 9. Master-Slave-J-K Flip-Flop

Figure 10 shows a functional block diagram of a master slave J-K flip-flop using NAND gates. Gates C and D are the master flip-flop. Gates G and H are the slave flip-flop. Gates A and B are the steering network of the master flip-flop and the steering network for the slave flip-flop is comprised of gates E, F, and I. The 1 output of the master flip-flop is point X. The operation of the flip-flop will be studied by examining the "1" to "0" transition of the flip-flops, with both the J and the K inputs enabled with a HI level before the clock pulse. When the leading edge of a HI clock pulse occurs, gate B will be enabled with three HI inputs. This will provide a RESET signal for the master flip-flop which will then go to the "0" condition. The slave flip-flop remains in the "1" condition while the clock pulse is HI because gate I is providing a LO signal to both gates E and F, thereby blocking inputs to the slave flip-flop. When the trailing edge of the clock pulse occurs, gate F will be enabled with a HI level at both its inputs and a RESET signal will be provided to the slave flip-flop, which will then go to the "0" condition. The next clock pulse, with both the J and K enabled, would cause the master flip-flop to go to the "1" condition on the leading edge of the clock pulse and cause the slave flip-flop to go to the "1" condition on the trailing edge of the pulse. Figure 10 is a truth table for the J-K flip-flop showing all eight possible initial conditions.

INITIAL CONDITIONS		INPUTS		FINAL CONDITIONS	
OUTPUTS		J	K	OUTPUTS	
1	0	J	K	1	0
LO	HI	LO	LO	LO	HI
LO	HI	LO	HI	LO	HI
LO	HI	HI	LO	HI	LO
LO	HI	HI	HI		
HI	LO	LO	LO		
HI	LO	LO	HI		
HI	LO	HI	LO		
HI	LO	HI	HI		

Figure 10. Master-Slave J-K Flip-Flop Truth Table

UNUSED INPUTS (GATES AND FLIP-FLOPS)

Since the input of a TTL device is an emitter of a multiple-emitter transistor, care must be exercised when an input is not to be used for logic signals. These emitters provide excellent coupling into the driving portions of the circuit when left unconnected. To insure maximum noise immunity, it is necessary to connect these inputs to a source of Logic 1 (High). Two methods are recommended to accomplish this:

1. Connect these inputs to a well filtered and regulated source of +3 volts. Pins U1 and V1 are provided on the M113, M117, M119, M121, M617, and M627 for this purpose.
2. Connect these inputs to one of the active inputs on the same gate. This results in a higher leakage current due to the parallel emitters and should be considered as an additional unit load when calculating the loading of the driving gate.

Connection of unused inputs to the supply voltage, V_{cc} , is not advisable, since power supplies are subject to transients and voltage excursions which could damage the input transistor.

TIMING CONSIDERATIONS

Standard Timing Pulse: In digital system design, a reference for system timing is usually required. The M Series modules M401 or M405 produces a standard pulse which provides such a reference. The standard pulse derived from each of these two modules is shown in Figure 11.

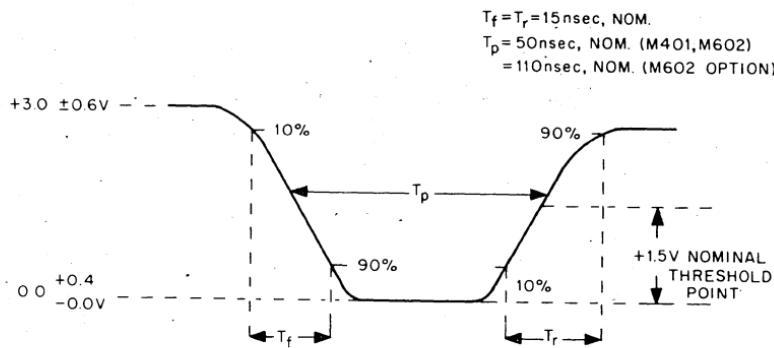


Figure 11. Standard Pulse

NAND Gate and Power Amplifier Propagation Delays: The standard pulse (Figure 11) is distributed throughout a system in negative form to maintain the leading edge integrity. (Since the TTL gate drives current in the logic 0 state, the falling edge is more predictable for timing purposes.) However, the standard pulse is of the wrong polarity for use as a clocking input to the type D and J-K flip-flops, requiring the use of a local inverter. Ordinarily, a NAND inverter is adequate. Where high fan-out is necessary, a M617 Power NAND is preferred.

For applications requiring both high fan-out and critical timing the M627 Power Amplifier is available. This module contains extremely high-speed gates which exhibit turn-on times differing by only a few nanoseconds.

Simultaneity is desirable in clock or shift pulses distributed to extended shift registers or synchronous counters.

Delays introduced by inverting gates and power amplifiers are illustrated in Figure 12. (Delays are measured between threshold points.)

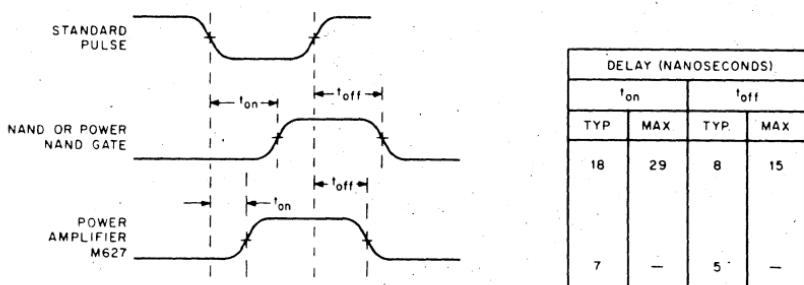


Figure 12. NAND Gate and Power Amplifier Delays

Flip-Flop Propagation Delays: D type flip-flops trigger on the leading edge of a positive clock pulse; the propagation delay is measured from the threshold point of this edge. The set-up time of the D flop is also measured from this threshold point. Data on the D input must be settled at least 20 nanoseconds prior to the clock transition. The advantage of the D-flip-flop, however, is that the leading edge triggering allows the flip-flop AND gates to propagate while the clock pulse is still high. Figure 13 illustrates this situation.

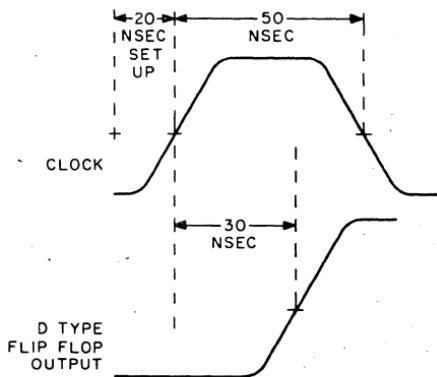


Figure 13. D Type Flip-Flop Timing

JK type flip-flops are, in effect, trailing edge triggering devices as explained previously. The only restriction on the J and K inputs is that they must be settled by the time that the rising edge occurs. Timing is shown in Figure 14.

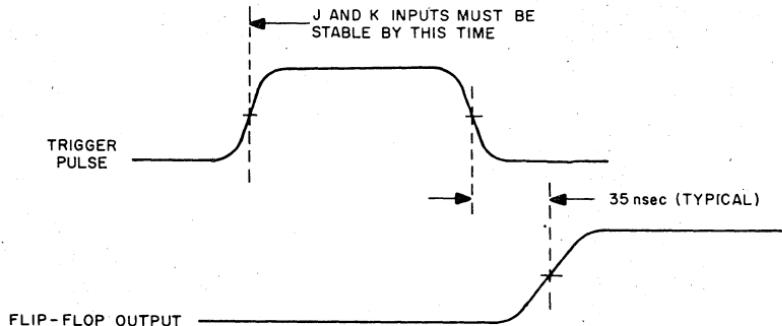


Figure 14. J-K Flip-Flop Timing

When using the dc Set or Reset inputs of either flip-flop type, propagation delays are referenced to the falling edge of the pulse. This is due to the inverted sense of these inputs. When resetting ripple type counters (where the output of one flip-flop is used as the trigger input to the next stage) the reset pulse must be longer than the maximum propagation delay of a single stage. This will ensure that a slow flip-flop does not introduce a false transition, which could ripple through and result in an erroneous count.

One-Shot Delay: Calibrated time delays of adjustable duration are generated by the M302 Delay Multivibrator. When triggered by a level change from a logical one to a logical zero, this module produces a positive output pulse that is adjustable in duration from 50 to 750 nsec with no added capacitance. Delays up to 7.5 milliseconds are possible without external capacitance. (See M302 specification.) Basic timing and the logic symbol are shown in Figure 15. The 100 picofarad internal capacitance produces a recovery time of 30 nsec. Recovery time with additional capacitance can be calculated using the formula;

$$t_r \text{ Nanoseconds} = \frac{30 \text{ C Total (Picofarads)}}{100}$$

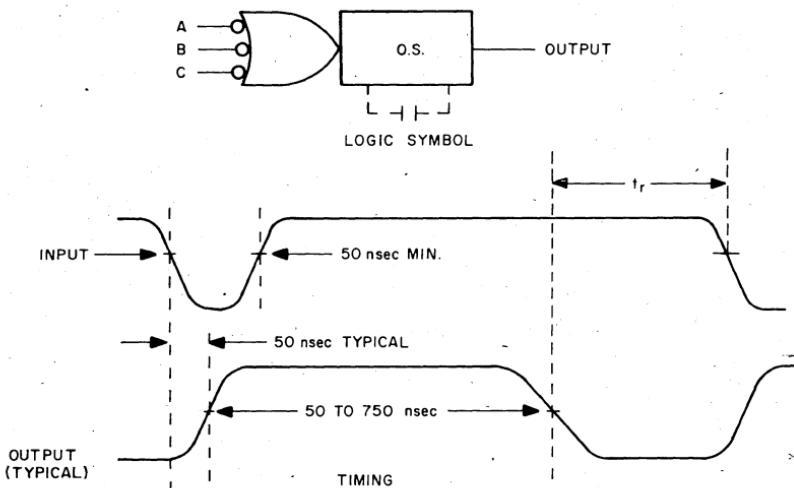


Figure 15. One-Shot Delay Timing and Logic Symbol

SYSTEM OPERATING FREQUENCY

Although individual propagation delays are significant in the design of digital logic, even more important is the maximum operating frequency of a system which is composed of these individual modules. Specifically designed systems may be operated at 10 MHz, but a more conservative design may result in a somewhat lower operating speed. M Series modules can be designed into a system with a 6 MHz clock rate with relative ease. This system frequency is derived by summing the delays in a simple logic chain:

1. A standard clock pulse width of 50 nsec is assumed. This period is measured from the threshold point of the leading edge to the threshold point of the trailing edge.
2. One flip-flop propagation delay of 35 nsec from the trailing edge of the clock pulse to the threshold point of the final state of the flip-flop is allowed.
3. Two gate-pair delays of 30 nsec each are assumed. (A gate-pair consists of two inverting gates in series.) Two gate-pair delays are usually required to perform a significant logic function with a minimum of parallel operations. The two gate-pair delays total 60 nsec.

The time necessary to perform these operations before the next occurrence of the clock pulse is the sum of the delays; $50 + 35 + 60$, or 145 nsec. Allowing 20 nsec for variations within the system, the resulting period is 165 nsec, corresponding to a 6 MHz clock rate. This timing is demonstrated in Figure 16.

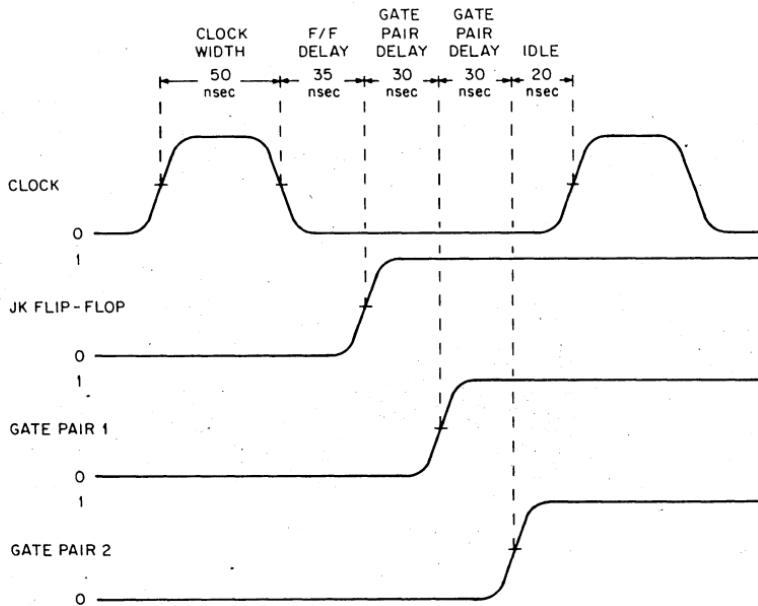
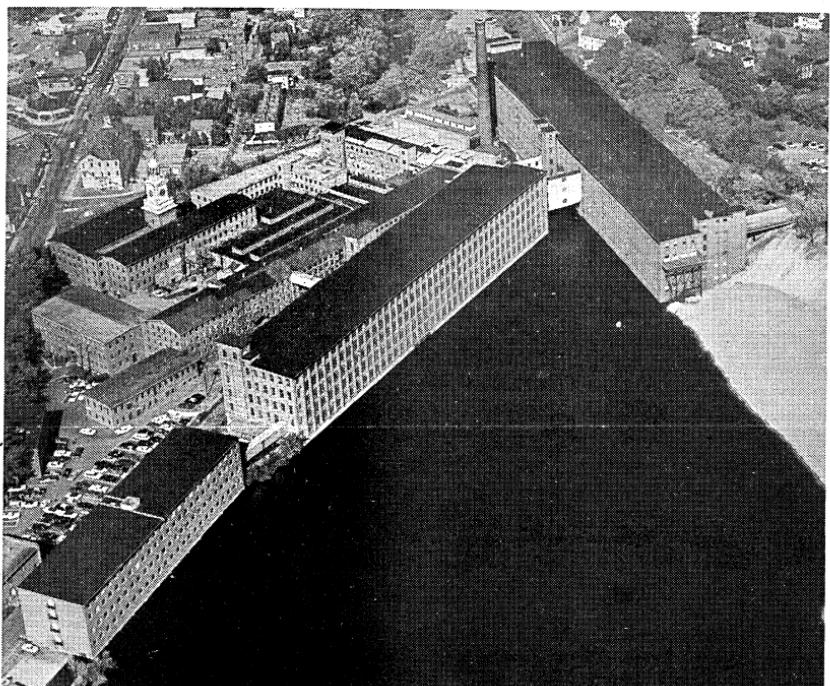


Figure 16. Delays Determining System Operating Frequency

Substitution of a D type flip-flop results in a similar timing situation. In a system using both D and J-K flip-flops, note that the D flip-flop triggers on the leading edge of the clock pulse and the J-K flip-flop triggers on the trailing edge. When calculating system timing using D flip-flops, remember that the flip-flop inputs must be settled at least 20 nsec prior to the occurrence of the clock pulse.

Preparation of a timing diagram that considers delays introduced by all logic elements will aid the designer in achieving predictable system performance.

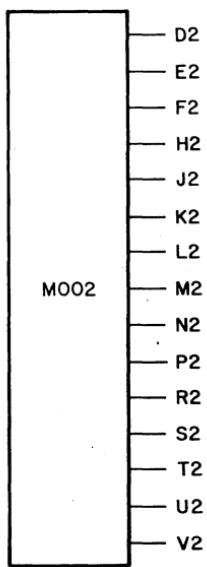


DIGITAL's home office and main manufacturing facilities are located in this former woolen mill complex in Maynard, Massachusetts. We have 900,000 square feet here, about 100 times more than when the company started producing digital modules eleven years ago. We also manufacture at three other locations.

LOGIC 1 SOURCE

M002

M
SERIES



POWER

← A2 — +5V

← C2 — GRD

To hold unused M-Series TTL gate inputs high, the M002 provides 15 outputs at +3 volts (Logic 1), on pins D2 through V2. Up to 10 unused M-Series gate inputs may be connected to any one output. If a M002 circuit is driven by a gate, it appears as two TTL unit loads or 3.2 ma. at ground.

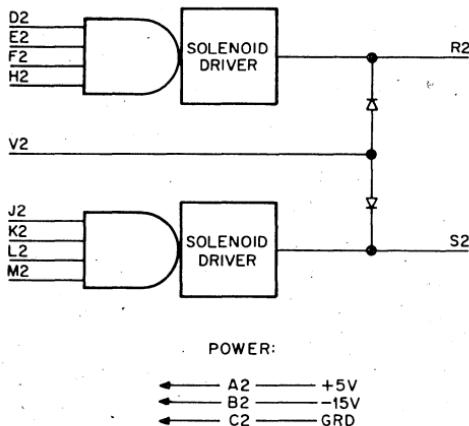
Power: +5 v at 16 ma. (max.)

M002 — \$10

SOLENOID DRIVER

M040

**M
SERIES**



M040 Solenoid Driver

These high current drivers can drive relays, solenoids, stepping motor windings, or other similar loads. The output levels are -2 volts and a more negative voltage determined by an external power supply. One terminal of the load device should be connected to the external power source, the other to the driver output. There are two drivers per module.

Pin V of the driver module must be connected to the external supply so that the drivers will be protected from the back voltage generated by inductive loads. If the wire to the power supply is more than 3 feet long it may have to be by-passed at the module with an electrolytic capacitor to reduce the short over-shoot caused by the inductance of the wire. If pin V is connected to the supply through a resistor, the recovery time of inductive loads can be decreased at a sacrifice in maximum drive voltage capability. Maximum rated supply voltage less actual supply voltage should be divided by load current to find the maximum safe resistance. When both circuits on a module are used, the load current for the above calculation is the sum of the currents.

Inputs: Each input presents one unit load.

Outputs: The M040 has maximum ratings of -70 volts and 0.6 amp. Typical delay for the circuit is 5 μ sec. No more than two circuits should be paralleled to drive loads beyond the current capabilities of single circuits.

Grounding: High current loads should be grounded at pin C2 of the M040. -15 volt at 9 ma. (max.)

Power: +5 volt at 47 ma. (max.)

The external voltage supply must provide the output current of the two drivers. (1.2 amps. max.)

Note:

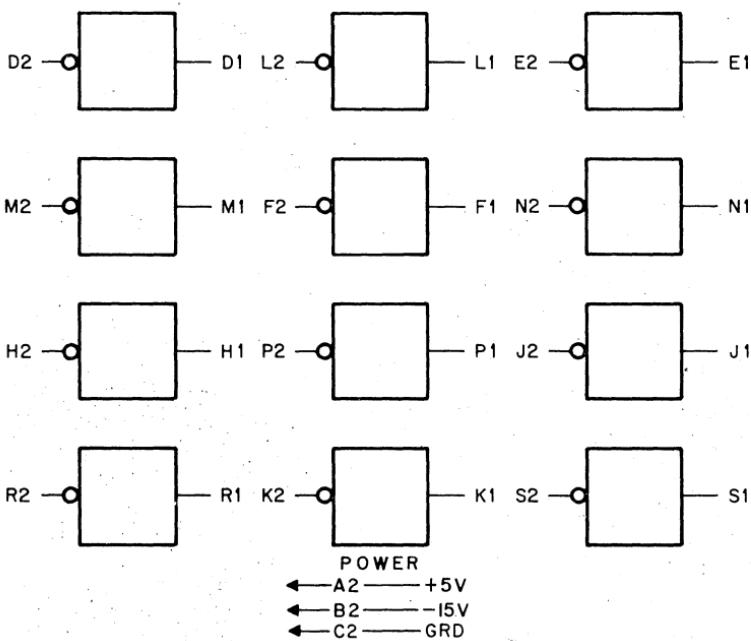
Refer to K Series driver modules for increased current drive, increased voltage breakdown or AC current drive capability.

M040 — \$39

50 MA. INDICATOR DRIVER

M050

**M
SERIES**



M050 INDICATOR DRIVER

The M050 contains twelve transistor inverters that can drive miniature incandescent bulbs such as those on an indicator panel. It is used to provide drive current for a remote indicator, such as Drake 11-504, Dialco 39-28-375, or Digital Indicator type 4908, or level conversion to drive 4917 and 4918 indicator boards (See the Hardware Section.) A low level on the input of the driver causes current to flow in the output.

Inputs: Each input presents two unit loads.

Outputs: Each output is capable of driving 50 ma. into an external load connected to any voltage between ground and -20 volts.

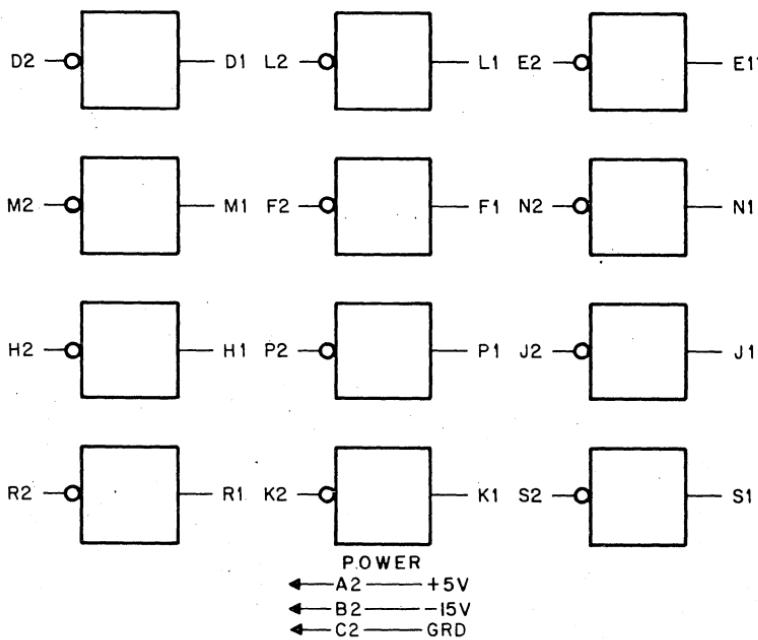
Power: +5 volt at 47 ma. (max.)
-15 volt at 16 ma. (max.)

Note: For those applications requiring the sinking of current, refer to K Series.

M050—\$31

LEVEL CONVERTER M051

M
SERIES



The M051 contains twelve level converters that can be used to shift M and K Series logic levels to negative logic levels of ground and -3 volts. A grounded input on the driver generates a grounded output.

Inputs: Each input presents two TTL unit loads.

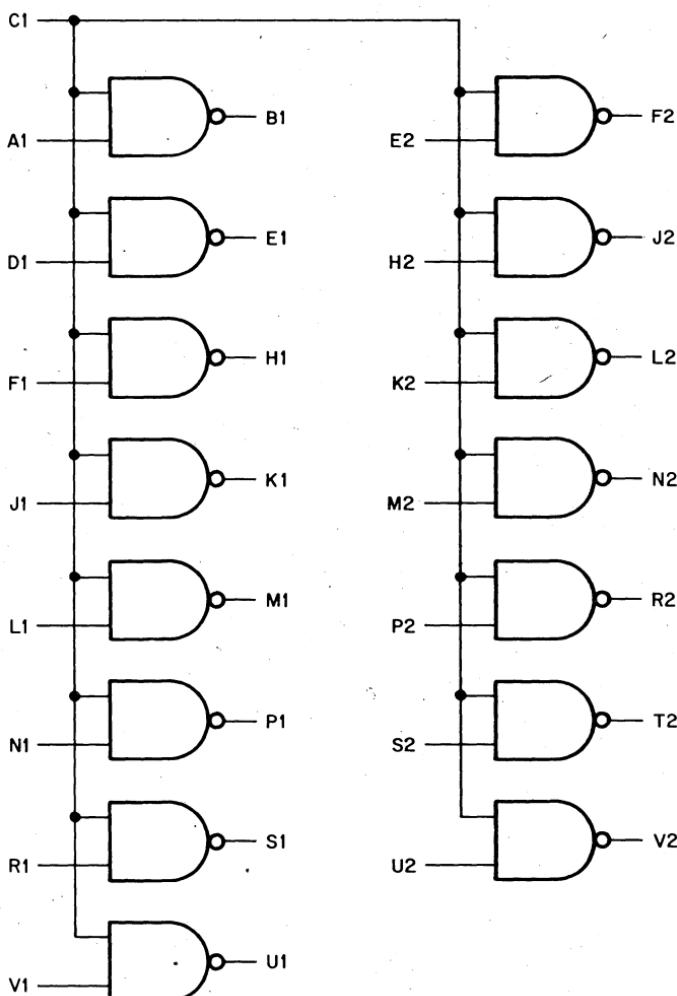
Outputs: The output consists of an open collector PNP transistor and can drive 20 ma. to ground -6 V maximum may be applied to the output.

Power: +5V at 47 ma. (max.); -15 V at 16 ma. (max.)

M051—\$31

BUS DATA INTERFACE
M101

M
SERIES



POWER

← A2 — +5V

← C2, T1 — GRD

The M101 contains fifteen, two-input NAND gates arranged for convenient data strobing off of the PDP8/I or PDP8/L positive bus. One input of each gate is tied to a common line so that all data signals on the second input of each gate can be enabled simultaneously. The M101 can also be used as inverters or a data multiplexer. All data inputs are protected from a negative of more than -0.8 volts.

Inputs: Each data signal input presents one TTL unit load. The common line input presents fifteen unit loads.

Outputs: Each output can drive ten unit loads.

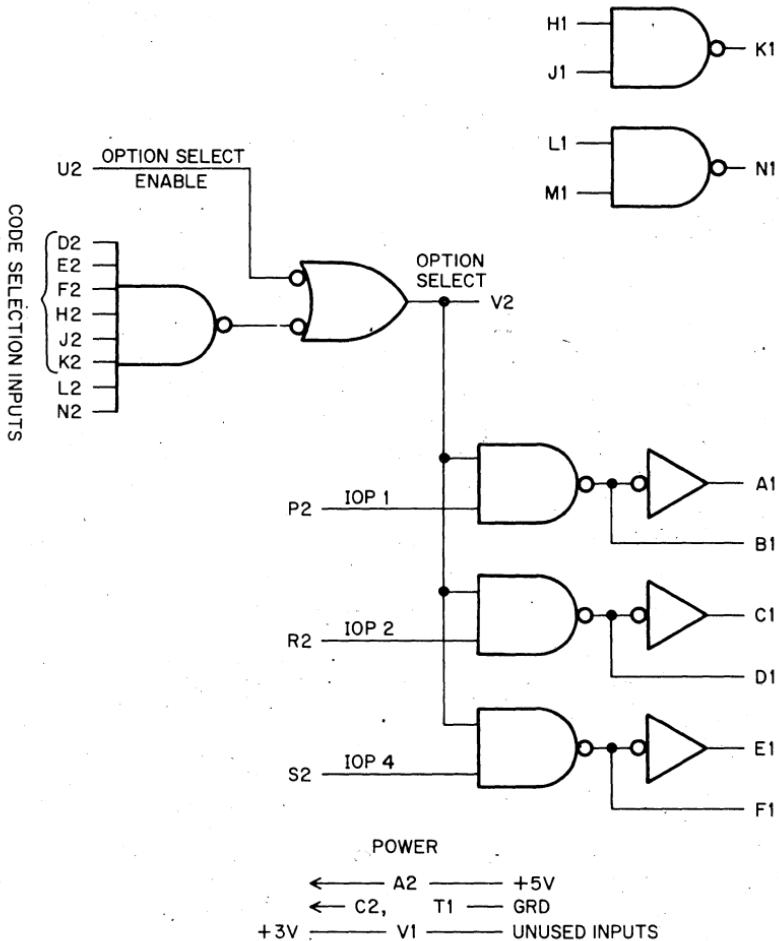
Power: +5V at 82 ma. (max.)

M101—\$24

DEVICE SELECTOR

M103

**M
SERIES**



The M103 is used to decode the six device bits transmitted in complement pairs on the positive bus of the PDP8/I and PDP8/L. Selection codes are obtained by selective wiring of the bus signals to the code select inputs D2, E2, F2, H2, J2, and K2. This module also includes pulse buffering gates for the IOP signals found on the positive bus of the above computers. Two two-input NAND gates are also provided for any additional buffering that is required.

Inputs: All inputs which receive positive bus signals are protected from negative voltage undershoot of more than -0.8V.

The following inputs each present one TTL unit load D2, E2, F2, H2, J2, K2 H1, J1, L1, and M1. Inputs P2, R2, and S2 present 2.5 TTL unit loads. Inputs U2, L2 and N2 each present 1.25 unit loads. These inputs need not be tied to a source of logic 1 when not used.

Outputs: Gate outputs K1 and N1 can each drive ten TTL unit loads.

Pulse buffering outputs A1, B1, C1, D1, E1 and F1 can each drive 37 TTL unit loads.

The Option Select output can drive 16 TTL unit loads.

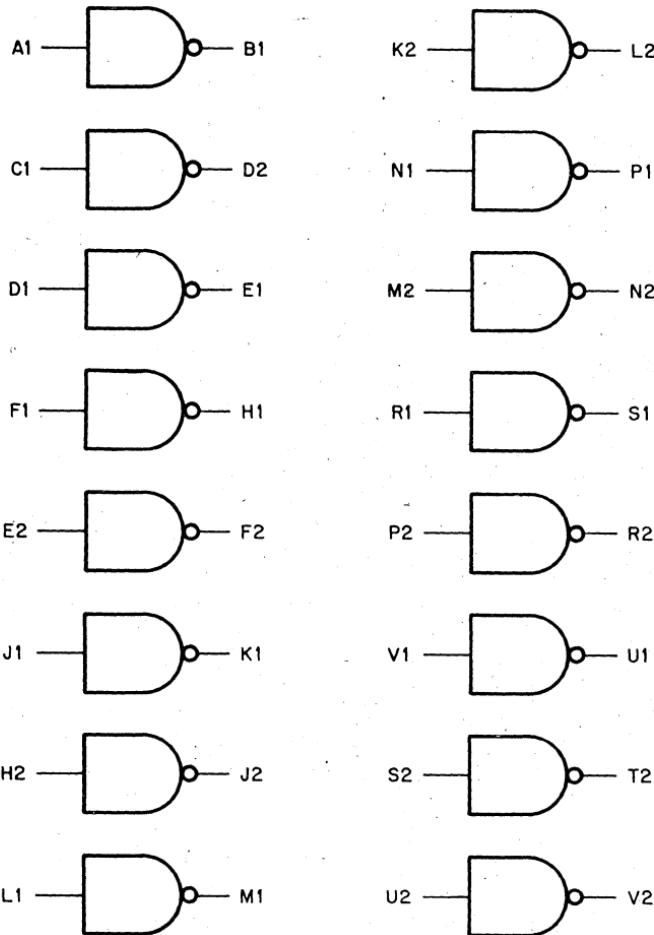
Power: +5 volts at 110 ma. (max.)

M103—\$50

INVERTER

M111

M
SERIES



POWER

← A2 — +5V

← C2, T1 — GRD

Sixteen Inverters with input/output connections as shown.

Input: Each input presents one unit load.

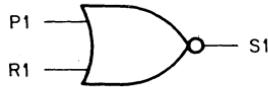
Output: Each output can drive up to ten unit loads.

Power: +5 volts, 87 ma. (max.)

M111—\$24

NOR GATE M112

M
SERIES



POWER

\leftarrow A2 \rightarrow +5V

\leftarrow C2, T1 \rightarrow GRD

+3V \leftarrow U1, V1 \rightarrow UNUSED INPUTS

The M112 contains ten positive NOR gates, each performing the function $A + B$. Pins U1 and V1 provide +3 volts, each capable of holding High (Logic 1) up to 40 unused M-Series inputs.

Input: Each input presents one unit load.

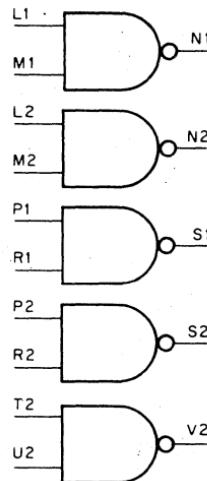
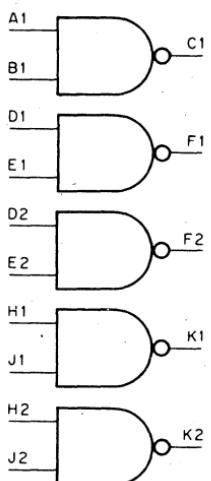
Output: Each output can drive up to ten unit loads.

Power: +5V at 50 ma. (max.)

M112—\$37

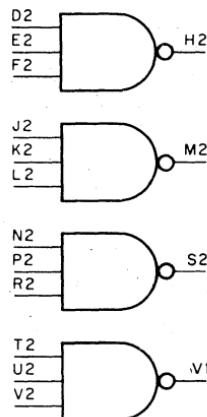
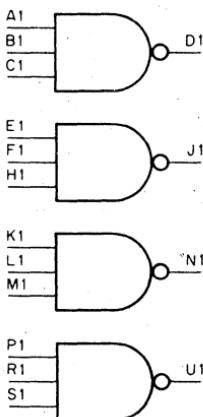
NAND GATES
M113, M115, M117, M119

**M
SERIES**



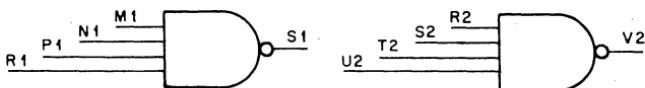
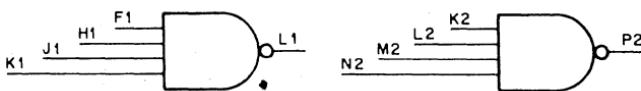
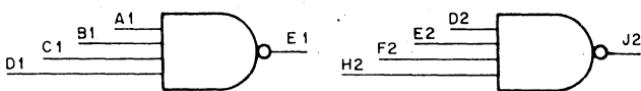
POWER:
 ← A2 → +5V
 ← C2, T1 → GRD
 +3V ← U1, V1 → UNUSED INPUTS

M113 2-INPUT NAND GATES



POWER:
 ← A2 → +5V
 ← C2, T1 → GRD

M115 3-INPUT NAND GATES



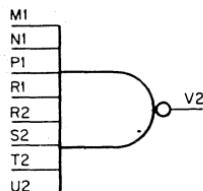
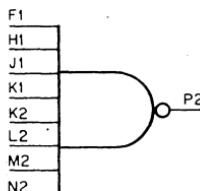
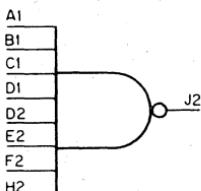
POWER:

← A2 → +5V

← C2, T1 → GRD

+3 VOLTS ← U1, V1 → UNUSED INPUTS

M117 4-INPUT NAND GATES



POWER:

← A2 → +5V

← C2, T1 → GRD

+3 VOLTS ← U1, V1 → UNUSED INPUTS

M119 8-INPUT NAND GATES

These modules provide general-purpose gating for the M Series, and are most commonly used for decoding, comparison, and control. Each module performs the NAND function $A \cdot B \cdot \dots \cdot N$, depending upon the number of inputs.

M113—Ten, two-input NAND gates that also may be used as inverters.

M115—Eight, three-input NAND gates.

M117—Six, four-input NAND gates.

M119—Three, eight-input NAND gates.

Unused inputs on any gate must be returned to a source of logic 1, for maximum noise immunity. In the M113, M117, M119, M121, M617 and M627 modules, two pins are provided (U1 and V1) as source of +3 volts for this purpose. Each pin can supply up to 40 unit loads.

M103, M111 and M002 provide additional sources of logic 1 level.

Typical propagation delay of M Series gates is 15 nsec.

Inputs: Each input presents one unit load.

Outputs: Each output is capable of supplying 10 unit loads.

Power:

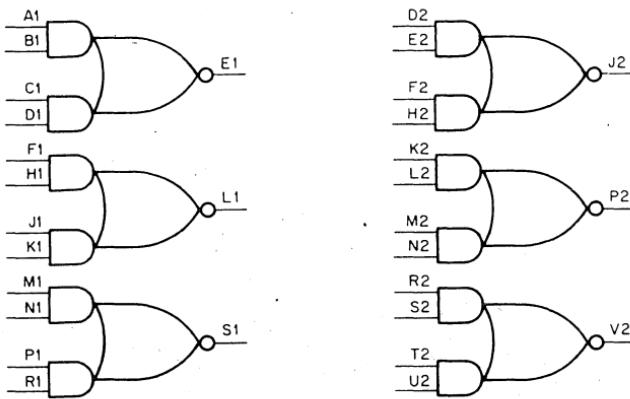
M113: 71 ma.
M115: 41 ma.
M117: 41 ma.
M119: 9 ma. } +Max. current at 5 volts.

M113—\$20
M115—\$20
M117—\$21
M119—\$20

AND/NOR GATE

M121

**M
SERIES**



POWER:
A2 → +5V
C2, T1 → GRD
+3V → U1, V1 → UNUSED INPUTS

M121 AND/NOR GATES

The M121 module contains six AND/NOR gates which perform the function $AB + CD$. By proper connection of signals to the AND inputs, the exclusive OR, coincidence, and NOR functions can be performed.

Typical propagation delay of an M121 gate is 15 nsec.

Inputs: Each input presents one unit load to the driving module.

Outputs: Each output is capable of driving up to 10 unit loads.

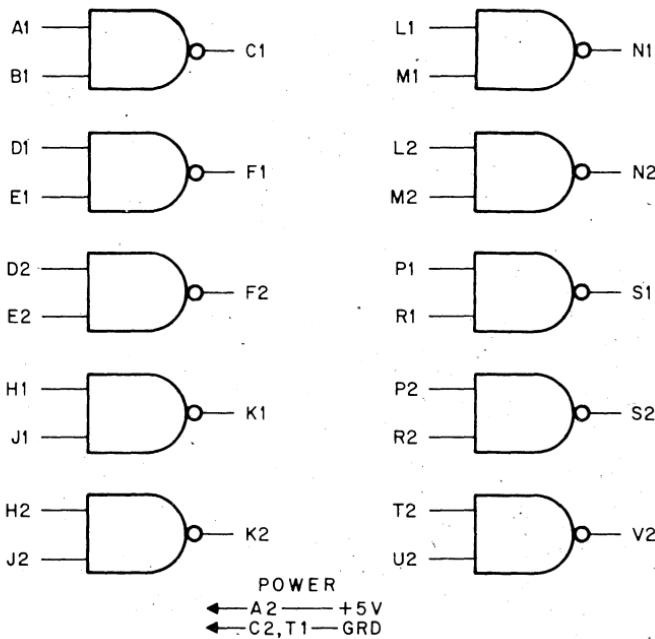
Power: +5volt at 50 ma. (max.)

M121—\$25

INPUT NAND GATES

M133

**M
SERIES**



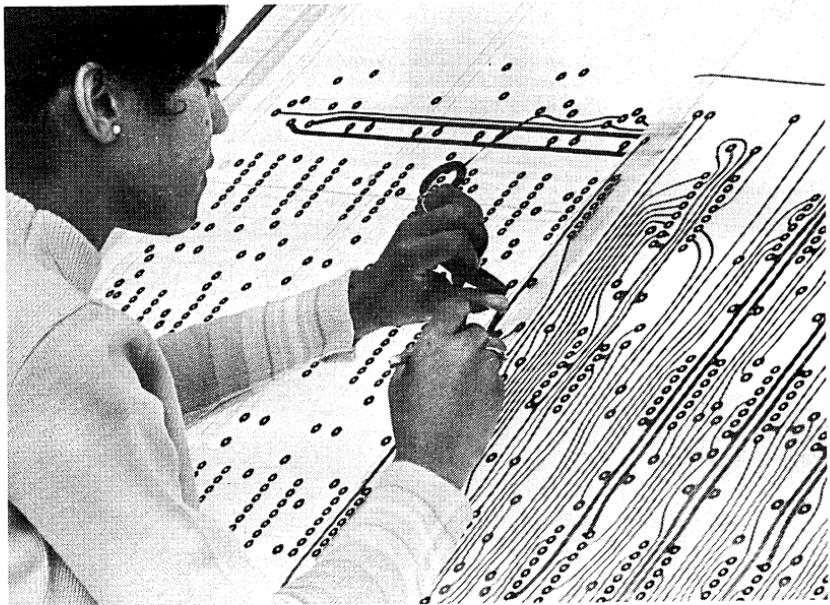
This module provides general purpose high speed gating for the M-Series. Maximum output propagation delay to a logic 1 or 0 is 10 nsec. The high speed characteristic of these gates frequently will solve tight timing problems in complex systems. Unused inputs on any gate must be returned to a source of logic 1 for maximum speed and noise immunity.

Inputs: Each input presents 1.25 unit loads.

Outputs: Each output is capable of driving 12.5 unit loads.

Power: +5V at 160 ma. (max.)

M133—\$29

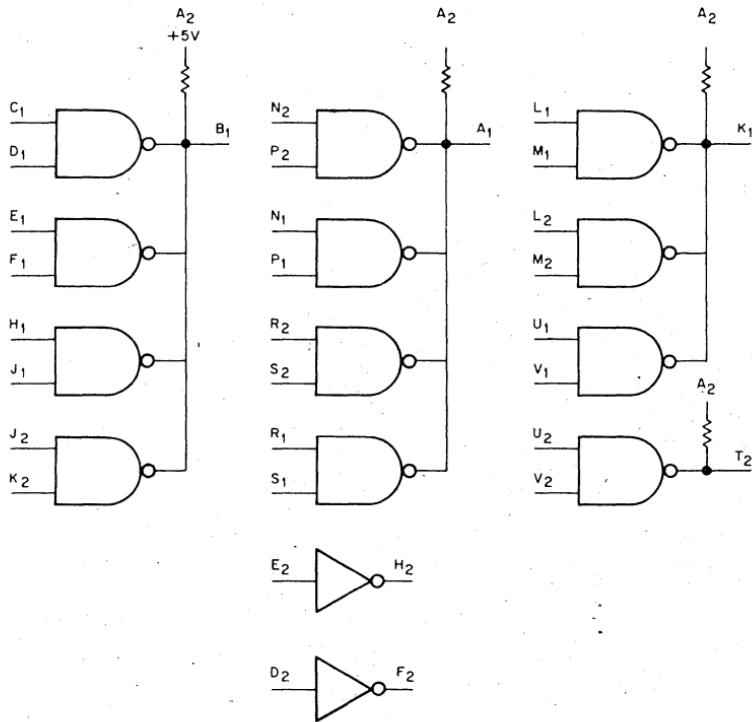


The printed circuit board layout is a crucial step in module production. Tolerances are checked to within 1/5000 of an inch.

NAND/OR GATES

M141

**M
SERIES**



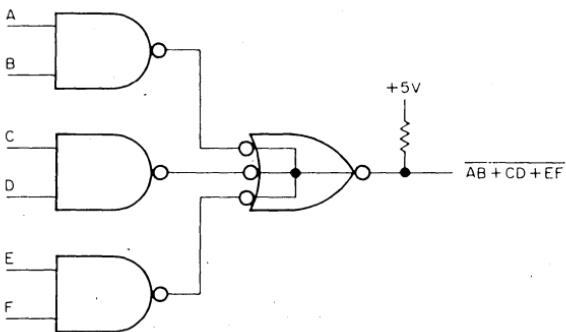
POWER:

← A2 → +5V
← C1, T1 → GRD

M141 NAND/OR GATE

The M141 NAND/OR gate performs two levels of logic. The first is the NAND function which is identical to the M113 NAND gate. The second level is that of a wired OR for low logic levels. The two input NAND gate which is used in the M141 does not have the standard TTL output circuit, but only the lower half of the totem pole output. This allows the outputs of these gates to be connected together and to share a common pull-up resistor. Propagation delay through these gates is a maximum of 70 nsec.

The NAND/OR gates are arranged in four groups consisting of 4, 4, 3, and 1 two input NAND gates respectively. The outputs in each group are connected together which provide a wired OR for low levels. The function of these gates can be shown as:



By using one of the two inverters provided, a true AND/OR function can be realized. A maximum of four groups of gates can be connected together. Connection is made by merely connecting output pins together.

Inputs: Each input presents one unit load.

Outputs: Four gate outputs, each capable of driving 7 unit loads. The load resistor of each output presents 2 unit loads when connected to another output. For example, four groups are connected together, therefore 3 groups present two unit loads each to the fourth group, totalling 6 unit loads. This leaves 1 unit load capability. Each inverter output is capable of driving up to 10 unit loads.

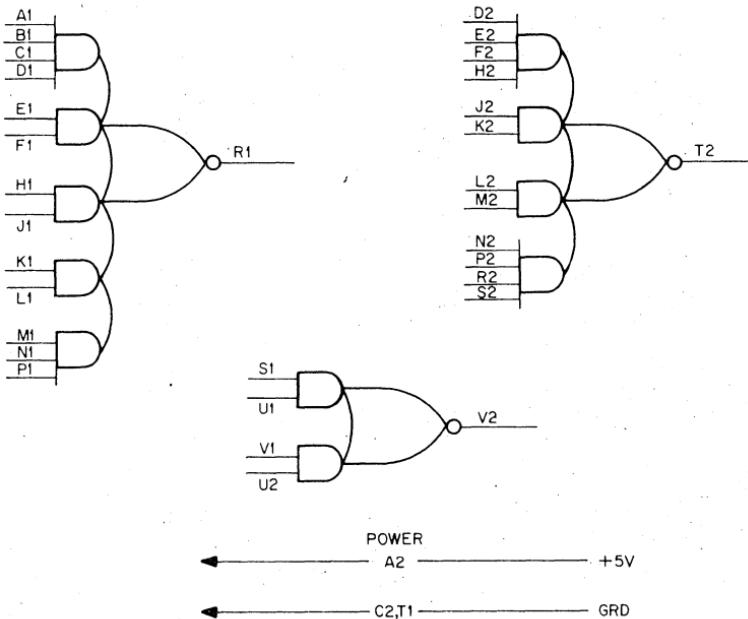
Power: +5 volts at 117 ma. (max.)

M141—\$30

AND/NOR GATE

M160

M
SERIES



M160 AND/NOR GATES

The M160 module contains three general purpose AND/NOR gates which perform functions similar to the M121. By connecting signals to the AND inputs, these gates can be used to select and place on a single output any of several input signals.

Typical propagation delay of an M160 gate is 20 nsec.

Inputs: Each input presents one unit load

Outputs: Each output is capable of driving 10 unit loads

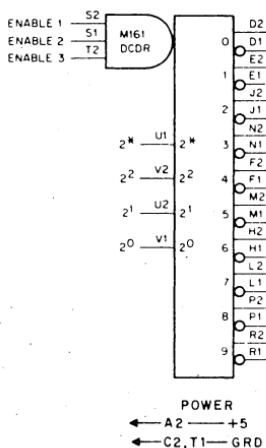
Power: 5 volt at 30 ma. (max.)

M160—\$35

BINARY TO OCTAL/DECIMAL DECODER

M161

M
SERIES



M161 BINARY TO OCTAL/DECIMAL DECODER

The M161 is a functional decoding module which can be used as a binary-to-octal or binary-coded decimal (8421 or 2421 codes) to decimal decoder. In the binary-to-octal configuration, up to eight M161's can be linked together to provide decoding of up to six bits. Three ENABLE inputs are provided for selective enabling of modules in decoders of more than one digit. In the octal mode, the bit 2³ input is connected to ground, which automatically inhibits the 8 and 9 outputs. Connections for a 5-bit binary/octal decoder (4² modules) are shown below. The figure assumes that the inputs to the decoder are the outputs of flip-flops such as FF2° (1), 1 output side; and FF2° (0), 0 output side.

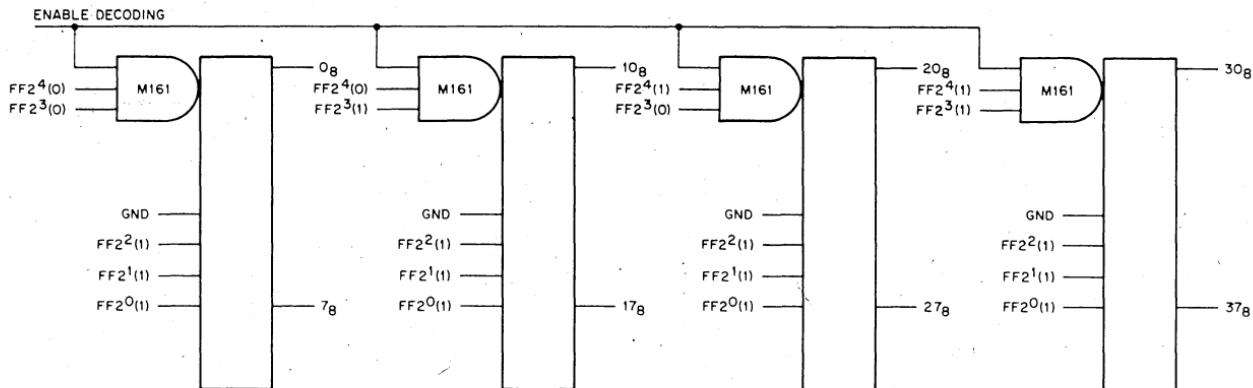
The 2³ input may be of decimal value 2, 4, 6, 8 as long as illegal combinations are inhibited before connections to the inputs, and the 4-2-1 part of the code is in binary.

The propagation delay through the decoder is typically 55 nsec in the binary-to-octal mode, and 75 nsec in the BCD-to-decimal mode. The maximum delay in the BCD-to-decimal mode is 120 nsec, frequency-limiting this module to 8MHz when used in this fashion. The enable inputs can be used to strobe output data providing inputs 2° — 2³ have settled at least 50 nsec prior to the input pulse.

Inputs: 2° through 2³, 1 unit load each; ENABLE 1 through ENABLE 3, 2 unit loads each.

Outputs: Each positive output is capable of driving 10 unit loads, and each negative output, 9 unit loads.

Power: 5 volts at 120 ma. (max.)



5-BIT BINARY/OCTAL DECODER
(OUTPUTS ARE REPRESENTED IN
OCTAL $37_8 = 31_{10}$)

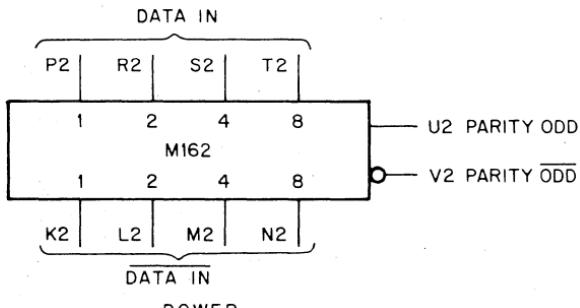
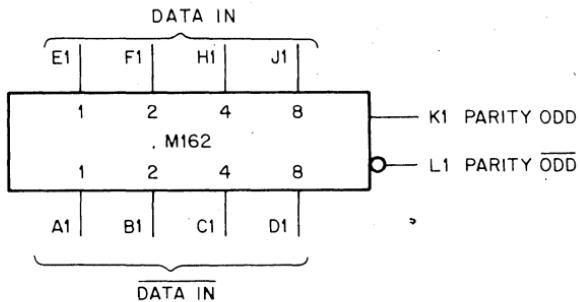
5-BIT BINARY/OCTAL DECODER

M161 — \$60

PARITY CIRCUIT

M162 -

**M
SERIES**



The M162 is a parity detector and contains two Parity Circuits. Each circuit indicates whether the Binary Data presented to it contains an ODD or EVEN number of ONES. The DATA and its complement are required as shown.

Indication of ODD PARITY is given by a High level of pins K1 and U2 respectively. Pins L1 and V2, when High, indicate EVEN PARITY or no input.

Input: Each input presents four unit loads.

Output: Pins L1 and V2 can each supply up to ten unit loads. Pin K1 and U2 can each supply up to six unit loads.

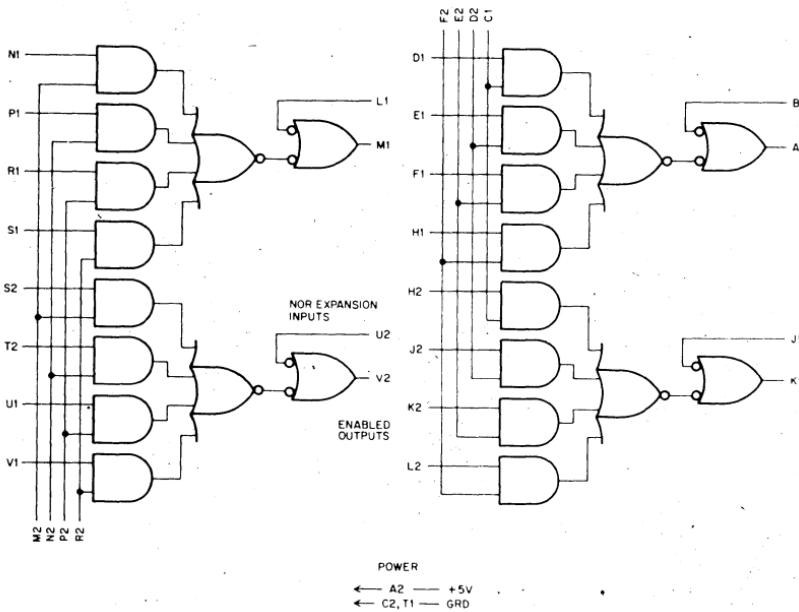
Power: +5 volts at 102 ma. (max.)

M162 — \$68

GATING MODULE

M169

**M
SERIES**



M169 GATING MODULE

The M169 provides a general gating function, and may be used as a four-output multiplexer. Raising High a DATA INPUT and selecting a corresponding INPUT ENABLE line, generates a High at the appropriate ENABLED OUTPUT, A1, K1, M1 or V2. Any of the ENABLED OUTPUTS may be enabled directly through an M121 or M160 AND/NOR gate, used as an NOR Expander. Maximum input to output propagation delay for any circuit is 45 nsec.

Inputs: Each DATA INPUT pin and EXPANSION INPUT pin presents one unit load. Each INPUT ENABLE pin presents two unit loads.

Outputs: Each output can drive up to ten unit loads.

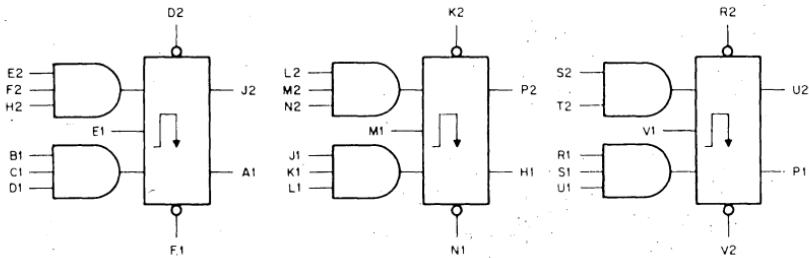
Power: +5 volts at 50 ma. (max.)

M169 — \$35

TRIPLE J-K FLIP-FLOP

M202

M
SERIES



A2, +5V
C2, T1, GROUND
B2, NOT USED

The M202 contains three J-K flip-flops augmented by multiple-input and gates. For general use as gated control flip flops or buffers.

Logical operation of the J-K flip flops used in this module is identical to those flip-flops used in the M207 (described in detail) except clock, J-K inputs, inputs, direct clear, direct set and both output lines for each flip-flop are independent.

Inputs: All gate inputs represent 1 unit load. The dc set and clear input each represent two unit loads. Clock inputs represent two unit loads.

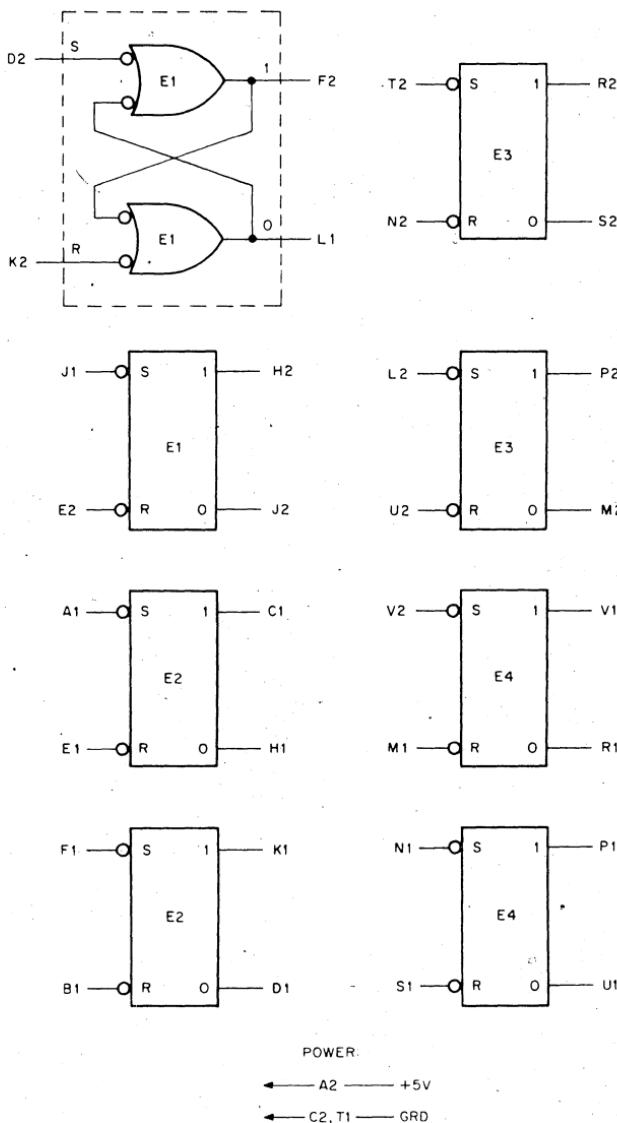
Outputs: Each output will drive 10 unit loads.

Power: +5 v at 57 ma. (max.)

M202 — \$30

8-R/S FLIP-FLOPS
M203

**M
SERIES**



M203 8-R/S FLIP-FLOPS

The M203 is made up of 8 R/S type flip-flops. Each flip-flop is made up of two 2-input NAND gates whose outputs are cross coupled. R/S flip-flops provide an inexpensive method of storage but care must be taken to inhibit placing the Set and Reset inputs low at the same time. In this case, the last of the inputs to be removed will control the final state of the flip-flop.

The propagation delay of the M203 is approximately 30 nsec.

Inputs: All inputs present 1 unit load.

Outputs: All outputs are capable of driving 9 unit loads.

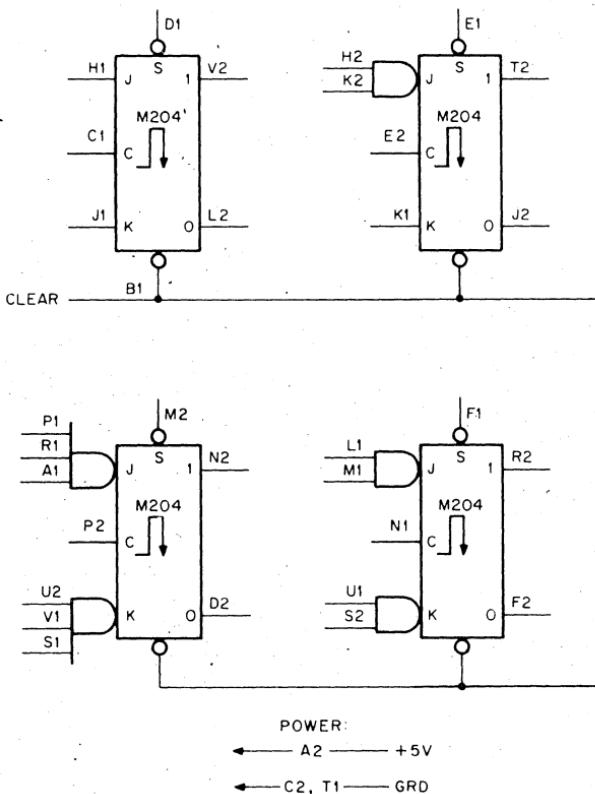
Power: +5 volts, 55 ma. (max.)

M203 — \$28

GENERAL-PURPOSE BUFFER AND COUNTER

M204

M
SERIES



M204 GENERAL-PURPOSE BUFFER AND COUNTER

The M204 contains four J-K type flip-flops, augmented by multiple-input AND gates, for general use as gated control flip-flops or buffers. The gating scheme permits the formation of counters of most moduli up to 16, by simple connector wiring. Clock, trigger and input lines for each flip-flop are independent. A common CLEAR input is provided.

Input information is transferred to the outputs when the threshold point is reached on the trailing (negative going voltage) edge of the clock pulse.

Logical operation of the J-K flip-flops used in this module is identical to the M207 (described in detail) except for the addition of dc set inputs.

Inputs: The "C" inputs present two unit loads each to the source. The dc set ("S") inputs present two unit loads each. The common CLEAR line presents 8 unit loads. All other inputs present one unit load to the source.

Outputs: Each output, before interconnection as a counter, is capable of driving 10 unit loads.

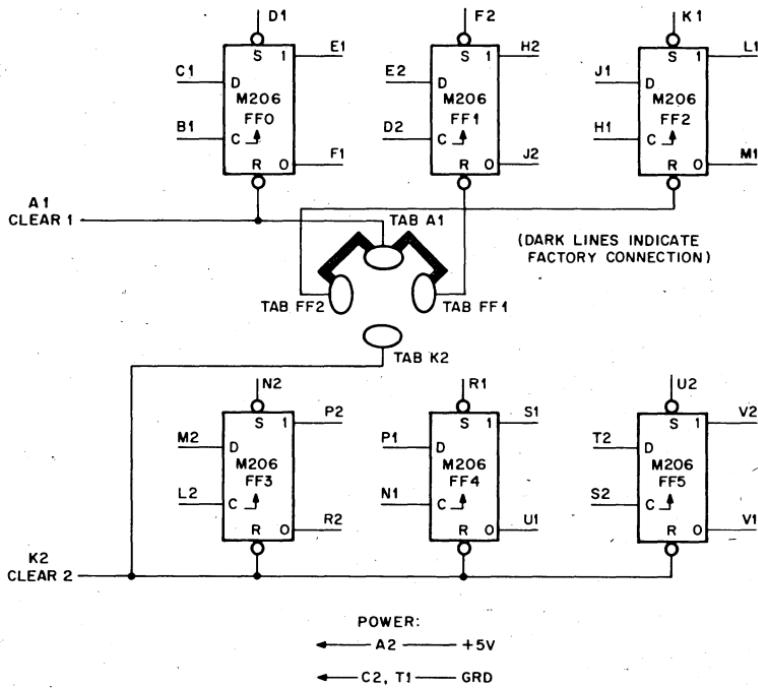
Power: +5 volts, 74 ma. (max.)

M204 — \$36

GENERAL-PURPOSE FLIP-FLOPS

M206

**M
SERIES**



M206 D TYPE FLIP-FLOPS

The M206 contains six separate D-Type flip-flops. Each flip-flop has independent gated data, clock, and dc set inputs.

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flops. All M206 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

CONFIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1, & 2	FF3, 4, & 5		
4-2	FF0 & 1	FF2, 3, 4, & 5	A1 to FF2	K2 to FF2
5-1	FF0	FF1, 2, 3, 4, & 5	A1 to FF2 A1 to FF1	K2 to FF2 K2 to FF1

Information must be present on the D input 20 nsec (max) prior to a standard clock pulse and should remain at the input at least 5 nsec (max) after the clock pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop will be stable at the output within 50 nsec, maximum. Typical width requirement for the clock, dc reset and dc set pulses is 30 nsec each.

Information present on the D input is transferred to the output when the threshold is reached on the leading (positive going voltage) edge of the clock pulse.

Inputs: D inputs present 1 unit load each. C inputs present 2 unit loads each. CLEAR lines present 3 unit loads per connected flip-flop. S inputs present 2 unit loads each.

Outputs: Each output is capable of driving 10 unit loads.

Power: +5 volts, 87 ma. (max.)

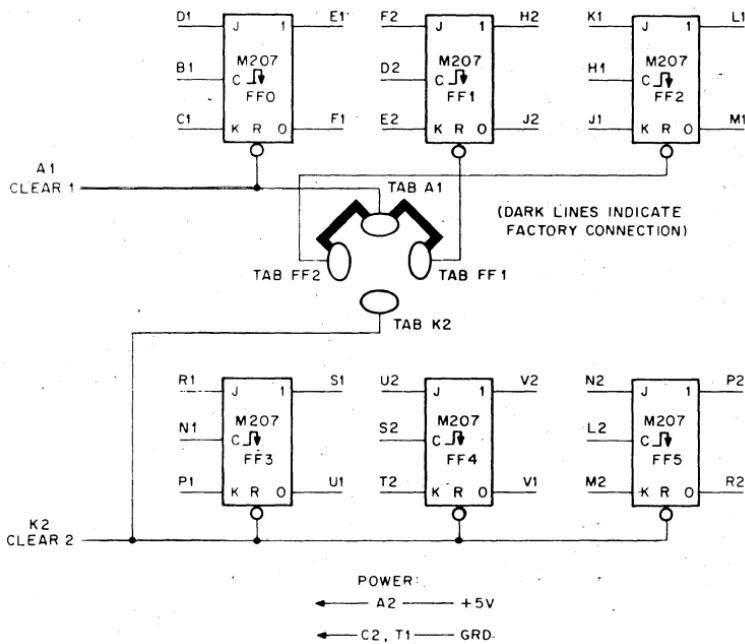
A common clear for all six flip-flops can be obtained by wiring pins A1 and K2 together externally. **CAUTION:** The loading of each clear line is calculated on the basis of 3 unit loads per flip-flop. For example, the 4-2 configuration results in 12 unit loads at input K2 and 6 unit loads at input A1.

M206 — \$36

GENERAL-PURPOSE FLIP-FLOP

M207

**M
SERIES**



M207 J-K FLIP FLOPS

The M207 contains six J-K type flip-flops which can be used as buffers, control flip-flops, shift registers, and counters. A truth table for clocked set and reset conditions appears below. Note that when the J and K inputs are both high, the flip-flop complements on each clock pulse.

STARTING CONDITION (OUTPUT)		INPUT CONDITION		RESULT AT END OF STANDARD CLOCK PULSE (OUTPUT)	
1	0	J	K	1	0
L	H	L	L	No change	
		L	H	No change	
		H	L	H	L
		H	H	H	L
H	L	L	L	No change	
		L	H	L	H
		H	L	No change	
		H	H	L	H

Application of a low level to an R input for at least 25 nsec resets the flip-flop unconditionally. Two CLEAR inputs are provided, with jumper terminals for optional clearing in groups of 3 and 3 (standard), 4 and 2, 5 and 1, or 6 and 0.

J and K inputs must be stable during the leading-edge threshold of a standard clock input and must remain stable during the positive state of the clock. Data transferred into the flip-flop will be stable at the output within 30 nsec (typical) of the clock pulse trailing edge threshold (negative going voltage).

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flop. All M207 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

CONFIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1, & 2	FF3, 4, & 5		
4-2	FF0 & 1	FF2, 3, 4, & 5	A1 to FF2	K2 to FF2
5-1	FF0	FF1, 2, 3, 4, & 5	A1 to FF2 A1 to FF1	K2 to FF2 K2 to FF1

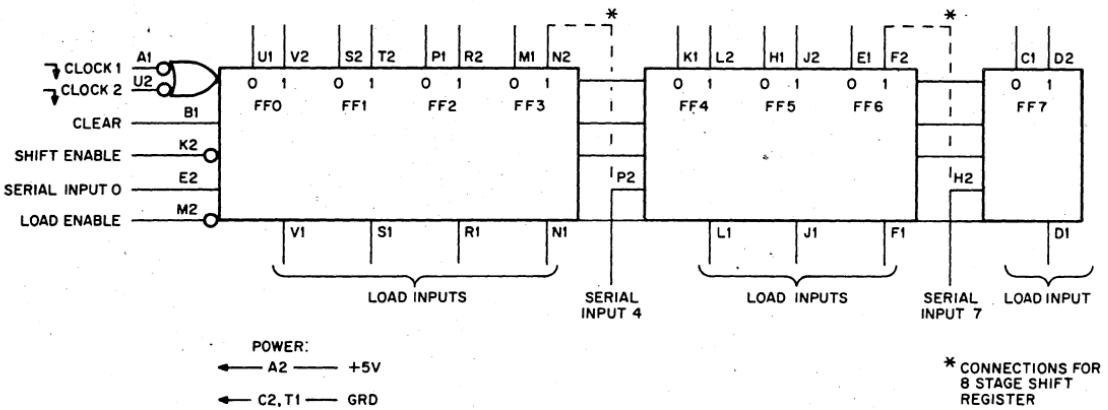
Inputs: J or K inputs present 1 unit load each. C inputs present 2 unit loads each. CLEAR lines present 2 unit loads per connected flip-flop.

Outputs: Each output is capable of driving 10 unit loads.

Power: +5 volts, 96 ma. (max.)

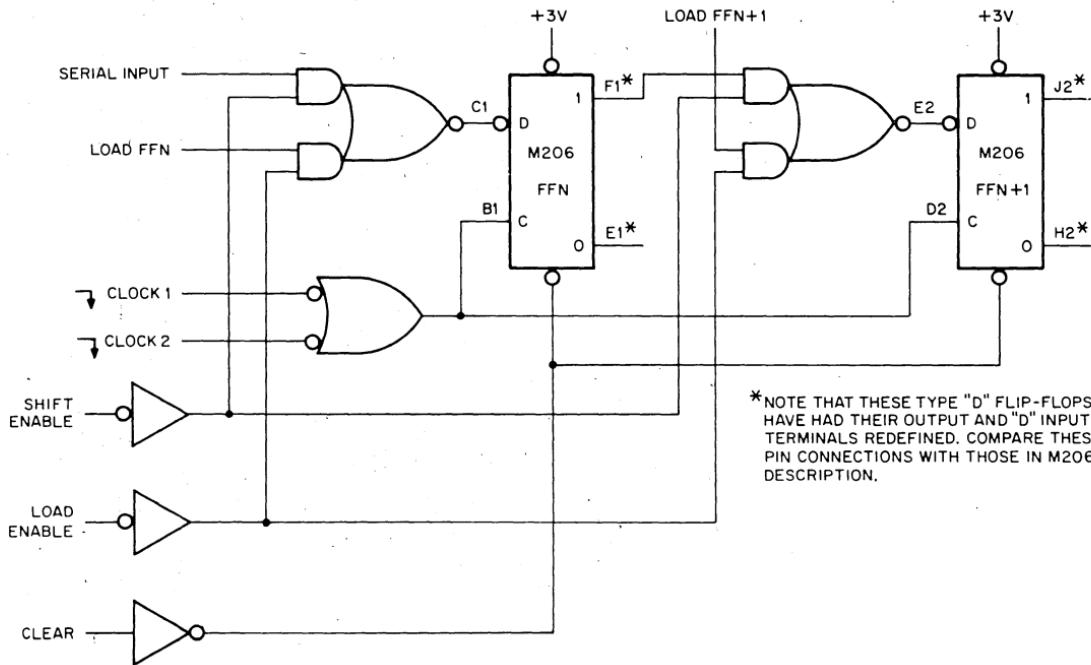
M207 — \$36

8-BIT BUFFER/SHIFT REGISTER M208



M208 8-BIT BUFFER/SHIFT REGISTER

M
SERIES



TWO REPRESENTATIVE STAGES

The M208 is an internally connected 8-bit buffer/shift register. Provisions are made for gated single-ended parallel load, bipolar parallel output, and serial input. The shift register is divided into three segments:

- Bits 0 through 3: Serial input to bit 0, bipolar outputs from bits 0 through 3.
- Bits 4 through 6: Serial input to bit 4, bipolar outputs from bits 4 through 6.
- Bit 7: Serial input to 7, bipolar outputs from bit 7.

Each of these groups shares a common shift line (the ORed CLOCK 1 and CLOCK 2 inputs) and a common parallel load line (LOAD ENABLE). To form a 6-bit shift register, for example, the true output of bit 3 is connected to the serial input of stage 4. A shift register of 8 bits may be constructed from a single module. Modules may be cascaded to form shift registers of any desired length. A few additional stages may be formed more economically from NAND and AND/NOR gates plus a D-type flip-flop. A representative stage of this type is illustrated.

Two clock inputs are provided so that individual Load and Shift clock sources may be used. Care must be taken that the clock inputs remain in the high state in the off condition because either input going to the low state will produce a positive edge at the output of the NAND gate and trigger the D type flip-flop. Data shifted or parallel loaded into the M208 will appear on the outputs within 55 nsec (max) of the clock pulse leading edge threshold. Load of Shift Enable levels and parallel data must be present at least 50 nsec prior to a clock pulse. Propagation delay from the leading edge of a CLEAR pulse to the outputs is 40 nsec max.

Inputs: Serial data, dc set, and enable inputs present one unit load each to the source module. Each clock input presents $2\frac{1}{2}$ unit loads. The CLEAR input presents two unit loads.

Outputs: Parallel outputs are capable of driving 10 unit loads each.

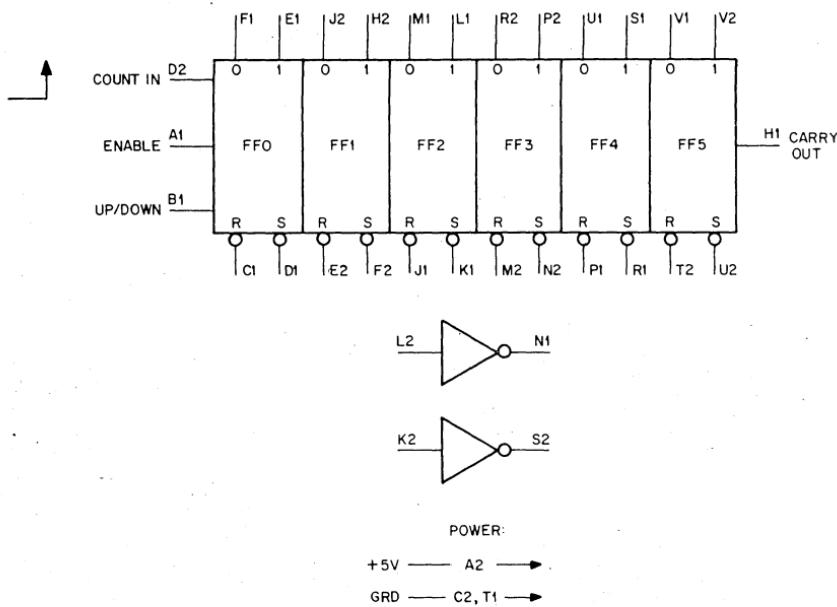
Power: +5 volts, 184 ma. (max.)

M208 — \$84

BINARY UP/DOWN COUNTER

M211

**M
SERIES**



M211 BINARY UP/DOWN COUNTER

The M211 is a 6 bit binary UP/DOWN counter. It can switch counting mode (UP or DOWN) without disturbing the contents of the counter. Maximum count rate is 10 MHz. SET/RESET inputs are available for each bit. Maximum carry propagation time is 80 ns per bit.

Enable Line: The Enable input must be negated 100 nsec. prior to an UP/DOWN level command.

The Enable input must **not** be negated earlier than 500 nsec. after the leading edge (positive going voltage) of the clock pulse.

The Enable input must be asserted at least 60 nsec. prior to the first count.

UP/DOWN Control Line: A logical 1 on this line will yield an up count.

A logical 0 on this line will yield a down count.

Carry Out: The Carry Out will yield a positive level change whenever a carry or borrow occurs.

Inputs: Count In—positive transition or pulse with less than 400 nsec rise-time. Count In presents 2 unit loads. Reset—Each reset input presents 3 unit loads. Set—Each set input presents 2 units loads. All other inputs present 1 unit load.

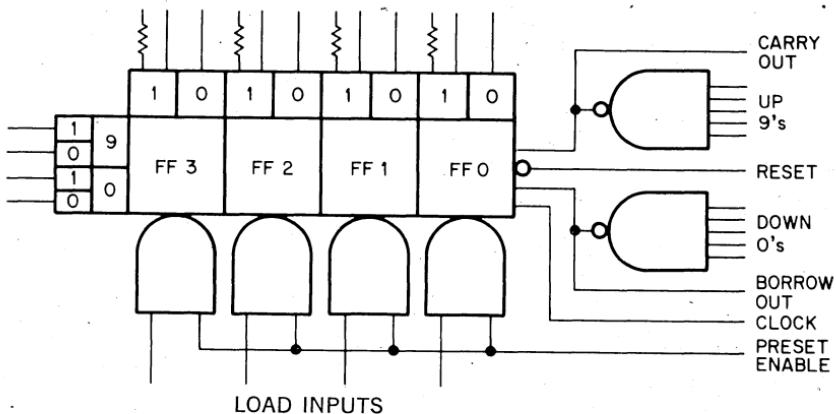
Outputs: Each flip flop output (1 or 0) can drive 8 unit loads. Carry Out can drive 10 unit loads. Each inverter output can drive 30 unit loads.

Power: +5.0 volts, 217 ma. (max.)

M211 — \$75.00

BCD UP/DOWN COUNTER
M213

**M
SERIES**



PIN	A CONNECTOR		B CONNECTOR	
	SIDE (1)	SIDE (2)	SIDE (1)	SIDE (2)
A	—	+5	—	+5
B	—	—	—	—
C	—	Ground	—	Ground
D	9 (0) Out	9 (1) Out	0 (0) Out	0 (1) Out
E	9 In	Up	0 In	Down
F	9 In	9 In	0 In	0 In
H	Carry Out	9 In	Borrow Out	0 In
J	Test Point	9 In	—	0 In
K	—	9 In	—	0 In
L	—	9 In	—	0 In
M	Test Point	Preset Enable	—	—
N	—	Clock	Test Point	Reset
P	Test Point	Load FF 0	Test Point	Load FF 2
R	Test Point	Load FF 1	Test Point	Load FF 3
S	FF 0 (0)	FF 0 (1)	FF 2 (0)	FF 2 (1)
T	Ground	FF 0 (1)	Ground	FF 2 (1)
U	FF 1 (0)	FF 1 (1)	FF 3 (0)	FF 3 (1)
V	—	FF 1 (1)	—	FF 3 (1)

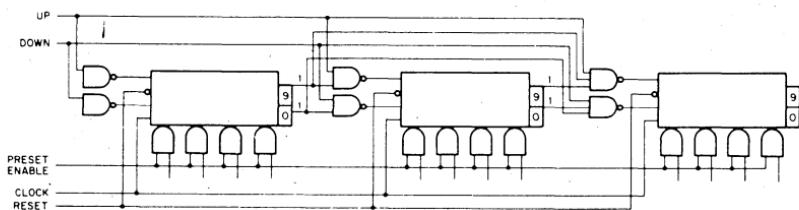
The M213 can be used to construct multi-digit synchronous counters for up/down counting in binary coded decimal. The maximum counting rate is 5 MHz. The counting direction is controlled by enabling the up or down control gate inputs. For maximum noise immunity, the up and down control lines should be kept low until counting is desired. Clock pulses that occur while the up and down lines are both low will not change the contents of the counter. Unpredictable operation will result if both the up and down lines are high at the same time. Positive clock pulses should not occur sooner than 50 ns after any change in the up or down control lines.

The "1" side of each flip-flop output is available directly for controlling nearby logic or through an isolation resistor when decoding displays are being driven at the end of long lines.

The counter may be preset by first resetting the counters and enabling the preset line. The clock input should then be pulsed once with a positive pulse to transfer data from the load inputs into the flip-flops. The up and down control lines must both be low for correct preset operation.

Counter Construction: The up and down input gate wiring for cascading M213 modules makes it possible to construct the hardware for fixed decimal point counters so that additional digits to the left or right of the decimal point can be added later as options. If the sockets are wired initially for a larger counter than is thought to be required, the unused high order digits may be left blank. Unused low order digit sockets should have pins AD2 and BD2 connected to +3 volts. When it is found that additional counter capacity or accuracy is needed, M213 modules can be plugged into the blank sockets on either side of the decimal point as required.

The diagram below shows how to connect three M213 counters for up/down counting. Notice that all the counters are clocked at the same time, but that a counter will not count unless the counters of lower significant digits all contain 9's for up counting or 0's for down counting. All unused module inputs should be connected to +3 volts.



Inputs: The input loads presented are:

CLOCK	— Eight unit loads
RESET	— Eight unit loads
PRESET ENABLE	— Four unit loads
All other inputs	— One unit load

Pulse widths required:

CLOCK	POSITIVE	> 20 nsec
RESET	NEGATIVE	> 25 nsec

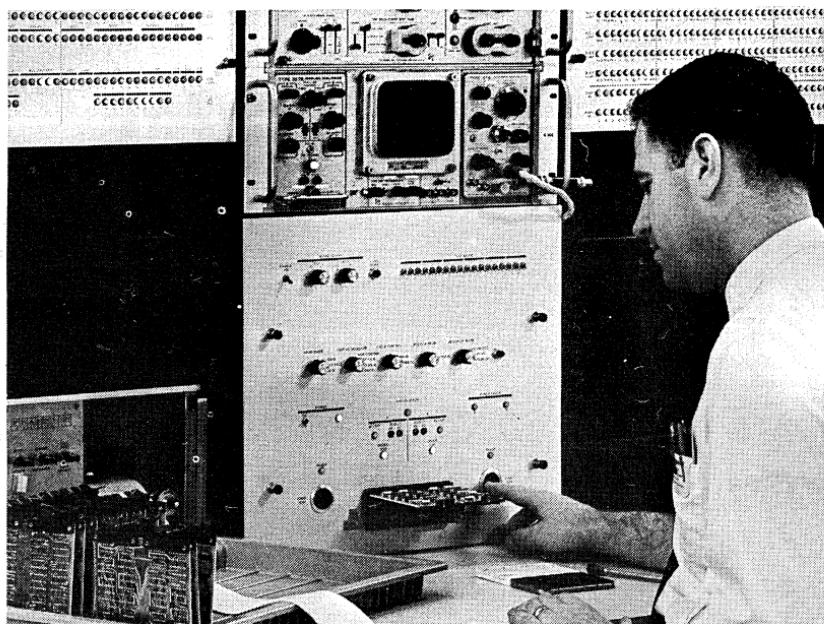
Outputs: Output drive ability:

FLIP-FLOP 1 or 0	— Seven unit loads
FLIP-FLOP 1 (Resistor)	— Five unit loads
(Total load on a 1 output is 7 unit loads.)	
CARRY OUT	— Eight unit loads
BORROW OUT	— Eight unit loads

Cascade Outputs:

9 (1), 9 (0)	
0 (1), 0 (0)	Ten unit loads

Power: +5 volts at 160 ma. (max.)

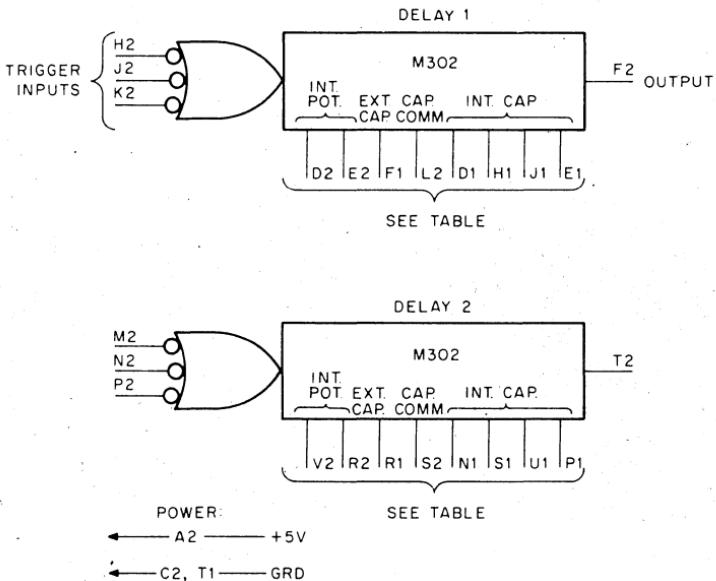


DEC thoroughly tests all finished modules, performing 100 ac and dc tests in less than 5 seconds. Most testing is done automatically on one of three computer-operated test stations like this one.

DUAL DELAY MULTIVIBRATOR

M302

**M
SERIES**



The M302 contains two delays (one-shot multivibrators) which are triggered by a level change from high to low or a pulse to low whose duration is equal to or greater than 50 nanoseconds. When the input is triggered, the output changes from low to high for a predetermined length of time and then returns to low. The basic DELAY RANGE is determined by an internal capacitor. The delay range may be increased by selection of additional capacitance which is available by connecting various module pins or by the addition of external capacitance. An internal potentiometer can be connected for fine delay adjustments within each range or an external resistance may be used. If an external resistance is used, the combined resistance of the internal potentiometer and the external resistance should be limited of 10,000 ohms.

The fall time of the input trigger should be less than 400 nanoseconds.

The delay time is adjustable from 50 nanoseconds to 7.5 milliseconds using the internal capacitors and can be extended by adding an external capacitor.

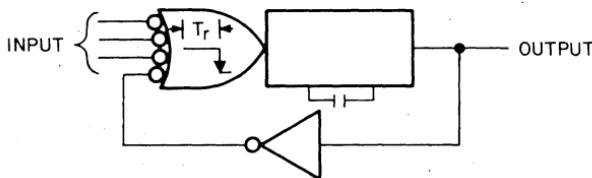
Care should be exercised in the selection of external capacitors to assure low leakage as leakage will affect the time delay.

Recovery time is determined by the size of the capacitance used. The minimum recovery time of this module is 30 nanoseconds when not using any additional capacitance. Recovery time with additional capacitance can be calculated using the formula:

$$T_r = 300 C$$

Where T_r is in seconds
C is in farads

Recovery time is defined for this module as follows: Recovery time, T_r , is the minimum time interval which must exist before each trigger with all inputs high and the output low. The figure shown below illustrates these conditions:



Delay Range	Capacitor Value	Interconnections Required	
		Delay 1	Delay 2
50 nsec — 750 nsec	100 pf (internal)	None	None
500 nsec — 7.5 usec	1000 pf (internal)	D1 — L2	N1 — S2
5 usec — 75 usec	0.01 uf (internal)	H1 — L2	S1 — S2
50 usec — 750 usec	0.10 uf (internal)	J1 — L2	U1 — S2
500 usec — 7.5 msec	1.0 uf (internal)	E1 — L2	P1 — S2
Above 7.5 msec	Add external capacitors between specified pins	F1 — L2	R1 — S2

Adjustable Delays: connect pins to add internal adjustment potentiometer. Without a potentiometer, the delay will not recover. An external potentiometer of less than $10K\Omega$ can be used by connecting it between E2 or R2 and ground pin C2. Use of an external adjustment resistor will cause some increase in jitter. It is recommended that leads to an external potentiometer be twisted pairs and as short as possible.

Inputs: Each input presents $2\frac{1}{2}$ unit loads.

Outputs: Each output is capable of driving 25 unit loads.

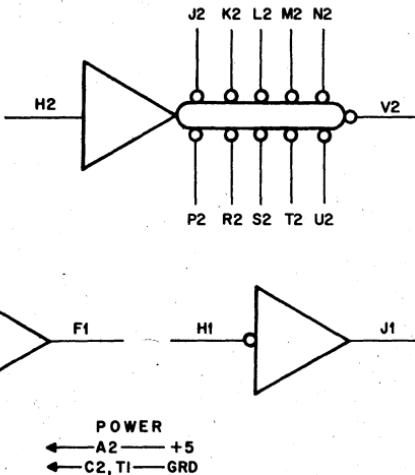
Power: +5 volts, 166 ma. (max.)

M302 — \$46

DELAY LINE

M310

M
SERIES



The M310 consists of a tapped delay line with associated circuitry and two pulse amplifiers. The total delay is 500 nanoseconds with taps available at 50 nanosecond intervals.

The time delay is increased when the amplifier is connected to the delay line taps in ascending order as follows: J₂, K₂, L₂, M₂, N₂, P₂, R₂, S₂, T₂, U₂, and V₂. The tap J₂ yielding the minimum delay and the tap V₂ yielding the maximum delay.

The pulse amplifiers are intended to be used to standardize the outputs of the delay line. The output of the pulse amplifier is a positive pulse whose duration is typically 50 to 200 nanoseconds. These amplifiers are not intended to be driven by TTL IC logic.

Inputs: Pin H2 represents four unit load.

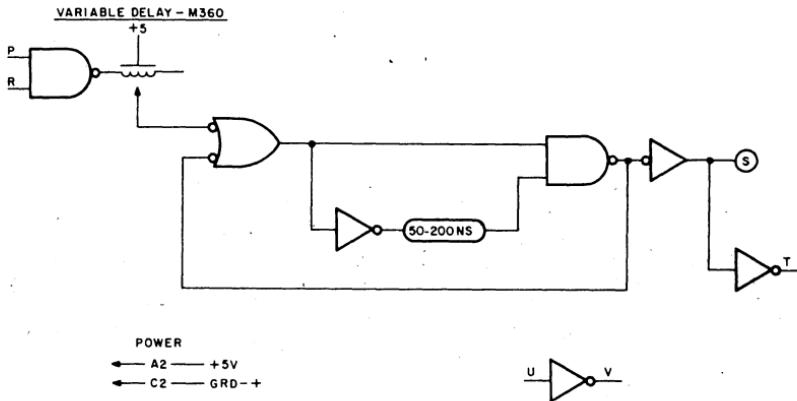
Outputs: Pin F1 and J1 outputs can drive 30 unit loads.

Power: +5 volts at 89 ma. (max.)

M310 — \$58

VARIABLE DELAY M360

M
SERIES



The M360 contains an adjustable delay line with a standardizing amplifier. The delay is adjustable between the limits of 50 nanoseconds to 300 nanoseconds by means of a slotted screw which is accessible from the handle end of the module. The resolution of the delay adjustment is approximately 1 nanosecond. The output consists of a positive pulse whose width is nominally 50 to 200 nanoseconds and the leading (positive going voltage) edge of which, is delayed with respect to the leading (positive going voltage) edge of the input by a length of time as determined by the setting of the delay line adjustment.

Inputs: Pins P and R represent one TTL unit load. Pin U represents two TTL unit loads.

Outputs: Pin S can drive 27 TTL unit loads. Pins T and V are outputs consisting of open collector NPN transistors and can sink 30 milliamperes to ground. Voltage applied to Pins T and V must **not** exceed +20 volts.

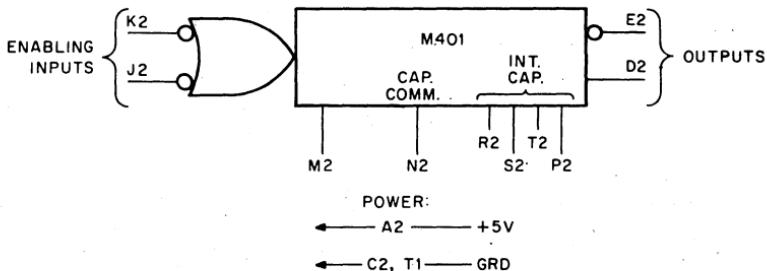
Power: +5 volts, 50 ma. (max.)

M360 — \$68

VARIABLE CLOCK

M401

**M
SERIES**



M401 VARIABLE CLOCK

The M401 Variable Clock is a stable RC-coupled multivibrator which produces standard timing pulses at adjustable repetition rates.

The module is intended for use as the primary source of timing signals in a digital system. Repetition rate is adjustable from 175 HZ to 10 MHz in five ranges. Internal capacitors, selected by jumper pin connections, provide coarse frequency control. An internal potentiometer provides continuously variable adjustment within each range.

A two-input OR gating input is provided for start-stop control of the pulse train. A level change from high to low with fall time less than 400 nsec is required to enable the clock.

If the input is derived from the output of TTL logic and propagation time is 50 nanoseconds, as measured from the +1.5 volt point of the negative going voltage edge of the input to the +1.5 volt point of the negative going edge of the output at pin E2.

Frequency Range	Interconnections Required
1.5 MHz to 10 MHz	(100 pf) NONE
175 KHz to 1.75 MHz	(1000 pf) N2 — R2
17.5 KHz to 175 KHz	(.01 µfd) N2 — S2
1.75 KHz to 17.5 KHz	(0.1 µfd) N2 — T2
175 Hz to 1.75 KHz	(1.0 µfd) N2 — P2

Fine Frequency Adjustment:

Controlled by an internal potentiometer. No provision is made for any external connections.

External capacitor may be added by connection between pin N2 and ground.

The M401 may also be voltage controlled by applying a control voltage to pin M. This feature is available only in M401 modules using printed circuit board revision "E" or later. The voltage applied to Pin M should be limited to the range of 0 volts to +10.0 volts. This voltage swing will allow the frequency to be shifted by approximately 30 percent in the frequency range using the internal capacitors of 1.0, 0.1, 0.01 and 0.001 ufd. If the voltage applied to Pin M is D.C. or low frequency (below 1 KHz), Pin M will appear approximately as a +1.0 volt source with a Thevenin resistance of 800 ohms. Modulating the M401 with a 10V P-P signal about a center frequency, as derived by the application of a mean voltage of +5 volts to Pin M, will yield a typical frequency excursion of —0 in excess of $\pm 15\%$ about the center frequency. Typical frequency excursions which may be obtained are shown below:

Voltage applied to Pin M	CAPACITOR			
	1.0 ufd.	0.1 ufd.	0.01 ufd.	.001 ufd.
0	1.000	10.00	100.0	1000
+1	1.054	10.49	104.6	1036
+2	1.101	10.94	109.2	1071
+3	1.147	11.39	113.6	1108
+4	1.193	11.83	118.0	1142
+5	1.238	12.26	122.2	1181
+6	1.282	12.69	126.4	1271
+7	1.325	13.10	130.4	1295
+8	1.368	13.50	134.2	1312
+9	1.408	13.87	137.7	1322
+10	1.443	14.20	140.9	1323
Output frequency in KHz				

Inputs: Each enable input represents 1 unit load. Pin M, refer to text above.

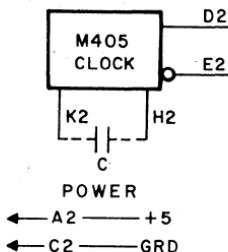
Outputs: The positive output can drive 10 unit loads; the negated output, 9 unit loads.

Power: +5 volts, 80 ma. (max.).

M401 — \$55

CRYSTAL CLOCK M405

M
SERIES



The M405 clock employs a series resonant crystal oscillator to obtain a frequency stability of .01% of specified value between 0°C and +55°C. The clock frequency may be specified anywhere in the range of 5 KHz to 10 MHz by the customer.

Outputs: Outputs at pins D2 and E2 are respectively positive and negative going 0-+3 volt 50 nsec pulses. Pin D2 can drive 10 unit loads while E2 can drive only 9 unit loads. Pulses at pins D2 and E2 are time shifted by one gate delay with negative pulse at pin E2 leading the positive pulse at D2 by a maximum of 20 nsec. The output pulse width can be modified by the addition of an external capacitor between pins K2 and H2. This capacitor will increase the output pulse width by approximately 1 nsec per 2.5 mmfd of additional capacitance. Output pulse width should not exceed 100 nsec between MHz and 10 MHz and 10% of the period at any other frequency.

Power: +5 volts, 50 ma. (maximum)

Ordering Information: When ordering the M405 always specify frequency. Allow six weeks for delivery.

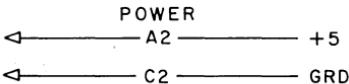
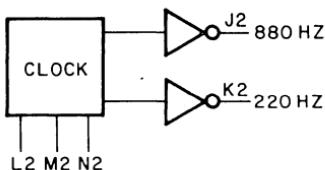
Standard Stock Frequencies: 1.333 MHz, 2.000 MHz, 5.000 MHz.

M405 — \$100

VARIABLE CLOCK

M452

M
SERIES



The M452 is a free running clock which generates the necessary timing signals for the PDP 8/I teletype control. Frequency adjustment of this module is limited to less than 5% and the overall clock stability with respect to supply voltage and temperature variations is about 1%. The available output frequencies are 880Hz, and 220Hz. A pulse amplifier is provided for the generation of nominal 150 nsec pulses.

Inputs: The pulse amplifier input presents one unit load.

Outputs: Pin J2 drives 30 unit loads at 880Hz. Pins N2 and M2 drive 9 unit loads at 330Hz. Pin L2 drives 9 unit loads at 220Hz. Pin K2 drives 30 unit loads at 220Hz. Pin R2 drives 10 unit loads with a nominal 150 nsec positive output pulse. Under normal operating conditions, pins L2, M2, N2, are used as test points.

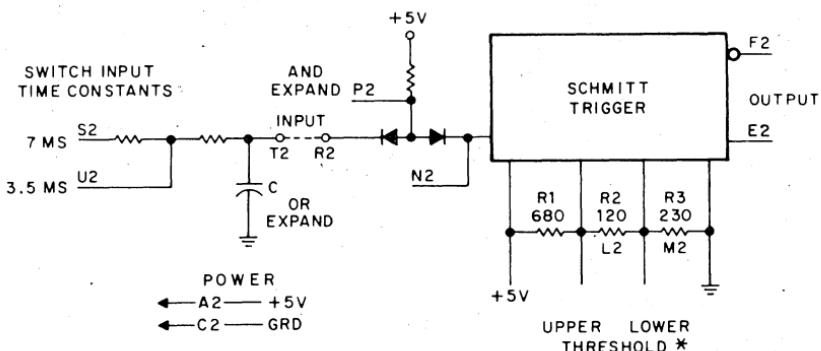
Power: +5 volts, 77 ma. (max.)

M452 — \$40

SCHMITT TRIGGER

M501

**M
SERIES**

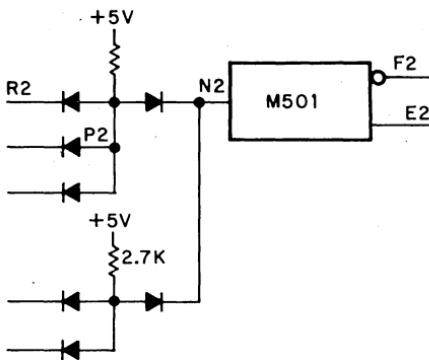


Basically a Schmitt Trigger with variable thresholds, the M501 is used as a Switch Filter, Pulse Shaper and Threshold Detector. Complementary positive logic levels are provided as outputs.

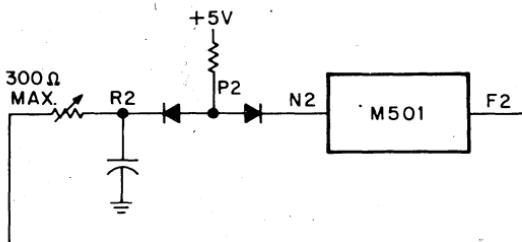
The INPUT on PIN R2 is compared with the thresholds set on PINS L2 and M2, Upper and Lower respectively. AND and OR EXPANSION may be performed on PINS P2 and N2. Module R001 and R002 provide the diodes required. An integrator is provided on the input, allowing SWITCHES to be connected to the Schmitt Trigger with contact bounce effects eliminated. Two switch TIME CONSTANTS are provided. Inputs to PIN S2 result in a 7 m sec TIME CONSTANT, to PIN U2, 3.5 m sec.

The Upper and Lower threshold are preset at 1.7 volts and 1.1 volts. They may be modified by the addition of resistor combination in parallel with the internal network. However, the upper threshold must not exceed 2.0 volts or the lower threshold fall below 0.8 v.

R _x	PARALLEL	R2	—	THRESHOLD CLOSER
R _x	PARALLEL	R1	—	UPPER RISES
R _x	PARALLEL	R3	—	LOWER FALLS



Connecting a resistor from OUTPUT PIN F TO INPUT PIN R with PIN T tied to PIN R forms an oscillator.



Inputs: Input signal swing on PIN R2 is limited to ± 20 volts.

Input Pin R2: $2.7\text{ K}\Omega$ to $+5$ volts or 1.8 mA . at ground.

Pin P2—AND EXPAND input

Pin N2—OR EXPAND input

Pin S2—RC SWITCH INPUT Filter 7 msec

Pin U2—RC SWITCH INPUT Filter 3.5 msec

Pin L2, M2—Available for threshold modification.

Outputs: PIN F2 goes to GROUND when the input on PIN R2 rises above the UPPER threshold, having been below the lower threshold.

PIN F2 rises to $+3$ volts when the input on PIN R2 falls below the LOWER threshold, having been above the upper threshold.

PIN E2 is the complement of the PIN F2.

PIN E2 can drive ten unit loads.

PIN F2 can drive eight unit loads.

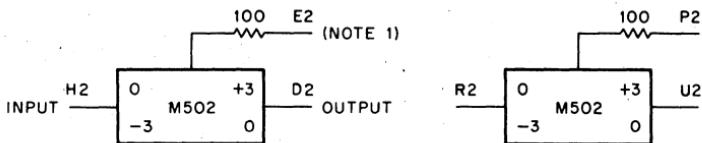
Power: $+5$ volts at 31 mA . (max.)

M501 — \$25

NEGATIVE INPUT CONVERTER

M502

**M
SERIES**

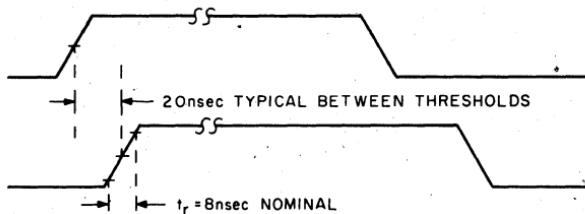


POWER:

← A2 ————— +5V
← B2 ————— -15V
← C2, M2 ————— GRD

NOTE

1. CONNECT TO OUTPUT WHEN NOT DRIVING 92ohm COAX.



M502 NEGATIVE INPUT CONVERTER

INPUT

0v
-3v

OUTPUT

+3v
0v

The M502 contains two non-inverting high-speed signal converters which interface standard negative (-3v and ground) DIGITAL logic levels or pulses with M and K Series positive logic modules. These converters provide sufficient current drive at a low output impedance for system interconnections by means of terminated 92-ohm coaxial cable. The converters operate at frequencies up to 10 MHz, with typical output rise and fall times of 8 nsec. Propagation times for output rise and fall are typically 20 nsec.

Inputs: Input loading is equivalent to a 3 ma. clamped load.

Outputs: Each output can drive terminated 92-ohm coaxial cable, and supply an additional 30 ma. at +3 volts or sink an additional 30 ma. at ground. Output rise and fall times depend on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds are increased by connecting the 100 ohm resistor to the output.

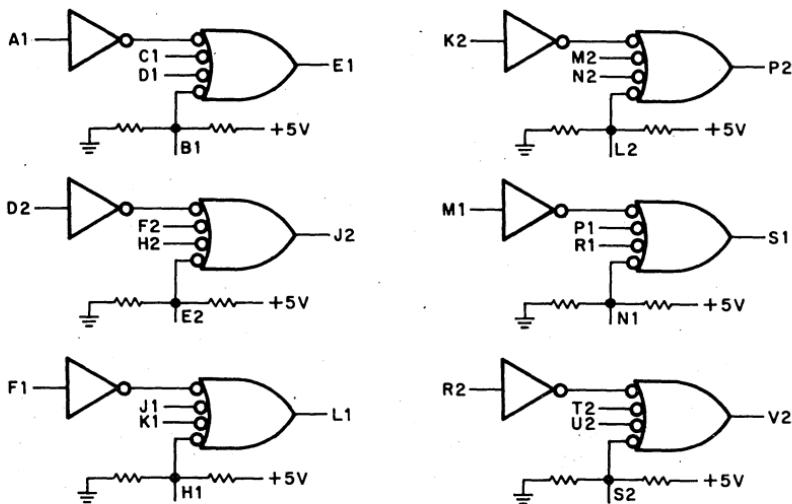
Power: +5 volts, 49 ma. (max.); -15 volts, 92 ma. (max.). Add 44 ma. for each 100 ohm resistor connected to outputs.

M502 — \$26

NEGATIVE INPUT CONVERTER

M506

**M
SERIES**



POWER

← A2 — +5V
 ← B2 — -15V
 ← C2, T1 — GRD
 -3 in => 0 OUT
 0 in => +3 OUT

The M506 contains three non-inverting signal converters which can be used to interface the negative logic levels or pulses of duration greater than 100 nsec to M and K Series positive logic levels of +3 volts and ground. These converters operate at frequencies up to 2 MHz with typical rise and fall propagation time of respectively 70 nsec and 40 nsec.

In addition, to the negative level inputs, each converter circuit has three additional NOR inputs for positive logic levels of +3 volts and ground. One of these inputs is tied to +3 volts so that unused inputs can be tied to a source of logic 1.

Inputs: All negative level inputs (A1, D2, . . . R2) present a 10 ma. at ground load.

Inputs B1, E2, . . . S2 present five TTL unit loads and can drive seven TTL unit loads at logic 1 if not used as an input.

All other inputs present 1 unit load.

Outputs: Each output can drive 10 TTL unit loads.

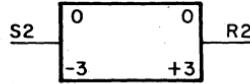
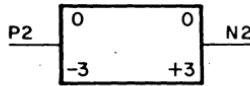
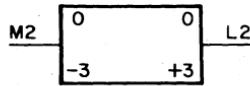
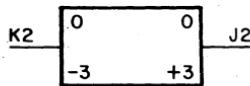
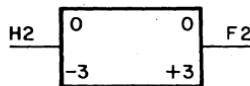
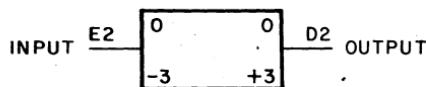
Power: +5 v at 81 ma. (max.); -15v at 115 ma. (max.).

M506 — \$53

BUS CONVERTER

M507

**M
SERIES**



POWER

← A2 — + 5V
← B2 — -15V
← C2 — GRD

INPUT
GRD
-3V

OUTPUT
GRD
+3V

The M507 contains six inverting level shifters which will accept -3 volts and GRD as inputs. The input to each level shifter consists of a 10 ma. clamped load and is diode protected against positive voltage excursions.

The output consists of an open collector NPN transistor. The output of each level shifter will sink 100 ma. to GRD. The maximum voltage which may be applied to the output is +20 volts. The output transistor is protected against negative voltage excursions by a diode connected between the collector and GRD. The output rise is delayed by 100 nsec. for pulse spreading.

The principle use of this module is to convert negative voltage logic levels or pulses of duration greater than 100 nsec.

Inputs: Input loading is equivalent to a 3 ma. clamped load.

Outputs: Each output can sink 100 ma. to GRD. Maximum voltage applied to any output is +20 volts.

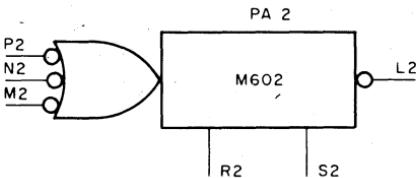
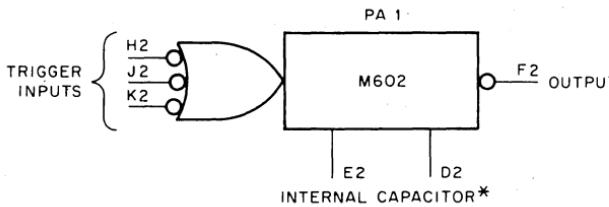
Power: +5 volts, 42 ma. (max.); -15 volts, 115 ma. (max.).

M507 — \$45

PULSE AMPLIFIER

M602

**M
SERIES**



POWER:
 ← A2 — +5V
 ← C2, T1 — GRD

* JUMPER E2-D2 OR R2-S2 FOR
 110 NSEC PULSE WIDTH. STAN-
 DARD PULSE WIDTH IS 50 NSEC.

The M602 contains two pulse amplifiers which provide power amplification, standardize pulses in amplitude and width, and transform level changes into a standard pulse. A negative pulse output is produced when the input is triggered by a transition from high to low. Propagation time between input and output thresholds is 30 nsec maximum. An internal capacitor is brought out to pin connections to permit the standard 50 nsec output pulse to be increased to 110 nsec (nominal). Recovery time is equal to that of the output pulse width. The input must have a fall time (10% to 90% points) of less than 400 nsec and must remain below 0.8 volts for at least 30 nanoseconds. Maximum PRF is 10 MHz.

Inputs: Each input presents 2½ unit loads.

Outputs: Each output is capable of driving 30 unit loads.

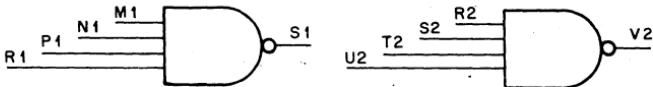
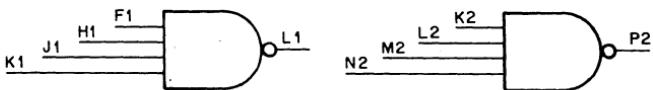
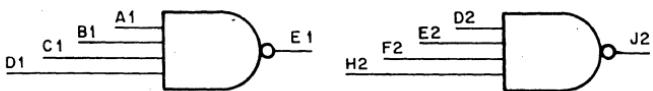
Power: +5 volts, 213 ma. (max.)

M602 — \$28

FOUR-INPUT POWER NAND GATE

M617

M
SERIES



POWER:

← A2 → + 5 V

← C2, T1 → GRD

+ 3 VOLTS — U1, V1 — UNUSED INPUTS

M617 POWER NAND GATE

The M617 contains 6 four-input NAND gates each capable of driving up to 30 unit loads. Typical gate propagation delay is 15 nsec. Physical configuration and logical operation are identical to the M117.

Inputs: Each input presents 1 unit load.

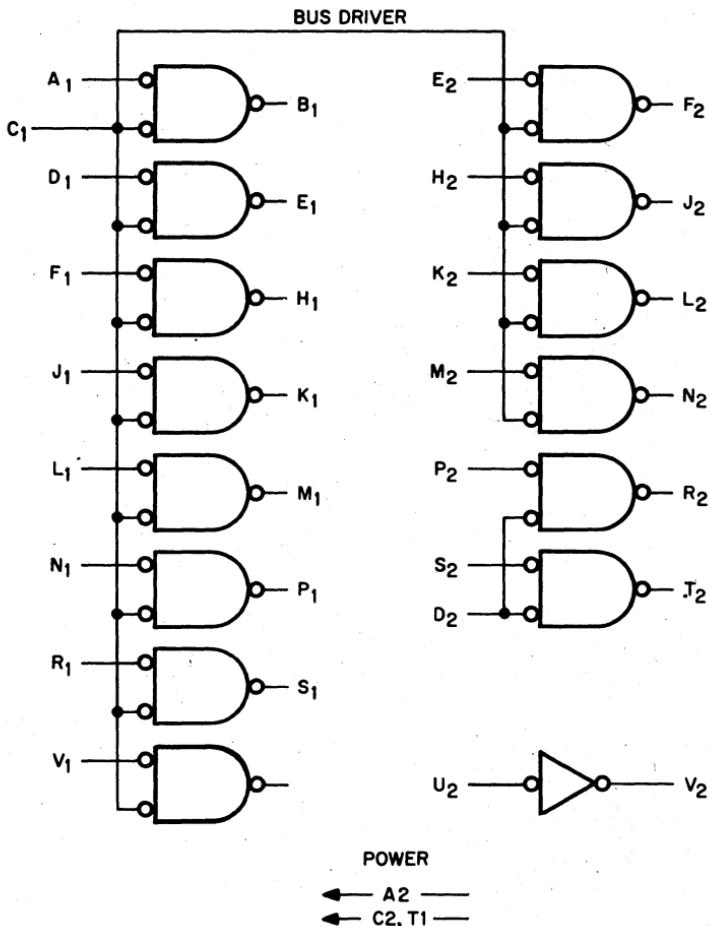
Outputs: Each output is capable of driving 30 unit loads.

Power: +5 volts, 97 ma. (max.).

M617 — \$27

BUS DRIVER M624

M
SERIES



The M624 contains fifteen bus drivers intended for convenient driving of the positive input bus of either the PDP-8I or PDP-8L. Twelve of the drivers have a common gate line and would be used for DATA. There are three additional drivers, two of which share a common gate line and the third without a gate line. These three additional drivers were intended to accommodate the functions of "Program Interrupt", "IO Skip" and "Clear AC".

Inputs: Pin C1 presents 12 TTL unit loads.
Pin D2 and U2 present two unit loads.
All other input pins present one unit load.

Outputs: All outputs can sink 100 ma. to ground. Voltage applied to the output should be equal to or less than +20 volts. The output consists of an open collector NPN transistor. Output rise and fall TTT are typically 30 nanoseconds when a 100 ma. resistive load to +5.0 volts is connected to a driver output.

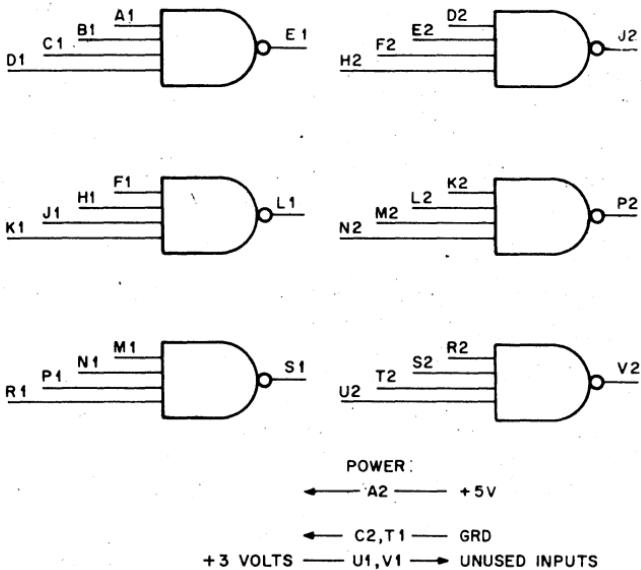
Power: +5 volts, 89 ma. (max.). (Driver outputs not connected).

M624 — \$45

NAND POWER AMPLIFIER

M627

M
SERIES



M627 NAND POWER AMPLIFIER

The M627 combines power amplification with high-speed gating, specifically for high fan-out of clock or shift pulses to expanded counters and shift registers. Propagation time between input and output transitions is typically 6 nsec. To utilize the timing accuracy of this module, wire runs of minimum length are recommended.

The module may also be used as a four-input NAND gate. In the pulse amplifier application, unused inputs should be connected to the +3 volt pins provided.

Inputs: Each input presents 2½ unit loads.

Outputs: Each output is capable of driving 40 unit loads.

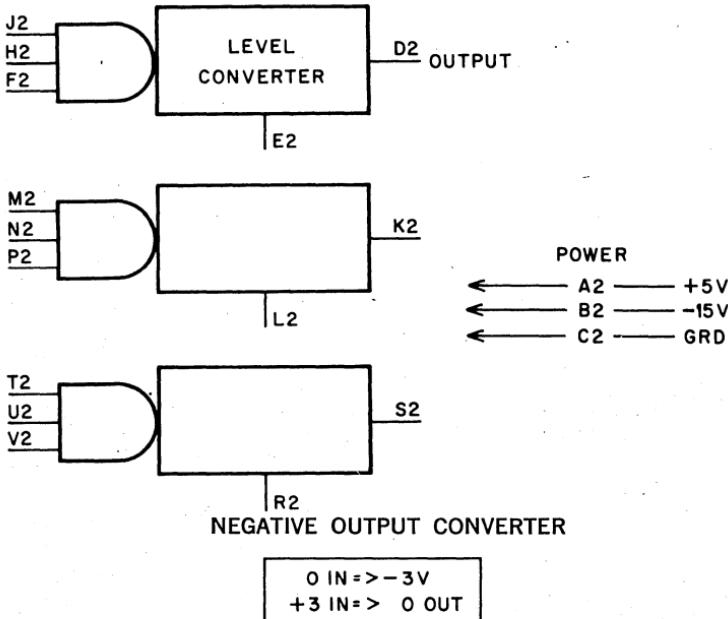
Power: +5 volts, 136 ma. (max.)

M627 — \$32

NEGATIVE OUTPUT CONVERTER

M650

**M
SERIES**



The M650 contains three non-inverting signal converters which can be used to interface the positive logic levels or pulses (of duration greater than 100 nsec) of K and M series to DIGITAL negative logic levels of -3 volts and ground. These converters provide current drive at a low output impedance so that unterminated cables or wires can be driven with a minimum of ringing and reflections.

The converters operate at frequencies up to 2 Mc with maximum rise and fall total transition of respectively 75 nsec and 115 nsec. By grounding pin E2 (L2 or R2) the rise and fall total transition times can be increased to avoid ringing on exceptionally long lines. The converter then operates at frequencies up to 500 KHz with typical rise and fall total transition times of 500 nsec.

A positive AND condition at the input gate produces a ground output. If any input is at ground the converter output is at -3 volts.

Inputs: Each input presents 1 unit load.

Outputs: Each output is capable of driving ma. at ground and at -3 volts.

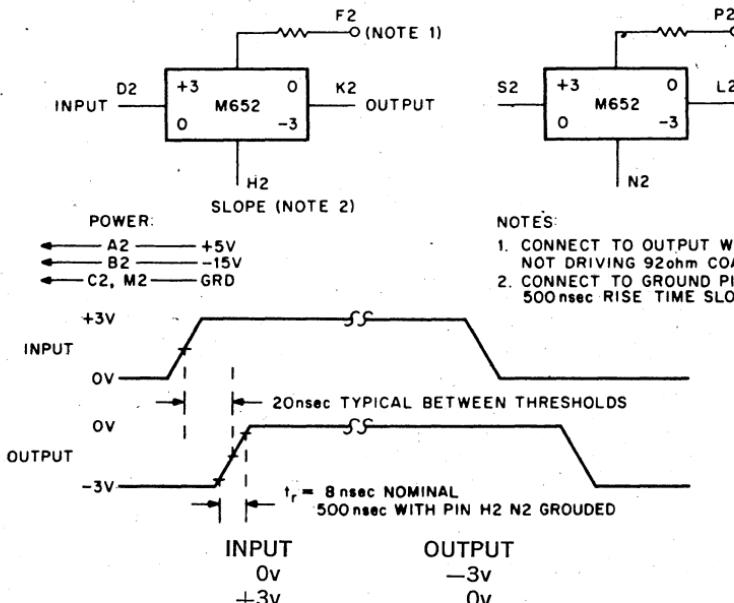
Power: +5 volts, 37 ma. (max.); -15 volts, 29 ma. (max.)

M650 — \$25

NEGATIVE OUTPUT CONVERTER

M652

**M
SERIES**



The M652 contains two non-inverting high-speed signal converters which can be used to interface the positive logic levels or pulses of the K and M Series to DIGITAL negative logic levels of -3 volts and ground. These converters provide current drive at a low output impedance so that system interconnections can be made using terminated 92-ohm coaxial cable. The converters operate at frequencies up to 10 MHz with typical output rise and fall times of 8 nsec. Propagation times for output rise and fall are typically 20 nsec. The slope of the output transition can be decreased by grounding an internal RC network, to avoid ringing on exceptionally long lines. The converter then operates at frequencies up to 1 MHz.

Inputs: Positive logic levels of 0 and +3 volts (nominal). Input loading is 2 unit loads. Input signals more positive than +6 volts will damage the circuit.

Outputs: Each output can drive terminated 92 ohm coaxial cable and supply an additional 20 ma. at ground or sink an additional 20 ma. at -3 volts. Output rise and fall times are dependent on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds will be increased by connecting the 100-ohm resistor to the output.

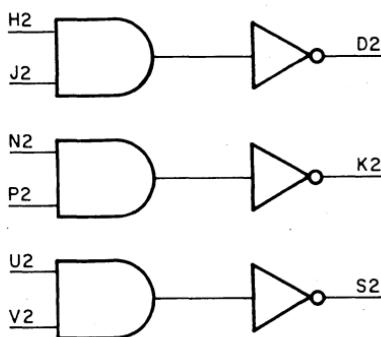
Power: +5 volts, 122 ma. (max.); -15 volts, 202 ma. (max.)

M652 — \$26

POSITIVE LEVEL DRIVER

M660

M
SERIES



POWER

A2 ————— +5V

C2 ————— GRD

+3 IN => 0 OUT
0 IN => +3 OUT

The M660 Cable Driver consists of three circuits each of which will drive 100 ohm terminated cable with M Series levels or pulses whose duration is greater than 100 nsec.

Inputs: Each input represents 1 unit load.

Outputs: M Series logic levels with 50 ma. drive current at logic "1" or "0".

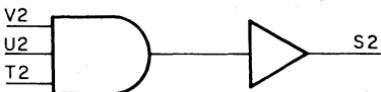
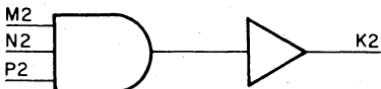
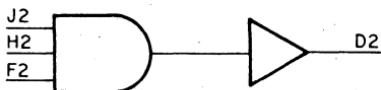
Power: +5v, 71 ma. (max.)

M660 — \$25

POSITIVE LEVEL DRIVER

M661

M
SERIES



POWER

← A2 → +5V
← C2 → GRD

+3 IN => +3 OUT
0 IN => 0 OUT

The M661 contains three circuits which may be used to drive low impedance unterminated cable with M Series logic levels or pulses whose duration is 100 nsec or greater.

Inputs: Each input represents 1 unit load.

Outputs: M Series logic "1" at 5 ma.
M Series logic "0" at 20 ma.

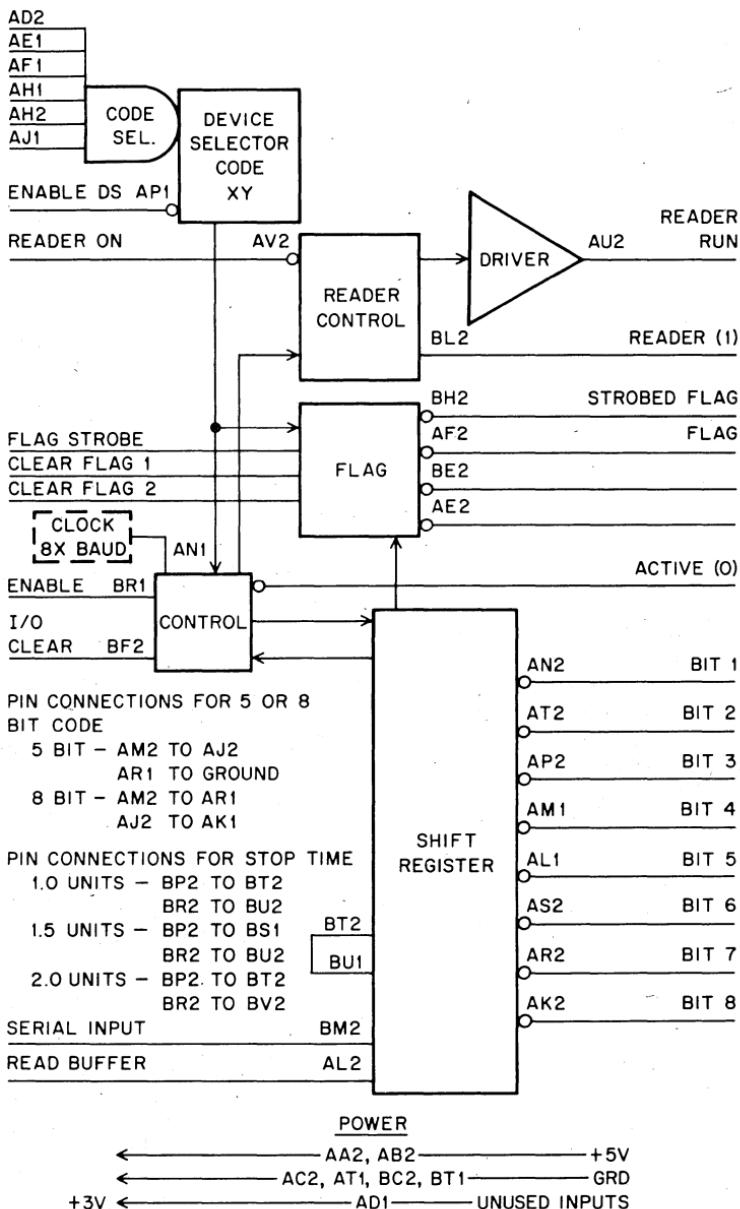
Power: +5v, 111 ma. (max.)

M661 — \$15

TELETYPE RECEIVER

M706

**M
SERIES**



The M706 Teletype Receiver is a serial-to-parallel teletype code converter self contained on a double height module. This module includes all of the serial-to-parallel conversion, buffering, gating, and timing (excluding only an external clock necessary to transfer information in an asynchronous manner between a serial data line or teletype device and a parallel binary device). Either a 5-bit serial character consisting of 7.0, 7.5, or 8.0 units or an 8-bit serial character of 10.0, 10.5, or 11.0 units can be assembled into parallel form by the M706 through the use of different pin connections on the module. When conversion is complete, the start and stop bits accompanying the serial character are removed. The serial character is expected to be received with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with reception of the center of bit eight, the Flag output goes low indicating that a new character is ready for transmission into the parallel device. The parallel data is available at the Bit 1 through Bit 8 outputs until the beginning of the start bit of a new serial character as received on the serial input. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M706 includes the necessary logic to provide rejection of spurious start bits less than one-half unit long, and half-duplex system operation in conjunction with the M707. Device selector gating is also provided so that this module can be used on the positive I/O bus of either the PDP8/I or the PDP8/L. To obtain additional applications information on the M706, write for Applications Note AP-M-013.

Inputs: All inputs present one TTL unit load except where noted. When input pulses are required, they must have a width of 50 nsec or greater.

Clock: The clock frequency must be eight times the serial input bit rate (baud rate). This input can be either pulses or a square wave. Input loading on the clock line is three unit loads.

Enable: This input when brought to ground will inhibit reception of new characters. It can be grounded any time during character reception, but returned high only between the time the Flag output goes to ground and a new character start bit is received at the serial input. When not used this input should be tied to a source of +3 volts.

I/O Clear: A high level or positive pulse at this input clears the Flag and initializes the state of the control. When not used, or during reception, this input should be at ground.

Code Select Inputs: When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Read Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex receiver modules when a signal like Read Buffer is common to many modules. The inputs can also be used for device Selector inputs when the M706 is used on the positive I/O bus of the PDP8/I or PDP8/L. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to bypass the code select inputs, they can be left open and the Enable D.S. line tied to ground.

Clear Flag 1: A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared is a maximum of 100 nsec. The Flag cannot be set if this input is held high.

Clear Flag 2: A high level or positive pulse at this input, independent of the state of the code select inputs, will clear the Flag. All other characteristics are identical to those of Clear Flag 1.

Flag Strobe: If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

Read Buffer: A high level or positive pulse at this input while the code select inputs are all high will transfer the state of the shift register to outputs Bit 1 through Bit 8. Final parallel character data can be read by this input as soon as the Flag output goes to ground. Output data will be available a maximum of 100 nsec after the rising edge of this input. See the timing diagram of Figure 1 for additional information.

Reader On: A low level or ground at this input will turn the internal reader flip-flop on. This element is turned off at the beginning of a received character start bit. This input can also be pulsed by tying it to one of the signals derived at output pins AE2 or BE2.

Serial Input: Serial data received on this input is expected to have a logical zero (space) equal to +3 volts and a logical 1 (mark) of ground. The input receiver on the M706 is a schmitt trigger with hysteresis thresholds of nominally 1.0 and 1.7 volts so that serial input data can be filtered up to 10% of bit width on each transition to remove noise. This input is diode protected from voltage overshoot above +5.9 volts and undershoot below -0.9 volts. Input loading is four unit loads.

Outputs: All outputs can drive ten unit loads unless otherwise specified.

Bits 1 through 8: A read Buffer input signal will transfer the present shift register contents to these outputs with a received logical 1 appearing as a ground output. If the Read Buffer input is not present, all outputs are at logical 1. When the M706 is used for reception of 5-bit character codes, the output data will appear on output lines Bit 1 through 5 and bits 6, 7, 8 will have received logical zeros.

Active (0): This output goes low at the beginning of the start bit of each received character and returns high at the completion of reception of bit 8 for an 8-bit character or of bit 5 for a 5-bit character. Since this signal uses from ground to +3 volts one-half bit time after the Flag output goes to ground, it can be used to clear the flag through Clear Flag 2 input while the Flag Output after being inverted can strobe parallel data out when connected to Read Buffer.

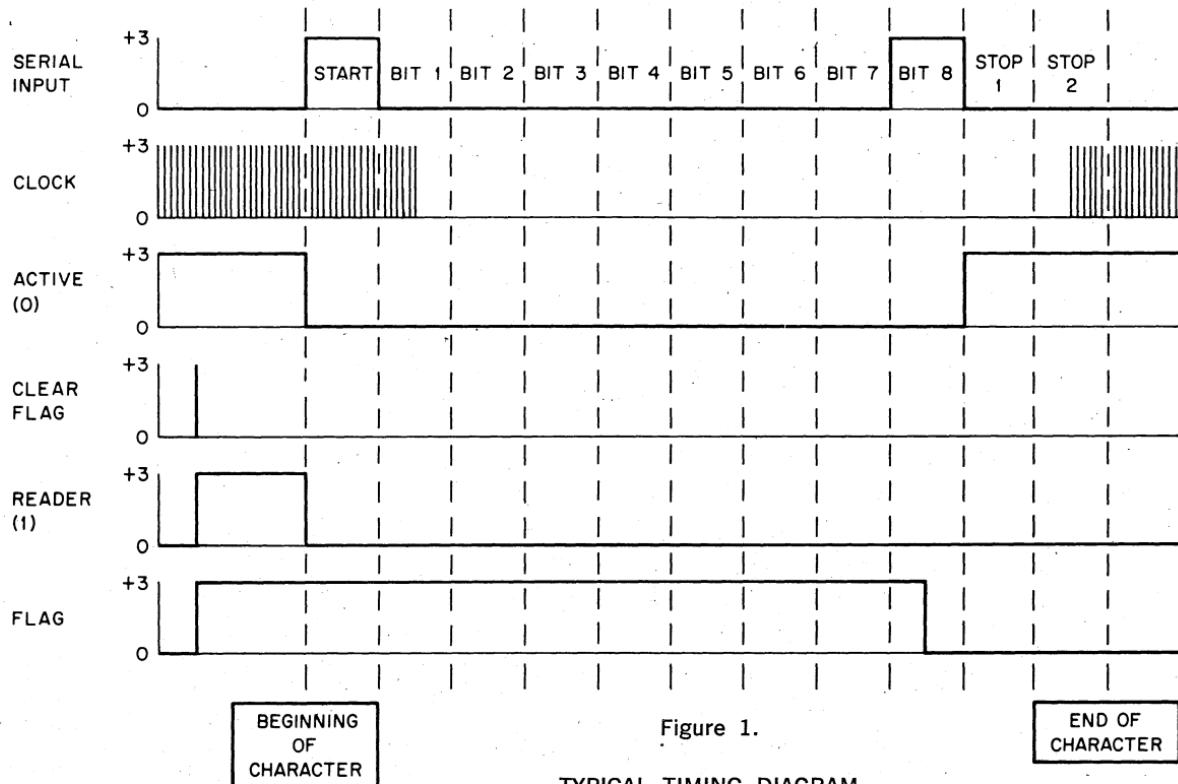


Figure 1.

TYPICAL TIMING DIAGRAM
Serial Input-Parallel Output 8-Bit (01, 111, 111)-2 Unit Stop Time

If an M706 and M707 are to be used in half duplex mode, this output should be tied to the Wait input of the M707 to inhibit M707 transmission during M706 reception. Output drive is eight unit loads.

Flag: This output falls from +3 volts to ground when the serial character data has been fully converted to parallel form. Relative to serial bit positions, this time occurs during the center of either bit 8 or bit 5 depending respectively on the character length. If the M706 is receiving at a maximum character rate, i.e. one character immediately follows another; the parallel output data is available for transfer from the time the Flag output falls to ground until the beginning of a new start bit. This is Stop bit time plus one-half bit time.

Strobed Flag: This output is the NAND realization of the inverted Flag output and Flag Strobe.

Reader (1): Whenever the internal reader flip-flop is set by the Reader ON input, this output rises to +3 volts. It is cleared whenever a start bit of a new character received on the serial input.

Reader Run: For use with Digital modified ASR33 and ASR35 teletypes which have relay controlled paper tape readers. This output can drive a 20 ma at +0.7 volts load. The common end of the load can be returned to any negative voltage not exceeding -20 volts.

Pin AE2: This output is the logical realization of NOT (Clear Flag 1 or Clear Flag 2 or I/O Clear) and is a +3 volts to ground output level or pulse depending on the input. This signal can be used to pulse Reader On for control of Reader Run as used in DEC PDP8/I or PDP8/L computers.

Pin BE2: This output is brought from +3 volts to ground by an enabled Clear Flag 1 input. It can be connected to Reader On for a different form of control of Reader Run.

+3 Volts: Pin AD1 can drive ten unit loads at a +3 volt level.

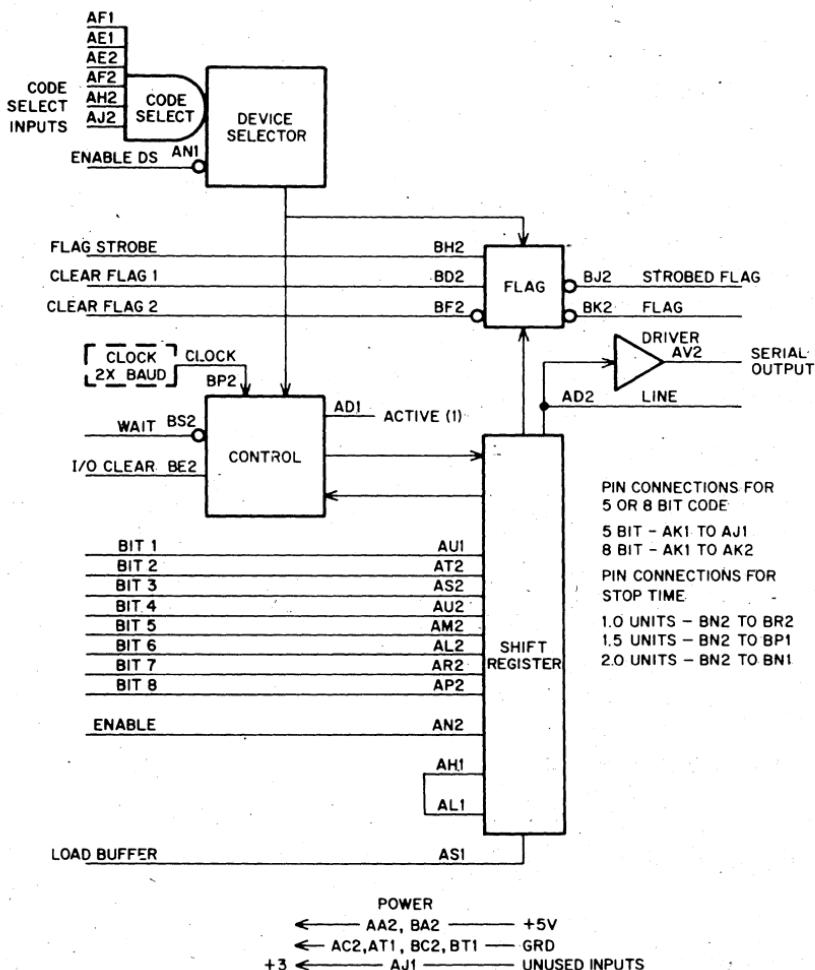
Power: +5 volts at 400 ma. (max.).

M706 — \$175

TELETYPE TRANSMITTER

M707

**M
SERIES**



The M707 Teletype Transmitter is a parallel-to-serial teletype code converter self contained on a double height module. This module includes all of the parallel-to-serial conversion, buffering, gating, and timing (excluding only an external clock) necessary to transfer information in an asynchronous manner between a parallel binary device and a serial data line or teletype device. Either a 5-bit or an 8-bit parallel character can be assembled into a 7.0, 7.5, or 8.0 unit serial character or a 10.0, 10.5, or 11.0 unit serial character by the M707 through the use of different pin connections on the module. When conversion is complete, the necessary start bit and selected stop bits (1.0, 1.5, or 2.0 units) have been added to the original parallel character and transmitted over the serial line. The serial character is transmitted with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with the stop bit being put on the serial line, the Flag output goes low indicating that the previous character has been transmitted and a new parallel character can be loaded into the M707. Transmission of this new character will not occur until the stop bits from the previous character are completed. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M707 includes the necessary gating so that it can be used in a half-duplex system with the M706. Device selector gating is also provided so that this module can be used on the positive bus of either the PDP8/I or the PDP8/L. To obtain additional applications information on the M707 write for Applications Note AP-M-013.

Inputs: All inputs present one TTL unit load with the exception of the Clock input which presents ten unit loads. Where the use of input pulses is required, they must have width of 50 nsec or greater.

Clock: The clock frequency must be twice the serial output bit rate. This input can be either pulses or a square wave.

Bits 1 through 8: A high level at these inputs is reflected as a logic 1 or mark in the serial output. When a 5-bit code is used, bit inputs 1 through 5 should contain the parallel data, bit 6 should be considered as an Enable, and bits 7, 8 and Enable should be grounded.

Enable: This input provides the control flexibility necessary for transmitter multiplexing. When grounded during a Load Buffer pulse, this input prevents transmission of a character. It can be driven from the output of an M161 for scanning purposes or in the case of a single transmitter, simply tied to +3 volts.

Wait: If this input is grounded prior to the stop bits of a transmitted character, it will hold transmission of a succeeding character until it is brought to a high level. A ground on this line will not prevent a new character from being loaded into the shift register. This line is normally connected to Active (0) on a M706 in half duplex two wire systems. When not used, this line should be tied to +3 volts.

Code Select Inputs: When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Load Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex transmitter modules when signals like Load Buffer are common to many modules. These inputs can also be used for device selector inputs when the M707 is used on the positive bus of the PDP8/I or PDP8/L. The

code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to by-pass the code select inputs, they can be left open and the Enable DS line tied to ground.

Clear Flag 1: A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared at the Flag output is a maximum of 100 nsec. The Flag cannot be set if this input is held at logic 1.

Clear Flag 2: A low level or negative pulse at this input will clear the Flag. When not used this input should be tied to +3 volts. The Flag will remain cleared if this input is grounded. Propagation from input fall to Flag output rise is a maximum of 80 nsec. If it is desired to clear the flag on a load buffer pulse, Clear Flag 2 can be tied to pin AR1 of the module.

Flag Strobe: If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

I/O Clear: A high level or positive pulse at this input clears the Flag, clears the shift register and initializes the state of the control. This signal is not necessary if the first serial character transmitted after power turn-on need not be correct. When not used, or during transmission, this input should be at ground.

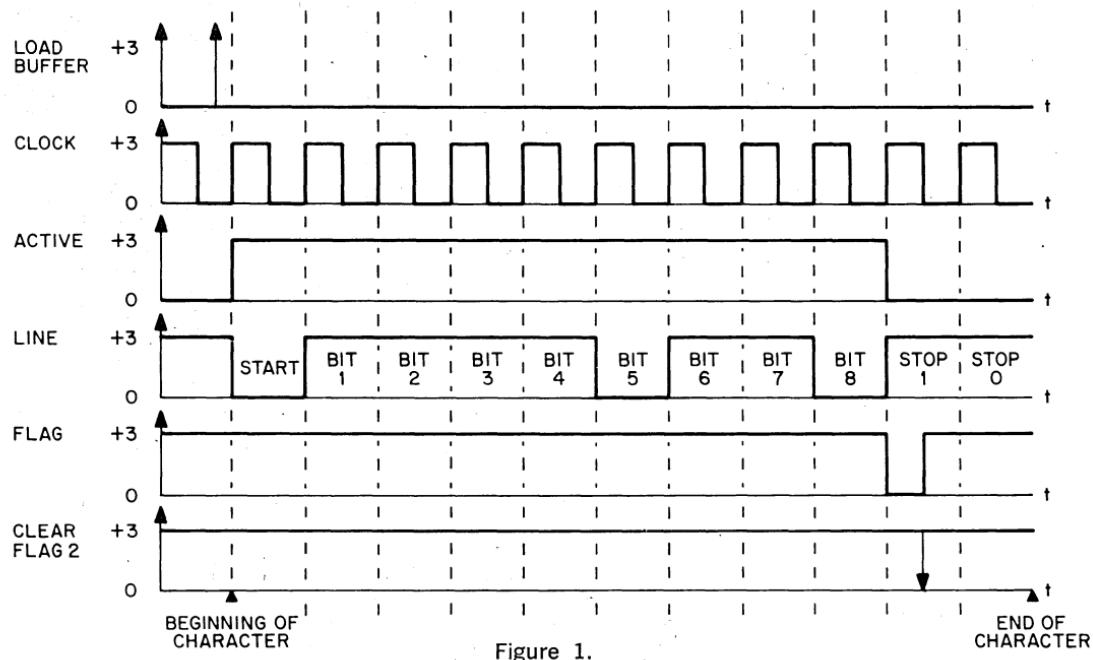
Load Buffer: A high level or positive pulse at this input while the code select inputs are all high will load the shift register buffer with the character to be transmitted. If the Enable input is high when this input occurs, transmission will begin as soon as the stop bits from the previous character are counted out. If a level is used, it must be returned to ground within one bit time (twice the period of the clock).

Outputs: All outputs present TTL logic levels except the serial output driver which is an open collector PNP transistor with emitter returned to +5 volts.

Serial Output: This open collector PNP transistor output can drive 20 ma into any load returned to a voltage between +4 volts and -15 volts. A logical output or mark is +5 volts and a logical 0 or space is an open circuit. If inductive loads are driven by this output, diode protection must be provided by connecting the cathode of a high speed silicon diode to the output and the diode anode to the coil supply voltage.

Line: This output can drive ten TTL unit loads and presents the serial output signal with a logical 1 as +3 volts and logical 0 as ground.

Active: During the time period from the occurrence of the serial start bit and the beginning of the stop bits, this output is high. This signal is often used in half duplex systems to obtain special control signals. Output drive is eight TTL unit loads.



Typical Timing Diagram, Parallel
input, 8-Bit Character (11, 110, 110) With two bit Stop time.

Flag: This output falls from +3 volts to ground at the beginning of the stop bits driving a character transmission. The M707 can now be reloaded and the Flag cleared (set to +3 volts). This output can drive ten TTL unit loads.

Strobed Flag: This output is the NAND realization of the inverted Flag output and Flag Strobe. Output drive is ten TTL unit loads.

+3 volts: Pin BJ1 can drive ten TTL unit loads at a +3 volt level.

Power: +5 volts at 375 ma. (max.)

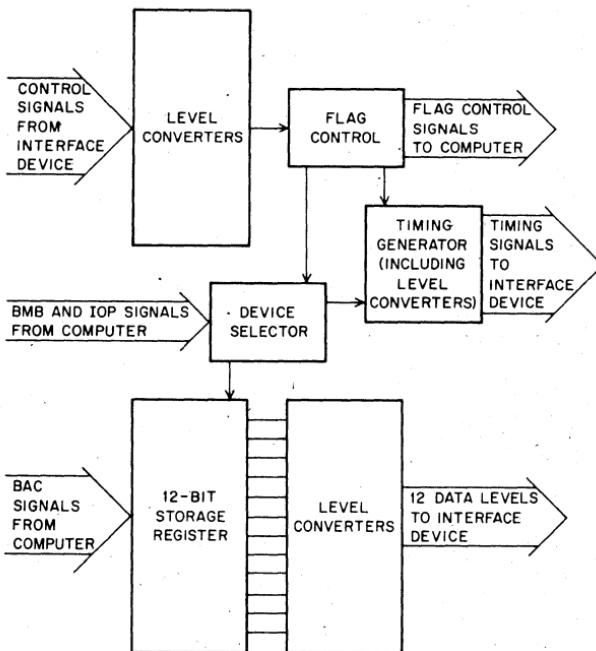
M707 — \$175



These pantograph-controlled insertion machines position and crimp pre-tested components onto four module boards at a time. A press will cut the modules apart after assembly is completed, minimizing handling up to that point.

BUS INTERFACE TYPES M730 & M731

M
SERIES



The M730 and M731 interface modules provide extremely flexible interface control logic to connect devices, systems, and instruments to the output half of the programmed I/O transfer bus of either a PDP8/I or a PDP8/L positive bus computer. Peripheral equipment which operates either asynchronously or synchronously to a computer and expects to receive data from that computer, can to a large degree be interfaced by either the M730 or M731. Basic restrictions on the device or system to be interfaced are simply that it receive data in parallel, provide one or more control lines, and operate at a data transfer rate of less than 20 KHz. Complete interfaces to such peripheral gear as card punches and other repetitive devices is possible using the M730 and M731; however part of the controlling functions, such as counting etc. must be performed by computer software.

Functionally, these modules contain five distinct sections which are as follows:

1. Device Selector—This logic network converts the buffered memory buffer (BMB) signals and IOP timing pulses from the computer into internal module control pulses.
2. Timing Generator—Through the use of device selector signals, control signals from the interfaced device, and module jumpers, this unit can supply variable width pulses or synchronous control levels at amplitudes specified in section 5 below.
3. Storage Register—This 12-bit flip-flop buffer register provides output data storage for information to be transmitted to the interfaced device.
4. Flag Control—Provisions for generation of I/O Skip and Program Interrupt signals for the computer are made in this area.
5. Level Converters—All level converters from the storage register or timing generator are open-collector transistor types which can drive 30 ma at ground. The M730 has npn drivers and can interface loads returned to a maximum positive supply of +20 volts and the M731 has pnp drivers which can interface loads returned to a maximum negative supply of -20 volts. Level converters which input control signals to the Flag control can receive signals of the same polarity and magnitude as the output drivers can sustain.

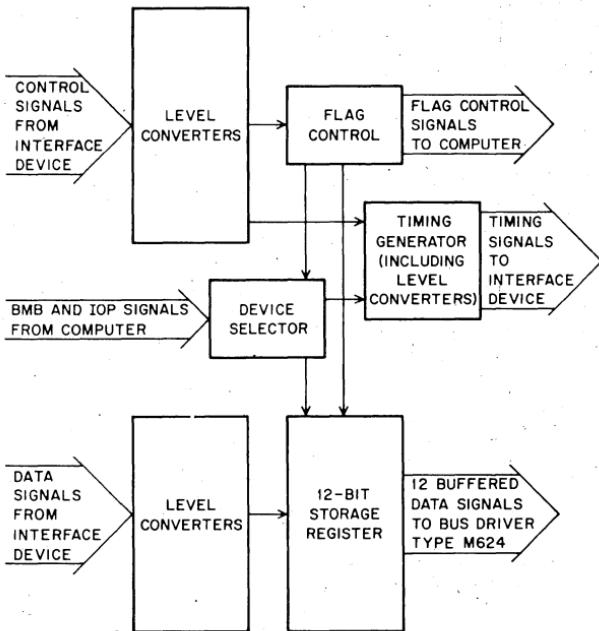
Thresholds on the input converters are +1.5 volts and -1.5 volts for the M730 and M731 respectively. All positive voltage levels are compatible with K and M series and all negative voltage signals are compatible with R, B and W Series.

For additional information, technical specifications and applications assistance, a Digital module specialist can be contacted at any Digital Sales office. Application Note AP-M-017 contains useful information concerning the use of the M730 and M731.

M730 — \$185
M731 — \$185

BUS INTERFACE TYPES M732 & M733

M
SERIES



The M732 and M733 interface modules provide extremely flexible interface control logic to connect devices, systems, and instruments to the input half of the programmed I/O transfer bus of either a positive bus PDP8/I or PDP8/L computer. Peripheral equipment which operates either asynchronously or synchronously to a computer and expects to transmit data to that computer, can to a large degree be interfaced by either the M732 or M733. Basic restrictions on the device or system to be interfaced are simply that it transmit data in parallel, provide one or more control lines, and operate at a data transfer rate of less than 20KHZ. Complete interfaces to such peripheral gear as card readers and other repetitive devices is possible using the M732 and M733; however, part of the controlling functions such as counting, etc., must be performed by computer software.

Functionally, these modules contain five distinct sections which are as follows:

1. Device Selector—This logic network converts the buffered memory buffer (BMB) signals and IOP timing pulses from the computer into internal module control pulses.
2. Timing Generator—Through the use of device selector signals, control signals from the interfaced device, and module jumpers, this unit can supply variable width pulses or synchronous control levels at amplitudes specified in section 5 below.
3. Storage Register—This 12-bit flip-flop buffer register provides input data storage of information received from the interfaced device. Information is loaded into this register by a control line from the peripheral.
4. Flag Control—Provisions for generation of I/O Skip and Program Interrupt signals for the computer are made in this area.
5. Level Converters—All level converters from the timing generator are open collector transistor types which can drive 30 ma at ground. The M732 has npn drivers and can interface loads returned to a maximum positive supply of +20 volts and the M733 has pnp drivers which can interface to a maximum negative supply of -20 volts. Level converters which input control and data signals to these modules can receive signals of the same polarity and magnitude as the output drivers can sustain. Thresholds on the input converters are +1.5 volts and -1.5 volts for the M732 and M733 respectively.

All positive voltage levels are compatible with K and M Series and all voltage signals are compatible with R, B, and W Series.

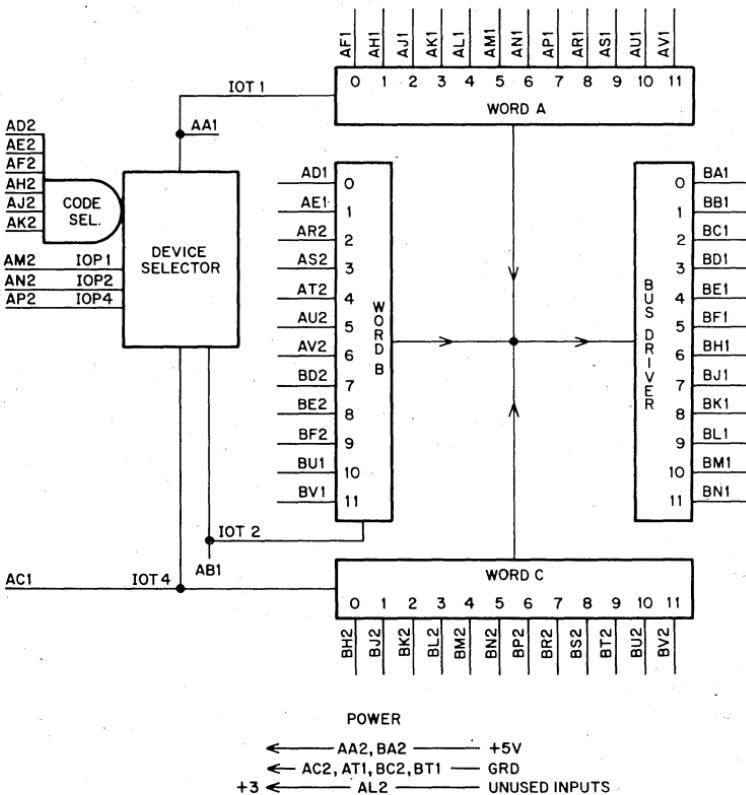
For additional information, technical specifications and applications assistance, a Digital module specialist can be contacted at any Digital Sales Office. Application Note AP-M-018 contains useful information concerning the use of the M732 and M733.

M732 — \$185.00
M733 — \$190.00

I/O BUS INPUT MULTIPLEXER

M734

**M
SERIES**



The M734 is a double height, single width module and is a three word multiplexer used for strobing twelve-bit words on the positive voltage input bus; usually the input of the PDP8/I or the PDP8/L. Device selector gating is provided. The data outputs of the M734 Multiplexer consist of open collector npn transistors which allow these outputs to be directly connected to the bus. All inputs present one TTL unit load and function as follows:

Code select Inputs: When a positive AND condition occurs at these inputs, the pulse inputs IOP1, IOP2, and IOP4 are enabled for use in strobing input data. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If all select inputs are not required, unused inputs must be tied to a source of +3 volts (Pin AL2). These inputs are all clamped so that no input can go more negative than -0.9 volts.

IOP1, 2, 4: These three 50 nsec or longer positive pulse inputs strobe respectively 12-bit words A, B, and C into the bus driver. All three lines are clamped so that no input can go more negative than -0.9 volts.

Data inputs: Bit 0-11 on words A, B, and C are strobed in 12-bit words as above. Bus driver output lines correspond numerically (0-11) to the selected word input lines (0-11). A high data input will force a bus driver output to ground during a data strobe. Inputs must be present at least 30 nsec prior to issuance of IOP 1, 2, or 4.

Bus driver: These open collector npn transistor bus driver outputs can sink 30 ma at ground. The maximum output voltage must not exceed +20 volts. Each driver output is protected from negative undershoot by a diode clamp. When this module is used with the PDP8/I or PDP8/L, these outputs would be connected to the accumulator input lines of the I/O bus. Typical rise and fall TTT at these outputs with a 30 ma resistive load are 100 nsec.

Data Strobes: Pins AA1, AB1, and AC1 can each drive 18 TTL unit loads. These outputs appear coincident with IOP1, IOP2, and IOP4 respectively only if the code select inputs are all high.

+3V—Pin AL2 can drive 19 inputs at a high logic level.

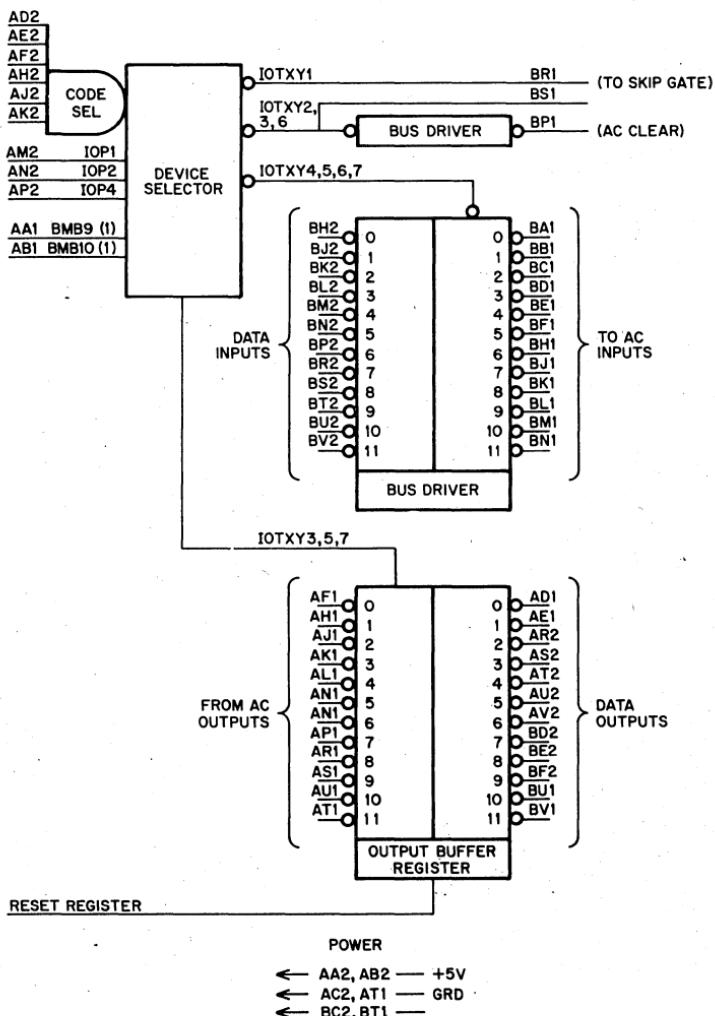
Power: +5 volts at 290 ma. (max.).

M734 — \$110.00

I/O BUS TRANSFER REGISTER

M735

**M
SERIES**



The M735 provides one 12-bit input bus driver and one 12-bit output buffer register for input and output data transfers on the positive I/O bus of either a PDP8/I or a PDP8/L. Device selector gating plus additional signal lines provide the flexibility necessary for a complete interface with the exception of flag sense signals. Use of the M735 is not restricted to a computer, as it can be used in many systems to provide reception and transmission of data over cables.

Inputs:

All inputs present one TTL unit load with few exceptions as noted in the functional descriptions below:

Code Select Inputs: When a positive AND condition occurs at these inputs, the pulse input gates for IOP1, IOP2, and IOP4 are enabled for use as detailed below. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If all select inputs are not required, unused inputs must be tied to a source of +3 volts. These inputs are all clamped so that no input can go more negative than -0.9 volts. When this module is used with the PDP8/I or PDP8/L these inputs would be connected to BMB outputs 3-8 to generate a device code. Where required in discussions below, this 6-bit device code will be referred to as code XY.

IOP1, 2, 4, BMB9(1) and BMB10(1): These three IOP's 50 nsec or longer positive pulse inputs, in conjunction with control level inputs BMB9(1) (Pin AA) and BMB10(1) (Pin AB1) provide all of the necessary signals for operation of this module. Table 1 below indicates the recommended use of these pulses and levels. A "1" or "0" in this table indicates the presence or absence respectively of a pulse (an IOP) or the logic level at pins AA1 or AB1.

The M735 module operation as associated with the various mnemonic IOT codes is quite explicit with the exception of IOTXY5. This code (IOTXY5) would be used to load zeros into the M735 with IOTXY1 and then to load into the AC the data present at the data inputs of the bus driver when IOTXY4 occurs. In this particular operation the AC has been effectively cleared as the content of the AC was zero during IOTXY1 thereby allowing the transfer of data into the AC without the use of the AC clear command usually generated by IOT2.

IOP 4	IOP 2	IOP 1	BMB 9(1)	BMB 10(1)	PDP/8 Mnemonic	Module Operation
0	0	1	0	0	IOTXY1	+3V → OV output pulse on pin BR1 used for skip function.
0	1	0	0	1	IOTXY2	+3V → OV output pulse on pin BS1, bus driver output on BP1 pulsed to ground and is used for the AC clear function.
0	1	1	0	1	IOTXY3	Load output register from accumulator outputs on IOP1 execute IOTXY2.
1	0	0	1	0	IOTXY4	Data inputs strobed onto accumulator inputs.
1	0	1	1	0	IOTXY5	Load output register on IOP1, Execute IOTXY4.
1	1	0	1	1	IOTXY6	Execute IOTXY2, and IOTXY4.
1	1	1	1	1	IOTXY7	Execute IOTXY3, and IOTXY4.

Although it is not implicit from Table 1, BMB9(1) and BMB10(1) inputs are gated in a positive OR circuit, so that when the M735 is not used on a PDP8/I or PDP8/L I/O bus one of these inputs can be grounded and the other used for control. They must appear at least 50 nsec prior to an IOP pulse. If the M735 is used with one of the above computers, these inputs must be tied to the corresponding I/O bus lines. The input load on IOP1 is two TTL unit loads. All five inputs are clamped so that no input can go more negative than -0.9 volts.

Data Inputs: Each data input when at ground, enables the corresponding bus driver output to be pulsed to ground during IOTXY4. A high input will inhibit the bus driver from being strobed. Since each input is ANDed with IOTXY4, any change of data after this strobe begins will change the bus driver output.

Accumulator Inputs: The input level presented to these inputs will be the same as that assumed by the buffer outputs after executing inputs strobes IOTXY , 5, or 7. Input data must be present at least 50 nsec prior to an IOP. Each input is protected from negative undershoot by a diode clamp.

Reset Register Pin AL2: A positive pulse of 50 nsec or longer at this input sets all buffer outputs to ground. When high, this input overrides any data loading from the accumulator inputs. The output register will be cleared within 70 nsec from the rising edge of this input. Diode input clamping is provided to limit negative undershoot to -0.9 volts.

Outputs:

Pin BR1: This output can drive ten TTL unit loads and has a propagation delay of less than 20 nsec. See Table 1.

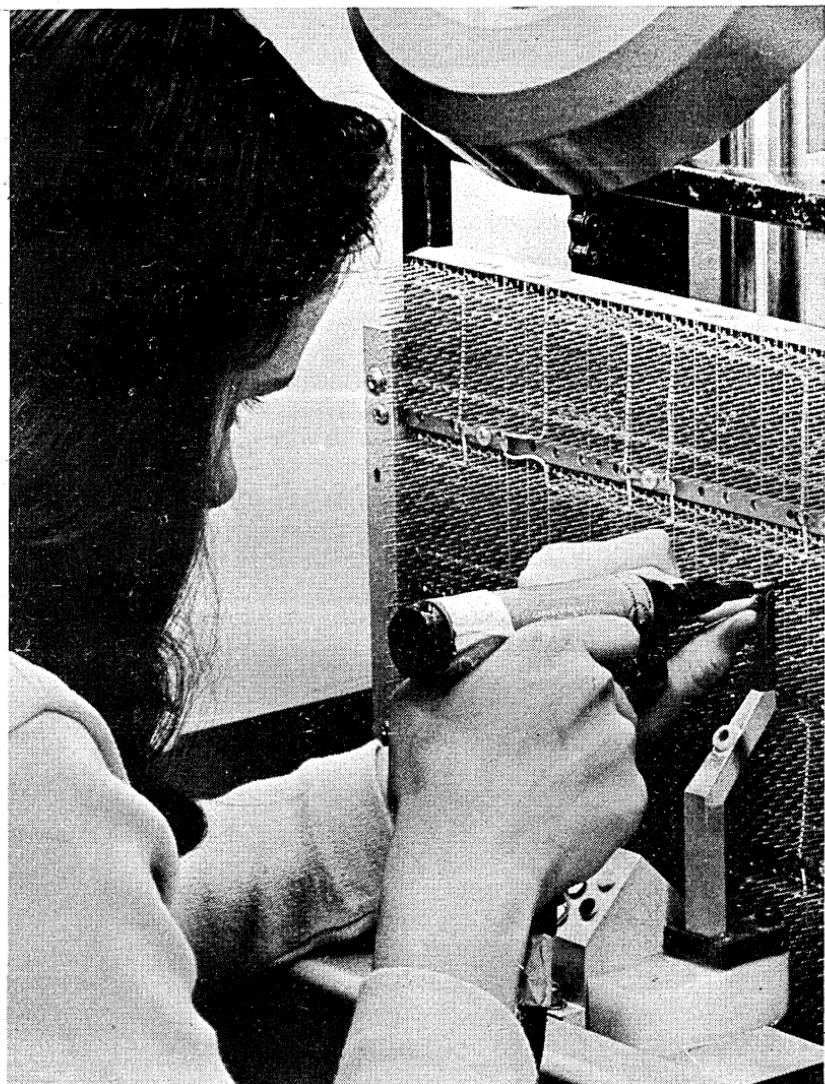
Bus Driver: These open collector npn transistor bus driver outputs, including pin BP1, can sink 30 ma. at ground. The maximum output voltage cannot exceed +20 volts and each driver output is protected from negative undershoot by a diode clamp. When this module is used with the PDP8/I or PDP8/L,

output pins BA1—BN1 would be connected to the accumulator input lines and pin BP1 to the clear accumulator line of the I/O bus. Typical rise and fall TTT of these outputs with a 30ma resistive load are 100 nsec.

Buffer Outputs: Each output can drive ten TTL unit loads.

Power: +5 volts at 385 ma. (max.)

M735 — \$140

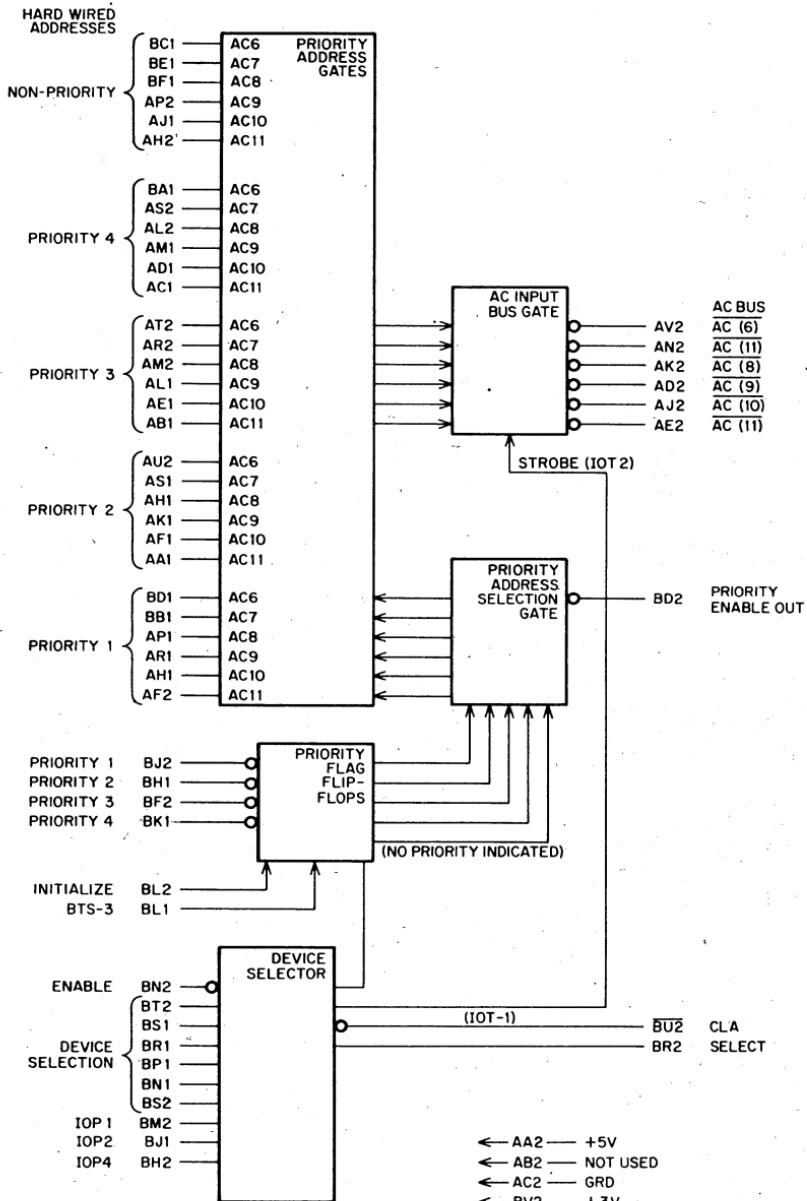


The computer-controlled, semi-automatic wire wrap automatically locates the correct pin and helps position the wire wrap tool for complex back panel wiring. This operation makes it possible for DEC to wire wrap all of its systems with great speed and accuracy and pass on a substantial savings to its customers.

PRIORITY INTERRUPT MODULE

M736

**M
SERIES**



The M736 is used in conjunction with the PDP8/I or 8/L to provide the capability of assigning priorities to various I/O devices connected to the I/O bus of the computer. The M736 can be used to assign priorities for one thru four external devices. Priority assignment may be provided for more than four devices by using additional M736 modules for each additional group of four devices. All M736's in a particular priority system would utilize the same device code.

THEORY OF OPERATION

Basically the M736 module consists of the following:

1. The M103 device selector function.
2. A Bit Time State-3 (BTS-3) input.
3. Four priority input lines.
4. Priority enable line, input and output.
5. Five groups of six gates, each of which is capable of being hard wired to provide address information to locate subroutines to service the various devices associated with the priority interrupt system. The output of each of these gates is strobed onto the accumulator input bus on lines AC(6) thru AC(11).

SEQUENCE OF OPERATION

The external device activates its skip and/or interrupt FLAG flip-flop. The activation of the FLAG causes two things to happen; (a) The computer's interrupt request line is pulled to ground. This tells the computer that an external device requires service and requests the computer to jump to an I/O priority interrupt service subroutine as soon as the computer completes its present cycle. (b) The external device FLAG pulls to ground the appropriate hard wired priority line connected to a "D" flip-flop in the M736.

A Bit Time State-3 (BTS-3) pulse from the computer is applied to the clock input of the "D" flip-flop to which the activating device flag is connected, as mentioned in section 1b above, and causes this flip-flop in the M736 to set. If more than one priority devices called to be serviced at the same time, all of the associated priority "D" flip-flops in the M736 would be set at this time. The outputs of the priority flip-flops in the M736 are connected to a priority gate structure which is arranged in such a manner that only one output line will be activated and that line will be associated with the external device with the highest priority.

This activated output of the priority gate structure is applied to one group of six two-input gates which make up the address gate. The other input of each of the six two-input gates of the address gate is hard wired to provide a discrete address which will correspond to the starting location of the particular

subroutine associated with that priority request. Each of the six output lines of the activated address gates is applied to one input of a two-input gate of the AC input strobe gate.

The computer now has had time to jump to the priority interrupt service routine and now issues a device selection code corresponding to the hard wired device selection code assigned to the M736 priority interrupt modules. This device selection code will pre-enable the IOP gates of the M736 of M736's.

The computer now issues an IOP-1 pulse to the IOP-1 gate of the M736 module. The output of the IOP-1 gate now produces an IOT-1 pulse which causes the "Clear the AC" line of the I/O bus to be pulled to ground, and thereby clears the AC.

The computer issues an IOP-2 pulse to the IOP-2 gate of the M736 module. The output of the IOP-2 gate produces an IOT-2 pulse which is applied to the strobe inputs of the AC input bus gate. As the other inputs of the AC input bus gate are connected to the outputs of the address gate, appropriate lines of the AC input bus (AC 6 thru AC 11) will be pulled to ground thereby loading into the AC the starting address of the subroutine associated with the particular priority I/O device to be serviced.

The computer now refuses to accept any further interrupt requests and jumps to the subroutine with the particular starting address which was loaded into the AC. The service routine of the particular priority device contains an instruction to clear the interrupt flag flip-flop of the particular I/O device and at the end of the subroutine issues the M736 device selector code with an IOP-4 which clears the priority flag flip-flops of the M736. The computer now turns on the priority interrupt system capability which allows the computer to service any future interrupt requests.

USING THE M736 PRIORITY INTERRUPT MODULES

1. Assign a device selection code to the M736 priority system and connect the device selection inputs of the M736 to the proper device selection lines to assure decoding for that code. If more than one M736 is used connect the device selection lines for each M736 in exactly the same manner. Each M736 will use the same device selection code.
These inputs are: BT2, BS1, BR1, BP1, BN1 and BS2.
2. Connect the enable input, BN2, of each M736 to GRD.
3. Connect the IOP-1 input, BM2, to the IOP-1 bus line.
4. Connect the IOP-2 input, BJ1, to the IOP-2 bus line.
5. Connect the IOP-4 input, BL2, to the IOP-4 bus line.
6. Connect the BTS-3 input, BL1, to the BTS-3 bus line.
7. Connect the outputs of the external I/O device flag flip-flops to the priority

NOTE: In normal operation, IOP-4, is not required as the flag flip-flop in the external priority I/O device is cleared by the subroutine servicing that device. When the flag in the I/O device is cleared, the next BTS03 pulse will load the disabled flag output into its respective priority flag flip-flop in the M736 effectively clearing the priority flag flip-flop.

inputs in such a manner as to pull the corresponding priority input line of the M736 to GRD when the device flag is activated. These inputs are as follows:

1st priority	BH1	"	"	"
2nd priority	BF2	"	"	"
3rd priority	BK1	2nd	"	"
4th priority	BJ2	"	"	"
5th priority	BH1	"	"	"
6th priority	BJ2	1st	M736 module	
etc. carry on for additional priority interrupt devices.				

8. Assign starting address to the subroutines which will service each priority interrupt device attached to the priority interrupt system. Also assign a starting address for the subroutine to service non-priority devices. Hard-wire the various starting address of the service routines as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Priority 1	BD1	BB1	AP1	AR1	AH1	AF2
Priority 2	AU2	AS1	AN1	AK1	AF1	AA1
Priority 3	AT2	AR2	AM2	AL2	AE1	AB1
Priority 4	BA1	AS2	AL2	AM1	AD1	AC1
NON-Priority	BC1	BE1	BF1	AP2	AJ1	AH2

NOTE: If more than four external I/O devices require priority assignments, the NON-priority address inputs BC1, BE1, BF1, AP2, AJ1 and AH2 of the M736 module used for the first four highest priorities, must be connected to GRD. If more than two M736 modules are required all of the NON-priority address lines of each module except the last M736 containing the lowest priorities, must be connected to GRD. The NON-Priority address is hardwired to the NON-Priority address inputs of only the lowest priority M736 module. All un-used priority address inputs must be grounded. Logic 1 level for address may be obtained from module pin BV2 of each M736 module. Lower priority addresses would be hardwired on succeeding M736 modules in the same order hard wired to the second M736 module as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Priority 5	BD1	BB1	AP1	AR1	AH1	AF2
Priority 6	AU2	AH2	AK2	AD2	AJ2	AE2

9. Connect the AC input bus gate outputs to the AC bus as follows:

Module Pins	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
	AV2	AH2	AK2	AD2	AJ2	AE2

10. Connect the Priority Enable input line BE2, of the M736 with the highest priorities, or the only priorities, to ground.
11. If lower priorities of 5 or more are assigned, connect the Priority output of the module with the higher priorities, Pin BD2, to the next M736 module (with the next following four lesser priorities) Priority enable input pin BE2.
12. Last, but not least, connect the INITIALIZE input, BL2 to the Initialize line of the computer I/O bus.

M736 — \$130

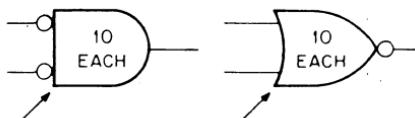
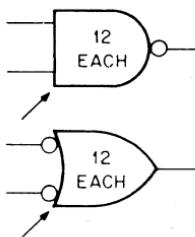
LOGIC APPLIQUES

M
SERIES

For convenient drawing of neat block diagrams, to supplement the DEC drawing template, self sticking matte-surface appliques lift from backing with a sharp knife.

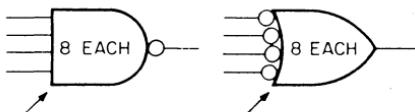
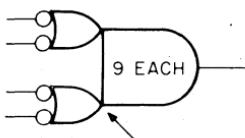
DIAGRAMS	MODULES	APPLIQUE TYPE
12 2-input NOR, 12 2-input NAND	M101, M113 K113, M141	DRT-1-47
10 2-input NAND, 10 2-input NOR	M112	DRT-1-03
8 4-input NOR, 8 4-input NAND	M117, M617, M627	DRT-1-35
10 8-input NOR, 10 8-input NAND	M119	DRT-1-51
9 4-input AND/NOR 9 4-input NOR/AND	M121, M160	DRT-1-25
3 Binary to Octal/Decimal Decoder	M161	DRT-1-20
24 JK Flip-flops	M203, M206, M207	DRT-1-23
16 JK Flip-flops with gates	M204	DRT-1-22
3 8-bit Buffer/Shift Register	M208	DRT-1-41
18 Level Converters	M502, M652	DRT-1-39
10 NOR Level Converters 10 NAND Level Converters	M506	DRT-1-52
7 NOR Pulse Amplifiers 7 AND Pulse Amplifiers	M602, M650	DRT-1-34
2 12-input AND/NOR 2 12-input NOR/AND 2 Timers, 2 clocks	M160, M302 M401	DRT-1-21

PRICE: \$1.50/sheet

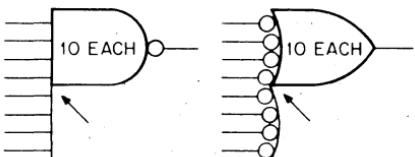
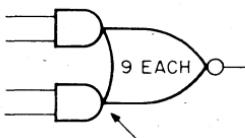


M117, M617, M627

M121, M160

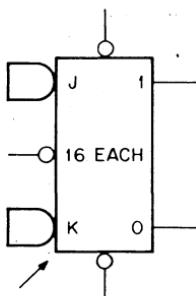
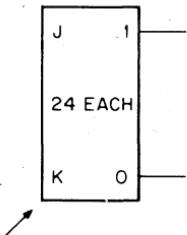


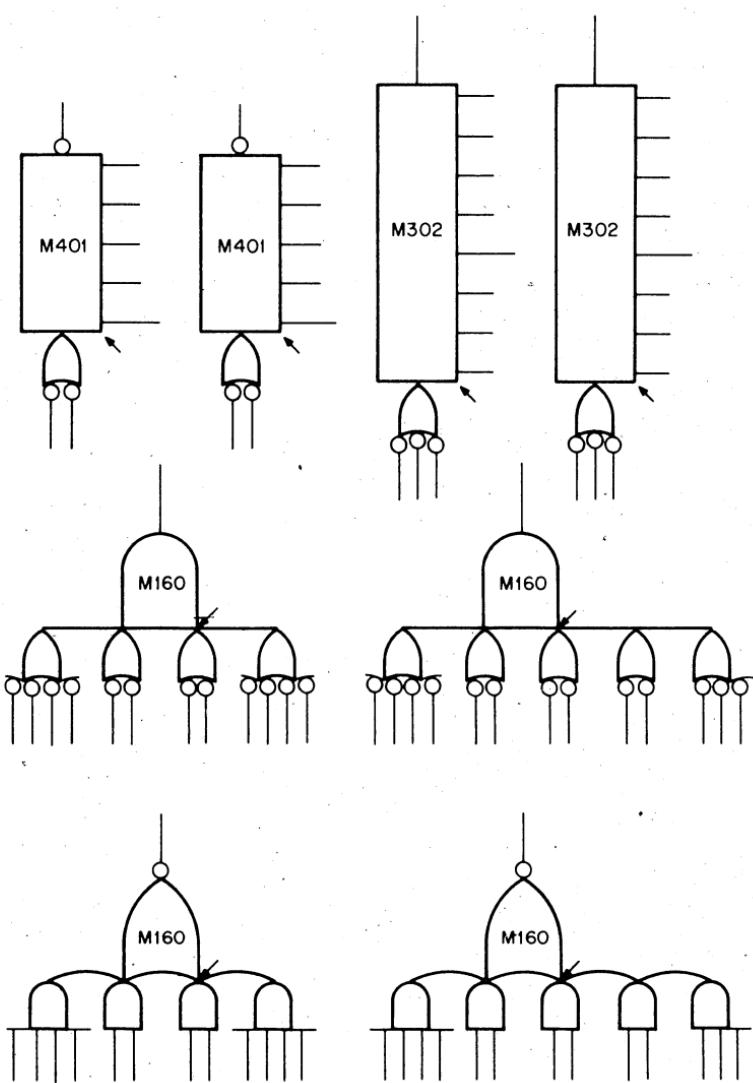
M119



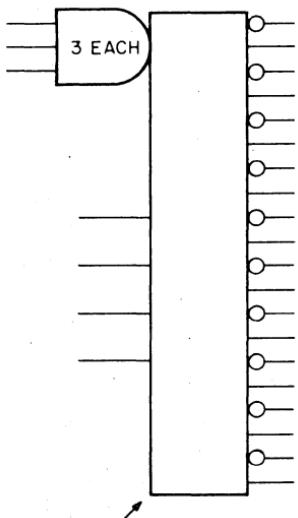
M203, M206, M207

M204

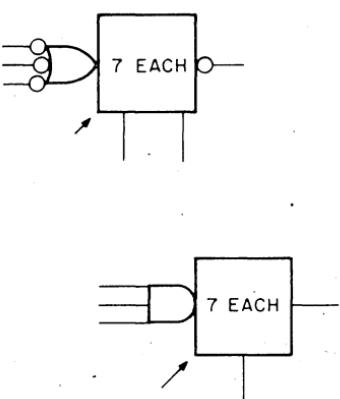




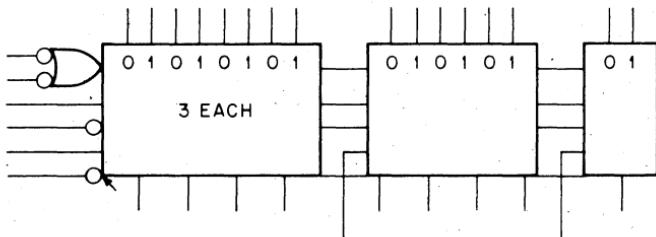
M161



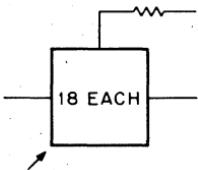
M602, M650



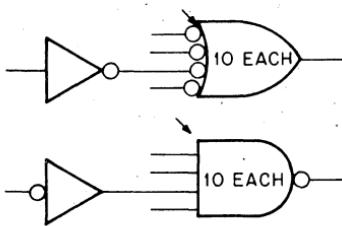
M208



M502, M652

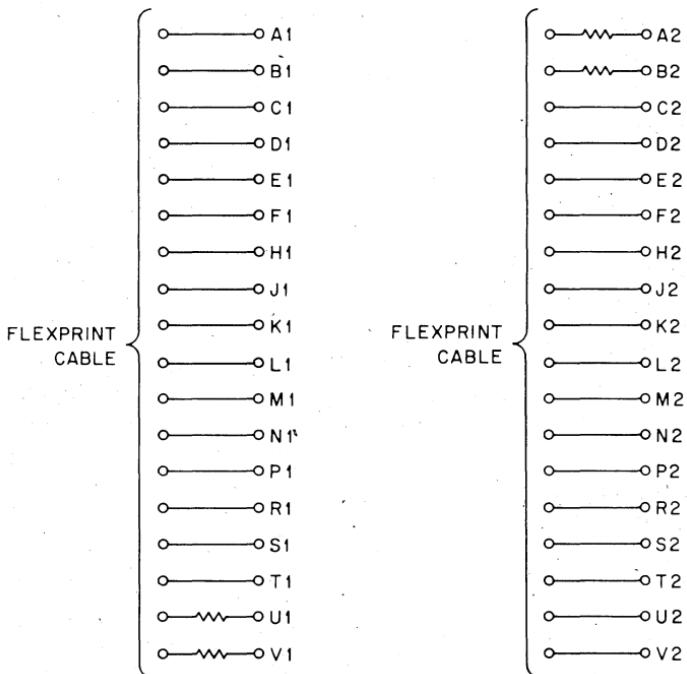


M506



FLEXPRINT CABLE CONNECTOR M901

M
SERIES



PL - 0272

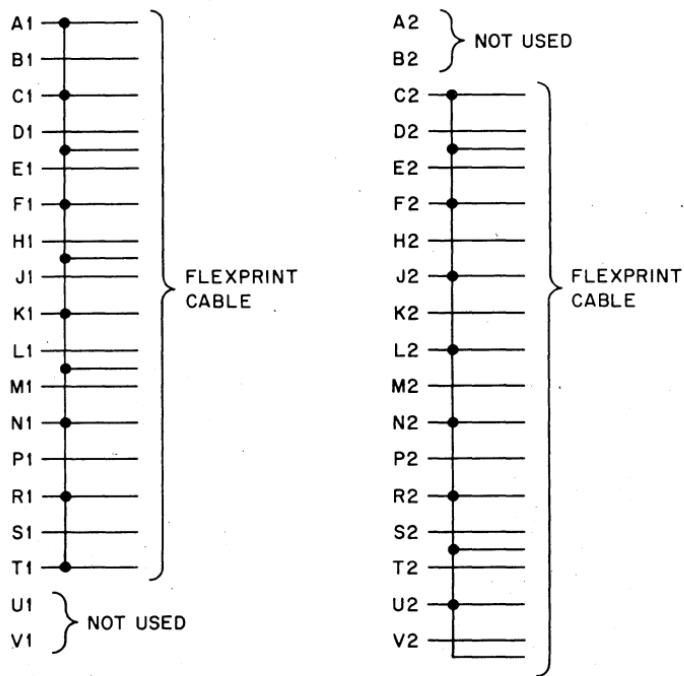
This module allows 36 lines to be used as signals and/or grounds. The 100 ohm resistors connected in series with the modules pins A2, B2, U1 and V1 are provided to afford some measure of protection in the event that these pins are inadvertently connected to a source of supply voltage.

Input: Recommended current per line is 100 ma. maximum.

M901 — \$16

FLEXPRINT CONNECTOR M903

**M
SERIES**



The M903 connector is a single sized, double sided board.

This connector provides high density cable connections using two single flex-print cables. Eighteen signal leads and grounds are used as listed below.

Signal: B1, D1, E1, H1, J1, L1, M1, P1, S1
D2, E2, H2, K2, M2, P2, S2, T2, V2

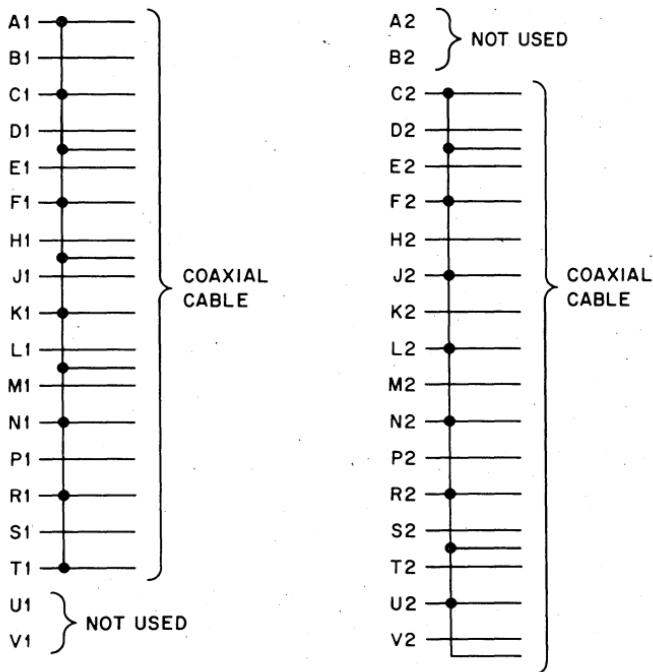
Common Ground: A1, C1, F1, K1, N1, R1, T1
C2, F2, J2, L2, N2, R2, U2

M903 — \$12.50

COAXIAL CABLE CONNECTOR

M904

M
SERIES



The M904 connector is a single sized, double sided board.

This connector provides high density cable connections using coaxial cable. Provisions are made for connection of two nine-conductor coaxial cables to this connector. Eighteen signal leads and grounds are used.

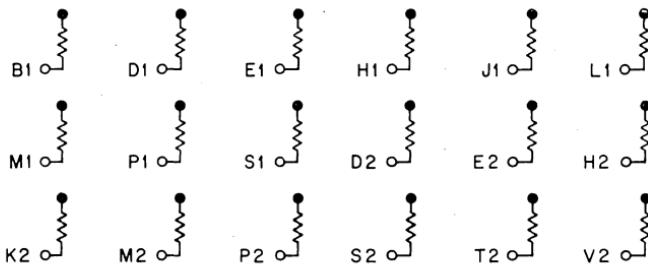
Signal: B1, D1, E1, H1, J1, L1, M1, P1, S1
D2, E2, H2, K2, M2, P2, S2, T2, V2

Common (ground): A1, C1, F1, K1, N1, R1, T1
C2, F2, J2, L2, N2, R2, U2

M904 — \$14

CABLE TERMINATOR M906

M
SERIES



The M906 cable terminator module contains 18 load resistors which are clamped to prevent excursions beyond +3V and ground. It may be used in conjunction with M623 to provide cable driving ability similar to M661 using fewer module slots.

The M906 may be used to terminate inputs. In this configuration, M906 and M111 are a good combination.

Inputs:

This module is normally used standard M-Series levels of 0 and +3V to partially terminate 100 ohm cable. It presents a load of 22.5 ma or 14 TTL unit loads at ground, and therefore, must be driven from at least an M617 type circuit, or preferably a cable driver.

The following pins MUST be grounded: A1, C1, F1, K1, N1, R1, T1
C2, F2, J2, L2, N2, R2, U2-

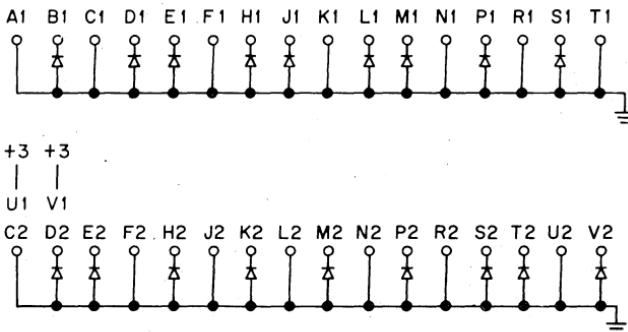
Power: +5V @ 440 ma. (max.) (all lines grounded).

M906 — \$20

DIODE CLAMP CONNECTOR

M907

**M
SERIES**



The M907 is used to provide proper undershoot ground clamps for PDP8/I positive bus signals not using M103 or M101 inputs.

The M907 also provides +3V for clamping 25 unused inputs. Diode clamps appear on signal leads used in double-sided alternate ground I/O cables.

Diode clamp: B1, D1, E1, H1, J1, L1, M1, P1, S1,
D2, E2, H2, K2, M2, P2, S2, T2, V2

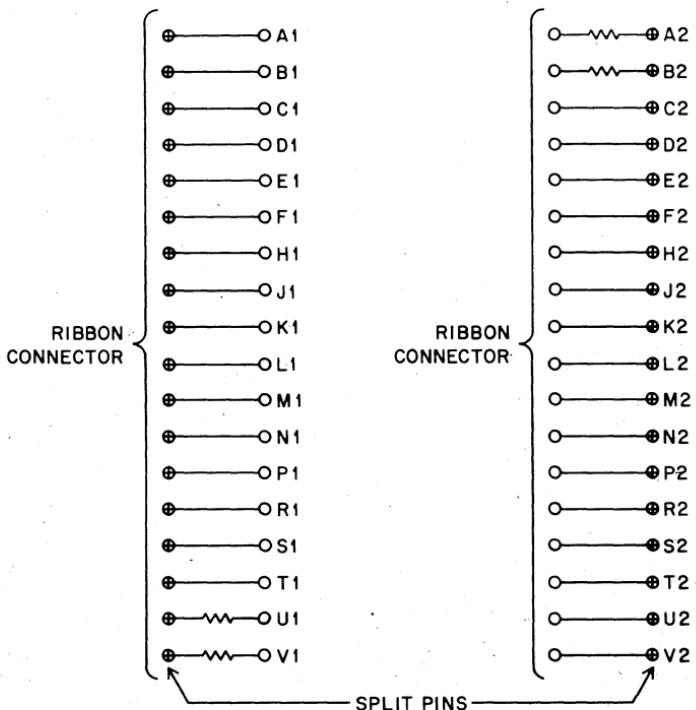
Ground: A1, C1, F1, K1, N1, R1, T1,
C2, F2, J2, L2, N2, R2, U2

Power: +5v at 10.2 ma. (max.)

M907 — \$16

RIBBON CONNECTOR M908

M
SERIES



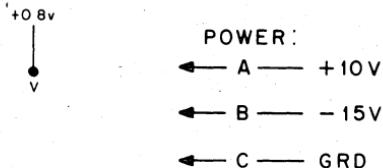
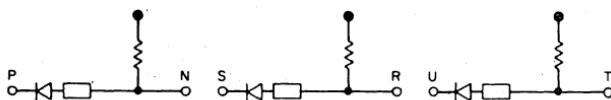
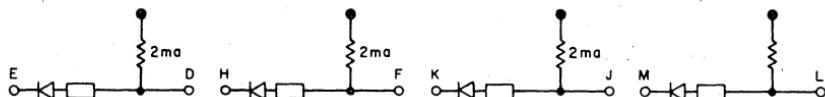
The M908 cable connector consists of a single sized, double sided board which contains thirty-six split pins which allows the connection of thirty-six separate wires. All connections are made on the component side of the module. The 10 ohm, $\frac{1}{4}$ watt resistors connected in series with module pins A2, B2, U1 and V1 are provided to afford some measure of protection in the event that these pins are inadvertently connected to a source of supply voltage.

The M908 is primarily intended for use with ribbon cable and is normally supplied with a ribbon cable clamp unless otherwise specified.

M908 — \$18

POSITIVE LEVEL CONVERTER W512

**W
SERIES**



INPUT	OUTPUT
+ GRD	-3V GRD

W512 POSITIVE LEVEL CONVERTER

Positive logic systems, such as those using monolithic integrated circuits, can use the W512 to make available standard DEC levels of -3V and ground to accessory modules in the W and A series.

Input threshold voltage to each converter is normally 1.6 volts for compatibility with DTL and TTL levels. This threshold can be set at 0.8 volts by grounding pin V for RTL level conversion.

Inputs: Input current 1 ma or less for input voltages between 0.3 volts and the threshold. 100 μ A for inputs above the threshold. Input voltages must not exceed 6.0 volts with pin V open, or 5.3 volts with pin V grounded. Inputs must exceed nominal thresholds by at least 0.4 volts for full switching with minimum noise rejection.

Outputs: Each output can supply up to 8 ma at ground. Grounded inputs provide grounded outputs and positive inputs provide negative outputs. Output rise and fall times are less than respectively 70 and 200 nsec.

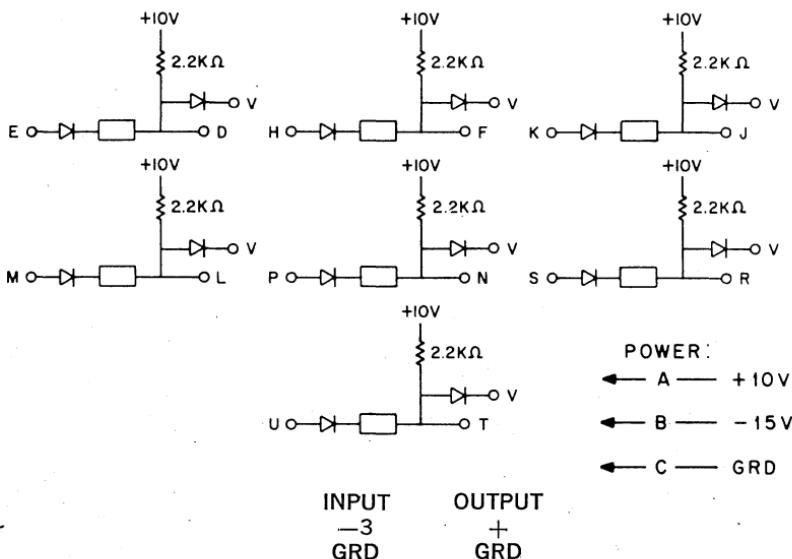
Power: 10v (A)/104 ma: 15 v (B)/30 ma.

W512 — \$25

POSITIVE LEVEL AMPLIFIER

W603

**W
SERIES**



W603 POSITIVE LEVEL AMPLIFIER

Positive logic systems such as those using RTL, DTL, or TTL monolithic integrated circuits can be driven from FLIP CHIP systems through the W603. Clamped load resistors at the output of each circuit permit output levels to be adjusted to the type of circuit being driven. This clamp voltage is common to all seven converters on the module.

Inputs: 1 ma at ground.

Outputs: Each output can supply up to 5 ma at ground. Drive capability at the positive output voltage is provided by internal 2200-ohm resistors returned to +10 volts. The upper positive level will be no more than 0.8 volts above the clamp voltage.

Grounded inputs provide grounded outputs; negative inputs produce positive outputs. Output rise and fall TTT are less than respectively 100 and 150 nsec.

Power: +10(A)/35 ma. — 15(B)/7 ma.

When the W603 is used to drive M or K series modules, the module pins V and A may be tied to the +5 volt logic power supply. The following drive capability will result:

Each output will supply one M series unit load, or two K series unit loads.

W603 — \$23



K SERIES

INTRODUCTION

Control system complexity and demands on reliability are rising with ever-increasing automation. More and more, control system designers are looking to solid state electronics for new answers to the old problems of reliability, complexity, and economy. Some of the answers are provided by solid-state digital logic designed for the industrial environment, and solid state analog-digital conversion to link analog sensors and actuators to digital control.

Why Solid State?

The time-honored way to do control logic is with the deceptively simple-looking relay. The metal-to-metal contact area sees physical and chemical actions of remarkable complexity. Even the mechanical-magnetic interactions are involved enough to cause problems now and then. Still, relays sometimes respond beautifully to simple maintenance. If the contacts stick, force them apart; if they are dirty, clean them.

Railway signaling relays, operating perhaps a hundred times a day, accumulate 25 years and a million operations without failure. And modern sealed-contact relays can do 10 billion operations under the right conditions without wearing out. So why abandon well-proven, reliable components? Only because it is necessary. And it is necessary in a growing number of applications.

Reliability

As profit margins grow tighter, and maximum process efficiency becomes a necessity rather than an ideal, control system reliability assumes greater importance. Faulty operation and machine downtime can swiftly and disastrously cut into the profit picture. With a highly complex control system, check-out can easily become a very costly and time consuming operation. Many factors affect the reliability of a control system. A major consideration is the speed at which the logic control elements must operate. At 1KHz, near the maximum rate for dry reed relays, 100 million operations accumulate in about 30 hours. Longer-lived mercury-wetted contacts operating 100 times per second, accumulate 10 billion operations in about four years. Even if a four year component life is enough, there are applications where 100 operations per second are not. Solid state logic, with nothing to wear out, stick, or corrode, can operate almost indefinitely at 100,000 operations per second.

Complexity is another factor. Demands for more automation, more efficiency, more safety, more accuracy all result in increased control system complexity. As a result, the sheer numbers of logical decisions demand component reliability far greater than that acceptable in a small system. Solid state logic provides the degree of reliability needed in a large system, at reasonable cost.

Size

Even the tiniest-contact reed relay coil is enormous alongside a transistor, or a complete integrated circuit. And most small control systems are not built with reed relays: to get the advantage of ruggedness or standardization, usually all the relays used are built to 300 volt or even 600 volt specifications whether they drive external loads or just relay coils. But a single small printed circuit board can easily accommodate a half dozen or more relay equivalents in logic capability, in a small fraction of the space of one 300 volt relay.

Computer Tie-In

There are several levels of computer involvement possible, extending from incorporation of a computer as a part of an individual control system to the use of a central computer to monitor the performance of many independent control systems. Regardless of the level at which the computer interacts, its presence demands an interface between solid-state circuitry and the controlled machine or process. If such an interface is forced into existence by the present or projected future use of a computer, why not put solid state control logic behind it and gain the benefits of solid state speed, compactness, and reliability through the entire system?

Also solid-state logic can communicate with existing analog sensors and actuators through solid-state analog-to-digital (A/D) and digital-to-analog (D/A) converters.

All of these factors tend to make solid state control systems increasingly attractive, particularly as their costs come down.

Who Should Be Designing For Solid State Controls?

Broadly speaking, the decision between conventional relay controls and the new solid state controls, like most engineering decisions, hinges on comparative overall costs. Where three or four or a half dozen relays can do the whole job, the cost of a solid-state interface will seldom be justified unless high speeds are required. Very large or computer-oriented systems leave little justification for the use of relays.

For intermediate systems, the comparison is more complicated. The tabulation below can serve as a framework for a systematic review of factors you should consider before you specify your next control system.

Considerations	Factors Suggesting Relays	Factors Suggesting Solid State
Reliability	Control system failure causes no panic. Temporary manual control acceptable. Simple system, easy to trouble shoot.	Downtime cuts quickly into process profitability. Quick check-out of entire system in case of trouble desirable, instead of on-the-spot checking. Lives and property might be endangered by failure.
Cost	Low cost relays acceptable. Maintenance costs need not be considered. Personnel training costs important. System failures will not cause significant secondary costs.	High quality relays used for comparison. Costs of failure high. Installation space costly. Cost of future modifications must be considered. Maintenance costs over life could be important.
Complexity	Small systems, perhaps a half dozen relays or fewer.	Complicated systems, which would require fifteen or more relays to implement.
Sophistication	Traditional performance still acceptable.	New levels of performance are needed, calling for increased control system complexity to remain competitive.

Considerations	Factors Suggesting Relays	Factors Suggesting Solid State
Familiarity	Controls that must be serviced by electricians who can not be retrained.	Environments already include other solid-state components or they will soon be added. Also, multi-system installations where a few controls technicians will cover a lot of equipment.
Growth	No foreseeable use of computers. Little likelihood of important modifications.	Added performance or safety features may be wanted later without tearing the system down. Computer tie-in might become desirable or is planned already.
Size	Plenty of space available.	Relay equipment might require separate balconies, restrict maintenance of machinery, or block aisles. Features added later must fit original enclosure.
Speed	Control system delays of tens of milliseconds acceptable. Operating rate is low, relay wearout no problem.	Compatibility with pulse tachometers, photoelectric pickups, electronic instruments required. Closed-loop stability demands quick response. High repetition rate that would cause wearout of moving parts.

Why Digital?

Relays, solenoids, switches, fuses, locks, counters, annunciators, panel lights and panic buttons all have one thing in common: they are digital. All these devices (when working properly) are up, down, on, off, in, out; but never in-between. Strictly speaking, of course, you cannot get from on to off without passing through in-between. But digital devices pass through in-between at maximum speed, and without waiting around for doubt to creep in.

Non-digital devices like panel meters, potentiometers, and slide rules work in the "in-between" area, producing outputs that are proportional to the input. The angular position of a panel meter pointer is the analog of the magnitude of the electrical input. A potentiometer's voltage output is the analog of mechanical shaft position. In a slide rule, position is the analog of magnitude.

In a slide rule, accuracy is limited by the thickness of the calibrating marks and the difficulty of estimating values between them. Each space is an area of uncertainty. The same kind of uncertainty exists in every proportional electrical system, in the form of noise. In all but the most expensive analog equipment, the amount of noise, like slide rule error, limits accuracy to two or three significant figures.

Noise taken in this broad sense affects every proportional device. Noise is a major reason for the dominance of digital computers over analog computers where complex calculations are required. Small amounts of noise contributed by each analog input or computing element add up to degrade the accuracy of the answer. In digital circuits, the noise can be disregarded as long as it is below an "off" or "on" threshold level.

Analog controllers and servo systems, chart recorders, panel meters, and small analog computers are often simpler and cheaper than their digital equivalents, and should be used wherever they can do the job. But since so many commonly used control devices (from relays to panic buttons) are digital anyway, all-digital control is convenient. For complex control situations, digital methods can deliver accuracy and perform types of control beyond the ability of an analog system at any cost. And using solid state digital control, analog and digital devices can work together through A/D and D/A conversion. Better still, noise-free direct digital sensors and actuators can be used in the design of new process equipment.

Noise Immune Control Modules

Because of their high sensitivity and speed, solid state components can respond to noise that relays would safely ignore. To use solid state logic with freedom from noise problems in the neighborhood of arcing contacts, brushes, welders, etc. requires special design considerations.

Unlike analog devices, digital circuits have a noise "threshold" above which a noise or signal must rise to cause any change in the output of the circuit. It is this threshold that accounts for the superiority of digital circuits in processing information through complex manipulations without loss of accuracy. In the design of solid state logic for industrial use, this basic threshold feature of digital circuits can be exploited. By adding external capacitance, the speed, and thus the sensitivity, of the circuit can be lowered.

Noise

Suppose that on the basis of the above, you find you should be using solid-state digital logic. But will the system "drop bits," or otherwise go haywire in your environment? How well can noise trouble be anticipated, and what measures should be taken? How can you compare the noise immunity of competing manufacturers' circuits? These questions need some kind of answer before you can feel confidence in taking the step.

A logical starting point is the noise itself. What is its amplitude? Its frequency distribution? How does it vary with time? With temperature? How many picofarads of coupling capacitance between the noise sources and the logic wiring? How many nanohenries of shared inductance in the logic and noise ground return paths?

Right away you suspect these questions are going to be difficult to answer. You may be able to say that typical noise source voltages are "measured in

kilovolts" and are "strongest in the Megahertz frequencies." But going beyond such hazy estimates will require detailed knowledge of the physical conditions that interact to produce electrical noise. You'll need to know the materials used in all metal-to-metal contacts, and the condition of the contact surfaces. You'll need the inductance and capacitance of the wires connecting them. And the inductance and capacitance of the loads they drive. And the gases in the atmosphere surrounding the contacts. Even the exact routing of the wires will have to be examined.

Is solid-state out of the question after all, because analysing the noise environment is impractical? No, solid-state is not impractical: provided you use circuits designed specifically for noisy environments, where the focus is on qualitative rather than quantitative factors.

Engineering For the Unknown

Engineers prefer to deal in quantities: "how big," "how many," and "how much." Success in dealing with noise requires a different approach because very few if any accurate numbers about noise will be forthcoming. Qualitative considerations, those that affect the overall character of circuit behavior rather than specific numerical details, are central to this approach.

We can group the qualitative tools available for dealing with electrical noise into two groups: those that keep noise out of the solid-state logic, and those that minimize the influence of noise that gets in. Keeping noise out is cheaper than electrically rejecting it, since primarily mechanical and packaging considerations rather than electronic aspects are involved. Here are some of the ways you can keep noise out:

1. Segregate logic wiring from field wiring. Don't design input converters and output drivers so field wiring goes through the same connectors used to carry logic signals. Arrange to use opposite ends of printed boards for logic and field wiring connections, and never allow the two kinds of wiring to lie side-by-side or be bundled together.
2. Don't mix logic ground with field ground. This doesn't mean logic ground should float; on the contrary. But heavy currents should not pass through the logic ground system on their way back to a power supply. An excellent scheme is to switch the AC line with isolated triacs. DC solenoid drivers might seem difficult to isolate, but judicious use of ground isolating resistors and auxiliary chassis tiepoints can force most of the load current outside of the logic ground system.
3. Use high-density packaging. Computer type modular construction minimizes lead lengths in the logic, minimizing the capacitive coupling between logic wiring and nearby field wiring. Dense packing also cuts resistance and inductance in the logic grounding system, minimizing interference from any residual noise currents that may flow there.
4. Where logic and power circuits must be adjacent, use shielding. For example, a group of printed boards carrying field circuits can be shielded from general purpose logic modules simply by inserting un-etched copper clad boards in the sockets that separate the two groups. (Logic power must skip these sockets to avoid shorting the supply.) A single ground connection to the shield board is perfectly adequate, since the noise currents it carries will be limited by the small capacitance involved.

5. Filter the line voltage where it enters the logic power supply, or at supply output terminals. Supplies for panel lamps should also be filtered, if their wiring approaches logic wiring. Do not use logic power for any other function or carry supply output wires into the field for any reason.

The above five measures may suffice to allow even fast, computer-speed logic to be used in the vicinity of severe noise. Often, however, some forgotten loophole in the noise exclusion plan will spoil the dependability of an otherwise noise-tight system. All it takes is one such leak to cause real headaches if the logic itself is sensitive to noise. A good belt-and-braces approach will include not only these noise isolation qualities, but several noise desensitizing qualities as well:

1. Slow speed of response. Noise is usually most intense at high frequencies (in the Megahertz). Metal-to-metal contacts are nearly ideal step generators, and wiring resonances often dictate high-frequency noise peaks. A circuit that can't be switched for five microseconds is deaf to all but the biggest and slowest of noises, and usually will be entirely undisturbed. But be careful to use discrete capacitors, not sluggish semiconductors to obtain circuit slowdown. Semiconductor manufacturers "improve" their products regularly, often by increasing their speed.
2. Good current threshold and voltage thresholds. By "good" is meant "measured in milliamperes and volts." The bigger the better, but guard against falling in love with numbers. A factor of two in voltage threshold means little if you can't predict noise amplitudes to the nearest order of magnitude.
3. Risetime independence. Circuits that don't care what risetime you feed them give you an important insurance policy. If all else fails, you can hang a capacitor to ground at any troublesome point, without worrying about the effect this has on risetime. Even more than the other qualities, risetime independence is a prime example of engineering for the unknown.
4. Special care in timer and flip-flop design. These are the circuits that stretch a noise spike to damaging length. A system that has noise-immune, risetime-independent flip-flops and timers will for most purposes be as noise immune with ultra-fast gates as with slow gates.

Looking Ahead

Many of the factors listed above cost nothing more than forethought. All are applicable regardless of choices between discrete components, integrated circuits, or a combination. As the qualitative approach to noise avoidance is more widely understood and applied, solid-state logic will become more accepted, more universal. Fears will disappear. Should your next control system be solid-state?

K SERIES CONTROL MODULES

Computer-oriented logic, by its very nature, is high speed (1 MHz and above), and provides noise immunity far below that required in a process control environment. The upper frequency range of the K-Series modules is 100 KHz, with provision for reduction to 5 KHz for maximum noise immunity. These modules incorporate all silicon diodes, transistors, and integrated circuits, deliberately slowed.

Either English (non-inverting) logic or NAND/NOR logic is compatible with K Series. The hardware for this series is specifically designed for standard NEMA enclosures. FLIP CHIPTM mounting hardware can likewise be used for rack-mounting, inasmuch as K-Series modules fit standard DEC sockets.

Proven FLIP CHIPTM connectors, used for years in applications from steel mills to lathe controls, provide modularity. Even the connection between terminal strips and electronics can be plugged for installing the logic after field wiring is complete, and removing it quickly for modifications or additions.

Checkout and trouble shooting is easy with K-Series logic. Every system input and output has an indicator light at its screw terminal. A special test probe provides its own local illumination and built-in indication of transients, as well as steady states. Every point in the system is a test point, and consistent pin assignments reduce the need to consult prints.

Construction materials and methods are the same as for other high-production FLIP CHIPTM modules, including a computer-controlled operating test of each complete module. K-Series modules further offer the size reduction, reliability, flexibility, and low cost of solid state logic, with an added bonus of easy interconnection. FLIP CHIPTM industrial modules are ideal for interfacing high speed M-series or computer-systems to machinery and processes. Sensing and output circuits operate at 120 vac for full electromechanical capability. Inputs from contact devices see a moderate reactive load to assure normal contact life. Solid state ac switches are fully protected against false triggering. Voltages from the external environment are excluded from the wire-wrap connections within the logic.

K SERIES SPECIFICATIONS

SUMMARY

Frequency range: DC to 100 KHz. Control points on each module allow reduction to 5 KHz for maximum noise immunity for critical functions.

Signal levels: Ov and +5v, regardless of fanout used.

Fan-out: 15 ma available from all outputs; typical inputs 1-3 ma.

Waveforms: Trapezoidal. No fast transients to cause cross talk. External capacitive loading affects speed only; no risetime dependence.

Temperature range: -20°C to $+65^{\circ}\text{C}$, using all-silicon diodes, transistors, and monolithic integrated circuits (0° to 150°F). Limited to 0°C on four module types.

Noise immunity: False "1":20 ma at 1.6v for 1.5 μsec typical. False "0":3 ma at 3v for 1.5 μsec typical. Time thresholds can be increased by a factor of 20 for critical points by wiring the slowdown control pins.

Simple power requirements: Single voltage supply, $+5\text{v} \pm 10\%$. Dissipation typically 120 mw per counting or shifting flip-flop, 30 mw per control flip-flop, 25 mw per two-stage diode gate.

Control system voltage: 120 VAC, 50 or 60 hertz.

Mounting provisions: Standard NEMA industrial enclosures. May also be used in 19" electronics cabinets.

GENERAL SPECIFICATIONS

Construction Features

K-Series modules include the quality features of older lines of FLIP CHIP modules: flame-resistant epoxy-glass laminates, all-silicon semiconductors, gold plated fingers and solid gold connector contacts. Thorough testing of each module is by computer operated automatic tester for most modules, or by specialized equipment for those which are not amenable to automatic test. A test specification sheet or data sheet is packaged with each module, including a circuit schematic for that type. Monolithic or hybrid integrated circuits are included wherever they can improve the performance-cost ratio. Versatile mounting hardware imposes as few physical constraints as practicable.

Logic Signals

There are no ultra-fast transients at any K Series output. Logic signal "1" and "0" levels are essentially independent of fanout. Rise and fall transitions have controlled slopes which are not strongly influenced by normal changes in fanout, lead length, temperature, or repetition rate. The fastest K Series trapezoidal logic signal can be fully analyzed with a 500KC oscilloscope. Logic "1" or "true" is +5 volts and logic "0" or "false" is zero volts except where redefined by logic designs. Counters and shift registers advance on the "1" to "0" transition and are cleared by a "0" level. Any unused input may be left open relative to noise considerations.

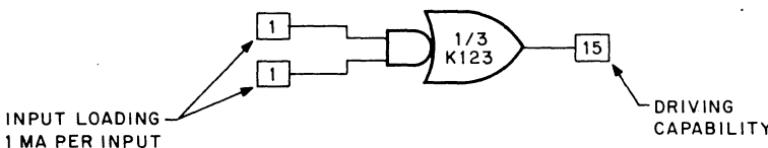
M Series Compatibility

M Series outputs can drive K Series logic gates and output converters K604 and K644 directly, and any K Series input after passing through a K Series gate, provided they meet timing requirements. See Applications Notes.

Fanout and Fanin

K Series fanout capabilities are sufficient to relegate fanout calculations to the final checking phases of logic design. Logic outputs from any module type can drive up to 15 milliamperes. Logic gate inputs consume 1 millampere

per input. Other loadings range from 1 to 4 milliamperes as indicated by the loading numbers enclosed in squares on each specification diagram.



FANIN AND FANOUT

Expandable gates give K Series a fanin capability well beyond typical logic requirements. The most restrictive fanin limitation in K Series logic concerns the wired AND configuration, for which several logic outputs are simply wired in common: the wired AND fanout capability is reduced to three milliamperes when the maximum of 5 outputs are tied together. The second level of logic (the OR node) within K113 and K123 gates is limited to less than 10 OR inputs to preserve output falltime control. The input AND gates of K113 or K123 modules may be extended with K003 expanders up to a maximum of 100 inputs, well beyond any practical requirement.

Operating Temperature

K-Series modules are designed for operation in free-air ambient temperatures between -20°C and $+65^{\circ}\text{C}$ (0°F to 150°F) except the following types which are restricted to 0°C (32°F) minimum: K202, K220, K230.

Speed

Many applications for K Series modules involve operation at rates lower than relay speeds. Even at speeds many times faster than relay capabilities, timing need not be considered unless the logic includes a "loop". A flip-flop constructed of logic gates is such a loop, in which the output at a given point feeds back to influence itself, thus demanding input durations longer than total loop delay. Proper operation of such loops should be verified by calculation using the specifications below. For a complex loop an experiment should be made if possible to look for flaws in the calculations.

When anticipated repetition rates will be of the same order of magnitude as rated logic frequency, more care is required in timing design. K Series circuits are intentionally slowed to the maximum extent practicable for 100 KHz operation, and the resulting propagation delays can limit complex logic systems to 50 KHz or even 30 KHz repetition rates. In addition, timing loops must be examined just as carefully in fast logic as in slow. If K Series speed appears marginal or insufficient for the job at hand, use M Series high speed logic modules.

K-SERIES TIMING

Timing Characteristics for K113, K123, K202, K210, K220, K230	Time (μ sec)		
	Min.	Typ.	Max.
Logic Gate Propagation Delay, Output Rise (0V to +5V) Output D only, when connected to pin B	0.5 7.5	2.0 40	3.0 180
Logic Gate Propagation Delay, Output Fall (+5V to 0V) Output D only, when connected to pin B	0.3 4.5	1.0 20	6.0 180
Count/Shift Input Propagation Delay, Output Rise As above, but pin B grounded to pin C	2.0 10	5.0 30	9.0 100
Count/Shift Input Propagation Delay, Output Fall As above, but pin B grounded to Pin C	1.0 10	4.0 30	9.0 100
Rise time, all unslowed outputs Pin D outputs only, when connected to pin B	2.0 30	5.0 100	9.0 240
Fall time, all unslowed outputs Pin D outputs only, when connected to pin B	0.5 7.5	1.0 20	4.0 120
Minimum time between successive input transi- tions on any module which has one or more Count/Shift inputs As above, put pin B grounded to pin C	4 10		

Exceptions:

Input transitions at pins J and K may follow other input transitions with delays down to zero; For characteristics not listed above, see timing information on individual data pages.

NOTE: Count Shift inputs are included in types K202, K210, K220 and K230

Noise Immunity

Two properties of electrical interference often overlooked in evaluating logic noise immunity are its source impedance and its frequency distribution. Unless the digital logic is spread over several feet or yards so that high potentials can be induced in the ground system, most noise will be injected via very small stray capacitances and hence will have a high source impedance. The voltages at the noise source itself are usually measured in thousands of volts. Consequently, voltage thresholds alone cannot provide adequate noise rejection. The noise appears to come from a current source, so that logic circuit current thresholds are also an important measure of noise immunity.

Capacitance-coupled interference is strongest at the highest frequencies. Logic circuits which respond slowly can reject high frequency interference peaks that exceed dc current and voltage thresholds. K Series modules get their outstanding noise immunity from a balanced combination of current voltage, and time thresholds.

Important as good noise thresholds are, practical noise environments are only vaguely predictable, so that the following design features are probably still more important:

1. All field wiring is isolated from K Series logic wiring pins.
2. Logic power is not transmitted outside the logic environment for contact sensing, etc.
3. W994 electrostatic shields may be plugged in to further isolate pilot circuit noise: see Construction Recommendations (Applications Note)
4. Plug-in module compactness keeps logic wiring short, to reduce noise injection capacitance, and confines the ground mesh for reduced ground noise.
5. Every third logic gate has optional slowdown control, ample for slowdown of all control flip-flops.
6. If all else fails, lack of risetime dependence permits any K Series output to be loaded with 0.01 mfd to ground to further reduce impedance and speed of response. Each K003 diode expander has such a capacitor available at pin B.

K Series Typical Noise Thresholds

To be falsely interpreted as a high level, a low (zero volts) K Series logic level would have to be raised 1.6 volts and held there for 1.5 microseconds; to do this would require 20 milliamperes to be supplied somehow from the noise source to the K Series output in question for this period of time. To be falsely interpreted as a low level, a high (+5V) K Series logic level would have to be reduced 3 volts and held there for 1.5 microseconds; to do this would require 3 milliamperes to be supplied somehow from the noise source to the K Series output in question for this period of time.

Power Requirements

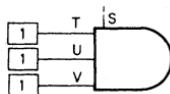
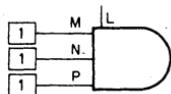
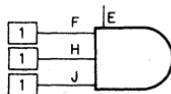
A simple 5 volt supply operates any K Series system. Tolerance at room temperature: $\pm 10\%$. K Series regulators K731 and K732 have a built-in temperature coefficient of approximately minus 1% for $3^{\circ}\text{C}(5^{\circ}\text{F})$ to obtain full logic fanout over a wide temperature range and to minimize the temperature coefficient of K303 timers. Both regulators run from a nominal 12.6 volt center-tapped transformer secondary, with hash removed. See Construction Recommendations for information about alternate sources of logic power. Logic power is not used for contact sensing; 120 VAC is specified to provide full compatibility with silver contacts and noisy environments.

GATE EXPANDERS

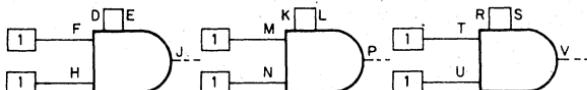
K003, K012, K026, K028

**K
SERIES**

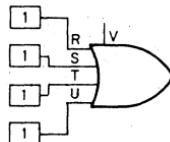
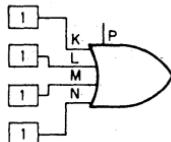
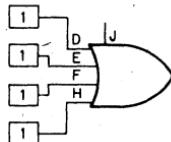
K003
AS EXPANDERS FOR
INPUT AND GATES OF
K113 OR K123 OR K134



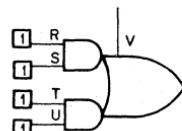
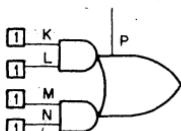
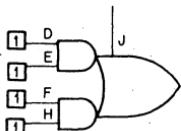
K003
AS INDEPENDENT GATES
FOR AND/OR EXPANSION
OF K113 OR K123



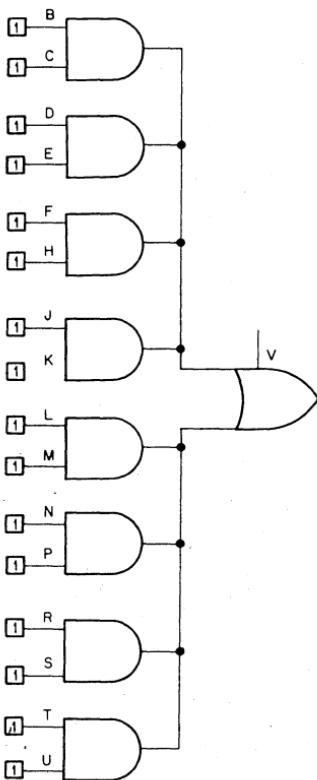
K012
AS EXPANDERS FOR
OR GATING IN K113
OR K123



K026 AS INDEPENDENT
GATES FOR AND/OR
EXPANSION OF
K113 OR K123



K028 AS EXPANDER
FOR K113 OR K123



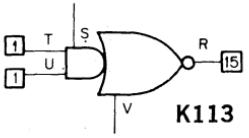
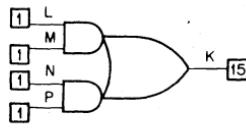
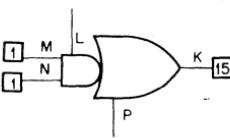
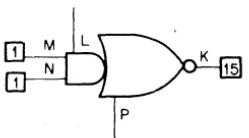
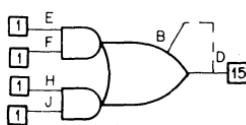
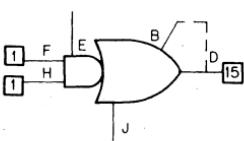
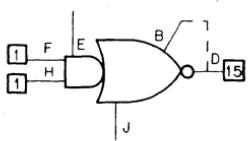
These inexpensive gate expanders offer great logic flexibility and versatility without a proliferation of module types. Logic functions performed by expanders are illustrated in combination with the K113 and K123 gates in several pages that follow the data sheet for the gates themselves.

K003 — \$4
K012 — \$7
K026 — \$6
K028 — \$7

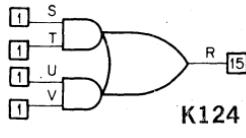
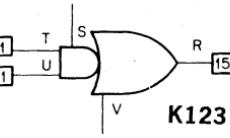
LOGIC GATES

K113, K123, K124

**K
SERIES**



K113



K123

Together with the K003, K012, K026 or K028 expanders, these gates perform any desired logic function, including AND, OR, AND/OR, NAND, NOR, exclusive OR, and wired AND.

Logic gate type K123 is an AND/OR non-inverting gate subject to expansion at either the AND or the OR node. Logic symbols and equivalent schematics are compared in the following illustrations. Typical pin connections are shown.

The AND input can be expanded up to 100 inputs total. The OR input can be expanded by any of the expanders, up to 9 inputs total. More OR inputs can be added if faster fall times are acceptable.

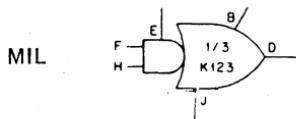
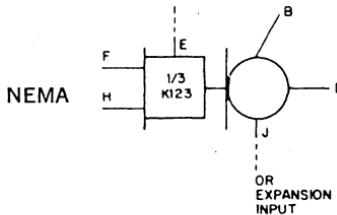
Expansion of the K113 inverting gate is identical. The equivalent circuit is the same except for inversion in the output amplifier.

The K124 provides a convenient way to implement non-inverting gate control flip-flops, exclusive ORs, and two term OR logic equations without the need for expanders. The module is electrically the same as a K123 gate with a K003 expander.

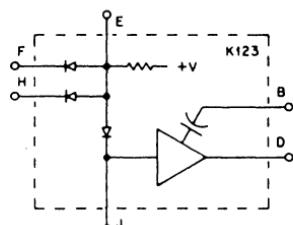
All three gate types include a slowdown capacitor that can be connected to the output of one circuit to increase its noise rejection when gates are interconnected to make control flip-flops. Use of this capacitor increases rise and fall time by approximately a factor of 20.

K113 — \$11
K123 — \$12
K124 — \$14

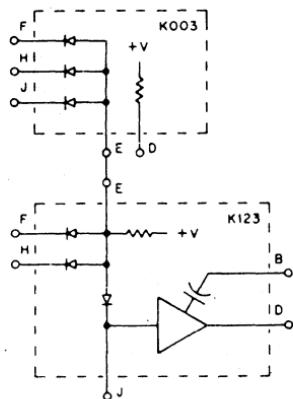
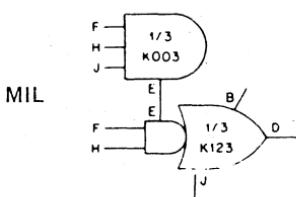
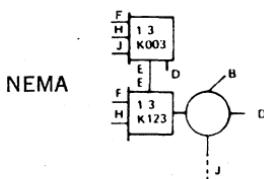
LOGIC SYMBOL



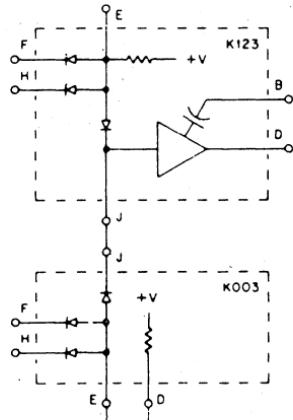
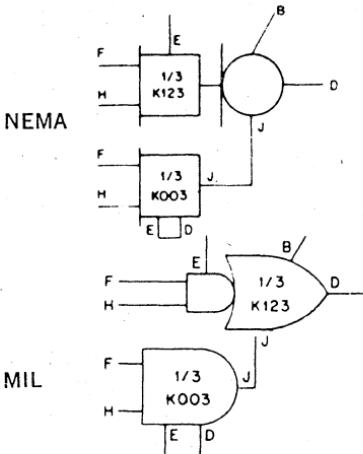
SIMPLIFIED SCHEMATIC



BASIC GATE

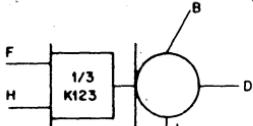


K003 AND EXPANSION

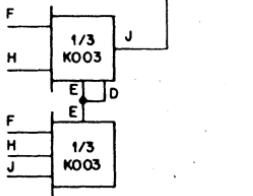


K003 OR EXPANSION

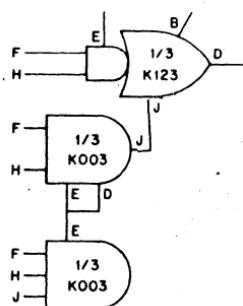
LOGIC SYMBOL



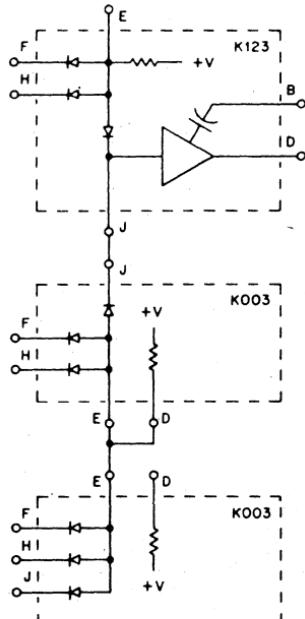
NEMA



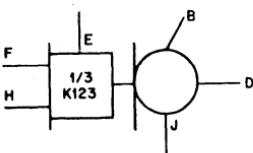
MIL



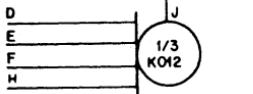
SIMPLIFIED SCHEMATIC



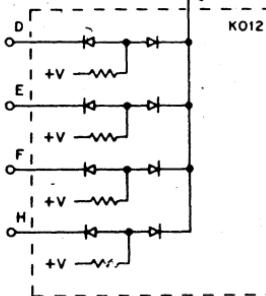
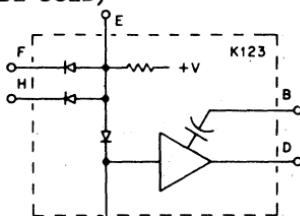
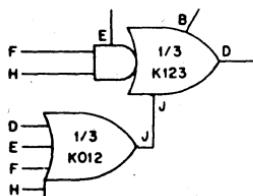
K003 AND/OR EXPANSION
(K026 MAY ALSO BE USED)



NEMA



MIL

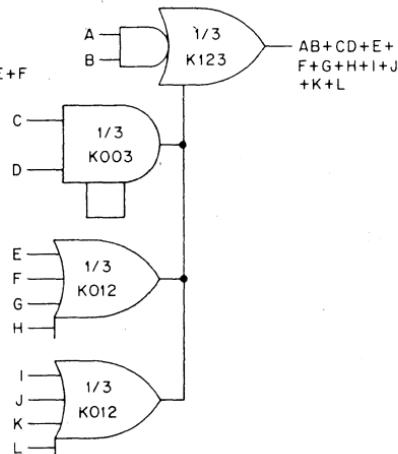
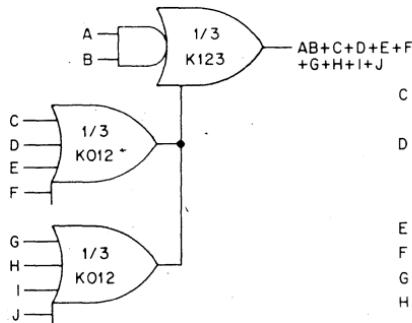
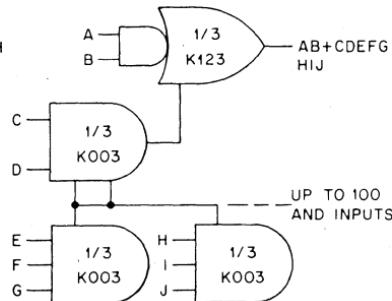
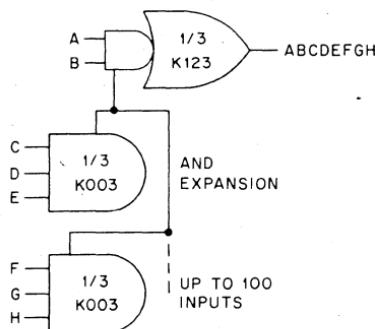
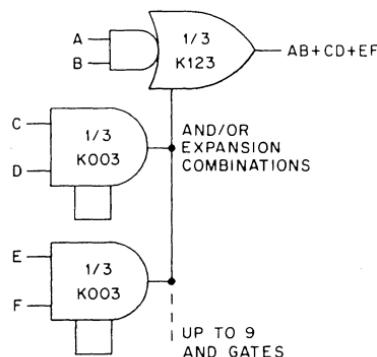


K012 OR EXPANSION

The basic types of logic function obtainable by expansion are shown below for the K123 non-inverting gate. Logic functions for the expanded K113 inverting gate are identical except for inversion of the output. Letters refer to logic signal names rather than module pin numbers.



BASIC NON INVERTING GATE



LOGIC FUNCTIONS WITH GATE EXPANSION

NAND, NOR, EXCLUSIVE OR

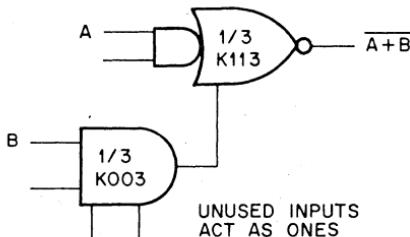
The K113 inverting gate performs the NAND function directly, and performs the NOR function when combined with a K003 expander.

With proper input connections, the K124 non-inverting gate performs the exclusive OR function.



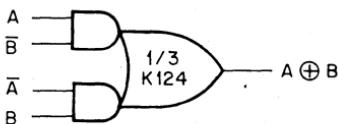
A	B	\overline{AB}
0	0	1
0	1	1
1	0	1
1	1	0

NAND FUNCTION OF BASIC INVERTING GATE



A	B	$A+B$
0	0	1
0	1	0
1	0	0
1	1	0

NOR FUNCTION OF BASIC INVERTING GATE
WITH EXPANDER

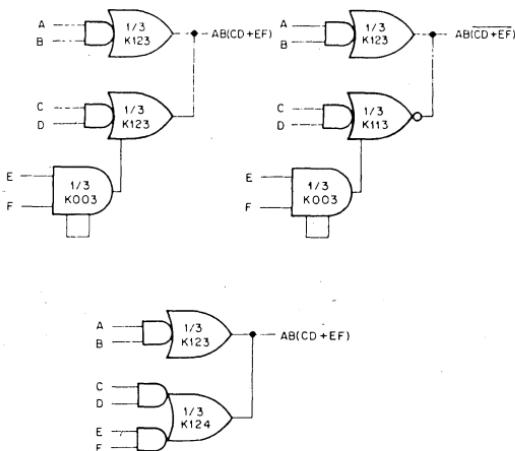


A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

EXCLUSIVE OR USING THE K124 GATE

WIRED AND

Wired AND functions can be obtained by connecting K123 outputs to other K124, K123 or K113 outputs as shown below.



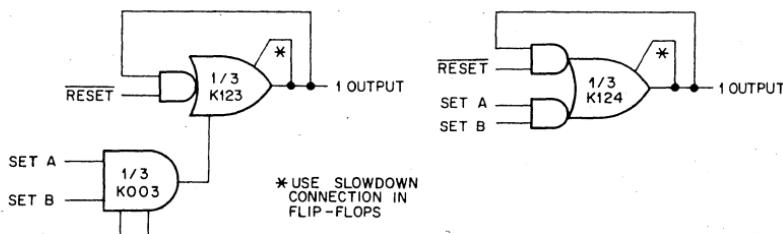
WIRED AND EXAMPLES

SUMMARY OF GATE-EXPANDER LOGIC COMBINATIONS

FOR ZERO VOLTS DEFINED AS LOGIC ZERO standard definition				FOR ZERO VOLTS DEFINED AS LOGIC ONE (inverted definition)			
Logic Function	No. of Inputs	Expanders	Gates	Logic Function	No. of Inputs	Expanders	Gates
AND	2	none	1/3 K123	AND	2	1/3 K003	1/3 K123
	3-5	1/3 K003	1/3 K123		3-5	or 1/3 K012	1/3 K123
	6-8	2/3 K003	1/3 K123		6-9	1/3 K012	1/3 K123
OR	2	1/3 K003 or 1/3 K012	1/3 K123	OR	2	none	1/3 K123
	3-5	1/3 K012	1/3 K123		3-5	1/3 K003	1/3 K123
	6-9	2/3 K012	1/3 K123		6-8	2/3 K003	1/3 K123
NAND	2	none	1/3 K113	NAND	2	1/3 K003 or 1/3 K012	1/3 K113
	3-5	1/3 K003	1/3 K113		3-5	1/3 K012	1/3 K113
	6-8	2/3 K003	1/3 K113		6-9	2/3 K012	1/3 K113
NOR	2	1/3 K003 or 1/3 K012	1/3 K113	NOR	2	none	1/3 K113
	3-5	1/3 K012	1/3 K113		3-5	1/3 K003	1/3 K113
	6-9	2/3 K012	1/3 K113		6-8	2/3 K003	1/3 K113

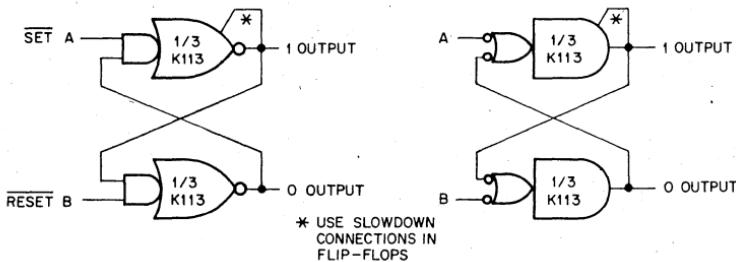
CONTROL FLIP-FLOPS FROM GATES

Control flip-flops can be formed by interconnection of gates as shown below.



NON-INVERTING GATE CONTROL FLIP-FLOP

The output of the flip-flop above is set to a ONE when the two SET inputs are both ONES. A ZERO at the RESET input returns the output to ZERO, provided at least one of the SET inputs is also ZERO.

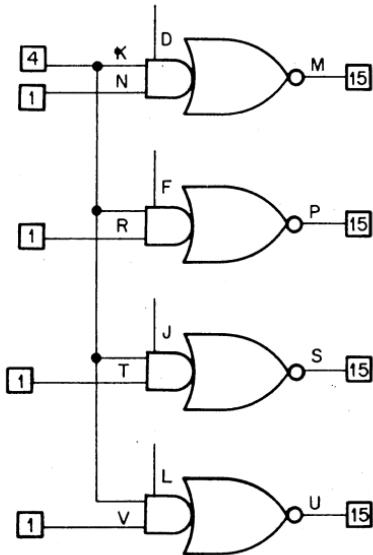


INVERTING GATE CONTROL FLIP-FLOP

The flip-flop above, made from two inverting gates, provides complementary 1 and 0 outputs. A truth table is shown below.

TRUTH TABLE

SET	RESET	1 OUTPUT	0-OUTPUT
0	0	1	1
0	1	1	0
1	0	0	1
1	1	NO CHANGE	

**K134 INVERTERS**

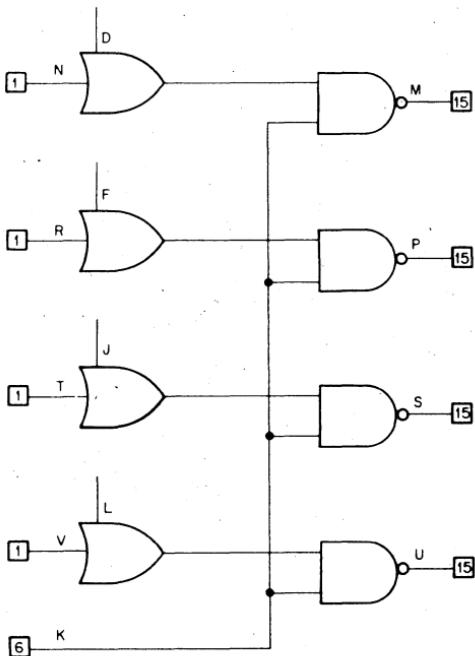
Four flip-flop functional modules such as K210, K220, K230 can conveniently be augmented by a K134 to get "0" as well as "1" outputs. The K134 is also provided with expansion and inhibit inputs for use as the readout element of ready-only memories using K281 diode memories (See Applications Notes). A common input at pin K can force all four outputs high, a helpful feature for building large K281 memories or very large K161 decoders.

K134 inverters may also be AND expanded by K003 gate expanders, providing an efficient way to obtain 4-input NAND or inverted NOR gates.

K134 — \$13

INVERTERS K135

K
SERIES



K135 INVERTERS

The K135 module was designed primarily for the K725 I/O box, but it may be used in applications that require inverters with "OR" expandability. A common input at pin K can force all four outputs high regardless of the "OR" gate inputs. This feature is useful if a K161 decoder is used for multiplexing K135 modules, since all outputs for the same bit can be wire "AND"ed together.

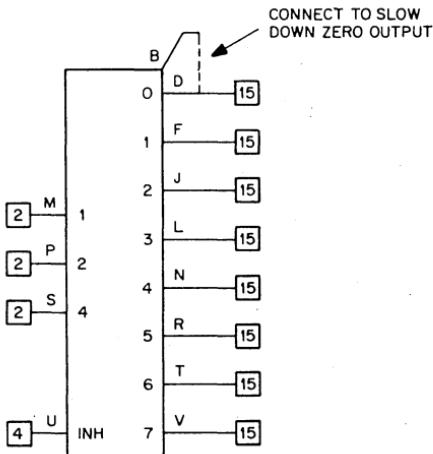
The loading on pin K is initially 6 with no "OR" expansions and increases by "1" unit load for each "OR" input that is added to the module. For example, if a K012 expander was added to each of the four inverters, the total pin K load would be 22 unit loads.

K003 expanders can be used for AND/OR expandability. The number of AND inputs on a given OR input does not affect the loading of pin K.

K135 — \$13

BINARY TO OCTAL DECODER K161

K
SERIES



K161 DECODER

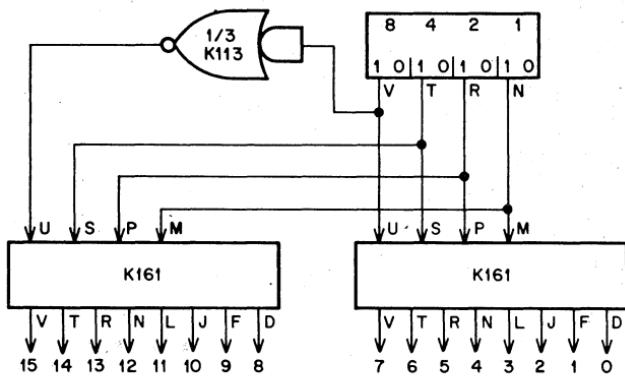
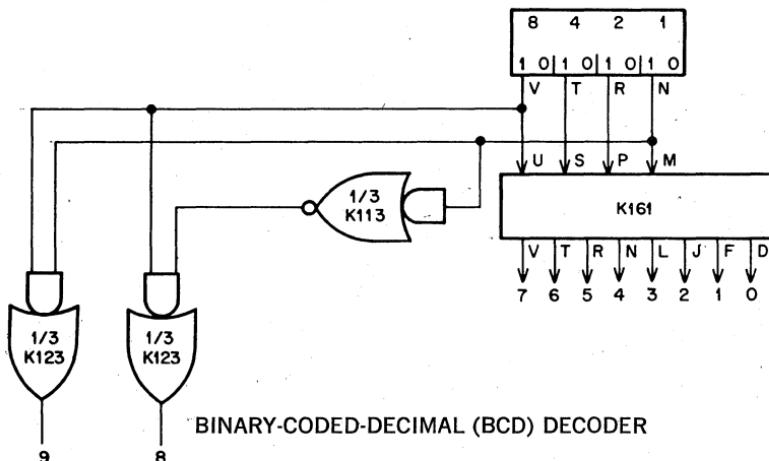
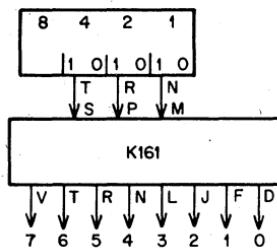
Three-bit binary numbers at the input to the K161 will be decoded into eight one-at-a-time outputs. Both inputs and outputs are high for assertion. The inhibit input allows BCD to ten line decoders to be built, or permits several decoders to be interconnected for sixteen, twenty-four, thirty-two outputs, etc. Inhibit input may be left open if unused, even though high is the inhibit state. When the K161 is being used with M series, all input signals must be buffered with K series gates. This is necessary due to the 3 volt thresholds in the K161.

Standard K Series slowdown circuits on each output minimize and for most purposes nullify the splinter pulses that all decoders emit during input transitions. Additional slowdown available on the zero output can usually suppress the larger splinter that may occur there. But since splinter size is ultimately determined by input timing tolerances, it is cleanest to avoid logic designs in which a decoder output is used as a source of pulses.

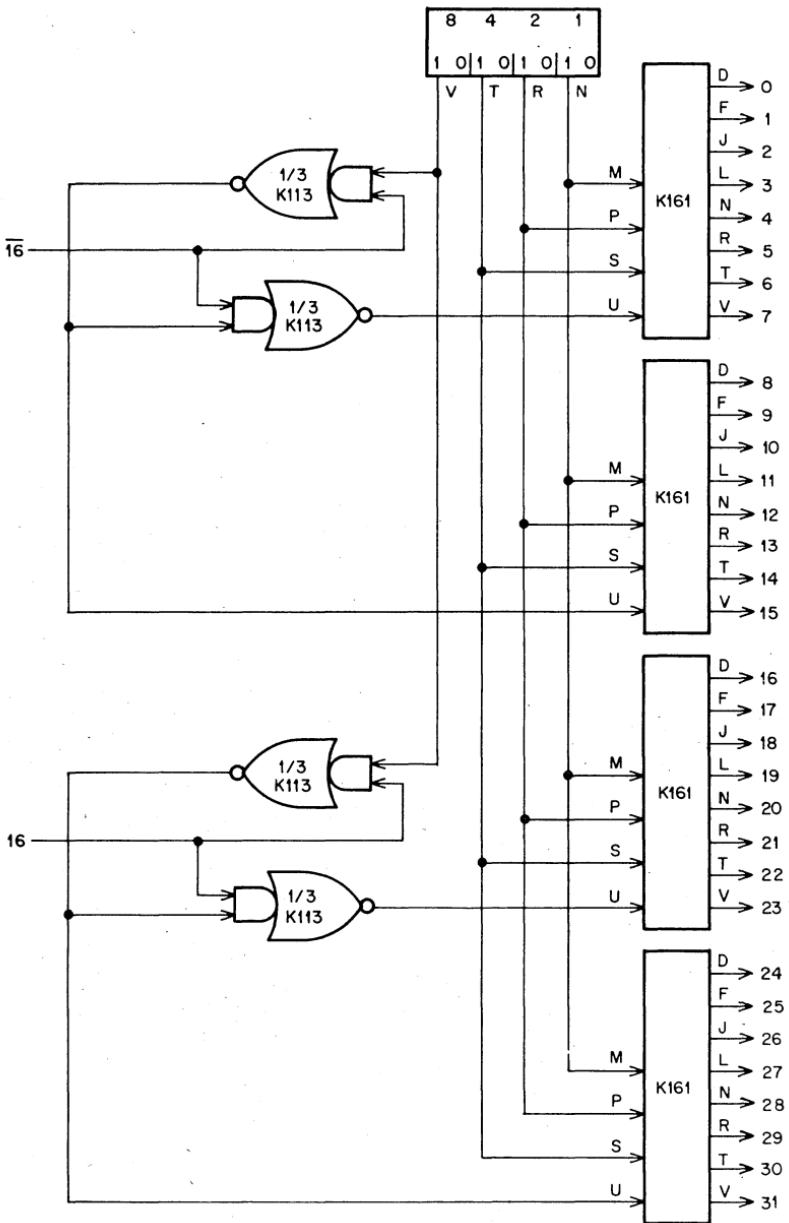
The diagrams below show how to connect decoders for 8, 10, 16 and 32 outputs. Much larger decoders are possible, and in fact up to 256 outputs or even more can be obtained by inhibiting all but one of several decoders.

K161 — \$25

8 STATE DECODER



16 STATE DECODER

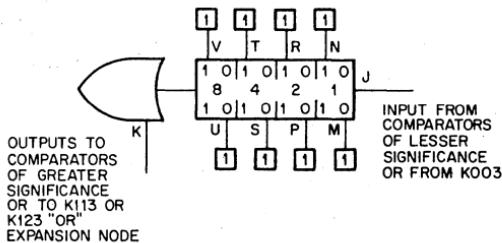


32 STATE DECODER

DIGITAL COMPARATOR

K174

**K
SERIES**



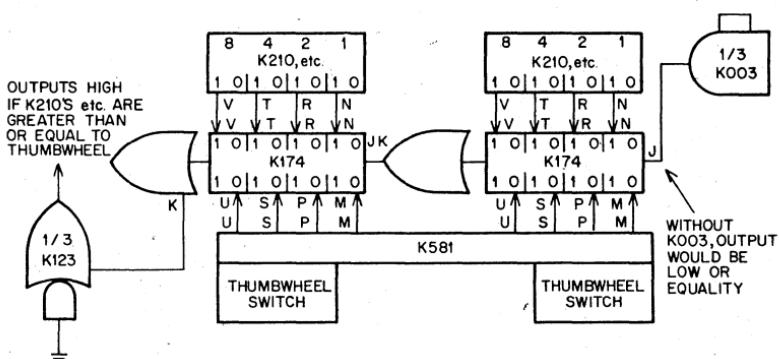
K174 DIGITAL COMPARATOR

Numerical comparisons such as those required in digital positioning controls are facilitated by the K174. Performing the same function as the comparator in closed-loop analog systems, the K174 tells which of two quantities is larger.

Fundamentally, the K174 performs a subtraction to determine whether a "borrow" would be needed to obtain a positive result. The magnitude of the difference is not available; only the sign.

Note in the example below that the output on pin K will be low only if the magnitude of the number in the K210's is less than the thumbwheels.

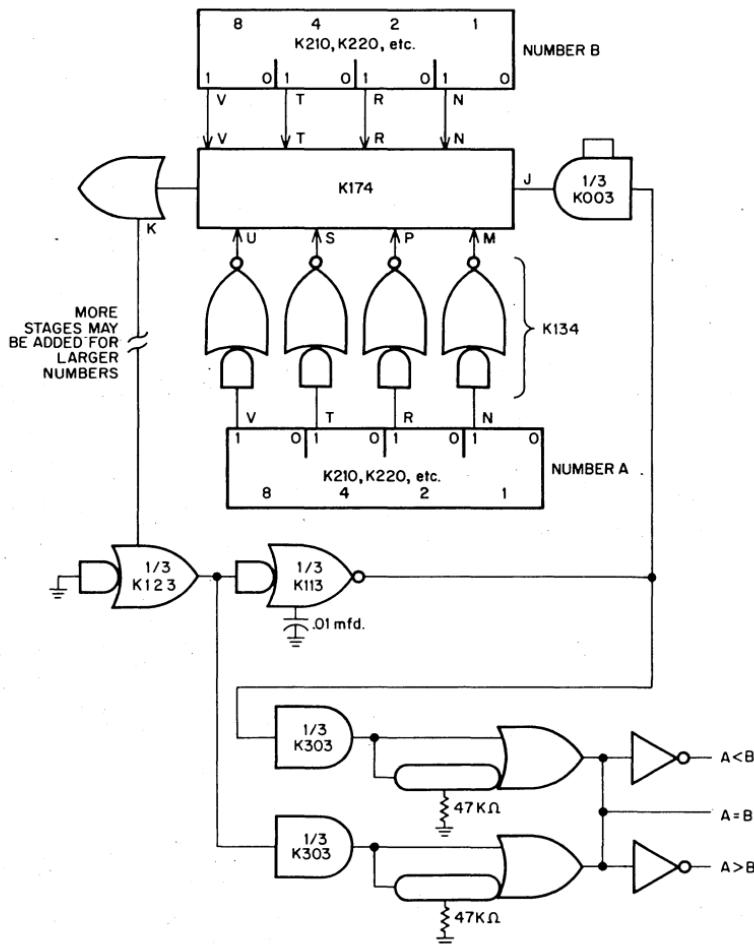
If more than four bits are to be compared, several comparators may be cascaded as shown below. Note use of K003 as if expanding an "OR" to control the state of the output for the case of equal input numbers.



TWO DIGIT COMPARISON OF THUMBWHEELS AGAINST K210, ETC.

If the numbers being compared are not multiples of 4 bits then one of the inputs on each unused comparitor position must be connected to +5 and the other one to ground.

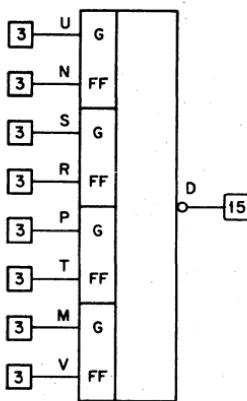
The K174 can also be used to obtain three independent outputs for full-greater-than, equal-to, less-than capability. The application below takes advantage of the fact that if A is equal to B, K will go high if J goes high and K will go low if J goes low. By inverting the output at pin K and feeding it back to pin J, the K174 will oscillate if $A = B$. If the timers are adjusted for a delay longer than the period of oscillation, the three possible output states can be obtained (High for assertion). With the values shown, the frequency will be approximately 50 KHz. Outputs respond to new conditions in 100 μ sec.



K174 — \$18

RATE MULTIPLIER K184

K
SERIES



If the four outputs of K210 counter are wired to K184 "F" inputs, and a four-bit binary fraction presented in reverse order to the corresponding "G" inputs, a pulse train is emitted at an average rate equal to the product of the K210 input rate and the binary fraction. Each transition from "0" to "1" at an FF input produces a 5 μ sec output pulse to ground, if the corresponding "G" input has been high for 5 microseconds or more. Inputs are not rise-time sensitive. Outputs from several rate multipliers may be combined to give any desired precision.

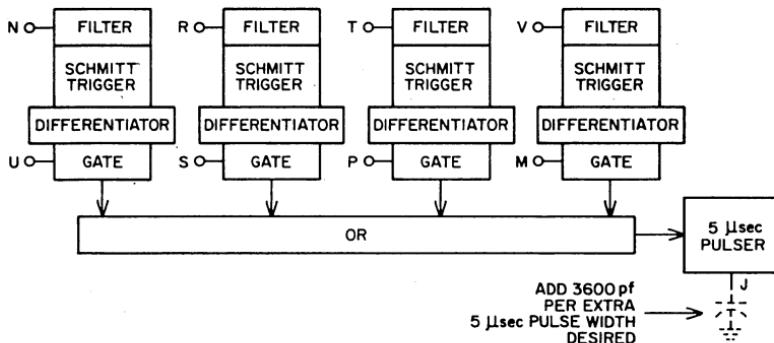
Rate multipliers are primarily useful in numerical control applications, such as those described in the following magazine articles:

"Linear Interpolation" *Control Engineering*, June '64, p. 79.

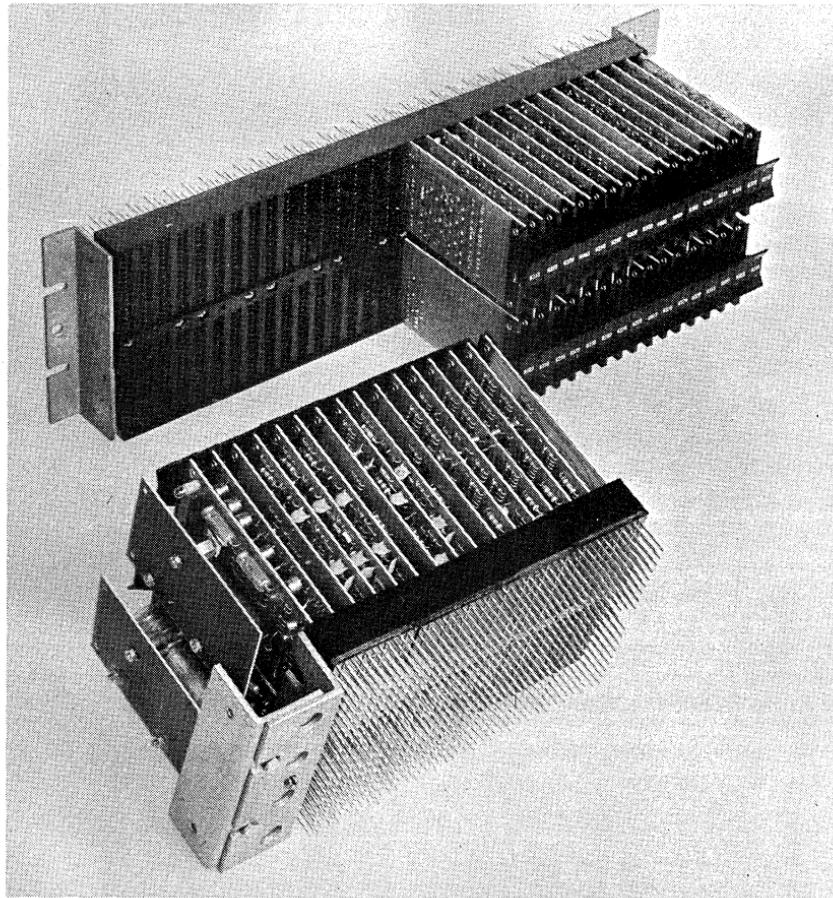
"Curvilinear Interpolation" *Control Engineering*, April '68, p. 81.

"Many Digital Functions Can Be Generated With A Rate Multiplier" *Electronic Design*, Feb. 1, '68, p. 82.

In addition, the K184 can provide several other useful functions that take advantage of its internal complexities.



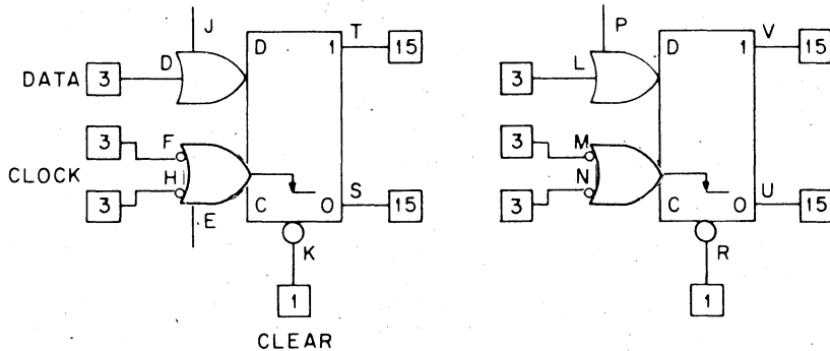
K184 — \$18



FLIP-FLOP

K202

K
SERIES



K202 flip-flops do shifting, complementing, counting, and other functions beyond the capabilities of simple set-reset flip-flops built up from logic gates. They also may be used to extend K210 counters or K230 shift registers.

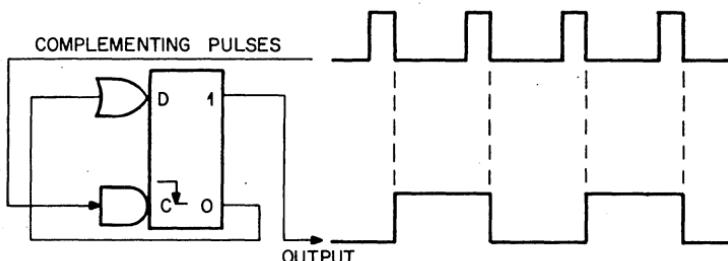
When the output of the clock gate falls from high to low, the information at the OR input (pins D-J, L-P) is transferred into the flip-flop. Pin J (or P) is ORed with the pin D (or L) input. Like pins J and P of a logic gate, these pins can be driven only from a K003, K012 or K026 expander.

Time is required for flip-flops and delayed inputs to adjust to new signals. The clock gate output must not fall to zero sooner than 4 μ sec after its own rise, the end of a clear signal, or a change on associated data input pins.

A K202 flip-flop is cleared by grounding the clear input pin. The flip-flop is held in the zero state as long as the clear input is zero volts, regardless of other inputs.

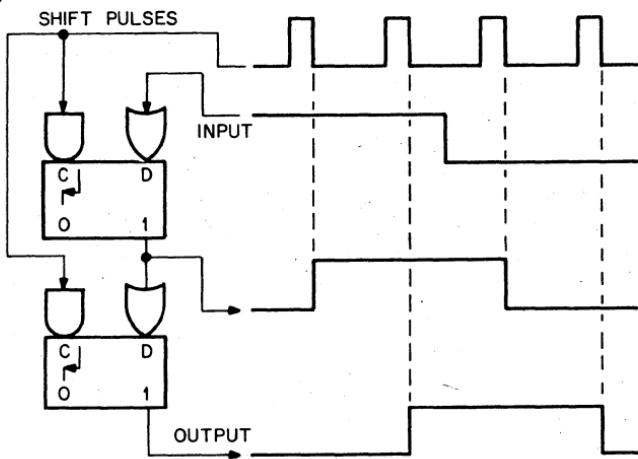
When using a K202 flip-flop to extend the length of a K230 shift register, pins B on both modules must be left open (unslowed). Pin B slows the clock inputs of the K202 for complementing correctly at slow speeds in very noisy surroundings; but the data inputs are not affected by pin B.

Complementing: Below is shown a complementing application. Here the information stored at the data input is the opposite of the flip-flop's present state. Each time the clock gate output changes from "1" to "0", the opposite of the current state is read in.



K202 COMPLEMENTING

Shift Register: The diagram below shows two flip-flops connected as a two-stage shift register. At each step the incoming signal, whether high or low, is set into the first stage of the register, and the original content of the first stage is set into the second stage. The input to each flip-flop must be stable for at least 4 microseconds before another shift pulse occurs, for reliable shifting.



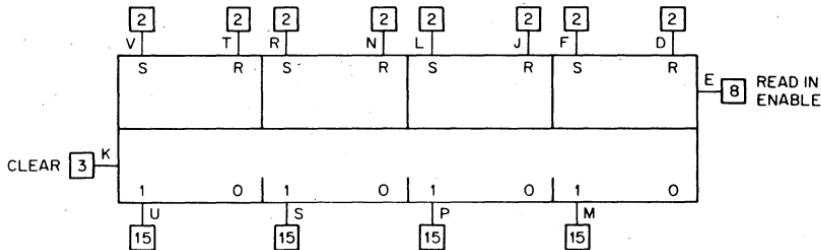
K202 2-STAGE SHIFT REGISTER

Note: In older systems of logic, most flip-flop functions had to be performed by general-purpose flip-flops like the K202. The K Series, however, includes functional types K210, K220, and K230 which are both less expensive and easier to use than the K202 for most applications. Think of the K202 primarily as a complementing control flip-flop and register extender.

K202 — \$27

FLIP-FLOP REGISTER K206

K
SERIES



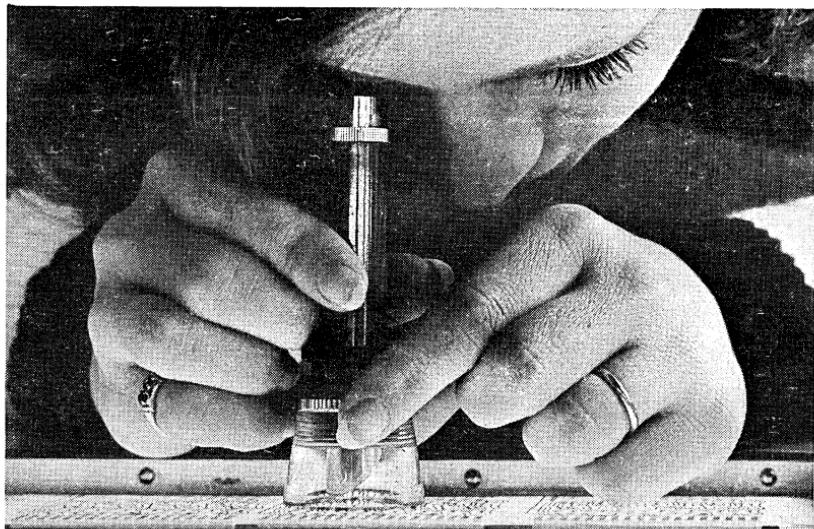
K206 FLIP-FLOP REGISTER

The four set-reset flip-flops in the K206 are arranged for convenient addressing from the outputs of a K161 Binary to Octal Decoder. The flip-flop outputs can then be wired to control and maintain the state of corresponding output drivers, providing addressable output conditioning from teletypes, computers, or fixed-memory sequence controllers.

In addition, the same decoder may be used to address a particular K578 input sampler by grounding the K206 enable input when flip-flop changes are not desired. Pin E enable fanin on the K206 is reduced to 2 milliamperes when K161 addressing is used.

Since most control systems have about half as many digital outputs as inputs, it is convenient to use the least significant bit of the K161 address to determine which flip-flop state is wanted. Odd addresses allow for setting; even addresses, resetting. All flip-flops may be reset together by grounding the clear input, pin K.

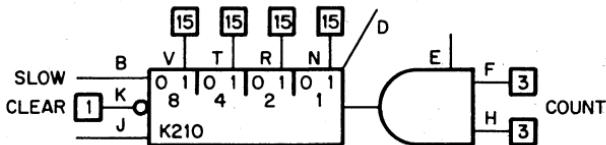
K206 — \$20



All DEC modules are exhaustively inspected and tested, both visually and electronically. A typical module undergoes a printed circuit board inspection procedure that consists of over 70 individual steps.

COUNTER K210

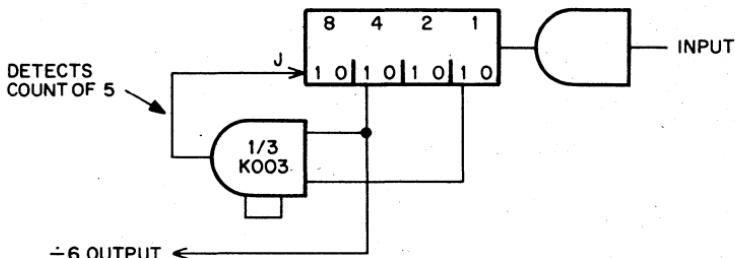
K SERIES



The K210 is a binary or BCD counter that can be wired to return to zero after any number of input cycles from 2 to 16. Count-up occurs when the COUNT gate output steps to zero. Decimal counting logic is built in; when pin D is unused, the counter resets to zero on the next count after nine. When pin D is grounded, the counter overflows to zero, after a count of 15. (Pin D is not intended for dynamic switching between binary and BCD counting.)

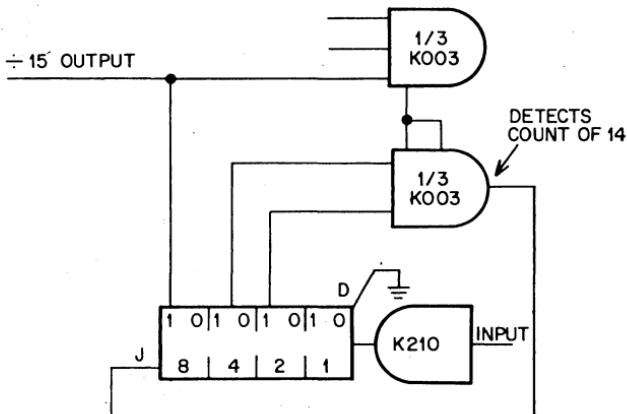
The counter is reset by grounding the clear input for 4 microseconds or more. A positive level at the J input from a K003 expander also resets the counter on the next high to low transition of the COUNT gate output for counts other than 10 or 16.

Wire the K003 as a decoder to detect one count less than the desired modulus. (Detect 5 for a count-of-6 counter, etc.)



K210 CONNECTED FOR COUNT OF 6

For counts above 10, ground pin D. Combine two K003 expanders as shown below, where three counter outputs must be sensed (to divide by 12, 14, or 15).

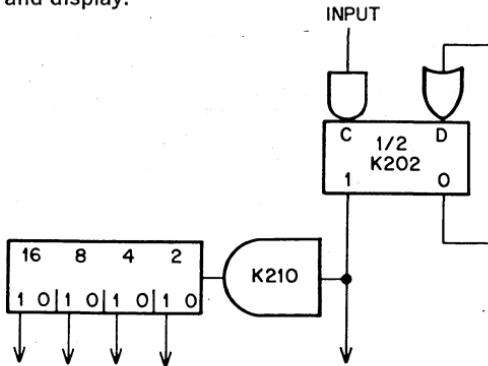


K210 CONNECTED FOR COUNT OF 15

Time is required for flip-flops and pin J reset logic to adjust to new inputs. The count gate output must not step to zero sooner than 4.0 μ sec after its own rise, a change at pin J, or the end of a clearing signal at pin K. **When pin B is grounded for slowdown, allow 50 μ sec.** Larger counters are obtained by cascading K210's or adding K202 flip-flops. To cascade K210 modules, wire the most significant output of one counter to the input gate of the next. Inputs to the least significant stage can be either pulses or logic transitions to ground; risetime is not important.

Any transducer such as a switch, photocell, pulse tachometer, thermistor probe, or others compatible with K508 or K524 input converters can generate the signal which is to be counted. The lack of input risetime restrictions may allow transducer outputs to drive K210 counters directly if damaging transients can be avoided, as when the transducer shares the logic system environment.

For visual readout of binary-coded decimal counters, the four outputs from each K210 may be connected to corresponding input pins on a K671 decoding driver and display.

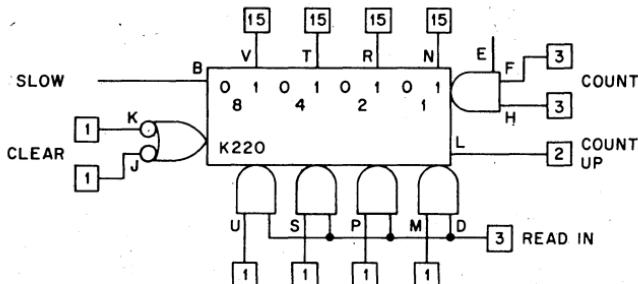


K210 AUGMENTED WITH K202 FOR COUNT OF 32

K210 — \$27

UP/DOWN COUNTER K220

**K
SERIES**

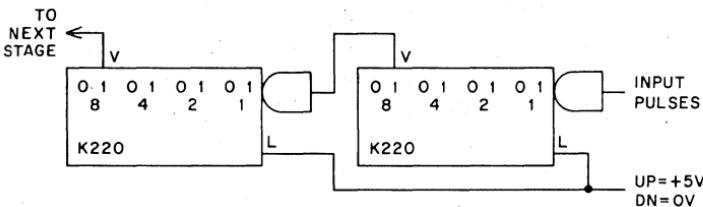


(DOUBLE-SIZE BOARD)

Four flip-flops and all the gates needed for binary-coded decimal up counting, down counting, presetting, and clearing are built into the K220. Up-down counters are useful for many digital position readout and feedback applications.

The direction of counting is established by the signal at pin L, high for up counting and low for down counting. Pin L count direction changes should finish no later than 4.0 μ sec before next count input.

When K220 counters are cascaded, a single connection from the "8" output of one K220 to the count input gate of the next establishes both carry and borrow propagation.



CASCADED K220 COUNTER

K220 — \$52

Up-counts occur when input makes the transition from high to low (-5 v to 0 v), as in K210 and K230. Down-counts, however, take place on the transition from low to high (0 v to +5 v). Thus both carry and borrow signals propagate via the simple connection from 8-weight output to 10-weight input.

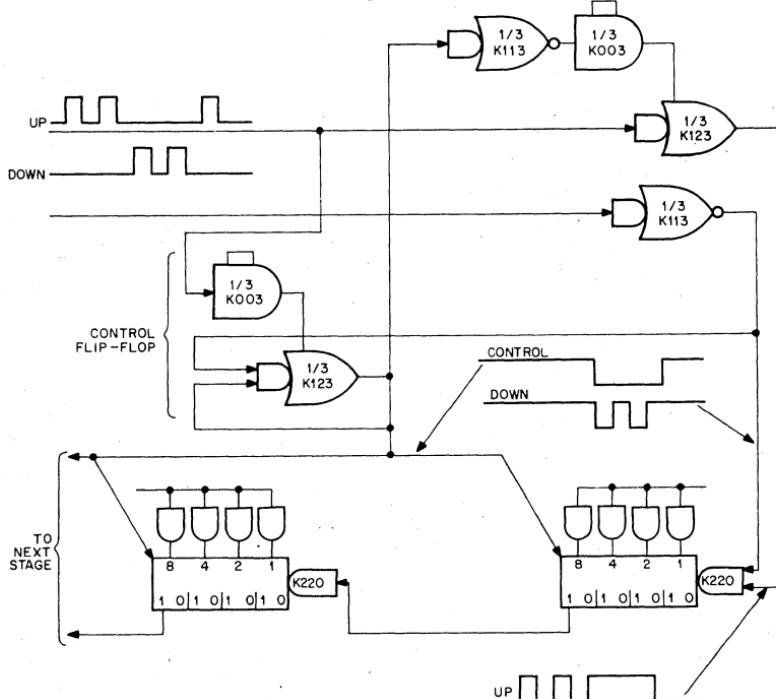
ONEs present at readin gate pins U,S,P, or M are read into the respective flip-flops when pin D makes the transitions from low to high. The transition at pin D should finish not later than 4.0 μ sec before next count input. Transition from low to high at pin D should also begin no sooner than 4.0 μ sec after any previous transition at pins D,M,P,S, or U. Ground any unused readin gate inputs to prevent readin of undesired ONEs.

Grounding pin J or K forces all flip-flops to zero for as long as either clear input remains low.

Time is required for flip-flops, counting logic, or readin gates to adjust to new inputs. Except clear inputs, no counter input may be changed within 4 μ sec of a transition at any other input (Refers to logical output of count gate). When pin B is grounded for slowdown, allow 50 μ sec.

All connections are made on the upper connector, except two: binary Up/Down counting may be obtained by grounding pins D and E on lower connector.

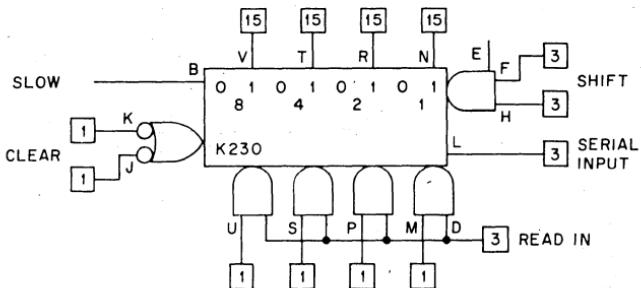
Below is shown a means for accepting up and down pulse-trains from two separate sources. For this application input pulse spacing should be at least 20 μ sec and input pulse width should be at least 10 μ sec.



UP/DOWN COUNTER
FOR SEPARATE PULSE SOURCES TO 50Kc

SHIFT REGISTER K230

K
SERIES



(DOUBLE-HEIGHT BOARD, ALL
CONNECTIONS ARE TO UPPER SOCKET)

Information presented to pin L of this four stage flip-flop register is shifted toward pin V with each transition from "1" to "0" at the shift input gate.

ONEs present at readin gate input pins M,P,S, or U are read into the respective flip-flops when pin D makes the transition from low to high. The pin D transition should finish no later than 4.0 μ sec before the next count input. Transition from low to high at pin D should also begin no sooner than 4.0 μ sec after any previous transition at pins D,M,P,S, or U. Ground any unused readin gate inputs to prevent readin of undesired ONEs.

Grounding pin J or K forces all flip-flops to zero for as long as either clear input remains low.

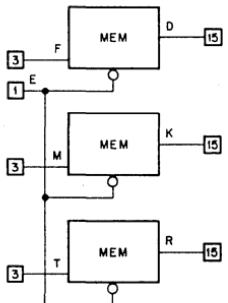
Shift registers of any length can be formed by tying pin V of one K230 to pin L of the next, and operating all shift gates together. Supply all shift pulses from the same device to maintain synchronism. The propagation delay of even one gate is too large a difference between two shift inputs on the same register. For every 20 bits that are required, duplicate the last stage of the shift-generating logic and tie the outputs in parallel to all K230 shift gate inputs.

Time is required for flip-flops, shifting logic or readin gates to adjust to new inputs. Except clear inputs, no register input may be changed within 4 μ sec after a transition at any other input. (Refers to logical output of shift gate). When pin B is grounded for slowdown, allow 50 μ sec.

K230 — \$36

RETENTIVE MEMORY K273

K
SERIES



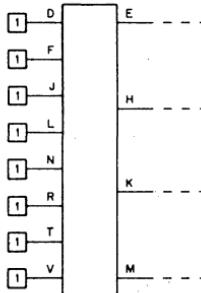
(DOUBLE THICKNESS MODULE)

Three magnetically latched mercury wetted contact relays in the K273 follow logic-level input information at rates up to 100 Hz, when pin E is grounded. Normally the OK Level output from a K731 source module drives pin E. When a line voltage failure is detected, pin E rises and each relay mechanically stores the last valid input data until full power returns.

K273 — \$72

FIXED MEMORY K281

K
SERIES



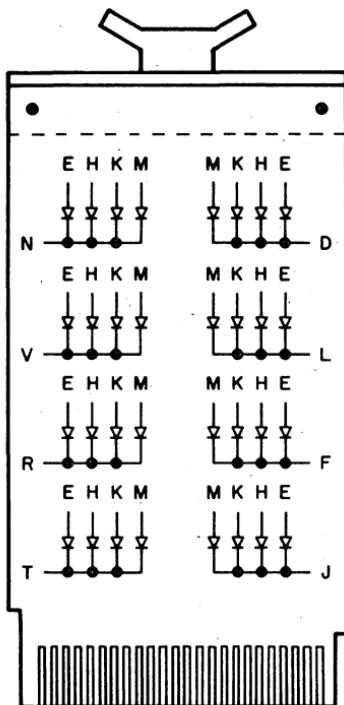
K281 FIXED MEMORY

The K281 is designed to be used with the K161 (Binary to Octal Decoder), the K681 (8-30 ma drivers) and the K134 (4 inverters), to build a read-only memory. Each K281 initially contains eight four-bit words consisting of only "1's". The user selects the codes he desires by cutting out diodes in the bit positions that are to be "0's". Additional K281 and K134 modules may be added to the system to generate more words and longer words. See Applications Notes for diagram of memory configuration.

K281 — \$8

CODING THE K281 DIODE MEMORY

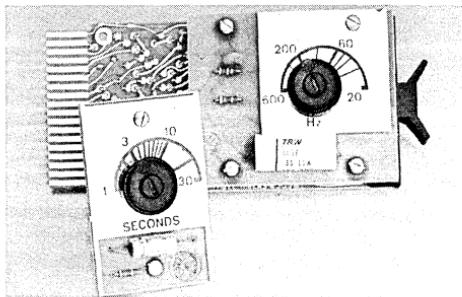
When the K281 is used to build a K-Series Read Only Memory, the codes are stored by cutting out diodes where zeros are desired. The diode map below shows the physical location of the diodes on the K281 and how they are connected to the module pins.



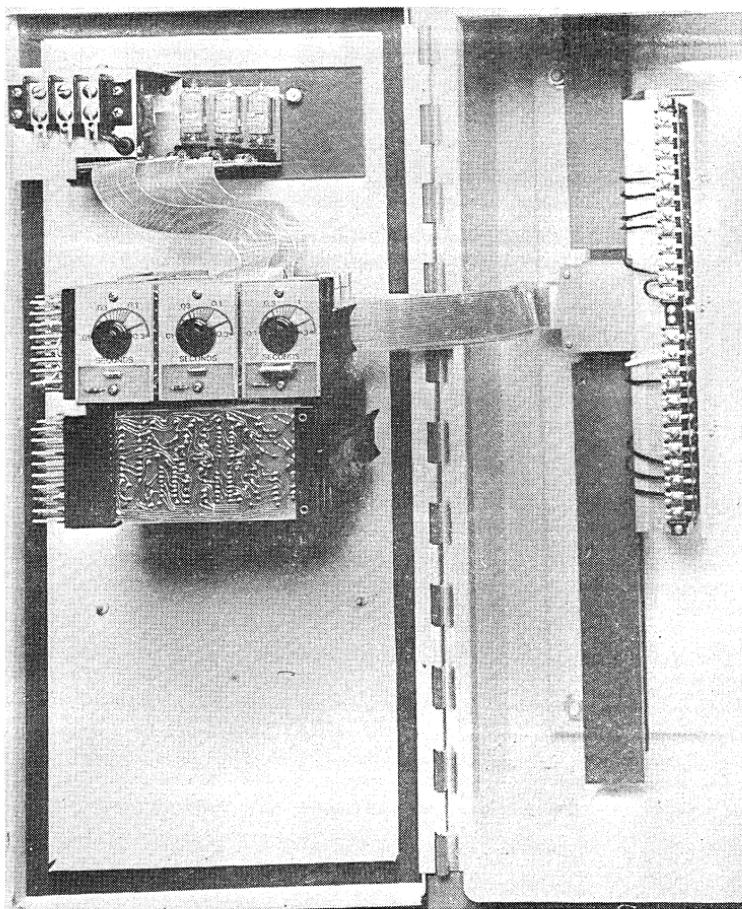
E, H, K, M are the four output pins.

D, F, J, L, N, R, T, V are the eight drive lines.

Component side up



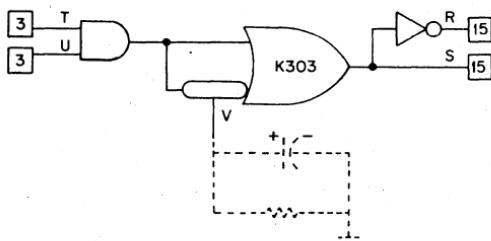
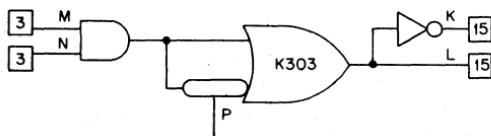
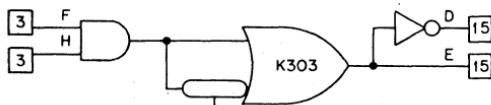
K303 WITH K373 AND K378



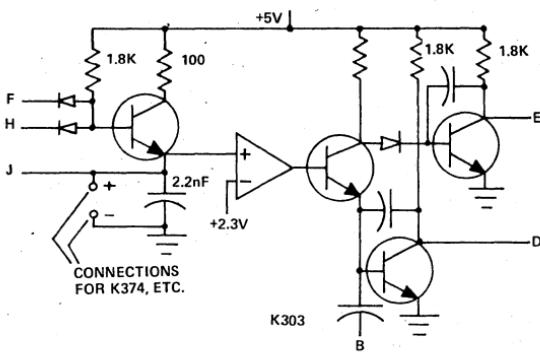
SMALL K-SERIES CONTROL INSTALLED IN NEMA 12 ENCLOSURE

TIMER AND CONTROLS
K303, K371, K373, K374, K375, K376, K378

**K
SERIES**

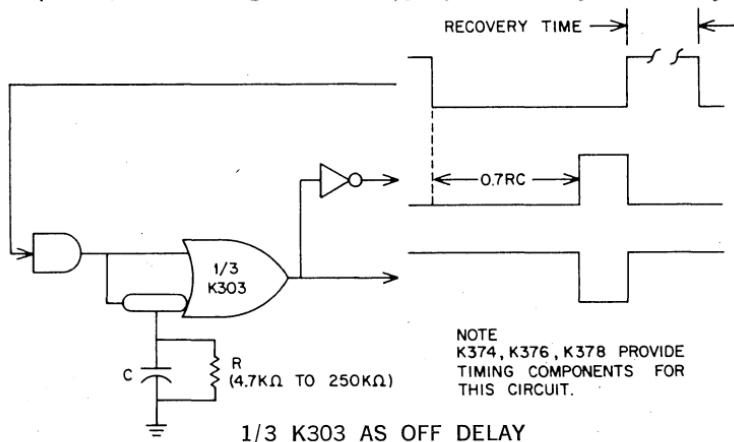


K303 timers provide time delays from 10 microseconds to 30 seconds and can be interconnected to form clocks with periods covering the same intervals. Fixed or adjustable delays and frequencies are obtainable. Calibrated controls are available (K371 through K378) for mounting directly on the K303. Remote controls can be added, if desired. A simplified schematic of the K303 is shown below. Note that the comparator has hysteresis, increasing the rejection of false "1" noise peaks at the input.



K303 TIMER SIMPLIFIED SCHEMATIC

When a K303 input gate steps to zero, the uninverted output falls after a controlled interval, while the inverted output rises. The interval can be as little as 10 μ sec or as long as 30 seconds, depending on the size of the R and C connected to pin J,P, or V. Recovery begins when the input gate rises to 1. Allow recovery time of at least 0.3% of the maximum delay obtainable from the capacitor, in order to guarantee 95% repeat accuracy in the delay.

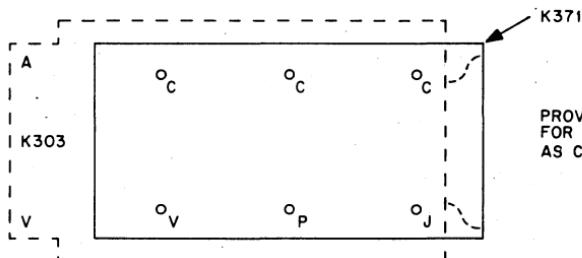


A positive step at the input gate resets the K303 timer outputs. If the step occurs before a timeout is complete, the timeout is terminated and no change appears at the outputs. This property is sometimes convenient for establishing a pulse repetition rate threshold (Frequency Setpoint).

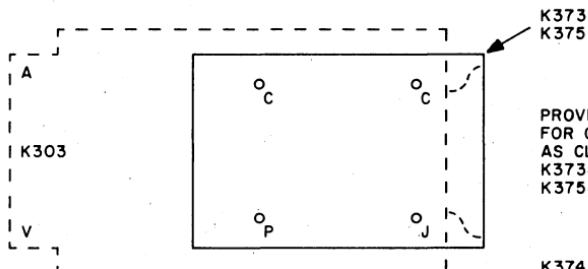
A built-in 2.2 nanofarad timing capacitor assures adequate noise rejection when external capacitors are mounted several inches from the timer. Time threshold for resetting is always several percent of rated recovery time, so that noise rejection time increases in proportion to the size of the timing capacitor. Remote rheostats and timing capacitors may be used, but noise rejection will be degraded. If several timing capacitors will be switch selected, wire in the smallest near the module and switch the others in parallel with it.

Variable or fixed timing resistors used with K303 timers may be any carbon composition, film, or wirewound rheostat or potentiometer. Delay time is linearly proportioned to resistance from 250K Ω down to a few thousand ohms, falling to zero (reset inhibited) below a few hundred ohms. Momentary shorting to ground of control pins will not cause damage, but a padding resistor of at least 300 Ω in series with variable controls is advisable both to prevent continuous grounding and to avoid confusion which may arise if resetting is inhibited.

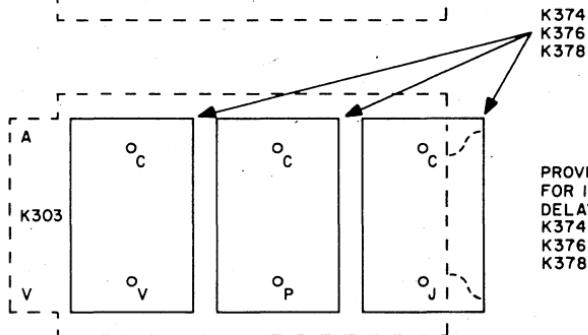
Timing capacitors may be any ordinary mica, paper, ceramic, or low leakage electrolytic type. For delays above a few seconds, wet slug tantalum electrolytic capacitors are advisable to avoid leakage-induced drift at high temperatures. Temperature coefficient of delay has been optimized for the carbon composition potentiometers and tantalum electrolytic capacitors used in the controls described below, and is typically less than $\pm 1\%$ in 5°C (9°F) using K731 and K732 regulators for power.



PROVIDES TIMING COMPONENTS
FOR OPERATION OF 3/3 K303
AS CLOCK FROM 200Hz to 6KHz



PROVIDE TIMING COMPONENTS
FOR OPERATION OF 2/3 K303
AS CLOCK:
K373: 600Hz to 20Hz
K375: 60Hz to 2Hz



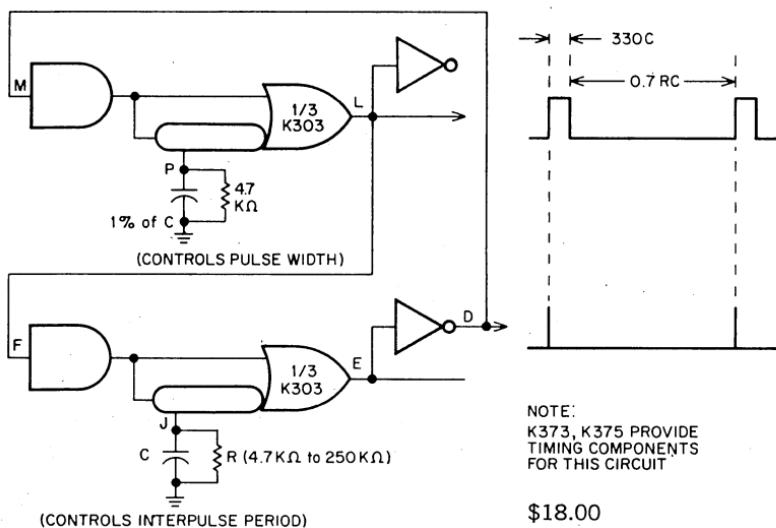
PROVIDE TIMING COMPONENTS
FOR INDIVIDUAL (1/3)K303
DELAYS:
K374: 0.01 to 0.3SEC
K376: 0.1 to 3.0SEC
K378: 1.0 to 30SEC

Calibrated controls for timers and clocks are available in several ranges. They mount to the K303 module by two screws per circuit, providing both mechanical and electrical connections. Each control includes a logarithmic potentiometer for easy settling over the full 30:1 calibrated range. Calibrations are approximate, meant for quick setup and easy control identification. Accurate time settings require the use of an oscilloscope, stopwatch, or other reliable time standard. These controls are intended for use at the end of K941 mounting bars.

Note: Time delay jitter is proportional to supply voltage ripple if times of the order of 1 msec are selected. For critical applications, use light loading on separate K731 or use H710 supply.

TIMER K303

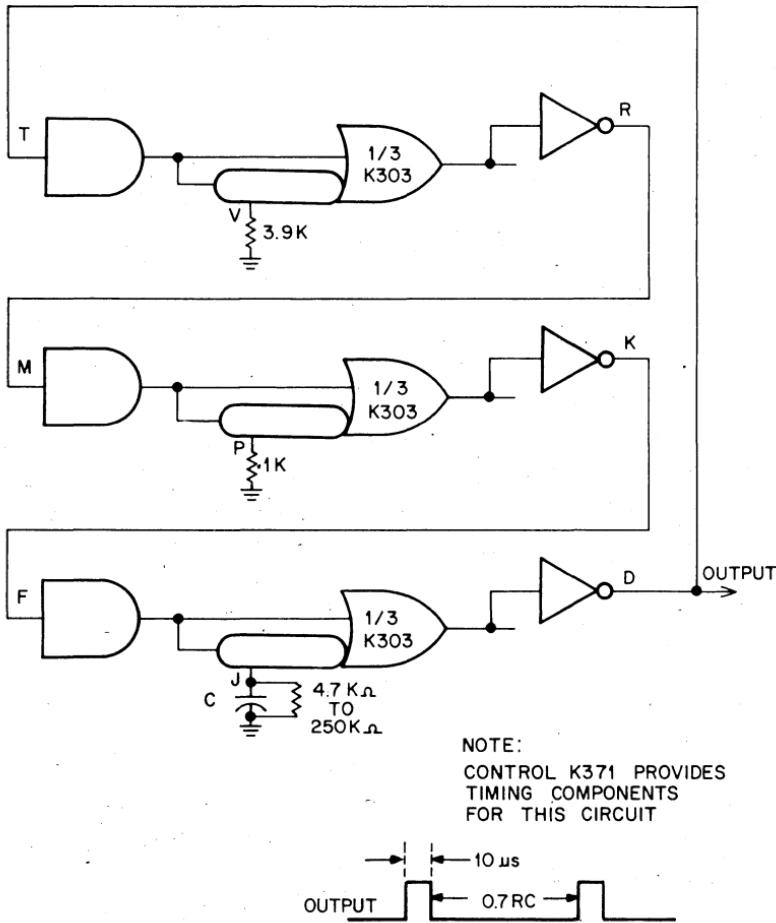
Two K303 sections can be interconnected to make a free-running oscillator if one of the timing capacitors is about 100 times smaller than the other. The circuit with the larger capacitor will predominantly control the frequency. The diagram below shows the interconnections.



2/3 K303 AS CLOCK BELOW 1 KHz

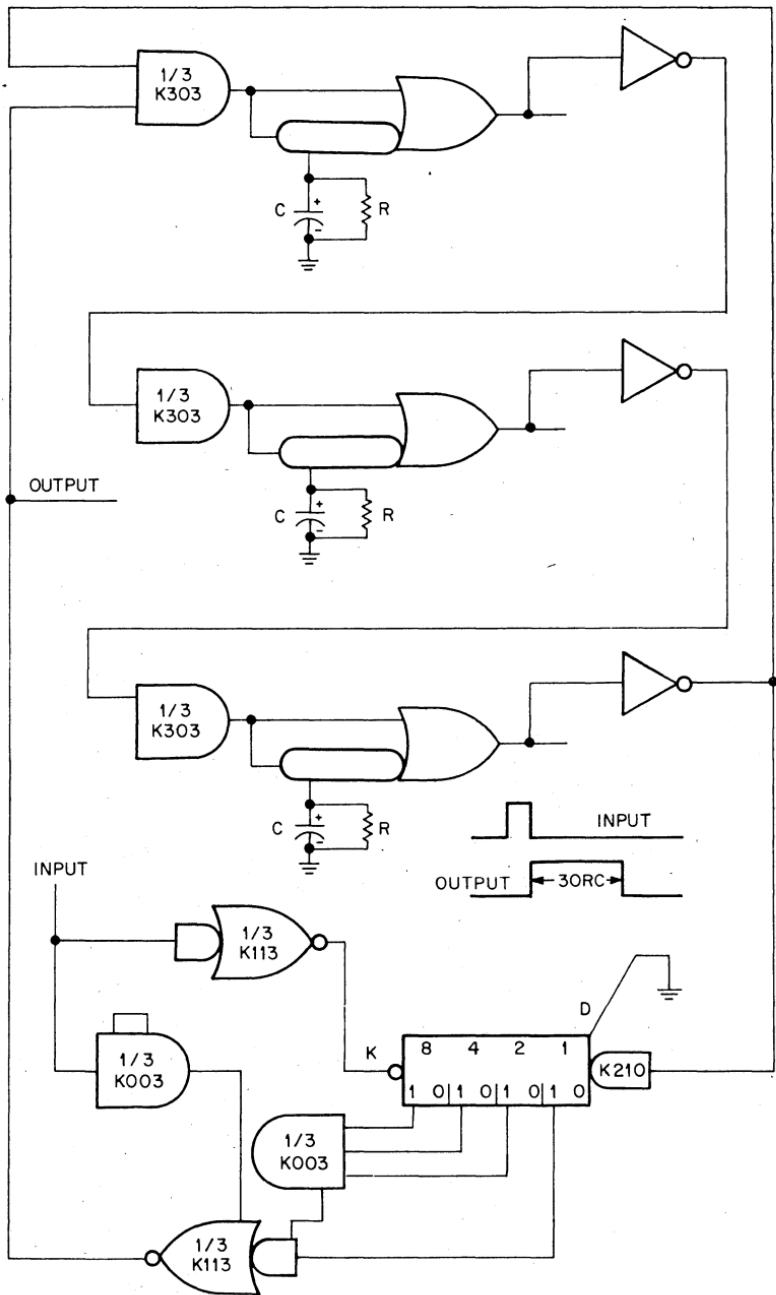
The 100 to 1 ratio of timing capacitors required limits this method to frequencies to 1 KHz or less, due to the 2.2 nanofarad capacitor built into each circuit. Three K303 circuits may be connected together for higher frequencies, as shown on next page.

K303 — \$27
K371 — \$8
K373 — \$8
K374 — \$7
K375 — \$8
K376 — \$7
K378 — \$9



3/3 K303 AS CLOCK ABOVE 500 Hz

Longer delays than 30 seconds using large electrolytic capacitors would suffer from increased drift due to capacitor leakage. Moreover, there are some applications in which moisture and contamination cannot reliably be excluded from the electronics environment, making 250K Ω timing resistance impractical due to leakage along board surfaces. For either situation, two techniques are available: either cascade several timer circuits, or combine a clock-connected K303 with one or more K210 counters. The clock may be gated off at an unused input to avoid synchronizing errors. The diagram below shows both techniques combined, using one K210 and all three sections of a K303 to obtain a 22-minute delay.

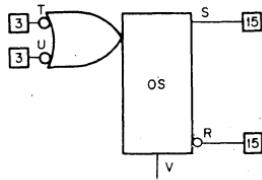
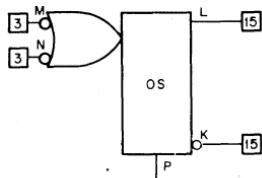
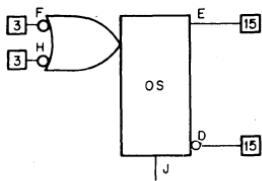


TIMER FOR UP TO 22 MINUTES

ONE SHOTS

K323

**K
SERIES**



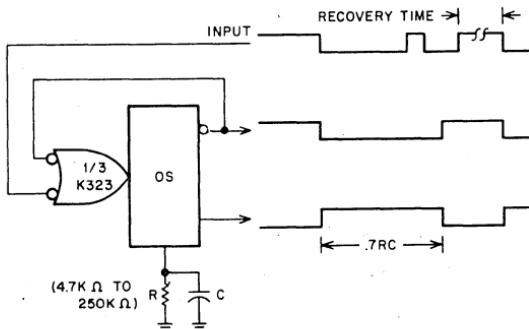
K323 one shots provide output pulse widths from 10 microseconds to 30 seconds with either fixed or adjustable delays. Calibrated controls are available (K374, K376 and K378) for mounting directly on the K323. Remote controls can be added, if desired.

When the K323 input gate steps to zero, the uninverted output rises and stays positive for the controlled interval time. The pulse width is controlled by the value of R and C connected to pin J, P, or V. The one shot recovery begins when the input gate rises to 1. Allow a recovery time of at least 0.3% of the maximum delay obtainable from the capacitor, in order to guarantee 95% repeat accuracy in pulse width.

K323 — \$35

A positive step at the input gate forces the uninverted output low. If the step occurs before a time out is complete, the timeout is terminated and the pulse width will be unknown. This premature resetting can be eliminated by connecting the inverted output of the one shot to one of its AND inputs. This will make the one shot insensitive to input transitions during the time out period.

A positive pulse does not terminate the timeout

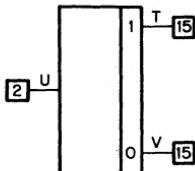
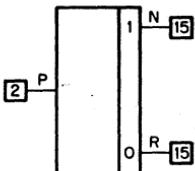
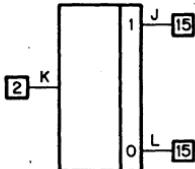
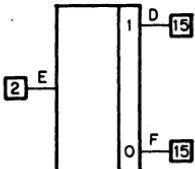


The K323 circuit is similar to the K303 Timer and uses the same techniques of noise rejection. For further information on resistors, capacitors and construction recommendations for external pulse width controls, please refer to the K303 module.

SCHMITT TRIGGERS

K501

K
SERIES



The K501 can be used with the K580, K581, or K578 to provide simultaneous true and complement signals with full K series drive. Built in hysteresis and slowed outputs insure reliable operation in noisy signal environments.

Schmitt Triggers can also be used to speed up signals with very slow rise or fall times for input into pulse formers or logic circuits where timing considerations are critical.

The K501 is not designed to be connected directly to unfiltered contacts or other noisy signal sources.

K501 — \$20

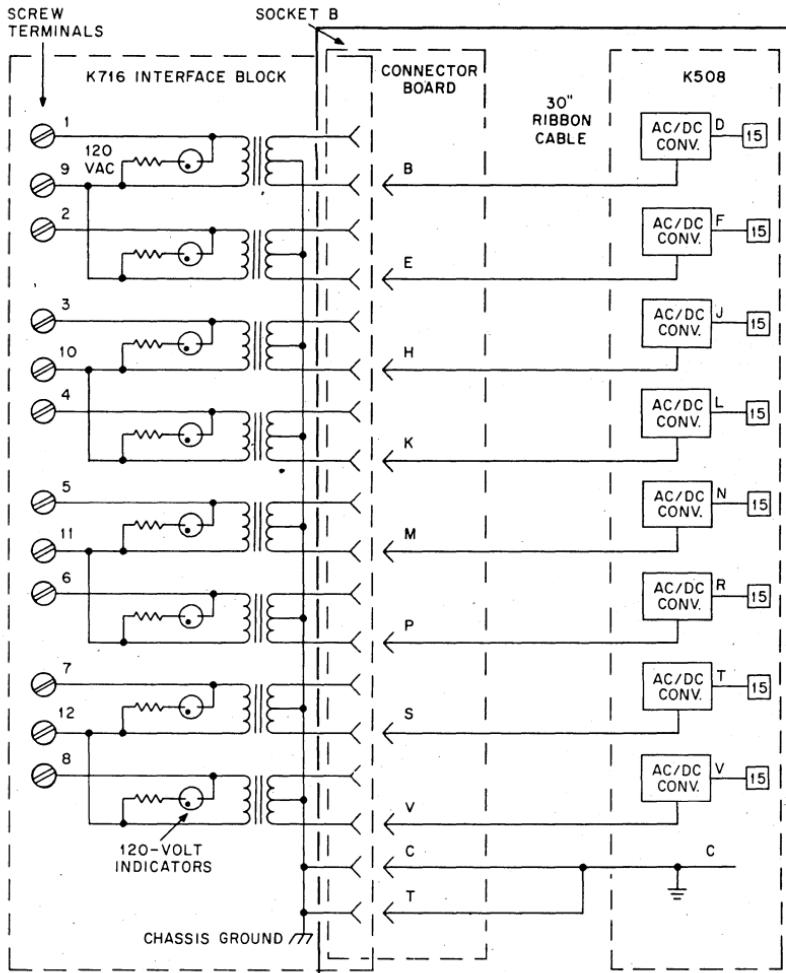
ACCESSORIES CONTAINING ELECTRONICS

On the following pages is a broad selection of interface modules. To help you get acquainted with the range of capabilities they offer, here is a summary table. Grouping by type of use to aid selection is not rigid. Maximum compatibility has been preserved to permit any combination of modules to be put together in the same system.

Logic-to-Interface Connection and Type of Use	Module Type	Compatible Accessories			
		K716 Inter- face Block	K724 K725 Shells	K782 Thru Ter- minal	K784 Diode Ter- minal
Integral 30" Flat cable connector. For small controls with heavy-duty field wiring	120 VAC input: K508 120/240 VAC output: K604 Transducer input: K524 2.5 Ampere DC Driver: K644	X X X X		X X X	
Integral Terminals for larger systems	120 VAC input: K578 120/240 VAC output: K614 250 Volt DC Driver: K656 4 Amp Driver: K658		X X		
Solder Lugs with strain relief. For indicators, control panels, and nearby transducers	Transducer Input: K522 Dry circuit switch filter: K580 Inverted switch filter: K581 Low power indicator driver: K681 Indicator/Relay driver: K683			X X X	X
Integral 12" flat cable with NIXIE® tubes	Decimal Display: K671				

AC INPUT CONVERTER TYPE K508

K
SERIES

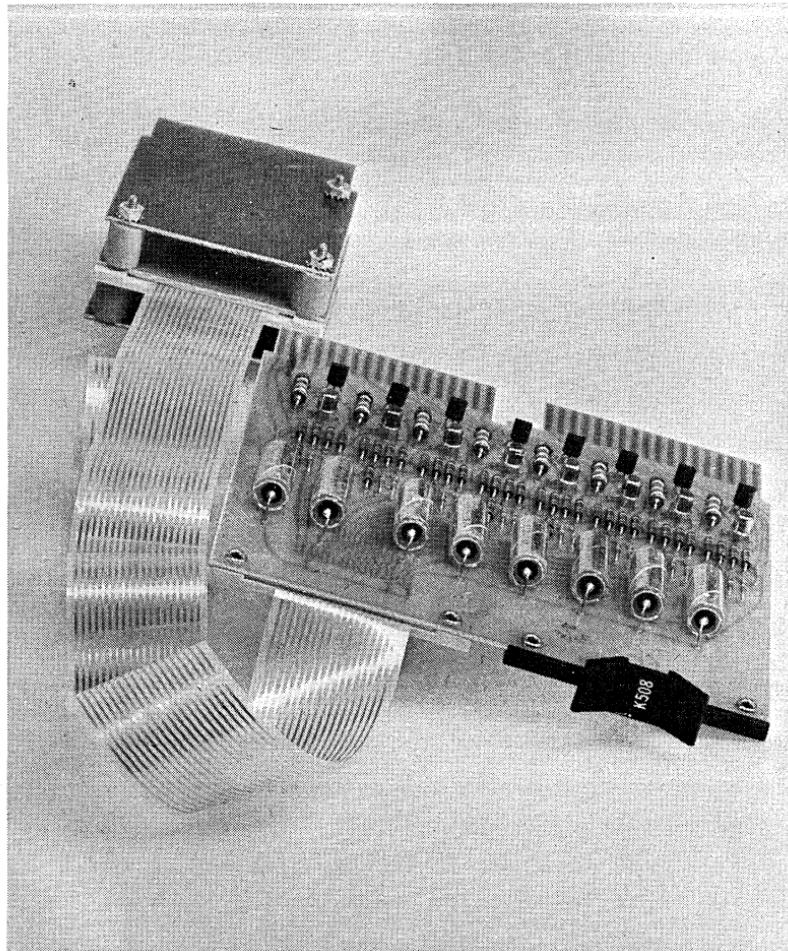


K508 — \$44

The K508 AC input converter, operating through the K716 interface block, is designed for use with ordinary silver contacts in limit switches, pressure switches, pushbuttons and the like. Each input terminal presents a reactive load of 1 volt-ampere, which together with an external 120 volt AC pilot circuit voltage inhibits contamination buildup at the contact surface.

Electrical noise riding on pilot circuit wiring is attenuated in the input transformers and by hash filters at the K508 module. Contact bounce filtering is designed to respond to the first signal, and to leave the logic output in the "1" state in spite of skips lasting up to 100 milliseconds.

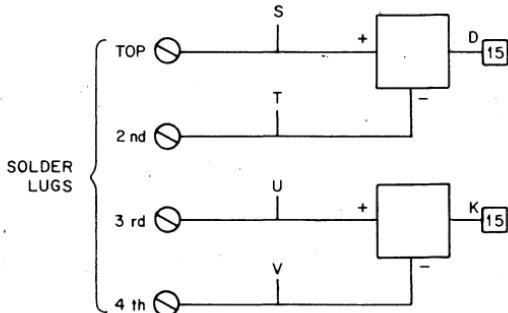
K508 output circuits have hysteresis, so that no intermediate output state can result from an ill-defined input condition. No separate Schmitt-triggers are required. Outputs are at ground for no input, at +5 volts when energized. All connections use upper connector.



SENSOR CONVERTER

K522

**K
SERIES**



K522 SENSOR CONVERTER

The K522 Sensor Converter can take signals from photocells, thermistors, and other variable-resistance sensors and convert them to logic levels. Its built-in +1.8 volt reference, programmable hysteresis, and noise cancelling ability make it simple to use. The K522 does not, however, provide the tolerance to high level noise or accidental application of line voltage which is obtainable from the K524. The table below should help in deciding between the two types.

CHARACTERISTICS	K522	K524
Number of circuits	2	4
Module size	single	double
Input connections	solder lugs	cable connector
Inputs accessible at module connector	yes	no
DC differential mode possible	no	yes
Provision for adding transducer biasing trim pots in predrilled holes on board	yes	yes
Noise cancellation range (common mode)	± 1 volt	± 7.5 volts
Maximum + input range for correct output	0 to +5V	± 30 V
Tolerance to overvoltage (no damage)	± 3 volts	140 VAC
Minimum hysteresis (deadband)	10mv	10mv
Maximum hysteresis	160mv	10mv
Maximum switching rate	50KHz	25KHz

K522 — \$22

Minimum transducer resistance (at threshold)	400Ω	400Ω
Maximum transducer resistance (at threshold)	20KΩ	100KΩ
Noise Cancellation ratio at Line Frequency (CMR)	10:1	10:1
Noise Cancellation ratio at 1 KHz	20:1	20:1
Temperature Coefficient of Threshold (typical)	±1mv/°C (0.1%)	±1mv/°C (0.1%)

Note: Outputs are high when + input is high.

In general, the K522 is suited to laboratory and light machinery use where transducers are nearby and there is little danger of high voltage being applied to them accidentally. This is especially important when low resistance transducers are used with board mounted trimpots, since the trimpot provides a path from the transducer leads back to the logic supply. (If high voltage such as 120 VAC) were to get to the logic supply, all modules in the system would be destroyed.

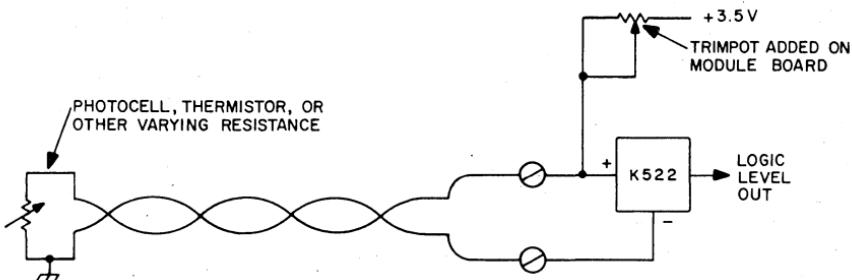
The hysteresis of each K522 circuit can easily be selected in increments of 10 mv from a minimum of 10 mv (no connection) to a maximum of 160 mv by connecting one or more programming pins to the output.

Below is a table of pin connections for programming the hysteresis of each circuit.

Value when wired to converter output	10mv	20mv	40mv	80mv
Circuit 1 (Pin D)	E	F	H	J
Circuit 2 (Pin K)	L	M	N	P
Table of Hysteresis Programming Pins				

Example: To add 30 mv hysteresis to the basic 10 mv hysteresis for a total of 40 mv hysteresis, connect pins E and F or L and M to the circuit outputs.

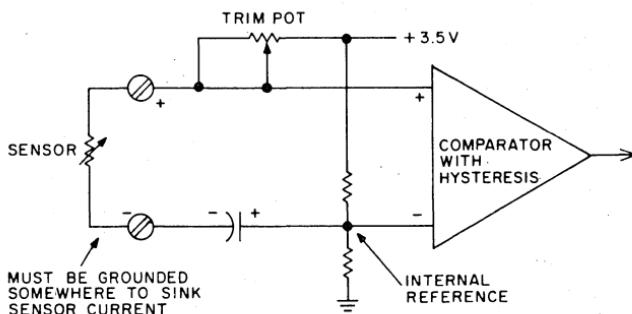
K 522 APPLICATIONS



K522 WITH NEARBY SENSOR

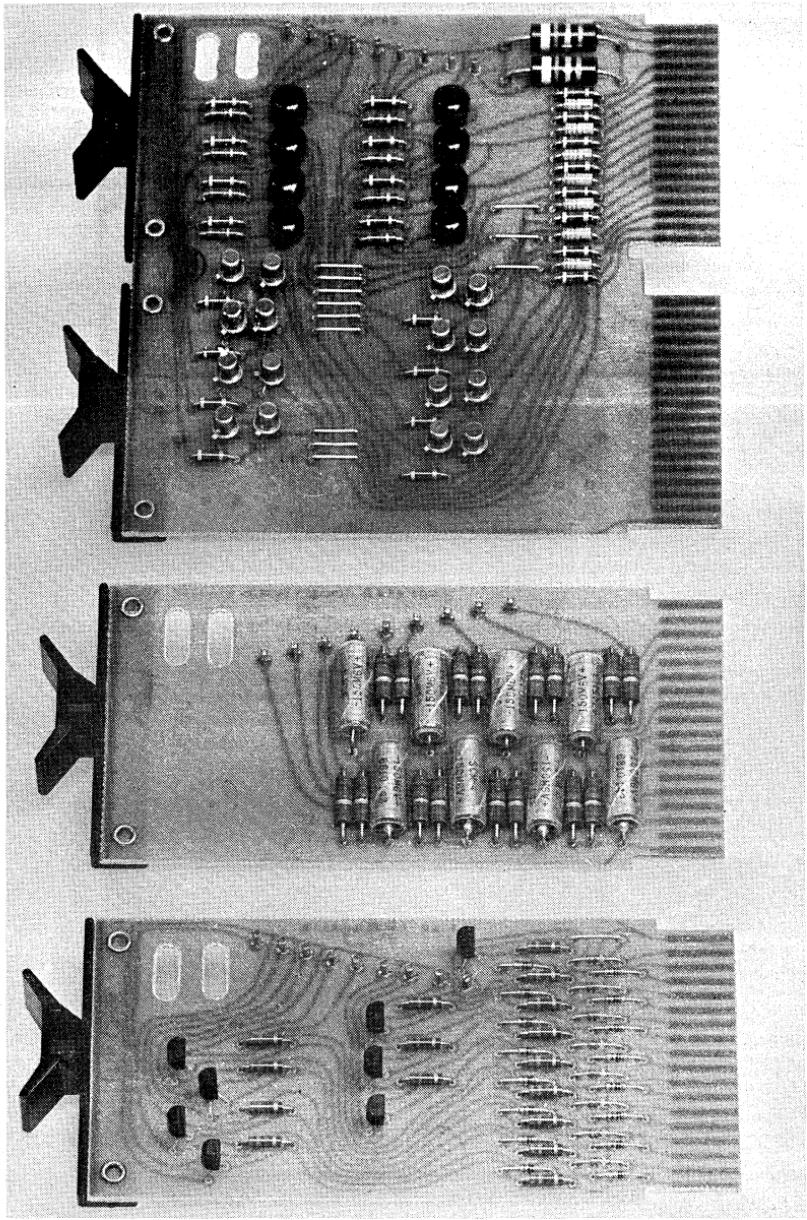
The diagram above shows how a sensor located a few feet from a K522 can be connected by a simple twisted pair of wires if the environmental noise is not too severe. Differences in potential between logic ground and chassis ground at the sensor are not likely to exceed ± 1 volt in such a case, so the noise cancellation ability of the K522 circuit would be adequate to maintain a consistent threshold. Since the built-in reference in the K522 is half the voltage on the trimpot, and the switching threshold is half the voltage on the trimpot; the switching threshold will be near the point where the sensor and trimming resistances are equal, if 3.5v is used for bias.

If the sensor is ungrounded, a ground return must be provided at the module by tying pin T and/or pin V to ground. The simplified equivalent circuit below shows the AC coupling capacitor which makes this necessary.



K522 EQUIVALENT CIRCUIT

The K522 can also be used with a self-generating sensor such as a tachometer pickup, just as the K524 can.

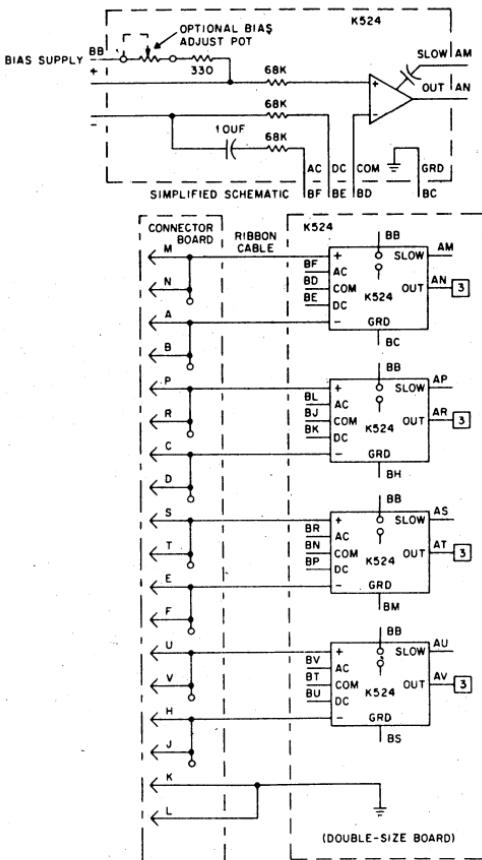


OTHER MODULES HAVING SOLDER LUGS AND STRAIN RELIEF HOLES
LIKE THE K522. SHOWN ARE K681, K580, AND K683.

SENSOR CONVERTER

K524

**K
SERIES**



Basically a noise-rejecting, threshold sensing differential voltage amplifier the K524 is readily adapted to sensing threshold points in DC analog signals, AC signals, and pulses. It can also be biased to sense resistance thresholds. The differential amplifying technique permits flexible grounding and shielding methods to accommodate floating signal generators and minimize noise.

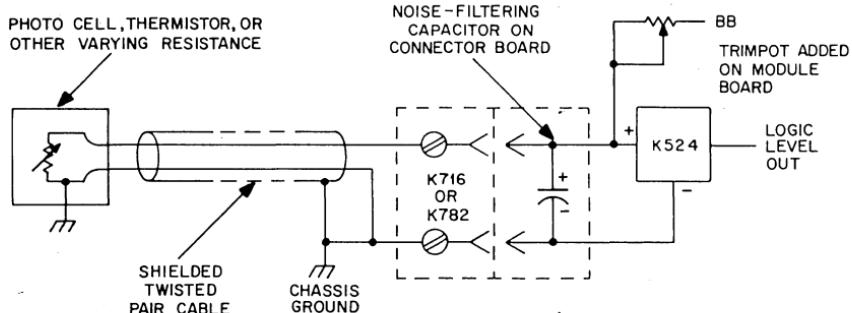
The K524 Sensor Converter senses voltage transitions or resistance thresholds by noise-rejecting differential amplification. A choice of AC or DC coupling is provided.

Output transitions occur when input voltage differentials are within 0.3 volts or less. When the "+" input is more positive, the output is a ONE. When the "+" input is more negative, the output is a ZERO.

K524 — \$98

K524 APPLICATIONS

Below is shown a K524 circuit used in the same application as the K522 above, but where longer sensor leads and hence more noise is expected.

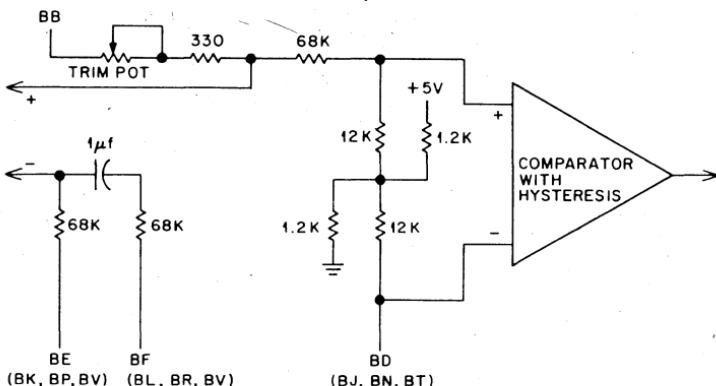


K524 WITH DISTANT SENSOR

Switching occurs at equality between sensor and biasing resistance when +5 volts is used for bias. Pin BB (pin B on lower connector) must be connected to an independent bias supply, such as a separate K731 operated from a separate transformer, to insure against damaging currents through the bias circuits to the logic in case of accidental high voltages at K524 inputs. This precaution is most essential in systems containing K604 or K644 output converters, since inadvertent use of the wrong K716 socket is possible. This problem does not arise with self-generating sensors or where bias is supplied externally to variable-resistance sensors.

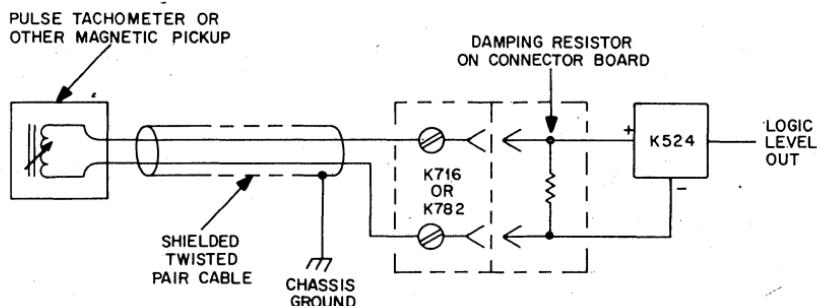
Since low-frequency noise injected by the chassis ground connection goes directly to the - input but is attenuated by the bias network at the + input, some loss of noise rejection will result. One way to restore full rejection would be to return the bias supply itself to the same noise source. If a K731 is used, this means both its transformer winding centertap and its pin C connections must be connected to ground only at the point where the cable is grounded.

Because of the more complex input network in the K524, allowing true DC differential operation if desired, one additional connection is required. The simplified schematic below shows that the inverting input to the internal comparator must be connected either to the DC-coupled or to the AC-coupled input attenuator via the module connector pins.



K524 EQUIVALENT CIRCUIT

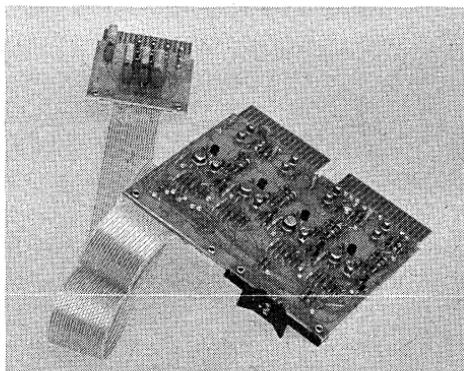
Below is shown another way to use the K524, this time with a self-generating transducer.



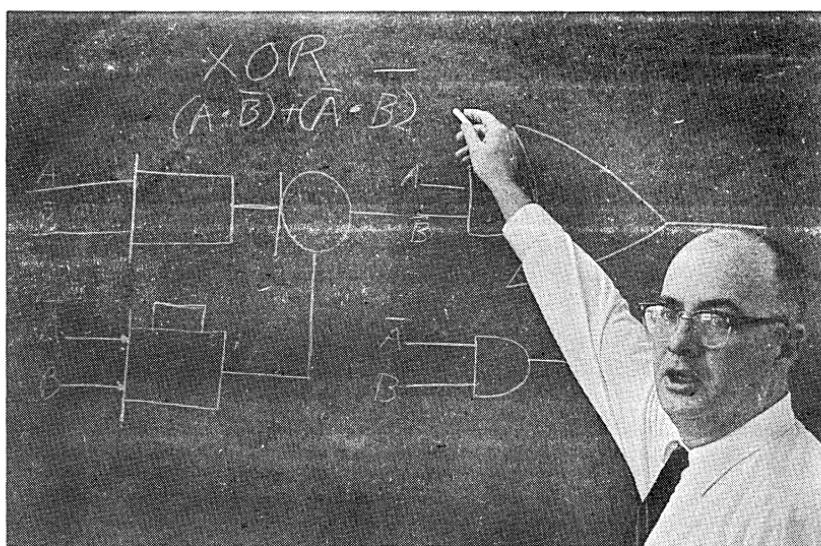
Here is a table showing the auxiliary pin connections on the lower module connector for the various applications of the K524.

APPLICATIONS	COUPLING	PIN CONNECTIONS
As low performance analog comparator, for comparing two photocells etc., or wherever reference is supplied externally.	DC (K524 only)	BD to BE, BJ to BK, BN to BP, BT to BV
Photocells, thermistors, pulse tachometers, pressure transducers or wherever it is convenient to use the internal 2.5 volt reference.	AC (see also K522)	BD to BF, BJ to BL, BN to BR, BT to BV

Signals up to 25 KHz, suitable for counting by K210 or K220 counters, can be obtained with symmetrical input signals having at least 1 volt excursions past the switching point. Maximum output rates can be limited to approximately 5KHz by tying together pins AM and AN, AP and AR, etc.



K524 SENSOR CONVERTER

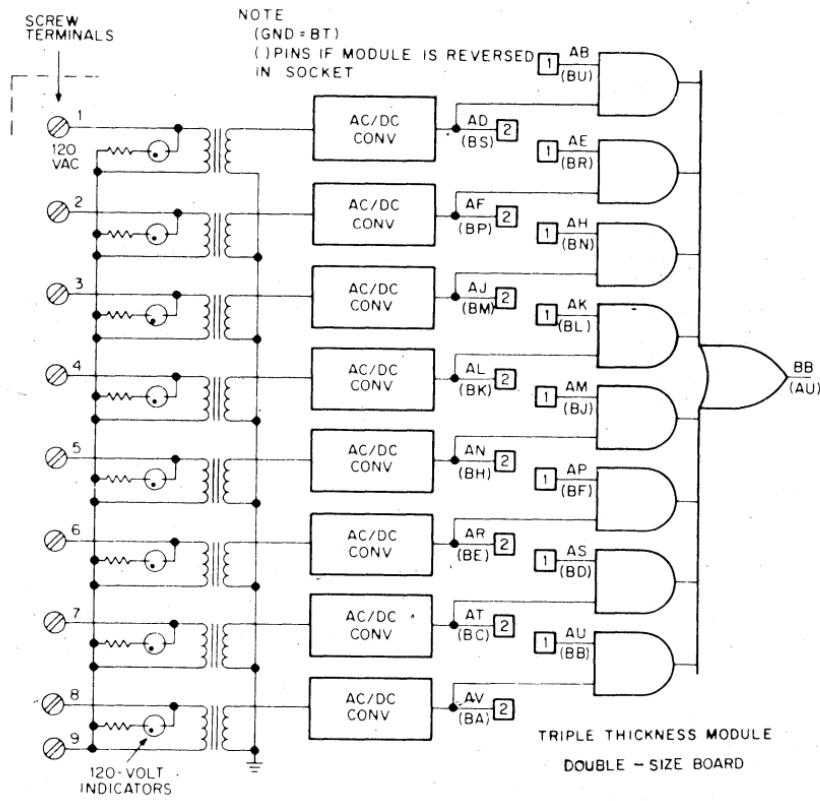


DEC provides a series of seminars to educate its customers on DEC's module products. Here, William G. McNamara, Module Marketing Manager, is explaining digital logic.

120 VAC INPUT CONVERTER

K578

**K
SERIES**



K578 AC INPUT CONVERTER

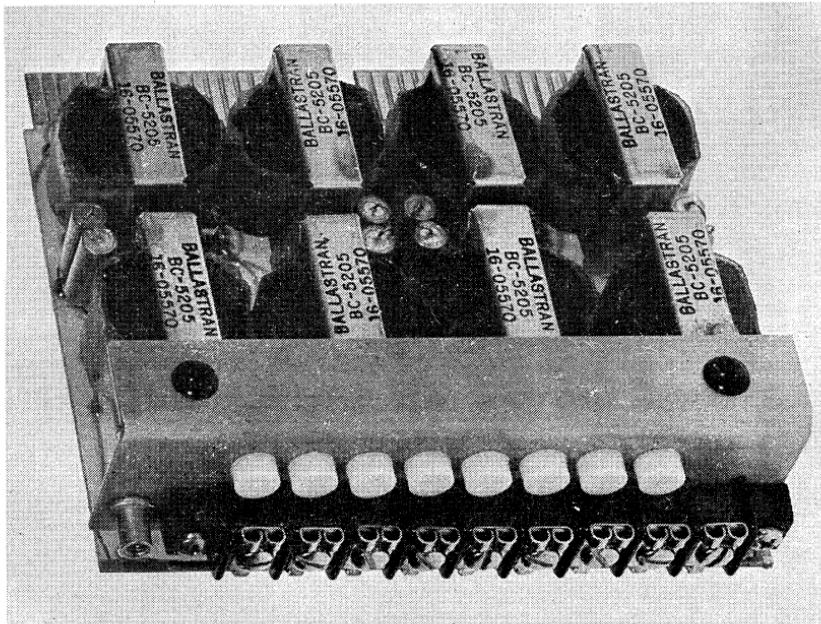
K578 — \$80

The K578 input converter, when mounted in a K724 or K725 interface shell, provides logic levels from 120 VAC signals from limit switches, relays etc. The 1VA reactive load provided by the K578 isolation transformers insures sparking at pilot contacts. Together with the ample circuit voltage used, this reactive load assures maximum contact reliability.

Electrical noise riding on pilot circuit wiring is attenuated both by the input transformer and by RC filtering. Bounce filtering is designed to pick up by the end of the first full cycle of contact, and to drop out (return to "zero" output state) by the end of three full cycles after the input is removed. (About 50 milliseconds.) This speed of response is desirable in large sequential scanning-type control systems, even though occasionally a heavy contact may be observed to produce more than one output transition due to very long bounce duration. If necessary, response speed may be cut in half by tying 150 mfd from the offending logic output to ground. However since no Schmitt triggers are included in the K578 (unlike the K508), a K184 or K501 must be used as described in the applications notes if it is important to know exactly how many contact closures have occurred in a given period.

Gating circuits equivalent to four K026 sections are included for contact scanning applications using the K161, or to facilitate forming the logical OR of many inputs. Direct outputs are from circuits similar to the K580, and may not be wired together.

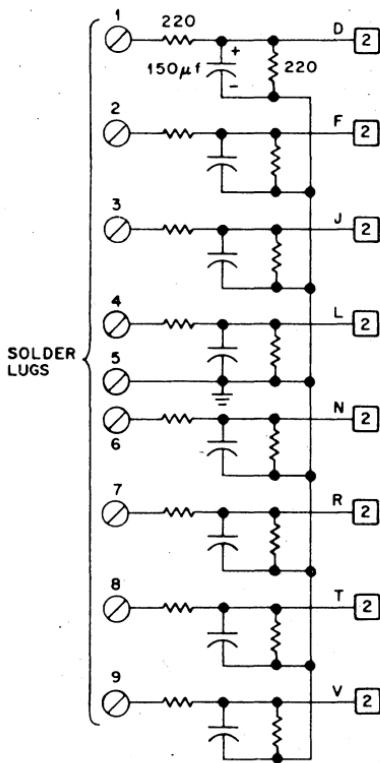
Clamp-type terminals on the K578 take two wires up to size 14. Neon indicators are included. The K578 can also be used in the K943 mounting panel, however some mechanical means of support must be provided to hold the K578 in its socket if vibration is a consideration.



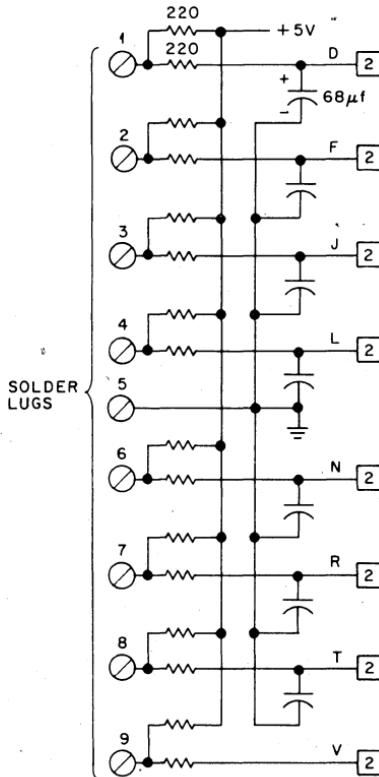
K578 TERMINAL STRIP CONNECTIONS FROM
LEFT TO RIGHT ARE NUMBERS 1 TO 9

DRY CONTACT FILTERS
K580, K581

**K
SERIES**



K580



K581

K580 — \$20
K581 — \$20

These filters convert signals from dry circuit or wiping contacts to logic levels. Primarily they are used with gold contacts such as the new encapsulated reed limit switches, thumbwheel switches, and the like. Those push-buttons or slide switches that provide good wiping action will also operate reliably with these filters, but silver contacts designed for long life on heavy duty loads are likely to give trouble. For them, use interfaces designed for such application like K508-K716 or K578, or at least switch a high voltage. (see K580 voltage table.)

Access to K580 and K581 inputs is by solder lugs only. Strain relief holes are provided in board (near handle) for a 9-wire cable. The avoidance of contact connections on the logic wiring panel combined with heavy filtering guarantees noise isolation and protects modules by preventing accidental short circuits. Below is a summary of other characteristics.

	Contact Current	Contact Voltage	Output for Contact Closed	Time Delay on Closure	Time Delay on Opening
K580	22ma	See Table	high	10msec	30msec
K581	22ma	5V	low	20msec	20msec

(Time delay figures above are nominal, and assume connection to the input of a standard gate such as K113 or K123.)

The contact current for the K581 comes from the logic supply, making it very important to assure freedom from accidental high voltages on K581 inputs, which could damage many logic modules by getting through to the system power supply. This hazard is not present with the K580, which uses an external source of +10 volts or more. The table below shows how external dropping resistors may be added to provide higher voltage operation.

TABLE OF K580 VOLTAGE DROPPING RESISTANCES

CONTACT SUPPLY VOLTAGE	10	12	15	24	28	48	90	100	120
Dropping Resistance	0	82Ω	220Ω	620Ω	820Ω	1.8KΩ	3.6KΩ	3.9KΩ	4.7KΩ
Dissipation	—	0.05W	0.11W	0.3W	0.4W	0.85W	1.8W	2.0W	2.5W

When using dropping resistors and higher voltage supplies, total tolerance of resistors and supply should be $\pm 10\%$ to insure high levels between +4V and +6V at the logic. Also observe that a handful of dropping resistors in 90V or 120V systems may dissipate more power than the entire logic system, and must be located so as not to cause excessive temperature rise in the K series environment.

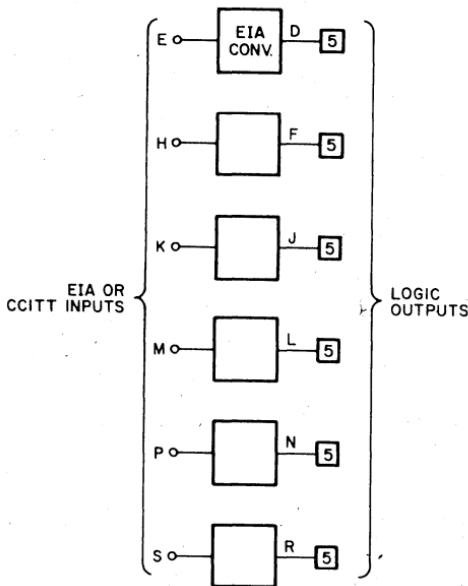
Note that these circuits may not be paralleled to obtain the wired OR or wired AND function, and that fanout is limited to 2 milliamperes in order to maintain the low (zero) output voltage within normal K-Series specifications. Fanout to ordinary logic gates and diode expanders may be raised to 4 milliamperes if some noise and contact bounce rejection can be traded off; but hysteresis inputs such as those at counter inputs, rate multiplier, etc., may not switch properly if the logic zero is allowed to rise much above +0.5V.

See application note for thumbwheel register multiplexing using K581.

EIA INPUT CONVERTER

K596

**K
SERIES**



Any bipolar input signals with amplitudes between ± 3 volts and ± 25 volts will be transformed by this non-inverting converter into standard K-Series or M-Series logic signals with driving capabilities of 5 ma or 3 unit loads, respectively. Load for paralleling (wired OR): 1 milliamperere. Input impedance stays between $3K\Omega$ and $6K\Omega$ for full capability with both the American EIA and the European CCITT standards for data transmission. Built-in noise filtering causes transition delays of several microseconds, limiting the maximum baud rate that can be handled.

Open-circuit inputs will produce low (zero-volts) outputs on the lower three circuits. The output stage of the first three circuits if inputs are open is controlled by pin B, which must be grounded for outputs low or connected to pin A (+ 5 volts) for outputs high. This last provision allows type 33 or type 35 current switching teletypes to be converted and wired ORed with modem interfaces. Pin B must be connected either to pin A or pin C: if it is left open, there may be crosstalk between circuits.

Please observe that noise and interference can enter a digital system through any wires that pass through a noise field. K596 modules should be located at the edge of the system, and communications wiring should not be allowed to lie close to logic wiring for more than a few inches.

K596 — \$16