

Chapter Outline

- 11-1 CC Amplifier
- 11-2 Output Impedance
- 11-3 Cascading CE and CC
- 11-4 Darlington Connections
- 11-5 Voltage Regulation
- 11-6 Common-Base Amplifier

Objectives

After studying this chapter, you should be able to:

- Draw a diagram of an emitter follower and describe its advantages.
- Analyze an emitter follower for dc and ac operation.
- Describe the purpose of cascading CE and CC amplifiers.
- State the advantages of a Darlington transistor.
- Draw a schematic for a zener follower and discuss how it increases the load current out of a zener regulator.
- Analyze a common-base amplifier for dc and ac operation.
- Compare the characteristics of CE, CC, and CB amplifiers.

Vocabulary

buffer	complementary Darlington	direct coupled
common-base (CB) amplifier	Darlington connection	emitter follower
common-collector (CC) amplifier	Darlington pair	zener follower

11-1 CC Amplifier

The emitter follower is also called a common-collector (CC) amplifier. The input signal is coupled to the base, and the output signal is taken from the emitter.

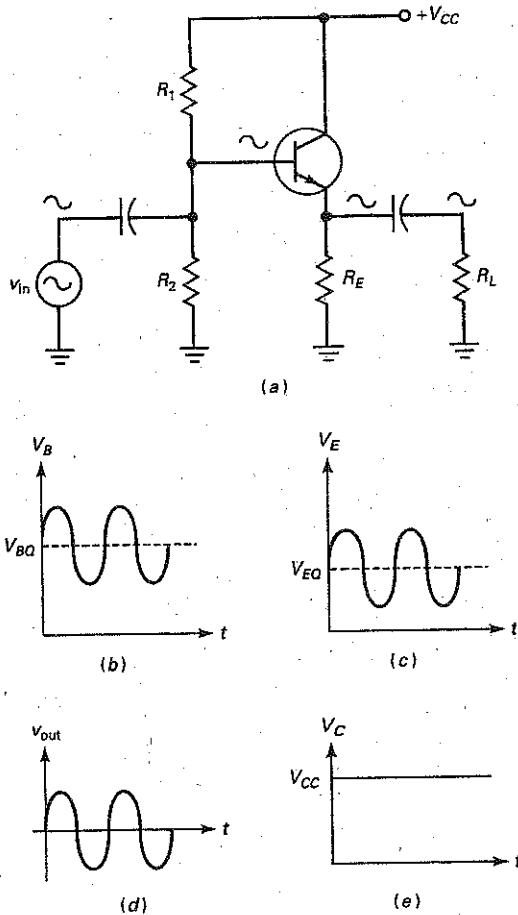
Basic Idea

Figure 11-1a shows an emitter follower. Because the collector is at ac ground, the circuit is a CC amplifier. The input voltage is coupled to the base. This sets up an ac emitter current and produces an ac voltage across the emitter resistor. This ac voltage is then coupled to the load resistor.

Figure 11-1b shows the total voltage between the base and ground. It has a dc component and an ac component. As you can see, the ac input voltage rides on the quiescent base voltage V_{BQ} . Similarly, Fig. 11-1c shows the total voltage between the emitter and ground. This time, the ac input voltage is centered on a quiescent emitter voltage V_{EQ} .

The ac emitter voltage is coupled to the load resistor. This output voltage is shown in Fig. 11-1d, a pure ac voltage. This output voltage is in phase and is

Figure 11-1 Emitter follower and waveforms.



GOOD TO KNOW

In some emitter-follower circuits, a small collector resistance is used to limit the dc collector current in the transistor in case a short occurs between the emitter and ground. If a small R_C is used, the collector will have a bypass capacitor going to ground. The small value of R_C will have only a slight bearing on the dc operation of the circuit and no bearing at all on the circuit's ac operation.

approximately equal to the input voltage. The reason the circuit is called an *emitter follower* is because the output voltage follows the input voltage.

Since there is no collector resistor, the total voltage between the collector and ground equals the supply voltage. If you look at the collector voltage with an oscilloscope, you will see a constant dc voltage like Fig. 11-1e. There is no ac signal on the collector because it is an ac ground point.

Negative Feedback

Like a swamped amplifier, the emitter follower uses negative feedback. But with the emitter follower, the negative feedback is massive because the feedback resistance equals all of the emitter resistance. As a result, the voltage gain is ultrastable, the distortion is almost nonexistent, and the input impedance of the base is very high. The trade-off is the voltage gain, which has a maximum value of 1.

AC Emitter Resistance

In Fig. 11-1a, the ac signal coming out of the emitter sees R_E in parallel with R_L . Let us define the ac emitter resistance as follows:

$$r_e = R_E \parallel R_L \quad (11-1)$$

This is the external ac emitter resistance, which is different from the internal ac emitter resistance r'_e .

Voltage Gain

Figure 11-2a shows the ac equivalent with the T model. Using Ohm's law, we can write these two equations:

$$v_{out} = i_e r_e$$

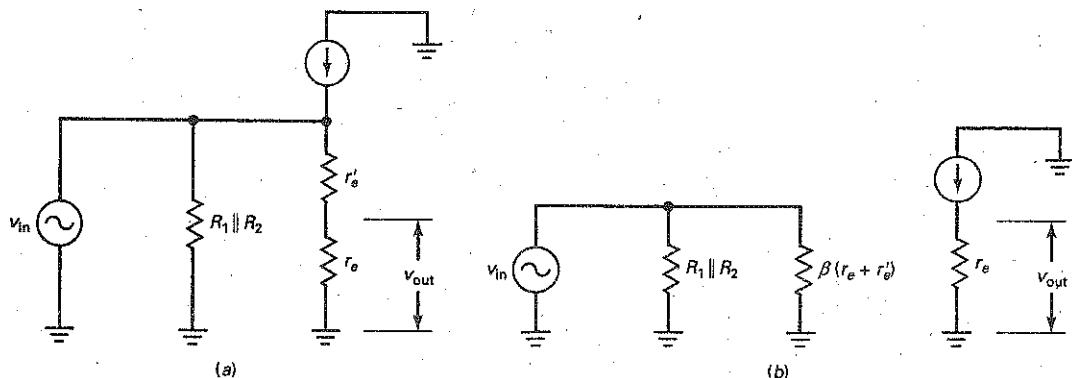
$$v_{in} = i_e (r_e + r'_e)$$

Divide the first equation by the second, and you get the voltage gain of the emitter follower:

$$A_V = \frac{r_e}{r_e + r'_e} \quad (11-2)$$

Usually, a designer makes r_e much greater than r'_e , so that the voltage gain equals 1 (approximately). This is the value to use for all preliminary analysis and troubleshooting.

Figure 11-2 AC equivalent circuits for emitter follower.



Why is an emitter follower called an *amplifier* if its voltage gain is only 1? Because it has a current gain of β . The stages near the end of a system need to produce more current because the final load is usually a low impedance. The emitter follower can produce the large output currents needed by low-impedance loads. In short, although it is not a voltage amplifier, the emitter follower is a current or power amplifier.

Input Impedance of the Base

Figure 11-2b shows the ac equivalent circuit with the π model of the transistor. As far as the input impedance of the base is concerned, the action is the same as that of a swamped amplifier. The current gain transforms the total emitter resistance up by a factor of β . The derivation is therefore identical to that of a swamped amplifier:

$$z_{in(base)} = \beta(r_e + r'_e) \quad (11-3)$$

For troubleshooting, you can assume that r_e is much greater than r'_e , which means that the input impedance is approximately βr_e .

The step-up in impedance is the major advantage of an emitter follower. Small load resistances that would overload a CE amplifier can be used with an emitter follower because it steps up the impedance and prevents overloading.

GOOD TO KNOW

In Fig. 11-3, the biasing resistors R_1 and R_2 lower z_{in} to a value that is not much different from that of a swamped CE amplifier. This disadvantage is overcome in most emitter follower designs by simply not using the biasing resistors R_1 and R_2 . Instead, the emitter follower is dc-biased by the stage driving the emitter follower.

Input Impedance of the Stage

When the ac source is not stiff, some of the ac signal will be lost across the internal resistance. If you want to calculate the effect of the internal resistance, you will need to use the input impedance of the stage, given by:

$$z_{in(stage)} = R_1 \parallel R_2 \parallel \beta(r_e + r'_e) \quad (11-4)$$

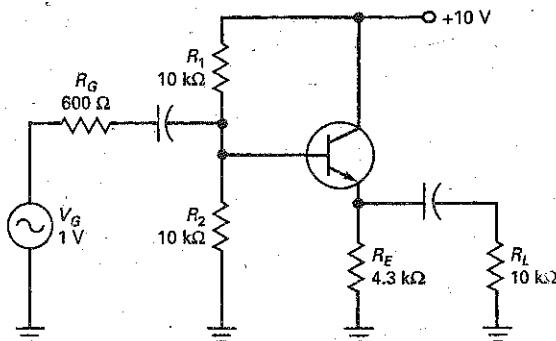
With the input impedance and the source resistance, you can use the voltage divider to calculate the input voltage reaching the base. The calculations are the same as shown in earlier chapters.

Example 11-1

Multisim

What is the input impedance of the base in Fig. 11-3 if $\beta = 200$? What is the input impedance of the stage?

Figure 11-3 Example.



SOLUTION Because each resistance in the voltage divider is $10\text{ k}\Omega$, the dc base voltage is half the supply voltage, or 5 V. The dc emitter voltage is 0.7 V less, or 4.3 V. The dc emitter voltage is 4.3 V divided by $4.3\text{ k}\Omega$, or 1 mA. Therefore, the ac resistance of the emitter diode is:

$$r'_e = \frac{25\text{ mV}}{1\text{ mA}} = 25\text{ }\Omega$$

The external ac emitter resistance is the parallel equivalent of R_E and R_L , which is:

$$r_e = 4.3\text{ k}\Omega \parallel 10\text{ k}\Omega = 3\text{ k}\Omega$$

Since the transistor has an ac current gain of 200, the input impedance of the base is:

$$z_{in(base)} = 200(3\text{ k}\Omega + 25\text{ }\Omega) = 605\text{ k}\Omega$$

The input impedance of the base appears in parallel with the two biasing resistors. The input impedance of the stage is:

$$z_{in(stage)} = 10\text{ k}\Omega \parallel 10\text{ k}\Omega \parallel 605\text{ k}\Omega = 4.96\text{ k}\Omega$$

Because the $605\text{ k}\Omega$ is much larger than $5\text{ k}\Omega$, troubleshooters usually approximate the input impedance of the stage as the parallel of the biasing resistors only:

$$z_{in(stage)} = 10\text{ k}\Omega \parallel 10\text{ k}\Omega = 5\text{ k}\Omega$$

PRACTICE PROBLEM 11-1 Find the input impedance of the base and the stage, using Fig. 11-3, if β changes to 100.

Example 11-2

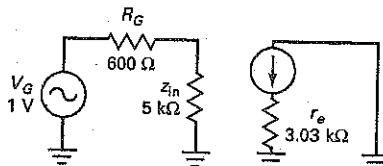
III Multisim

Assuming a β of 200, what is the ac input voltage to the emitter follower of Fig. 11-3?

SOLUTION Figure 11-4 shows the ac equivalent circuit. The ac base voltage appears across z_{in} . Because the input impedance of the stage is large compared to the generator resistance, most of the generator voltage appears at the base. With the voltage-divider theorem:

$$v_{in} = \frac{5\text{ k}\Omega}{5\text{ k}\Omega + 600\text{ }\Omega} 1\text{ V} = 0.893\text{ V}$$

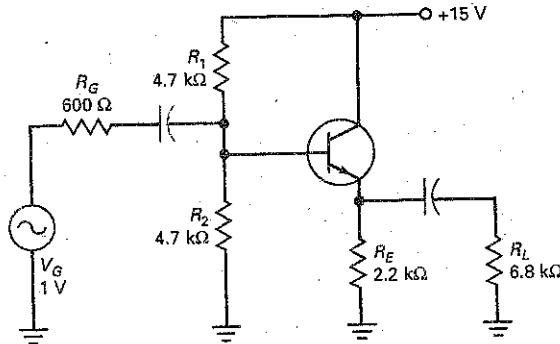
Figure 11-4 Example.



PRACTICE PROBLEM 11-2 If the β value is 100, find the ac input voltage of Fig. 11-3.

Example 11-3

What is the voltage gain of the emitter follower in Fig. 11-5? If $\beta = 150$, what is the ac load voltage?

Figure 11-5 Example.

SOLUTION The dc base voltage is half the supply voltage:

$$V_B = 7.5 \text{ V}$$

The dc emitter current is:

$$I_E = \frac{6.8 \text{ V}}{2.2 \text{ k}\Omega} = 3.09 \text{ mA}$$

and the ac resistance of the emitter diode is:

$$r'_e = \frac{25 \text{ mV}}{3.09 \text{ mA}} = 8.09 \Omega$$

The external ac emitter resistance is:

$$r_e = 2.2 \text{ k}\Omega \parallel 6.8 \text{ k}\Omega = 1.66 \text{ k}\Omega$$

The voltage gain equals:

$$A_v = \frac{1.66 \text{ k}\Omega}{1.66 \text{ k}\Omega + 8.09 \Omega} = 0.995$$

The input impedance of the base is:

$$Z_{\text{in(base)}} = 150(1.66 \text{ k}\Omega + 8.09 \Omega) = 250 \text{ k}\Omega$$

This is much larger than the biasing resistors. Therefore, to a close approximation, the input impedance of the emitter follower is:

$$Z_{\text{in(stage)}} = 4.7 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega = 2.35 \text{ k}\Omega$$

The ac input voltage is:

$$v_{\text{in}} = \frac{2.35 \text{ k}\Omega}{600 \Omega + 2.35 \text{ k}\Omega} 1 \text{ V} = 0.797 \text{ V}$$

The ac output voltage is:

$$v_{\text{out}} = 0.995(0.797 \text{ V}) = 0.793 \text{ V}$$

PRACTICE PROBLEM 11-3 Repeat Example 11-3 using an R_G value of 50 Ω.

11-2 Output Impedance

The output impedance of an amplifier is the same as its Thevenin impedance. One of the advantages of an emitter follower is its low output impedance.

As discussed in earlier electronics courses, maximum power transfer occurs when the load impedance is *matched* (made equal) to the source (Thevenin) impedance. Sometimes, when maximum load power is wanted, a designer can match the load impedance to the output impedance of an emitter follower. For instance, the low impedance of a speaker can be matched to the output impedance of an emitter follower to deliver maximum power to the speaker.

Basic Idea

Figure 11-6a shows an ac generator driving an amplifier. If the source is not stiff, some of the ac voltage is dropped across the internal resistance R_G . In this case, we need to analyze the voltage divider shown in Fig. 11-6b to get the input voltage v_{in} .

A similar idea can be used with the output side of the amplifier. In Fig. 11-6c, we can apply the Thevenin theorem at the load terminals. Looking back into the amplifier, we see an output impedance z_{out} . In the Thevenin equivalent circuit, this output impedance forms a voltage divider with the load resistance, as shown in Fig. 11-6d. If z_{out} is much smaller than R_L , the output source is stiff and v_{out} equals v_{th} .

CE Amplifiers

Figure 11-7a shows the ac equivalent circuit for the output side of a CE amplifier. When we apply Thevenin's theorem, we get Fig. 11-7b. In other words, the output

Figure 11-6 Input and output impedances.

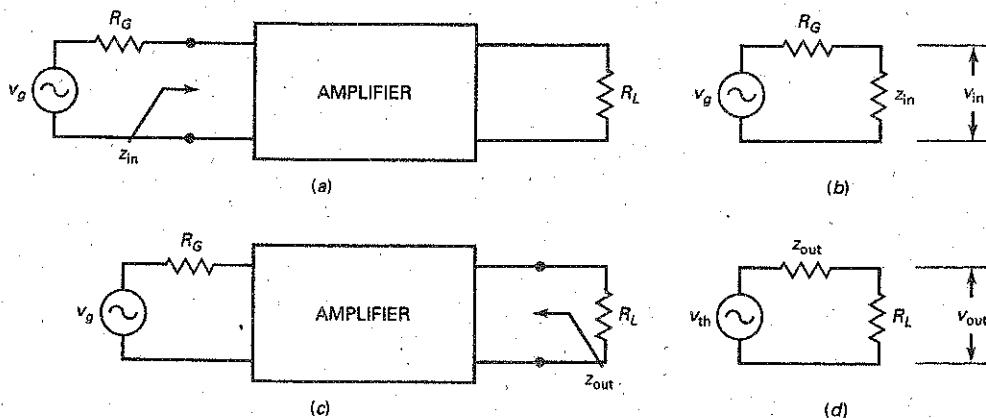


Figure 11-7 Output impedance of CE stage.

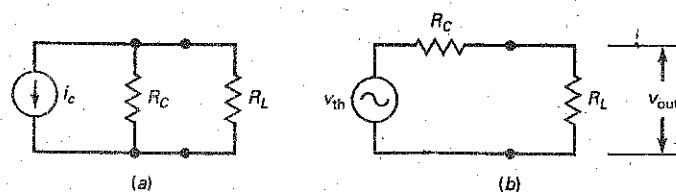
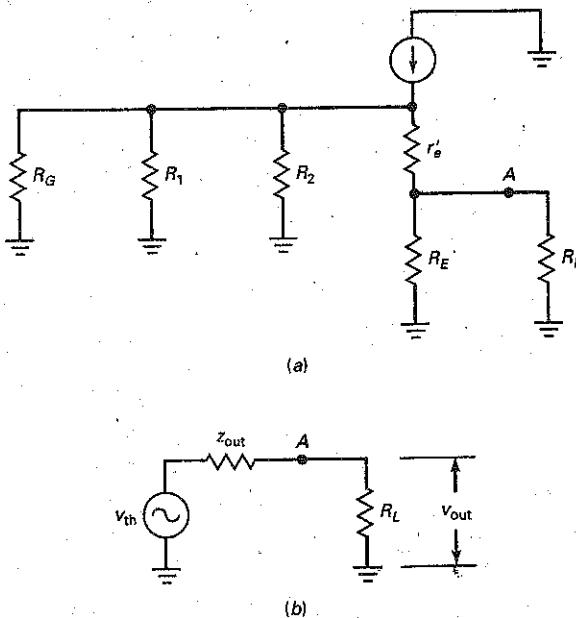


Figure 11-8 Output impedance of emitter follower.



impedance facing the load resistance is R_C . Since the voltage gain of a CE amplifier depends on R_C , a designer cannot make R_C too small without losing voltage gain. Stated another way, it is very difficult to get a small output impedance with a CE amplifier. Because of this, CE amplifiers are not suited to driving small load resistances.

Emitter Follower

Figure 11-8a shows the ac equivalent circuit for an emitter follower. When we apply Thevenin's theorem to point A, we get Fig. 11-8b. The output impedance z_{out} is much smaller than you can get with a CE amplifier. It equals:

$$z_{out} = R_E \parallel \left(r'_e + \frac{R_G \parallel R_1 \parallel R_2}{\beta} \right) \quad (11-5)$$

The impedance of the base circuit is $R_G \parallel R_1 \parallel R_2$. The current gain of the transistor steps this impedance down by a factor of β . The effect is similar to what we get with a swamped amplifier, except that we are moving from the base back to the emitter. Therefore, we get a reduction of impedance rather than an increase. The stepped-down impedance of $(R_G \parallel R_1 \parallel R_2)/\beta$ is in series with r'_e as indicated by Eq. (11-5).

Ideal Action

In some designs the biasing resistances and the ac resistance of the emitter diode become negligible. In this case, the output impedance of an emitter follower can be approximated by:

$$z_{out} = \frac{R_G}{\beta} \quad (11-6)$$

This brings out the key idea of an emitter follower: It steps the impedance of the ac source down by a factor of β . As a result, the emitter follower allows us to build stiff

GOOD TO KNOW

Transformers can also be used to match impedances between source and load. Looking into the transformer,

$$Z_{in} = \left(\frac{N_p}{N_s} \right)^2 R_L$$

ac sources. Instead of using a stiff ac source that maximizes the load voltage, a designer may prefer to maximize the load power. In this case, instead of designing for:

$$z_{\text{out}} \ll R_L \quad (\text{Stiff voltage source})$$

the designer will select values to get:

$$z_{\text{out}} = R_L \quad (\text{Maximum power transfer})$$

In this way, the emitter follower can deliver maximum power to a low-impedance load such as a stereo speaker. By basically removing the effect of R_L on the output voltage, the circuit is acting as a buffer between the input and output.

Equation (11-6) is an ideal formula. You can use it to get an approximate value for the output impedance of an emitter follower. With discrete circuits, the equation usually gives only an estimate of the output impedance. Nevertheless, it is adequate for troubleshooting and preliminary analysis. When necessary, you can use Eq. (11-5) to get an accurate value for the output impedance.

Example 11-4

Estimate the output impedance of the emitter follower of Fig. 11-9a.

SOLUTION Ideally, the output impedance equals the generator resistance divided by the current gain of the transistor:

$$z_{\text{out}} = \frac{600 \Omega}{300} = 2 \Omega$$

Figure 11-9b shows the equivalent output circuit. The output impedance is much smaller than the load resistance, so that most of the signal appears across the load resistor. As you can see, the output source of Fig. 11-9b is almost stiff because the ratio of load to source resistance is 50.

PRACTICE PROBLEM 11-4 Using Fig. 11-9, change the source resistance to $1 \text{ k}\Omega$ and solve for the approximate z_{out} value.

Example 11-5

Calculate the output impedance in Fig. 11-9a using Eq. (11-5).

SOLUTION The quiescent base voltage is approximately:

$$V_{BQ} = 15 \text{ V}$$

Ignoring V_{BE} , the quiescent emitter current is approximately:

$$I_{EQ} = \frac{15 \text{ V}}{100 \Omega} = 150 \text{ mA}$$

The ac resistance of the emitter diode is:

$$r'_e = \frac{25 \text{ mV}}{150 \text{ mA}} = 0.167 \Omega$$

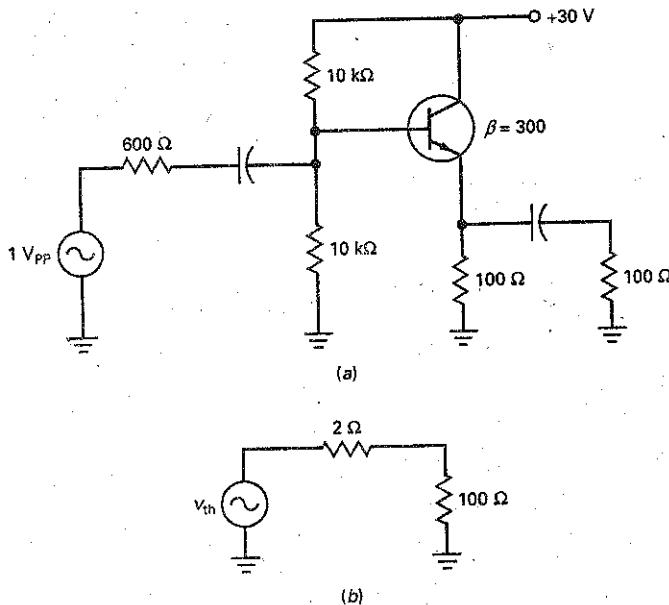
The impedance seen looking back from the base is:

$$R_G \parallel R_1 \parallel R_2 = 600 \Omega \parallel 10 \text{ k}\Omega \parallel 10 \text{ k}\Omega = 536 \Omega$$

The current gain steps this down to:

$$\frac{R_G \parallel R_1 \parallel R_2}{\beta} = \frac{536 \Omega}{300} = 1.78 \Omega$$

Figure 11-9 Example.



This is in series with r'_e , so that the impedance looking back into the emitter is:

$$r'_e + \frac{R_G \parallel R_1 \parallel R_2}{\beta} = 0.167 \Omega + 1.78 \Omega = 1.95 \Omega$$

This is in parallel with the dc emitter resistance, so that the output impedance is:

$$z_{out} = R_E \parallel \left(r'_e + \frac{R_G \parallel R_1 \parallel R_2}{\beta} \right) = 100 \Omega \parallel 1.95 \Omega = 1.91 \Omega$$

This accurate answer is extremely close to the ideal answer of 2Ω . This result is typical of many designs. For all troubleshooting and preliminary analysis, you can use the ideal method to estimate the output impedance.

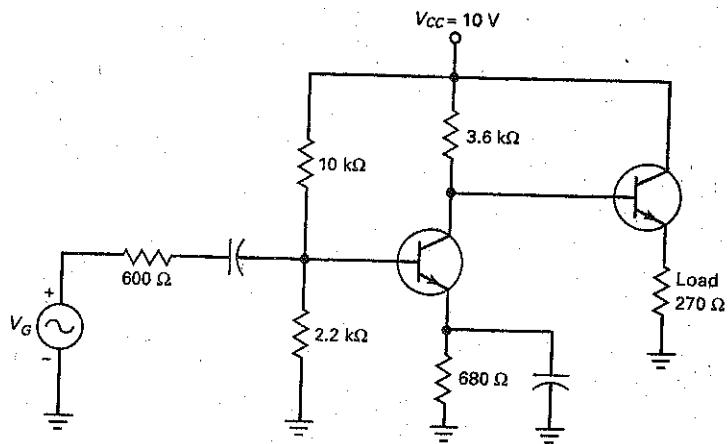
PRACTICE PROBLEM 11-5 Repeat Example 11-5 using an R_G value of $1 \text{ k}\Omega$.

11-3 Cascading CE and CC

To illustrate the buffering action of a CC amplifier, suppose we have a load resistance of 270Ω . If we try to couple the output of a CE amplifier directly into this load resistance, we may overload the amplifier. One way to avoid this overload is by using an emitter follower between the CE amplifier and the load resistance. The signal can be coupled capacitively (this means through coupling capacitors), or it may be direct coupled as shown in Fig. 11-10.

As you can see, the base of the second transistor is connected directly to the collector of the first transistor. Because of this, the dc collector voltage of the first transistor is used to bias the second transistor. If the dc current gain of the second transistor is 100, the dc resistance looking into the base of the second transistor is $R_{in} = 100 (270 \Omega) = 27 \text{ k}\Omega$.

Figure 11-10 Direct coupled output stage.



Because $27\text{ k}\Omega$ is large compared to the $3.6\text{ k}\Omega$, the dc collector voltage of the first stage is only slightly disturbed.

In Fig. 11-10, the amplified voltage out of the first stage drives the emitter follower and appears across the final load resistance of $270\text{ }\Omega$. Without the emitter follower, the $270\text{ }\Omega$ would overload the first stage. But with the emitter follower, its impedance effect is increased by a factor of β . Instead of appearing like $270\text{ }\Omega$, it now looks like $27\text{ k}\Omega$ in both the dc and the ac equivalent circuits.

This demonstrates how an emitter follower can act as a **buffer** between a high-output impedance and a low-resistance load.

Example 11-6

III Multisim

What is the voltage gain of the CE stage in Fig. 11-10 for a β of 100?

SOLUTION The dc base voltage of the CE stage is 1.8 V and the dc emitter voltage is 1.1 V. The dc emitter current is $I_E = \frac{1.1\text{ V}}{680\text{ }\Omega} = 1.61\text{ mA}$ and the ac resistance of the emitter diode is $r'_e = \frac{25\text{ mV}}{1.61\text{ mA}} = 15.5\text{ }\Omega$. Next, we need to calculate the input impedance of the emitter follower. Since there are no biasing resistors, the input impedance equals the input impedance looking into the base: $z_{in} = (100)(270\text{ }\Omega) = 27\text{ k}\Omega$. The ac collector resistance of the CE amplifier is $r_c = 3.6\text{ k}\Omega \parallel 27\text{ k}\Omega = 3.18\text{ k}\Omega$ and the voltage gain of this stage is $A_v = \frac{3.18\text{ k}\Omega}{15.5\text{ }\Omega} = 205$

PRACTICE PROBLEM 11-6 Using Fig. 11-10, find the voltage gain of the CE stage for a β of 300.

Example 11-7

III Multisim

Suppose the emitter follower is removed in Fig. 11-10 and a capacitor is used to couple the ac signal to the $270\text{ }\Omega$ load resistor. What happens to the voltage gain of the CE amplifier?

SOLUTION The value of r'_e remains the same for the CE stage: 15.5Ω . But the ac collector resistance is much lower. To begin with, the ac collector resistance is the parallel resistance of $3.6 \text{ k}\Omega$ and 270Ω : $r_c = 3.6 \text{ k}\Omega \parallel 270 \Omega = 251 \Omega$. Because this is much lower, the voltage gain decreases to $A_v = \frac{251 \Omega}{15.5 \Omega} = 16.2$.

PRACTICE PROBLEM 11-7 Repeat Example 11-7 using a load resistance of 100Ω .

This shows you the effects of overloading a CE amplifier. The load resistance should be much greater than the dc collector resistance to get maximum voltage gain. We have just the opposite; the load resistance (270Ω) is much smaller than the dc collector resistance ($3.6 \text{ k}\Omega$).

11-4 Darlington Connections

A **Darlington connection** is a connection of two transistors whose overall current gain equals the product of the individual current gains. Since its current gain is much higher, a Darlington connection can have a very high input impedance and can produce very large output currents. Darlington connections are often used with voltage regulators, power amplifiers, and high current switching applications.

Darlington Pair

Figure 11-11a shows a **Darlington pair**. Since the emitter current of Q_1 is the base current for Q_2 , the Darlington pair has an overall current gain of:

$$\beta = \beta_1 \beta_2 \quad (11-7)$$

For instance, if each transistor has a current gain of 200, the overall current gain is:

$$\beta = (200)(200) = 40,000$$

Semiconductor manufacturers can put a Darlington pair inside a single case like Fig. 11-11b. This device, known as a **Darlington transistor**, acts like a single transistor with a very high current gain. For instance, the 2N6725 is a Darlington transistor with a current gain of 25,000 at 200 mA. As another example, the TIP102 is a power Darlington with a current gain of 1000 at 3 A.

This is shown in the data sheet of Fig. 11-12. Notice that this device uses a TO-220 case style and has built-in base-emitter shunt resistors, along with an

Figure 11-11 (a) Darlington pair; (b) Darlington transistor; (c) complementary Darlington.

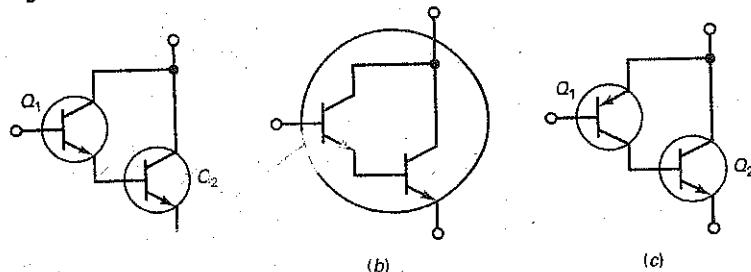


Figure 11-12 Darlington transistor. (Courtesy Fairchild Semiconductor Corporation)

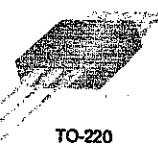
TIP100/101/102

FAIRCHILD
SEMICONDUCTOR®

TIP100/101/102

Monolithic Construction With Built In Base-Emitter Shunt Resistors

- High DC Current Gain : $h_{FE}=1000$ @ $V_{CE}=4V$, $I_C=3A$ (Min.)
- Collector-Emitter Sustaining Voltage
- Low Collector-Emitter Saturation Voltage
- Industrial Use
- Complementary to TIP105/106/107



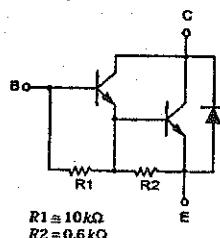
1.Base 2.Collector 3.Emitter

NPN Epitaxial Silicon Darlington Transistor

Absolute Maximum Ratings $T_C=25^\circ C$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Base Voltage : TIP100	60	V
	: TIP101	80	V
	: TIP102	100	V
V_{CEO}	Collector-Emitter Voltage : TIP100	60	V
	: TIP101	80	V
	: TIP102	100	V
V_{EB0}	Emitter-Base Voltage	5	V
I_C	Collector Current (DC)	8	A
I_{CP}	Collector Current (Pulse)	15	A
I_B	Base Current (DC)	1	A
P_c	Collector Dissipation ($T_a=25^\circ C$)	2	W
	Collector Dissipation ($T_C=25^\circ C$)	80	W
T_J	Junction Temperature	150	$^\circ C$
T_{STG}	Storage Temperature	-65 ~ 150	$^\circ C$

Equivalent Circuit



$R1 \approx 10k\Omega$
 $R2 \approx 0.6k\Omega$

Electrical Characteristics $T_C=25^\circ C$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage : TIP100	$I_C = 30mA$, $I_B = 0$	60		V
	: TIP101		80		V
	: TIP102		100		V
I_{CEO}	Collector Cut-off Current : TIP100	$V_{CE} = 30V$, $I_E = 0$		50	μA
	: TIP101	$V_{CE} = 40V$, $I_E = 0$		50	μA
	: TIP102	$V_{CE} = 50V$, $I_E = 0$		50	μA
I_{CBO}	Collector Cut-off Current : TIP100	$V_{CE} = 60V$, $I_E = 0$		50	μA
	: TIP101	$V_{CE} = 80V$, $I_E = 0$		50	μA
	: TIP102	$V_{CE} = 100V$, $I_E = 0$		50	μA
I_{EBO}	Emitter Cut-off Current	$V_{EB} = 5V$, $I_C = 0$		2	mA
h_{FE}	DC Current Gain	$V_{CE} = 4V$, $I_C = 3A$ $V_{CE} = 4V$, $I_C = 8A$	1000 200	20000	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 3A$, $I_B = 5mA$		2	V
		$I_C = 8A$, $I_B = 80mA$		2.5	V
$V_{BE(on)}$	Base-Emitter ON Voltage	$V_{CE} = 4V$, $I_C = 8A$		2.8	V
C_{ob}	Output Capacitance	$V_{CE} = 10V$, $I_E = 0$, $f = 0.1MHz$		200	pF

internal diode. These internal components must be taken into consideration when testing this device with an ohmmeter.

The analysis of a circuit using a Darlington transistor is almost identical to the emitter follower analysis. With the Darlington transistor, since there are two transistors, there are two V_{BE} drops. The base current of Q_2 is the same as the emitter current of Q_1 . Also, the input impedance at the base of Q_1 can be found by $Z_{in(base)} \approx \beta_1 \beta_2 r_e$ or stated as:

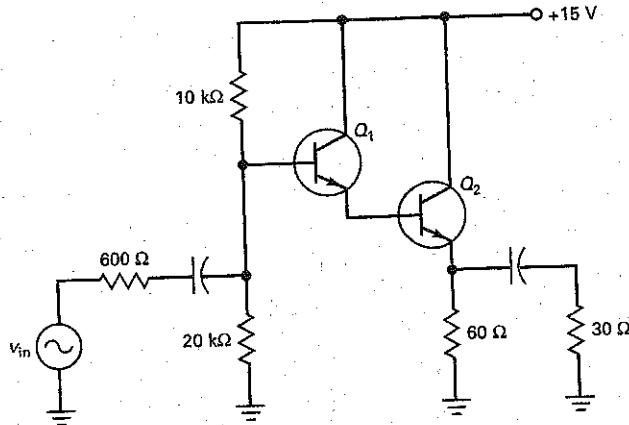
$$Z_{in(base)} \approx \beta_1 \beta_2 r_e \quad (11-8)$$

Example 11-8

Multisim

If each transistor of Fig. 11-13 has a beta value of 100, what is the overall current gain, base current of Q_1 , and input impedance at the base of Q_1 ?

Figure 11-13 Example.



SOLUTION The overall current gain is found by:

$$\beta = \beta_1 \beta_2 = (100)(100) = 10,000$$

The dc emitter current of Q_2 is:

$$I_{EZ} = \frac{10 \text{ V} - 1.4 \text{ V}}{60 \Omega} = 143 \text{ mA}$$

The emitter current of Q_1 is equal to the base current of Q_2 . This is found by:

$$I_{E1} = I_{B2} \equiv \frac{I_{EZ}}{\beta_2} = \frac{143 \text{ mA}}{100} = 1.43 \text{ mA}$$

The base current of Q_1 is:

$$I_{B1} = \frac{I_{E1}}{\beta_1} = \frac{1.43 \text{ mA}}{100} = 14.3 \mu\text{A}$$

To find the input impedance at the base of Q_1 , first solve for r_e . The ac emitter resistance is:

$$r_e = 60 \Omega \parallel 30 \Omega = 20 \Omega$$

The input impedance of the Q_1 base is: $Z_{in(base)} = (10,000)(20 \Omega) = 200 \text{ k}\Omega$

PRACTICE PROBLEM 11-8 Repeat Example 11-8 using a Darlington pair with each transistor having a current gain of 75.

GOOD TO KNOW

The complementary Darlington transistor in Fig. 11-11c was originally developed because complementary high-power transistors were not readily available. The complementary transistor is often used in a special stage known as a *quasi-complementary output stage*.

Complementary Darlington

Figure 11-11c shows another Darlington connection called a **complementary Darlington**, a connection of *npn* and *pnp* transistors. The collector current of Q_1 is the base current of Q_2 . If the *pnp* transistor has a current gain of β_1 and the *npn* output transistor has a current gain of β_2 the complementary Darlington acts like a single *pnp* transistor with a current gain of $\beta_1\beta_2$.

Npn and *pnp* Darlington transistors can be manufactured to be complements to each other. As an example, the TIP105/106/107 *pnp* Darlington series is complementary to the TIP101/102 *npn* series.

11-5 Voltage Regulation

Besides being used in buffer circuits and impedance matching amplifiers, the emitter follower is widely used in voltage regulators. In conjunction with a zener diode, the emitter follower can produce regulated output voltages with much larger output currents.

Zener Follower

Figure 11-14a shows a zener follower, a circuit that combines a zener regulator and an emitter follower. Here is how it works: The zener voltage is the input to the base of the emitter follower. The dc output voltage of the emitter follower is:

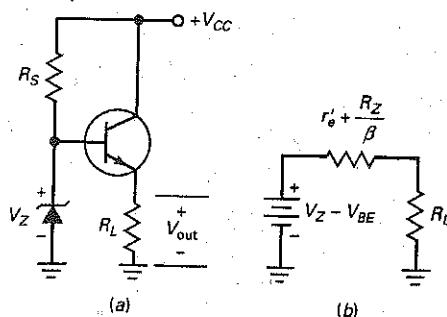
$$V_{\text{out}} = V_Z - V_{BE} \quad (11-9)$$

This output voltage is fixed so that it is equal to the zener voltage minus the V_{BE} drop of the transistor. If the supply voltage changes, the zener voltage remains approximately constant, and so does the output voltage. In other words, the circuit acts like a voltage regulator because the output voltage is always one V_{BE} drop less than the zener voltage.

GOOD TO KNOW

In Fig. 11-14, the emitter-follower circuit reduces the zener current variations by a factor of β if you compare the zener current variations that would exist if the transistor were not there.

Figure 11-14 (a) Zener follower; (b) ac equivalent circuit.



The zener follower has two advantages over an ordinary zener regulator: First, the zener diode of Fig. 11-14a has to produce a load current of only

$$I_B = \frac{I_{\text{out}}}{\beta_{\text{dc}}} \quad (11-10)$$

Since this base current is much smaller than the output current, we can use a much smaller zener diode.

For instance, if you are trying to supply several amperes to a load resistor, an ordinary zener regulator requires a zener diode capable of handling several amperes. On the other hand, with the improved regulator of Fig. 11-14a, the zener diode needs to handle only tens of milliamperes.

The second advantage of a zener follower is its low output impedance. In an ordinary zener regulator, the load resistor sees an output impedance of approximately R_Z , the zener impedance. But in the zener follower, the output impedance is:

$$z_{\text{out}} = r'_e + \frac{R_Z}{\beta_{\text{dc}}} \quad (11-11)$$

Figure 11-14b shows the equivalent output circuit. Because z_{out} is usually very small compared to R_L , an emitter follower can hold the dc output voltage almost constant because the source looks stiff.

In summary, the zener follower provides the regulation of a zener diode with the increased current-handling capability of an emitter follower.

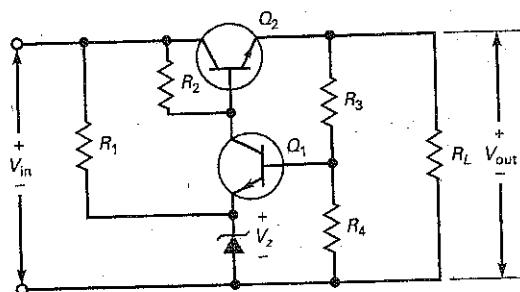
Two-Transistor Regulator

Figure 11-15 shows another voltage regulator. The dc input voltage V_{in} comes from an unregulated power supply such as a bridge rectifier with a capacitor-input filter. Typically, V_{in} has a peak-to-peak ripple of about 10 percent of the dc voltage. The final output voltage V_{out} has almost no ripple and is almost constant in value, even though the input voltage and load current may vary over a large range.

How does it work? Any attempted change in output voltage produces an amplified feedback voltage that opposes the original change. For instance, suppose the output voltage increases. Then, the voltage appearing at the base of Q_1 will increase. Since Q_1 and Q_2 form a CE amplifier, the collector voltage of Q_1 will decrease because of the voltage gain.

Since the collector voltage of Q_1 has decreased, the base voltage of Q_2 decreases. Because Q_2 is an emitter follower, the output voltage will decrease. In other words, we have negative feedback. The original increase in output voltage produces an opposing decrease in output voltage. The overall effect is that the output voltage will increase only slightly, much less than it would without the negative feedback.

Figure 11-15 Transistor voltage regulator.



Conversely, if the output voltage tries to decrease, less voltage appears at the Q_1 base, more voltage appears at the Q_1 collector, and more voltage appears at the Q_2 emitter. Again, we have a returning voltage that opposes the original change in output voltage. Therefore, the output voltage will decrease only a little, far less than without the negative feedback.

Because of the zener diode, the Q_1 emitter voltage equals V_Z . The Q_1 base voltage is one V_{BE} drop higher. Therefore, the voltage across R_4 is:

$$V_4 = V_Z + V_{BE}$$

With Ohm's law, the current through R_4 is:

$$I_4 = \frac{V_Z + V_{BE}}{R_4}$$

Since this current flows through R_3 in series with R_4 , the output voltage is:

$$V_{out} = I_4(R_3 + R_4)$$

After expanding:

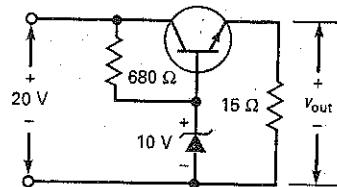
$$V_{out} = \frac{R_3 + R_4}{R_4} (V_Z + V_{BE}) \quad (11-12)$$

Example 11-9

 Multisim

Figure 11-16 shows a zener follower as it is usually drawn on a schematic diagram. What is the output voltage? What is the zener current if $\beta_{dc} = 100$?

Figure 11-16 Example.



SOLUTION The output voltage is approximately:

$$V_{out} = 10 \text{ V} - 0.7 \text{ V} = 9.3 \text{ V}$$

With a load resistance of 15Ω , the load current is:

$$I_{out} = \frac{9.3 \text{ V}}{15 \Omega} = 0.62 \text{ A}$$

The base current is:

$$I_B = \frac{0.62 \text{ A}}{100} = 6.2 \text{ mA}$$

The current through the series resistor is:

$$I_S = \frac{20 \text{ V} - 10 \text{ V}}{680 \Omega} = 14.7 \text{ mA}$$

The zener current is:

$$I_Z = 14.7 \text{ mA} - 6.2 \text{ mA} = 8.5 \text{ mA}$$

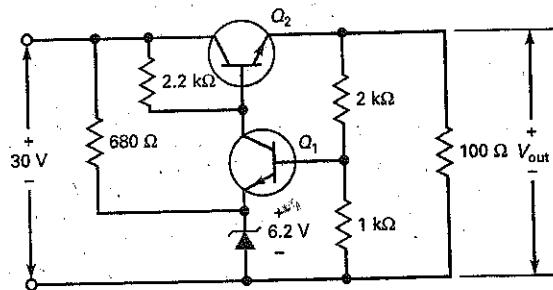
PRACTICE PROBLEM 11-9 Repeat Example 11-9 using an 8.2 V zener diode and an input voltage of 15 V.

Example 11-10

Multisim

What is the output voltage in Fig. 11-17?

Figure 11-17 Example.



SOLUTION With Eq. (11-12):

$$V_{\text{out}} = \frac{2 \text{ k}\Omega + 1 \text{ k}\Omega}{1 \text{ k}\Omega} (6.2 \text{ V} + 0.7 \text{ V}) = 20.7 \text{ V}$$

You can also solve the problem as follows: The current through the 1-kΩ resistor is:

$$I_4 = \frac{6.2 \text{ V} + 0.7 \text{ V}}{1 \text{ k}\Omega} = 6.9 \text{ mA}$$

This current flows through a total resistance of 3 kΩ, which means that the output voltage is:

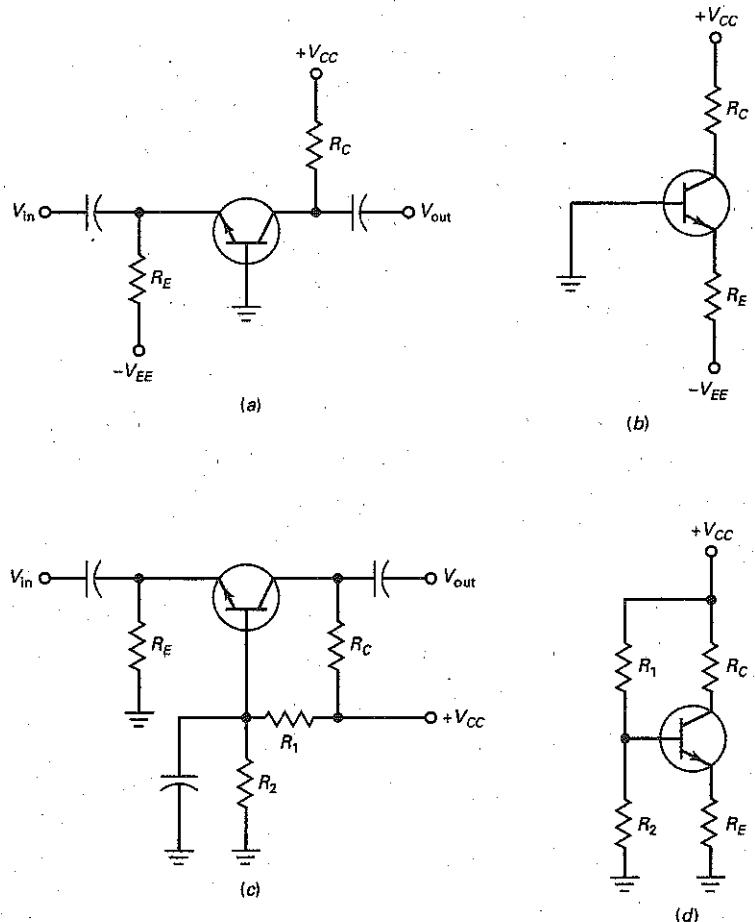
$$V_{\text{out}} = (6.9 \text{ mA})(3 \text{ k}\Omega) = 20.7 \text{ V}$$

PRACTICE PROBLEM 11-10 Using Fig. 11-17, change the zener value to 5.6 V and find the new V_{out} value.

11-6 The Common-Base Amplifier

Figure 11-18a shows a common-base (CB) amplifier using a dual polarity or split power supply. Since the base is grounded, this circuit is also called a grounded-based amplifier. The Q point is set by emitter bias as shown by the dc

Figure 11-18 CB amplifier. (a) Split supply; (b) emitter-biased dc equivalent circuit; (c) single supply; (d) voltage-divider-biased dc equivalent circuit.



equivalent circuit shown in Fig. 11-18b. Therefore, the dc emitter current is found by:

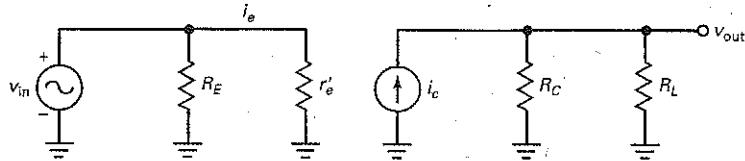
$$I_E = \frac{V_{EE} - V_{BE}}{R_E} \quad (11-13)$$

Figure 11-18c shows a voltage-divider bias CB amplifier using a single power supply source. Notice the bypass capacitor across R_2 . This places the base at ac ground. By drawing the dc equivalent circuit, as shown in Fig. 11-18d, you should recognize the voltage-divider bias configuration.

In either amplifier, the base is at ac ground. The input signal drives the emitter, and the output signal is taken from the collector. Figure 11-19a shows the ac equivalent circuit of a CB amplifier during the positive half-cycle of input voltage. In this circuit, the ac collector voltage, or v_{out} , equals:

$$v_{out} \cong i_C r_C$$

Figure 11-19 AC equivalent circuit.



This is in phase with the ac input voltage v_e . Since the input voltage equals:

$$v_{in} = i_e r'_e$$

The voltage gain is:

$$A_V = \frac{v_{out}}{v_{in}} = \frac{i_c r_C}{i_e r'_e}$$

because $i_c \equiv i_e$, the equation simplifies to:

$$A_V = \frac{r_C}{r'_e} \quad (11-14)$$

Notice that the voltage gain has the same magnitude as it would in an unswamped CE amplifier. The only difference is the phase of the output voltage. Whereas the output signal of a CE amplifier is 180° out of phase with the input signal, the output voltage of the CB amplifier is in phase with the input signal.

Ideally, the collector current source of Fig. 11-19 has an infinite internal impedance. Therefore, the output impedance of a CB amplifier is:

$$z_{out} \cong R_C \quad (11-15)$$

One of the major differences between the CB amplifier and other amplifier configurations is its low input impedance. Looking into the emitter of Fig. 11-19, we have an input impedance of:

$$z_{in(emitter)} = \frac{v_e}{i_e} = \frac{i_e r'_e}{i_e} \quad \text{OR} \quad z_{in(emitter)} = r'_e$$

The input impedance of the circuit is:

$$z_{in} = R_E \parallel r'_e$$

Since R_E is normally much larger than r'_e , the circuit input impedance is approximately:

$$z_{in} \cong r'_e \quad (11-16)$$

As an example, if $I_E = 1 \text{ mA}$, the input impedance of a CB amplifier is only 25Ω . Unless the input ac source is very small, most of the signal will be lost across the source resistance.

The input impedance of a CB amplifier is normally so low that it overloads most signal sources. Because of this, a discrete CB amplifier is not used too often at low frequencies. It is mainly used in high-frequency applications (above 10 MHz) where low source impedances are common. Also, at high frequencies, the base separates the input and output resulting in fewer oscillations at these frequencies.

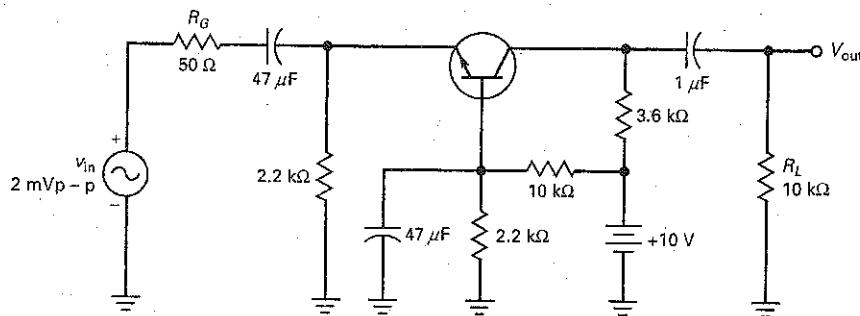
An emitter follower circuit was used in applications where a high impedance source needed to drive a low impedance load. Just the opposite, a common-base circuit can be used to couple a low impedance source to a high impedance load.

Example 11-11

Multisim

What is the output voltage of Fig. 11-20?

Figure 11-20 Example.



SOLUTION The circuit needs to have its *Q* point determined.

$$V_B = \frac{2.2 \text{ k}\Omega}{10 \text{ k}\Omega + 2.2 \text{ k}\Omega} (+10 \text{ V}) = 1.8 \text{ V}$$

$$V_E = V_B - 0.7 \text{ V} = 1.8 \text{ V} - 0.7 \text{ V} = 1.1 \text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{1.1 \text{ V}}{2.2 \text{ k}\Omega} = 500 \mu\text{A}$$

$$\text{Therefore, } r'_e = \frac{25 \text{ mV}}{500 \mu\text{A}} = 50 \Omega$$

Now, solving for the ac circuit values:

$$z_{in} = R_E \parallel r'_e = 2.2 \text{ k}\Omega \parallel 50 \Omega \cong 50 \Omega$$

$$z_{out} = R_C = 3.6 \text{ k}\Omega$$

$$A_V = \frac{r_c}{r'_e} = \frac{3.6 \text{ k}\Omega \parallel 10 \text{ k}\Omega}{50 \Omega} = \frac{2.65 \text{ k}\Omega}{50 \Omega} = 53$$

$$v_{in(base)} = \frac{r'_e}{R_G} (v_{in}) = \frac{50 \Omega}{50 \Omega + 50 \Omega} (2 \text{ mV}_{pp}) = 1 \text{ mV}_{pp}$$

$$v_{out} = (A_V)(v_{in(base)}) = (53)(1 \text{ mV}_{pp}) = 53 \text{ mV}_{pp}$$

PRACTICE PROBLEM 11-11 In Fig. 11-20, change V_{CC} to 20 V and find v_{out} .

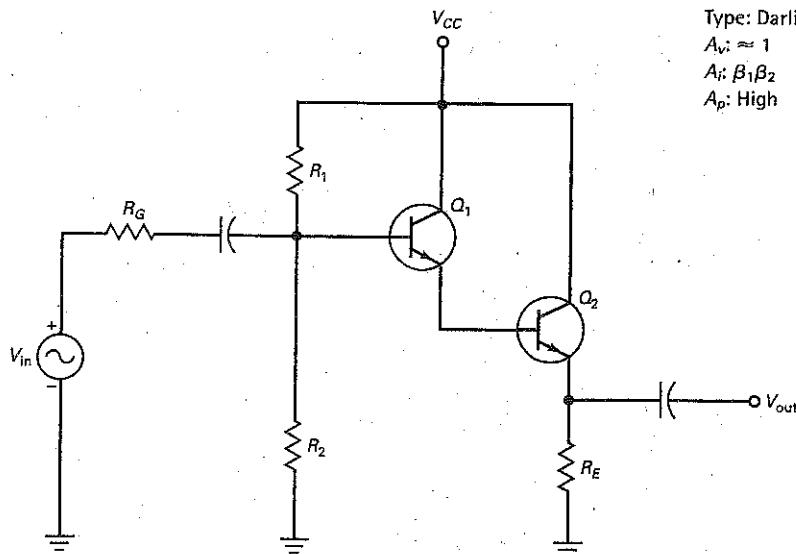
A summary of the four common transistor amplifier configurations is shown in Summary Table 11-1. It is important to be able to recognize the amplifier configuration, know its basic characteristics, and understand its common applications.

Summary Table 11-1

Common Amplifier Configurations

	Type: CE A_v : Medium-High A_i : β A_p : High	$\phi: 180^\circ$ Z_{in} : Medium Z_{out} : Medium Applications: General purpose amplifier, with voltage and current gain
	Type: CC $A_v \approx 1$ A_i : β A_p : Medium	$\phi: 0^\circ$ Z_{in} : High Z_{out} : Low Applications: Buffer, impedance matching, high current driver
	Type: CB A_v : Medium-high $A_i \approx 1$ A_p : Medium	$\phi: 0^\circ$ Z_{in} : Low Z_{out} : High Applications: High-frequency amplifier, low to high impedance matching

Summary Table 11-1 (continued)



Type: Darlington

$A_v \approx 1$

$A_i: \beta_1\beta_2$

$A_p: \text{High}$

$\phi: 0^\circ$

$Z_{in}: \text{Very high}$

$Z_{out}: \text{Low}$

Applications: Buffer,
high current driver,
and amplifier

Summary

SEC. 11-1 CC AMPLIFIER

A CC amplifier, better known as an emitter follower, has its collector at ac ground. The input signal drives the base and the output signal comes from the emitter. Because it is heavily swamped, an emitter follower has stable voltage gain, high input impedance, and low distortion.

SEC. 11-2 OUTPUT IMPEDANCE

The output impedance of an amplifier is the same as its Thevenin impedance. An emitter follower has a low output impedance. The current gain of a transistor transforms the source impedance driving the base to a much lower value when seen from the emitter.

SEC. 11-3 CASCADING CE AND CC

When a low resistance load is connected to the output of a CE amplifier, it may

become overloaded resulting in a very small voltage gain. A CC amplifier placed between the CE output and load will significantly reduce this effect. In this way, the CC amplifier is acting as a buffer.

SEC. 11-4 DARLINGTON CONNECTIONS

Two transistors can be connected as a Darlington pair. The emitter of the first is connected to the base of the second. This produces an overall current gain equal to the product of the individual current gains.

SEC. 11-5 VOLTAGE REGULATION

By combining a zener diode and an emitter follower, we get a zener follower. This circuit produces regulated output voltage with large load currents. The advantage is that the zener current is

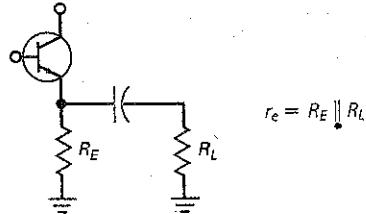
much smaller than the load current. By adding a stage of voltage gain, a larger regulated output voltage can be produced.

SEC. 11-6 COMMON-BASE AMPLIFIER

The CB amplifier configuration has its base at ac ground. The input signal drives the emitter and the output signal comes from the collector. Even though this circuit has no current gain, it can produce a significant voltage gain. The CB amplifier has a low input impedance and high output impedance, and is used in high-frequency applications.

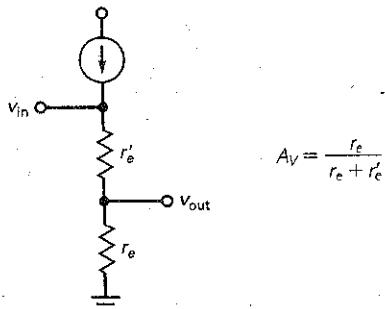
Definitions

(11-1) AC emitter resistance:

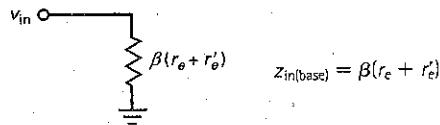


Derivations

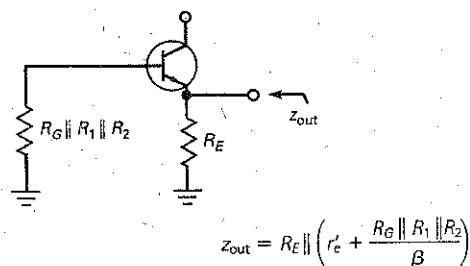
(11-2) Emitter-follower voltage gain:



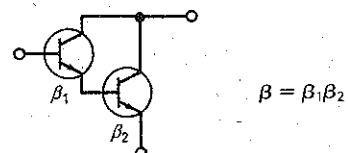
(11-3) Emitter-follower input impedance of base:



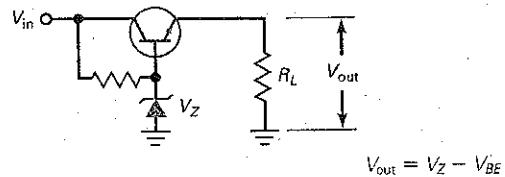
(11-5) Emitter-follower output impedance:



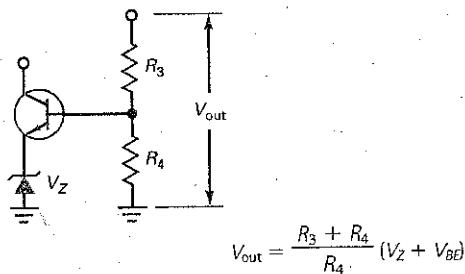
(11-7) Darlington current gain:



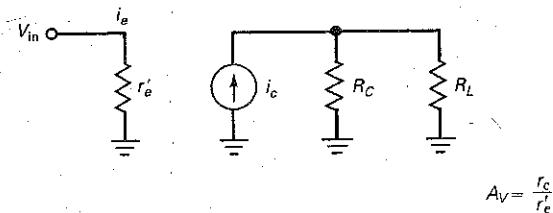
(11-9) Zener follower:



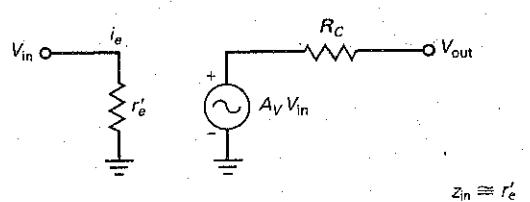
(11-12) Voltage regulator:



(11-14) Common-base voltage gain:



(11-16) Common-base input impedance:



Student Assignments

1. An emitter follower has a voltage gain that is
 - Much less than one
 - Approximately equal to one
 - Greater than one
 - Zero
2. The total ac emitter resistance of an emitter follower equals
 - r'_e
 - r_e
 - $r_e + r'_e$
 - R_E
3. The input impedance of the base of an emitter follower is usually
 - Low
 - High
 - Shorted to ground
 - Open
4. The dc current gain of an emitter follower is
 - 0
 - ≈ 1
 - β_{dc}
 - Dependant on r'_e
5. The ac base voltage of an emitter follower is across the
 - Emitter diode
 - DC emitter resistor
 - Load resistor
 - Emitter diode and external ac emitter resistance
6. The output voltage of an emitter follower is across the
 - Emitter diode
 - DC collector resistor
 - Load resistor
 - Emitter diode and external ac emitter resistance
7. If $\beta = 200$ and $r_e = 150 \Omega$, the input impedance of the base is
 - $30 \text{ k}\Omega$
 - 600Ω
 - $3 \text{ k}\Omega$
 - $5 \text{ k}\Omega$
8. The input voltage to an emitter follower is usually
 - Less than the generator voltage
 - Equal to the generator voltage
 - Greater than the generator voltage
 - Equal to the supply voltage
9. The ac emitter current is closest to
 - V_G divided by r_e
 - v_{in} divided by r'_e
 - V_B divided by r'_e
 - v_{in} divided by r_e
10. The output voltage of an emitter follower is approximately
 - 0
 - V_G
 - v_{in}
 - V_{CC}
11. The output voltage of an emitter follower is
 - In phase with v_{in}
 - Much greater than v_{in}
 - 180° out of phase
 - Generally much less than v_{in}
12. An emitter-follower buffer is generally used when
 - $R_G \ll R_L$
 - $R_G = R_L$
 - $R_L \ll R_G$
 - R_L is very large
13. For maximum power transfer, a CC amplifier is designed so
 - $R_G \ll Z_{in}$
 - $Z_{out} \gg R_L$
 - $Z_{out} \ll R_L$
 - $Z_{out} = R_L$
14. If a CE stage is directly coupled to an emitter follower
 - Low and high frequencies will be passed
 - Only high frequencies will be passed
 - High-frequency signals will be blocked
 - Low-frequency signals will be blocked
15. If the load resistance of an emitter follower is very large, the external ac emitter resistance equals
 - Generator resistance
 - Impedance of the base
 - DC emitter resistance
 - DC collector resistance
16. If an emitter follower has $r'_e = 10 \Omega$ and $r_e = 90 \Omega$, the voltage gain is approximately
 - 0
 - 0.5
 - 0.9
 - 1
17. An emitter follower circuit always makes the source resistance
 - β times smaller
 - β times larger
 - Equal to the load
 - Zero
18. A Darlington transistor has
 - A very low input impedance
 - Three transistors
 - A very high current gain
 - One V_{BE} drop
19. The amplifier configuration that produces a 180° phase shift is the
 - CB
 - CC
 - CE
 - All of the above
20. If the generator voltage is 5 mV in an emitter follower, the output voltage across the load is closest to
 - 5 mV
 - 150 mV
 - 0.25 V
 - 0.5 V
21. If the load resistor of Fig. 11-1a is shorted, which of the following are different from their normal values?
 - Only ac voltages
 - Only dc voltages
 - Both dc and ac voltages
 - Neither dc nor ac voltages

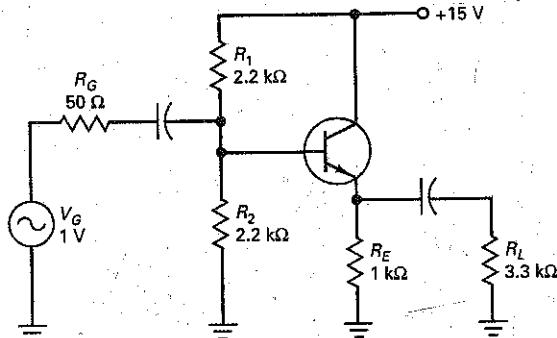
22. If R_1 is open in an emitter follower, which of these is true?
- DC base voltage is V_{CC}
 - DC collector voltage is zero
 - Output voltage is normal
 - DC base voltage is zero
23. Usually, the distortion in an emitter follower is
- Very low
 - Very high
 - Large
 - Not acceptable
24. The distortion in an emitter follower is
- Seldom low
 - Often high
 - Always low
 - High when clipping occurs
25. If a CE stage is direct coupled to an emitter follower, how many coupling capacitors are there between the two stages?
- 0
 - 1
 - 2
 - 3
26. A Darlington transistor has a β of 8000. If $R_E = 1\text{ k}\Omega$ and $R_L = 100\text{ }\Omega$, the input impedance of the base is closest to
- $8\text{ k}\Omega$
 - $800\text{ k}\Omega$
 - $80\text{ k}\Omega$
 - $8\text{ M}\Omega$
27. The ac emitter resistance of an emitter follower
- Equals the dc emitter resistance
 - Is larger than the load resistance
 - Is β times smaller than the load resistance
 - Is usually less than the load resistance
28. A common-base amplifier has a voltage gain that is
- Much less than one
 - Approximately equal to one
 - Greater than one
 - Zero
29. An application of a common-base amplifier is when
- $R_{source} \gg R_L$
 - $R_{source} \ll R_L$
 - A high current gain is required
 - High frequencies need to be blocked
30. A common-base amplifier can be used when
- Matching low to high impedances
 - A voltage gain without a current gain is required
 - A high-frequency amplifier is needed
 - All of the above
31. The zener current in a zener follower is
- Equal to the output current
 - Smaller than the output current
 - Larger than the output current
 - Prone to thermal runaway
32. In the two-transistor voltage regulator, the output voltage
- Is regulated
 - Has much smaller ripple than the input voltage
 - Is larger than the zener voltage
 - All of the above

Problems

SEC. 11-1 CC AMPLIFIER

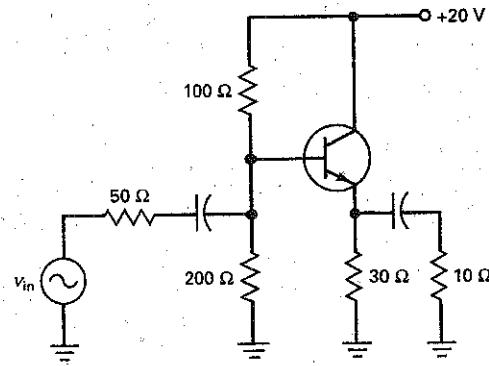
- 11-1 In Fig. 11-21, what is the input impedance of the base if $\beta = 200$? The input impedance of the stage?
- 11-2 If $\beta = 150$ in Fig. 11-21, what is the ac input voltage to the emitter follower?
- 11-3 What is the voltage gain in Fig. 11-21? If $\beta = 175$, what is the ac load voltage?

Figure 11-21



- 11-4 What is the input voltage in Fig. 11-21 if β varies over a range of 50 to 300?
- 11-5 All resistors are doubled in Fig. 11-21. What happens to the input impedance of the stage if $\beta = 150$? To the input voltage?
- 11-6 What is the input impedance of the base if $\beta = 200$ in Fig. 11-22? The input impedance of the stage?

Figure 11-22



11-7 In Fig. 11-22, what is the ac input voltage to the emitter follower if $\beta = 150$ and $V_{in} = 1\text{ V}$?

11-8 What is the voltage gain in Fig. 11-22? If $\beta = 175$, what is the ac load voltage?

SEC. 11-2 OUTPUT IMPEDANCE

11-9 What is the output impedance in Fig. 11-21 if $\beta = 200$?

11-10 What is the output impedance in Fig. 11-22 if $\beta = 100$?

11-12 If both transistors in Fig. 11-23 have a dc and ac current gain of 150, what is the output voltage when $V_G = 10\text{ mV}$?

11-13 If both transistors have a dc and ac current gain of 200 in Fig. 11-23, what is the voltage gain of the CE stage if the load resistance drops to $125\text{ }\Omega$?

11-14 In Fig. 11-23, what would happen to the voltage gain of the CE amplifier if the emitter follower stage were removed and a capacitor were used to couple the ac signal to the $150\text{ }\Omega$ load?

SEC. 11-3 CASCADING CE AND CC

11-11 What is the voltage gain of the CE stage in Fig. 11-23 if the second transistor has a dc and ac current gain of 200?

SEC. 11-4 DARLINGTON CONNECTIONS

11-15 If the Darlington pair of Fig. 11-24 has an overall current gain of 5000, what is the input impedance of the Q_1 base?

Figure 11-23

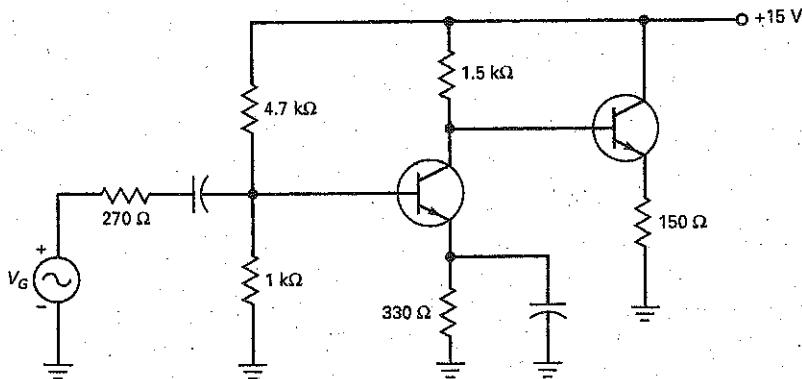


Figure 11-24

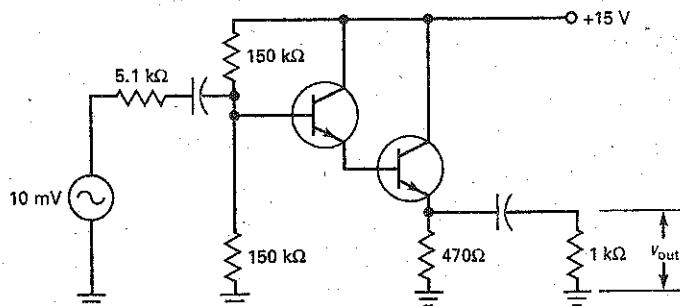
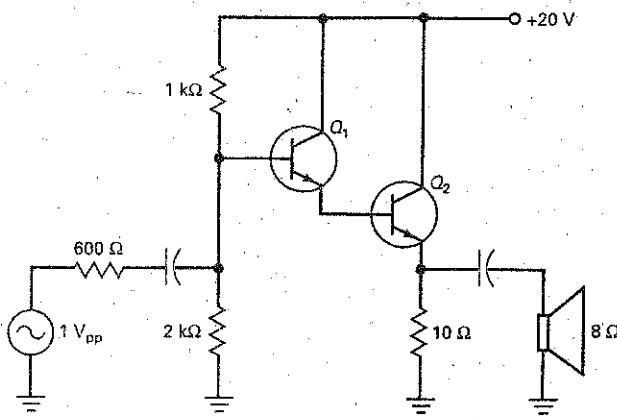


Figure 11-25



- 11-16 In Fig. 11-24, what is the ac input voltage to the Q_1 base if the Darlington pair has an overall current gain of 7000?
- 11-17 Both transistors have a β of 150 in Fig. 11-25. What is the input impedance of the first base?
- 11-18 In Fig. 11-25, what is the ac input voltage to the Q_1 base if the Darlington pair has an overall current gain of 2000?

SEC. 11-5 VOLTAGE REGULATION

- 11-19 The transistor of Fig. 11-26 has a current gain of 150. If the 1N958 has a zener voltage of 7.5 V, what is the output voltage? The zener current?
- 11-20 If the input voltage of Fig. 11-26 changes to 25 V, what is the output voltage? The zener current?
- 11-21 The potentiometer of Fig. 11-27 can vary from 0 to 1 k Ω . What is the output voltage when the wiper is at the center?

Figure 11-26

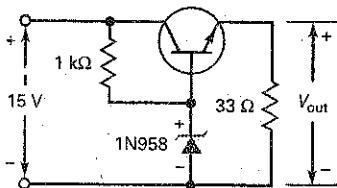
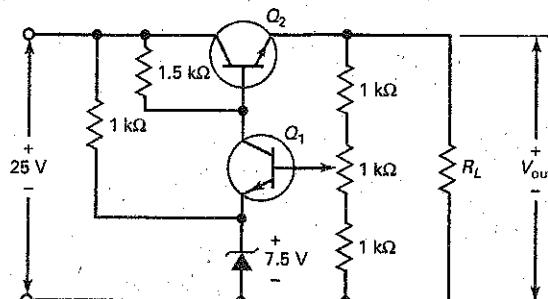


Figure 11-27

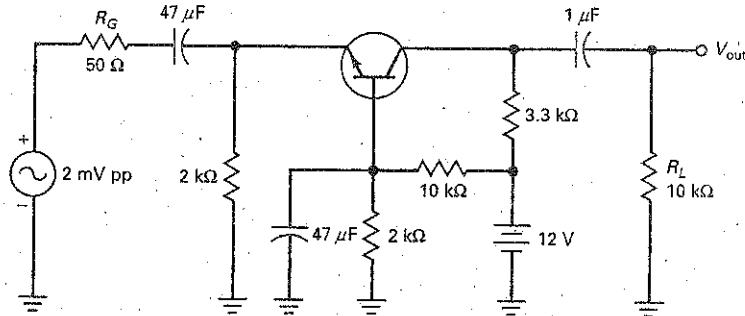


- 11-22 What is the output voltage in Fig. 11-27 if the wiper is all the way up? If it is all the way down?

SEC. 11-6 COMMON-BASE AMPLIFIER

- 11-23 In Fig. 11-28, what is the Q point emitter current?
- 11-24 What is the approximate voltage gain of Fig. 11-28?
- 11-25 In Fig. 11-28, what is the input impedance looking into the emitter? What is the input impedance of the stage?
- 11-26 In Fig. 11-28, with an input of 2 mV from the generator, what is the value of V_{out} ?
- 11-27 In Fig. 11-28, if the V_{CC} supply voltage were increased to 15 V, what would V_{out} equal?

Figure 11-28

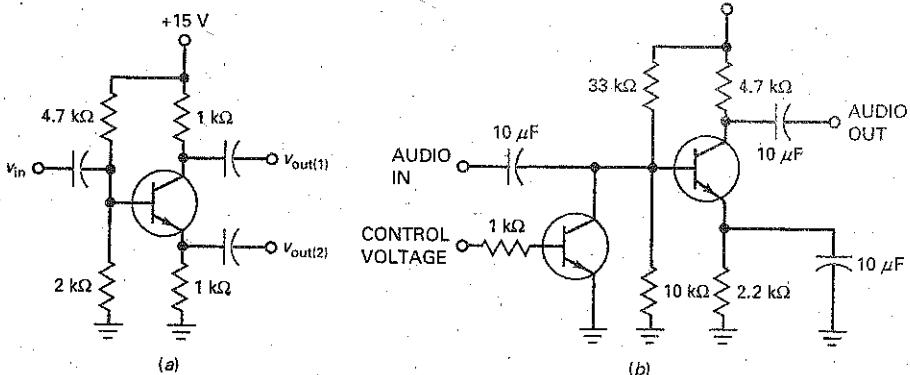


Critical Thinking

- 11-28 In Fig. 11-26, what is the power dissipation of the transistor if the current gain is 100 and the zener voltage is 7.5 V?
- 11-29 In Fig. 11-28a, the transistor has a β_{dc} of 150. Calculate the following dc quantities: V_B , V_E , V_G , I_B , I_C and I_B .
- 11-30 If an input signal with a peak-to-peak value of 5 mV drives the circuit of Fig. 11-29a, what are the two ac output voltages? What do you think is the purpose of this circuit?
- 11-31 Figure 11-29b shows a circuit in which the control voltage can be 0 V or +5 V. If the audio input voltage is 10 mV, what is the audio output voltage when the control voltage is 0 V? When the control voltage is +5 V? What do you think this circuit is supposed to do?
- 11-32 In Fig. 11-26, what would the output voltage be if the zener diode opened?

- 11-33 In Fig. 11-26, if the 33Ω load shorts, what is the transistor's power dissipation?
- 11-34 In Fig. 11-27, what is the power dissipation of Q_2 when the wiper is at the center and the load resistance is 100Ω ?
- 11-35 Using Fig. 11-24, if both transistors have a β of 100, what is the approximate output impedance of the amplifier?
- 11-36 In Fig. 11-23, if the input voltage from the generator were 100 mV pp and the emitter-bypass capacitor opened, what would the output voltage across the load be?
- 11-37 In Fig. 11-28, what would be the output voltage if the base-bypass capacitor shorted?

Figure 11-29



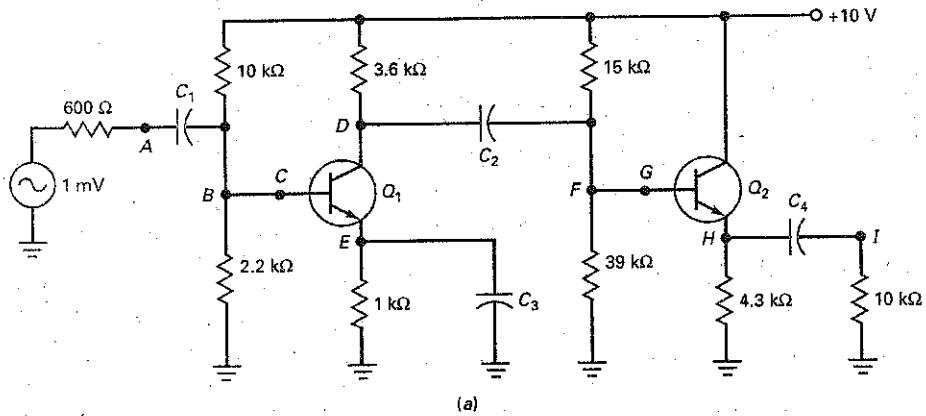
Troubleshooting

Use Fig. 11-30 for the remaining problems. The table labeled "Ac Millivolts" contains the measurements of the ac voltages expressed in millivolts. For this exercise, all resistors are OK. The troubles are limited to open capacitors, open connecting wires, and open transistors.

- 11-38 Find Troubles T1 to T3.

- 11-39 Find Troubles T4 to T7.

Figure 11-30



(a)

Ac Millivolts

Trouble	V_A	V_B	V_C	V_D	V_E	V_F	V_G	V_H	V_I
OK	0.6	0.6	0.6	70	0	70	70	70	70
T1	0.6	0.6	0.6	70	0	70	70	70	0
T2	0.6	0.6	0.6	70	0	70	0	0	0
T3	1	0	0	0	0	0	0	0	0
T4	0.75	0.75	0.75	2	0.75	2	2	2	2
T5	0.75	0.75	0	0	0	0	0	0	0
T6	0.6	0.6	0.6	95	0	0	0	0	0
T7	0.6	0.6	0.6	70	0	70	70	0	0

(b)

Job Interview Questions

1. Draw the schematic diagram of an emitter follower. Tell me why this circuit is widely used in power amplifiers and voltage regulators.
2. Tell me all that you know about the output impedance of an emitter follower.
3. Draw a Darlington pair and explain why the overall current gain is the product of the individual current gains.
4. Draw a zener follower and explain why it regulates the output voltage against changes in the input voltage.
5. What is the voltage gain of an emitter follower? This being the case, in what applications would such a circuit be useful?
6. Explain why a Darlington pair has a higher power gain than a single transistor.
7. Why are "follower" circuits so important in acoustic circuits?
8. What is the approximate ac voltage gain for a CC amplifier?
9. What is another name for a common-collector amplifier?
10. What is the relationship between an ac signal phase (output to input) and a common-collector amplifier?
11. If a technician measures unity voltage gain (output voltage divided by input voltage) from a CC amplifier, what is the problem?
12. The Darlington amplifier is used in the final power amplifier (FPA) in most higher-quality audio amplifiers because it increases the power gain. How does a Darlington amplifier increase the power gain?

Self-Test Answers

- | | | |
|-------|-------|-------|
| 1. b | 12. c | 23. a |
| 2. c | 13. d | 24. d |
| 3. b | 14. a | 25. a |
| 4. c | 15. c | 26. c |
| 5. d | 16. c | 27. d |
| 6. c | 17. a | 28. c |
| 7. a | 18. c | 29. b |
| 8. a | 19. c | 30. d |
| 9. d | 20. a | 31. b |
| 10. c | 21. a | 32. d |
| 11. a | 22. d | |

Practice Problem Answers

- | | | |
|---|---|--|
| 11-1 $Z_{in(base)} = 303 \text{ k}\Omega$;
$Z_{in(stage)} = 4.92 \text{ k}\Omega$ | 11-5 $Z_{out} = 2.86 \Omega$ | 11-9 $V_{out} = 7.5 \text{ V}$;
$I_z = 5 \text{ mA}$ |
| 11-2 $V_{in} \approx 0.893 \text{ V}$ | 11-6 $A_v = 222$ | 11-10 $V_{out} = 18.9 \text{ V}$ |
| 11-3 $V_{in} = 0.979 \text{ V}$;
$V_{out} = 0.974 \text{ V}$ | 11-7 $A_v = 6.28$ | 11-11 $V_{out} = 76.9 \text{ mVpp}$ |
| 11-4 $Z_{out} = 3.33 \Omega$ | 11-8 $\beta = 5625$;
$I_B = 14.3 \mu\text{A}$;
$Z_{in(base)} = 112.5 \text{ k}\Omega$ | |

12

Power Amplifiers

- In a stereo, radio, or television, the input signal is small. After several stages of voltage gain, however, the signal becomes large and uses the entire load line. In these later stages of a system, the collector currents are much larger because the load impedances are much smaller. Stereo amplifier speakers, for example, may have an impedance of $8\ \Omega$ or less.

As indicated in Chap. 6, small-signal transistors have a power rating of less than 1 W, whereas power transistors have a power rating of more than 1 W. Small-signal transistors are typically used at the front end of systems where the signal power is low, and power transistors are used near the end of systems because the signal power and current are high.

Chapter Outline

- 12-1 Amplifier Terms
- 12-2 Two Load Lines
- 12-3 Class A Operation
- 12-4 Class B Operation
- 12-5 Class B Push-Pull Emitter Follower
- 12-6 Biasing Class B/AB Amplifiers
- 12-7 Class B/AB Driver
- 12-8 Class C Operation
- 12-9 Class C Formulas
- 12-10 Transistor Power Rating

Objectives

After studying this chapter, you should be able to:

- Show how the dc load line, ac load line, and Q point are determined for CE and CC power amplifiers.
- Calculate the maximum peak-to-peak (MPP) unclipped ac voltage that is possible with CE and CC power amplifiers.
- Describe the characteristics of amplifiers, including classes of operation, types of coupling, and frequency ranges.
- Draw a schematic of class B/AB push-pull amplifier and explain its operation.
- Determine the efficiency of transistor power amplifiers.
- Discuss the factors that limit the power rating of a transistor and what can be done to improve the power rating.

Vocabulary

ac output compliance	crossover distortion	power gain
ac load line	current drain	preamp
audio amplifier	direct coupling	push-pull circuit
bandwidth (BW)	driver stage	radio-frequency (RF) amplifier
capacitive coupling	duty cycle	thermal runaway
class A operation	efficiency	transformer coupling
class AB operation	harmonics	tuned RF amplifier
class B operation	large-signal operation	wideband amplifier
class C operation	narrowband amplifier	
compensating diodes	power amplifier	

GOOD TO KNOW

As we progress through the letters A, B, and C designating the various classes of operation, we can see that linear operation occurs for shorter and shorter intervals of time. A class D amplifier is one whose output is switched on and off; that is, it essentially spends zero time during each input cycle in the linear region of operation. A class D amplifier is often used as a pulse-width modulator, which is a circuit whose output pulses have widths that are proportional to the amplitude level of the amplifier's input signal.

GOOD TO KNOW

Most integrated circuit amplifiers use direct coupling between stages.

12-1 Amplifier Terms

There are different ways to describe amplifiers. For instance, we can describe them by their class of operation, by their interstage coupling, or by their frequency range.

Classes of Operation

Class A operation of an amplifier means that the transistor operates in the active region at all times. This implies that collector current flows for 360° of the ac cycle, as shown in Fig. 12-1a. With a class A amplifier, the designer usually tries to locate the Q point somewhere near the middle of the load line. This way, the signal can swing over the maximum possible range without saturating or cutting off the transistor, which would distort the signal.

Class B operation is different. It means that collector current flows for only half the cycle (180°), as shown in Fig. 12-1b. To have this kind of operation, a designer locates the Q point at cutoff. Then, only the positive half of ac base voltage can produce collector current. This reduces the wasted heat in power transistors.

Class C operation means that collector current flows for less than 180° of the ac cycle, as shown in Fig. 12-1c. With class C operation, only part of the positive half cycle of ac base voltage produces collector current. As a result, we get brief pulses of collector current like those of Fig. 12-1c.

Types of Coupling

Figure 12-2a shows **capacitive coupling**. The coupling capacitor transmits the amplified ac voltage to the next stage. Figure 12-2b illustrates **transformer coupling**. Here the ac voltage is coupled through a transformer to the next stage. Capacitive coupling and transformer coupling are both examples of ac coupling, which blocks the dc voltage.

Direct coupling is different. In Fig. 12-2c, there is a direct connection between the collector of the first transistor and the base of the second transistor.

Figure 12-1 Collector current: (a) class A; (b) class B; (c) class C.

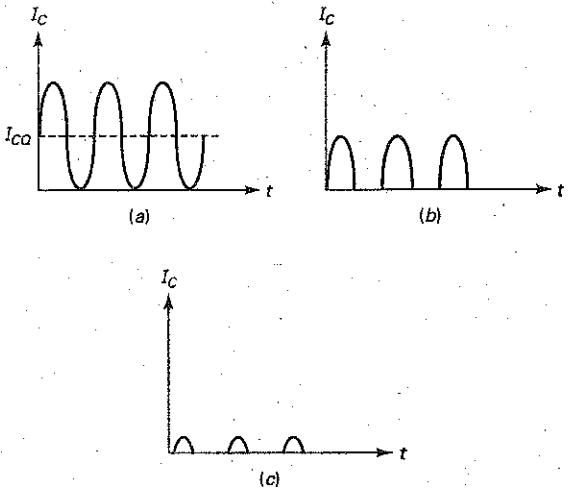
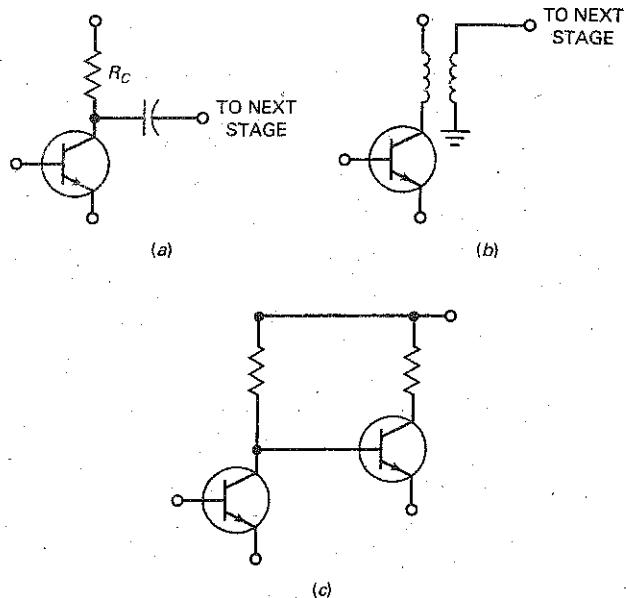


Figure 12-2 Types of coupling: (a) capacitive; (b) transformer; (c) direct.



Because of this, both the dc and the ac voltages are coupled. Since there is no lower frequency limit, a direct-coupled amplifier is sometimes called a *dc amplifier*.

Ranges of Frequency

Another way to describe amplifiers is by stating their frequency range. For instance, an **audio amplifier** refers to an amplifier that operates in the range of 20 Hz to 20 kHz. On the other hand, a **radio-frequency (RF) amplifier** is one that amplifies frequencies above 20 kHz, usually much higher. For instance, the RF amplifiers in AM radios amplify frequencies between 535 and 1605 kHz, and the RF amplifiers in FM radios amplify frequencies between 88 and 108 MHz.

Amplifiers are also classified as **narrowband** or **wideband**. A narrowband amplifier works over a small frequency range like 450 to 460 kHz. A wideband amplifier operates over a large frequency range like 0 to 1 MHz.

Narrowband amplifiers are usually **tuned RF amplifiers**, which means that their ac load is a high-*Q* resonant tank tuned to a radio station or television channel. Wideband amplifiers are usually untuned; that is, their ac load is resistive.

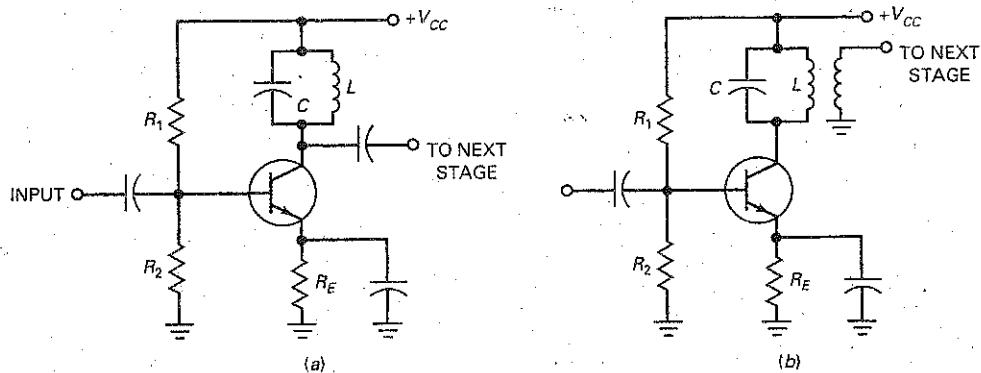
Figure 12-3a is an example of a tuned RF amplifier. The *LC* tank is resonant at some frequency. If the tank has a high *Q*, the bandwidth is narrow. The output is capacitively coupled to the next stage.

Figure 12-3b is another example of a tuned RF amplifier. This time, the narrowband output signal is transformer-coupled to the next stage.

Signal Levels

We have already described **small-signal operation**, in which the peak-to-peak swing in collector current is less than 10 percent of quiescent collector current. In **large-signal operation**, a peak-to-peak signal uses all or most of the load line. In a stereo system, the small signal from a radio tuner, tape player, or compact disc

Figure 12-3 Tuned RF amplifiers: (a) capacitive coupling; (b) transformer coupling.



player is used as the input to a **preamp**, an amplifier that produces a larger output suitable for driving tone and volume controls. The signal is then used as the input to a **power amplifier**, which produces output power ranging from a few hundred milliwatts up to hundreds of watts.

In the remainder of this chapter, we will discuss power amplifiers and related topics like the ac load line, power gain, and efficiency.

12-2 Two Load Lines

Every amplifier has a dc equivalent circuit and an ac equivalent circuit. Because of this, it has two load lines: a dc load line and an ac load line. For small-signal operation, the location of the *Q* point is not critical. But with large-signal amplifiers, the *Q* point has to be at the middle of the ac load line to get the maximum possible output swing.

DC Load Line

Figure 12-4a is a voltage-divider-based (VDB) amplifier. One way to move the *Q* point is by varying the value of R_2 . For very large values of R_2 , the transistor goes into saturation and its current is given by:

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C + R_E} \quad (12-1)$$

Very small values of R_2 will drive the transistor into cutoff, and its voltage is given by:

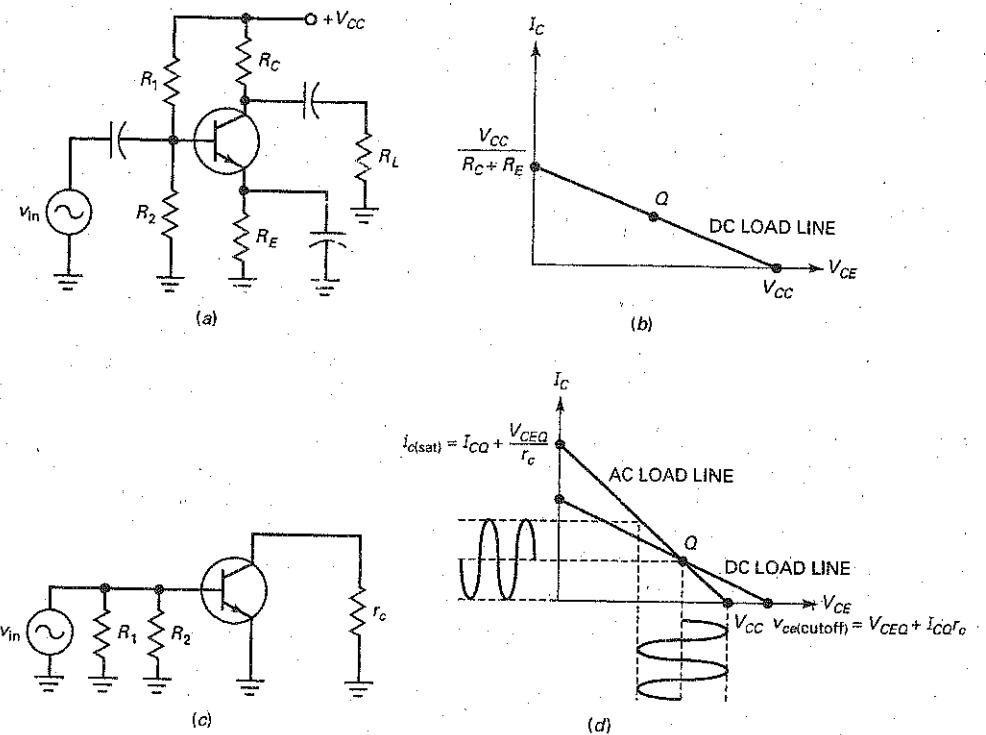
$$V_{CE(\text{cutoff})} = V_{CC} \quad (12-2)$$

Figure 12-4b shows the dc load line with the *Q* point.

AC Load Line

Figure 12-4c is the ac equivalent circuit for the VDB amplifier. With the emitter at ac ground, R_E has no effect on the ac operation. Furthermore, the ac collector resistance is less than the dc collector resistance. Therefore, when an ac signal comes in, the instantaneous operating point moves along the ac load line of Fig. 12-4d. In other words, the peak-to-peak sinusoidal current and voltage are determined by the ac load line.

Figure 12-4 (a) VDB amplifier; (b) dc load line; (c) ac equivalent circuit; (d) ac load line.



As shown in Fig. 12-4d, the saturation and cutoff points on the ac load line differ from those on the dc load line. Because the ac collector and emitter resistance are lower than the respective dc resistance, the ac load line is much steeper. It's important to note that the ac and dc load lines intersect at the Q point. This happens when the ac input voltage is crossing zero.

Here's how to determine the ends of the ac load line. Writing a collector voltage loop gives us:

$$v_{ce} + i_c r_c = 0$$

or

$$i_c = -\frac{v_{ce}}{r_c} \quad (12-3)$$

The ac collector current is given by:

$$i_c = \Delta I_C = I_C - I_{CQ}$$

and the ac collector voltage is:

$$v_{ce} = \Delta V_{CE} = V_{CE} - V_{CEO}$$

When substituting these expressions into Eq. (12-3) and rearranging, we arrive at:

$$I_C = I_{CQ} + \frac{V_{CEO}}{r_c} - \frac{V_{CE}}{r_c} \quad (12-4)$$

This is the equation of the ac load line. When the transistor goes into saturation, V_{CE} is zero, and Eq. (12-4) gives us:

$$i_{c(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_c} \quad (12-5)$$

where $i_{c(\text{sat})}$ = ac saturation current

I_{CQ} = dc collector current

V_{CEQ} = dc collector-emitter voltage

r_c = ac resistance seen by the collector

When the transistor goes into cutoff, I_c equals zero. Since

$$v_{ce(\text{cutoff})} = V_{CEQ} + \Delta V_{CE}$$

and

$$\Delta V_{CE} = (\Delta I_C)(r_c)$$

we can substitute to get:

$$\Delta V_{CE} = (I_{CQ} - OA)(r_c)$$

resulting in:

$$v_{ce(\text{cutoff})} = V_{CEQ} + I_{CQ}r_c \quad (12-6)$$

Because the ac load line has a higher slope than the dc load line, the maximum peak-to-peak (MPP) output is always less than the supply voltage. As a formula:

$$\text{MPP} < V_{CC} \quad (12-7)$$

For instance, if the supply voltage is 10 V, the maximum peak-to-peak sinusoidal output is less than 10 V.

Clipping of Large Signals

When the Q point is at the center of the dc load line (Fig. 12-4d), the ac signal cannot use all of the ac load line without clipping. For instance, if the ac signal increases, we will get the cutoff clipping shown in Fig. 12-5a.

If the Q point is moved higher as shown in Fig. 12-5b, a large signal will drive the transistor into saturation. In this case, we get saturation clipping. Both cutoff and saturation clipping are undesirable because they distort the signal. When a distorted signal like this drives a loudspeaker, it sounds terrible.

A well-designed large-signal amplifier has the Q point at the middle of the ac load line (Fig. 12-5c). In this case, we get a maximum peak-to-peak unclipped output. This maximum unclipped peak-to-peak ac voltage is also referred to as its ac output compliance.

Maximum Output

When the Q point is below the center of the ac load line, the maximum peak (MP) output is $I_{CQ}r_c$, as shown in Fig. 12-6a. On the other hand, if the Q point is above the center of the ac load line, the maximum peak output is V_{CEQ} , as shown in Fig. 12-6b.

For any Q point, therefore, the maximum peak output is:

$$\text{MP} = I_{CQ}r_c \text{ or } V_{CEQ}, \text{ whichever is smaller} \quad (12-8)$$

and the maximum peak-to-peak output is twice this amount:

$$\text{MPP} = 2\text{MP} \quad (12-9)$$

Equations (12-8) and (12-9) are useful in troubleshooting to determine the largest unclipped output that is possible.

Figure 12-5 (a) Cutoff clipping; (b) saturation clipping; (c) optimum *Q* point.

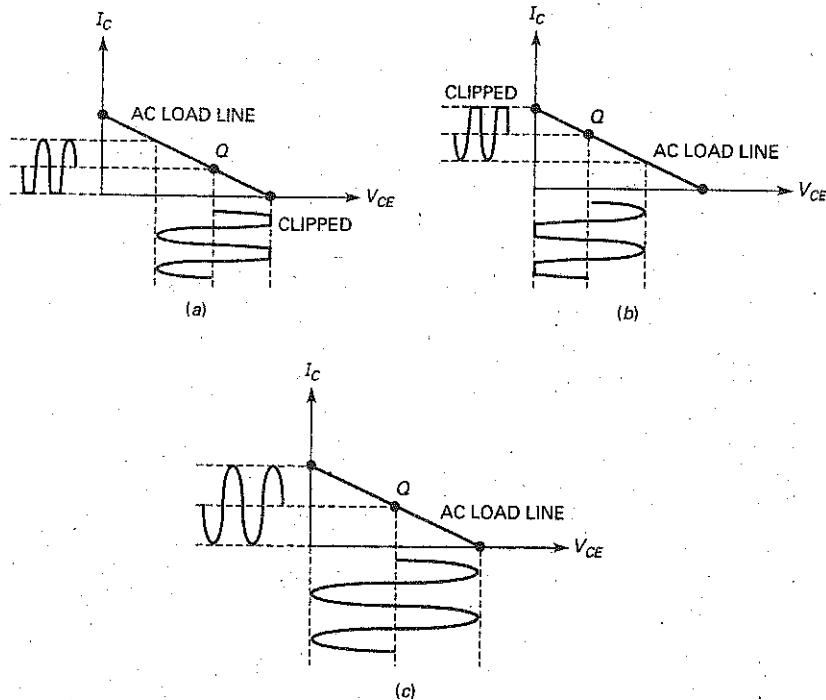
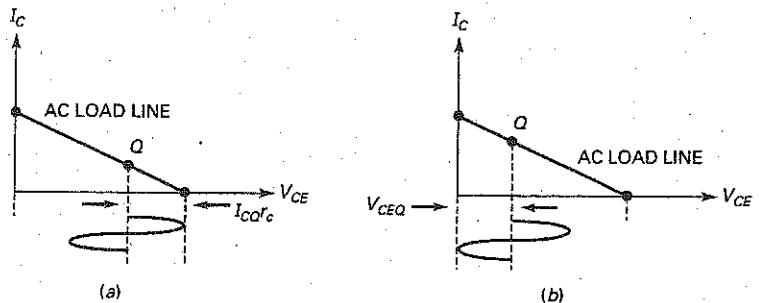


Figure 12-6 *Q* point at center of ac load line.



When the *Q* point is at the center of the ac load line:

$$I_{CQ}r_e = V_{CEQ} \quad (12-10)$$

A designer will try to satisfy this condition as closely as possible, given the tolerance of biasing resistors. The circuit's emitter resistance can be adjusted to find the optimum *Q* point. A formula that can be derived for the optimum emitter resistance is:

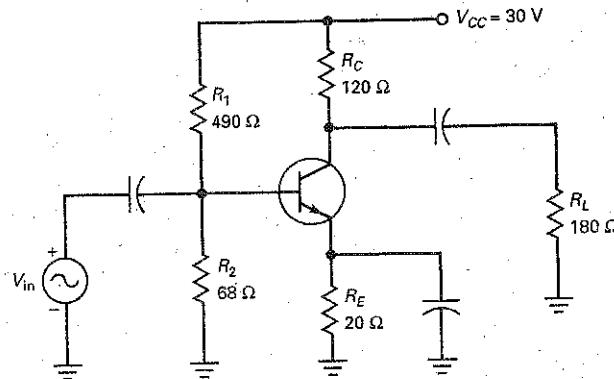
$$R_E = \frac{R_C + r_e}{V_{CC}/V_E - 1} \quad (12-11)$$

Example 12-1

Multisim

What are the values of I_{CQ} , V_{CEQ} and r_c in Fig. 12-7?

Figure 12-7 Example.



SOLUTION

$$V_B = \frac{68 \Omega}{68 \Omega + 490 \Omega} (30 \text{ V}) = 3.7 \text{ V}$$

$$V_E = V_B - 0.7 \text{ V} = 3.7 \text{ V} - 0.7 \text{ V} = 3 \text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{3 \text{ V}}{20 \Omega} = 150 \text{ mA}$$

$$I_{CQ} \approx I_E = 150 \text{ mA}$$

$$V_{CEQ} = V_C - V_E = 12 \text{ V} - 3 \text{ V} = 9 \text{ V}$$

$$r_c = R_C \parallel R_L = 120 \Omega \parallel 180 \Omega = 72 \Omega$$

PRACTICE PROBLEM 12-1 In Fig. 12-7, change R_E from 20Ω to 30Ω . Solve for I_{CQ} and V_{CEQ} .

Example 12-2

Determine the ac load line saturation and cutoff points in Fig. 12-7. Also, find the maximum peak-to-peak output voltage.

SOLUTION From Example 12-1, the transistor's Q point is:

$$I_{CQ} = 150 \text{ mA} \quad \text{and} \quad V_{CEQ} = 9 \text{ V}$$

To find the ac saturation and cutoff points, first determine the ac collector resistance, r_c :

$$r_c = R_C \parallel R_L = 120 \Omega \parallel 180 \Omega = 72 \Omega$$

Next find the ac load line end points:

$$i_{c(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_c} = 150 \text{ mA} + \frac{9 \text{ V}}{72 \Omega} = 275 \text{ mA}$$

$$v_{ce(\text{cutoff})} = V_{CEQ} + I_{CQ}r_c = 9 \text{ V} + (150 \text{ mA})(72 \Omega) = 19.8 \text{ V}$$

Now determine the MPP value. With a supply voltage of 30 V:

$$MPP < 30 \text{ V}$$

MP will be the smaller value of:

$$I_{CQ}r_c = (150 \text{ mA})(72 \Omega) = 10.8 \text{ V}$$

or

$$V_{CEQ} = 9 \text{ V}$$

$$\text{Therefore, } MPP = 2(9 \text{ V}) = 18 \text{ V}$$

PRACTICE PROBLEM 12-2 Using Example 12-2, change R_E to 30Ω and find $i_{c(\text{sat})}$, $v_{ce(\text{cutoff})}$, and MPP.

12-3 Class A Operation

GOOD TO KNOW

The power gain A_p of a common-emitter amplifier equals $A_V \times A_I$.

Since A_I can be expressed as $A_I = A_V \times Z_{in}/R_L$, then A_p can be

expressed as $A_p = A_V \times A_V \times Z_{in}/R_L$ or $A_p = A^2_V \times Z_{in}/R_L$.

The VDB amplifier of Fig. 12-8a is a class A amplifier as long as the output signal is not clipped. With this kind of amplifier, collector current flows throughout the cycle. Stated another way, no clipping of the output signal occurs at any time during the cycle. Now, we discuss a few equations that are useful in the analysis of class A amplifiers.

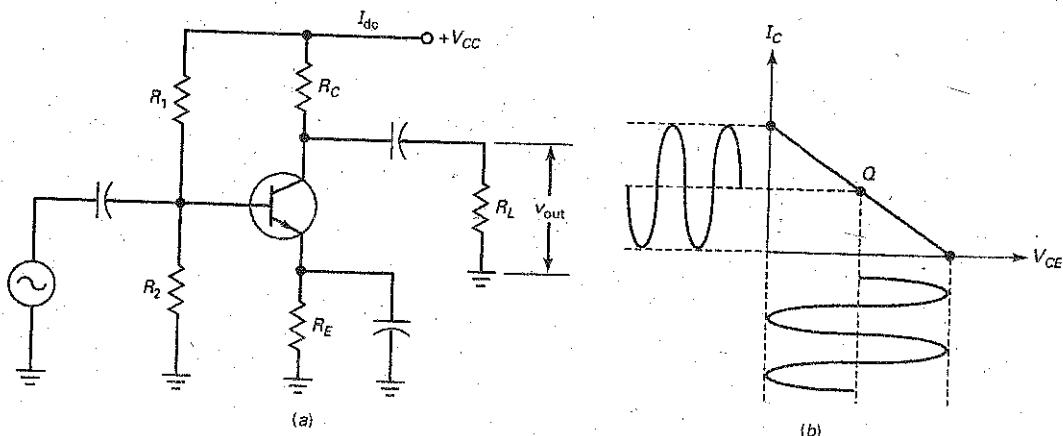
Power Gain

Besides voltage gain, any amplifier has a power gain, defined as:

$$A_p = \frac{P_{out}}{P_{in}} \quad (12-12)$$

In words, the power gain equals the ac output power divided by the ac input power.

Figure 12-8 (Class A amplifier.



For instance, if the amplifier of Fig. 12-8a has an output power of 10 mW and an input power of 10 μ W, it has a power gain of:

$$A_p = \frac{10 \text{ mW}}{10 \mu\text{W}} = 1000$$

Output Power

If we measure the output voltage of Fig. 12-8a in rms volts, the output power is given by

$$P_{\text{out}} = \frac{v_{\text{rms}}^2}{R_L} \quad (12-13)$$

Usually, we measure the output voltage in peak-to-peak volts with an oscilloscope. In this case, a more convenient equation to use for output power is:

$$P_{\text{out}} = \frac{v_{\text{pp}}^2}{8R_L} \quad (12-14)$$

The factor of 8 in the denominator occurs because $v_{\text{pp}} = 2\sqrt{2} v_{\text{rms}}$. When you square $2\sqrt{2}$, you get 8.

The maximum output power occurs when the amplifier is producing the maximum peak-to-peak output voltage, as shown in Fig. 12-8b. In this case, v_{pp} equals the maximum peak-to-peak output voltage and the maximum output power is:

$$P_{\text{out(max)}} = \frac{MPP^2}{8R_L} \quad (12-15)$$

Transistor Power Dissipation

When no signal drives the amplifier of Fig. 12-8a, the quiescent power dissipation is:

$$P_{DQ} = V_{CEO}I_{CQ} \quad (12-16)$$

This makes sense. It says that the quiescent power dissipation equals the dc voltage times the dc current.

When a signal is present, the power dissipation of a transistor decreases because the transistor converts some of the quiescent power to signal power. For this reason, the quiescent power dissipation is the worst case. Therefore, the power rating of a transistor in a class A amplifier must be greater than P_{DQ} ; otherwise, the transistor will be destroyed.

Current Drain

As shown in Fig. 12-8a, the dc voltage source has to supply a dc current I_{dc} to the amplifier. This dc current has two components: the biasing current through the voltage divider and the collector current through the transistor. The dc current is called the **current drain** of the stage. If you have a multistage amplifier, you have to add the individual current drains to get the total current drain.

Efficiency

The dc power supplied to an amplifier by the dc source is:

$$P_{dc} = V_{CC}I_{dc} \quad (12-17)$$

To compare the design of power amplifiers, we can use the **efficiency**, defined by:

$$\eta = \frac{P_{\text{out}}}{P_{dc}} \times 100\% \quad (12-18)$$

GOOD TO KNOW

Efficiency can also be defined as the amplifier's ability to convert its dc input power to useful ac output power.

This equation says that the efficiency equals the ac output power divided by the dc input power.

The efficiency of any amplifier is between 0 and 100 percent. Efficiency gives us a way to compare two different designs because it indicates how well an amplifier converts the dc input power to ac output power. The higher the efficiency, the better the amplifier is at converting dc power to ac power. This is important in battery-operated equipment because high efficiency means that the batteries last longer.

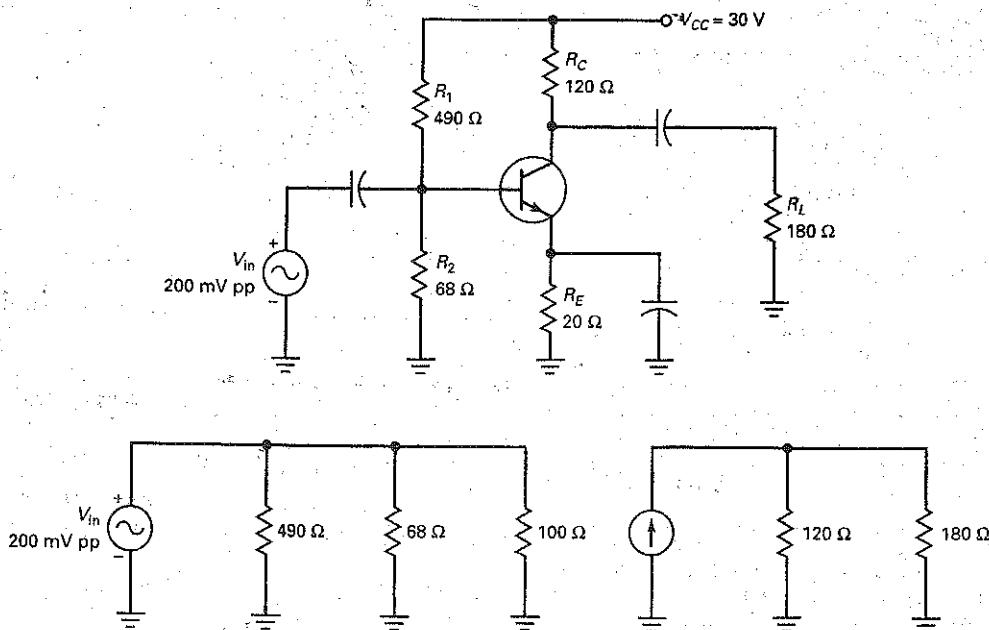
Since all resistors except the load resistor waste power, the efficiency is less than 100 percent in a class A amplifier. In fact, it can be shown that the maximum efficiency of a class A amplifier with a dc collector resistance and a separate load resistance is 25 percent.

In some applications, the low efficiency of class A is acceptable. For instance, the small-signal stages near the front of a system usually work fine with low efficiency because the dc input power is small. In fact, if the final stage of a system needs to deliver only a few hundred milliwatts, the current drain on the power supply may still be low enough to accept. But when the final stage needs to deliver watts of power, the current drain usually becomes too large with class A operation.

Example 12-3

If the peak-to-peak output voltage is 18 V and the input impedance of the base is 100 Ω , what is the power gain in Fig. 12-9a?

Figure 12-9 Example.



SOLUTION As shown in Fig. 12-9b:

$$z_{in(stage)} = 490 \Omega \parallel 68 \Omega \parallel 100 \Omega = 37.4 \Omega$$

The ac input power is:

$$P_{in} = \frac{(200 \text{ mV})^2}{8(37.4)} = 133.7 \mu\text{W}$$

The ac output power is:

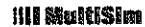
$$P_{out} = \frac{(18 \text{ V})^2}{8(180 \Omega)} = 225 \text{ mW}$$

The power gain is:

$$A_p = \frac{225 \text{ mW}}{133.7 \mu\text{W}} = 1683$$

PRACTICE PROBLEM 12-3 In Fig. 12-9a, if R_L is 120Ω and the peak-to-peak output voltage equals 12 V, what is the power gain?

Example 12-4



What is the transistor power dissipation and efficiency of Fig. 12-9a?

SOLUTION The dc emitter current is:

$$I_E = \frac{3 \text{ V}}{20 \Omega} = 150 \text{ mA}$$

The dc collector voltage is:

$$V_C = 30 \text{ V} - (150 \text{ mA})(120 \Omega) = 12 \text{ V}$$

and the dc collector-emitter voltage is:

$$V_{CEQ} = 12 \text{ V} - 3 \text{ V} = 9 \text{ V}$$

The transistor power dissipation is:

$$P_{DQ} = V_{CEQ} I_{CQ} = (9 \text{ V})(150 \text{ mA}) = 1.35 \text{ W}$$

To find the stage efficiency:

$$I_{bias} = \frac{30 \text{ V}}{490 \Omega + 68 \Omega} = 53.8 \text{ mA}$$

$$I_{dc} = I_{bias} + I_{CQ} = 53.8 \text{ mA} + 150 \text{ mA} = 203.8 \text{ mA}$$

The dc input power to the stage is:

$$P_{dc} = V_{CC} I_{dc} = (30 \text{ V})(203.8 \text{ mA}) = 6.11 \text{ W}$$

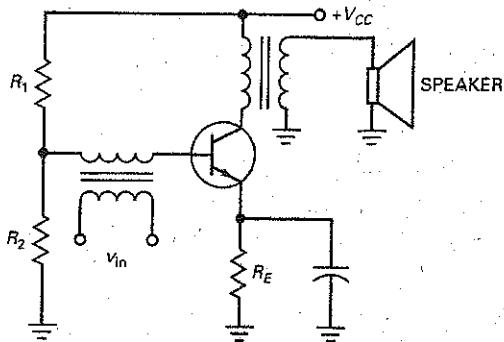
Since the output power (found in Example 12-3) is 225 mW, the efficiency of the stage is:

$$\eta = \frac{225 \text{ mW}}{6.11 \text{ W}} \times 100\% = 3.68\%$$

Example 12-5

Describe the action of Fig. 12-10.

Figure 12-10 Class A power amplifier.



SOLUTION This is a class A power amplifier driving a loudspeaker. The amplifier uses voltage-divider bias, and the ac input signal is transformer-coupled to the base. The transistor produces voltage and power gain to drive the loudspeaker through the output transformer.

A small speaker with an impedance of 3.2Ω needs only 100 mW in order to operate. A slightly larger speaker with an impedance of 8Ω needs 300 to 500 mW for proper operation. Therefore, a class A power amplifier like Fig. 12-10 may be adequate if all you need is a few hundred milliwatts of output power. Since the load resistance is also the ac collector resistance, the efficiency of this class A amplifier is higher than that of the class A amplifier discussed earlier. Using the impedance-reflecting ability of the transformer, the speaker load resistance appears $\left(\frac{N_P}{N_S}\right)^2$ times larger at the collector. If the transformer's turns ratio were 10:1, a 32Ω speaker would appear as 320Ω at the collector.

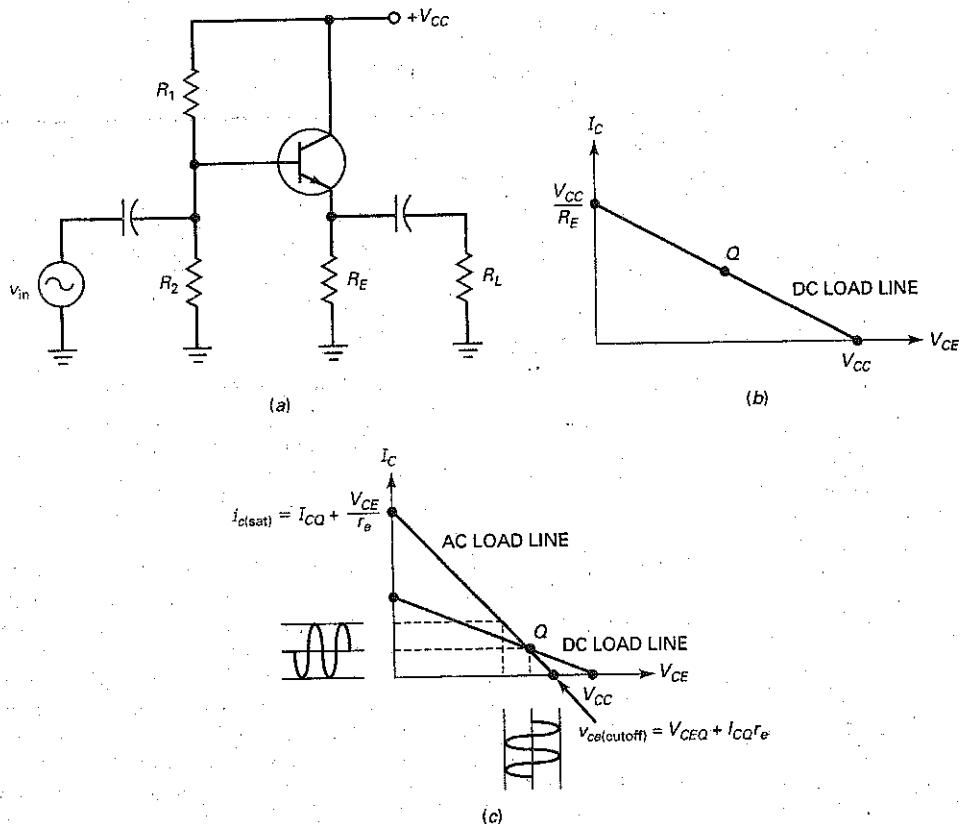
The class A amplifier discussed earlier had a separate collector resistance R_C and a separate load resistance R_L . The best you can do in this case is to match the impedances, $R_L = R_C$, to get a maximum efficiency of 25 percent. When the load resistance becomes the ac collector resistor, as shown in Fig. 12-10, it receives twice as much output power, and the maximum efficiency increases to 50 percent.

PRACTICE PROBLEM 12-5 In Fig. 12-10, what resistance would an 8Ω speaker appear to the collector as, if the transformer's turns ratio were 5 : 1?

Emitter-Follower Power Amplifier

When the emitter follower is used as class A power amplifier at the end of a system, a designer will usually locate the Q point at the center of the ac load line to get maximum peak-to-peak (MPP) output.

Figure 12-11 DC and ac load lines.



In Fig. 12-11a, large values of \$R_2\$ will saturate the transistor, producing a saturation current of:

$$I_{C(sat)} = \frac{V_{CC}}{R_E} \quad (12-19)$$

Small values of \$R_2\$ will drive the transistor into cutoff, producing a cutoff voltage of:

$$V_{CE(cutoff)} = V_{CC} \quad (12-20)$$

Fig. 12-11b shows the dc load line with the \$Q\$ point.

In Fig. 12-11a, the ac emitter resistance is less than the dc emitter resistance. Therefore, when an ac signal comes in, the instantaneous operating point moves along the ac load line of Fig. 12-11c. The peak-to-peak sinusoidal current and voltage are determined by the ac load line.

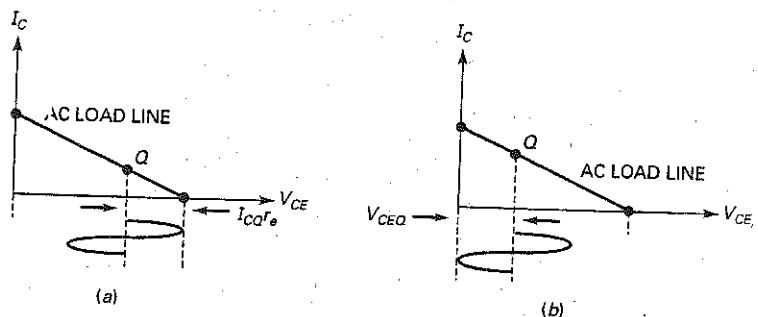
As shown in Fig. 12-11c, the ac load line end points are found by:

$$i_{c(sat)} = I_{CQ} + \frac{V_{CE}}{r_e} \quad (12-21)$$

and

$$V_{CE(cutoff)} = V_{CE} + I_{CQ} r_e \quad (12-22)$$

Figure 12-12 Maximum peak excursions.



Because the ac load line has a higher slope than the dc load line, the maximum peak-to-peak output is always less than the supply voltage. As with the class A CE amplifier, $MPP < V_{CC}$.

When the Q point is below the center of the ac load line, the maximum peak (MP) output is $I_{CQ}r_e$, as shown in Fig. 12-12a. On the other hand, if the Q point is above the center of the load line, the maximum peak output is V_{CEQ} , as shown in Fig. 12-12b.

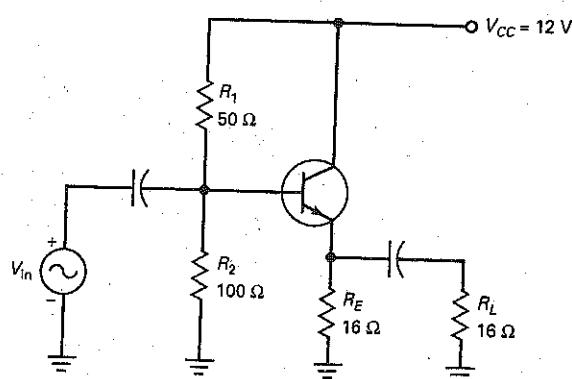
As you can see, determining the MPP value for an emitter-follower amplifier is essentially the same as for a CE amplifier. The difference is the need to use the emitter ac resistance, r_e , instead of the collector ac resistance, r_c . To increase the output power level, the emitter follower may also be connected in a Darlington configuration.

Example 12-6

III Multisim

What are the values of I_{CQ} , V_{CEQ} , and r_e in Fig. 12-13?

Figure 12-13 Emitter-follower power amplifier.



SOLUTION.

$$I_{CQ} = \frac{8 \text{ V} - 0.7 \text{ V}}{16 \Omega} = 456 \text{ mA}$$

$$V_{CEQ} = 12 \text{ V} - 7.3 \text{ V} = 4.7 \text{ V}$$

and

$$r_e = 16 \Omega \parallel 16 \Omega = 8 \Omega$$

PRACTICE PROBLEM 12-6 In Fig. 12-13, change R_1 to 100Ω and find I_{CQ} , V_{CEQ} , and r_e .

Example 12-7

Determine the ac saturation and cutoff points in Fig. 12-13. Also, find the circuit's MPP output voltage.

SOLUTION From Example 12-6, the dc Q point is:

$$I_{CQ} = 456 \text{ mA} \quad \text{and} \quad V_{CEQ} = 4.7 \text{ V}$$

The ac load line saturation and cutoff points are found by:

$$r_e = R_C \parallel R_L = 16 \Omega \parallel 16 \Omega = 8 \Omega$$

$$i_{c(\text{sat})} = I_{CQ} + \frac{V_{CE}}{r_e} = 456 \text{ mA} + \frac{4.7 \text{ V}}{8 \Omega} = 1.04 \text{ A}$$

$$v_{ce(\text{cutoff})} = V_{CEQ} + I_{CQ}r_e = 4.7 \text{ V} + (456 \text{ mA})(8 \Omega) = 8.35 \text{ V}$$

MPP is found by determining the smaller value of:

$$\text{MPP} = I_{CQ}r_e = (456 \text{ mA})(8 \Omega) = 3.65 \text{ V}$$

or

$$\text{MP} = V_{CEQ} = 4.7 \text{ V}$$

$$\text{Therefore, MPP} = 2(3.65 \text{ V}) = 7.3 \text{ V}_{\text{pp}}$$

PRACTICE PROBLEM 12-7 In Fig. 12-13, if $R_1 = 100 \Omega$, solve for its MPP value.

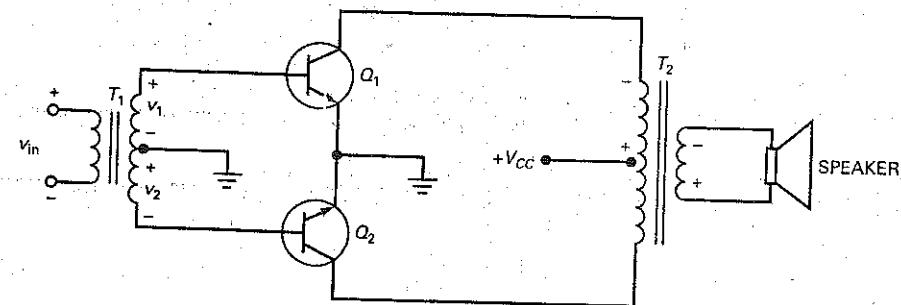
12-4 Class B Operation

Class A is the common way to run a transistor in linear circuits because it leads to the simplest and most stable biasing circuits. But class A is not the most efficient way to operate a transistor. In some applications, like battery-powered systems, current drain and stage efficiency become important considerations in the design. This section introduces the basic idea of class B operation.

Push-Pull Circuit

Figure 12-14 shows a basic class B amplifier. When a transistor operates as class B, it clips off half a cycle. To avoid the resulting distortion, we can use two

Figure 12-14 Class B push-pull amplifier.



transistors in a push-pull arrangement like that of Fig. 12-14. **Push-pull** means that one transistor conducts for half a cycle while the other is off, and vice versa.

Here is how the circuit works: On the positive half cycle of input voltage, the secondary winding of T_1 has voltage v_1 and v_2 , as shown. Therefore, the upper transistor conducts and the lower one cuts off. The collector current through Q_1 flows through the upper half of the output primary winding. This produces an amplified and inverted voltage, which is transformer-coupled to the loudspeaker.

On the next half cycle of input voltage, the polarities reverse. Now, the lower transistor turns on and the upper transistor turns off. The lower transistor amplifies the signal, and the alternate half cycle appears across the loudspeaker.

Since each transistor amplifies one-half of the input cycle, the loudspeaker receives a complete cycle of the amplified signal.

Advantages and Disadvantages

Since there is no bias in Fig. 12-14, each transistor is at cutoff when there is no input signal, an advantage because there is no current drain when the signal is zero.

Another advantage is improved efficiency where there is an input signal. The maximum efficiency of a class B push-pull amplifier is 78.5 percent, so a class B push-pull power amplifier is more commonly used for an output stage than a class A power amplifier.

The main disadvantage of the amplifier shown in Fig. 12-14 is the use of transformers. Audio transformers are bulky and expensive. Although widely used at one time, a transformer-coupled amplifier like Fig. 12-14 is no longer popular. Newer designs have eliminated the need for transformers in most applications.

12-5 Class B Push-Pull Emitter Follower

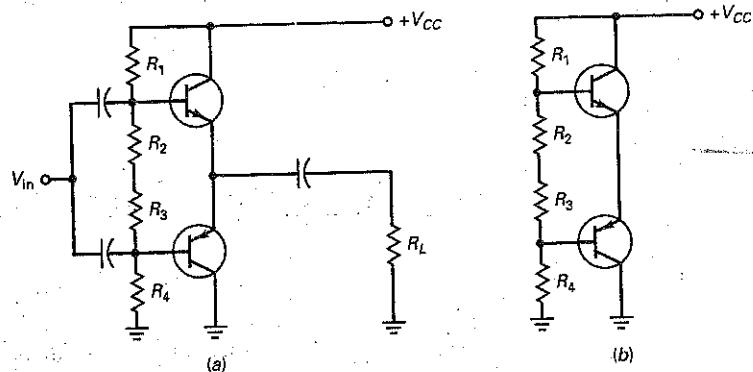
Class B operation means that the collector current flows for only 180° of the ac cycle. For this to occur, the Q point is located at cutoff on both the dc and the ac load lines. The advantage of class B amplifiers is lower current drain and higher stage efficiency.

Push-Pull Circuit

Figure 12-15a shows one way to connect a class B push-pull emitter follower. Here, we have an *npn* emitter follower and a *pnp* emitter follower connected in a push-pull arrangement.

Let's begin the analysis with the dc equivalent circuit of Fig. 12-15b. The designer selects biasing resistors to set the Q point at cutoff. This biases the

Figure 12-15 Class B push-pull emitter follower: (a) complete circuit; (b) dc equivalent circuit.



emitter diode of each transistor between 0.6 and 0.7 V, so that it is on the verge of conduction. Ideally:

$$I_{CQ} = 0$$

Because the biasing resistors are equal, each emitter diode is biased with the same value of voltage. As a result, half the supply voltage is dropped across each transistor's collector-emitter terminals. That is:

$$V_{CEQ} = \frac{V_{CC}}{2} \quad (12-23)$$

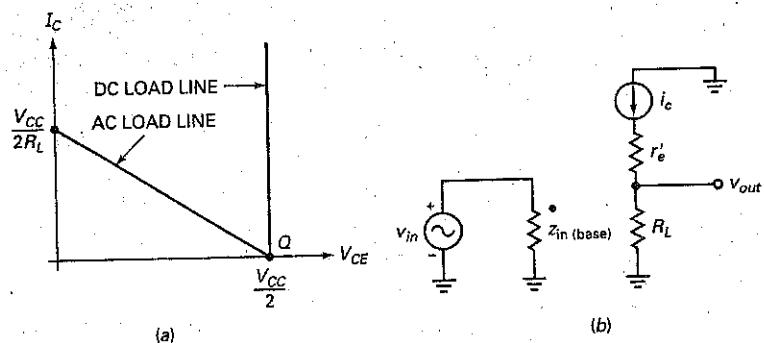
DC Load Line

Since there is no dc resistance in the collector or emitter circuits of Fig. 12-15b, the dc saturation current is infinite. This means that the dc load line is vertical, as shown in Fig. 12-16a. If you think that this is a dangerous situation, you are right. The most difficult thing about designing a class B amplifier is setting up a stable *Q* point at cutoff. Any significant decrease in V_{BE} with temperature can move the *Q* point up the dc load line to dangerously high currents. For the moment, assume that the *Q* point is rock-solid at cutoff, as shown in Fig. 12-16a.

AC Load Line

Figure 12-16a shows the ac load line. When either transistor is conducting, its operating point moves up along the ac load line. The voltage swing of the

Figure 12-16 (a) DC and ac load lines; (b) ac equivalent circuit.



conducting transistor can go all the way from cutoff to saturation. On the alternate half cycle, the other transistor does the same thing. This means that the maximum peak-to-peak output is:

$$MPP = V_{CC} \quad (12-24)$$

AC Analysis

Figure 12-16b shows the ac equivalent of the conducting transistor. This is almost identical to the class A emitter follower. Ignoring r'_e , the voltage gain is:

$$Av \approx 1 \quad (12-25)$$

and the input impedance of the base is:

$$Z_{in(base)} \approx \beta R_L \quad (12-26)$$

Overall Action

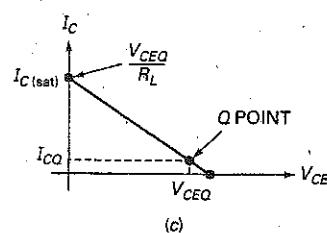
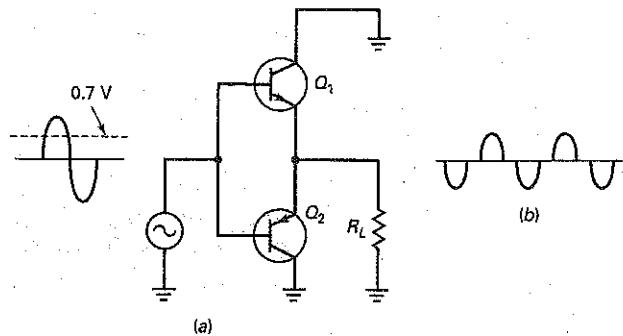
On the positive half cycle of input voltage, the upper transistor of Fig. 12-15a conducts and the lower one cuts off. The upper transistor acts like an ordinary emitter follower, so that the output voltage approximately equals the input voltage.

On the negative half cycle of input voltage, the upper transistor cuts off and the lower transistor conducts. The lower transistor acts like an ordinary emitter follower and produces a load voltage approximately equal to the input voltage. The upper transistor handles the positive half cycle of input voltage, and the lower transistor takes care of the negative half cycle. During either half cycle, the source sees a high input impedance looking into either base.

Crossover Distortion

Figure 12-17a shows the ac equivalent circuit of a class B push-pull emitter follower. Suppose that no bias is applied to the emitter diodes. Then, the incoming ac

Figure 12-17 (a) AC equivalent circuit; (b) crossover distortion; (c) Q point is slightly above cutoff.



GOOD TO KNOW

Some power amplifiers are biased to operate as class AB amplifiers to improve the linearity of the output signal. A class AB amplifier has a conduction angle of roughly 210° . The improved linearity of the output signal does not come without a price, however—a reduction in the circuit's efficiency.

voltage has to rise to about 0.7 V to overcome the barrier potential of the emitter diodes. Because of this, no current flows through Q_1 when the signal is less than 0.7 V.

The action is similar on the other half cycle. No current flows through Q_2 until the ac input voltage is more negative than -0.7 V. For this reason, if no bias is applied to the emitter diodes, the output of a class B push-pull emitter follower looks like Fig. 12-17b.

Because of clipping between half cycles, the output is distorted. Since the clipping occurs between the time one transistor cuts off and the other one comes on, we call it **crossover distortion**. To eliminate crossover distortion, we need to apply a slight forward bias to each emitter diode. This means locating the Q point slightly above cutoff, as shown in Fig. 12-17c. As a guide, an I_{CQ} from 1 to 5 percent of $I_{C(sat)}$ is enough to eliminate crossover distortion.

Class AB

In Fig. 12-17c, the slight forward bias implies that the conduction angle will be slightly greater than 180° because the transistor will conduct for a bit more than half a cycle. Strictly speaking, we no longer have class B operation. Because of this, the operation is sometimes referred to as **class AB**, defined as a conduction angle between 180° and 360° . But it is barely class AB. For this reason, many people still refer to the circuit as a *class B push-pull amplifier* because the operation is class B to a close approximation.

Power Formulas

The formulas shown in Table 12-1 apply to all classes of operation including class B push-pull operation.

When using these formulas to analyze a class B/AB push-pull emitter follower, remember that the class B/AB push-pull amplifier has the ac load line and waveforms of Fig. 12-18a. Each transistor supplies half of a cycle.

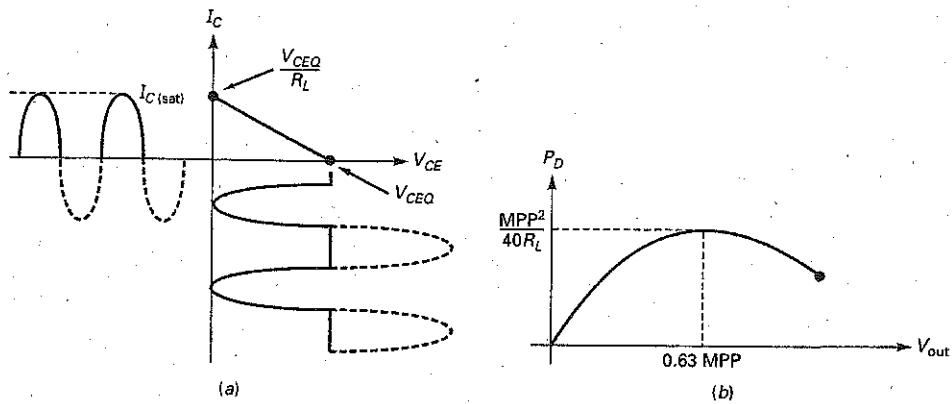
Transistor Power Dissipation

Ideally, the transistor power dissipation is zero when there is no input signal because both transistors are cut off. If there is a slight forward bias to prevent crossover distortion, the quiescent power dissipation in each transistor is still very small.

Table 12-1 | Amplifier Power Formulas

Equation	Value
$A_p = \frac{P_{out}}{P_{in}}$	Power gain
$P_{out} = \frac{V_{out}^2}{8R_L}$	AC output power
$P_{out(max)} = \frac{MPP^2}{8R_L}$	Maximum ac output power
$P_{dc} = V_{CC}I_{dc}$	DC input power
$\eta = \frac{P_{out}}{P_{dc}} \times 100\%$	Efficiency

Figure 12-18 (a) Class B load line; (b) transistor power dissipation.



When an input signal is present, the transistor power dissipation becomes significant. The transistor power dissipation depends on how much of the ac load line is used. The maximum transistor power dissipation of each transistor is:

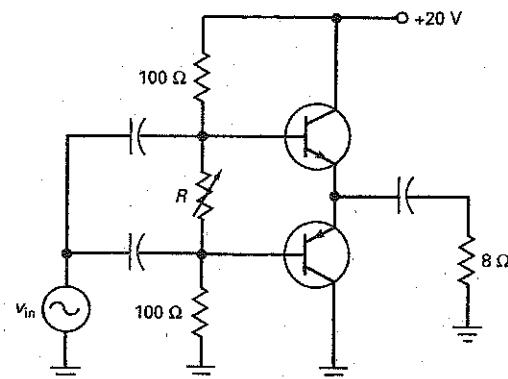
$$P_{D(\max)} = \frac{MPP^2}{40R_L} \quad (12-27)$$

Figure 12-18b shows how the transistor power dissipation varies according to the peak-to-peak output voltage. As indicated, P_D reaches a maximum when the peak-to-peak output is 63 percent of MPP. Since this is the worst case, each transistor in a class B/AB push-pull amplifier must have a power rating of at least $MPP^2/40R_L$.

Example 12-8

The adjustable resistor of Fig. 12-19 sets both emitter diodes on the verge of conduction. What is the maximum transistor power dissipation? The maximum output power?

Figure 12-19 Example.



SOLUTION The maximum peak-to-peak output is:

$$MPP = V_{CC} = 20 \text{ V}$$

With Eq. (12-27):

$$P_{D(\max)} = \frac{MPP^2}{40R_L} = \frac{(20 \text{ V})^2}{40(8 \Omega)} = 1.25 \text{ W}$$

The maximum output power is:

$$P_{out(\max)} = \frac{MPP^2}{8R_L} = \frac{(20 \text{ V})^2}{8(8 \Omega)} = 6.25 \text{ W}$$

PRACTICE PROBLEM 12-8 In Fig. 12-19, change V_{CC} to +30 V and calculate $P_{D(\max)}$ and $P_{out(\max)}$.

Example 12-9

If the adjustable resistance is 15Ω , what is the efficiency in the preceding example?

SOLUTION The dc current through the biasing resistors is:

$$I_{bias} \approx \frac{20 \text{ V}}{215 \Omega} = 0.093 \text{ A}$$

Next, we need to calculate the dc current through the upper transistor. Here is how to do it: As shown in Fig. 12-18a, the saturation current is:

$$I_{C(sat)} = \frac{V_{CEO}}{R_L} = \frac{10 \text{ V}}{8 \Omega} = 1.25 \text{ A}$$

The collector current in the conducting transistor is a half-wave signal with a peak of $I_{C(sat)}$. Therefore, it has an average value of:

$$I_{av} = \frac{I_{C(sat)}}{\pi} = \frac{1.25 \text{ A}}{\pi} = 0.398 \text{ A}$$

The total current drain is:

$$I_{dc} = 0.093 \text{ A} + 0.398 \text{ A} = 0.491 \text{ A}$$

The dc input power is:

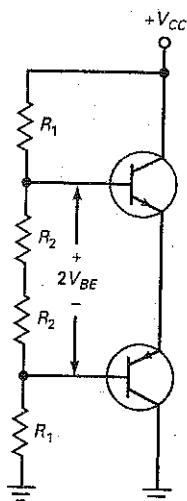
$$P_{dc} = (20 \text{ V})(0.491 \text{ A}) = 9.82 \text{ W}$$

The efficiency of the stage is:

$$\eta = \frac{P_{out}}{P_{dc}} \times 100\% = \frac{6.25 \text{ W}}{9.82 \text{ W}} \times 100\% = 63.6\%$$

PRACTICE PROBLEM 12-9 Repeat Example 12-9 using +30 V for V_{CC} .

Figure 12-20 Voltage-divider bias of class B push-pull amplifier.



12-6 Biasing Class B/AB Amplifiers

As mentioned earlier, the hardest thing about designing a class B/AB amplifier is setting up a stable Q point near cutoff. This section discusses the problem and its solution.

Voltage-Divider Bias

Figure 12-20 shows voltage-divider bias for a class B/AB push-pull circuit. The two transistors have to be complementary; that is, they must have similar V_{BE} curves, maximum ratings, and so forth. For instance, the 2N3904 and 2N3906 are complementary, the first being an *npn* transistor and the second being a *pnp*. They have similar V_{BE} curves, maximum ratings, and so on. Complementary pairs like these are available for almost any class B/AB push-pull design.

To avoid crossover distortion in Fig. 12-20, we set the Q point slightly above cutoff, with the correct V_{BE} somewhere between 0.6 and 0.7 V. But here is the major problem: The collector current is very sensitive to changes in V_{BE} . Data sheets indicate that an increase of 60 mV in V_{BE} produces 10 times as much collector current. Because of this, an adjustable resistor is needed to set the correct Q point.

But an adjustable resistor does not solve the temperature problem. Even though the Q point may be perfect at room temperature, it will change when the temperature changes. As discussed earlier, V_{BE} decreases approximately 2 mV per degree rise. As the temperature increases in Fig. 12-20, the fixed voltage on each emitter diode forces the collector current to increase rapidly. If the temperature increases 30°, the collector current increases by a factor of 10 because the fixed bias is 60 mV too high. Therefore, the Q point is very unstable with voltage-divider bias.

The ultimate danger in Fig. 12-20 is **thermal runaway**. When the temperature increases, the collector current increases. As the collector current increases, the junction temperature increases even more, further reducing the correct V_{BE} . This escalating situation means that the collector current may "run away" by rising until excessive power destroys the transistor.

Whether or not thermal runaway takes place depends on the thermal properties of the transistor, how it is cooled, and the type of heat sink used. More often than not, voltage-divider bias like Fig. 12-20 will produce thermal runaway, which destroys the transistors.

Diode Bias

One way to avoid thermal runaway is with diode bias, shown in Fig. 12-21. The idea is to use **compensating diodes** to produce the bias voltage for the emitter diodes. For this scheme to work, the diode curves must match the V_{BE} curves of the transistors. Then, any increase in temperature reduces the bias voltage developed by the compensating diodes by just the right amount.

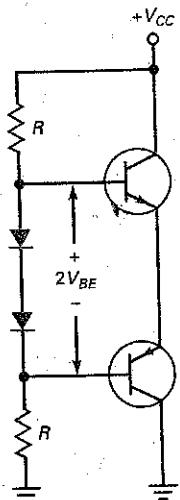
For instance, assume that a bias voltage of 0.65 V sets up 2 mA of collector current. If the temperature rises 30°C, the voltage across each compensating diode drops 60 mV. Since the required V_{BE} also decreases by 60 mV, the collector current remains fixed at 2 mA.

For diode bias to be immune to changes in temperature, the diode curves must match the V_{BE} curves over a wide temperature range. This is not easily done with discrete circuits because of the tolerance of components. But diode bias is easy to implement with integrated circuits because the diodes and transistors are on the same chip, which means that they have almost identical curves.

GOOD TO KNOW

In actual designs, the compensating diodes are mounted on the case of the power transistors so that, as the transistors heat up so do the diodes. The diodes are usually mounted to the power transistors with a nonconductive adhesive that has good thermal transfer characteristics.

Figure 12-21 Diode bias of class B push-pull amplifier.



With diode bias, the bias current through the compensating diodes of Fig. 12-21 is:

$$I_{\text{bias}} = \frac{V_{CC} - 2V_{BE}}{2R} \quad (12-28)$$

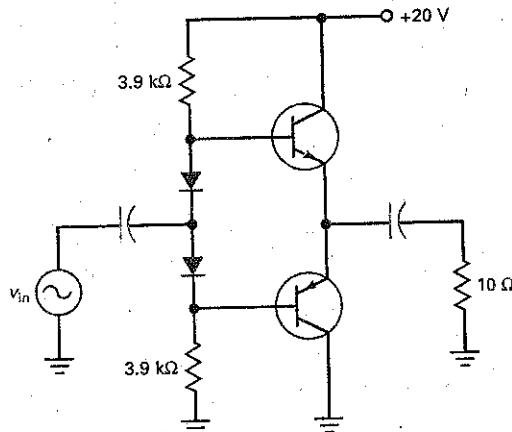
When the compensating diodes match the V_{BE} curves of the transistors, I_{CQ} has the same value as I_{bias} . (For details, see Sec. 17-7.) As mentioned earlier, I_{CQ} should be between 1 and 5 percent of $I_{C(\text{sat})}$ to avoid crossover distortion.

Example 12-10

Multisim

What is the quiescent collector current in Fig. 12-22? The maximum efficiency of the amplifier?

Figure 12-22 Example.



SOLUTION The bias current through the compensating diodes is:

$$I_{\text{bias}} = \frac{20 \text{ V} - 1.4 \text{ V}}{2(3.9 \text{ k}\Omega)} = 2.38 \text{ mA}$$

This is the value of the quiescent collector current, assuming that the compensating diodes match the emitter diodes.

The collector saturation current is:

$$I_{C(\text{sat})} = \frac{V_{CEQ}}{R_L} = \frac{10 \text{ V}}{10 \Omega} = 1 \text{ A}$$

The average value of the half-wave collector current is:

$$I_{\text{av}} = \frac{I_{C(\text{sat})}}{\pi} = \frac{1 \text{ A}}{\pi} = 0.318 \text{ A}$$

The total current drain is:

$$I_{\text{dc}} = 2.38 \text{ mA} + 0.318 \text{ A} = 0.32 \text{ A}$$

The dc input power is:

$$P_{dc} = (20 \text{ V})(0.32 \text{ A}) = 6.4 \text{ W}$$

The maximum ac output power is:

$$P_{out(max)} = \frac{MPP^2}{8R_L} = \frac{(20 \text{ V})^2}{8(10 \Omega)} = 5 \text{ W}$$

The efficiency of the stage is:

$$\eta = \frac{P_{out}}{P_{dc}} \times 100\% = \frac{5 \text{ W}}{6.4 \text{ W}} \times 100\% = 78.1\%$$

PRACTICE PROBLEM 12-10 Repeat Example 12-10 using +30 V for V_{CC} .

12-7 Class B/AB Driver

In the earlier discussion of the class B/AB push-pull emitter follower, the ac signal was capacitively coupled into the bases. This is not the preferred way to drive a class B/AB push-pull amplifier.

CE Driver

The stage that precedes the output stage is called a **driver**. Rather than capacitively couple into the output push-pull stage, we can use the direct-coupled CE driver shown in Fig. 12-23a. Transistor Q_1 is a current source that sets up the dc biasing current through the diodes. By adjusting R_2 , we can control the dc emitter current through R_4 . This means that Q_1 sources the biasing current through the compensating diodes.

When an ac signal drives the base of Q_1 , it acts like a swamped amplifier. The amplified and inverted ac signal at the Q_1 collector drives the bases of Q_2 and Q_3 . On the positive half cycle, Q_2 conducts and Q_3 cuts off. On the negative half cycle, Q_2 cuts off and Q_3 conducts. Because the output coupling capacitor is an ac short, the ac signal is coupled to the load resistance.

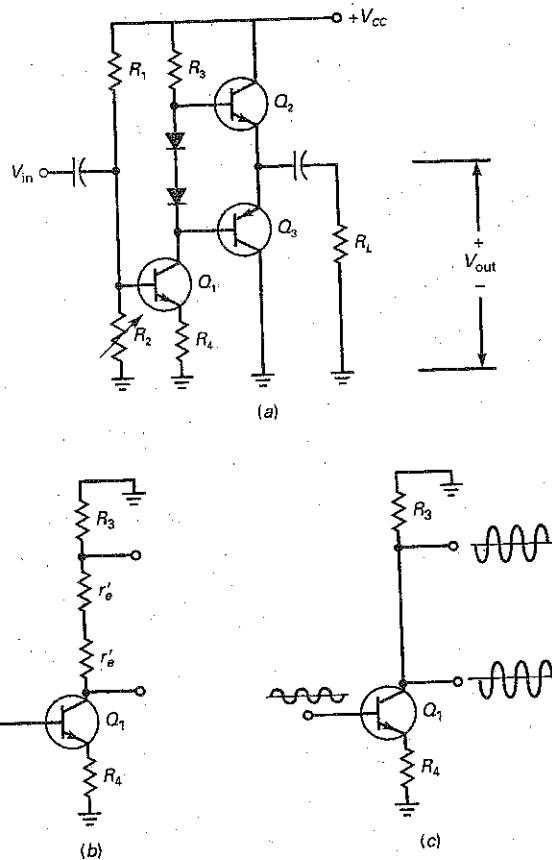
Figure 12-23b shows the ac equivalent circuit of the CE driver. The diodes are replaced by their ac emitter resistances. In any practical circuit, r'_e is at least 100 times smaller than R_3 . Therefore, the ac equivalent circuit simplifies to Fig. 12-23c.

Now, we can see that the driver stage is a swamped amplifier whose amplified and inverted output drives both bases of the output transistors with the same signal. Often, the input impedance of the output transistors is very high, and we can approximate the voltage gain of the driver by:

$$A_V = \frac{R_3}{R_4}$$

In short, the driver stage is a swamped voltage amplifier that produces a large signal for the output push-pull amplifier.

Figure 12-23 (a) Direct-coupled CE driver; (b) ac equivalent circuit; (c) simplified ac equivalent circuit.



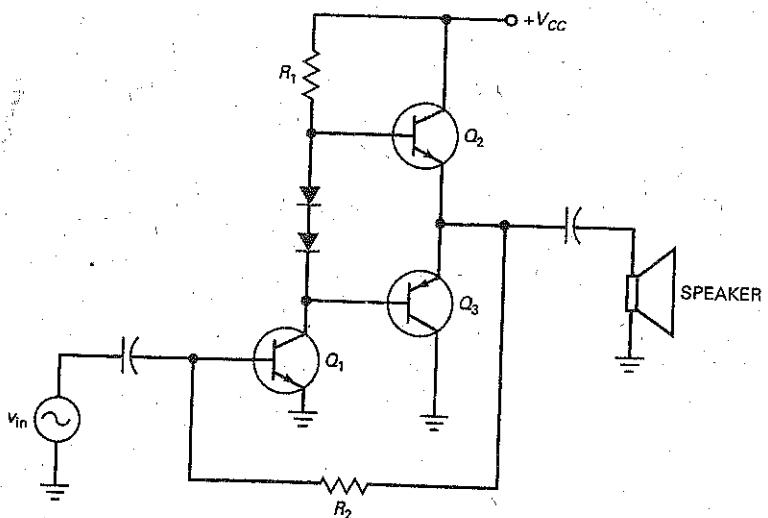
Two-Stage Negative Feedback

Figure 12-24 is another example of using a large-signal CE stage to drive a class B/AB push-pull emitter follower. The input signal is amplified and inverted by the Q_1 driver. The push-pull stage then provides the current gain needed to drive the low-impedance loudspeaker. Notice that the CE driver has its emitter connected to ground. As a result, this driver has more voltage gain than the driver of Fig. 12-23a.

The resistance R_2 does two useful things: First, since it is connected to a dc voltage of $+V_{CC}/2$, this resistance provides the dc bias for Q_1 . Second, R_2 produces negative feedback for the ac signal. Here's why: A positive-going signal on the base of Q_1 produces a negative-going signal on the Q_1 collector. The output of the emitter follower is therefore negative-going. When fed back through R_2 to the Q_1 base, this returning signal opposes the original input signal. This is negative feedback, which stabilizes the bias and the voltage gain of the overall amplifier.

Integrated circuit (IC) audio power amplifiers are often used in low- to medium-power applications. These amplifiers, such as a LM380 IC, contain class AB biased output transistors and will be discussed in Chap. 18.

Figure 12-24 Two-stage negative feedback to CE driver.



12-8 Class C Operation

With class B, we need to use a push-pull arrangement. That's why almost all class B amplifiers are push-pull amplifiers. With class C, we need to use a resonant circuit for the load. This is why almost all class C amplifiers are tuned amplifiers.

Resonant Frequency

With class C operation, the collector current flows for less than half a cycle. A parallel resonant circuit can filter the pulses of collector current and produce a pure sine wave of output voltage. The main application for class C is with tuned RF amplifiers. The maximum efficiency of a tuned class C amplifier is 100 percent.

Figure 12-25a shows a tuned RF amplifier. The ac input voltage drives the base, and an amplified output voltage appears at the collector. The amplified and inverted signal is then capacitively coupled to the load resistance. Because of the parallel resonant circuit, the output voltage is maximum at the resonant frequency, given by:

$$f_r = \frac{1}{2\pi\sqrt{LC}} \quad (12-29)$$

On either side of the resonant frequency f_r , the voltage gain drops off as shown in Fig. 12-25b. For this reason, a tuned class C amplifier is always intended to amplify a narrow band of frequencies. This makes it ideal for amplifying radio and television signals because each station or channel is assigned a narrow band of frequencies on both sides of a center frequency.

The class C amplifier is unbiased, as shown in the dc equivalent circuit of Fig. 12-25c. The resistance R_s in the collector circuit is the series resistance of the inductor.

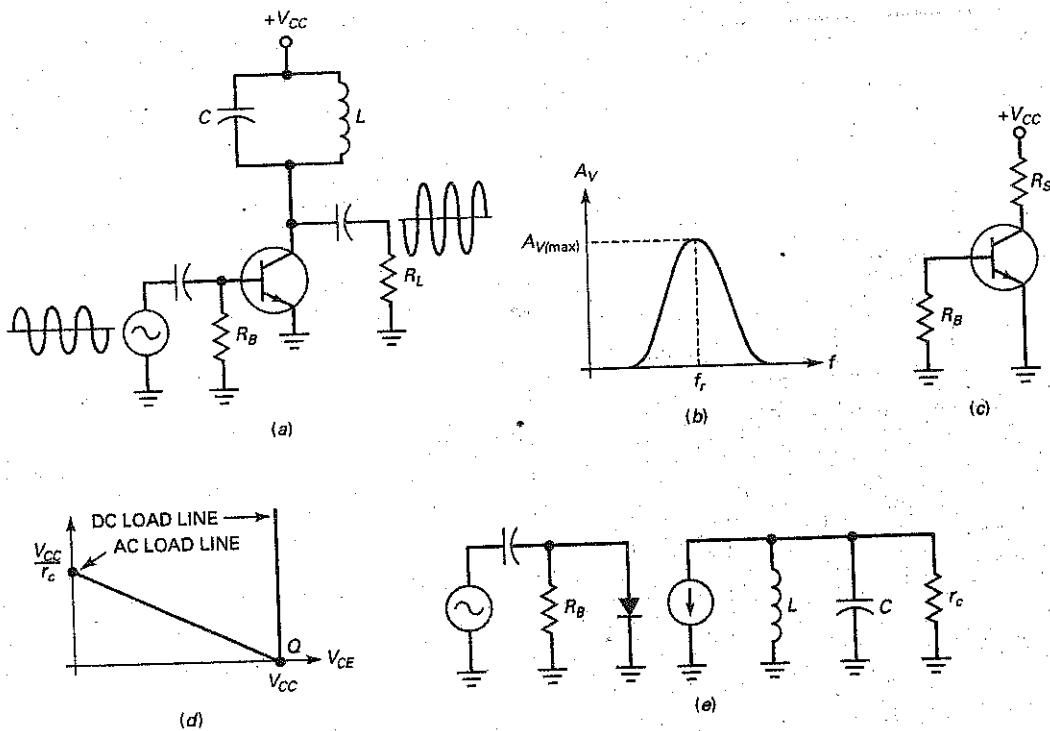
Load Lines

Figure 12-25d shows the two load lines. The dc load line is approximately vertical because the winding resistance R_s of an RF inductor is very small. The dc load

GOOD TO KNOW

Most class C amplifiers are designed so that the peak value of input voltage is just sufficient to drive the transistor into saturation.

Figure 12-25 (a) Tuned class C amplifier; (b) voltage gain versus frequency; (c) dc equivalent circuit is unbiased; (d) two load lines; (e) ac equivalent circuit.



line is not important because the transistor is unbiased. What is important is the ac load line. As indicated, the Q point is at the lower end of the ac load line. When an ac signal is present, the instantaneous operating point moves up the ac load line toward the saturation point. The maximum pulse of collector current is given by the saturation current V_{CC}/r_c .

DC Clamping of Input Signal

Figure 12-25e is the ac equivalent circuit. The input signal drives the emitter diode, and the amplified current pulses drive the resonant tank circuit. In a tuned-class C amplifier the input capacitor is part of a negative dc clamer. For this reason, the signal appearing across the emitter diode is negatively clamped.

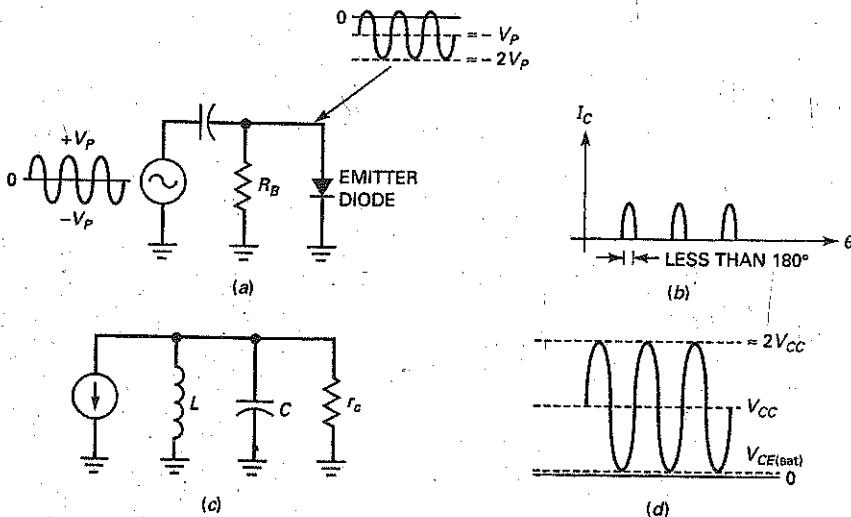
Figure 12-26a illustrates the negative clamping. Only the positive peaks of the input signal can turn on the emitter diode. For this reason, the collector current flows in brief pulses like those of Fig. 12-26b.

Filtering the Harmonics

Chapter 5 briefly discussed the concept of harmonics. The basic idea is this: A nonsinusoidal waveform like Fig. 12-26b is rich in harmonics, multiples of the input frequency. In other words, the pulses of Fig. 12-26b are equivalent to a group of sine waves with frequencies of $f, 2f, 3f, \dots, nf$.

The resonant tank circuit of Fig. 12-26c has a high impedance only at the fundamental frequency f . This produces a large voltage gain at the fundamental frequency. On the other hand, the tank circuit has a very low impedance to the

Figure 12-26 (a) Input signal is negatively clamped at base; (b) collector current flows in pulses; (c) ac collector circuit; (d) collector voltage waveform.



higher harmonics, producing very little voltage gain. This is why the voltage across the resonant tank looks almost like the pure sine wave of Fig. 12-26d. Since all higher harmonics are filtered, only the fundamental frequency appears across the tank circuit.

Troubleshooting

Since the tuned class C amplifier has a negatively clamped input signal, you can use a high-impedance dc voltmeter to measure the voltage across the emitter diode. If the circuit is working correctly, you should read a negative voltage approximately equal to the peak of the input signal.

The voltmeter test just described is useful when an oscilloscope is not handy. If you have an oscilloscope, however, an even better test is to look across the emitter diode. You should see a negatively clamped waveform when the circuit is working properly.

Example 12-11

III Multisim

Describe the action of Fig. 12-27.

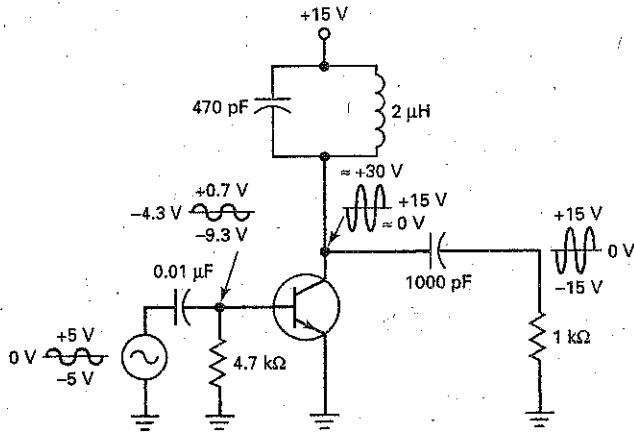
SOLUTION The circuit has a resonant frequency of:

$$f_r = \frac{1}{2\pi\sqrt{(2 \mu H)(470 \text{ pF})}} = 5.19 \text{ MHz}$$

If the input signal has this frequency, the tuned class C circuit will amplify the input signal.

In Fig. 12-27, the input signal has a peak-to-peak value of 10 V. The signal is negatively clamped at the base of the transistor with a positive peak of

Figure 12-27 Example.



+0.7 V and a negative peak of -9.3 V. The average base voltage is -4.3 V, which can be measured with a high-impedance dc voltmeter.

The collector signal is inverted because of the CE connection. The dc or average voltage of the collector waveform is +15 V, the supply voltage. Therefore, the peak-to-peak collector voltage is 30 V. This voltage is capacitively coupled to the load resistance. The final output voltage has a positive peak of +15 V and a negative peak of -15 V.

PRACTICE PROBLEM 12-11 Using Fig. 12-27, change the 470 pF capacitor to 560 pF and V_{CC} to +12 V. Solve the circuit for f_1 and V_{out} peak-to-peak.

12-9 Class C Formulas

A tuned class C amplifier is usually a narrowband amplifier. The input signal in a class C circuit is amplified to get large output power with an efficiency approaching 100 percent.

Bandwidth

As discussed in basic courses, the **bandwidth (BW)** of a resonant circuit is defined as:

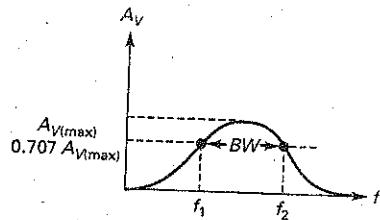
$$BW = f_2 - f_1 \quad (12-30)$$

where f_1 = lower half-power frequency

f_2 = upper half-power frequency

The half-power frequencies are identical to the frequencies at which the voltage gain equals 0.707 times the maximum gain, as shown in Fig. 12-28. The smaller BW is, the narrower the bandwidth of the amplifier.

Figure 12-28 Bandwidth.



With Eq. (12-30), it is possible to derive this new relation for bandwidth:

$$BW = \frac{f_0}{Q} \quad (12-31)$$

where Q is the quality factor of the circuit. Equation (12-31) says that the bandwidth is inversely proportional to Q . The higher the Q of the circuit, the smaller the bandwidth.

Class C amplifiers almost always have a circuit Q that is greater than 10. This means that the bandwidth is less than 10 percent of the resonant frequency. For this reason, class C amplifiers are narrowband amplifiers. The output of a narrowband amplifier is a large sinusoidal voltage at resonance with a rapid drop-off above and below resonance.

Current Dip at Resonance

When a tank circuit is resonant, the ac load impedance seen by the collector current source is maximum and purely resistive. Therefore, the collector current is minimum at resonance. Above and below resonance, the ac load impedance decreases and the collector current increases.

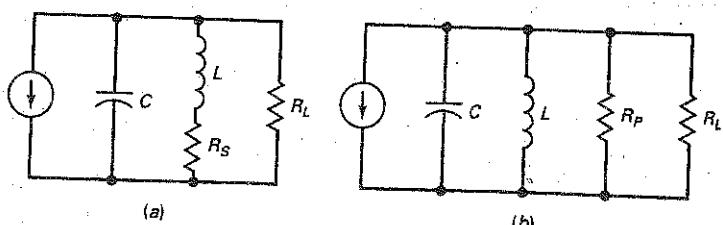
One way to tune a resonant tank is to look for a decrease in the dc current supplied to the circuit, as shown in Fig. 12-29. The basic idea is to measure the current I_{dc} from the power supply while tuning the circuit (varying either L or C). When the tank is resonant at the input frequency, the ammeter reading will dip to a minimum value. This indicates that the circuit is correctly tuned because the tank has a maximum impedance at this point.

AC Collector Resistance

Any inductor has a series resistance R_s , as indicated in Fig. 12-30a. The Q of the inductor is defined as:

$$Q_L = \frac{X_L}{R_s} \quad (12-32)$$

Figure 12-30 (a) Series equivalent resistance for inductor; (b) parallel equivalent resistance for inductor.



where Q_L = quality factor of coil

X_L = inductive reactance

R_S = coil resistance

Remember that this is the Q of the coil only. The overall circuit has a lower Q because it includes the effect of load resistance as well as coil resistance.

As discussed in basic ac courses, the series resistance of the inductor can be replaced by a parallel resistance R_P , as shown in Fig. 12-30b. When Q is greater than 10, this equivalent resistance is given by:

$$R_P = Q_L X_L \quad (12-33)$$

In Fig. 12-30b, X_L cancels X_C at resonance, leaving only R_P in parallel with R_L . Therefore, the ac resistance seen by the collector at resonance is:

$$r_c = R_P \parallel R_L \quad (12-34)$$

The Q of the overall circuit is given by:

$$Q = \frac{r_c}{X_L} \quad (12-35)$$

This circuit Q is lower than Q_L , the coil Q . In practical class C amplifiers, the Q of the coil is typically 50 or more, and the Q of the circuit is 10 or more. Since the overall Q is 10 or more, the operation is narrowband.

Duty Cycle

The brief turn-on of the emitter diode at each positive peak produces narrow pulses of collector current, as shown in Fig. 12-31a. With pulses like these, it is convenient to define the **duty cycle** as:

$$D = \frac{W}{T} \quad (12-36)$$

where D = duty cycle

W = width of pulse

T = period of pulses

For instance, if an oscilloscope displays a pulse width of $0.2 \mu s$ and a period of $1.6 \mu s$, the duty cycle is:

$$D = \frac{0.2 \mu s}{1.6 \mu s} = 0.125$$

The smaller the duty cycle, the narrower the pulses compared to the period. The typical class C amplifier has a small duty cycle. In fact, the efficiency of a class C amplifier increases as the duty cycle decreases.

Conduction Angle

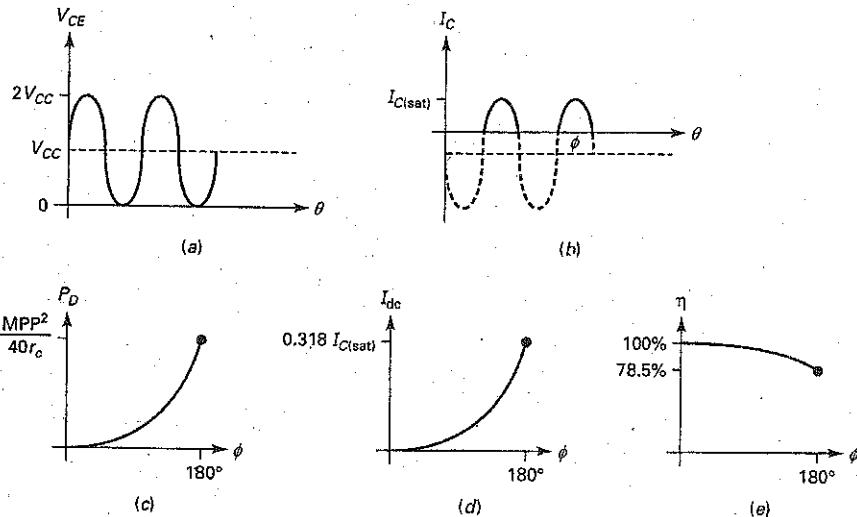
An equivalent way to state the duty cycle is by using the conduction angle ϕ , shown in Fig. 12-31b:

$$D = \frac{\phi}{360^\circ} \quad (12-37)$$

Figure 12-31 Duty cycle.



Figure 12-32 (a) Maximum output; (b) conduction angle; (c) transistor power dissipation; (d) current drain; (e) efficiency.



For instance, if the conduction angle is 180° , the duty cycle is:

$$D = \frac{180^\circ}{360^\circ} = 0.05$$

Transistor Power Dissipation

Figure 12-32a shows the ideal collector-emitter voltage in a class C transistor amplifier. In Fig. 12-32a, the maximum output is given by:

$$MPP = 2V_{CC} \quad (12-38)$$

Since the maximum voltage is approximately $2V_{CC}$, the transistor must have a V_{CEO} rating greater than $2V_{CC}$.

Figure 12-32b shows the collector current for a class C amplifier. Typically, the conduction angle ϕ is much less than 180° . Notice that the collector current reaches a maximum value of $I_{C(sat)}$. The transistor must have a peak current rating greater than this. The dotted parts of the cycle represent the off time of the transistor.

The power dissipation of the transistor depends on the conduction angle. As shown in Fig. 12-32c, the power dissipation increases with the conduction angle up to 180° . The maximum power dissipation of the transistor can be derived with calculus:

$$P_D = \frac{MPP^2}{40r_c} \quad (12-39)$$

Equation (12-39) represents the worst case. A transistor operating as class C must have a power rating greater than this or it will be destroyed. Under normal drive conditions, the conduction angle will be much less than 180° and the transistor power dissipation will be less than $MPP^2/40r_c$.

Stage Efficiency

The dc collector current depends on the conduction angle. For a conduction angle of 180° (a half-wave signal), the average or dc collector current is $0.318 I_{C(sat)}$. For smaller conduction angles, the dc collector current is less than this, as shown in

Fig. 12-32d. The dc collector current is the only current drain in a class C amplifier because it has no biasing resistors.

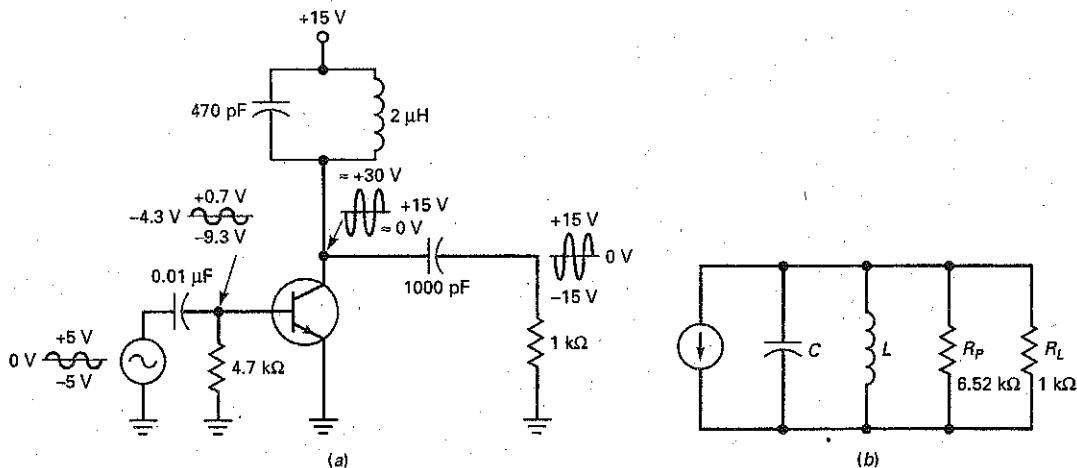
In a class C amplifier, most of the dc input power is converted into ac load power because the transistor and coil losses are small. For this reason, a class C amplifier has high stage efficiency.

Figure 12-32e shows how the optimum stage efficiency varies with conduction angle. When the angle is 180° , the stage efficiency is 78.5 percent, the theoretical maximum for a class B amplifier. When the conduction angle decreases, the stage efficiency increases. As indicated, class C has a maximum efficiency of 100 percent, approached at very small conduction angles.

Example 12-12

If $Q_L = 100$ in Fig. 12-33, what is the bandwidth of the amplifier?

Figure 12-33 Example.



SOLUTION At the resonant frequency (found in Example 12-11):

$$X_L = 2\pi f L = 2\pi(5.19 \text{ MHz})(2 \mu\text{H}) = 65.2 \Omega$$

With Eq. (12-33), the equivalent parallel resistance of the coil is:

$$R_P = Q_L X_L = (100)(65.2 \Omega) = 6.52 \text{ k}\Omega$$

This resistance is in parallel with the load resistance, as shown in Fig. 12-33b. Therefore, the ac collector resistance is:

$$r_c = 6.52 \text{ k}\Omega \parallel 1 \text{ k}\Omega = 867 \Omega$$

With Eq. (12-35), the Q of the overall circuit is:

$$Q = \frac{r_c}{X_L} = \frac{867 \Omega}{65.2 \Omega} = 13.3$$

Since the resonant frequency is 5.19 MHz, the bandwidth is:

$$BW = \frac{5.19 \text{ MHz}}{13.3} = 390 \text{ kHz}$$

Example 12-13

In Fig. 12-33a, what is the worst-case power dissipation?

SOLUTION The maximum peak-to-peak output is:

$$MPP = 2V_{CC} = 2(15 \text{ V}) = 30 \text{ V pp}$$

Equation (12-39) gives us the worst-case power dissipation of the transistor:

$$P_D = \frac{MPP^2}{40r_c} = \frac{(30 \text{ V})^2}{40(867 \Omega)} = 26 \text{ mW}$$

PRACTICE PROBLEM 12-13. In Fig. 12-33, if V_{CC} is +12 V, what is the worst case power dissipation?

GOOD TO KNOW

With integrated circuits, a maximum junction temperature cannot be specified because there are so many transistors. Therefore, ICs have a maximum device temperature or case temperature instead. For example, the μ A741 op amp IC has a power rating of 500 mW if it is in a metal package, 310 mW if it is in a dual-inline package, and 570 mW if it is in a flatpack.

Summary Table 12-1 illustrates the characteristics of class A, B/AB, and C amplifiers.

12-10 Transistor Power Rating

The temperature at the collector junction places a limit on the allowable power dissipation P_D . Depending on the transistor type, a junction temperature in the range of 150 to 200°C will destroy the transistor. Data sheets specify this maximum junction temperature as $T_{J(max)}$. For instance, the data sheet of a 2N3904 gives a $T_{J(max)}$ of 150°C; the data sheet of a 2N3719 specifies a $T_{J(max)}$ of 200°C.

Ambient Temperature

The heat produced at the junction passes through the transistor case (metal or plastic housing) and radiates to the surrounding air. The temperature of this air, known as the *ambient temperature*, is around 25°C, but it can get much higher on hot days. Also, the ambient temperature may be much higher inside a piece of electronic equipment.

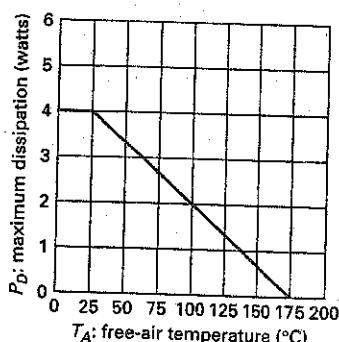
Derating Factor

Data sheets often specify the $P_{D(max)}$ of a transistor at an ambient temperature of 25°C. For instance, the 2N1936 has a $P_{D(max)}$ of 4 W for an ambient temperature of 25°C. This means that a 2N1936 used in a class A amplifier can have a quiescent power dissipation as high as 4 W. As long as the ambient temperature is 25°C or less, the transistor is within its specified power rating.

What do you do if the ambient temperature is greater than 25°C? You have to derate (reduce) the power rating. Data sheets sometimes include a *derating curve* like the one in Fig. 12-34. As you can see, the power rating decreases when the ambient temperature increases. For instance, at an ambient temperature of 100°C, the power rating is 2 W.

Some data sheets do not give a derating curve like the one in Fig. 12-34. Instead, they list a derating factor D . For instance, the derating factor of a 2N1936

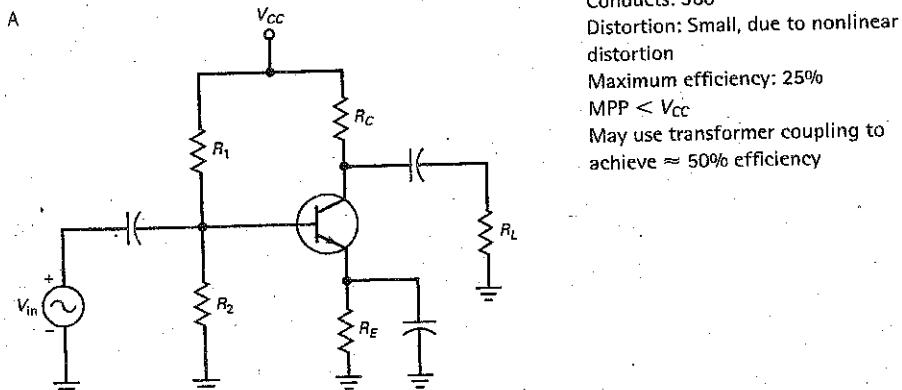
Figure 12-34 Power rating versus ambient temperature.



Summary Table 12-1

Amplifier Classes

Circuit



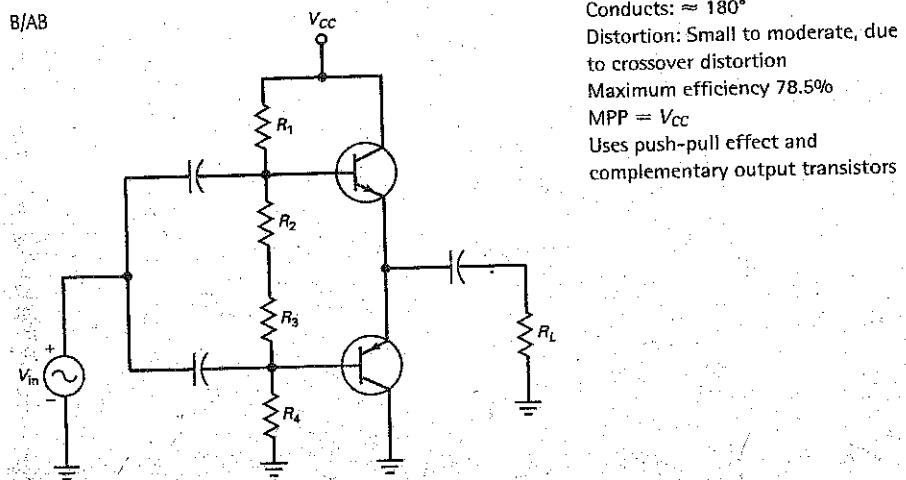
Characteristics

Conducts: 360°
 Distortion: Small, due to nonlinear distortion
 Maximum efficiency: 25%
 $MPP < V_{cc}$
 May use transformer coupling to achieve $\approx 50\%$ efficiency

Where used

Low-power amplifier where efficiency is not important

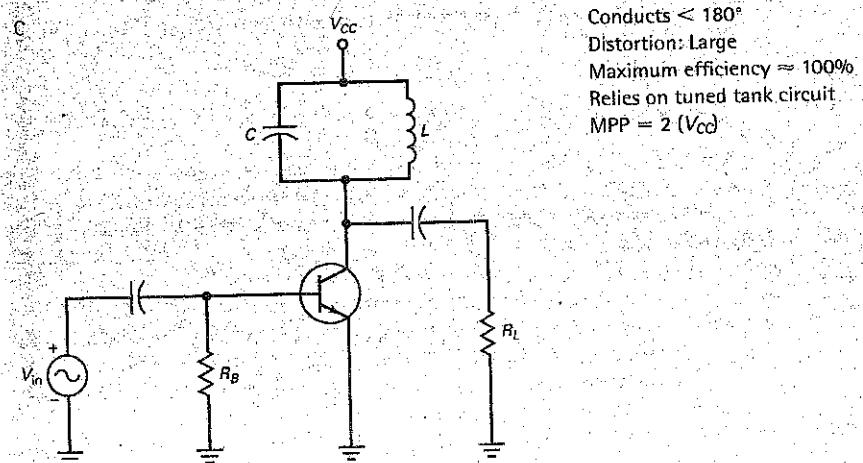
B/AB



Conducts: $\approx 180^\circ$
 Distortion: Small to moderate, due to crossover distortion
 Maximum efficiency 78.5%
 $MPP = V_{cc}$
 Uses push-pull effect and complementary output transistors

Output power amp; may use Darlington configurations and diodes for biasing

C



Conducts $< 180^\circ$
 Distortion: Large
 Maximum efficiency $\approx 100\%$
 Relies on tuned tank circuit
 $MPP = 2(V_{cc})$

Tuned RF power amplifier; final amp stage in communications circuits

is 26.7 mW/°C. This means that you have to subtract 26.7 mW for each degree the ambient temperature is above 25°C. In symbols:

$$\Delta P = D(T_A - 25^\circ\text{C}) \quad (12-40)$$

where ΔP = decrease in power rating

D = derating factor

T_A = ambient temperature

As an example, if the ambient temperature rises to 75°C, you have to reduce the power rating by:

$$\Delta P = 26.7 \text{ mW}(75 - 25) = 1.34 \text{ W}$$

Since the power rating is 4 W at 25°C, the new power rating is:

$$P_{D(\max)} = 4 \text{ W} - 1.34 \text{ W} = 2.66 \text{ W}$$

This agrees with the derating curve of Fig. 12-34.

Whether you get the reduced power rating from a derating curve like the one in Fig. 12-34 or from a formula like the one in Eq. (12-40), the important thing to be aware of is the reduction in power rating as the ambient temperature increases. Just because a circuit works well at 25°C doesn't mean it will perform well over a large temperature range. When you design circuits, therefore, you must take the operating temperature range into account by derating all transistors for the highest expected ambient temperature.

Heat Sinks

One way to increase the power rating of a transistor is to get rid of the heat faster. This is why heat sinks are used. If we increase the surface area of the transistor case, we allow the heat to escape more easily into the surrounding air. Look at Fig. 12-35a. When this type of heat sink is pushed on to the transistor case, heat radiates more quickly because of the increased surface area of the fins.

Figure 12-35b shows the power-tab transistor. The metal tab provides a path out of the transistor for heat. This metal tab can be fastened to the chassis of electronics equipment. Because the chassis is a massive heat sink, heat can easily escape from the transistor to the chassis.

Large power transistors like Fig. 12-35c have the collector connected directly to the case to let heat escape as easily as possible. The transistor case is then fastened to the chassis. To prevent the collector from shorting to the chassis ground, a thin insulating washer and a thermal conductive paste are used between the transistor case and the chassis. The important idea here is that heat can leave

Figure 12-35 (a) Push-on heat sink; (b) power-tab transistor; (c) power transistor with collector connected to case.

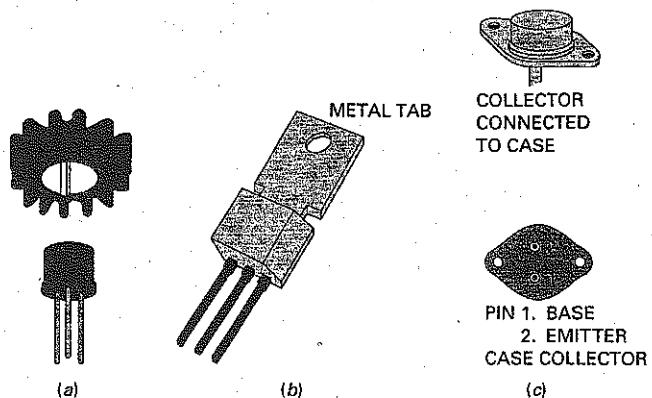
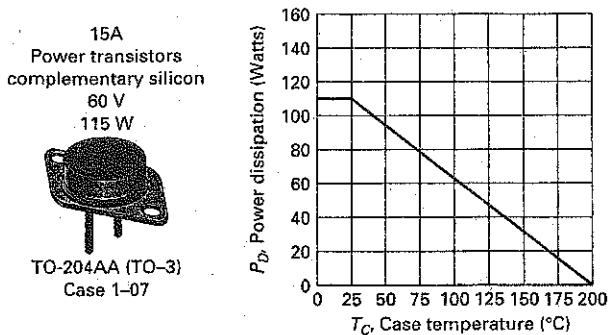


Figure 12-36 2N3055 derating curve. (courtesy of onsemi.com) on semiconductor



the transistor more rapidly, which means that the transistor has a higher power rating at the same ambient temperature.

Case Temperature

When heat flows out of a transistor, it passes through the case of the transistor and into the heat sink, which then radiates the heat into the surrounding air. The temperature of the transistor case T_C will be slightly higher than the temperature of the heat sink T_s , which in turn is slightly higher than the ambient temperature T_A .

The data sheets of large power transistors give derating curves for the case temperature rather than the ambient temperature. For instance, Fig. 12-36 shows the derating curve of a 2N3055. The power rating is 115 W at a case temperature of 25°C; then it decreases linearly with temperature until it reaches zero for a case temperature of 200°C.

Sometimes you get a derating factor instead of a derating curve. In this case, you can use the following equation to calculate the reduction in power rating:

$$\Delta P = D(T_C - 25^\circ\text{C}) \quad (12-41)$$

where ΔP = decrease in power rating

D = derating factor

T_C = case temperature

To use the derating curve of a large power transistor, you need to know what the case temperature will be in the worst case. Then you can derate the transistor to arrive at its maximum power rating.

Example 12-14

The circuit of Fig. 12-37 is to operate over an ambient temperature range of 0 to 50°C. What is the maximum power rating of the transistor for the worst-case temperature?

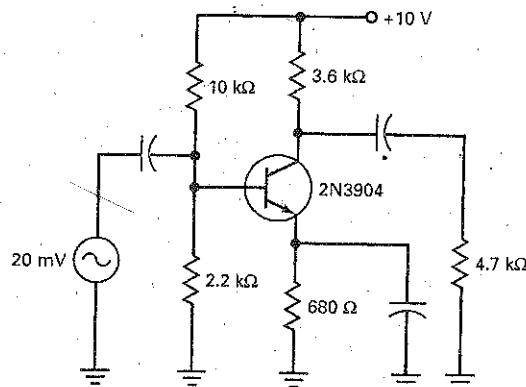
SOLUTION The worst-case temperature is the highest one because you have to derate the power rating given on a data sheet. If you look at the data sheet of a 2N3904 in Fig. 6-15, you will see the maximum power rating is listed as:

$$P_D = 625 \text{ mW at } 25^\circ\text{C ambient}$$

and the derating factor is given as:

$$D = 5 \text{ mW/}^\circ\text{C}$$

Figure 12-37 Example.



With Eq. (12-40), we can calculate:

$$\Delta P = (5 \text{ mW})(50 - 25) = 125 \text{ mW}$$

Therefore, the maximum power rating at 50°C is:

$$P_{D(\max)} = 625 \text{ mW} - 125 \text{ mW} = 500 \text{ mW}$$

PRACTICE PROBLEM 12-14 In Example 12-14, what is the transistor's power rating when the ambient temperature is 65°?

Summary

SEC. 12-1 AMPLIFIER TERMS

The classes of operation are A, B, and C. The types of coupling are capacitive, transformer, and direct. Frequency terms include audio, RF, narrowband, and wideband. Some types of audio amplifiers are preamps and power amplifiers.

SEC. 12-2 TWO LOAD LINES

Every amplifier has a dc load line and an ac load line. To get maximum peak-to-peak output, the Q point should be in the center of the ac load line.

SEC. 12-3 CLASS A OPERATION

The power gain equals the ac output power divided by the ac input power. The power rating of a transistor must be greater than the quiescent power dissipation. The efficiency of an amplifier

stage equals the ac output power divided by the dc input power, times 100 percent. The maximum efficiency of class A with a collector and load resistor is 25%. If the load resistor is the collector resistor or uses a transformer, the maximum efficiency increases to 50 percent.

SEC. 12-4 CLASS B OPERATION

Most class B amplifiers use a push-pull connection of two transistors. While one transistor conducts, the other is cut off, and vice versa. Each transistor amplifies one-half of the ac cycle. The maximum efficiency of class B is 78.5 percent.

SEC. 12-5 CLASS B PUSH-PULL Emitter Follower

Class B is more efficient than class A. In a class B push-pull emitter follower,

complementary *npn* and *pnp* transistors are used. The *npn* transistor conducts on one half-cycle, and the *pnp* transistor on the other.

SEC. 12-6 BIASING CLASS B/AB AMPLIFIERS

To avoid crossover distortion, the transistors of a class B push-pull emitter follower have a small quiescent current. This is referred to as a class AB. With voltage divider bias, the Q point is unstable and may result in thermal runaway. Diode bias is preferred because it can produce a stable Q point over a large temperature range.

SEC. 12-7 CLASS B/AB DRIVER

Rather than capacitive couple the signal into the output stage, we can use a

direct-coupled driver stage. The collector current out of the driver sets up the quiescent current through the complementary diodes.

SEC. 12-8 CLASS C OPERATION

Most class C amplifiers are tuned RF amplifiers. The input signal is negatively clamped, which produces narrow pulses of collector current. The tank circuit is

tuned to the fundamental frequency, so that all higher harmonics are filtered out.

SEC. 12-9 CLASS C FORMULAS

The bandwidth of a class C amplifier is inversely proportional to the Q of the circuit. The ac collector resistance includes the parallel equivalent resistance of the inductor and the load resistance.

SEC. 12-10 TRANSISTOR POWER RATING

The power rating of a transistor decreases as the temperature increases. The data sheet of a transistor either lists a derating factor or shows a graph of the power rating versus temperature. Heat sinks can remove the heat more rapidly, producing a higher power rating.

Definitions

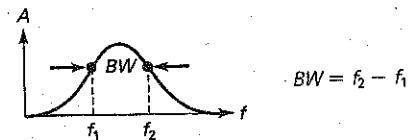
(12-12) Power gain:

$$P_{\text{in}} \xrightarrow{A_p} P_{\text{out}} \quad A_p = \frac{P_{\text{out}}}{P_{\text{in}}}$$

(12-18) Efficiency:

$$\eta = \frac{P_{\text{out}}}{P_{\text{dc}}} \times 100\%$$

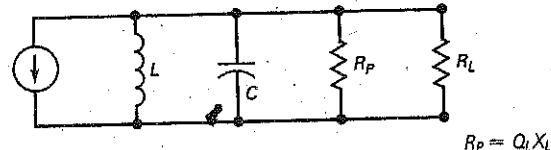
(12-30) Bandwidth:



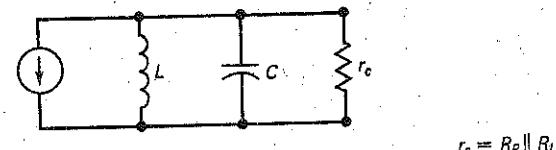
(12-32) Q of inductor:

$$Q_L = \frac{X_L}{R_S}$$

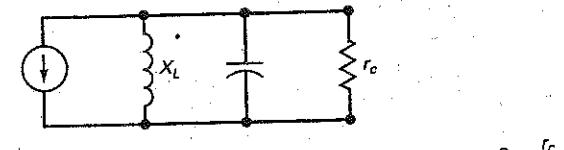
(12-38) Equivalent parallel R :



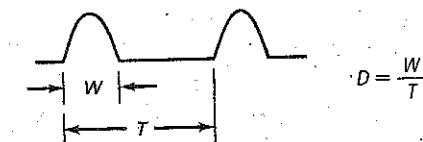
(12-34) AC collector resistance:



(12-35) Q of amplifier:

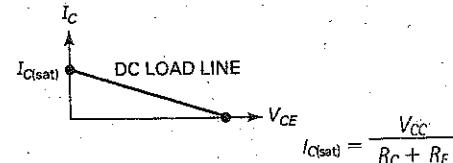


(12-36) Duty cycle:

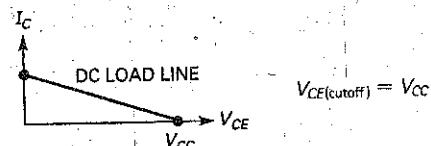


Derivations

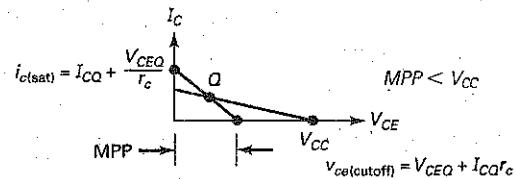
(12-1) Saturation current:



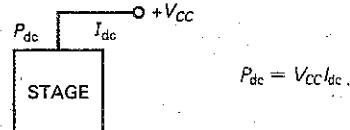
(12-2) Cutoff voltage:



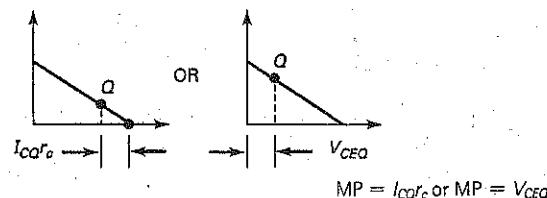
(12-7) Limit on output:



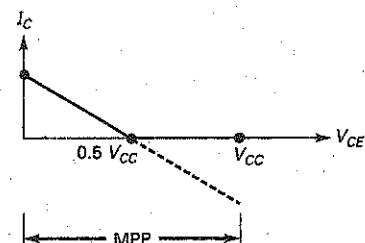
(12-17) DC input power:



(12-8) Maximum peak:

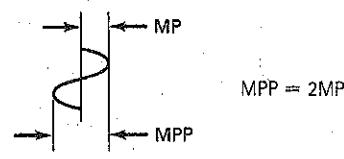


(12-24) Class B maximum output:

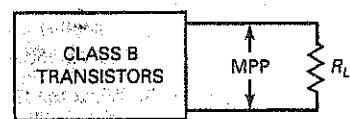


$$MPP = V_{CC}$$

(12-9) Maximum peak-to-peak output:

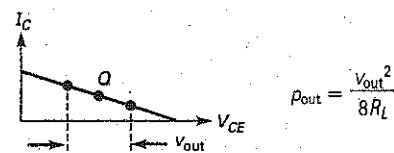


(12-27) Class B transistor output:

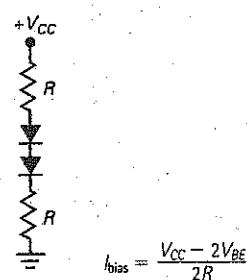


$$P_{D(max)} = \frac{MPP^2}{40R_L}$$

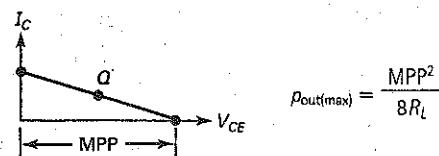
(12-14) Output power:



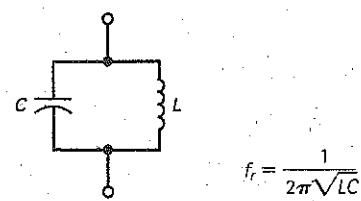
(12-28) Class B bias:



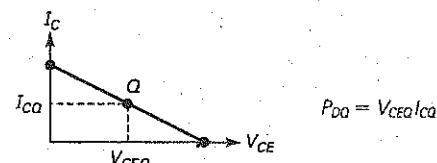
(12-15) Maximum output:



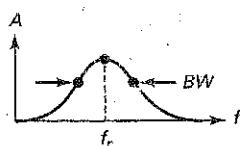
(12-29) Resonant frequency:



(12-16) Transistor power:

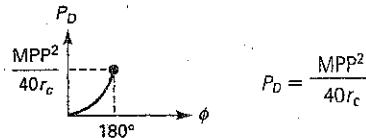


(12-31) Bandwidth:



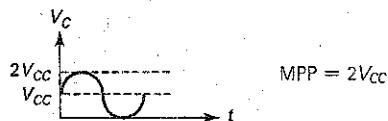
$$BW = \frac{f_r}{Q}$$

(12-39) Power dissipation:



$$P_D = \frac{MPP^2}{40r_c}$$

(12-38) Maximum output:



Student Assignments

1. For class B operation, the collector current flows for
 - a. The whole cycle
 - b. Half the cycle
 - c. Less than half a cycle
 - d. Less than a quarter of a cycle
2. Transformer coupling is an example of
 - a. Direct coupling
 - b. AC coupling
 - c. DC coupling
 - d. Impedance coupling
3. An audio amplifier operates in the frequency range of
 - a. 0 to 20 Hz
 - b. 20 Hz to 2 kHz
 - c. 20 to 20 kHz
 - d. Above 20 kHz
4. A tuned RF amplifier is
 - a. Narrowband
 - b. Wideband
 - c. Direct-coupled
 - d. A dc amplifier
5. The first stage of a preamp is
 - a. A tuned RF stage
 - b. Large signal
 - c. Small signal
 - d. A dc amplifier
6. For maximum peak-to-peak output voltage, the Q point should be
 - a. Near saturation
 - b. Near cutoff
 - c. At the center of the dc load line
 - d. At the center of the ac load line
7. An amplifier has two load lines because
 - a. It has ac and dc collector resistances
 - b. It has two equivalent circuits
 - c. DC acts one way and ac acts another
 - d. All of the above
8. When the Q point is at the center of the ac load line, the maximum peak-to-peak output voltage equals
 - a. V_{CEO}
 - b. $2V_{CEO}$
 - c. I_{CA}
 - d. $2I_{CA}$
9. Push-pull is almost always used with
 - a. Class A
 - b. Class B
 - c. Class C
 - d. All of the above
10. One advantage of a class B push-pull amplifier is
 - a. No quiescent current drain
 - b. Maximum efficiency of 78.5 percent
 - c. Greater efficiency than class A
 - d. All of the above
11. Class C amplifiers are almost always
 - a. Transformer-coupled between stages
 - b. Operated at audio frequencies
 - c. Tuned RF amplifiers
 - d. Wideband
12. The input signal of a class C amplifier
 - a. Is negatively clamped at the base
 - b. Is amplified and inverted
 - c. Produces brief pulses of collector current
 - d. All of the above
13. The collector current of a class C amplifier
 - a. Is an amplified version of the input voltage
 - b. Has harmonics
 - c. Is negatively clamped
 - d. Flows for half a cycle
14. The bandwidth of a class C amplifier decreases when the
 - a. Resonant frequency increases
 - b. Q increases
 - c. X_L decreases
 - d. Load resistance decreases
15. The transistor dissipation in a class C amplifier decreases when the
 - a. Resonant frequency increases
 - b. coil Q increases
 - c. Load resistance decreases
 - d. Capacitance increases
16. The power rating of a transistor can be increased by
 - a. Raising the temperature
 - b. Using a heat sink
 - c. Using a derating curve
 - d. Operating with no input signal

17. The ac load line is the same as the dc load line when the ac collector resistance equals the
- DC emitter resistance
 - AC emitter resistance
 - DC collector resistance
 - Supply voltage divided by collector current
18. If $R_C = 100 \Omega$ and $R_L = 180 \Omega$, the ac load resistance equals
- 64Ω
 - 90Ω
 - 100Ω
 - 180Ω
19. The quiescent collector current is the same as the
- DC collector current
 - AC collector current
 - Total collector current
 - Voltage-divider current
20. The ac load line usually
- Equals the dc load line
 - Has less slope than the dc load line
 - Is steeper than the dc load line
 - Is horizontal
21. For a Q point closer to cutoff than saturation on a CE dc load line, clipping is more likely to occur on the
- Positive peak of input voltage
 - Negative peak of input voltage
 - Negative peak of output voltage
 - Negative peak of emitter voltage
22. In a class A amplifier, the collector current flows for
- Less than half the cycle
 - Half the cycle
 - Less than the whole cycle
 - The entire cycle
23. With class A, the output signal should be
- Unclipped
 - Clipped on positive voltage peak
 - Clipped on negative voltage peak
 - Clipped on negative current peak
24. The instantaneous operating point swings along the
- AC load line
 - DC load line
 - Both load lines
 - Neither load line
25. The current drain of an amplifier is the
- Total ac current from the generator
 - Total dc current from the supply
 - Current gain from base to collector
 - Current gain from collector to base
26. The power gain of an amplifier
- Is the same as the voltage gain
 - Is smaller than the voltage gain
 - Equals output power divided by input power
 - Equals load power
27. Heat sinks reduce the
- Transistor power
 - Ambient temperature
 - Junction temperature
 - Collector current
28. When the ambient temperature increases, the maximum transistor power rating
- Decreases
 - Increases
 - Remains the same
 - None of the above
29. If the load power is 300 mW and the dc power is 1.5 W, the efficiency is
- 0
 - 2 percent
 - 3 percent
 - 20 percent
30. The ac load line of an emitter follower is usually
- The same as the dc load line
 - Vertical
 - More horizontal than the dc load line
 - Steeper than the dc load line
31. If an emitter follower has $V_{CEO} = 6 \text{ V}$, $I_{CQ} = 200 \text{ mA}$, and $r_e = 10 \Omega$, the maximum peak-to-peak unclipped output is
- 2 V
 - 4 V
 - 6 V
 - 8 V
32. The ac resistance of compensating diodes
- Must be included
 - Is very high
 - Is usually small enough to ignore
 - Compensates for temperature changes
33. If the Q point is at the middle of the dc load line, clipping will first occur on the
- Left voltage swing
 - Upward current swing
 - Positive half-cycle of input
 - Negative half-cycle of input
34. The maximum efficiency of a class B push-pull amplifier is
- 25 percent
 - 50 percent
 - 78.5 percent
 - 100 percent
35. A small quiescent current is necessary with a class AB push-pull amplifier to avoid
- Crossover distortion
 - Destroying the compensating diodes
 - Excessive current drain
 - Loading the driver stage

Problems

SEC. 12-2 TWO LOAD LINES

- 12-1 What is the dc collector resistance in Fig. 12-38? What is the dc saturation current?
- 12-2 In Fig. 12-38, what is the ac collector resistance? What is the ac saturation current?
- 12-3 What is the maximum peak-to-peak output in Fig. 12-38?
- 12-4 All resistances are doubled in Fig. 12-38. What is the ac collector resistance?
- 12-5 All resistances are tripled in Fig. 12-38. What is the maximum peak-to-peak output?

Figure 12-38

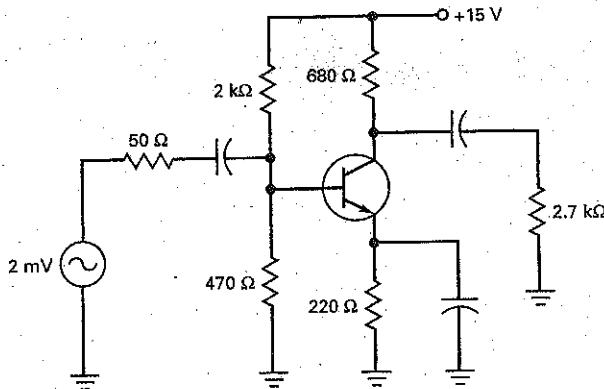
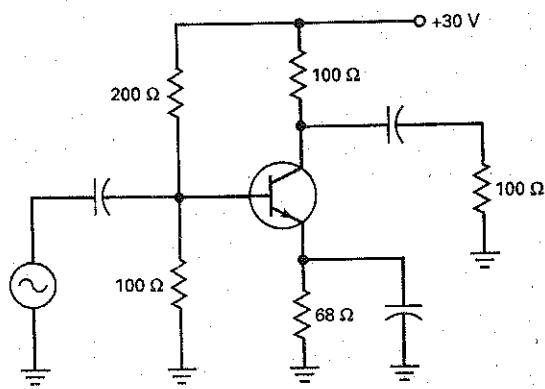


Figure 12-39

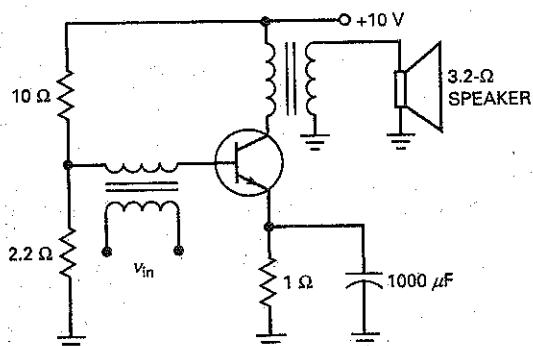


- 12-6 What is the dc collector resistance in Fig. 12-39? What is the dc saturation current?
- 12-7 In Fig. 12-39, what is the ac collector resistance? What is the ac saturation current?
- 12-8 What is the maximum peak-to-peak output in Fig. 12-39?
- 12-9 All resistances are doubled in Fig. 12-39. What is the ac collector resistance?
- 12-10 All resistances are tripled in Fig. 12-39. What is the maximum peak-to-peak output?

SEC. 12-3 CLASS A OPERATION

- 12-11 An amplifier has an input power of 4 mW and output power of 2 W. What is the power gain?
- 12-12 If an amplifier has a peak-to-peak output voltage of 15 V across a load resistance of 1 kΩ, what is the power gain if the input power is 400 μW?
- 12-13 What is the current drain in Fig. 12-38?
- 12-14 What is the dc power supplied to the amplifier of Fig. 12-38?

Figure 12-40



12-15 The input signal of Fig. 12-38 is increased until maximum peak-to-peak output voltage is across the load resistor. What is the efficiency?

12-16 What is the quiescent power dissipation in Fig. 12-38?

12-17 What is the current drain in Fig. 12-39?

12-18 What is the dc power supplied to the amplifier of Fig. 12-39?

12-19 The input signal of Fig. 12-39 is increased until maximum peak-to-peak output voltage is across the load resistor. What is the efficiency?

12-20 What is the quiescent power dissipation in Fig. 12-39?

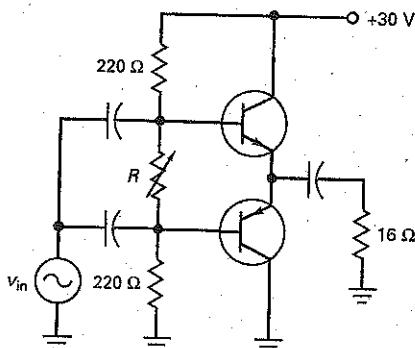
12-21 If $V_{BE} = 0.7$ V in Fig. 12-40, what is the dc emitter current?

12-22 The speaker of Fig. 12-40 is equivalent to a load resistance of 3.2Ω . If the voltage across the speaker is 5 V pp, what is the output power? What is the efficiency of the stage?

SEC. 12-6 BIASING CLASS B/AB AMPLIFIERS

- 12-23 The ac load line of a class B push-pull emitter follower has a cutoff voltage of 12 V. What is the maximum peak-to-peak voltage?

Figure 12-41



- 12-24 What is the maximum power dissipation of each transistor of Fig. 12-41?
- 12-25 What is the maximum output power in Fig. 12-41?
- 12-26 What is the quiescent collector current in Fig. 12-42?
- 12-27 In Fig. 12-42, what is the maximum efficiency of the amplifier?

Figure 12-42

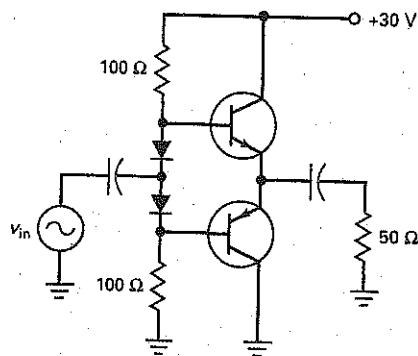
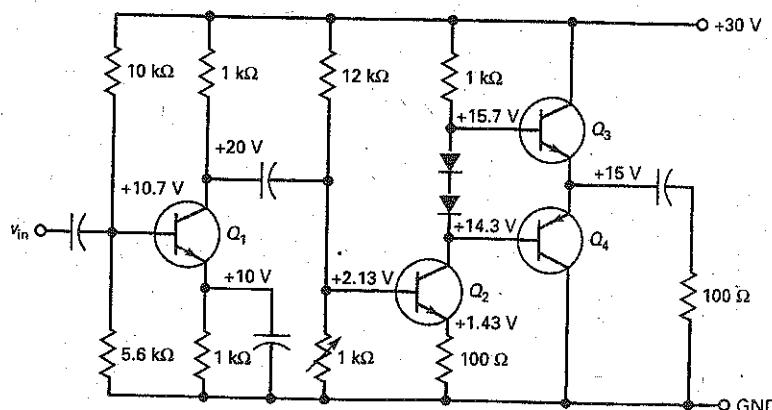


Figure 12-43



- 12-28 If the biasing resistors of Fig. 12-42 are changed to 1 kΩ, what is the quiescent collector current? The efficiency of the amplifier?

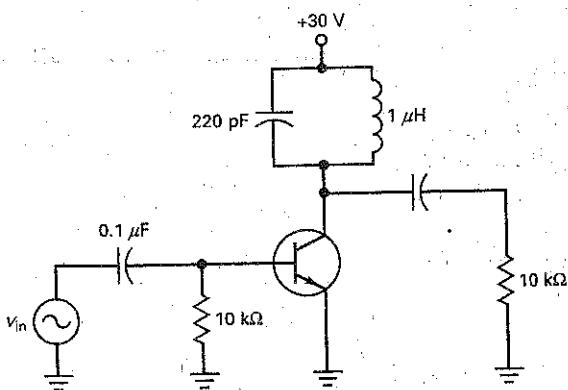
SEC. 12-7 CLASS B/AB DRIVERS

- 12-29 What is the maximum output power in Fig. 12-43?
- 12-30 In Fig. 12-43, what is the voltage gain of the first stage if $\beta = 200$?
- 12-31 If Q_3 and Q_4 have current gains of 200 in Fig. 12-43, what is the voltage gain of the second stage?
- 12-32 What is the quiescent collector current in Fig. 12-43?
- 12-33 What is the overall voltage gain for the three-stage amplifier in Fig. 12-43?

SEC. 12-8 CLASS C OPERATION

- 12-34 **||| Multisim** If the input voltage equals 5 V rms in Fig. 12-44, what is the peak-to-peak input voltage? If the dc voltage between the base and ground is measured, what will the voltmeter indicate?
- 12-35 **||| Multisim** What is the resonant frequency in Fig. 12-44?
- 12-36 **||| Multisim** If the inductance is doubled in Fig. 12-44, what is the resonant frequency?
- 12-37 **||| Multisim** What is the resonance in Fig. 12-44 if the capacitance is changed to 100 pF?
- 12-38 If the class C amplifier of Fig. 12-44 has an output power of 11 mW and an input power of 50 μ W, what is the power gain?
- 12-39 What is the output power in Fig. 12-44 if the output voltage is 50 V pp?
- 12-40 What is the maximum ac output power in Fig. 12-44?
- 12-41 If the current drain in Fig. 12-44 is 0.5 mA, what is the dc input power?
- 12-42 What is the efficiency of Fig. 12-44 if the current drain is 0.4 mA and the output voltage is 30 V pp?

Figure 12-44



Critical Thinking

- 12-48 The output of an amplifier is a square-wave output even though the input is a sine wave. What is the explanation?
- 12-49 A power transistor like the one in Fig. 12-36 is used in an amplifier. Somebody tells you that since the case is grounded, you can safely touch the case. What do you think about this?
- 12-50 You are in a bookstore and you read the following in an electronics book: "Some power amplifiers can have an

12-43 If the Q of the inductor is 125 in Fig. 12-44, what is the bandwidth of the amplifier?

12-44 What is the worst-case transistor power dissipation in Fig. 12-44 ($Q = 125$)?

SEC. 12-10 TRANSISTOR POWER RATING

12-45 A 2N3904 is used in Fig. 12-44. If the circuit has to operate over an ambient temperature range of 0 to 100°C, what is the maximum power rating of the transistor in the worst case?

12-46 A transistor has the derating curve shown in Fig. 12-34. What is the maximum power rating for an ambient temperature of 100°C?

12-47 The data sheet of a 2N3055 lists a power rating of 115 W for a case temperature of 25°C. If the derating factor is 0.657 W/°C, what is $P_{D(\max)}$ when the case temperature is 90°C?

efficiency of 125 percent." Would you buy the book? Explain your answer.

12-51 Normally, the ac load line is more vertical than the dc load line. A couple of classmates say that they are willing to bet that they can draw a circuit whose ac load line is less vertical than the dc load line. Would you take the bet? Explain.

12-52 Draw the dc and ac load lines for Fig. 12-38.

Up-Down Analysis

In Fig. 12-45, P_L is the output power in the load resistor, and P_S is the dc input power from the supply.

- 12-53 Predict the response of the dependent variables to a slight increase in V_{CC} . Use the table to check your predictions.
- 12-54 Repeat Prob. 12-53 for a slight increase in R_1 .
- 12-55 Repeat Prob. 12-53 for a slight increase in R_2 .

12-56 Repeat Prob. 12-53 for a slight increase in R_E .

12-57 Repeat Prob. 12-53 for a slight increase in R_C .

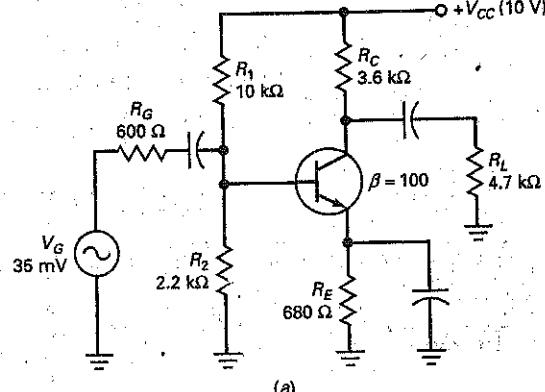
12-58 Repeat Prob. 12-53 for a slight increase in V_G .

12-59 Repeat Prob. 12-53 for a slight increase in R_G .

12-60 Repeat Prob. 12-53 for a slight increase in R_L .

12-61 Repeat Prob. 12-53 for a slight increase in β .

Figure 12-45



UP-Down Analysis

Slight increase	P_L	P_D	P_S	MPP	η
V_{CC}					
R_1					
R_2					
R_E					
R_C					
V_G					
R_G					
R_L					
β					

(a)

(b)

Job Interview Questions

1. Tell me about the three classes of amplifier operation. Illustrate the classes by drawing collector current waveforms.
2. Draw brief schematics showing the three types of coupling used between amplifier stages.
3. Draw a VDB amplifier. Then, draw its dc load line and ac load line. Assuming that the Q point is centered on the ac load lines, what is the ac saturation current? The ac cutoff voltage? The maximum peak-to-peak output?
4. Draw the circuit of a two-stage amplifier and tell me how to calculate the total current drain on the supply.
5. Draw a class C tuned amplifier. Tell me how to calculate the resonant frequency, and tell me what happens to the ac signal at the base. Explain how it is possible that the brief pulses of collector current produce a sine wave of voltage across the resonant tank circuit.
6. What is the most common application of a class C amplifier? Could this type of amplifier be used for an audio application? If not, why not?
7. Explain the purpose of heat sinks. Also, why do we put an insulating washer between the transistor and the heat sink?
8. What is meant by the duty cycle? How is it related to the power supplied by the source?
9. Define Q .
10. Which class of amplifier operation is most efficient? Why?
11. You have ordered a replacement transistor and heat sink. In the box with the heat sink is a package containing a white substance. What is it?
12. Comparing a class A amplifier to a class C amplifier, which has the greater fidelity? Why?
13. What type of amplifier is used when only a small range of frequencies is to be amplified?
14. What other types of amplifiers are you familiar with?

Self-Test Answers

1. b
2. b
3. c
4. a
5. c
6. d
7. d
8. b
9. b
10. d
11. c
12. d
13. b
14. b
15. b
16. b
17. c
18. a
19. a
20. c
21. b
22. d
23. a
24. a
25. b
26. c
27. c
28. a
29. d
30. d
31. b
32. c
33. d
34. c
35. a

Practice Problem Answers

12-1 $I_{CQ} = 100 \text{ mA}$
 $V_{CEQ} = 15 \text{ V}$

12-2 $I_{C(\text{sat})} = 350 \text{ mA}$
 $V_{CE(\text{cutoff})} = 21 \text{ V}$
 $\text{MPP} = 12 \text{ V}$

12-3 $A_P = 1122$

12-5 $R = 200 \Omega$

12-6 $I_{CQ} = 331 \text{ mA}$
 $V_{CEQ} = 6.7 \text{ V}$
 $r_e = 8 \Omega$

12-7 $\text{MPP} = 5.3 \text{ V}$

12-8 $P_D(\text{max}) = 2.8 \text{ W}$
 $P_{\text{out}(\text{max})} = 14 \text{ W}$

12-9 Efficiency $\approx 63\%$

12-10 Efficiency $= 78\%$

12-11 $f_r = 4.76 \text{ MHz}$
 $V_{\text{out}} = 24 \text{ V pp}$

12-13 $P_D = 16.6 \text{ mW}$

12-14 $P_D(\text{max}) = 425 \text{ mW}$

13

JFETs

- The bipolar junction transistor (BJT) relies on two types of charge: free electrons and holes. This is why it is called *bipolar*; the prefix *bi* stands for "two." This chapter discusses another kind of transistor called the **field-effect transistor (FET)**. This type of device is *unipolar* because its operation depends on only one type of charge, either free electrons or holes. In other words, an FET has majority carriers but not minority carriers.

For most linear applications, the BJT is the preferred device. But there are some linear applications in which the FET is better suited because of its high input impedance and other properties. Furthermore, the FET is the preferred device for most switching applications. Why? Because there are no minority carriers in an FET. As a result, it can switch off faster since no stored charge has to be removed from the junction area.

There are two kinds of unipolar transistors: JFETs and MOSFETs. This chapter discusses the *junction field-effect transistor (JFET)* and its applications. In Chapter 14, we discuss the *metal-oxide semiconductor FET (MOSFET)* and its applications.

Chapter Outline

- 13-1 Basic Ideas
- 13-2 Drain Curves
- 13-3 The Transconductance Curve
- 13-4 Biasing in the Ohmic Region
- 13-5 Biasing in the Active Region
- 13-6 Transconductance
- 13-7 JFET Amplifiers
- 13-8 The JFET Analog Switch
- 13-9 Other JFET Applications
- 13-10 Reading Data Sheets
- 13-11 JFET Testing

Objectives

After studying this chapter, you should be able to:

- Describe the basic construction of a JFET.
- Draw diagrams that show common biasing arrangements.
- Identify and describe the significant regions of JFET drain curves and transconductance curves.
- Calculate the proportional pinchoff voltage and determine which region a JFET is operating in.
- Determine the dc operating point using ideal and graphical solutions.
- Determine transconductance and use it to calculate gain in JFET amplifiers.
- Describe several JFET applications including switches, variable resistances, and choppers.
- Test JFETs for proper operation.

Vocabulary

automatic gain control (AGC)	gate	shunt switch
channel	gate bias	source
chopper	gate-source cutoff voltage	source follower
common-source (CS) amplifier	ohmic region	transconductance
current source bias	pinchoff voltage	transconductance curve
drain	self-bias	voltage-controlled device
field effect	series switch	voltage-divider bias
field-effect transistor (FET)		

GOOD TO KNOW

In general, JFETs are more temperature stable than bipolar transistors. Furthermore, JFETs are typically much smaller than bipolar transistors. This size difference makes them particularly suitable for use in ICs, where the size of each component is very critical.

13-1 Basic Ideas

Figure 13-1a shows a piece of *n*-type semiconductor. The lower end is called the **source**, and the upper end is called the **drain**. The supply voltage V_{DD} forces free electrons to flow from the source to the drain. To produce a JFET, a manufacturer diffuses two areas of *p*-type semiconductor into the *n*-type semiconductor, as shown in Fig. 13-1b. These *p* regions are connected internally to get a single external **gate lead**.

Field Effect

Figure 13-2 shows the normal biasing voltages for a JFET. The drain supply voltage is positive, and the gate supply voltage is negative. The term **field effect** is related to the depletion layers around each *p* region. These depletion layers exist because free electrons diffuse from the *n* regions into the *p* regions. The recombination of free electrons and holes creates the depletion layers shown by the colored areas.

Reverse Bias of Gate

In Fig. 13-2, the *p*-type gate and the *n*-type source form the gate-source diode. With a JFET, we always *reverse-bias* the gate-source diode. Because of reverse bias, the gate current I_G is approximately zero, which is equivalent to saying that the JFET has an almost infinite input resistance.

Figure 13-1 (a) Part of JFET; (b) single-gate JFET.

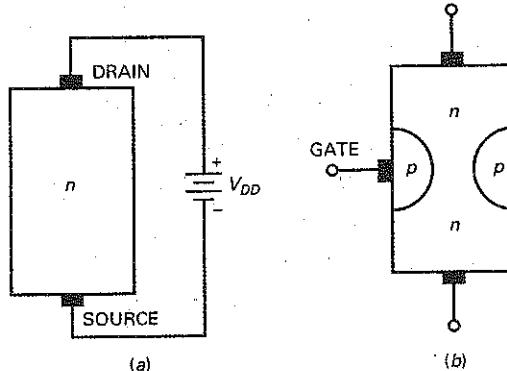
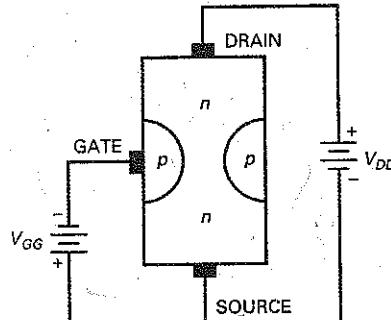


Figure 13-2 Normal biasing of JFET.



A typical JFET has an input resistance in the hundreds of megohms. This is the big advantage that a JFET has over a bipolar transistor. It is the reason that JFETs excel in applications in which a high input impedance is required. One of the most important applications of the JFET is the *source follower*, a circuit like the emitter follower, except that the input impedance is in the hundreds of megohms for lower frequencies.

Gate Voltage Controls Drain Current

In Fig. 13-2, electrons flowing from the source to the drain must pass through the narrow channel between the depletion layers. When the gate voltage becomes more negative, the depletion layers expand and the conducting channel becomes narrower. The more negative the gate voltage, the smaller the current between the source and the drain.

The JFET is a **voltage-controlled device** because an input voltage controls an output current. In a JFET, the gate-to-source voltage V_{GS} determines how much current flows between the source and the drain. When V_{GS} is zero, maximum drain current flows through the JFET. This is why a JFET is referred to as a normally on device. On the other hand, if V_{GS} is negative enough, the depletion layers touch and the drain current is cut off.

Schematic Symbol

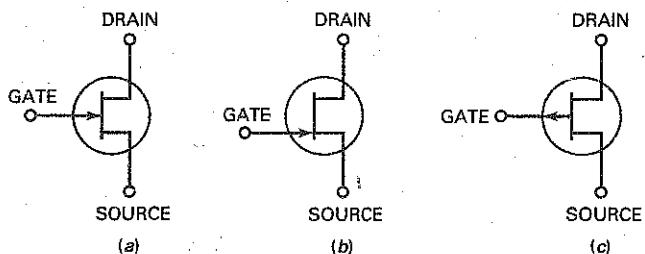
The JFET of Fig. 13-2 is an *n-channel JFET* because the channel between the source and the drain is an *n-type semiconductor*. Figure 13-3a shows the schematic symbol for an *n-channel JFET*. In many low-frequency applications, the source and the drain are interchangeable because you can use either end as the source and the other end as the drain.

The source and drain terminals are not interchangeable at high frequencies. Almost always, the manufacturer minimizes the internal capacitance on the drain side of the JFET. In other words, the capacitance between the gate and the drain is smaller than the capacitance between the gate and the source. You will learn more about internal capacitances and their effect on circuit action in a later chapter.

Figure 13-3b shows an alternative symbol for an *n-channel JFET*. This symbol with its offset gate is preferred by many engineers and technicians. The offset gate points to the source end of the device, a definite advantage in complicated multistage circuits.

There is also a *p-channel JFET*. The schematic symbol for a *p-channel JFET*, shown in Fig. 13-3c, is similar to that for the *n-channel JFET*, except that the gate arrow points in the opposite direction. The action of a *p-channel JFET* is complementary; that is, all voltages and currents are reversed. To reverse bias a *p-channel JFET*, the gate is made positive in respect to the source. Therefore, V_{GS} is made positive.

Figure 13-3 (a) Schematic symbol; (b) offset-gate symbol; (c) p-channel symbol.



GOOD TO KNOW

The depletion layers are actually wider near the top of the *p-type* materials and narrower at the bottom. The reason for the change in the width can be understood by realizing that the drain current I_D will produce a voltage drop along the length of the channel. With respect to the source, a more positive voltage is present as you move up the channel toward the drain end. Since the width of a depletion layer is proportional to the amount of reverse-bias voltage, the depletion layer of the *pn* junction must be wider at the top, where the amount of reverse-bias voltage is greater.

Example 13-1

A 2N5486 JFET has a gate current of 1 nA when the reverse gate voltage is 20 V. What is the input resistance of this JFET?

SOLUTION Use Ohm's law to calculate:

$$R_{in} = \frac{20 \text{ V}}{1 \text{ nA}} = 20,000 \text{ M}\Omega$$

PRACTICE PROBLEM 13-1 In Example 13-1, calculate the input resistance if the JFET's gate current is 2 nA.

13-2 Drain Curves

Figure 13-4a shows a JFET with normal biasing voltages. In this circuit, the gate-source voltage V_{GS} equals the gate supply voltage V_{GG} , and the drain-source voltage V_{DS} equals the drain supply voltage V_{DD} .

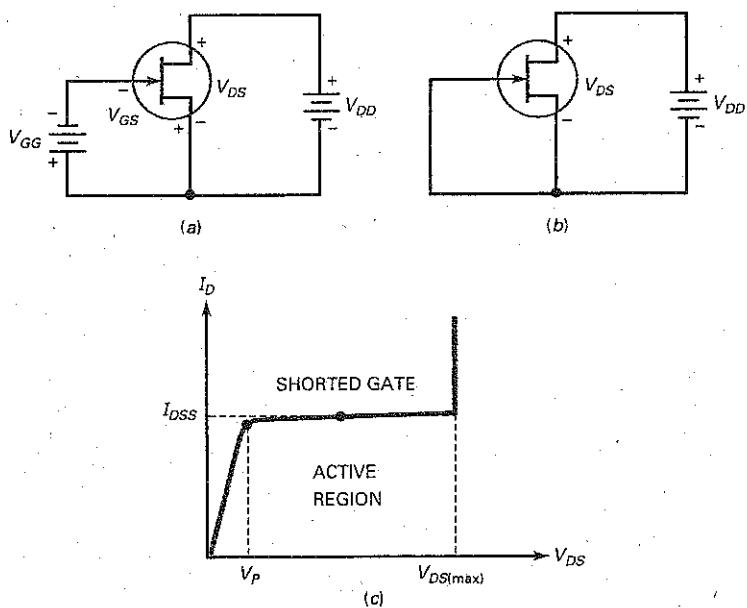
Maximum Drain Current

GOOD TO KNOW

The pinchoff voltage V_p is the point at which further increases in V_{DS} are offset by a proportional increase in the channel's resistance. This means that if the channel resistance is increasing in direct proportion to V_{DS} above V_p , I_D must remain the same above V_p .

If we short the gate to the source, as shown in Fig. 13-4b, we will get maximum drain current because $V_{GS} = 0$. Figure 13-4c shows the graph of drain current I_D versus drain-source voltage V_{DS} for this shorted-gate condition. Notice how the drain current increases rapidly and then becomes almost horizontal when V_{DS} is greater than V_p .

Figure 13-4 (a) Normal bias; (b) zero gate voltage; (c) shorted gate drain current.



Why does the drain current become almost constant? When V_{DS} increases, the depletion layers expand. When $V_{DS} = V_p$, the depletion layers are almost touching. The narrow conducting channel therefore pinches off or prevents a further increase in current. This is why the current has an upper limit of I_{DSS} .

The active region of a JFET is between V_p and $V_{DS(\max)}$. The minimum voltage V_p is called the *pinchoff voltage*, and the maximum voltage $V_{DS(\max)}$ is the *breakdown voltage*. Between pinchoff and breakdown, the JFET acts like a current source of approximately I_{DSS} when $V_{GS} = 0$.

I_{DSS} stands for the current drain to source with a shorted gate. This is the maximum drain current a JFET can produce. The data sheet of any JFET lists the value of I_{DSS} . This is one of the most important JFET quantities, and you should always look for it first because it is the upper limit on the JFET current.

The Ohmic Region

In Fig. 13-5, the pinchoff voltage separates two major operating regions of the JFET. The almost-horizontal region is the active region. The almost-vertical part of the drain curve below pinchoff is called the *ohmic region*.

When operated in the ohmic region, a JFET is equivalent to a resistor with a value of approximately:

$$R_{DS} = \frac{V_p}{I_{DSS}} \quad (13-1)$$

R_{DS} is called the *ohmic resistance of the JFET*. In Fig. 13-5, $V_p = 4$ V and $I_{DSS} = 10$ mA. Therefore, the ohmic resistance is:

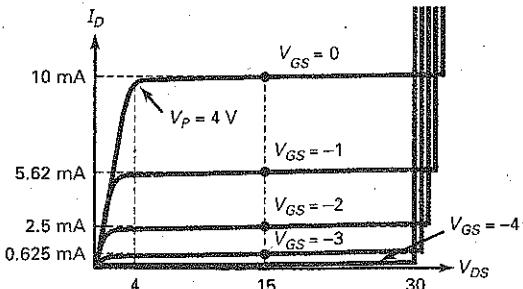
$$R_{DS} = \frac{4 \text{ V}}{10 \text{ mA}} = 400 \Omega$$

If the JFET is operating anywhere in the ohmic region, it has an ohmic resistance of 400 Ω .

Gate Cutoff Voltage

Figure 13-5 shows the drain curves for a JFET with an I_{DSS} of 10 mA. The top curve is always for $V_{GS} = 0$, the shorted-gate condition. In this example, the pinchoff voltage is 4 V and the breakdown voltage is 30 V. The next curve down is for $V_{GS} = -1$ V, the next for $V_{GS} = -2$ V, and so on. As you can see, the more negative the gate-source voltage, the smaller the drain current.

Figure 13-5 Drain curves.



GOOD TO KNOW

There is often a lot of confusion in textbooks and in manufacturers' data sheets regarding the terms *cutoff* and *pinchoff*. $V_{GS(\text{off})}$ is the value of V_{GS} that completely pinches off the channel, thus reducing the drain current to zero. On the other hand, the pinchoff voltage is the value of V_{DS} at which I_D levels off with $V_{GS} = 0 \text{ V}$.

The bottom curve is important. Notice that a V_{GS} of -4 V reduces the drain current to almost zero. This voltage is called the **gate-source cutoff voltage** and is symbolized by $V_{GS(\text{off})}$ on data sheets. At this cutoff voltage the depletion layers touch. In effect, the conducting channel disappears. This is why the drain current is approximately zero.

In Fig. 13-5, notice that

$$V_{GS(\text{off})} = -4 \text{ V} \quad \text{and} \quad V_P = 4 \text{ V}$$

This is not a coincidence. The two voltages always have the same magnitude because they are the values where the depletion layers touch or almost touch. Data sheets may list either quantity, and you are expected to know that the other has the same magnitude. As an equation:

$$V_{GS(\text{off})} = -V_P \quad (13-2)$$

Example 13-2

An MPF4857 has $V_P = 6 \text{ V}$ and $I_{DSS} = 100 \text{ mA}$. What is the ohmic resistance? The gate-source cutoff voltage?

SOLUTION The ohmic resistance is:

$$R_{DS} = \frac{6 \text{ V}}{100 \text{ mA}} = 60 \Omega$$

Since the pinchoff voltage is 6 V , the gate-source cutoff voltage is:

$$V_{GS(\text{off})} = -6 \text{ V}$$

PRACTICE PROBLEM 13-2 A 2N5484 has a $V_{GS(\text{off})} = -3.0 \text{ V}$ and $I_{DSS} = 5 \text{ mA}$. Find its ohmic resistance and V_P values.

13-3 The Transconductance Curve

The transconductance curve of a JFET is a graph of I_D versus V_{GS} . By reading the values of I_D and V_{GS} of each drain curve in Fig. 13-5, we can plot the curve of Fig. 13-6a. Notice that the curve is nonlinear because the current increases faster when V_{GS} approaches zero.

Any JFET has a transconductance curve like Fig. 13-6b. The end points on the curve are $V_{GS(\text{off})}$ and I_{DSS} . The equation for this graph is:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2 \quad (13-3)$$

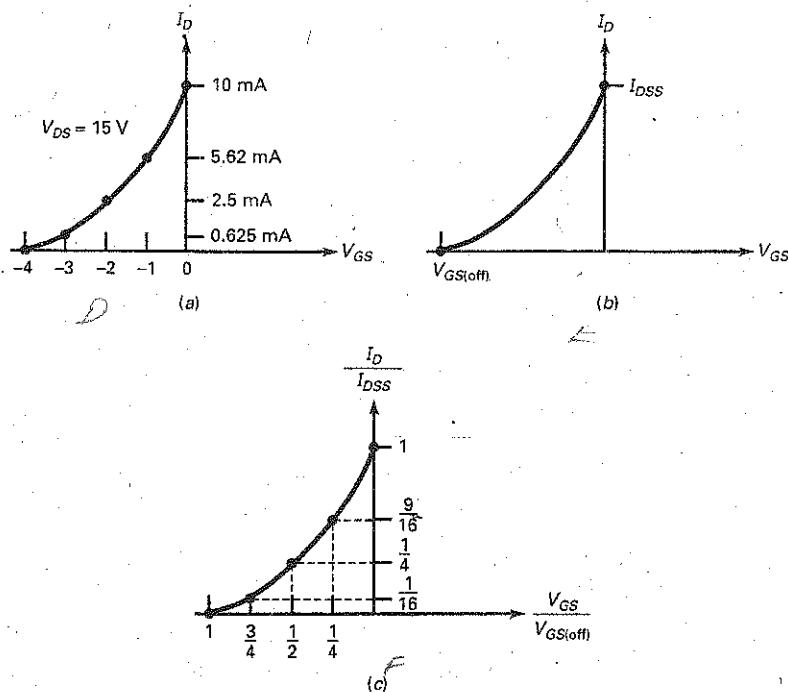
Because of the squared quantity in this equation, JFETs are often called *square-law devices*. The squaring of the quantity produces the nonlinear curve of Fig. 13-6b.

Figure 13-6c shows a *normalized transconductance curve*. Normalized means that we are graphing ratios like I_D/I_{DSS} and $V_{GS}/V_{GS(\text{off})}$.

GOOD TO KNOW

The transconductance curve of a JFET is unaffected by the circuit or configuration in which the JFET is used.

Figure 13-6. Transconductance curve.



In Fig. 13-6c, the half-cutoff point

$$\frac{V_{GS}}{V_{GS(\text{off})}} = \frac{1}{2}$$

produces a normalized current of:

$$\frac{I_D}{I_{DSS}} = \frac{1}{4}$$

In words: When the gate voltage is half the cutoff voltage, the drain current is one quarter of maximum.

Example 13-3

A 2N5668 has $V_{GS(\text{off})} = -4 \text{ V}$ and $I_{DSS} = 5 \text{ mA}$. What are the gate voltage and drain current at the half cutoff point?

SOLUTION At the half cutoff point:

$$V_{GS} = \frac{-4 \text{ V}}{2} = -2 \text{ V}$$

and the drain current is:

$$I_D = \frac{5 \text{ mA}}{4} = 1.25 \text{ mA}$$

Example 13-4

A 2N5459 has $V_{GS(\text{off})} = -8 \text{ V}$ and $I_{DSS} = 16 \text{ mA}$. What is the drain current at the half cutoff point?

SOLUTION The drain current is one quarter of the maximum, or:

$$I_D = 4 \text{ mA}$$

The gate-source voltage that produces this current is -4 V , half of the cutoff voltage.

PRACTICE PROBLEM 13-4 Repeat Example 13-4 using a JFET with $V_{GS(\text{off})} = -6 \text{ V}$ and $I_{DSS} = 12 \text{ mA}$.

13-4 Biasing in the Ohmic Region

The JFET can be biased in the ohmic or in the active region. When biased in the ohmic region, the JFET is equivalent to a resistance. When biased in the active region, the JFET is equivalent to a current source. In this section, we discuss gate bias, the method used to bias a JFET in the ohmic region.

Gate Bias

Figure 13-7a shows gate bias. A negative gate voltage of $-V_{GG}$ is applied to the gate through biasing resistor R_G . This sets up a drain current that is less than I_{DSS} . When the drain current flows through R_D , it sets up a drain voltage of:

$$V_D = V_{DD} - I_D R_D \quad (13-4)$$

Gate bias is the worst way to bias a JFET in the active region because the Q point is too unstable.

For example, a 2N5459 has the following spreads between minimum and maximum: I_{DSS} varies from 4 to 16 mA, and $V_{GS(\text{off})}$ varies from -2 to -8 V . Figure 13-7b shows the minimum and maximum transconductance curves. If a gate bias of -1 V is used with this JFET, we get the minimum and maximum Q points shown. Q_1 has a drain current of 12.3 mA, and Q_2 has a drain current of only 1 mA.

Hard Saturation

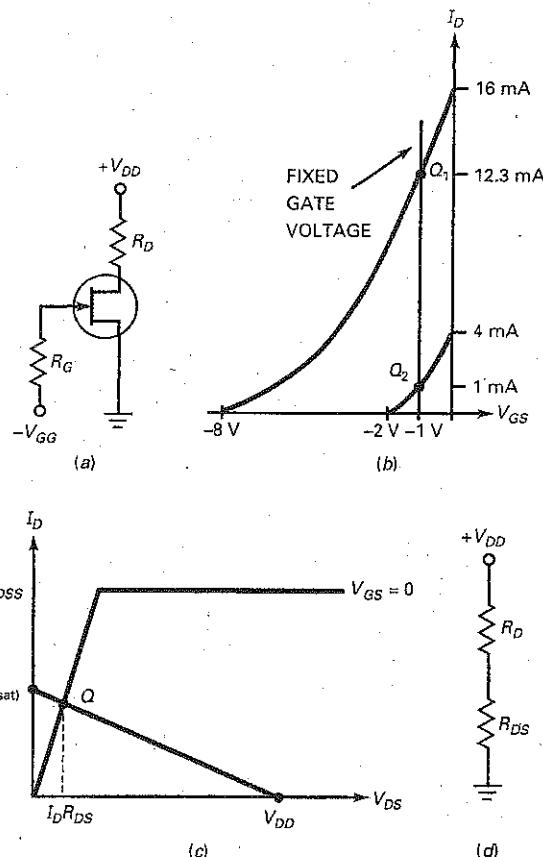
Although not suitable for active-region biasing, gate bias is perfect for ohmic-region biasing because stability of the Q point does not matter. Figure 13-7c shows how to bias a JFET in the ohmic region. The upper end of the dc load line has a drain saturation current of:

$$I_{D(\text{sat})} = \frac{V_{DD}}{R_D}$$

To ensure that a JFET is biased in the ohmic region, all we need to do is use $V_{GS} = 0$ and:

$$I_{D(\text{sat})} \ll I_{DSS} \quad (13-5)$$

Figure 13-7 (a) Gate bias; (b) Q point unstable in active region; (c) biased in ohmic region; (d) JFET is equivalent to resistance.



The symbol \ll means "much less than." This equation says that the drain saturation current must be much less than the maximum drain current. For instance, if a JFET has $I_{DSS} = 10$ mA, hard saturation will occur if $V_{GS} = 0$ and $I_{D(sat)} \ll 1$ mA.

When a JFET is biased in the ohmic region, we can replace it by a resistance of R_{DS} , as shown in Fig. 13-7d. With this equivalent circuit, we can calculate the drain voltage. When R_{DS} is much smaller than R_D , the drain voltage is close to zero.

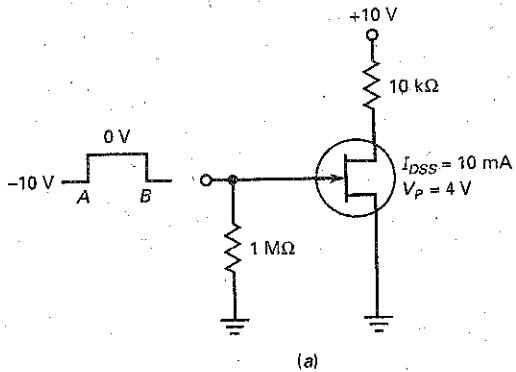
Example 13-5

What is the drain voltage in Fig. 13-8a?

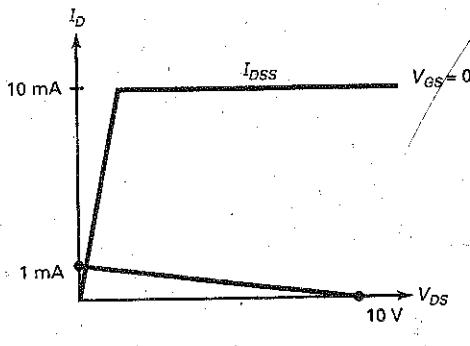
SOLUTION Since $V_P = 4$ V, $V_{GS(off)} = -4$ V. Before point A in time, the input voltage is -10 V and the JFET is cut off. In this case, the drain voltage is:

$$V_D = 10 \text{ V}$$

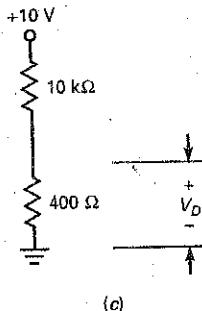
Figure 13-8 Example.



(a)



(b)



(c)

Between points A and B, the input voltage is 0 V. The upper end of the dc load line has a saturation current of:

$$I_{D(\text{sat})} = \frac{10 \text{ V}}{10 \text{ k}\Omega} = 1 \text{ mA}$$

Figure 13-8b shows the dc load line. Since $I_{D(\text{sat})}$ is much less than I_{DSS} , the JFET is in hard saturation.

The ohmic resistance is:

$$R_{DS} = \frac{4 \text{ V}}{10 \text{ mA}} = 400 \Omega$$

In the equivalent circuit of Fig. 13-8c, the drain voltage is:

$$V_D = \frac{400 \Omega}{10 \text{ k}\Omega + 400 \Omega} 10 \text{ V} = 0.385 \text{ V}$$

PRACTICE PROBLEM 13-5 Using Fig. 13-8a, find R_{DS} and V_D if $V_p = 3 \text{ V}$.

13-5 Biasing in the Active Region

JFET amplifiers need to have a Q point in the active region. Because of the large spread in JFET parameters, we cannot use gate bias. Instead, we need to use other biasing methods. Some of these methods are similar to those used with bipolar junction transistors.

The choice of analysis technique depends on the level of accuracy needed. For example, when doing preliminary analysis and troubleshooting of biasing circuits, it is often desirable to use ideal values and circuit approximations. In JFET circuits, this means that we will often ignore V_{GS} values. Usually, the ideal answers will have an error of less than 10 percent. When closer analysis is called for, we can use graphical solutions to determine a circuit's Q point. If you are designing JFET circuits or need even greater accuracy, you should use a circuit simulator like MultiSim (EWB).

Self-Bias

Figure 13-9a shows self-bias. Since drain current flows through the source resistor R_S , a voltage exists between the source and ground, given by:

$$V_S = I_D R_S \quad (13-6)$$

Since V_G is zero,

$$V_{GS} = -I_D R_S \quad (13-7)$$

This says that the gate-source voltage equals the negative of the voltage across the source resistor. Basically, the circuit creates its own bias by using the voltage developed across R_S to reverse bias the gate.

Figure 13-9b shows the effect of different source resistors. There is a medium value of R_S at which the gate-source voltage is half of the cutoff voltage. An approximation for this medium resistance is:

$$R_S \approx R_{DS} \quad (13-8)$$

This equation says that the source resistance should equal the ohmic resistance of the JFET. When this condition is satisfied, the V_{GS} is roughly half the cutoff voltage and the drain current is roughly one-quarter of I_{DSS} .

Figure 13-9 Self-bias.

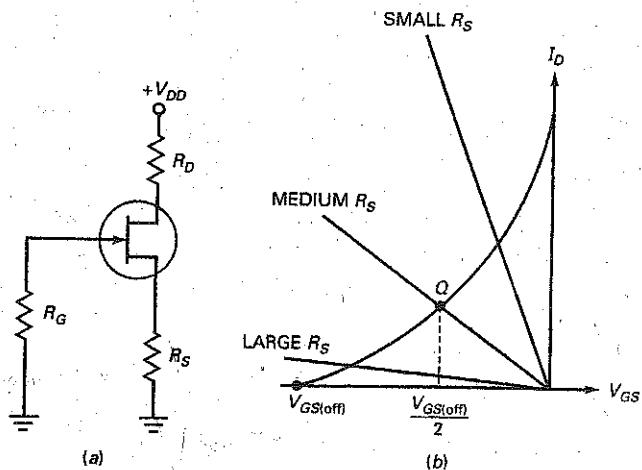
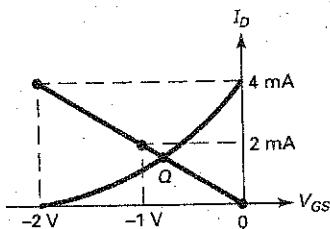


Figure 13-10 Self-bias Q point.



When a JFET's transconductance curves are known, we can analyze a self-bias circuit using graphical methods. Suppose a self-bias JFET has the transconductance curve shown in Fig. 13-10. The maximum drain current is 4 mA, and the gate voltage has to be between 0 and -2 V. By graphing Eq. (13-7), we can find out where it intersects the transconductance curve and determine the values of V_{GS} and I_D . Since Eq. (13-7) is a linear equation, all we have to do is plot two points and draw a line through them.

Suppose the source resistance is 500Ω . Then Eq. (13-7) becomes:

$$V_{GS} = -I_D (500 \Omega)$$

Since any two points can be used, we choose the two convenient points corresponding to $I_D = -(0)(500 \Omega) = 0$, therefore, the coordinates for the first point are $(0, 0)$, which is the origin. To get the second point, find V_{GS} for $I_D = I_{DSS}$. In this case, $I_D = 4 \text{ mA}$ and $V_{GS} = -(4 \text{ mA})(500 \Omega) = -2 \text{ V}$, therefore, the coordinates of the second point are at $(4 \text{ mA}, -2 \text{ V})$.

We now have two points on the graph of Eq. (13-7). The two points are $(0, 0)$ and $(4 \text{ mA}, -2 \text{ V})$. By plotting these two points as shown in Fig. 13-10, we can draw a straight line through the two points as shown. This line will, of course, intersect the transconductance curve. This intersection point is the operating point of the self-biased JFET. As you can see, the drain current is slightly less than 2 mA, and the gate-source voltage is slightly less than -1 V.

In summary, here is a process for finding the Q point of any self-biased JFET, provided you have the transconductance curve. If the curve is not available, you can use the $V_{GS(\text{off})}$ and I_{DSS} rated values, along with the square law equation (13-3), to develop one:

1. Multiply I_{DSS} by R_S to get V_{GS} for the second point.
2. Plot the second point (I_{DSS} , V_{GS}).
3. Draw a line through the origin and the second point.
4. Read the coordinates of the intersection point.

The Q point with self-bias is not extremely stable. Because of this, self-bias is used only with small-signal amplifiers. This is why you may see self-biased JFET circuits near the front end of communication receivers where the signal is small.

Example 13-6

In Fig. 13-11a, what is a medium source resistance using the rule discussed earlier? Estimate the drain voltage with this source resistance.

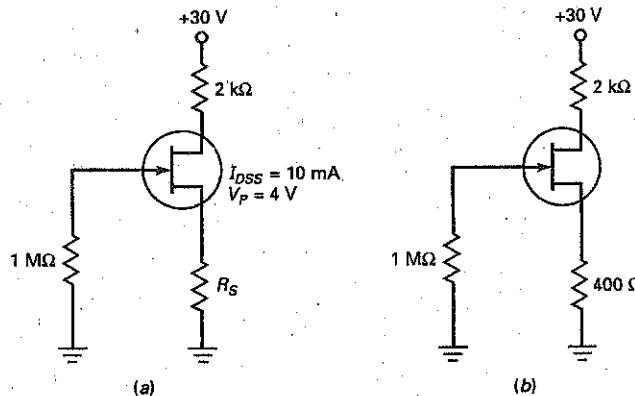
SOLUTION As discussed earlier, self-bias works fine if you use a source resistance equal to the ohmic resistance of the JFET:

$$R_{DS} = \frac{4 \text{ V}}{10 \text{ mA}} = 400 \Omega$$

Figure 13-11b shows a source resistance of 400Ω . In this case, the drain current is around one-quarter of 10 mA, or 2.5 mA, and the drain voltage is roughly:

$$V_D = 30 \text{ V} - (2.5 \text{ mA})(2 \text{ k}\Omega) = 25 \text{ V}$$

Figure 13-11 Example.



PRACTICE PROBLEM 13-6 Repeat Example 13-6 using a JFET with $I_{DSS} = 8 \text{ mA}$. Determine R_S and V_D .

Example 13-7



Using the MultiSim circuit of Fig. 13-12a, along with the minimum and maximum transconductance curves for a 2N5486 JFET shown in Fig. 13-12b, determine the range of V_{GS} and I_D Q point values. Also, what would be the optimum source resistor for this JFET?

SOLUTION First, multiply I_{DSS} by R_S to get V_{GS} :

$$V_{GS} = -(20 \text{ mA})(270 \Omega) = -5.4 \text{ V}$$

Second, plot the second point (I_{DSS} , V_{GS}):

(20 mA, -5.4 V)

Now draw a line through the origin $(0, 0)$ and the second point. Then read the coordinates of the intersection points for the minimum and maximum Q point values.

$$\begin{array}{lll} Q \text{ point (min)} & V_{GS} = -0.8 \text{ V} & I_D = 2.8 \text{ mA} \\ Q \text{ point (max)} & V_{GS} = -2.1 \text{ V} & I_D = 8.0 \text{ mA} \end{array}$$

Note that the MultiSim measured values of Fig. 13-12a are between the minimum and maximum values. The optimum source resistor can be found by:

$$R_S = \frac{V_{GS(\text{off})}}{I_{DSS}} \quad \text{or} \quad R_S = \frac{V_P}{I_{DSS}}$$

using minimum values:

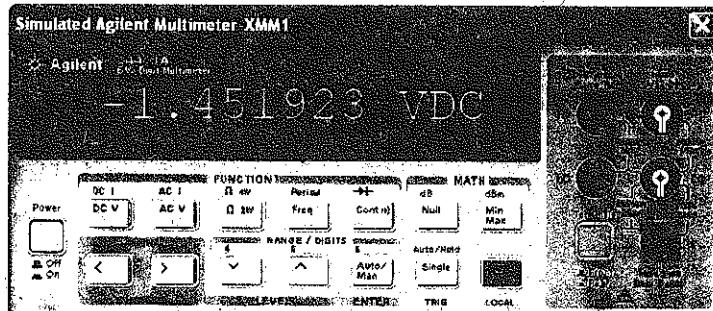
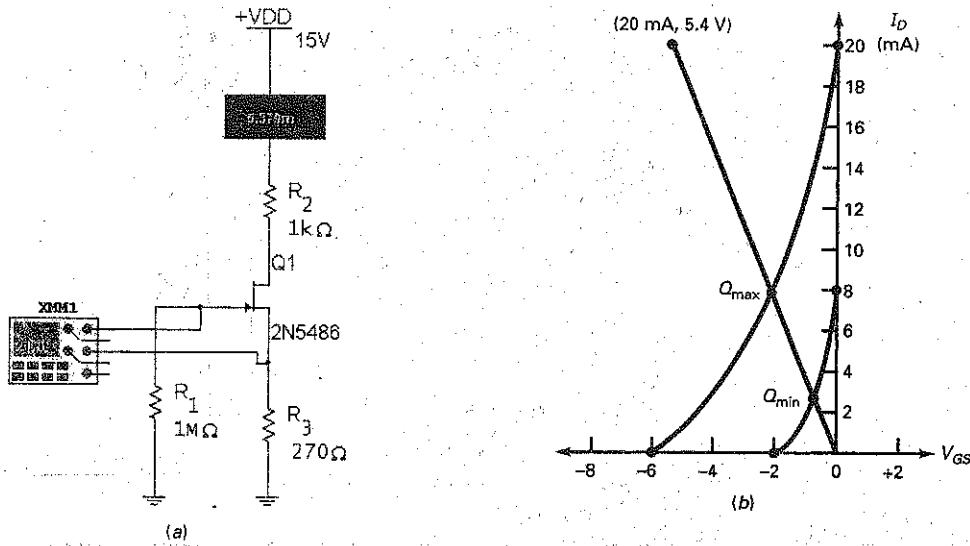
$$R_S = \frac{2 \text{ V}}{8 \text{ mA}} = 250 \Omega$$

using maximum values:

$$R_S = \frac{6\text{ V}}{20\text{ mA}} = 300\Omega$$

Notice the value of R_S in Fig. 13-12a is an approximate midpoint value between $R_{S(\min)}$ and $R_{S(\max)}$.

Figure 13-12 (a) Self-bias example; (b) transconductance curves.



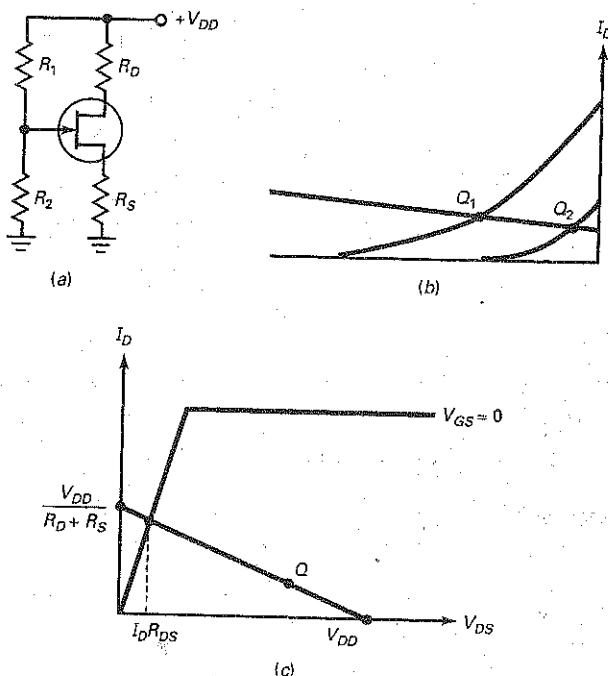
PRACTICE PROBLEM 13-7 In Fig. 13-12a, change R_3 to $390\ \Omega$ and find the Q point values.

Voltage-Divider Bias

Figure 13-13a shows voltage-divider bias. The voltage divider produces a gate voltage that is a fraction of the supply voltage. By subtracting the gate-source voltage, we get the voltage across the source resistor:

$$V_S = V_G - V_{GS} \quad (13-9)$$

Figure 13-13 Voltage-divider bias.



Since V_{GS} is a negative, the source voltage will be slightly larger than the gate voltage. When you divide this source voltage by the source resistance, you get the drain current:

$$I_D = \frac{V_G - V_{GS}}{R_S} \approx \frac{V_G}{R_S} \quad (13-10)$$

When the gate voltage is large, it can swamp out the variations in V_{GS} from one JFET to the next. Ideally, the drain current equals the gate voltage divided by the source resistance. As a result, the drain current is almost constant for any JFET, as shown in Fig. 13-13b.

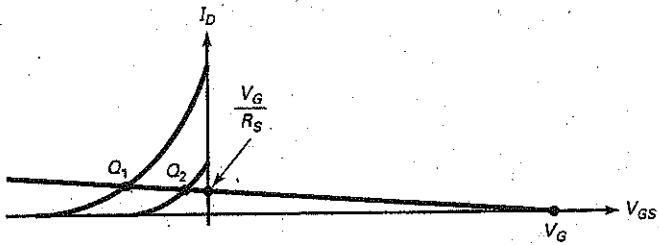
Figure 13-13c shows the dc load line. For an amplifier, the Q point has to be in the active region. This means that V_{DS} must be greater than $I_D R_{DS}$ (ohmic region) and less than V_{DD} (cutoff). When a large supply voltage is available, voltage-divider bias can set up a stable Q point.

When more accuracy is needed in determining the Q point for a voltage-divider bias circuit, a graphical method can be used. This is especially true when the minimum and maximum V_{GS} values for a JFET vary several volts from each other. In Fig. 13-13a, the voltage applied to the gate is

$$V_G = \frac{R_2}{R_1 + R_2} (V_{DD}) \quad (13-11)$$

Using transconductance curves, as in Fig. 13-14, plot the V_G value on the horizontal, or x -axis, of the graph. This becomes one point on our bias line. To get the second point, use Eq. (13-10) with $V_{GS} = 0$ V to determine I_D . This second point, where $I_D = V_G/R_S$, is plotted on the vertical, or y -axis, of the transconductance curve. Next, draw a line between these two points and extend the line so it intersects the transconductance curves. Finally, read the coordinates of the intersection points.

Figure 13-14 VDB Q point.



Example 13-8

Draw the dc load line and the Q point for Fig. 13-15a using ideal methods.

SOLUTION The 3:1 voltage divider produces a gate voltage of 10 V. Ideally, the voltage across the source resistor is:

$$V_S = 10 \text{ V}$$

The drain current is:

$$I_D = \frac{10 \text{ V}}{2 \text{ k}\Omega} = 5 \text{ mA}$$

and the drain voltage is:

$$V_D = 30 \text{ V} - (5 \text{ mA})(1 \text{ k}\Omega) = 25 \text{ V}$$

The drain-source voltage is:

$$V_{DS} = 25 \text{ V} - 10 \text{ V} = 15 \text{ V}$$

The dc saturation current is:

$$I_{D(\text{sat})} = \frac{30 \text{ V}}{3 \text{ k}\Omega} = 10 \text{ mA}$$

and the cutoff voltage is:

$$V_{DS(\text{cutoff})} = 30 \text{ V}$$

Figure 13-15 Example:

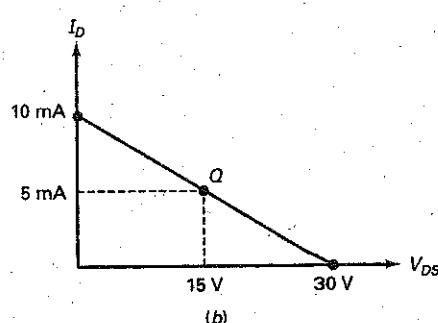
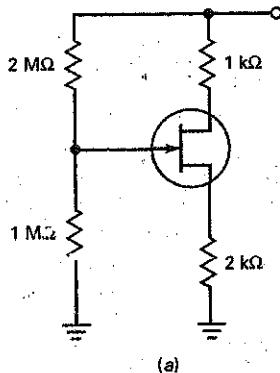


Figure 13-15b shows the dc load line and the Q point.

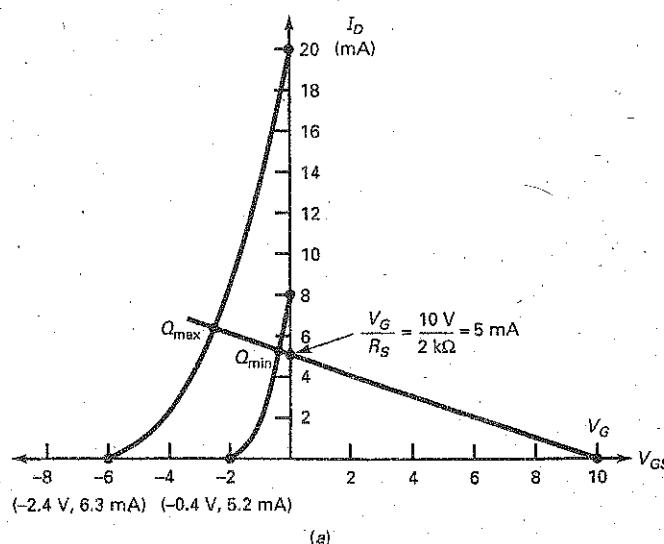
PRACTICE PROBLEM 13-8 In Fig. 13-15, change V_{DD} to 24 V. Solve for I_D and V_{DS} using ideal methods.

Example 13-9

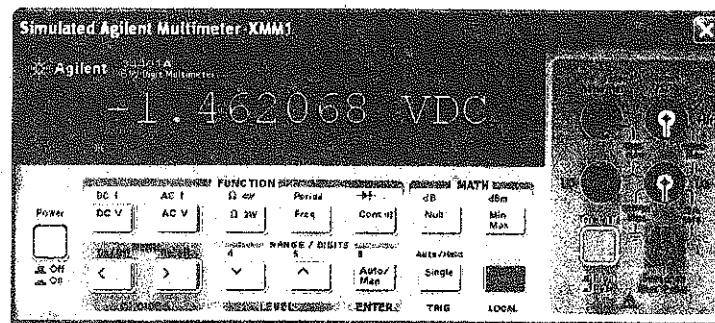
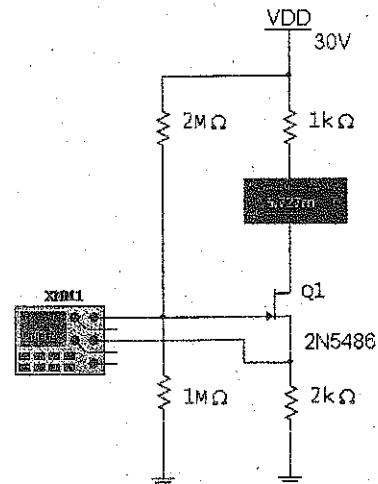
III Multisim

Again using Fig. 13-15a, solve for the minimum and maximum Q point values using the graphical method and transconductance curves for a 2N5486 JFET shown in Fig. 13-16a. How does this compare to the measured values using MultiSim?

Figure 13-16 (a) Transconductance; (b) MultiSim measurements.



(a)



(b)

SOLUTION First, the value of V_G is found by:

$$V_G = \frac{1 \text{ M}\Omega}{2 \text{ M}\Omega + 1 \text{ M}\Omega} (30 \text{ V}) = 10 \text{ V}$$

This value is plotted on the x -axis.

Next, find the second point:

$$I_D = \frac{V_G}{R_S} = \frac{10 \text{ V}}{2 \text{ K}} = 5 \text{ mA}$$

This value is plotted on the y -axis.

By drawing a line between these two points extending through the minimum and maximum transconductance curves, we find:

$$V_{GS(\min)} = -0.4 \text{ V} \quad I_{D(\min)} = 5.2 \text{ mA}$$

and

$$V_{GS(\max)} = -2.4 \text{ V} \quad I_{D(\max)} = 6.3 \text{ mA}$$

Fig. 13-16b shows that the measured MultiSim values fall between the calculated minimum and maximum values.

PRACTICE PROBLEM 13-9 Using Fig. 13-15a, find the maximum I_D value using graphical methods when $V_{DD} = 24 \text{ V}$.

Two-Supply Source Bias

Figure 13-17 shows two-supply source bias. The drain current is given by:

$$I_D = \frac{V_{SS} - V_{GS}}{R_S} \approx \frac{V_{SS}}{R_S} \quad (13-12)$$

Again, the idea is to swamp out the variations in V_{GS} by making V_{SS} much larger than V_{GS} . Ideally, the drain current equals the source supply voltage divided by the source resistance. In this case, the drain current is almost constant in spite of JFET replacement and temperature change.

Current-Source Bias

When the drain supply voltage is not large, there may not be enough gate voltage to swamp out the variations in V_{GS} . In this case, a designer may prefer to use the current-source bias of Fig. 13-18a. In this circuit, the bipolar junction transistor pumps a fixed current through the JFET. The drain current is given by:

$$I_D = \frac{V_{EE} - V_{BE}}{R_E} \quad (13-13)$$

Figure 13-18b illustrates how effective current-source bias is. Both Q points have the same current. Although V_{GS} is different for each Q point, V_{GS} no longer has an effect on the value of drain current.

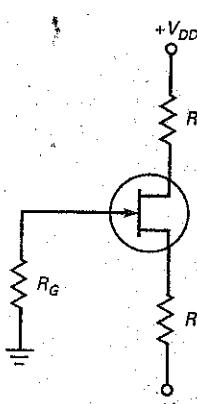
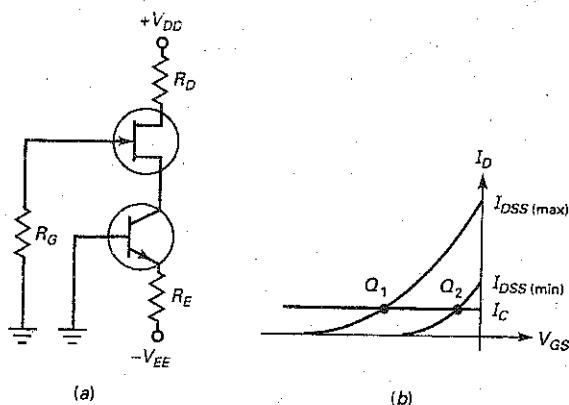


Figure 13-17 Two-supply source bias.

Figure 13-18 Current-source bias.



Example 13-10

What is the drain current in Fig. 13-19a? The voltage between the drain and ground?

SOLUTION Ideally, 15 V appears across the source resistor, producing a drain current of:

$$I_D = \frac{15 \text{ V}}{3 \text{ k}\Omega} = 5 \text{ mA}$$

The drain voltage is:

$$V_D = 15 \text{ V} - (5 \text{ mA})(1 \text{ k}\Omega) = 10 \text{ V}$$

Figure 13-19 Example.

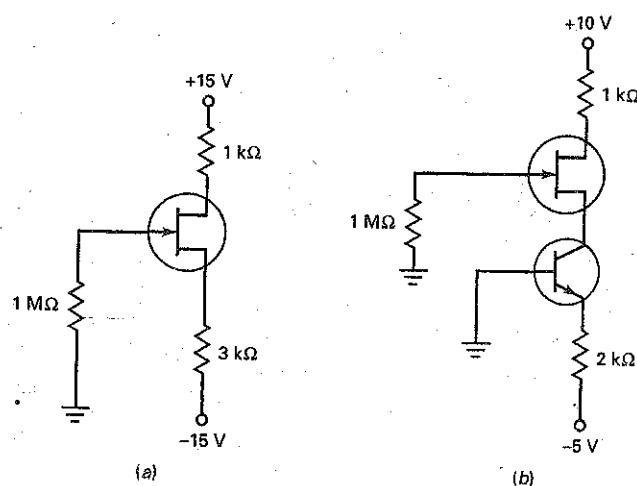
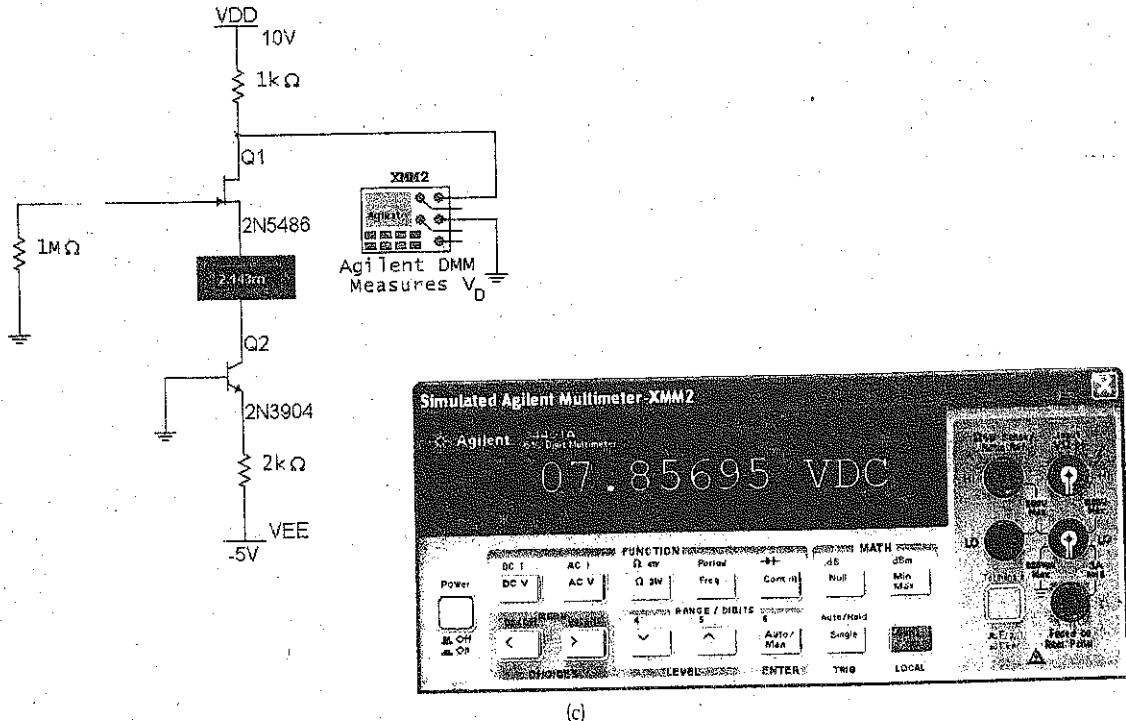


Figure 13-19 (continued)



Example 13-11

Multisim

In Fig. 13-19b, what is the drain current? The drain voltage?

SOLUTION The bipolar junction transistor sets up a drain current of:

$$I_D = \frac{5 \text{ V} - 0.7 \text{ V}}{2 \text{ k}\Omega} = 2.15 \text{ mA}$$

The drain voltage is:

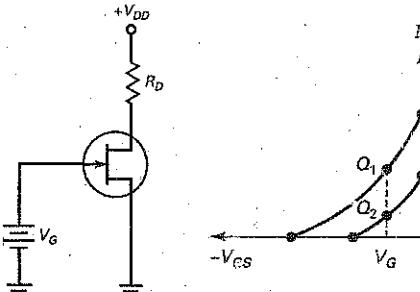
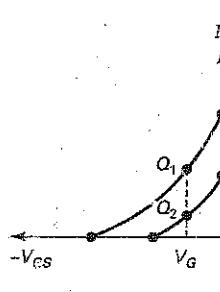
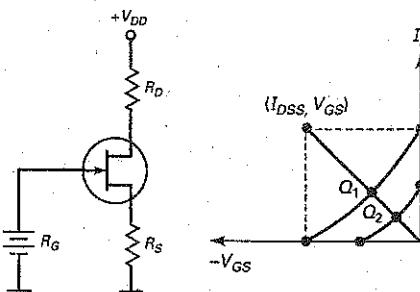
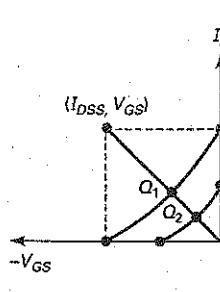
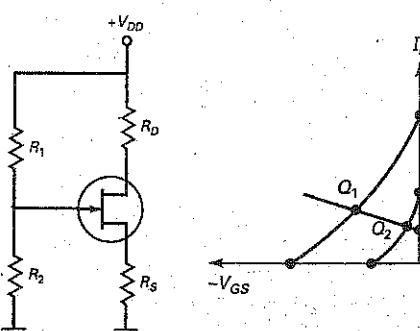
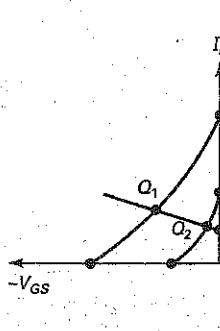
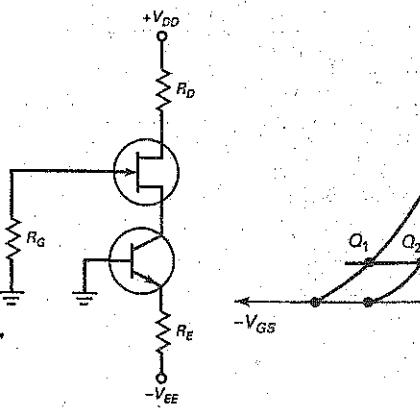
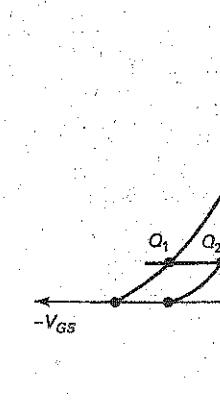
$$V_D = 10 \text{ V} - (2.15 \text{ mA})(1 \text{ k}\Omega) = 7.85 \text{ V}$$

Fig. 13-19c shows how close the Multisim measured values are to the calculated values.

PRACTICE PROBLEM 13-11 Repeat Example 13-11 with $R_E = 1 \text{ k}\Omega$.

Summary Table 13-1 shows the most popular types of JFET bias circuits. The graphical operating points on the transconductance curves should clearly demonstrate the advantage of one biasing technique over another.

Summary Table 13-1 JFET Biasing

Gate bias 		$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2$ $V_{GS} = V_G$ $V_D = V_{DD} - I_D R_D$
Self-bias 		$V_{GS} = -I_D(R_S)$ Second point = $(I_{DSS})(R_S)$
VDB 		$V_G = \frac{R_2}{R_1 + R_2} (V_{DD})$ $I_D = \frac{V_G}{R_S}$ $V_{DS} = V_D - V_S$
Current-source bias 		$I_D = \frac{V_{EE} - V_{BE}}{R_E}$ $V_D = V_{DD} - I_D R_D$

13-6 Transconductance

To analyze JFET amplifiers, we need to discuss **transconductance**, designated g_m and defined as:

$$g_m = \frac{i_d}{v_{gs}} \quad (13-14)$$

This says that transconductance equals the ac drain current divided by the ac gate-source voltage. Transconductance tells us how effective the gate-source voltage is in controlling the drain current. The higher the transconductance, the more control the gate voltage has over the drain current.

For instance, if $i_d = 0.2 \text{ mA pp}$ when $v_{gs} = 0.1 \text{ V pp}$, then:

$$g_m = \frac{0.2 \text{ mA}}{0.1 \text{ V}} = 2(10^{-3}) \text{ mho} = 2000 \mu\text{mho}$$

On the other hand, if $i_d = 1 \text{ mA pp}$ when $v_{gs} = 0.1 \text{ V pp}$, then:

$$g_m = \frac{1 \text{ mA}}{0.1 \text{ V}} = 10,000 \mu\text{mho}$$

In the second case, the higher transconductance means that the gate is more effective in controlling the drain current.

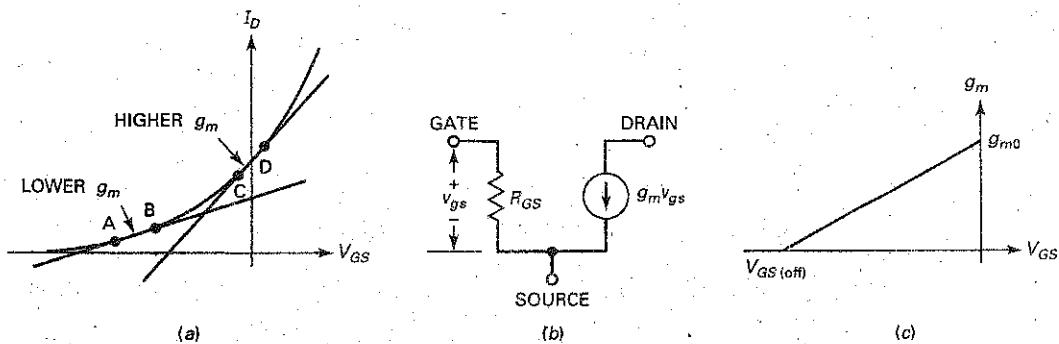
Siemen

The unit *mho* is the ratio of current to voltage. An equivalent and modern unit for the mho is the *siemen* (*S*), so the foregoing answers can be written as $2000 \mu\text{S}$ and $10,000 \mu\text{S}$. On data sheets, either quantity (mho or siemen) may be used. Data sheets may also use the symbol g_{fs} instead of g_m . As an example, the data sheet of a 2N5451 lists a g_{fs} of $2000 \mu\text{S}$ for a drain current of 1 mA . This is identical to saying that the 2N5451 has a g_m of $2000 \mu\text{mho}$ for a drain current of 1 mA .

Slope of Transconductance Curve

Figure 13-20a brings out the meaning of g_m in terms of the transconductance curve. Between points A and B, a change in V_{GS} produces a change in I_D . The change in I_D divided by the change in V_{GS} is the value of g_m between A and B. If

Figure 13-20 (a) Transconductance; (b) ac equivalent circuit; (c) variation of g_m .



we select another pair of points farther up the curve at *C* and *D*, we get a bigger change in I_D for the same change in V_{GS} . Therefore, g_m has a larger value higher up the curve. Stated another way, g_m is the slope of the transconductance curve. The steeper the curve is at the *Q* point, the higher the transconductance.

Figure 13-20b shows an ac equivalent circuit for a JFET. A very high resistance R_{GS} is between the gate and the source. The drain of a JFET acts like a current source with a value of $g_m v_{gs}$. Given the values of g_m and v_{gs} , we can calculate the ac drain current.

Transconductance and Gate-Source Cutoff Voltage

The quantity $V_{GS(\text{off})}$ is difficult to measure accurately. On the other hand, I_{DSS} and g_{m0} are easy to measure with high accuracy. For this reason, $V_{GS(\text{off})}$ is often calculated with the following equation:

$$V_{GS(\text{off})} = \frac{-2I_{DSS}}{g_{m0}} \quad (13-15)$$

In this equation, g_{m0} is the value of transconductance when $V_{GS} = 0$. Typically, a manufacturer will use the foregoing equation to calculate the value of $V_{GS(\text{off})}$ for use on data sheets.

The quantity g_{m0} is the maximum value of g_m for a JFET because it occurs when $V_{GS} = 0$. When V_{GS} becomes negative, g_m decreases. Here is the equation for calculating g_m for any value of V_{GS} :

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right) \quad (13-16)$$

Notice that g_m decreases linearly when V_{GS} becomes more negative, as shown in Fig. 13-20c. Changing the value of g_m is useful in *automatic gain control*, which is discussed later.

Example 13-12

A 2N5457 has $I_{DSS} = 5 \text{ mA}$ and $g_{m0} = 5000 \mu\text{S}$. What is the value of $V_{GS(\text{off})}$? What does g_m equal when $V_{GS} = -1 \text{ V}$?

SOLUTION With Eq. (13-15):

$$V_{GS(\text{off})} = \frac{-2(5 \text{ mA})}{5000 \mu\text{S}} = -2 \text{ V}$$

Next, use Eq. (13-16) to get:

$$g_m = (5000 \mu\text{S}) \left(1 - \frac{-1 \text{ V}}{-2 \text{ V}} \right) = 2500 \mu\text{S}$$

PRACTICE PROBLEM 13-12 Repeat Example 13-12 using $I_{DSS} = 8 \text{ mA}$ and $V_{GS} = -2 \text{ V}$.

13-7 JFET Amplifiers

GOOD TO KNOW

Because of the extremely high input impedance of a JFET, the input current is generally assumed to be 0 μA , and the current gain of a JFET amplifier is an undefined quantity.

GOOD TO KNOW

For any JFET small-signal amplifier, the input signal that drives the gate should never reach a point at which the gate-source junction is forward biased.

Figure 13-21a shows a common-source (CS) amplifier. The coupling and bypass capacitors are ac shorts. Because of this, the signal is coupled directly into the gate. Since the source is bypassed to ground, all of the ac input voltage appears between the gate and the source. This produces an ac drain current. Since the ac drain current flows through the drain resistor, we get an amplified and inverted ac output voltage. This output signal is then coupled to the load resistor.

Voltage Gain of CS Amplifier

Figure 13-21b shows the ac equivalent circuit. The ac drain resistance r_d is defined as:

$$r_d = R_D \parallel R_L$$

The voltage gain is:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_m v_{in} r_d}{v_{in}}$$

which simplifies to:

$$A_v = g_m r_d \quad (13-17)$$

This says that the voltage gain of a CS amplifier equals the transconductance times the ac drain resistance.

Source Follower

Figure 13-22 shows a source follower. The input signal drives the gate, and the output signal is coupled from the source to the load resistor. Like the emitter follower, the source follower has a voltage gain less than 1. The main advantage of the source

Figure 13-21 (a) CS amplifier; (b) ac equivalent circuit.

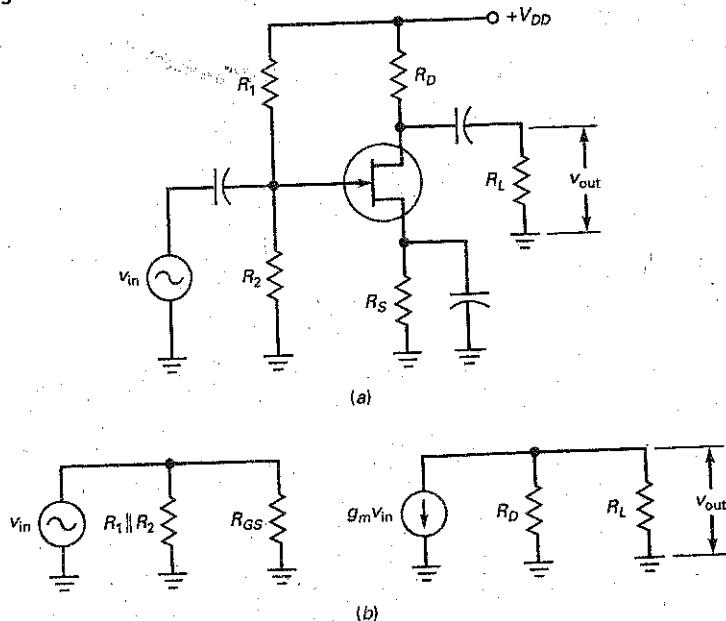
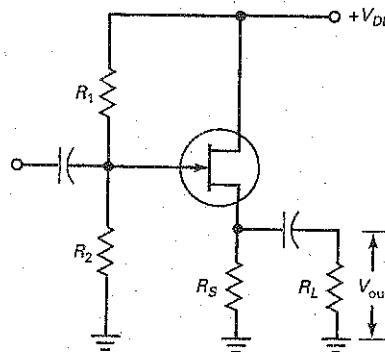


Figure 13-22 Source follower.



follower is its very high input resistance. Often, you will see a source follower used at the front end of a system, followed by bipolar stages of voltage gain.

In Fig. 13-22, the ac source resistance is defined as:

$$r_s = R_S \parallel R_L$$

It is possible to derive this equation for the voltage gain of a source follower:

$$A_v = \frac{g_m r_s}{1 + g_m r_s} \quad (13-18)$$

Because the denominator is always greater than the numerator, the voltage gain is always less than 1.

Example 13-13

Multisim

If $g_m = 5000 \mu S$ in Fig. 13-23, what is the output voltage?

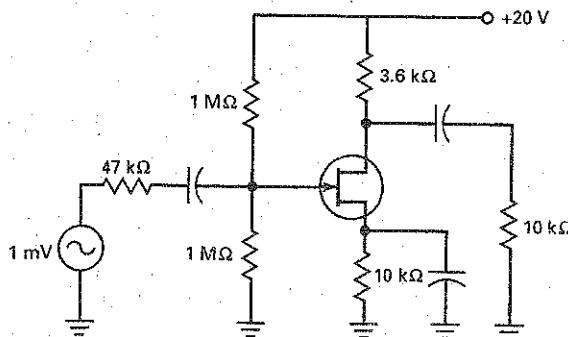
SOLUTION The ac drain resistance is:

$$r_d = 3.6 \text{ k}\Omega \parallel 10 \text{ k}\Omega = 2.65 \text{ k}\Omega$$

The voltage gain is:

$$A_v = (5000 \mu S)(2.65 \text{ k}\Omega) = 13.3$$

Figure 13-23 Example of CS amplifier.



The output voltage is:

$$v_{\text{out}} = 13.3(1 \text{ mV pp}) = 13.3 \text{ mV pp}$$

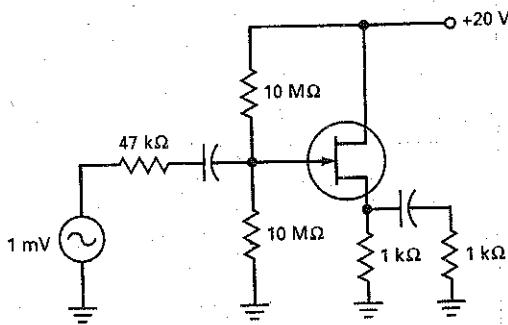
PRACTICE PROBLEM 13-13 Using Fig. 13-23, what is the output voltage if $g_m = 2000 \mu\text{S}$?

Example 13-14

Multisim

If $g_m = 2500 \mu\text{S}$ in Fig. 13-24, what is the output voltage of the source follower?

Figure 13-24 Example of source follower.



SOLUTION The ac source resistance is:

$$r_s = 1 \text{ k}\Omega \parallel 1 \text{ k}\Omega = 500 \text{ }\Omega$$

With Eq. (13-18), the voltage gain is:

$$A_v = \frac{(2500 \mu\text{S})(500 \Omega)}{1 + (2500 \mu\text{S})(500 \Omega)} = 0.556$$

Because the input impedance of the stage is $5 \text{ M}\Omega$, the input signal to the gate is approximately 1 mV. Therefore, the output voltage is:

$$v_{\text{out}} = 0.556(1 \text{ mV}) = 0.556 \text{ mV}$$

PRACTICE PROBLEM 13-14 What is the output voltage of Fig. 13-24 if $g_m = 5000 \mu\text{S}$?

Example 13-15

Multisim

Figure 13-25 includes a variable resistor of $1 \text{ k}\Omega$. If this is adjusted to 780Ω , what is the voltage gain?

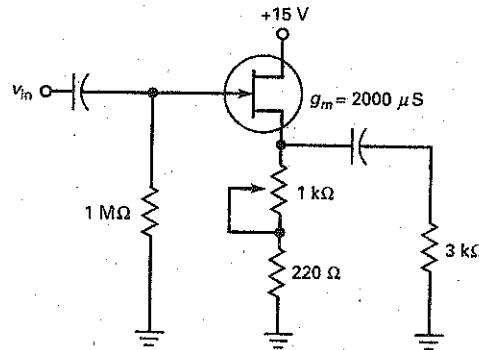
SOLUTION The total dc source resistance is:

$$R_S = 780 \Omega + 220 \Omega = 1 \text{ k}\Omega$$

The ac source resistance is:

$$r_s = 1 \text{ k}\Omega \parallel 3 \text{ k}\Omega = 750 \Omega$$

Figure 13-25 Example.



The voltage gain is:

$$A_v = \frac{(2000 \mu S)(750 \Omega)}{1 + (2000 \mu S)(750 \Omega)} = 0.6$$

PRACTICE PROBLEM 13-15 Using Fig. 13-25, what is the maximum voltage gain possible when adjusting the variable resistor?

Example 13-16

III Multisim

In Fig. 13-26, what is the drain current? The voltage gain?

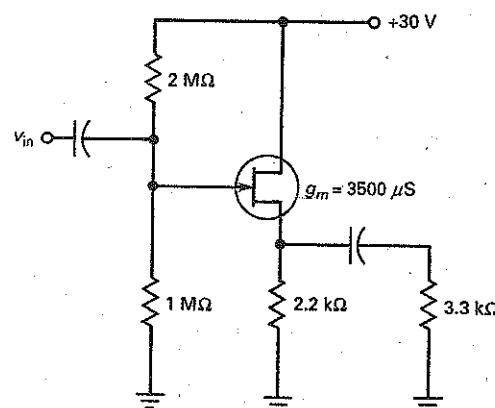
SOLUTION The 3:1 voltage divider produces a dc gate voltage of 10 V. Ideally, the drain current is:

$$I_D = \frac{10 \text{ V}}{2.2 \text{ k}\Omega} = 4.55 \text{ mA}$$

The ac source resistance is:

$$r_s = 2.2 \text{ k}\Omega \parallel 3.3 \text{ k}\Omega = 1.32 \text{ k}\Omega$$

Figure 13-26 Example.



The voltage gain is:

$$A_v = \frac{(3500 \mu\text{S})(1.32 \text{ k}\Omega)}{1 + (3500 \mu\text{S})(1.32 \text{ k}\Omega)} = 0.822$$

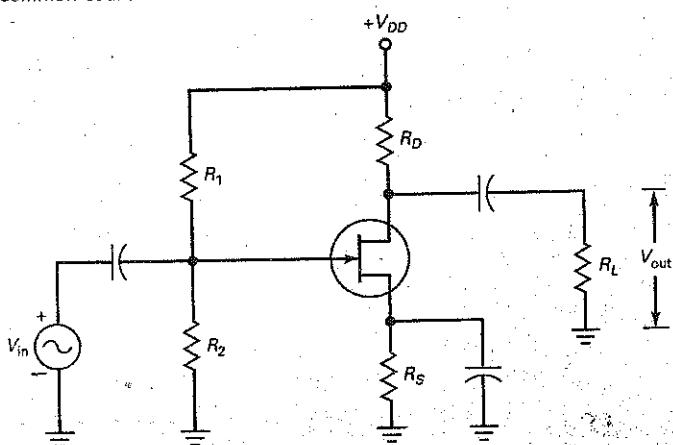
PRACTICE PROBLEM 13-16 In Fig. 13-26, what would the voltage gain change to if the 3.3 kΩ resistor opened?

Summary Table 13-2 shows the common-source and source follower amplifier configurations and equations.

Summary Table 13-2 JFET Amplifiers

Circuit

Common-source



Characteristics

$$V_G = \frac{R_1}{R_1 + R_2} (V_{DD})$$

$V_S \approx V_G$ or use graphical method

$$I_D = \frac{V_S}{R_S} \quad V_D = V_{DD} - I_D R_D$$

$$V_{GS(\text{off})} = \frac{-2I_{DSS}}{g_m}$$

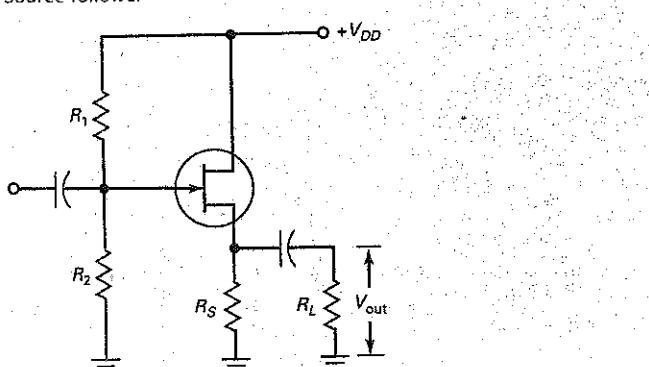
$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)$$

$$r_d = R_D \parallel R_L$$

$$A_v = g_m r_d$$

Phase shift = 180°

Source follower



$$V_G = \frac{R_1}{R_1 + R_2} (V_{DD})$$

$V_S \approx V_G$ or use graphical method

$$I_D = \frac{V_S}{R_S} \quad V_{DS} = V_{DD} - V_S$$

$$V_{GS(\text{off})} = \frac{-2I_{DSS}}{g_m}$$

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)$$

$$A_v = \frac{g_m r_s}{1 + g_m r_s}$$

Phase shift = 0°

13-8 The JFET Analog Switch

Besides the source follower, another major application of the JFET is *analog switching*. In this application, the JFET acts as a switch that either transmits or blocks a small ac signal. To get this type of action, the gate-source voltage V_{GS} has only two values: either zero or a value that is greater than $V_{GS(\text{off})}$. In this way, the JFET operates either in the ohmic region or in the cutoff region.

Shunt Switch

GOOD TO KNOW

The ohmic resistance of a JFET can be determined for any value of V_{GS} by using the following equation:

$$R_{DS} = \frac{R_{DS(\text{on})}}{1 - V_{GS}/V_{GS(\text{off})}}$$

where $R_{DS(\text{on})}$ is the ohmic resistance when V_{DS} is small and $V_{GS} = 0$.

$$R_D \gg R_{DS}$$

When V_{GS} is high, the JFET operates in the ohmic region and the switch of Fig. 13-27b is closed. Since R_{DS} is much smaller than R_D , v_{out} is much smaller than v_{in} . When V_{GS} is low, the JFET cuts off and the switch of Fig. 13-27b opens. In this case, $v_{out} = v_{in}$. Therefore, the JFET shunt switch either transmits the ac signal or blocks it.

Series Switch

Figure 13-27c shows a JFET series switch, and Fig. 13-27d is its equivalent circuit. When V_{GS} is high, the switch is closed and the JFET is equivalent to a resistance of R_{DS} . In this case, the output approximately equals the input. When V_{GS} is low, the JFET is open and v_{out} is approximately zero.

Figure 13-27 JFET analog switches: (a) Shunt type; (b) shunt equivalent circuit; (c) series type; (d) series equivalent circuit.

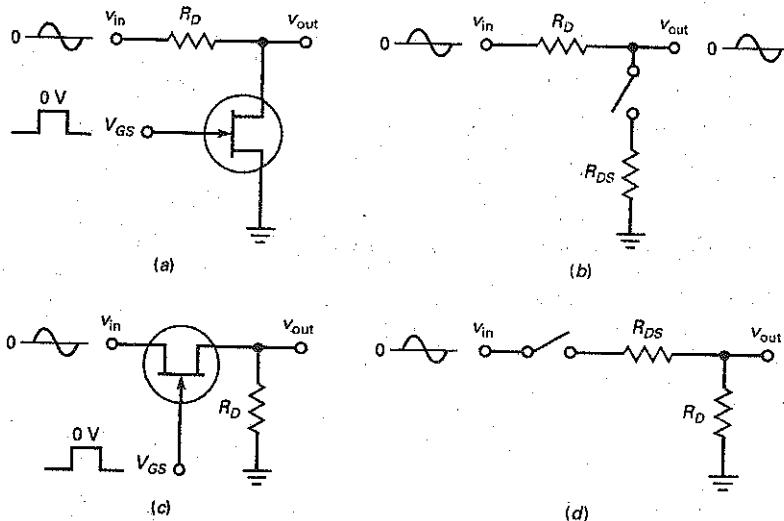
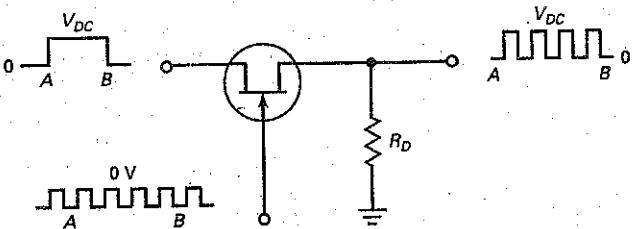


Figure 13-28 Chopper.



The on-off ratio of a switch is defined as the maximum output voltage divided by the minimum output voltage:

$$\text{On-off ratio} = \frac{V_{\text{out(max)}}}{V_{\text{out(min)}}} \quad (13-19)$$

When a high on-off ratio is important, the JFET series switch is a better choice because its on-off ratio is higher than that of the JFET shunt switch.

Chopper

Figure 13-28 shows a JFET chopper. The gate voltage is a continuous square wave that continuously switches the JFET on and off. The input voltage is a rectangular pulse with a value of V_{DC} . Because of the square wave on the gate, the output is *chopped* (switched on and off), as shown.

A JFET chopper can use either a shunt or a series switch. Basically, the circuit converts a dc input voltage to a square-wave output. The peak value of the chopped output is V_{DC} . As will be described later, a JFET chopper can be used to build a *dc amplifier*, a circuit that can amplify frequencies all the way down to zero frequencies.

Example 13-17

A JFET shunt switch has $R_D = 10 \text{ k}\Omega$, $I_{DSS} = 10 \text{ mA}$, and $V_{GS(\text{off})} = -2 \text{ V}$. If $v_{in} = 10 \text{ mV pp}$, what are output voltages? What is the on-off ratio?

SOLUTION The ohmic resistance is:

$$R_{DS} = \frac{2 \text{ V}}{10 \text{ mA}} = 200 \Omega$$

Figure 13-29a shows the equivalent circuit when the JFET is conducting. The output voltage is:

$$v_{\text{out}} = \frac{200 \Omega}{10.2 \text{ k}\Omega} (10 \text{ mV pp}) = 0.196 \text{ mV pp}$$

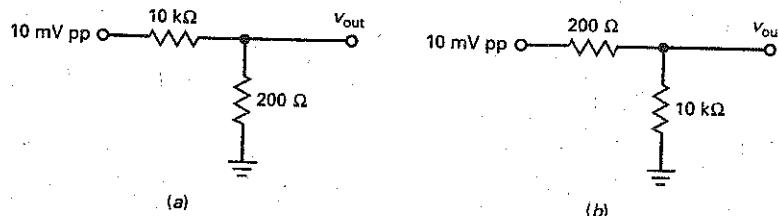
When the JFET is off:

$$v_{\text{out}} = 10 \text{ mV pp}$$

The on-off ratio is:

$$\text{On-off ratio} = \frac{10 \text{ mV pp}}{0.196 \text{ mV pp}} = 51$$

Figure 13-29 Examples.



PRACTICE PROBLEM 13-17 Repeat Example 13-17 using a $V_{GS(\text{off})}$ value of -4 V .

Example 13-18

A JFET series switch has the same data as in the preceding example. What are output voltages? If the JFET has a resistance of $10 \text{ M}\Omega$ when off, what is the on-off ratio?

SOLUTION Figure 13-29b shows the equivalent circuit when the JFET is conducting. The output voltage is:

$$v_{\text{out}} = \frac{10 \text{ k}\Omega}{10.2 \text{ k}\Omega} (10 \text{ mV pp}) = 9.8 \text{ mV pp}$$

When the JFET is off:

$$v_{\text{out}} = \frac{10 \text{ k}\Omega}{10 \text{ M}\Omega} (10 \text{ mV pp}) = 10 \mu\text{V pp}$$

The on-off ratio of the switch is:

$$\text{On-off ratio} = \frac{9.8 \text{ mV pp}}{10 \mu\text{V pp}} = 980$$

Compare this to the preceding example, and you can see that a series switch has a better on-off ratio.

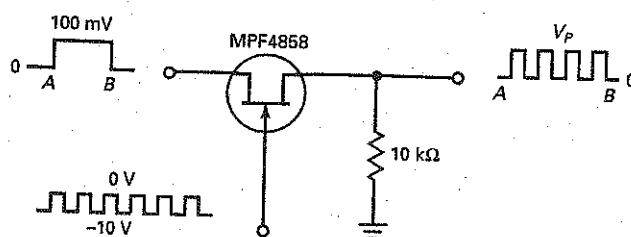
PRACTICE PROBLEM 13-18 Repeat Example 13-18 using a $V_{GS(\text{off})}$ value of -4 V .

Example 13-19

Multisim

The square wave on the gate of Fig. 13-30 has a frequency of 20 kHz . What is the frequency of the chopped output? If the MPF4858 has an R_{DS} of 50Ω , what is the peak value of the chopped output?

Figure 13-30 Example of chopper.



SOLUTION The output frequency is the same as the chopping or gate frequency:

$$f_{out} = 20 \text{ kHz}$$

Since $50\ \Omega$ is much smaller than $10\text{ k}\Omega$, almost all the input voltage reaches the output:

$$V_{peak} = \frac{10\text{ k}\Omega}{10\text{ k}\Omega + 50\ \Omega} (100 \text{ mV}) = 99.5 \text{ mV}$$

PRACTICE PROBLEM 13-19 Using Fig. 13-30 and a R_{DS} value of $100\ \Omega$, determine the peak value of the chopped output.

13-9 Other JFET Applications

A JFET cannot compete with a bipolar transistor for most amplifier applications. But its unusual properties make it a better choice in special applications. In this section, we discuss those applications where a JFET has a clear-cut advantage over the bipolar transistor.

Multiplexing

Multiplex means "many into one." Figure 13-31 shows an *analog multiplexer*, a circuit that steers one or more of the input signals to the output line. Each JFET acts like a series switch. The control signals (V_1 , V_2 , and V_3) turn the JFETs on and off. When a control signal is high, its input signal is transmitted to the output.

For instance, if V_1 is high and the others are low, the output is a sine wave. If V_2 is high and the others are low, the output is a triangular wave. When V_3 is the high input, the output is a square wave. Normally, only one of the control signals is high; this ensures that only one of the input signals is transmitted to the output.

Figure 13-31 Multiplexer.

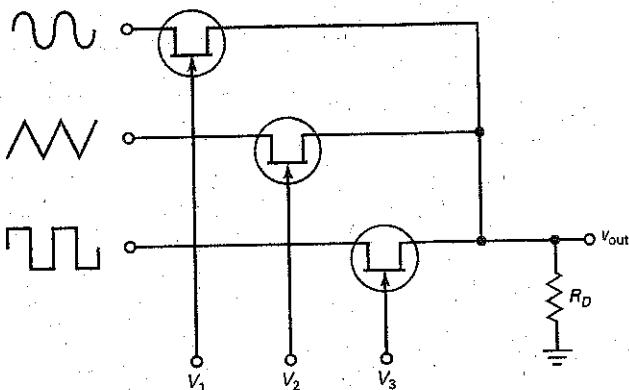
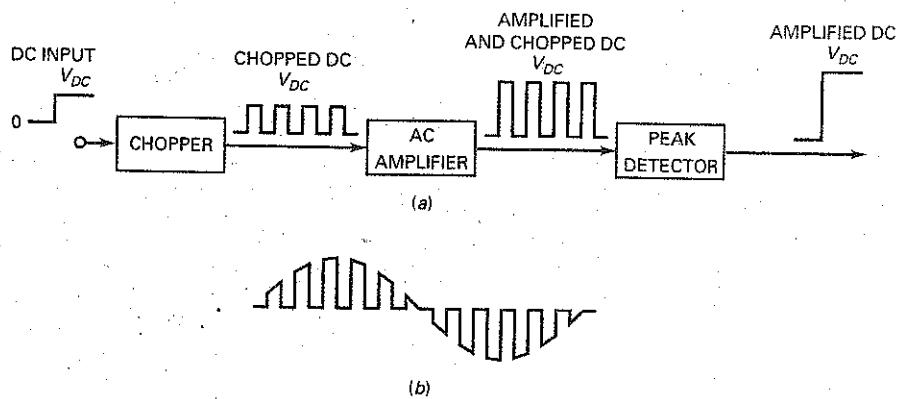


Figure 13-32 Chopper amplifier.



Chopper Amplifiers

We can build a direct-coupled amplifier by leaving out the coupling and bypass capacitors and connecting the output of each stage directly to the input of the next stage. In this way, dc voltages are coupled, as are ac voltages. Circuits that can amplify dc signals are called *dc amplifiers*. The major disadvantage of direct coupling is *drift*, a slow shift in the final dc output voltage produced by minor changes in supply voltage, transistor parameters, and temperature variations.

Figure 13-32a shows one way to overcome the drift problem of direct coupling. Instead of using direct coupling, we use a JFET chopper to convert the input dc voltage to a square wave. The peak value of this square wave equals V_{DC} . Because the square wave is an ac signal, we can use a conventional ac amplifier, one with coupling and bypass capacitors. The amplified output can then be peak-detected to recover an amplified dc signal.

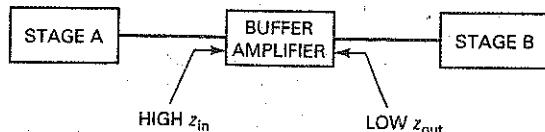
A chopper amplifier can amplify low-frequency signals as well as dc signals. If the input is a low-frequency signal, it gets chopped into the ac waveform of Fig. 13-32b. This chopped signal can be amplified by an ac amplifier. The amplified signal can then be peak-detected to recover the original input signal.

Buffer Amplifier

Figure 13-33 shows a buffer amplifier, a stage that isolates the preceding stage from the following stage. Ideally, a buffer should have a high input impedance. If it does, almost all the Thevenin voltage from stage A appears at the buffer input. The buffer should also have a low output impedance. This ensures that all its output voltage reaches the input of stage B.

The source follower is an excellent buffer amplifier because of its high input impedance (well into the megohms at low frequencies) and its low output impedance (typically a few hundred ohms). The high input impedance means

Figure 13-33 Buffer amplifiers isolates stages A and B.



light loading of stage A. The low output impedance means that the buffer can drive heavy loads (small load resistances).

Low-Noise Amplifier

Noise is any unwanted disturbance superimposed on a useful signal. Noise interferes with the information contained in the signal. For instance, the noise in television receivers produces small white or black spots on the picture. Severe noise can wipe out the picture altogether. Similarly, the noise in radio receivers produces crackling and hissing, which sometimes completely masks the signal. Noise is independent of the signal because it exists even when the signal is off.

The JFET is an outstanding low-noise device because it produces much less noise than a bipolar junction transistor. Low noise is very important at the front end of receivers because the later stages amplify front-end noise along with the signal. If we use a JFET amplifier at the front end, we get less amplified noise at the final output.

Other circuits near the front end of receivers include *frequency mixers* and *oscillators*. A frequency mixer is a circuit that converts a higher frequency to a lower one. An oscillator is a circuit that generates an ac signal. JFETs are often used for VHF/UHF amplifiers, mixers, and oscillators. *VHF* stands for "very high frequencies" (30 to 300 MHz), and *UHF*, for "ultra high frequencies" (300 to 3000 MHz).

Voltage-Controlled Resistance

When a JFET operates in the ohmic region, it usually has $V_{GS} = 0$ to ensure hard saturation. But there is an exception. It is possible to operate a JFET in the ohmic region with V_{GS} values between 0 and $V_{GS(\text{off})}$. In this case, the JFET can act like a *voltage-controlled resistance*.

Figure 13-34 shows the drain curves of a 2N5951 near the origin with V_{DS} less than 100 mV. In this region, the small-signal resistance r_{ds} is defined as the drain voltage divided by the drain current:

$$r_{ds} = \frac{V_{DS}}{I_D} \quad (13-20)$$

In Fig. 13-34, you can see that r_{ds} depends on which V_{GS} curve is used. For $V_{GS} = 0$, r_{ds} is minimum and equals R_{DS} . As V_{GS} becomes more negative, r_{ds} increases and becomes greater than R_{DS} .

For instance, when $V_{GS} = 0$ in Fig. 13-34, we can calculate:

$$r_{ds} = \frac{100 \text{ mV}}{0.8 \text{ mA}} = 125 \Omega$$

When $V_{GS} = -2 \text{ V}$:

$$r_{ds} = \frac{100 \text{ mV}}{0.4 \text{ mA}} = 250 \Omega$$

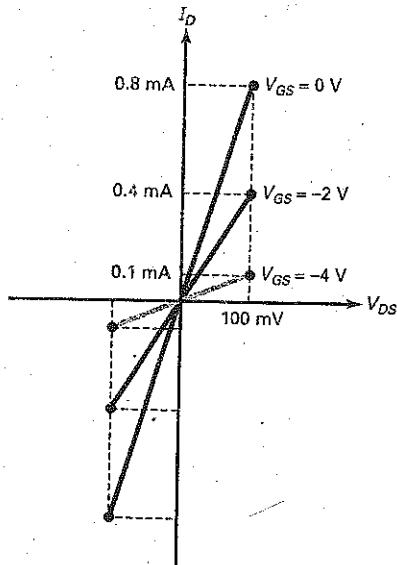
When $V_{GS} = -4 \text{ V}$:

$$r_{ds} = \frac{100 \text{ mV}}{0.1 \text{ mA}} = 1 \text{ k}\Omega$$

This means that a JFET acts like a voltage-controlled resistance in the ohmic region.

Recall that a JFET is a symmetrical device at low frequencies since either end can act like the source or the drain. This is why the drain curves of Fig. 13-34 extend on both sides of the origin. This means that a JFET can be used as a voltage-controlled resistance for small ac signals, typically those with a

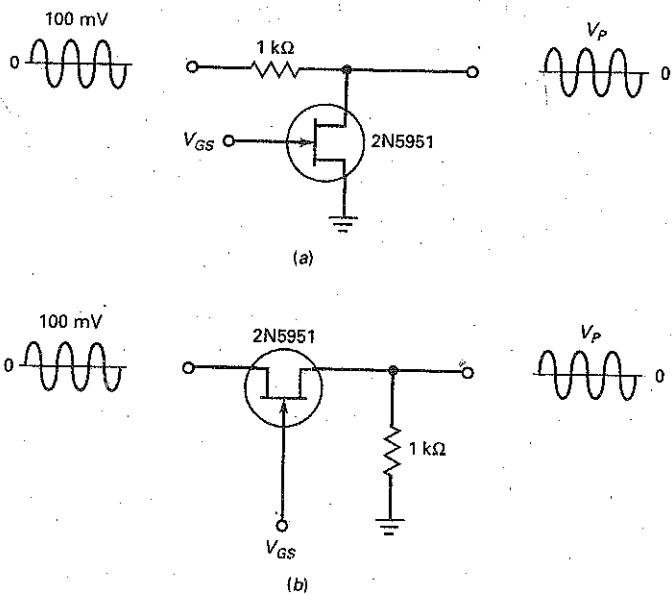
Figure 13-34 Small-signal r_{ds} is voltage-controlled.



peak-to-peak value of less than 200 mV. When it is used in this way, the JFET does not need a dc drain voltage from the supply because the small ac signal supplies the drain voltage.

Figure 13-35a shows a shunt circuit where the JFET is used as a voltage-controlled resistance. This circuit is identical to the JFET shunt switch discussed earlier. The difference is that the control voltage V_{GS} does not swing from 0 to a

Figure 13-35 Example of voltage-controlled resistance.



large negative value. Instead, V_{GS} can vary continuously; that is, it can have any value between 0 and $V_{GS(\text{off})}$. In this way, V_{GS} controls the resistance of the JFET, which then changes the peak output voltage.

Figure 13-35b is a series circuit with the JFET used as a voltage-controlled resistance. The basic idea is the same. When you change V_{GS} , you change the ac resistance of the JFET, which changes the peak output voltage.

As calculated earlier, when $V_{GS} = 0$ V, the 2N5951 has a small-signal resistance of:

$$r_{ds} = 125 \Omega$$

In Fig. 13-35a, this means that the voltage divider produces a peak output voltage of:

$$V_p = \frac{125 \Omega}{1.125 \text{ k}\Omega} (100 \text{ mV}) = 11.1 \text{ mV}$$

If V_{GS} is changed to -2 V, r_{ds} increases to 250 Ω , and the peak output increases to:

$$V_p = \frac{250 \Omega}{1.25 \text{ k}\Omega} (100 \text{ mV}) = 20 \text{ mV}$$

When V_{GS} is changed to -4 V, r_{ds} increases to 1 k Ω , and the peak output increases to:

$$V_p = \frac{1 \text{ k}\Omega}{2 \text{ k}\Omega} (100 \text{ mV}) = 50 \text{ mV}$$

Automatic Gain Control

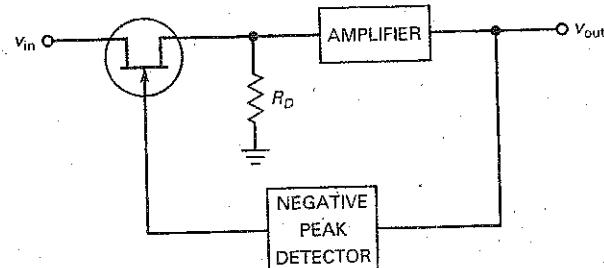
When a receiver is tuned from a weak to a strong station, the loudspeaker will blare (become loud) unless the volume is immediately decreased. The volume may also change because of fading, a decrease in signal caused by a change in the path between the transmitter and receiver. To prevent unwanted changes in the volume, most modern receivers use automatic gain control (AGC).

Figure 13-36 illustrates the basic idea of AGC. An input signal v_{in} passes through a JFET used as a voltage-controlled resistance. The signal is amplified to get the output voltage v_{out} . The output signal is fed back to a negative peak detector. The output of this peak detector then supplies the V_{GS} for the JFET.

If the input signal suddenly increases by a large amount, the output voltage will increase. This means that a larger negative voltage comes out of the peak detector. Since V_{GS} is more negative, the JFET has a higher ohmic resistance, which reduces the signal to the amplifier and decreases the output signal.

On the other hand, if the input signal fades, the output voltage decreases and the negative peak detector produces a smaller output. Since V_{GS} is less negative,

Figure 13-36 Automatic gain control.



the JFET transmits more signal voltage to the amplifier, which raises the final output. Therefore, the effect of any sudden change in the input signal is offset or at least reduced by the AGC action.

Another AGC Example

As shown earlier, the g_m of a JFET decreases when V_{GS} becomes more negative. The equation is:

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)$$

This is a linear equation. When it is graphed, it results in Fig. 13-37a. For a JFET, g_m reaches a maximum value when $V_{GS} = 0$. As V_{GS} becomes more negative, the value of g_m decreases. Since a CS amplifier has a voltage gain of:

$$A_v = g_m r_d$$

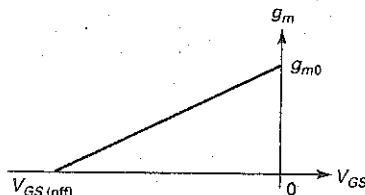
we can control the voltage gain by controlling the value of g_m .

Figure 13-37b shows how it's done. A JFET amplifier is near the front end of a receiver. It has a voltage gain of $g_m r_d$. Subsequent stages amplify the JFET output. This amplified output goes into a negative peak detector that produces voltage V_{AGC} . This negative voltage is applied to the gate of the CS amplifier.

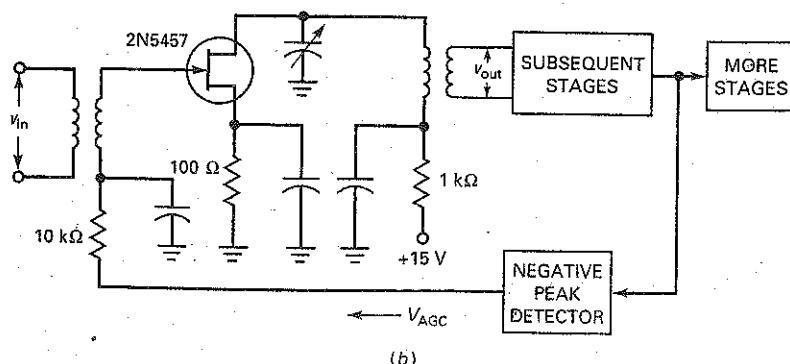
When the receiver is tuned from a weak to a strong station, a larger signal is peak-detected and V_{AGC} becomes more negative. This reduces the gain of the JFET amplifier. Conversely, if the signal fades, less AGC voltage is applied to the gate and the JFET stage produces a larger output signal.

The overall effect of AGC is this: The final output signal changes, but not nearly as much as it would without AGC. For instance, in some AGC systems an increase of 100 percent in the input signal results in an increase of less than 1 percent in the final output signal.

Figure 13-37 AGC used with receiver.

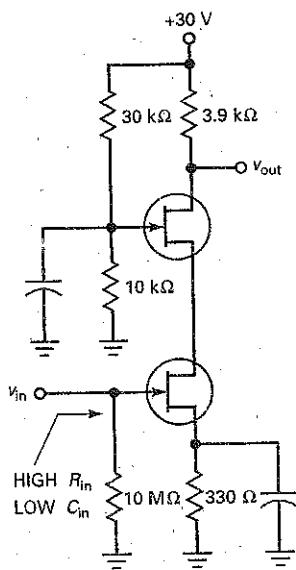


(a)



(b)

Figure 13-38 Cascode amplifier.



Cascode Amplifier

Figure 13-38 is an example of a cascode amplifier. It can be shown that the overall voltage gain of this two-FET connection is:

$$A_v = g_m r_d$$

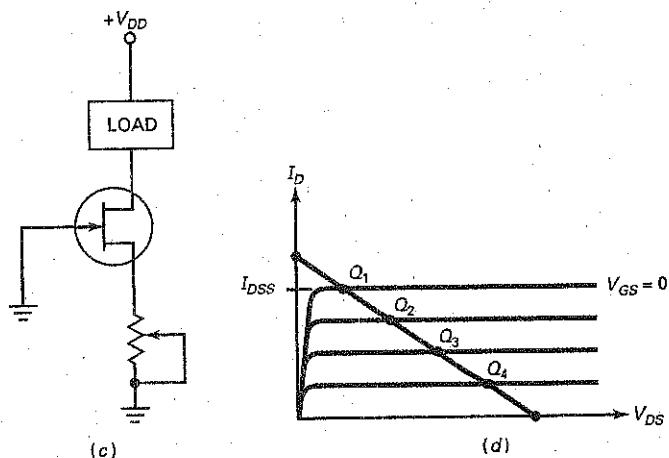
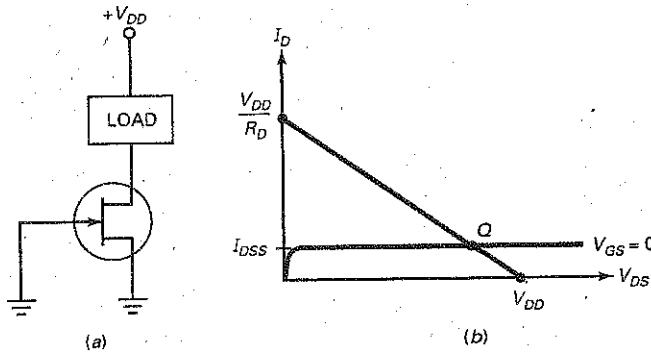
This is the same voltage gain as for a CS amplifier.

The advantage of the circuit is its low input capacitance, which is important with VHF and UHF signals. At these higher frequencies, the input capacitance becomes a limiting factor on the voltage gain. With a cascode amplifier, the low input capacitance allows the circuit to amplify higher frequencies than are possible with only a CS amplifier. Chapter 16 will mathematically analyze the effect of capacitance on high-frequency operation.

Current Sourcing

Suppose you have a load that requires a constant current. One solution is to use a shorted-gate JFET to supply the constant current. Figure 13-39a shows the basic idea. If the Q point is in the active region, as shown in Fig. 13-39b, the load current equals I_{DSS} . If the load can tolerate the change in I_D when JFETs are replaced, the circuit is an excellent solution.

Figure 13-39 JFET used as current source.



On the other hand, if the constant load current must have a specific value, we can use an adjustable source resistor, as shown in Fig. 13-39c. The self-bias will produce negative values of V_{GS} . By adjusting the resistor, we can set up different Q points, as shown in Fig. 13-39d.

Using JFETs like this is a simple way to produce a fixed load current, one that is constant even though the load resistance changes. In later chapters, we will discuss other ways to produce fixed load currents using op amps.

Current Limiting

Instead of sourcing current, a JFET can limit current. Figure 13-40a shows how. In this application, the JFET operates in the ohmic region rather than the active region. To ensure operation in the ohmic region, the designer selects values to get the dc load line of Fig. 13-40b. The normal Q point is in the ohmic region, and the normal load current is approximately V_{DD}/R_D .

If the load becomes shorted, the dc load line becomes vertical. In this case, the Q point changes to the new position shown in Fig. 13-40b. With this Q point, the current is limited to I_{DSS} . The point to remember is that a shorted load usually produces an excessive current. But with the JFET in series with the load, the current is limited to a safe value.

Conclusion

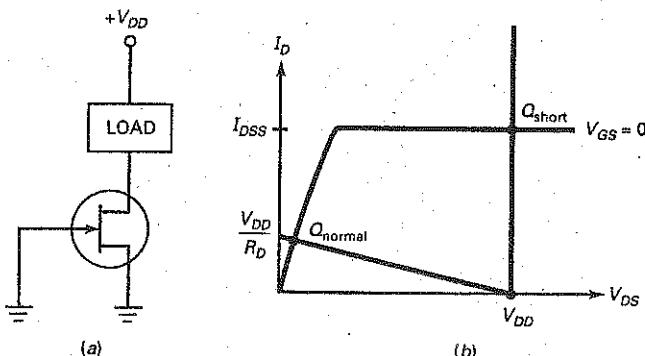
Look at Summary Table 13-3. Some of the terms are new and will be discussed in later chapters. The JFET buffer has the advantage of high input impedance and low output impedance. This is why the JFET is the natural choice at the front end of voltmeters, oscilloscopes, and other, similar equipment where you need high input resistances ($10 \text{ M}\Omega$ or more). As a guide, the input resistance at the gate of a JFET is more than $100 \text{ M}\Omega$.

When a JFET is used as a small-signal amplifier, its output voltage is linearly related to the input voltage because only a small part of the transconductance curve is used. Near the front end of television and radio receivers, the signals are small. Therefore, JFETs are often used as RF amplifiers.

But with larger signals, more of the transconductance curve is used, resulting in square-law distortion. This nonlinear distortion is unwanted in an amplifier. But in a frequency mixer, square-law distortion has a big advantage. This is why the JFET is preferred to the bipolar junction transistor for FM and television mixer applications.

As indicated in Summary Table 13-3, JFETs are also useful in AGC amplifiers, cascode amplifiers, choppers, voltage-controlled resistors, audio amplifiers, and oscillators.

Figure 13-40 JFET limits current if load shorts.



Summary Table 13-3 JFET Applications

Application	Main Advantage	Uses
Buffer	High Z_{in} , low Z_{out}	General-purpose measuring equipment, receivers
RF amplifier	Low noise	FM tuners, communication equipment
RF mixer	Low distortion	FM and television receivers, communication equipment
AGC amplifier	Ease of gain control	Receivers, signal generators
Cascode amplifier	Low input capacitance	Measuring instruments, test equipment
Chopper amplifier	No drift	DC amplifiers, guidance control systems
Variable resistor	Voltage-controlled	Op amps, organ tone controls
Audio amplifier	Small coupling capacitors	Hearing aids, inductive transducers
RF oscillator	Minimum frequency drift	Frequency standards, receivers

13-10 Reading Data Sheets

JFET data sheets are similar to bipolar junction data sheets. You will find maximum ratings, dc characteristics, ac characteristics, mechanical data, and so on. As usual, a good place to start is with the maximum ratings because these are the limits on the JFET currents, voltages, and other quantities.

Breakdown Ratings

As shown in Fig. 13-41, the data sheet of the MPF102 gives these maximum ratings:

V_{DS}	25 V
V_{GS}	-25 V
P_D	350 mW

As usual, a conservative design includes a safety factor for all of these maximum ratings.

As discussed earlier, the derating factor tells you how much to reduce the power rating of a device. The derating factor of an MPF102 is given as 2.8 mW/ $^{\circ}\text{C}$. This means that you have to reduce the power rating by 2.8 mW for each degree above 25°C.

I_{DSS} and $V_{GS(\text{off})}$

Two of the most important pieces of information on the data sheet of a depletion-mode device are the maximum drain current and the gate-source cutoff voltage. These values are given on the data sheet of the MPF102:

Symbol	Minimum	Maximum
$V_{GS(\text{off})}$	-	-8 V
I_{DSS}	2 mA	20 mA

Notice the 10 : 1 spread in I_{DSS} . This large spread is one of the reasons for using ideal approximations with a preliminary analysis of JFET circuits. Another reason

Figure 13-41 MPF102 data sheet.

ON Semiconductor™

JFET VHF Amplifier N-Channel – Depletion

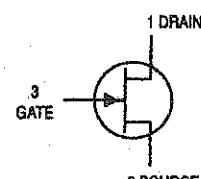
MPF102

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V _{DS}	25	Vdc
Drain–Gate Voltage	V _{DG}	25	Vdc
Gate–Source Voltage	V _{GS}	-25	Vdc
Gate Current	I _G	10	mAdc
Total Device Dissipation @ T _A = 25°C Derate above 25°C	P _D	350 2.8	mW mW/°C
Junction Temperature Range	T _J	125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C



CASE 29-11, STYLE 5
TO-92 (TO-226AA)



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate–Source Breakdown Voltage (I _G = -10 μAdc, V _{DS} = 0)	V _{(BR)GSS}	-25	-	Vdc
Gate Reverse Current (V _{GS} = -15 Vdc, V _{DS} = 0) (V _{GS} = -15 Vdc, V _{DS} = 0, T _A = 100°C)	I _{GSS}	- -	-2.0 -2.0	nAdc μAdc
Gate–Source Cutoff Voltage (V _{DS} = 15 Vdc, I _D = 2.0 nAdc)	V _{GS(off)}	-	-8.0	Vdc
Gate–Source Voltage (V _{DS} = 15 Vdc, I _D = 0.2 mAdc)	V _{GS}	-0.5	-7.5	Vdc
ON CHARACTERISTICS				
Zero–Gate–Voltage Drain Current ¹ (V _{DS} = 15 Vdc, V _{GS} = 0 Vdc)	I _{DS}	2.0	20	mAdc

SMALL-SIGNAL CHARACTERISTICS

Forward Transfer Admittance ¹ (V _{DS} = 15 Vdc, V _{GS} = 0, f = 1.0 kHz) (V _{DS} = 15 Vdc, V _{GS} = 0, f = 100 MHz)	y _{fs}	2000 1600	7500 -	μmhos
Input Admittance (V _{DS} = 15 Vdc, V _{GS} = 0, f = 100 MHz)	Re(y _{IS})	-	800	μmhos
Output Conductance (V _{DS} = 15 Vdc, V _{GS} = 0, f = 100 MHz)	Re(y _{OS})	-	200	μmhos
Input Capacitance (V _{DS} = 15 Vdc, V _{GS} = 0, f = 1.0 MHz)	C _{IS}	-	7.0	pF
Reverse Transfer Capacitance (V _{DS} = 15 Vdc, V _{GS} = 0, f = 1.0 MHz)	C _{RS}	-	3.0	pF

1. Pulse Test; Pulse Width ≤ 630 ms, Duty Cycle ≤ 10%.

Table 13-1 JFET Sampler

Device	$V_{GS(\text{off})}$, V	I_{DSS} , mA	g_m , μS	R_{DS} , Ω	Application
J202	-4	4.5	2,250	888	Audio
2N5668	-4	5	2,500	800	RF
MPF3822	-6	10	3,333	600	Audio
2N5459	-8	16	4,000	500	Audio
MPF102	-8	20	5,000	400	RF
J309	-4	30	15,000	133	RF
BF246B	-14	140	20,000	100	Switching
MPF4857	-6	100	33,000	60	Switching
MPF4858	-4	80	40,000	50	Switching

for using ideal approximations is this: Data sheets often omit values, so you really have no idea what some values may be. In the case of the MPF102, the minimum value of $V_{GS(\text{off})}$ is not listed on the data sheet.

Another important static characteristic of a JFET is I_{GSS} , which is the gate current when the gate-source junction is reverse biased. This current value allows us to determine the dc input resistance of the JFET. As shown on the data sheet, a MPF102 has an I_{GSS} value of 2 nAdc when $V_{GS} = -15$ V. Under these conditions, the gate-source resistance is $R = 15 \text{ V}/2 \text{ nA} = 7500 \text{ M}\Omega$.

Table of JFETs

Table 13-1 shows a sample of different JFETs. The data are sorted in ascending order for g_m . The data sheets for these JFETs show that some are optimized for use at audio frequencies and others for use at RF frequencies. The last three JFETs are optimized for switching applications.

JFETs are small-signal devices because their power dissipation is usually a watt or less. In audio applications, JFETs are often used as source followers. In RF applications, they are used as VHF/UHF amplifiers, mixers, and oscillators. In switching applications, they are typically used as analog switches.

13-11 JFET Testing

The data sheet for the MPF102 shows a maximum gate current I_G of 10 mA. This is the maximum forward gate-to-source or gate-to-drain current the JFET can handle. This can occur if the gate to channel *pn* junction becomes forward biased. If you are testing a JFET using an ohmmeter or digital multimeter on the diode test range, be sure that your meter doesn't cause excessive gate current. Many analog VOMs will provide approximately 100 mA in the $R \times 1$ range. The $R \times 100$ range generally results in a current of 1–2 mA. Most DMMs output a constant 1–2 mA of current when in the diode test range. This should allow safe testing of a JFET's gate-to-source and gate-to-drain *pn* junctions. To check the JFET's drain-to-source

channel resistance, connect the gate lead to the source lead. Otherwise, you will get erratic measurements due to the electric field produced in the channel.

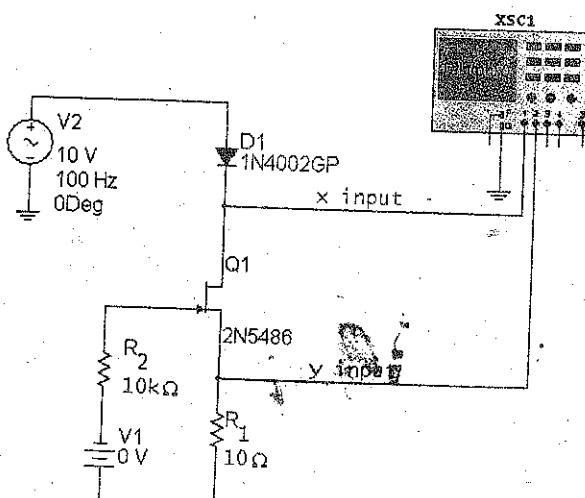
If you have a semiconductor curve tracer available, the JFET can be tested to display its drain curves. A simple test circuit using Multisim, shown in Fig. 13-42a, can also be used to display one drain curve at a time. By using the x-y display capability of most oscilloscopes, a drain curve similar to Fig. 13-42b can be displayed. By varying the reverse-bias voltage of V_1 , you can determine the approximate I_{DSS} and $V_{GS(\text{off})}$ values.

For example, as shown in Fig. 13-42a, the oscilloscope's y-input is connected across a $10\ \Omega$ source resistor. With the oscilloscope's vertical input set to $50\ \text{mV}/\text{division}$, this results in a vertical drain current measurement of

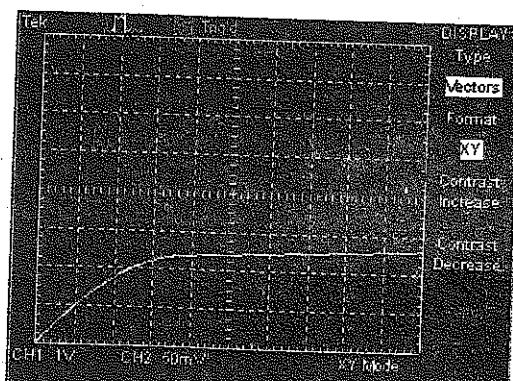
$$I_D = \frac{50\ \text{mV}/\text{div.}}{10\ \Omega} = 5\ \text{mA}/\text{div}$$

With V_1 adjusted to 0 V, the resulting I_D value (I_{DSS}) is approximately 12 mA. $V_{GS(\text{off})}$ can be found by increasing V_1 until I_D is zero.

Figure 13-42 (a) JFET test circuit; (b) drain curve.



(a)



(b)

Summary

SEC. 13-1 BASIC IDEAS

The junction FET, abbreviated *JFET*, has a source, gate, and drain. The JFET has two diodes: the gate-source diode and the gate-drain diode. For normal operation, the gate-source diode is reverse biased. Then, the gate voltage controls the drain current.

SEC. 13-2 DRAIN CURVES

Maximum drain current occurs when the gate-source voltage is zero. The pinchoff voltage separates the ohmic and active regions for $V_{GS} = 0$. The gate-source cutoff voltage has the same magnitude as the pinchoff voltage. $V_{GS(off)}$ turns the JFET off.

SEC. 13-3 THE TRANSCONDUCTANCE CURVE

This is a graph of drain current versus gate-source voltage. The drain current increases more rapidly as V_{GS} approaches zero. Because the equation for drain current contains a squared quantity, JFETs are referred to as *square-law* devices. The normalized transconductance curve shows that I_D equals one-quarter of maximum when V_{GS} equals half of cutoff.

SEC. 13-4 BIASING IN THE OHMIC REGION

Gate bias is used to bias a JFET in the ohmic region. When it operates in the ohmic region, a JFET is equivalent to a small resistance of R_{DS} . To ensure operation in the ohmic region, the JFET

is driven into hard saturation by using $V_{GS} = 0$ and $I_{D(sat)} \ll I_{DSS}$.

SEC. 13-5 BIASING IN THE ACTIVE REGION

When the gate voltage is much larger than V_{GS} , voltage-divider bias can set up a stable Q point in the active region. When positive and negative supply voltages are available, two-supply source bias can be used to swamp out the variations in V_{GS} and set up a stable Q point. When supply voltages are not large, current-source bias can be used to get a stable Q point. Self-bias is used only with small-signal amplifiers because the Q point is less stable than with the other biasing methods.

SEC. 13-6 TRANSCONDUCTANCE

Transconductance g_m tells us how effective the gate voltage is in controlling the drain current. The quantity g_m is the slope of the transconductance curve, which increases as V_{GS} approaches zero. Data sheets may list g_B and siemens, which are equivalent to g_m and mhos.

SEC. 13-7 JFET AMPLIFIERS

A CS amplifier has a voltage gain of $g_m R_d$ and produces an inverted output signal. One of the most important uses of a JFET amplifier is the source follower, which is often used at the front end of systems because of its high input resistance.

SEC. 13-8 THE JFET ANALOG SWITCH

In this application, the JFET acts like a switch that either transmits or blocks

a small ac signal. To get this type of action, the JFET is biased into hard saturation or cutoff, depending on whether V_{GS} is high or low. JFET shunt and series switches are used. The series type has a higher on-off ratio.

SEC. 13-9 OTHER JFET APPLICATIONS

JFETs are used in multiplexers (ohmic), chopper amplifiers (ohmic), buffer amplifiers (active), voltage-controlled resistors (ohmic), AGC circuits (ohmic), cascode amplifiers (active), current sources (active), and current limiters (ohmic and active).

SEC. 13-10 READING DATA SHEETS

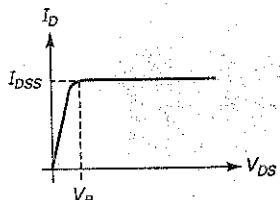
JFETs are mainly small-signal devices because most JFETs have a power rating of less than 1 W. When reading data sheets, start with the maximum ratings. Sometimes data sheets omit the minimum $V_{GS(off)}$ or other parameters. The large spread in JFET parameters justifies using ideal approximations for preliminary analysis and troubleshooting.

SEC. 13-11 JFET TESTING

JFETs can be tested using an ohmmeter or DMM on the diode test range. Care must be taken not to exceed the JFET's current limits. Curve tracers and circuits can be used to display a JFET's dynamic characteristics.

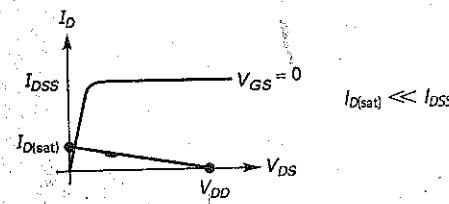
Definitions

(13-1) Ohmic resistance at pinchoff:

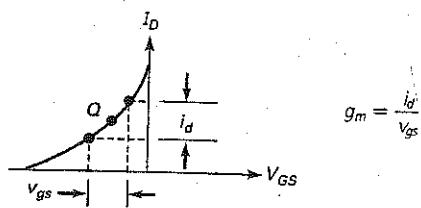


$$R_{DS} = \frac{V_p}{I_{DSS}}$$

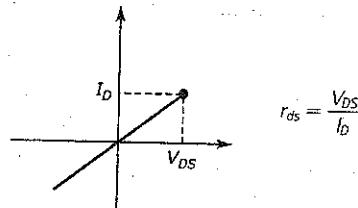
(13-5) Hard saturation:



(13-13) Transconductance:

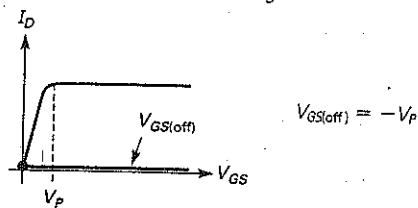


(13-19) Ohmic resistance near origin:

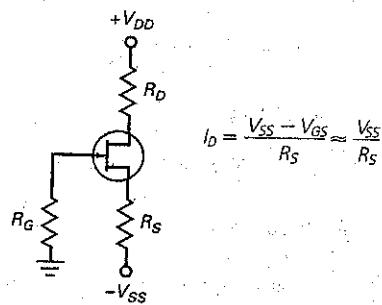


Derivations

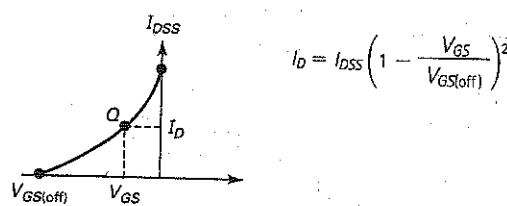
(13-2) Gate-source cutoff voltage:



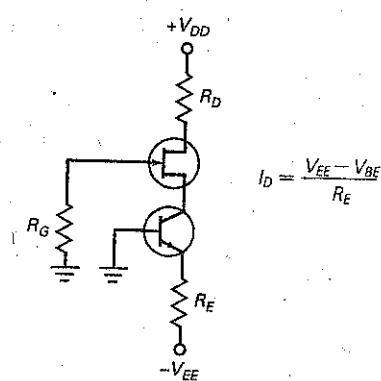
(13-12) Source bias:



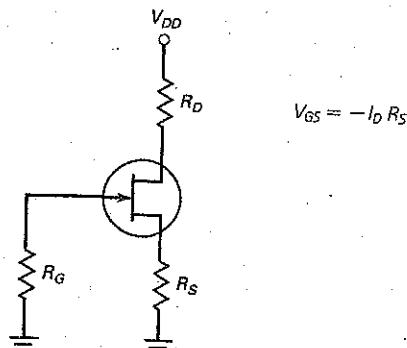
(13-3) Drain current:



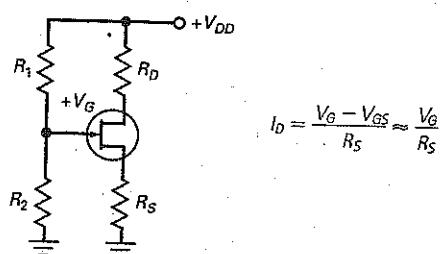
(13-13) Current-source bias:



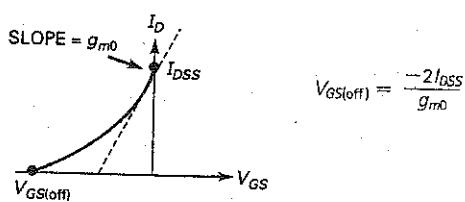
(13-7) Self-bias:



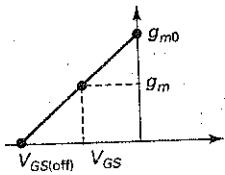
(13-10) Voltage-divider bias:



(13-15) Gate cutoff voltage:

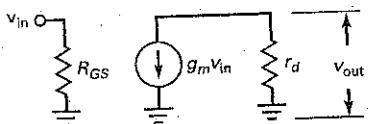


(13-16) Transconductance:



$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)$$

(13-17) CS voltage gain:

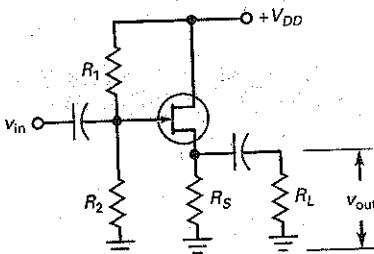


$$A_v = g_m r_d$$

Student Assignments

1. A JFET
 - a. Is a voltage-controlled device
 - b. Is a current-controlled device
 - c. Has a low input resistance
 - d. Has a very large voltage gain
2. A unipolar transistor uses
 - a. Both free electrons and holes
 - b. Only free electrons
 - c. Only holes
 - d. Either one or the other, but not both
3. The input impedance of a JFET
 - a. Approaches zero
 - b. Approaches one
 - c. Approaches infinity
 - d. Is impossible to predict
4. The gate controls
 - a. The width of the channel
 - b. The drain current
 - c. The gate voltage
 - d. All the above
5. The gate-source diode of a JFET should be
 - a. Forward biased
 - b. Reverse biased
 - c. Either forward or reverse biased
 - d. None of the above
6. Compared to a bipolar junction transistor, the JFET has a much higher
 - a. Voltage gain
 - b. Input resistance
7. The pinchoff voltage has the same magnitude as the
 - a. Gate voltage
 - b. Drain-source voltage
 - c. Gate-source voltage
 - d. Gate-source cutoff voltage
8. When the drain saturation current is less than I_{DSS} , a JFET acts like a
 - a. Bipolar junction transistor
 - b. Current source
 - c. Resistor
 - d. Battery
9. R_{DS} equals pinchoff voltage divided by
 - a. Drain current
 - b. Gate current
 - c. Ideal drain current
 - d. Drain current for zero gate voltage
10. The transconductance curve is
 - a. Linear
 - b. Similar to the graph of a resistor
 - c. Nonlinear
 - d. Like a single drain curve
11. The transconductance increases when the drain current approaches
 - a. 0
 - b. $I_{D(\text{sat})}$
 - c. I_{DSS}
 - d. I_S
12. A CS amplifier has a voltage gain of
 - a. $g_m r_d$
 - b. $g_m r_s$
 - c. $g_m r_s / (1 + g_m r_s)$
 - d. $g_m r_d / (1 + g_m r_s)$
13. A source follower has a voltage gain of
 - a. $g_m r_d$
 - b. $g_m r_s$
 - c. $g_m r_s / (1 + g_m r_s)$
 - d. $g_m r_d / (1 + g_m r_d)$
14. When the input signal is large, a source follower has
 - a. A voltage gain of less than 1
 - b. Some distortion
 - c. A high input resistance
 - d. All of these
15. The input signal used with a JFET analog switch should be
 - a. Small
 - b. Large
 - c. A square wave
 - d. Chopped
16. A cascode amplifier has the advantage of
 - a. Large voltage gain
 - b. Low input capacitance
 - c. Low input impedance
 - d. Higher g_m
17. VHF covers frequencies from
 - a. 300 kHz to 3 MHz
 - b. 3 to 30 MHz
 - c. 30 to 300 MHz
 - d. 300 MHz to 3 GHz

(13-18) Source follower:



$$A_v = \frac{g_m r_s}{1 + g_m r_s}$$

18. When a JFET is cut off, the depletion layers are
- Far apart
 - Close together
 - Touching
 - Conducting
19. When the gate voltage becomes more negative in an *n*-channel JFET, the channel between the depletion layers
- Shrinks
 - Expands
 - Conducts
 - Stops conducting
20. If a JFET has $I_{DSS} = 8 \text{ mA}$ and $V_P = 4 \text{ V}$, then R_{DS} equals
- 200Ω
 - 320Ω
 - 500Ω
 - $5 \text{ k}\Omega$
21. The easiest way to bias a JFET in the ohmic region is with
- Voltage-divider bias
 - Self-bias
 - Gate bias
 - Source bias
22. Self-bias produces
- Positive feedback
 - Negative feedback
 - Forward feedback
 - Reverse feedback
23. To get a negative gate-source voltage in a self-biased JFET circuit, you must have a
- Voltage divider
 - Source resistor
 - Ground
 - Negative gate supply voltage
24. Transconductance is measured in
- Ohms
 - Amperes
 - Volts
 - Mhos or siemens
25. Transconductance indicates how effectively the input voltage controls the
- Voltage gain
 - Input resistance
 - Supply voltage
 - Output current

Problems

SEC. 13-1 BASIC IDEAS

13-1 A 2N5458 has a gate current of 1 nA when the reverse voltage is -15 V . What is the input resistance of the gate?

13-2 A 2N5640 has a gate current of $1 \mu\text{A}$ when the reverse voltage is -20 V and the ambient temperature is 100°C . What is the input resistance of the gate?

SEC. 13-2 DRAIN CURVES

13-3 A JFET has $I_{DSS} = 20 \text{ mA}$ and $V_P = 4 \text{ V}$. What is the maximum drain current? The gate-source cutoff voltage? The value of R_{DS} ?

13-4 A 2N5555 has $I_{DSS} = 16 \text{ mA}$ and $V_{GS(off)} = -2 \text{ V}$. What is the pinchoff voltage for this JFET? What is the drain-source resistance R_{DS} ?

13-5 A 2N5457 has $I_{DSS} = 1$ to 5 mA and $V_{GS(off)} = -0.5$ to -6 V . What are the minimum and maximum values of R_{DS} ?

SEC. 13-3 THE TRANSCONDUCTANCE CURVE

13-6 A 2N5462 has $I_{DSS} = 16 \text{ mA}$ and $V_{GS(off)} = -6 \text{ V}$. What are the gate voltage and drain current at the half cutoff point?

13-7 A 2N5670 has $I_{DSS} = 10 \text{ mA}$ and $V_{GS(off)} = -4 \text{ V}$. What are the gate voltage and drain current at the half cutoff point?

13-8 If a 2N5486 has $I_{DSS} = 14 \text{ mA}$ and $V_{GS(off)} = -4 \text{ V}$, what is the drain current when $V_{GS} = -1 \text{ V}$? When $V_{GS} = -3 \text{ V}$?

SEC. 13-4 BIASING IN THE OHMIC REGION

13-9 What is the drain saturation current in Fig. 13-43a? The drain voltage?

13-10 If the $10\text{-k}\Omega$ resistor of Fig. 13-43a is increased to $20\text{k}\Omega$, what is the drain voltage?

13-11 What is the drain voltage in Fig. 13-43b?

13-12 If the $20\text{-k}\Omega$ resistor of Fig. 13-43b is decreased to $10\text{k}\Omega$, what is the drain saturation current? The drain voltage?

SEC. 13-5 BIASING IN THE ACTIVE REGION

For Problems 13-13 through 13-20, use preliminary analysis.

13-13 What is the ideal drain voltage in Fig. 13-44a?

13-14 Draw the dc load line and *Q* point for Fig. 13-44a.

13-15 What is the ideal drain voltage in Fig. 13-44b?

13-16 If the $18\text{k}\Omega$ of Fig. 13-44b is changed to $30\text{k}\Omega$, what is the drain voltage?

13-17 In Fig. 13-45a, what is the drain current? The drain voltage?

Figure 13-43

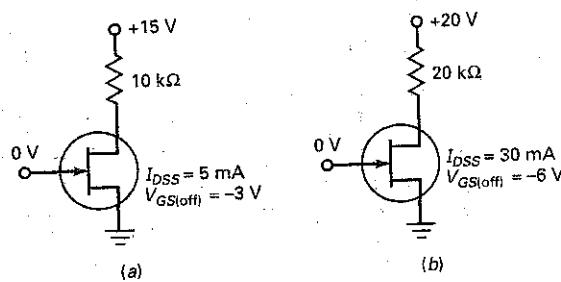


Figure 13-44

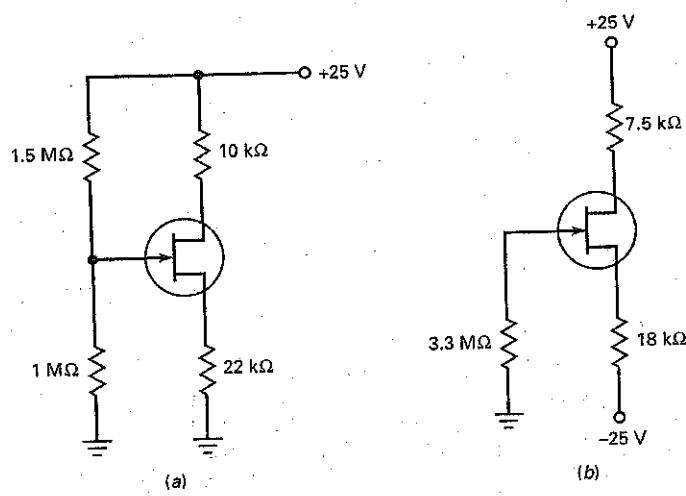
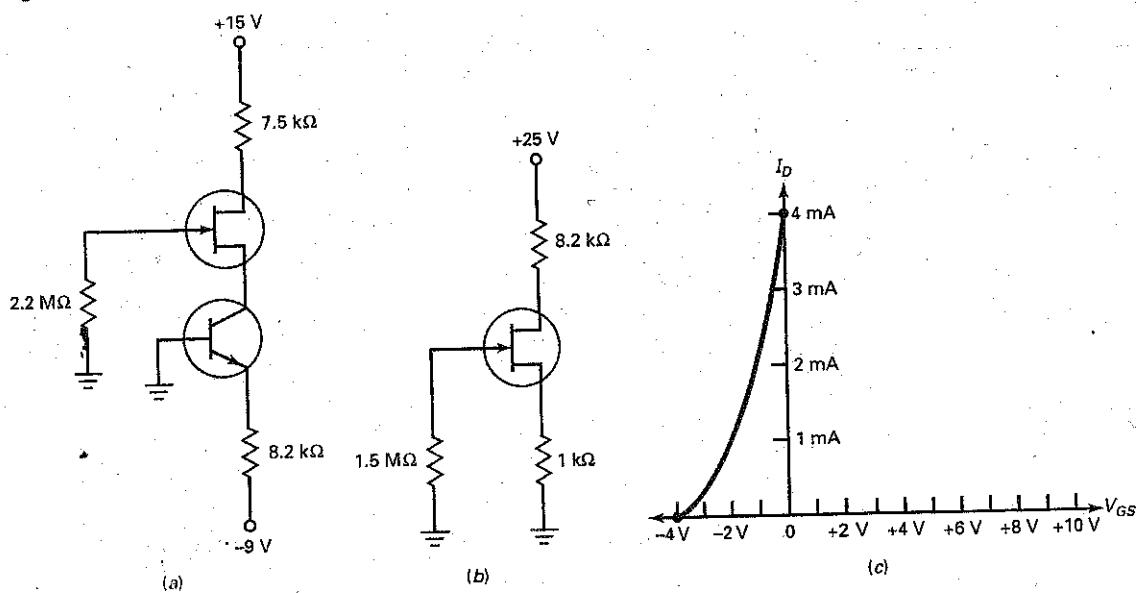


Figure 13-45



- 13-18 If the $7.5\text{ k}\Omega$ of Fig. 13-45a is changed to $4.7\text{ k}\Omega$, what is the drain current? The drain voltage?
- 13-19 In Fig. 13-45b, the drain current is 1.5 mA . What does V_{GS} equal? What does V_{DS} equal?

- 13-20 The voltage across the $1\text{ k}\Omega$ of Fig. 13-45b is 1.5 V . What is the voltage between the drain and ground?

For Problems 13-21 through 13-24, use Fig. 13-45c and graphical methods to find your answers.

- 13-21 In Fig. 13-44a, find V_{GS} and I_D using the transconductance curve of Fig. 13-45c.
- 13-22 In Fig. 13-45a, find V_{GS} and I_D using the transconductance curve of Fig. 13-45c.
- 13-23 In Fig. 13-45b, find V_{GS} and I_D using the transconductance curve of Fig. 13-45c.
- 13-24 Change R_S in Fig. 13-45b from $1\text{ k}\Omega$ to $2\text{ k}\Omega$. Use the curve of Fig. 13-45c to find V_{GS} , I_D , and V_{DS} .

SEC. 13-6 TRANSCONDUCTANCE

- 13-25 A 2N4416 has $I_{DSS} = 10\text{ mA}$ and $g_{m0} = 4000\text{ }\mu\text{S}$. What is its gate-source cutoff voltage? What is the value of g_m for $V_{GS} = -1\text{ V}$?
- 13-26 A 2N3370 has $I_{DSS} = 2.5\text{ mA}$ and $g_{m0} = 1500\text{ }\mu\text{S}$. What is the value of g_m for $V_{GS} = -1\text{ V}$?
- 13-27 The JFET of Fig. 13-46a has $g_{m0} = 6000\text{ }\mu\text{S}$. If $I_{DSS} = 12\text{ mA}$, what is the approximate value of I_D for V_{GS} of -2 V ? Find the g_m for this I_D .

SEC. 13-7 JFET AMPLIFIERS

- 13-28 If $g_m = 3000\text{ }\mu\text{S}$ in Fig. 13-46a, what is the ac output voltage?
- 13-29 The JFET amplifier of Fig. 13-46a has the transconductance curve of Fig. 13-46b. What is the approximate ac output voltage?
- 13-30 If the source follower of Fig. 13-47a has $g_m = 2000\text{ }\mu\text{S}$, what is the ac output voltage?

Figure 13-46

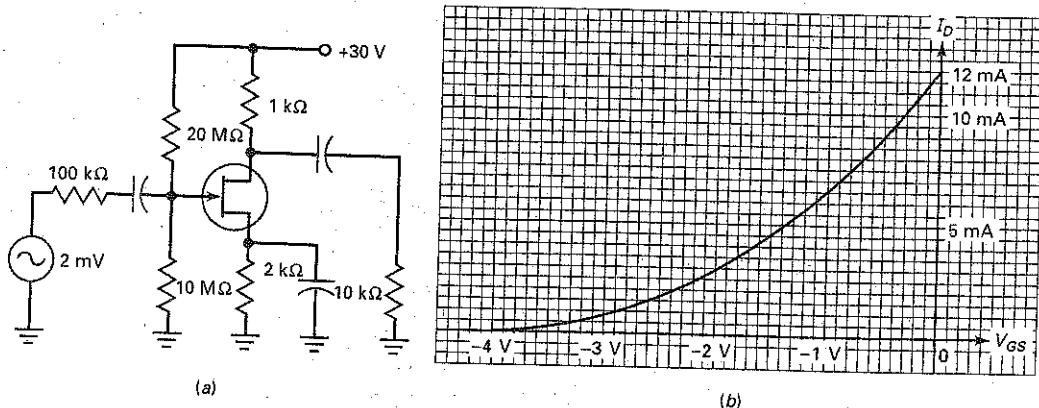


Figure 13-47

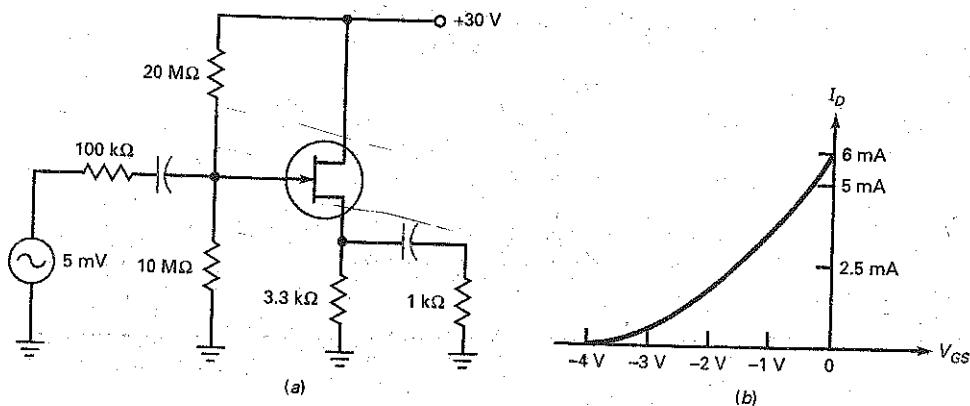
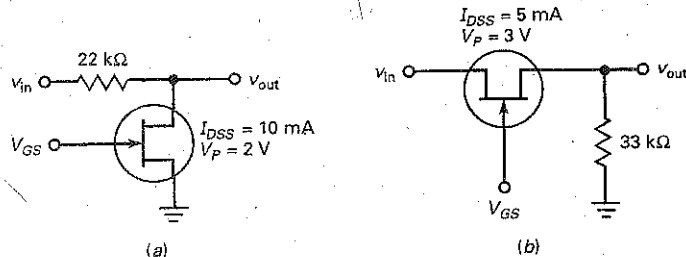


Figure 13-48



- 13-31 The source follower of Fig. 13-47a has the transconductance curve of Fig. 13-47b. What is the ac output voltage?

Critical Thinking

- 13-34 If a JFET has the drain curves of Fig. 13-49a, what does I_{DSS} equal? What is the maximum V_{DS} in the ohmic region? Over what voltage range of V_{DS} does the JFET act as a current source?
- 13-35 Write the transconductance equation for the JFET whose curve is shown in Fig. 13-49b. How much drain current is there when $V_{GS} = -4$ V? When $V_{GS} = -2$ V?
- 13-36 If a JFET has a square-law curve like Fig. 13-49c, how much drain current is there when $V_{GS} = -1$ V?
- 13-37 What is the dc drain voltage in Fig. 13-50? The ac output voltage if $g_m = 2000 \mu S$?
- 13-38 Figure 13-51 shows a JFET dc voltmeter. The zero adjust is set just before a reading is taken. The calibrate adjust is set periodically to give full-scale deflection when $V_{in} = -2.5$ V. A calibrate adjustment like this takes care of variations from one FET to another and FET aging effects.
- The current through the 510Ω equals 4 mA. How much dc voltage is there from the source to ground?

- 13-32 The input voltage of Fig. 13-48a is 50 mV pp. What is the output voltage when $V_{GS} = 0$ V? When $V_{GS} = -10$ V? The on-off ratio?
- 13-33 The input voltage of Fig. 13-48b is 25 mV pp. What is the output voltage when $V_{GS} = 0$ V? When $V_{GS} = -10$ V? The on-off ratio?
- 13-39 In Fig. 13-52a, the JFET has an I_{DSS} of 16 mA and an $R_{DS(on)}$ of 200Ω . If the load has a resistance of $10 \text{ k}\Omega$, what are the load current and the voltage across the JFET? If the load is accidentally shorted, what are the load current and the voltage across the JFET?
- 13-40 Figure 13-52b shows part of an AGC amplifier. A dc voltage is fed back from an output stage to an earlier stage such as the one shown here. Figure 13-46b is the transconductance curve. What is the voltage gain for each of these?
- $V_{AGC} = 0$
 - $V_{AGC} = -1$ V
 - $V_{AGC} = -2$ V
 - $V_{AGC} = -3$ V
 - $V_{AGC} = -3.5$ V

Figure 13-49

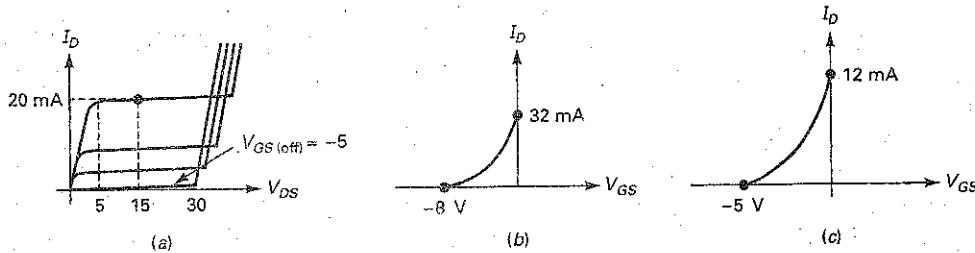


Figure 13-50

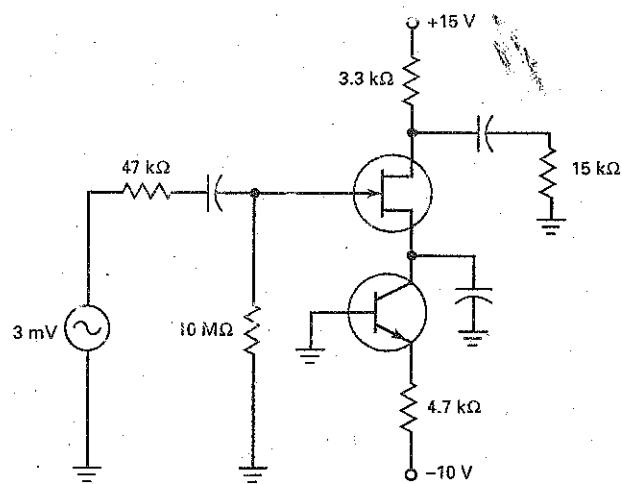


Figure 13-51

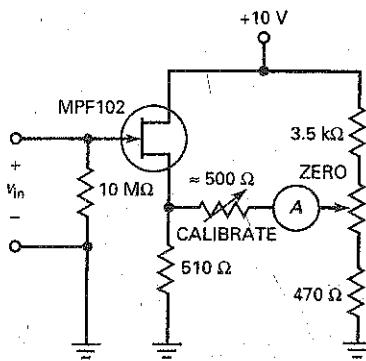
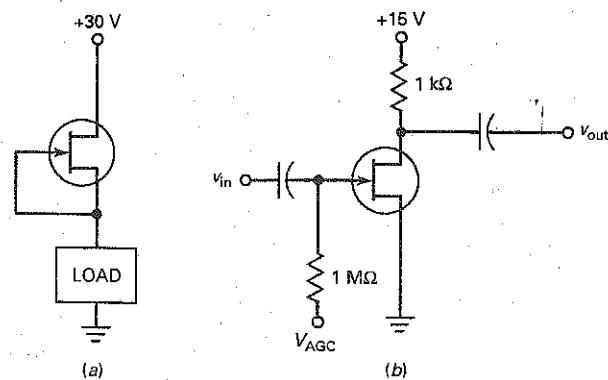


Figure 13-52



Troubleshooting

PROBLEMS Use Fig. 13-53 and the troubleshooting table to solve the remaining problems.

13-41 Find the trouble T_1 .

13-42 Find the trouble T_2 .

13-43 Find the trouble T_3 .

13-44 Find the trouble T_4 .

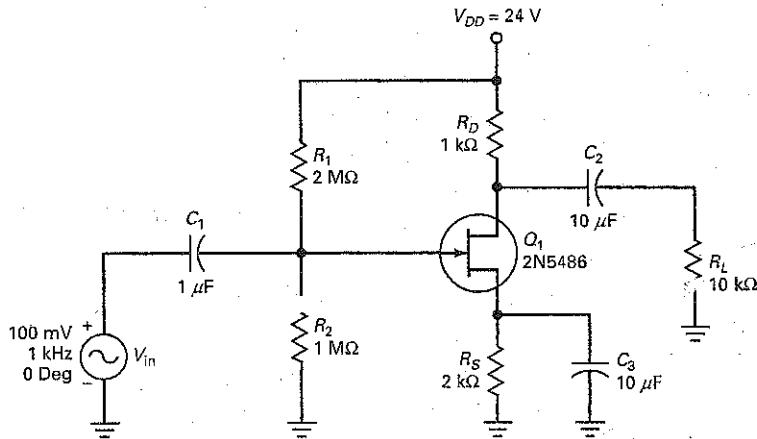
13-45 Find the trouble T_5 .

13-46 Find the trouble T_6 .

13-47 Find the trouble T_7 .

13-48 Find the trouble T_8 .

Figure 13-53 Troubleshooting.



Trouble	V_{GS}	I_D	V_{DS}	V_g	V_s	V_d	V_{out}
OK:	-1.6 V	4.8 mA	9.6 V	100 mV	0	357 mV	357 mV
T_1	-2.75 V	1.38 mA	19.9 V	100 mV	0	200 mV	200 mV
T_2	0.6 V	7.58 mA	1.25 V	100 mV	0	29 mV	29 mV
T_3	0.56 V	0	0	100 mV	0	0	0
T_4	-8 V	0	8 V	100 mV	0	0	0
T_5	8 V	0	24 V	100 mV	0	0	0
T_6	-1.6 V	4.8 mA	9.6 V	100 mV	87 mV	40 mV	40 mV
T_7	-1.6 V	4.8 mA	9.6 V	100 mV	0	397 mV	0
T_8	0	7.5 mA	1.5 V	1 mV	0	0	0

Job Interview Questions

1. Tell me how a JFET works, including the pinchoff and gate-source cutoff voltage in your explanation.
2. Draw the drain curves and the transconductance curve for a JFET.
3. Compare the JFET and the bipolar junction transistor. Your comments should include advantages and disadvantages of each.
4. How can you tell whether an FET is operating in the ohmic region or the active region?
5. Draw a JFET source follower and explain how it works.
6. Draw a JFET shunt switch and a JFET series switch. Explain how each works.
7. How can the JFET be used as a static electricity switch?
8. What input quantity controls the output current in a BJT? A JFET? If the quantities are different, explain.
9. A JFET is a device that controls current flow by placing a voltage on the gate. Explain this.
10. What is the advantage of a cascode amplifier?
11. Tell me why JFETs are sometimes found as the first amplifying device at the front end of radio receivers.

Self-Test Answers

- | | | |
|------|-------|-------|
| 1. a | 10. c | 18. c |
| 2. d | 11. c | 19. a |
| 3. c | 12. a | 20. c |
| 4. d | 13. c | 21. c |
| 5. b | 14. d | 22. b |
| 6. b | 15. a | 23. b |
| 7. d | 16. b | 24. d |
| 8. c | 17. c | 25. d |
| 9. d | | |

Practice Problem Answers

- | | | | | | | | | | | | | | | | | | | |
|-------------------------------|--|---|--|---|--|--|---|-------------------------------------|--|--|---|---------------------------------------|------------------------------------|---------------------|---------------------|---|---|------------------------------------|
| 13-1 $R_{in} = 10,000 \Omega$ | 13-2 $R_{DS} = 600 \Omega$; $V_p = 3.0 V$ | 13-3 $I_D = 3 \text{ mA}$; $V_{GS} = -3 V$ | 13-4 $R_{DS} = 300 \Omega$; $V_D = 0.291 V$ | 13-5 $R_{DS} = 300 \Omega$; $V_D = 26 V$ | 13-6 $R_S = 500 \Omega$; $V_D = 26 V$ | 13-7 $V_{GS(\min)} = -0.85$; $I_{D(\min)} = 2.2 \text{ mA}$ | 13-8 $V_{GS(\max)} = -2.5 V$; $I_{D(\max)} = 6.4 \text{ mA}$ | 13-9 $I_{D(\max)} = 5.6 \text{ mA}$ | 13-10 $I_D = 4 \text{ mA}$; $V_{DS} = 12 V$ | 13-11 $I_D = 4.3 \text{ mA}$; $V_D = 5.7 V$ | 13-12 $V_{GS(\text{off})} = -3.2 V$; $g_m = 1,875 \mu S$ | 13-13 $V_{out} = 5.3 \text{ mV}_{pp}$ | 13-14 $V_{out} = 0.714 \text{ mV}$ | 13-15 $A_v = 0.634$ | 13-16 $A_v = 0.885$ | 13-17 $R_{DS} = 400 \Omega$; on-off ratio = 26 | 13-18 $V_{out(\text{on})} = 9.6 \text{ mV}$; $V_{out(\text{off})} = 10 \mu V$ on-off ratio = 960 | 13-19 $V_{peak} = 99.0 \text{ mV}$ |
|-------------------------------|--|---|--|---|--|--|---|-------------------------------------|--|--|---|---------------------------------------|------------------------------------|---------------------|---------------------|---|---|------------------------------------|

14 MOSFETS

- The metal-oxide semiconductor FET, or MOSFET, has a source, gate, and drain. The MOSFET differs from the JFET, however, in that the gate is insulated from the channel. Because of this, the gate current is even smaller than it is in a JFET. The MOSFET is sometimes called an IGFET, which stands for insulated-gate FET.

There are two kinds of MOSFETs, the depletion-mode type and the enhancement-mode type. The enhancement-mode MOSFET is widely used in both discrete and integrated circuits. In discrete circuits, the main use is in power switching, which means turning large currents on and off. In integrated circuits, the main use is in digital switching, the basic process behind modern computers. Although their use has declined, depletion-mode MOSFETs are still found in high-frequency front-end communications circuits as RF amplifiers.

Objectives

After studying this chapter, you should be able to:

- Explain the characteristics and operation of both depletion-mode and enhancement-mode MOSFETs.
- Sketch the characteristic curves for D-MOSFETs and E-MOSFETs.
- Describe how E-MOSFETs are used as digital switches.
- Draw a schematic of a typical CMOS digital switching circuit and explain its operation.
- Compare power FETs with power bipolar junction transistors (BJTs).
- Name and describe several power FET applications.
- Analyze the dc and ac operation of both D-MOSFET and E-MOSFET amplifier circuits.

Chapter Outline

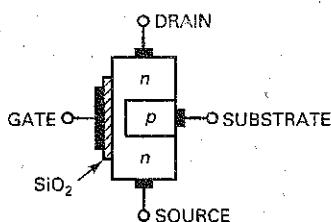
- 14-1 The Depletion-Mode MOSFET
- 14-2 D-MOSFET Curves
- 14-3 Depletion-Mode MOSFET Amplifiers
- 14-4 The Enhancement-Mode MOSFET
- 14-5 The Ohmic Region
- 14-6 Digital Switching
- 14-7 CMOS
- 14-8 Power FETs
- 14-9 E-MOSFET Amplifiers
- 14-10 MOSFET Testing

Vocabulary

active-load resistors	digital	power FET
analog	drain-feedback bias	substrate
complementary MOS (CMOS)	enhancement-mode MOSFET	threshold voltage
dc-to-ac converter	interface	uninterruptible power supply (UPS)
dc-to-dc converter	metal-oxide semiconductor FET (MOSFET)	vertical MOS (VMOS)
depletion-mode MOSFET		

14-1 The Depletion-Mode MOSFET

Figure 14-1 Depletion-mode MOSFET.



GOOD TO KNOW

Like a JFET, a depletion-mode MOSFET is considered a normally on device. This is because both devices have drain current when $V_{GS} = 0$ V. Recall that for a JFET, I_{DSS} is the maximum possible drain current. With a depletion-mode MOSFET, the drain current can exceed I_{DSS} if the gate voltage is of the correct polarity to increase the number of charge carriers in the channel. For an n-channel D-MOSFET, I_D is greater than I_{DSS} when V_{GS} is positive.

Figure 14-1 shows a depletion-mode MOSFET, a piece of *n* material with an insulated gate on the left and a *p* region on the right. The *p* region is called the **substrate**. Electrons flowing from source to drain must pass through the narrow channel between the gate and the *p* substrate.

A thin layer of silicon dioxide (SiO_2) is deposited on the left side of the channel. Silicon dioxide is the same as glass, which is an insulator. In a MOSFET, the gate is metallic. Because the metallic gate is insulated from the channel, negligible gate current flows even when the gate voltage is positive.

Figure 14-2a shows a depletion-mode MOSFET with a negative gate voltage. The V_{DD} supply forces free electrons to flow from source to drain. These electrons flow through the narrow channel on the left of the *p* substrate. As with a JFET, the gate voltage controls the width of the channel. The more negative the gate voltage, the smaller the drain current. When the gate voltage is negative enough, the drain current is cut off. Therefore, the operation of a depletion-mode MOSFET is similar to that of a JFET when V_{GS} is negative.

Since the gate is insulated, we can also use a positive input voltage, as shown in Fig. 14-2b. The positive gate voltage increases the number of free electrons flowing through the channel. The more positive the gate voltage, the greater the conduction from source to drain.

14-2 D-MOSFET Curves

Figure 14-3a shows the set of drain curves for a typical *n*-channel, depletion-mode MOSFET. Notice that the curves above $V_{GS} = 0$ are positive and the curves below $V_{GS} = 0$ are negative. As with a JFET, the bottom curve is for $V_{GS} = V_{GS(\text{off})}$ and the drain current will be approximately zero. As shown, when $V_{GS} = 0$ V, the drain current will equal I_{DSS} . This demonstrates that the depletion-mode MOSFET, or D-MOSFET, is a *normally on* device. When V_{GS} is made negative, the drain current will be reduced. In contrast to an *n*-channel JFET, the *n*-channel D-MOSFET can have V_{GS} made positive and still function properly. This is because there is no *pn* junction to become forward biased. When V_{GS} becomes positive, I_D will increase following the square-law equation

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2 \quad (14-1)$$

Figure 14-2 (a) D-MOSFET with negative gate; (b) D-MOSFET with positive gate.

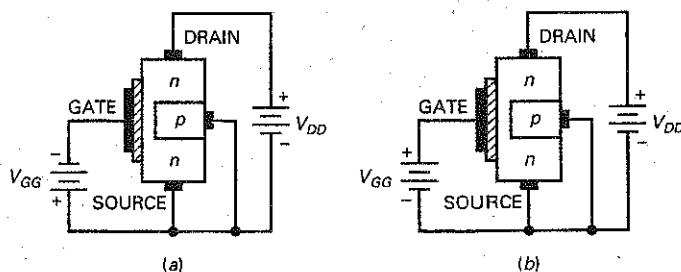
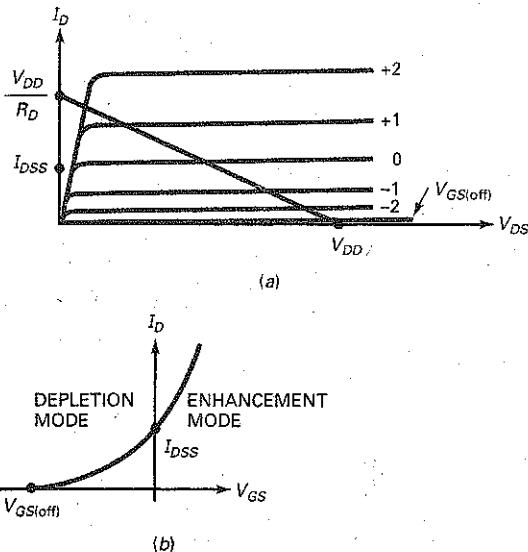


Figure 14-3 An *n*-channel, depletion-mode MOSFETs: (a) Drain curves; (b) transconductance curve.

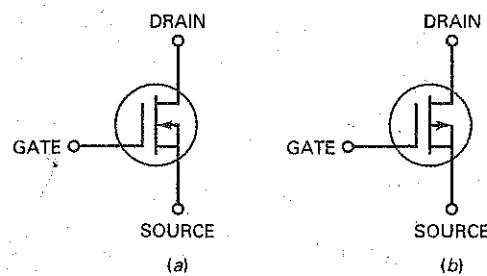


When V_{GS} is negative, the D-MOSFET is operating in the depletion mode. When V_{GS} is positive, the D-MOSFET is operating in the enhancement mode. Like the JFET, the D-MOSFET curves display an ohmic region, a current-source region, and a cutoff region.

Figure 14-3b is the transconductance curve for a D-MOSFET. Again, I_{DSS} is the drain current with the gate shorted to the source. I_{DSS} is no longer the maximum possible drain current. The parabolic transconductance curve follows the same square-law relation that exists with a JFET. As a result, the analysis of a depletion-mode MOSFET is almost identical to that of a JFET circuit. The major difference is enabling V_{GS} to be either negative or positive.

There is also a *p*-channel D-MOSFET. It consists of a drain-to-source *p*-channel, along with a *n*-type substrate. Once again, the gate is insulated from the channel. The action of a *p*-channel MOSFET is complementary to the *n*-channel MOSFET. The schematic symbols for both *n*-channel and *p*-channel D-MOSFETs are shown in Fig. 14-4.

Figure 14-4 D-MOSFET schematic symbols: (a) *n*-channel; (b) *p*-channel.



Example 14-1

A D-MOSFET has the values $V_{GS(\text{off})} = -3 \text{ V}$ and $I_{DSS} = 6 \text{ mA}$. What will the drain current equal when V_{GS} equals -1 V , -2 V , 0 V , $+1 \text{ V}$, and $+2 \text{ V}$?

SOLUTION Following the square-law equation (14-1), when

$$V_{GS} = -1 \text{ V} \quad I_D = 2.67 \text{ mA}$$

$$V_{GS} = -2 \text{ V} \quad I_D = 0.667 \text{ mA}$$

$$V_{GS} = 0 \text{ V} \quad I_D = 6 \text{ mA}$$

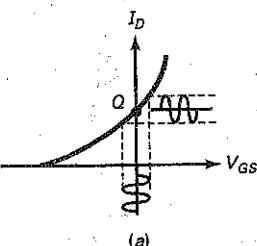
$$V_{GS} = +1 \text{ V} \quad I_D = 10.7 \text{ mA}$$

$$V_{GS} = +2 \text{ V} \quad I_D = 16.7 \text{ mA}$$

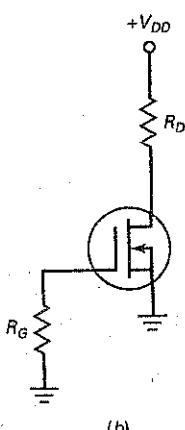
PRACTICE PROBLEM 14-1 Repeat example 14-1 using the values $V_{GS(\text{off})} = -4 \text{ V}$ and $I_{DSS} = 4 \text{ mA}$.

14-3 Depletion-Mode MOSFET Amplifiers

Figure 14-5 Zero-bias.



(a)



(b)

A depletion-mode MOSFET is unique because it can operate with a positive or a negative gate voltage. Because of this, we can set its Q point at $V_{GS} = 0 \text{ V}$, as shown in Fig. 14-5a. When the input signal goes positive, it increases I_D above I_{DSS} . When the input signal goes negative, it decreases I_D below I_{DSS} . Because there is no pn junction to forward bias, the input resistance of the MOSFET remains very high. Being able to use zero V_{GS} allows us to build the very simple bias circuit of Fig. 14-5b. Because I_G is zero, $V_{GS} = 0 \text{ V}$ and $I_D = I_{DSS}$. The drain voltage is:

$$V_{DS} = V_{DD} - I_{DSS} R_D \quad (14-2)$$

Due to the fact that a D-MOSFET is a normally on device, it is also possible to use self-bias by adding a source resistor. The operation becomes the same as a self-biased JFET circuit.

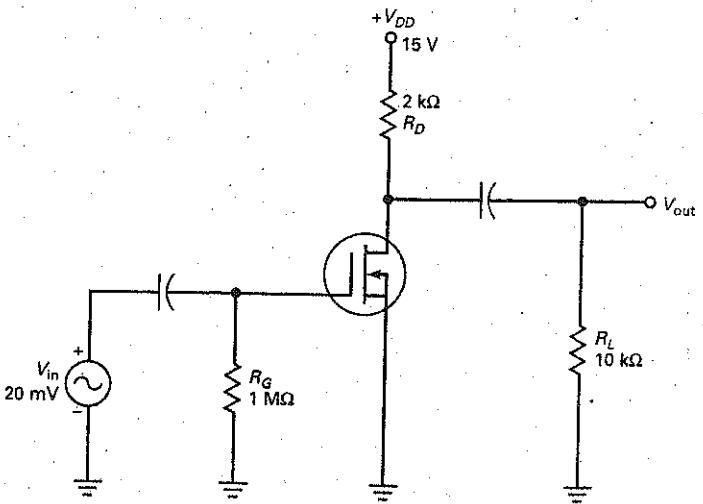
Example 14-2

The D-MOSFET amplifier shown in Fig. 14-6 has $V_{GS(\text{off})} = -2 \text{ V}$, $I_{DSS} = 4 \text{ mA}$, and $g_m = 2000 \mu\text{S}$. What is the circuit's output voltage?

SOLUTION With the source grounded, $V_{GS} = 0 \text{ V}$ and $I_D = 4 \text{ mA}$.

$$V_{DS} = 15 \text{ V} - (4 \text{ mA})(2 \text{ k}\Omega) = 7 \text{ V}$$

Figure 14-6 D-MOSFET amplifier.



Since $V_{GS} = 0$ V, $g_m = g_{mo} = 2000 \mu\text{S}$.
The amplifier's voltage gain is found by:

$$A_V = g_m r_d$$

The ac drain resistance is equal to:

$$r_d = R_D \parallel R_L = 2 \text{ K} \parallel 10 \text{ K} = 1.76 \text{ k}\Omega$$

and A_V is:

$$A_V = (2000 \mu\text{S})(1.67 \text{ k}\Omega) = 3.34$$

Therefore,

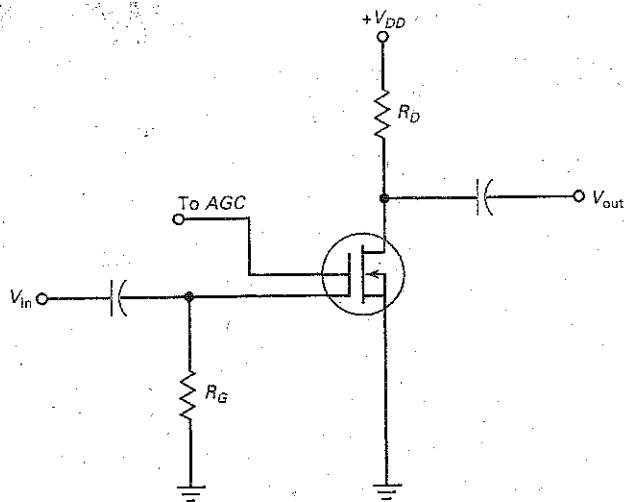
$$V_{out} = (V_{in})(A_V) = (20 \text{ mV})(3.34) = 66.8 \text{ mV}$$

PRACTICE PROBLEM 14-2 In Fig. 14-6, if the MOSFET's g_{mo} value is 3000 μS , what is the value of V_{out} ?

As shown by Example 14-2, the D-MOSFET has a relatively low voltage gain. One of the major advantages of this device is its extremely high input resistance. This allows us to use this device when circuit loading could be a problem. Also, MOSFETs have excellent low-noise properties. This is a definite advantage for any stage near the front end of a system where the signal is weak. This is very common in many types of electronic communications circuits.

Some D-MOSFETs, as shown in Fig. 14-7, are dual-gate devices. One gate can serve as the input signal point, while the other gate can be connected to an automatic gain control dc voltage. This allows the voltage gain of the MOSFET to be controlled and varied depending on the input signal strength.

Figure 14-7 Dual-gate MOSFET.



14-4 The Enhancement-Mode MOSFET

The depletion-mode MOSFET was part of the evolution toward the **enhancement-mode MOSFET**, abbreviated **E-MOSFET**. Without the E-MOSFET, the personal computers that are now so widespread would not exist.

The Basic Idea

Figure 14-8a shows an E-MOSFET. The *p* substrate now extends all the way to the silicon dioxide. As you can see, there no longer is an *n* channel between the source and the drain. How does an E-MOSFET work? Figure 14-8b shows normal biasing polarities. When the gate voltage is zero, the current between source and drain is zero. For this reason, an E-MOSFET is *normally off* when the gate voltage is zero.

The only way to get current is with a positive gate voltage. When the gate is positive, it attracts free electrons into the *p* region. The free electrons recombine with the holes next to the silicon dioxide. When the gate voltage is positive enough, all the holes touching the silicon dioxide are filled and free electrons begin to flow from the source to the drain. The effect is the same as creating a thin layer of *n*-type material next to the silicon dioxide. This thin conducting layer is

Figure 14-8 Enhancement-mode MOSFET: (a) Unbiased; (b) biased.

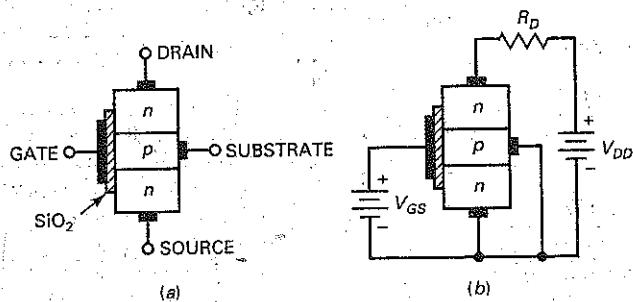
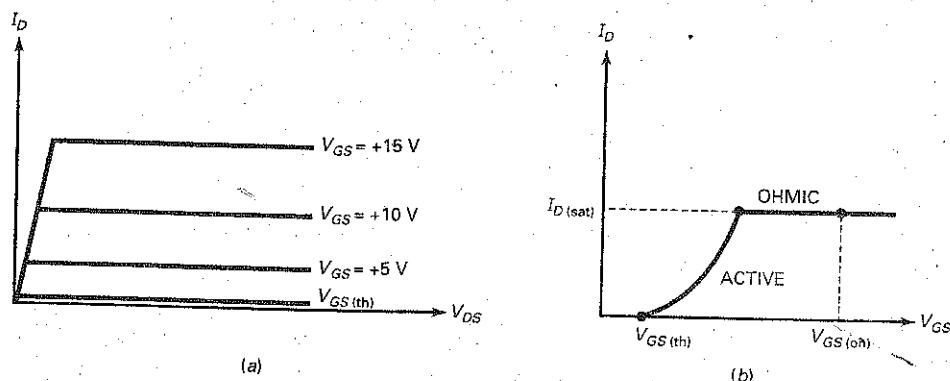


Figure 14-9 EMOS graphs: (a) Drain curves; (b) transconductance curve.



called the *n*-type inversion layer. When it exists, free electrons can flow easily from the source to the drain.

The minimum V_{GS} that creates the *n*-type inversion layer is called the **threshold voltage**, symbolized $V_{GS(\text{th})}$. When V_{GS} is less than $V_{GS(\text{th})}$, the drain current is zero. When V_{GS} is greater than $V_{GS(\text{th})}$, an *n*-type inversion layer connects the source to the drain and the drain current can flow. Typical values of $V_{GS(\text{th})}$ for small-signal devices are from 1 to 3 V.

The JFET is referred to as a *depletion-mode device* because its conductivity depends on the action of depletion layers. The E-MOSFET is classified as an *enhancement-mode device* because a gate voltage greater than the threshold voltage enhances its conductivity. With zero gate voltage, a JFET is *on*, whereas an E-MOSFET is *off*. Therefore, the E-MOSFET is considered to be a normally off device.

Drain Curves

A small-signal E-MOSFET has a power rating of 1 W or less. Figure 14-9a shows a set of drain curves for a typical small-signal E-MOSFET. The lowest curve is the $V_{GS(\text{th})}$ curve. When V_{GS} is less than $V_{GS(\text{th})}$, the drain current is approximately zero. When V_{GS} is greater than $V_{GS(\text{th})}$, the device turns on and the drain current is controlled by the gate voltage.

The almost-vertical part of the graph is the ohmic region, and the almost-horizontal parts are the active region. When biased in the ohmic region, the E-MOSFET is equivalent to a resistor. When biased in the active region, it is equivalent to a current source. Although the E-MOSFET can operate in the active region, the main use is the ohmic region.

Figure 14-9b shows a typical transconductance curve. There is no drain current until $V_{GS} = V_{GS(\text{th})}$. The drain current then increases rapidly until it reaches the saturation current $I_{D(\text{sat})}$. Beyond this point, the device is biased in the ohmic region. Therefore, I_D cannot increase, even though V_{GS} increases. To ensure hard saturation, a gate voltage of $V_{GS(\text{on})}$ well above $V_{GS(\text{th})}$ is used, as shown in Fig. 14-9b.

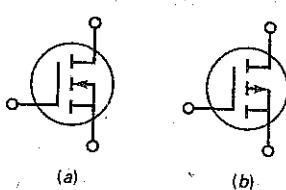
Schematic Symbol

When $V_{GS} = 0$, the E-MOSFET is off because there is no conducting channel between source and drain. The schematic symbol of Fig. 14-10a has a broken channel line to indicate this normally off condition. As you know, a gate voltage greater than the threshold voltage creates an *n*-type inversion layer that connects

GOOD TO KNOW

With the E-MOSFET, V_{GS} has to be greater than $V_{GS(\text{th})}$ to get any drain current at all. Therefore, when E-MOSFETs are biased, self-bias, current-source bias, and zero bias cannot be used because these forms of bias depend on the depletion mode of operation. This leaves gate bias, voltage-divider bias, and source bias as the means for biasing E-MOSFETs.

Figure 14-10 EMOS Schematic symbols: (a) N-channel device; (b) p-channel device.



GOOD TO KNOW

E-MOSFETs are often used in class AB amplifiers, where the E-MOSFET is biased with a value of V_{GS} slightly exceeding that of $V_{GS(th)}$. This "trickle bias" prevents crossover distortion. D-MOSFETs are not suitable for use in class B or class AB amplifiers because a large drain current flows for $V_{GS} = 0$ V.

the source to the drain. The arrow points to this inversion layer, which acts like an *n* channel when the device is conducting.

There is also a *p*-channel E-MOSFET. The schematic symbol is similar, except that the arrow points outward, as shown in Fig. 14-10b.

Maximum Gate-Source Voltage

MOSFETs have a thin layer of silicon dioxide, an insulator that prevents gate current for positive as well as negative gate voltages. This insulating layer is kept as thin as possible to give the gate more control over the drain current. Because the insulating layer is so thin, it is easily destroyed by excessive gate-source voltage.

For instance, a 2N7000 has a $V_{GS(max)}$ rating of ± 20 V. If the gate-source voltage becomes more positive than $+20$ V or more negative than -20 V, the thin insulating layer will be destroyed.

Aside from directly applying an excessive V_{GS} , you can destroy the thin insulating layer in more subtle ways. If you remove or insert a MOSFET into a circuit while the power is on, transient voltages caused by inductive kickback may exceed the $V_{GS(max)}$ rating. Even picking up a MOSFET may deposit enough static charge to exceed the $V_{GS(max)}$ rating. This is the reason why MOSFETs are often shipped with a wire ring around the leads, or wrapped in tin foil, or inserted into conductive foam.

Some MOSFETs are protected by a built-in zener diode in parallel with the gate and the source. The zener voltage is less than the $V_{GS(max)}$ rating. Therefore, the zener diode breaks down before any damage to the thin insulating layer occurs. The disadvantage of these internal zener diodes is that they reduce the MOSFET's high input resistance. The trade-off is worth it in some applications because expensive MOSFETs are easily destroyed without zener protection.

In conclusion, MOSFET devices are delicate and can be easily destroyed. You have to handle them carefully. Furthermore, you should never connect or disconnect them while the power is on. Finally, before you pick up a MOSFET device, you should ground your body by touching the chassis of the equipment you are working on.

14-5 The Ohmic Region

Although the E-MOSFET can be biased in the active region, this is seldom done because it is primarily a switching device. The typical input voltage is either low or high. Low voltage is 0 V, and high voltage is $V_{GS(on)}$, a value specified on data sheets.

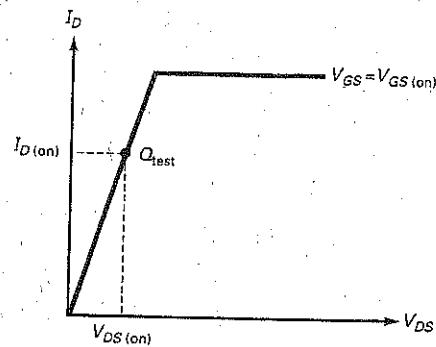
Drain-Source on Resistance

When an E-MOSFET is biased in the ohmic region, it is equivalent to a resistance of $R_{DS(on)}$. Almost all data sheets will list the value of this resistance at a specific drain current and gate-source voltage.

Figure 14-11 illustrates the idea. There is a Q_{test} point in the ohmic region of the $V_{GS} = V_{GS(on)}$ curve. The manufacturer measures $I_{D(on)}$ and $V_{DS(on)}$ at this Q_{test} point. From this, the manufacturer calculates the value of $R_{DS(on)}$ using this definition:

$$R_{DS(on)} = \frac{V_{DS(on)}}{I_{D(on)}} \quad (14-3)$$

Figure 14-11 Measuring $R_{DS(on)}$.



For instance, at the test point, a VN2406L has $V_{DS(on)} = 1$ V and $I_{D(on)} = 100$ mA. With Eq. (14-3):

$$R_{DS(on)} = \frac{1 \text{ V}}{100 \text{ mA}} = 10 \Omega$$

Fig. 14-12 shows the data sheet of a 2N7000 *n*-channel E-MOSFET. Notice that this E-MOSFET can also be packaged as a surface-mount device. Also make note of the internal diode between the drain and source leads. Minimum, typical, and maximum values are listed for this device. These device specifications often have a wide range of values.

Table of E-MOSFETs

Table 14-1 is a sample of small-signal E-MOSFETs. The typical $V_{GS(th)}$ values are 1.5 to 3 V. The $R_{DS(on)}$ values are 0.3 to 28 Ω , which means that the E-MOSFET has a low resistance when biased in the ohmic region. When biased at cutoff, it has a very high resistance, approximately an open circuit. Therefore, E-MOSFETs have excellent on-off ratios.

Table 14-1 Small-Signal EMOS Sampler

Device	$V_{GS(th)}$, V	$V_{GS(on)}$, V	$I_D(on)$	$R_{DS(on)}$, Ω	$I_D(max)$	$P_D(max)$
VN2406L	1.5	2.5	100 mA	10	200 mA	350 mW
BS107	1.75	2.6	20 mA	28	250 mA	350 mW
2N7000	2	4.5	75 mA	6	200 mA	350 mW
VN10LM	2.5	5	200 mA	7.5	300 mA	1 W
MPF930	2.5	10	1 A	0.9	2 A	1 W
IRFD120	3	10	600 mA	0.3	1.3 A	1 W

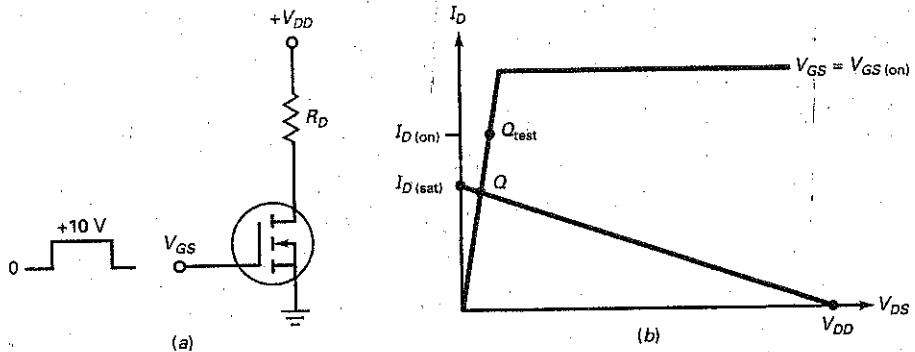
Figure 14-12 The 2N7000 data sheet.

FAIRCHILD SEMICONDUCTOR™					
2N7000 / 2N7002 / NDS7002A N-Channel Enhancement Mode Field Effect Transistor					
General Description	Features				
<p>These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while providing rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 400mA DC and can deliver pulsed currents up to 2A. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.</p>	<ul style="list-style-type: none"> ■ High density cell design for low $R_{DS(on)}$. ■ Voltage controlled small signal switch. ■ Rugged and reliable. ■ High saturation current capability. 				
<p>TO-92 2N7000</p>	<p>SOT-23 (TO-236AB)</p>				
Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted					
Symbol	Parameter	2N7000	2N7002	NDS7002A	Units
V_{DSS}	Drain-Source Voltage	60	60	60	V
V_{DSR}	Drain-Gate Voltage ($R_{GS} \leq 1 \text{ M}\Omega$)	60	60	60	V
V_{GSS}	Gate-Source Voltage - Continuous Non Repetitive ($t_p < 50\mu\text{s}$)	± 20	± 20	± 40	V
I_D	Maximum Drain Current - Continuous	200	115	280	mA
	- Pulsed	500	800	1500	
P_D	Maximum Power Dissipation Derated above 25°C	400	200	300	mW
		3.2	1.6	2.4	
T_J, T_{STO}		-55 to 150	-65 to 150	-65 to 150	°C
T_L		300			°C
THERMAL CHARACTERISTICS					
R_{JA}	Thermal Resistance, Junction-to-Ambient	312.5	625	417	°C/W

Figure 14-12 (continued)

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted							
Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
$V_{DS(BOSS)}$	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \mu\text{A}$	All	60			V
$I_{DS(BOSS)}$	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$	2N7000		1		μA
		$T_J = 125^\circ\text{C}$			1	mA	
$I_{GSS(F)}$	Gate - Body Leakage, Forward	$V_{GS} = 60 \text{ V}, V_{DS} = 0 \text{ V}$	2N7002 NDS7002A		1		μA
		$T_J = 125^\circ\text{C}$		0.5	mA		
$I_{GSS(R)}$	Gate - Body Leakage, Reverse	$V_{GS} = 15 \text{ V}, V_{DS} = 0 \text{ V}$	2N7000		10		nA
		$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	2N7002 NDS7002A	100	nA		
$I_{GSS(R)}$	Gate - Body Leakage, Reverse	$V_{GS} = -15 \text{ V}, V_{DS} = 0 \text{ V}$	2N7000		-10		nA
		$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$	2N7002 NDS7002A	-100	nA		
ON CHARACTERISTICS (Note 1)							
$V_{GS(ON)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1 \text{ mA}$	2N7000	0.8	2.1	3	V
		$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2N7002 NDS7002A	1	2.1	2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$	2N7000		1.2	5	Ω
		$T_J = 125^\circ\text{C}$			1.9	9	
		$V_{GS} = 4.5 \text{ V}, I_D = 75 \text{ mA}$			1.8	5.3	
		$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$	2N7002	1.2	7.5		
		$T_J = 100^\circ\text{C}$		1.7	13.5		
		$V_{GS} = 5.0 \text{ V}, I_D = 50 \text{ mA}$		1.7	7.6		
		$T_J = 100^\circ\text{C}$		2.4	13.5		
		$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$	NDS7002A	1.2	2		
		$T_J = 125^\circ\text{C}$		2	3.5		
		$V_{GS} = 5.0 \text{ V}, I_D = 50 \text{ mA}$		1.7	3		
$T_J = 125^\circ\text{C}$		2.8	5				
$V_{DS(ON)}$	Drain-Source On-Voltage	$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$	2N7000		0.6	2.5	V
		$V_{GS} = 4.5 \text{ V}, I_D = 75 \text{ mA}$			0.14	0.4	
		$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$	2N7002	0.6	3.75		
		$V_{GS} = 5.0 \text{ V}, I_D = 50 \text{ mA}$		0.09	1.5		
		$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$	NDS7002A	0.6	1		
		$V_{GS} = 5.0 \text{ V}, I_D = 50 \text{ mA}$		0.09	0.15		
		$T_J = 125^\circ\text{C}$					
Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted							
Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
ON CHARACTERISTICS Continued (Note 1)							
$I_{D(ON)}$	On-State Drain Current	$V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}$	2N7000	75	600		mA
		$V_{GS} = 10 \text{ V}, V_{DS} \geq 2 V_{DS(ON)}$	2N7002	500	2700		
		$V_{GS} = 10 \text{ V}, V_{DS} \geq 2 V_{DS(ON)}$	NDS7002A	500	2700		
G_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 200 \text{ mA}$	2N7000	100	320		mS
		$V_{DS} \geq 2 V_{DS(ON)}, I_D = 200 \text{ mA}$	2N7002	80	320		
		$V_{DS} \geq 2 V_{DS(ON)}, I_D = 200 \text{ mA}$	NDS7002A	80	320		

Figure 14-13 $I_D(\text{sat})$ less than $I_D(\text{on})$ with $V_{GS} = V_{GS(\text{on})}$ ensures saturation.



Biasing in Ohmic Region

In Fig. 14-13a, the drain saturation current in this circuit is:

$$I_{D(\text{sat})} = \frac{V_{DD}}{R_D} \quad (14-4)$$

and the drain cutoff voltage is $V_{DS(on)}$. Figure 14-13b shows the dc load line between a saturation current of $I_{D(\text{sat})}$ and a cutoff voltage of V_{DD} .

When $V_{GS} = 0$, the Q point is at the lower end of the dc load line. When $V_{GS} = V_{GS(\text{on})}$, the Q point is at the upper end of the load line. When the Q point is below the Q_{test} point, as shown in Fig. 14-13b, the device is biased in the ohmic region. Stated another way, an E-MOSFET is biased in the ohmic region when this condition is satisfied:

$$I_{D(\text{sat})} < I_{D(\text{on})} \quad \text{when} \quad V_{GS} = V_{GS(\text{on})} \quad (14-5)$$

Equation (14-5) is important. It tells us whether an E-MOSFET is operating in the active region or the ohmic region. Given an EMOS circuit, we can calculate the $I_{D(\text{sat})}$. If $I_{D(\text{sat})}$ is less than $I_{D(\text{on})}$ when $V_{GS} = V_{GS(\text{on})}$, we will know that the device is biased in the ohmic region and is equivalent to a small resistance.

Example 14-3

What is the output voltage in Fig. 14-14a?

SOLUTION For the 2N7000, the most important values in Table 14-1 are:

$$V_{GS(\text{on})} = 4.5 \text{ V}$$

$$I_{D(\text{on})} = 75 \text{ mA}$$

$$R_{DS(\text{on})} = 6 \Omega$$

Since the input voltage swings from 0 to 4.5 V, the 2N7000 is being switched on and off.

The drain saturation current in Fig. 14-14a is:

$$I_{D(\text{sat})} = \frac{20 \text{ V}}{1 \text{ k}\Omega} = 20 \text{ mA}$$

Figure 14-14 Switching between cutoff and saturation.

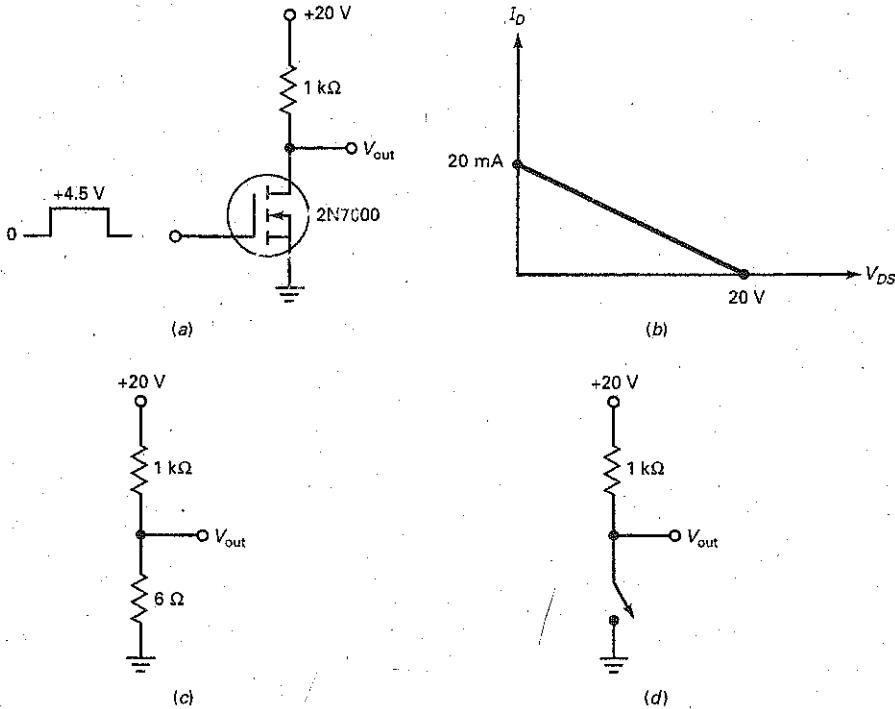


Figure 14-14b is the dc load line. Since 20 mA is less than 75 mA, the value of $I_{D(on)}$, the 2N7000 is biased in the ohmic region when the gate voltage is high.

Figure 14-14c is the equivalent circuit for a high-input gate voltage. Since the E-MOSFET has a resistance of $6\ \Omega$, the output voltage is:

$$V_{out} = \frac{6\ \Omega}{1\ k\Omega + 6\ \Omega} (20\ V) = 0.12\ V$$

On the other hand, when V_{GS} is low, the E-MOSFET is open (Fig. 14-14d), and the output voltage is pulled up to the supply voltage:

$$V_{out} = 20\ V$$

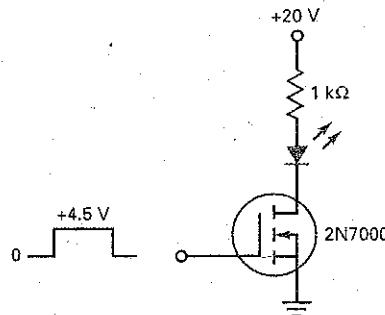
PRACTICE PROBLEM 14-3 Using Fig. 14-14a, replace the 2N7000 with a VN2406L E-MOSFET and find the output voltage value.

Example 14-4

III Multisim

What is the LED current in Fig. 14-15?

Figure 14-15 Turning an LED on and off.



SOLUTION When V_{GS} is low, the LED is off. When V_{GS} is high, the action is similar to that in the preceding example because the 2N7000 goes into hard saturation. If we ignore the LED voltage drop, the LED current is:

$$I_D \approx 20 \text{ mA}$$

If we allow 2 V for the LED drop:

$$I_D = \frac{20 \text{ V} - 2 \text{ V}}{1 \text{ k}\Omega} = 18 \text{ mA}$$

PRACTICE PROBLEM 14-4 Repeat Example 14-4 using a VN2406L E-MOSFET and a 560 Ω drain resistor.

Example 14-5

What does the circuit of Fig. 14-16a do if a coil current of 30 mA or more closes the relay contacts?

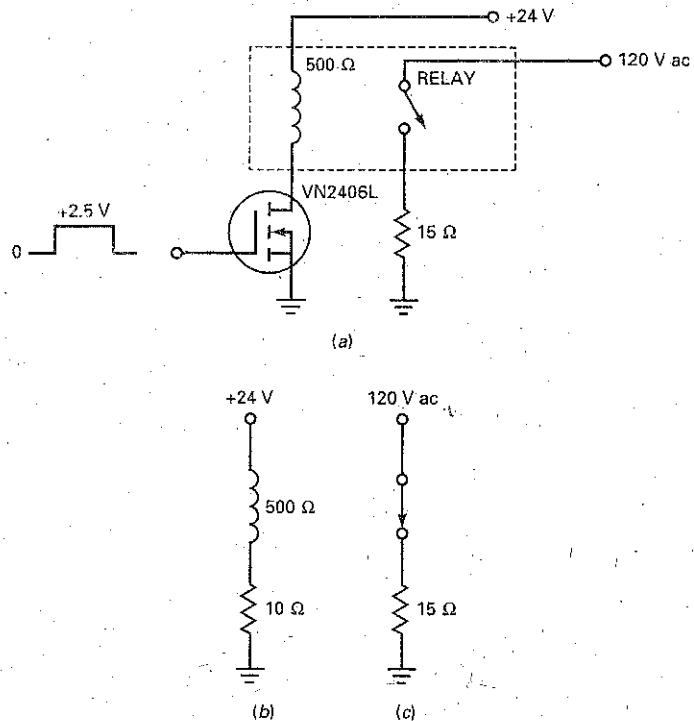
SOLUTION The E-MOSFET is being used to turn a relay on and off. Since the relay coil has a resistance of 500 Ω, the saturation current is:

$$I_{D(\text{sat})} = \frac{24 \text{ V}}{500 \text{ }\Omega} = 48 \text{ mA}$$

Because this is less than the $I_{D(\text{on})}$ of the VN2406L, the device has a resistance of only 10 Ω (see Table 14-1).

Figure 14-16b shows the equivalent circuit for high V_{GS} . The current through the relay coil is approximately 48 mA, more than enough to close the relay. When the relay is closed, the contact circuit looks like Fig. 14-16c. Therefore, the final load current is 8 A (120 V divided by 15 Ω).

Figure 14-16 Low-input current signal controls large output current.



In Figure 14-16a, an input voltage of only +2.5 V and almost zero input current control a load voltage of 120 V ac and a load current of 8 A. A circuit like this is useful with remote control. The input voltage could be a signal that has been transmitted a long distance through copper wire, fiber-optic cable, or outer space.

14-6 Digital Switching

Why has the E-MOSFET revolutionized the computer industry? Because of its threshold voltage, it is ideal for use as a switching device. When the gate voltage is well above the threshold voltage, the device switches from cutoff to saturation. This off-on action is the key to building computers. When you study computer circuits, you will see how a typical computer uses millions of E-MOSFETs as off-on switches to process data. (Data include numbers, text, graphics, and all other information that can be coded as binary numbers.)

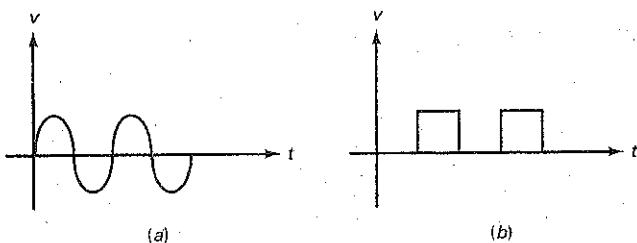
Analog, Digital, and Switching Circuits

The word **analog** means "continuous," like a sine wave. When we speak of an analog signal, we are talking about signals that continuously change in voltage like the one in Fig. 14-17a. The signal does not have to be sinusoidal. As long as

GOOD TO KNOW

Most physical quantities are analog in nature, and these are the quantities that are most often the inputs and outputs being monitored and controlled by a system. Some examples of analog inputs and outputs are temperature, pressure, velocity, position, fluid level, and flow rate. To take advantage of digital techniques when dealing with analog inputs, the physical quantities are converted to a digital format. A circuit that does this is called an *analog-to-digital (A/D) converter*.

Figure 14-17 (a) Analog signal; (b) digital signal.



there are no sudden jumps between two distinct voltage levels, the signal is referred to as an *analog signal*.

The word **digital** refers to a discontinuous signal. This means that the signal jumps between two distinct voltage levels like the waveform of Fig. 14-17b. Digital signals like these are the kind of signals inside computers. These signals are computer codes that represent numbers, letters, and other symbols.

The word *switching* is a broader word than *digital*. Switching circuits include digital circuits as a subset. In other words, switching circuits can also refer to circuits that turn on motors, lamps, heaters, and other heavy-current devices.

Passive-Load Switching

Figure 14-18 Passive load.

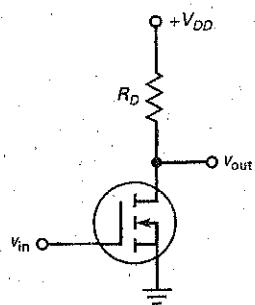


Figure 14-18 shows an E-MOSFET with a passive load. The word *passive* refers to ordinary resistors like R_D . In this circuit, v_{in} is either low or high. When v_{in} is low, the MOSFET is cut off, and v_{out} equals the supply voltage V_{DD} . When v_{in} is high, the MOSFET saturates and v_{out} drops to a low value. For the circuit to work properly, the drain saturation current $I_{D(sat)}$ has to be less than $I_{D(on)}$ when the input voltage is equal to or greater than $V_{GS(on)}$. This is equivalent to saying that the resistance in the ohmic region has to be much smaller than the passive drain resistance. In symbols:

$$R_{DS(on)} \ll R_D$$

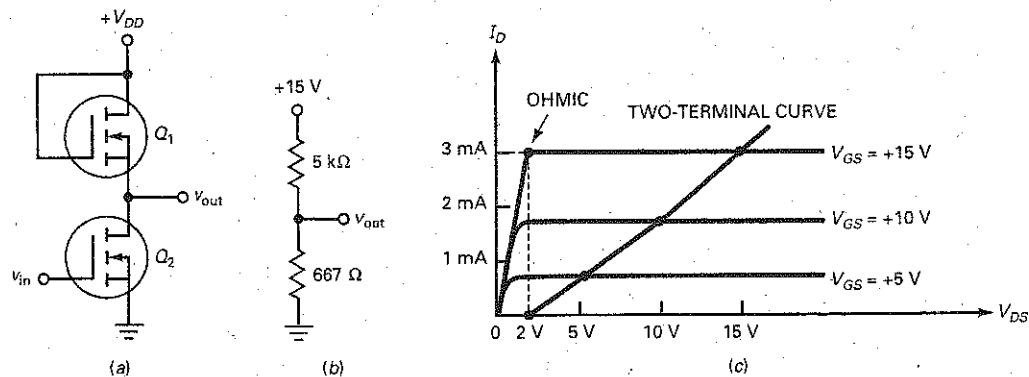
A circuit like Fig. 14-18 is the simplest computer circuit that can be built. It is called an *inverter* because the output voltage is the opposite of the input voltage. When the input voltage is low, the output voltage is high. When the input voltage is high, the output voltage is low. Great accuracy is not necessary when analyzing switching circuits. All that matters is that the input and output voltages can be easily recognized as low or high.

Active-Load Switching

Integrated circuits (ICs) consist of thousands of microscopically small transistors, either bipolar or MOS. The earliest integrated circuits used passive load resistors like the one of Fig. 14-18. But a passive load resistance presents a major problem. It is physically much larger than a MOSFET. Because of this, integrated circuits with passive-load resistors were too big until somebody invented **active-load resistors**. This greatly reduced the size of integrated circuits and led to the personal computers that we have today.

The key idea was to get rid of passive-load resistors. Figure 14-19a shows the invention: *active-load switching*. The lower MOSFET acts like a switch, but the upper MOSFET acts like large resistance. Notice that the upper

Figure 14-19 (a) Active load; (b) equivalent circuit; (c) $V_{GS} = V_{DS}$ produces a two-terminal curve.



MOSFET has its gate connected to its drain. Because of this, it becomes a *two-terminal device* with an active resistance of:

$$R_D = \frac{V_{DS(\text{active})}}{I_{D(\text{active})}} \quad (14-6)$$

where $V_{DS(\text{active})}$ and $I_{D(\text{active})}$ are voltages and currents in the active region.

For the circuit to work properly, the R_D of the upper MOSFET has to be large compared to the $R_{DS(\text{on})}$ of the lower MOSFET. For instance, if the upper MOSFET acts like an R_D of $5\text{ k}\Omega$ and the lower one like an $R_{DS(\text{on})}$ of $667\text{ }\Omega$, as shown in Fig. 14-19b, then the output voltage will be low.

Figure 14-19c shows how to calculate the R_D of the upper MOSFET. Because $V_{GS} = V_{DS}$, each operating point of this MOSFET has to fall along the two-terminal curve shown in Fig. 14-19c. If you check each plotted point on this two-terminal curve, you will see that $V_{GS} = V_{DS}$.

The two-terminal curve of Fig. 14-19c means that the upper MOSFET acts like a resistance of R_D . The value of R_D will change slightly for the different points. For instance, at the highest point shown in Fig. 14-19c, the two-terminal curve has $I_D = 3\text{ mA}$ and $V_{DS} = 15\text{ V}$. With Eq. (14-6), we can calculate:

$$R_D = \frac{15\text{ V}}{3\text{ mA}} = 5\text{ k}\Omega$$

The next point down has these approximate values: $I_D = 1.6\text{ mA}$ and $V_{DS} = 10\text{ V}$. Therefore:

$$R_D = \frac{10\text{ V}}{1.6\text{ mA}} = 6.25\text{ k}\Omega$$

By a similar calculation, the lowest point where $V_{DS} = 5\text{ V}$ and $I_D = 0.7\text{ mA}$ has $R_D = 7.2\text{ k}\Omega$.

If the lower MOSFET has the same set of drain curves as the upper one, then the lower MOSFET has an $R_{DS(\text{on})}$ of:

$$R_{DS(\text{on})} = \frac{2\text{ V}}{3\text{ mA}} = 667\text{ }\Omega$$

This is the value shown in Fig. 14-19b.

As already indicated, exact values don't matter with digital switching circuits as long as the voltages can be easily distinguished as low or high. Therefore, the exact value of R_D does not matter. It can be 5 , 6.25 , or $7.2\text{ k}\Omega$. Any of these values is large enough to produce a low output voltage in Fig. 14-19b.

Conclusion

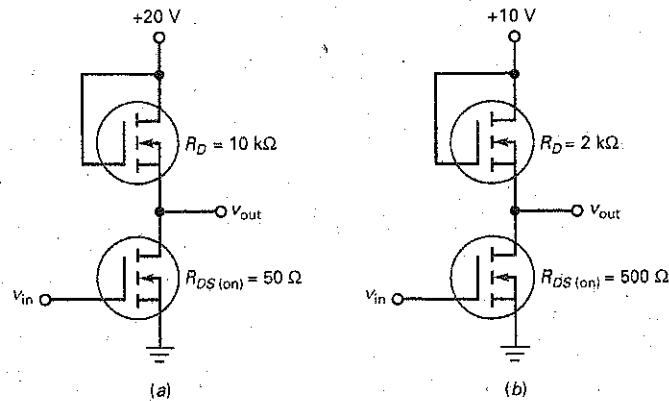
Active-load resistors are necessary with digital ICs because a small physical size is important with digital ICs. The designer makes sure that the R_D of upper MOSFET is large compared to the $R_{D(on)}$ of the lower MOSFET. When you see a circuit like Fig. 14-19a, all you have to remember is the basic idea: The circuit acts like a resistance of R_D in series with a switch. As a result, the output voltage is either high or low.

Example 14-6

III Multisim

What is the output voltage in Fig. 14-20a when the input is low? When it is high?

Figure 14-20 Examples.



SOLUTION When the input voltage is low, the lower MOSFET is open and the output voltage is pulled up to the supply voltage:

$$V_{out} = 20 \text{ V}$$

When the input voltage is high, the lower MOSFET has a resistance of 50Ω . In this case, the output voltage is pulled down toward ground:

$$V_{out} = \frac{50 \Omega}{10 \text{ k}\Omega + 50 \Omega} (20 \text{ V}) = 100 \text{ mV}$$

PRACTICE PROBLEM 14-6 Repeat Example 14-6 using a $R_{D(on)}$ value of 100Ω .

Example 14-7

What is the output voltage in Fig. 14-20b?

SOLUTION When the input voltage is low:

$$V_{out} = 10 \text{ V}$$

When the input voltage is high:

$$V_{out} = \frac{500\Omega}{2.5\text{ k}\Omega} (10\text{ V}) = 2\text{ V}$$

If you compare this to the preceding example, you can see that the on-off ratio is not as good. But with digital circuits, a high on-off ratio is not important. In this example, the output voltage is either 2 or 10 V. These voltages are easily distinguishable as low or high.

PRACTICE PROBLEM 14-7 Using Fig. 14-20b, how high can $R_{DS(on)}$ be and have a V_{out} value below 1 V when V_{in} is high?

14-7 CMOS

With active-load switching, the current drain with a low output is approximately equal to $I_{D(sat)}$. This may create a problem with battery-operated equipment. One way to reduce the current drain of a digital circuit is with **complementary MOS (CMOS)**. In this approach, the IC designer combines *n*-channel and *p*-channel MOSFETs.

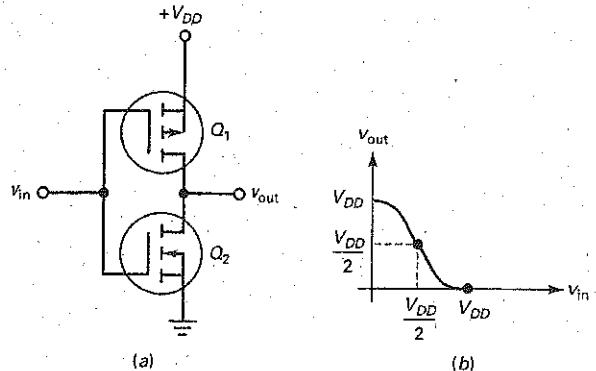
Figure 14-21a shows the idea. Q_1 is a *p*-channel MOSFET and Q_2 is an *n*-channel MOSFET. These two devices are complementary; that is, they have equal and opposite values of $V_{GS(th)}$, $V_{GS(on)}$, $I_{D(on)}$, and so on. The circuit is similar to a class B amplifier because one MOSFET conducts while the other is off.

Basic Action

When a CMOS circuit like Fig. 14-21a is used in a switching application, the input voltage is either high ($+V_{DD}$) or low (0 V). When the input voltage is high, Q_1 is off and Q_2 is on. In this case, the shorted Q_2 pulls the output voltage down to ground. On the other hand, when the input voltage is low, Q_1 is on and Q_2 is off. Now, the shorted Q_1 pulls the output voltage up to $+V_{DD}$. Since the output voltage is inverted, the circuit is called a *CMOS inverter*.

Figure 14-21b shows how the output voltage varies with the input voltage. When the input voltage is zero, the output voltage is high. When the input voltage is high, the output voltage is low. Between the two extremes, there is

Figure 14-21 CMOS inverter: (a) Circuit; (b) input-output graph.



a crossover point where the input voltage equals $V_{DD}/2$. At this point, both MOSFETs have equal resistances and the output voltage equals $V_{DD}/2$.

Power Consumption

The main advantage of CMOS is its extremely low power consumption. Because both MOSFETs are in series in Fig. 14-21a, the quiescent current drain is determined by the nonconducting device. Since its resistance is in the megohms, the *quiescent* (idling) power consumption approaches zero.

The power consumption increases when the input signal switches from low to high, and vice versa. The reason is this: At the midway point in a transition from low to high, or vice versa, both MOSFETs are on. This means that the drain current temporarily increases. Since the transition is very rapid, only a brief pulse of current occurs. The product of the drain supply voltage and the brief pulse of current means that the average *dynamic* power consumption is greater than the quiescent power consumption. In other words, a CMOS device dissipates more average power when it has transitions than when it is quiescent.

Since the pulses of current are very short, however, the average power dissipation is very low even when CMOS devices are switching states. In fact, the average power consumption is so small that CMOS circuits are often used for battery-powered applications such as calculators, digital watches, and hearing aids.

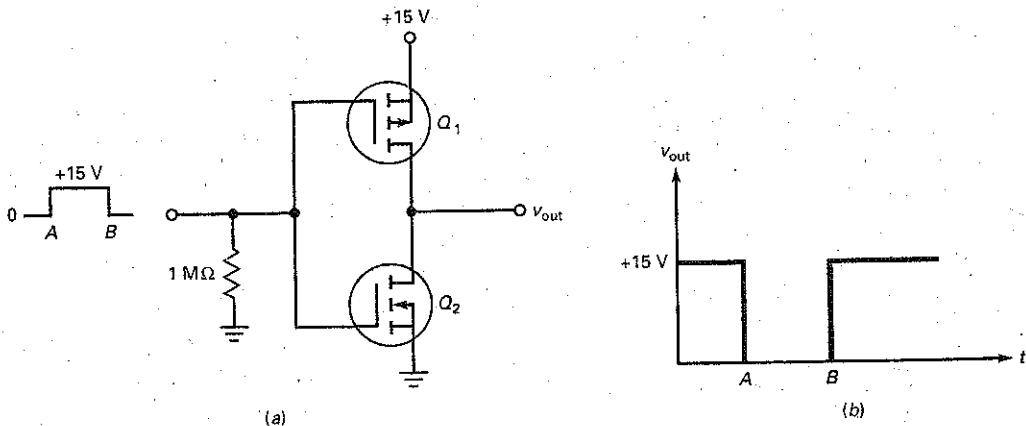
Example 14-8

The MOSFETs of Fig. 14-22a have $R_{DS(on)} = 100 \Omega$ and $R_{DS(off)} = 1 M\Omega$. What does the output waveform look like?

SOLUTION The input signal is a rectangular pulse that switches from 0 to +15 V at point A and from +15 V to 0 at point B. Before point A in time, Q_1 is on and Q_2 is off. Since Q_1 has a resistance of 100Ω compared to a resistance of $1 M\Omega$ for Q_2 , the output voltage is pulled up to +15 V.

Between points A and B, the input voltage is +15 V. This cuts off Q_1 and turns on Q_2 . In this case, the low resistance of Q_2 pulls the output voltage down to approximately zero. Figure 14-22b shows the output waveform.

Figure 14-22 Example.



PRACTICE PROBLEM 14-8 Repeat Example 14-8 with $V_{in} = +10 \text{ V}$ pulse between A and B.

14-8 Power FETs

In earlier discussions, we emphasized small-signal E-MOSFETs, that is, low-power MOSFETs. Although some discrete low-power E-MOSFETs are commercially available (see Table 14-1), the major use of low-power EMOS is with digital integrated circuits.

High-power EMOS is different. With high-power EMOS, the E-MOSFET is a discrete device widely used in applications that control motors, lamps, disk drives, printers, power supplies, and so on. In these applications, the E-MOSFET is called a **power FET**.

Discrete Devices

Manufacturers are producing different devices such as VMOS, TMOS, hexFET, trench MOSFET, and waveFET. All these power FETs use different channel geometries to increase their maximum ratings. These devices have current ratings from 1 A to more than 200 A, and power ratings from 1 W to more than 500 W.

Fig. 14-23a shows the structure of an enhancement-type MOSFET in an integrated circuit. The source is on the left, the gate in the middle, and the drain on the right. Free electrons flow horizontally from the source to the drain when V_{GS} is greater than $V_{GS(\text{th})}$. This structure limits the maximum current because free electrons must flow along the narrow inversion layer, symbolized by the dashed line. Because the channel is so narrow, conventional MOS devices have small drain currents and low power ratings.

Fig. 14-23b shows the structure of a **vertical MOS (VMOS)** device. It has two sources at the top, which are usually connected, and the substrate acts like the drain. When V_{GS} is greater than $V_{GS(\text{th})}$, free electrons flow vertically downward from the two sources to the drain. Because the conducting channel is much wider along both sides of the V groove, the current can be much larger. This enables the VMOS device to act as a power FET.

Figure 14-23 MOS structures: (a) Conventional MOSFET structure; (b) VMOS structure.

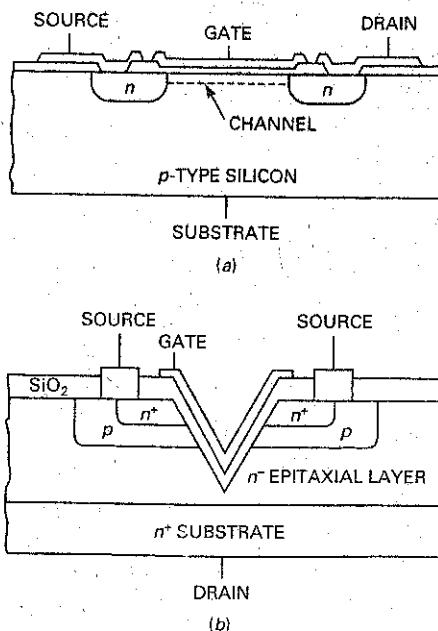


Table 14-2 | Power FET Sampler

Device	$V_{GS(on)}$, V	$I_D(on)$, A	$R_{DS(on)}$, Ω	$I_D(max)$, A	$P_{D(max)}$, W
MTP4N80E	10	2	1.95	4	125
MTV10N100E	10	5	1.07	10	250
MTW24N40E	10	12	0.13	24	250
MTW45N10E	10	22.5	0.035	45	180
MTE125N20E	10	62.5	0.012	125	460

Table 14-2 is a sample of commercially available power FETs. Notice that $V_{GS(on)}$ is 10 V for all these devices. Because they are physically larger devices, they require higher $V_{GS(on)}$ to ensure operation in the ohmic region. As you can see, the power ratings of these devices are substantial, capable of handling heavy-duty applications like automotive controls, lighting, and heating.

The analysis of a power FET circuit is the same as for small-signal devices. When driven by a $V_{GS(on)}$ of 10 V, a power FET has a small resistance of $R_{DS(on)}$ in the ohmic region. As before, an $I_{D(sat)}$ less than $I_{D(on)}$ when $V_{GS} = V_{GS(on)}$ guarantees that the device is biased in the ohmic region and acts like a small resistance.

Lack of Thermal Runaway

As discussed in Chap. 12, bipolar junction transistors may be destroyed by *thermal runaway*. The problem with bipolar transistors is the negative temperature coefficient of V_{BE} . When the internal temperature increases, V_{BE} decreases. This increases the collector current, forcing the temperature higher. But a higher temperature reduces V_{BE} even more. If not properly heat-sunked, the bipolar transistor will go into thermal runaway and be destroyed.

One major advantage of power FETs over bipolar transistors is the lack of thermal runaway. The $R_{DS(on)}$ of a MOSFET has a positive temperature coefficient. When the internal temperature increases, $R_{DS(on)}$ increases and reduces the drain current, which lowers the temperature. As a result, power FETs are inherently temperature-stable and cannot go into thermal runaway.

Power FETs in Parallel

Bipolar junction transistors cannot be connected in parallel because their V_{BE} drops do not match closely enough. If you try to connect them in parallel, *current hogging* occurs. This means that the transistor with the lower V_{BE} takes more collector current than the others.

Power FETs in parallel do not suffer from the problem of current hogging. If one of the power FETs tries to hog the current, its internal temperature will increase. This increases its $R_{DS(on)}$, which reduces its drain current. The overall effect is for all the power FETs to have equal drain currents.

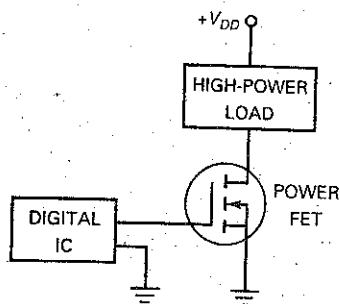
Faster Turnoff

As mentioned earlier, the minority carriers of bipolar transistors are stored in the junction area during forward bias. When you try to switch off a bipolar transistor, the stored charges flow for a while, preventing a fast turnoff. Since a power FET does not have minority carriers, it can switch a large current off faster than a bipolar transistor can. Typically, a power FET can switch off ampères of current

GOOD TO KNOW

In many cases, bipolar devices and MOS devices are used in the same electronic circuit. An interface circuit connects the output of one circuit to the input of the next; its function is to take the driver output signal and condition it so that it is compatible with the requirements of the load.

Figure 14-24 Power FET is the interface between low-power digital IC and high-power load.



in tens of nanoseconds. This is 10 to 100 times faster than with a comparable bipolar junction transistor.

Power FET as an Interface

Digital ICs are low-power devices because they can supply only small load currents. If we want to use the output of a digital IC to drive a high-current load, we can use a power FET as an **interface** (a device B that allows device A to communicate with or control device C).

Figure 14-24 shows how a digital IC can control a high-power load. The output of the digital IC drives the gate of the power FET. When the digital output is high, the power FET is like a closed switch. When the digital output is low, the power FET is like an open switch. Interfacing digital ICs (small-signal EMOS and CMOS) to high-power loads is one of the important applications of power FETs.

Figure 14-25 is an example of a digital IC controlling a high-power load. When the CMOS output is high, the power FET acts like a closed switch. The motor winding then has approximately 12 V across it, and the motor shaft turns. When the CMOS output is low, the power FET is open and the motor stops turning.

DC-to-AC Converters

When there is a sudden power failure, computers will stop operating and valuable data may be lost. One solution is to use an **uninterruptible power supply (UPS)**. A UPS contains a battery and a dc-to-ac converter. The basic idea is this: When there is a power failure, the battery voltage is converted to an ac voltage to drive the computer.

Figure 14-26 shows a **dc-to-ac converter**, the basic idea behind a UPS. When the power fails, other circuits (op amps, discussed later) are activated and

Figure 14-25. Using a power FET to control a motor.

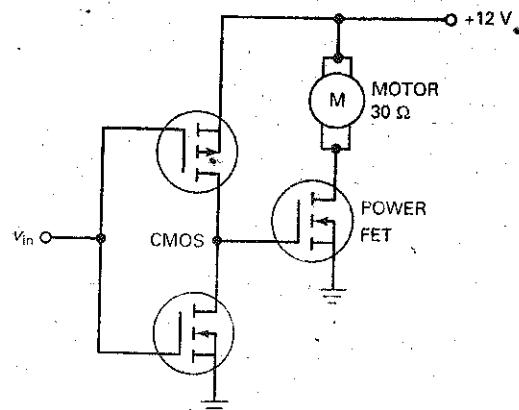


Figure 14-26 A rudimentary dc-to-ac converter.

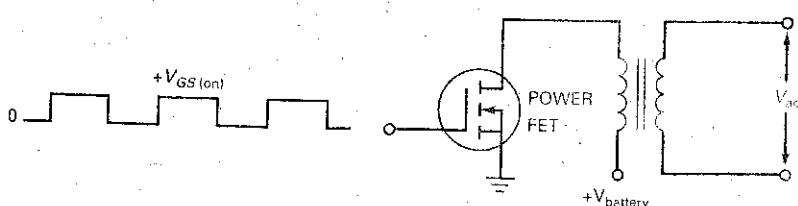
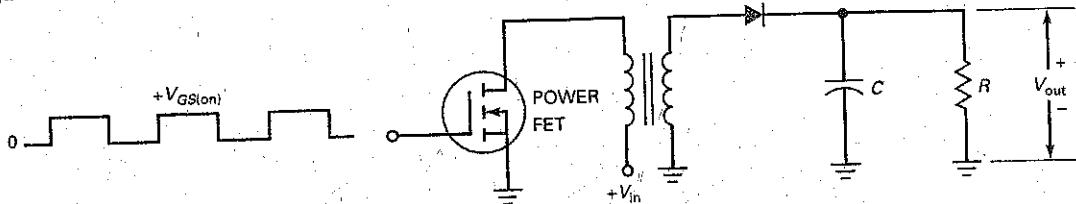


Figure 14-27 A rudimentary dc-to-dc converter.



generate a square wave to drive the gate. The square-wave input switches the power FET on and off. Since a square wave will appear across the transformer windings, the secondary winding can supply the ac voltage needed to keep the computer running. A commercial UPS is more complicated than this, but the basic idea of converting dc to ac is the same.

DC-to-DC Converters

Figure 14-27 is a **dc-to-dc converter**, a circuit that converts an input dc voltage to an output dc voltage that is either higher or lower. The power FET switches on and off, producing a square wave across the secondary winding. The half-wave rectifier and capacitor-input filter then produce the dc output voltage V_{out} . By using different turns ratios, we can get a dc output voltage that is higher or lower than the input voltage V_{in} . For lower ripple, a full-wave or bridge rectifier can be used. The dc-to-dc converter is one of the important sections of a switching or switch-mode power supply. This application will be examined in Chap. 24.

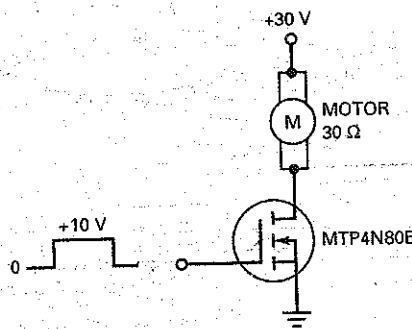
Example 14-9

What is the current through the motor winding of Fig. 14-28?

SOLUTION Table 14-2 gives $V_{GS(on)} = 10\text{ V}$, $I_{D(on)} = 2\text{ A}$, and $R_{DS(on)}$ of $1.95\ \Omega$ for an MTP4N80E. In Fig. 14-28, the saturation current is:

$$I_{D(sat)} = \frac{30\text{ V}}{30\ \Omega} = 1\text{ A}$$

Figure 14-28 Example of controlling a motor.



Since this is less than 2 A, the power FET is equivalent to a resistance of 1.95Ω . Ideally, the current through the motor winding is 1 A. If we include the 1.95Ω in the calculations, the current is:

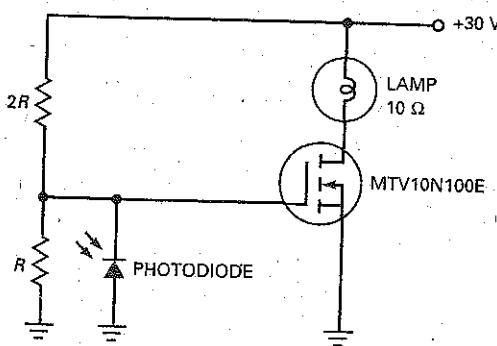
$$I_D = \frac{30 \text{ V}}{30 \Omega + 1.95 \Omega} = 0.939 \text{ A}$$

PRACTICE PROBLEM 14-9 Repeat Example 14-9 using a MTW24N40E found in Table 14-2.

Example 14-10

During the day, the photodiode of Fig. 14-29 is conducting heavily and the gate voltage is low. At night, the photodiode is off, and the gate voltage rises to $+10 \text{ V}$. Therefore, the circuit turns the lamp on automatically at night. What is the current through the lamp?

Figure 14-29 Automatic light control.



SOLUTION Table 14-2 gives $V_{GS(on)} = 10 \text{ V}$, $I_{D(on)} = 5 \text{ A}$, and $R_{DS(on)}$ of 1.07Ω for an MTV10N100E. In Fig. 14-29, the saturation current is:

$$I_{D(\text{sat})} = \frac{30 \text{ V}}{10 \Omega} = 3 \text{ A}$$

Since this is less than 5 A, the power FET is equivalent to a resistance of 1.07Ω , and the lamp current is:

$$I_D = \frac{30 \text{ V}}{10 \Omega + 1.07 \Omega} = 2.71 \text{ A}$$

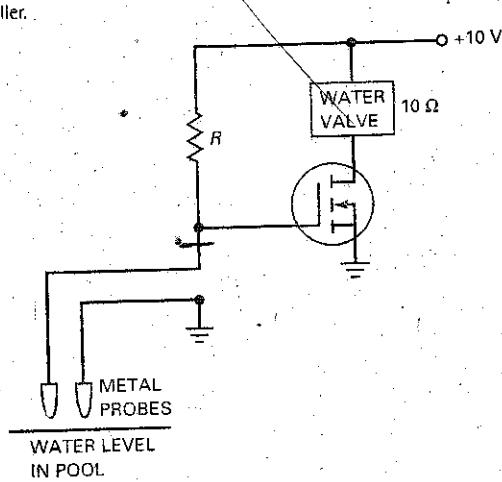
PRACTICE PROBLEM 14-10 Find the lamp current of Fig. 14-29 using a MTP4N80E found in Table 14-2.

Example 14-11

The circuit of Fig. 14-30 automatically fills a swimming pool when the water level is low. When the water level is below the two metal probes, the gate voltage is pulled up to $+10 \text{ V}$, the power FET conducts, and the water valve opens to put water in the pool.

When the water level eventually rises above the metal probes, the resistance between the probes becomes very low because water is a good conductor. In this case, the gate voltage goes low, the power FET opens, and the spring-loaded water valve closes.

Figure 14-30 Automatic pool filler.



What is the current through the water valve of Fig. 14-30 if the power FET operates in the ohmic region with an $R_{DS(on)}$ of 0.5Ω ?

SOLUTION The valve current is:

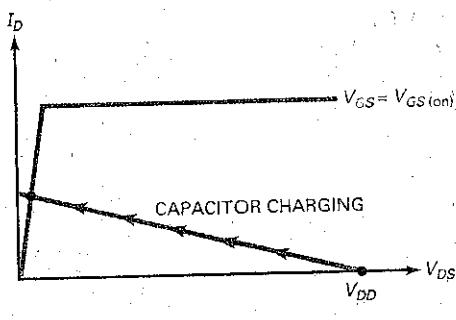
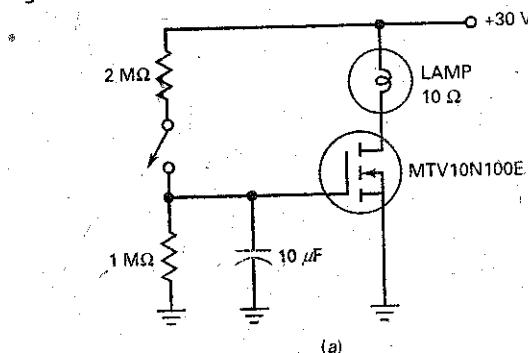
$$I_D = \frac{10 \text{ V}}{10 \Omega + 0.5 \Omega} = 0.952 \text{ A}$$

Example 14-12

What does the circuit of Fig. 14-31a do? What is the RC time constant? What is the lamp power at full brightness?

SOLUTION When the manual switch is closed, the large capacitor charges slowly toward 10 V. As the gate voltage increases above $V_{GS(on)}$, the power FET begins to conduct. Since the gate voltage is changing slowly, the operating point of the power FET has to pass slowly through the active region of Fig. 14-31b. Because of this, the lamp gets gradually

Figure 14-31 Soft turn-on of a lamp.



brighter. When the operating point of the power FET finally reaches the ohmic region, the lamp brightness is maximum. The overall effect is a *soft turn-on* of the lamp.

The Thevenin resistance facing the capacitor is:

$$R_{TH} = 2 \text{ M}\Omega \parallel 1 \text{ M}\Omega = 667 \text{ k}\Omega$$

The RC time constant is:

$$RC = (667 \text{ k}\Omega)(10 \mu\text{F}) = 6.67 \text{ s}$$

With Table 14-2, the $R_{DS(on)}$ of the MTV10N100E is 1.07 Ω . The lamp current is:

$$I_D = \frac{30 \text{ V}}{10 \Omega + 1.07 \Omega} = 2.71 \text{ A}$$

and the lamp power is:

$$P = (2.71 \text{ A})^2(10 \Omega) = 73.4 \text{ W}$$

14-9 E-MOSFET Amplifiers

As mentioned in previous sections, the E-MOSFET finds its use primarily as a switch. Applications do exist for this device to be used as an amplifier, however. These applications include front-end high-frequency RF amplifiers used in communications equipment and power E-MOSFETs used in class AB power amplifiers.

With E-MOSFETs, V_{GS} has to be greater than $V_{GS(th)}$ for drain current to flow. This eliminates self-bias, current-source bias, and zero bias because all these will have depletion-mode operation. This leaves gate bias and voltage-divider bias. Both of these biasing arrangements will work with E-MOSFETs because they can achieve enhancement mode operation.

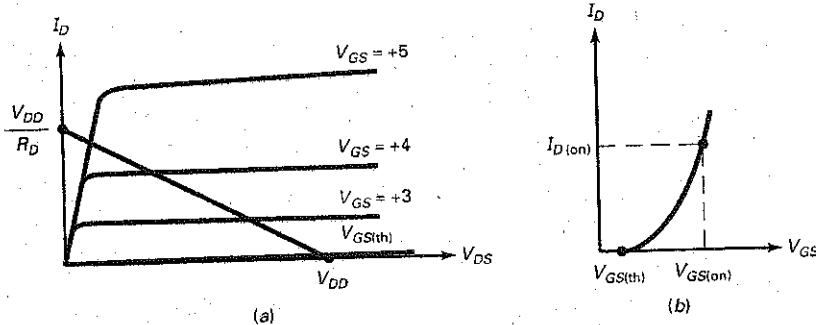
Fig. 14-32 shows the drain curves and the transconductance curve for an *n*-channel E-MOSFET. The parabolic transfer curve is similar to that of D-MOSFET with some important differences. The E-MOSFET operates only in the enhancement mode. Also, the drain current doesn't start until $V_{GS} = V_{GS(th)}$. Again, this demonstrates that the E-MOSFET is a voltage-controlled normally off device. Because the drain current is zero when $V_{GS} = 0$, the standard transconductance formula will not work with the E-MOSFET. The drain current can be found by:

$$I_D = k[V_{GS} - V_{GS(th)}]^2 \quad (14-7)$$

where k is a constant value for the E-MOSFET found by:

$$k = \frac{I_{D(on)}}{[V_{GS(on)} - V_{GS(th)}]^2} \quad (14-8)$$

Figure 14-32 An *n*-channel E-MOSFET: (a) Drain curves; (b) transconductance curve.



The data sheet for a 2N7000 *n*-channel enhancement-mode FET is shown in Fig. 14-12. Again, the important values needed are $I_{D(on)}$, $V_{GS(on)}$, and $V_{GS(th)}$. The specifications for the 2N7000 show a large variance in values. Typical values will be used in the following calculations. $I_{D(on)}$ is shown to be 600 mA when $V_{GS} = 4.5$ V. Therefore, use 4.5 V for the $V_{GS(on)}$ values. Also shown, $V_{GS(th)}$ has a typical value of 2.1 V when $V_{DS} = V_{GS}$ and $I_D = 1$ mA.

Example 14-13

Using the 2N7000 data sheet and typical values, find the constant k value and I_D at V_{GS} values of 3 V and 4.5 V.

SOLUTION Using these specified values and Eq. (14-8) k is found by:

$$k = \frac{600 \text{ mA}}{[4.5 \text{ V} - 2.1 \text{ V}]^2}$$

$$k = 104 \times 10^{-3} \text{ A/V}^2$$

With the constant value of k known, you then can solve for I_D at various V_{GS} values. For example, if $V_{GS} = 3$ V I_D is:

$$I_D = (104 \times 10^{-3} \text{ A/V}^2)[3 \text{ V} - 2.1 \text{ V}]^2$$

$$I_D = 84.4 \text{ mA}$$

and when $V_{GS} = 4.5$ V I_D is:

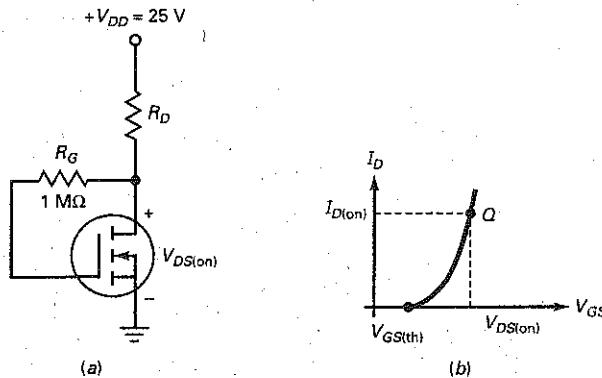
$$I_D = (104 \times 10^{-3} \text{ A/V}^2)[4.5 \text{ V} - 2.1 \text{ V}]^2$$

$$I_D = 600 \text{ mA}$$

PRACTICE PROBLEM 14-13 Using the 2N7000 data sheet and the listed minimum values of $I_{D(on)}$ and $V_{GS(th)}$, find the constant k value and I_D when $V_{GS} = 3$ V.

Fig. 14-33a shows another biasing method for E-MOSFETs called **drain-feedback bias**. This biasing method is similar to collector-feedback bias used with bipolar junction transistors. When the MOSFET is conducting, it has a

Figure 14-33 Drain-feedback bias: (a) Biasing method; (b) Q point.



drain current of $I_{D(on)}$ and a drain voltage of $V_{DS(on)}$. Because there is virtually no gate current, $V_{GS} = V_{DS(on)}$. As with collector-feedback, drain-feedback bias tends to compensate for changes in FET characteristics. For example, if $I_{D(on)}$ tries to increase for some reason, $V_{DS(on)}$ decreases. This reduces V_{GS} and partially offsets the original increase in $I_{D(on)}$.

Figure 14-33b shows the Q point on the transconductance curve. The Q point has the coordinates of $I_{D(on)}$ and $V_{DS(on)}$. Data sheets for E-MOSFETs often give a value of $I_{D(on)}$ for $V_{GS} = V_{DS(on)}$. When designing this circuit, select a value of R_D that produces the specified value of V_{DS} . This can be found by:

$$R_D = \frac{V_{DD} - V_{DS(on)}}{I_{D(on)}} \quad (14-9)$$

Example 14-14

The data sheet for the E-MOSFET shown in Fig. 14-33a specifies $I_{D(on)} = 3 \text{ mA}$ and $V_{DS(on)} = 10 \text{ V}$. If $V_{DD} = 25 \text{ V}$, select a value of R_D that allows the MOSFET to operate at the specified Q point.

SOLUTION Find the value of R_D using Eq. (14-9):

$$R_D = \frac{25 \text{ V} - 10 \text{ V}}{3 \text{ mA}}$$

$$R_D = 5 \text{ k}\Omega$$

PRACTICE PROBLEM 14-14 Using Fig. 14-33a, change V_{DD} to +22 V and solve for R_D .

The forward transconductance value, g_{FS} , is listed on most MOSFET data sheets. For the 2N7000, a minimum and typical value is given when $I_D = 200 \text{ mA}$. The minimum value is 100 mS and the typical value is 320 mS. The transconductance value will vary, depending on the circuit's Q point, following

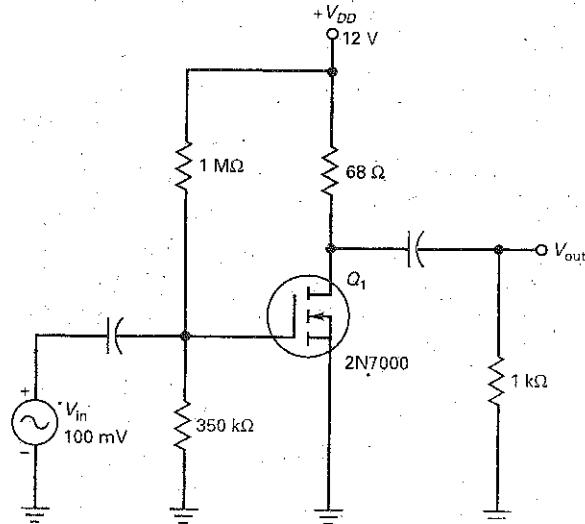
the relationship of $I_D = k [V_{GS} - V_{GS(\text{th})}]^2$ and $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$. From these equations, it can be determined that:

$$g_m = 2k [V_{GS} - V_{GS(\text{th})}] \quad (14-10)$$

Example 14-15

For the circuit of Fig. 14-34, find V_{GS} , I_D , g_m , and V_{out} . The MOSFET specifications are $k = 104 \times 10^{-3} \text{ A/V}^2$, $I_{D(\text{on})} = 600 \text{ mA}$, and $V_{GS(\text{th})} = 2.1 \text{ V}$.

Figure 14-34 E-MOSFET amplifier.



SOLUTION First, find the value of V_{GS} by:

$$V_{GS} = V_G$$

$$V_{GS} = \frac{350 \text{ k}\Omega}{350 \text{ k}\Omega + 1 \text{ M}\Omega} (12 \text{ V}) = 3.11 \text{ V}$$

Next, solve for I_D :

$$I_D = (104 \times 10^{-3} \text{ A/V}^2) [3.11 \text{ V} - 2.1 \text{ V}]^2 = 106 \text{ mA}$$

The transconductance value, g_m is found by:

$$g_m = 2k [3.11 \text{ V} - 2.1 \text{ V}] = 210 \text{ mS}$$

The voltage gain of this common-source amplifier is same as other FET devices:

$$A_V = g_m r_d$$

where $r_d = R_D \parallel R_L = 68 \Omega \parallel 1 \text{ k}\Omega = 63.7 \Omega$.
Therefore,

$$A_V = (210 \text{ mS})(63.7 \Omega) = 13.4$$

and

$$V_{out} = (A_V)(V_{in}) = (13.4)(100 \text{ mV}) = 1.34 \text{ mV}$$

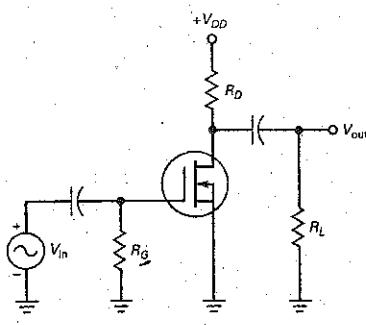
PRACTICE PROBLEM 14-15 Repeat Example 14-15 with $R_2 = 330 \text{ k}\Omega$.

Summary Table 14-1

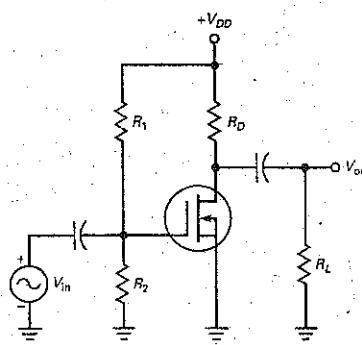
MOSFET Amplifiers

Circuit

D-MOSFET



E-MOSFET



Characteristics

- Normally on device.

- Biasing methods used:

Zero-bias, gate-bias,

self-bias, and voltage-divider bias

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2$$

$$V_{DS} = V_D - V_S$$

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)$$

$$A_V = g_m r_d \quad Z_{in} \approx R_g \quad Z_{out} \approx R_D$$

- Normally off device

- Biasing methods used:

Gate-bias, voltage-divider bias,

Drain-feedback bias

$$I_D = k [V_{GS} - V_{GS(\text{th})}]^2$$

$$k = \frac{I_{D(\text{on})}}{[V_{GS(\text{on})} - V_{GS(\text{th})}]^2}$$

$$g_m = 2 k [V_{GS} - V_{GS(\text{th})}]$$

$$A_V = g_m r_d \quad Z_{in} \approx R_1 \| R_2$$

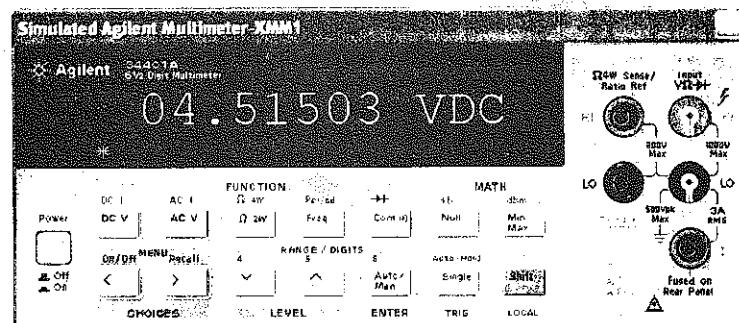
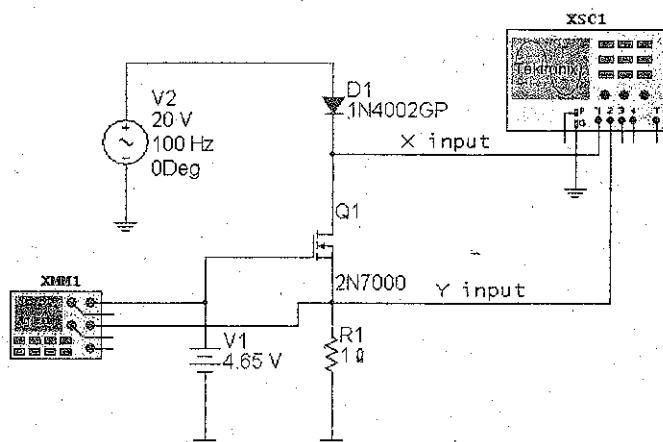
$$Z_{out} \approx R_D$$

Summary Table 14-1 shows a D-MOSFET and E-MOSFET amplifier along with their basic characteristics and equations.

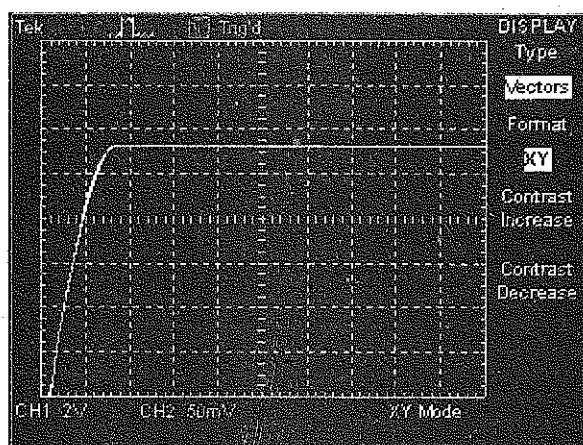
14-10 MOSFET Testing

MOSFET devices require special care when being tested for proper operation. As stated previously, the thin layer of silicon dioxide between the gate and channel can be easily destroyed when V_{GS} exceeds $V_{GS(\text{max})}$. Because of the insulated gate, along with the channel construction, testing MOSFET devices with an ohmmeter or DMM is not very effective. A good way to test these devices is with a semiconductor curve tracer. If a curve tracer is not available, special test circuits can be constructed. Fig. 14-35a shows a circuit capable of testing both depletion-mode and enhancement-mode MOSFETs. By changing the voltage level and polarity of V_1 , the device can be tested in either depletion or enhancement modes of operation. The drain curve shown in Fig. 14-35b shows the approximate drain current of 275 mA when $V_{GS} = 4.52$ V. The y-axis is set to display 50 mA/div.

Figure 14-35 MOSFET test circuit.



(a)



(b)

An alternative to the above testing methods is to simply use component substitution. By measuring in-circuit voltage values, it is often possible to deduct that the MOSFET is defective. Replacing the device with a known good component should lead you to a final conclusion.

Summary

SEC. 14-1 THE DEPLETION-MODE MOSFET

The depletion-mode MOSFET, abbreviated D-MOSFET, has a source, gate, and drain. The gate is insulated from the channel. Because of this, the input resistance is very high. The D-MOSFET has limited use, mainly in RF circuits.

SEC. 14-2 D-MOSFET CURVES

The drain curves for a D-MOSFET are similar to those of a JFET when the MOS device is operating in the depletion mode. Unlike JFETs, D-MOSFETs can also operate in the enhancement mode. When operating in the enhancement mode, the drain current is greater than I_{DSS} .

SEC. 14-3 DEPLETION-MODE MOSFET AMPLIFIERS

D-MOSFETs are mainly used as RF amplifiers. D-MOSFETs have good high-frequency response, generate low levels of electrical noise, and maintain high input impedance values when V_{GS} is negative or positive. Dual-gate D-MOSFETs can be used with automatic gain control (AGC) circuits.

SEC. 14-4 THE ENHANCEMENT-MODE MOSFET

The E-MOSFET is normally off. When the gate voltage equals the threshold voltage, an n-type inversion layer connects the

source to the drain. When the gate voltage is much greater than the threshold voltage, the device conducts heavily. Because of the thin insulating layer, MOSFETs are easily destroyed unless you take precautions in handling them.

SEC. 14-5 THE OHMIC REGION

Since the E-MOSFET is primarily a switching device, it usually operates between cutoff and saturation. When it is biased in the ohmic region, it acts like a small resistance. If $I_{D(sat)}$ is less than $I_{D(on)}$ when $V_{GS} = V_{GS(on)}$, the E-MOSFET is operating in the ohmic region.

SEC. 14-6 DIGITAL SWITCHING

Analog means that the signal changes continuously, that is, with no sudden jumps. *Digital* means that the signal jumps between two distinct voltage levels. Switching includes high-power circuits as well as small-signal digital circuits. Active-load switching means that one of the MOSFETs acts like a large resistor and the other like a switch.

SEC. 14-7 CMOS

CMOS uses two complementary MOSFETs, in which one conducts and the other shuts off. The CMOS inverter is a basic digital circuit. CMOS devices have the advantage of very low power consumption.

SEC. 14-8 POWER FETS

Discrete E-MOSFETs can be manufactured to switch very large currents. Known as power FETs, these devices are useful in automotive controls, disk drives, converters, printers, heating, lighting, motors, and other heavy-duty applications.

SEC. 14-9 E-MOSFET AMPLIFIERS

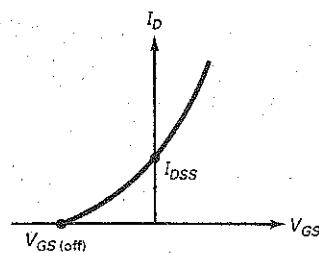
Besides their main use as power switches, E-MOSFETs find applications as amplifiers. The normally off characteristics of E-MOSFETs dictate that V_{GS} be greater than $V_{GS(th)}$ when used as an amplifier. Drain-feedback bias is similar to collector-feedback bias.

SEC. 14-10 MOSFET TESTING

It is difficult to safely test MOSFET devices using an ohmmeter. If a semiconductor curve tracer is not available, MOSFETs can be tested in test circuits or by simple substitution.

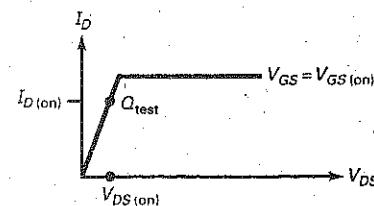
Definitions

(14-1) D-MOSFET drain current:



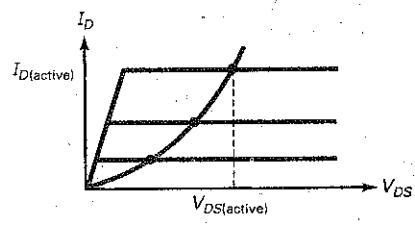
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$$

(14-3) On resistance:



$$R_{DS(on)} = \frac{V_{DS(on)}}{I_{D(on)}}$$

(14-6) Two-terminal resistance:



$$R_D = \frac{V_{DS(\text{active})}}{I_D(\text{active})}$$

(14-8) E-MOSFET constant k :

$$k = \frac{I_D(\text{on})}{[V_{GS(\text{on})} - V_{GS(\text{th})}]^2}$$

(14-10) E-MOSFET g_m :

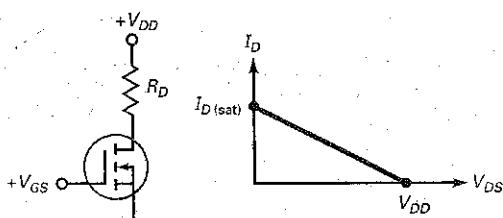
$$g_m = 2k[V_{GS} - V_{GS(\text{th})}]$$

Derivations

(14-2) D-MOSFET zero-bias:

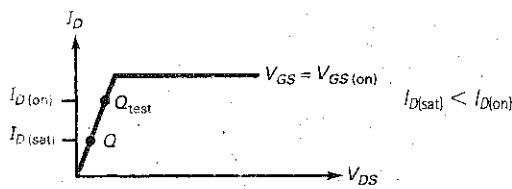
$$V_{DS} = V_{DD} - I_{DSS} R_D$$

(14-4) Saturation current:



$$I_{D(\text{sat})} = \frac{V_{DD}}{R_D}$$

(14-5) Ohmic region:



(14-7) E-MOSFET drain current:

$$I_D = k[V_{GS} - V_{GS(\text{th})}]^2$$

(14-9) R_D for drain-feedback bias:

$$R_D = \frac{V_{DD} - V_{DS(\text{on})}}{I_D(\text{on})}$$

Student Assignments

- A D-MOSFET can operate in the
 - Depletion-mode only
 - Enhancement-mode only
 - Depletion-mode or enhancement-mode
 - Low-impedance mode
- When an *n*-channel D-MOSFET has $I_D > I_{DSS}$, it
 - Will be destroyed
 - Is operating in the depletion mode
 - Is forward biased
 - Is operating in the enhancement mode
- The voltage gain of a D-MOSFET amplifier is dependent on
 - R_D
 - R_L
 - g_m
 - All of the above
- Which of the following devices revolutionized the computer industry?
 - JFET
 - D-MOSFET
 - E-MOSFET
 - Power FET
- The voltage that turns on an EMOS device is the
 - Gate-source cutoff voltage
 - Pinchoff voltage
 - Threshold voltage
 - Knee voltage
- Which of these may appear on the data sheet of an enhancement-mode MOSFET?
 - $V_{GS(\text{th})}$
 - $I_D(\text{on})$
 - $V_{GS(\text{on})}$
 - All the above
- The $V_{GS(\text{on})}$ of an *n*-channel E-MOSFET is
 - Less than the threshold voltage
 - Equal to the gate-source cutoff voltage
 - Greater than $V_{DS(\text{on})}$
 - Greater than $V_{GS(\text{th})}$
- An ordinary resistor is an example of
 - A three-terminal device
 - An active load
 - A passive load
 - A switching device
- An E-MOSFET with its gate connected to its drain is an example of
 - A three-terminal device
 - An active load
 - A passive load
 - A switching device

10. An E-MOSFET that operates at cutoff or in the ohmic region is an example of
- A current source
 - An active load
 - A passive load
 - A switching device
11. VMOS devices generally
- Switch off faster than BJTs
 - Carry low values of current
 - Have a negative temperature coefficient
 - Are used as CMOS inverters
12. A D-MOSFET is considered to be a
- Normally off device
 - Normally on device
 - Current controlled device
 - High-power switch
13. CMOS stands for
- Common MOS
 - Active-load switching
 - p*-channel and *n*-channel devices
 - Complementary MOS
14. $V_{GS(on)}$ is always
- Less than $V_{GS(th)}$
 - Equal to $V_{GS(on)}$
 - Greater than $V_{GS(th)}$
 - Negative
15. With active-load switching, the upper E-MOSFET is a
- Two-terminal device
 - Three-terminal device
 - Switch
 - Small resistance
16. CMOS devices use
- Bipolar transistors
 - Complementary E-MOSFETs
 - Class A operation
 - DMOS devices
17. The main advantage of CMOS is its
- High power rating
 - Small-signal operation
 - Switching capability
 - Low power consumption
18. Power FETs are
- Integrated circuits
 - Small-signal devices
 - Used mostly with analog signals
 - Used to switch large currents
19. When the internal temperature increases in a power FET, the
- Threshold voltage increases
 - Gate current decreases
 - Drain current decreases
 - Saturation current increases
20. Most small-signal E-MOSFETs are found in
- Heavy-current applications
 - Discrete circuits
 - Disk drives
 - Integrated circuits
21. Most power FETs are
- Used in high-current applications
 - Digital computers
 - RF stages
 - Integrated circuits
22. An *n*-channel E-MOSFET conducts when it has
- $V_{GS} > V_P$
 - An *n*-type inversion layer
 - $V_{DS} > 0$
 - Depletion layers
23. With CMOS, the upper MOSFET is
- A passive load
 - An active load
 - Nonconducting
 - Complementary
24. The high output of a CMOS inverter is
- $V_{DD}/2$
 - V_{GS}
 - V_{DS}
 - V_{DD}
25. The $R_{DS(on)}$ of a power FET
- Is always large
 - Has a negative temperature coefficient
 - Has a positive temperature coefficient
 - Is an active load

Problems

SEC. 14-2 D-MOSFET CURVES

14-1 An *n*-channel D-MOSFET has the specifications $V_{GS(off)} = -2\text{ V}$ and $I_{DSS} = 4\text{ mA}$. Given V_{GS} values of -0.5 V , -1.0 V , -1.5 V , $+0.5\text{ V}$, $+1.0\text{ V}$, and $+1.5\text{ V}$, determine I_D in the depletion mode only.

14-2 Given the same values as in the previous problem, calculate I_D for the enhancement mode only.

14-3 A *p*-channel D-MOSFET has $V_{GS(off)} = +3\text{ V}$ and $I_{DSS} = 12\text{ mA}$. Given V_{GS} values of -1.0 V , -2.0 V , 0 V , $+1.5\text{ V}$, and $+2.5\text{ V}$, determine I_D in the depletion mode only.

SEC. 14-3 DEPLETION-MODE MOSFET AMPLIFIERS

14-4 The D-MOSFET in Fig. 14-36 has $V_{GS(off)} = -3\text{ V}$ and $I_{DSS} = 12\text{ mA}$. Determine the circuit's drain current and V_{DS} values.

14-5 In Fig. 14-36, what are the values of r_d , A_V , and V_{out} using a g_m of $4000\ \mu\text{S}$?

14-6 Using Fig. 14-36 find r_d , A_V , and V_{out} if $R_D = 680\ \Omega$ and $R_L = 10\text{ k}\Omega$.

14-7 What is the approximate input impedance of Fig. 14-36?

SEC. 14-5 THE OHMIC REGION

14-8 Calculate $R_{DS(on)}$ for each of these E-MOSFET values:

- $V_{DS(on)} = 0.1\text{ V}$ and $I_{D(on)} = 10\text{ mA}$
- $V_{DS(on)} = 0.25\text{ V}$ and $I_{D(on)} = 45\text{ mA}$
- $V_{DS(on)} = 0.75\text{ V}$ and $I_{D(on)} = 100\text{ mA}$
- $V_{DS(on)} = 0.15\text{ V}$ and $I_{D(on)} = 200\text{ mA}$

Figure 14-36

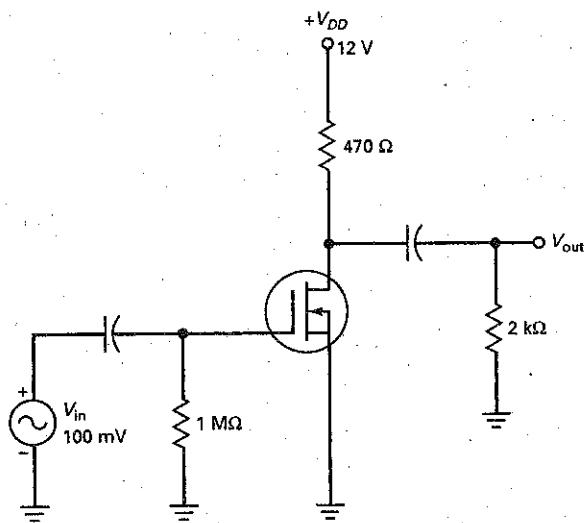
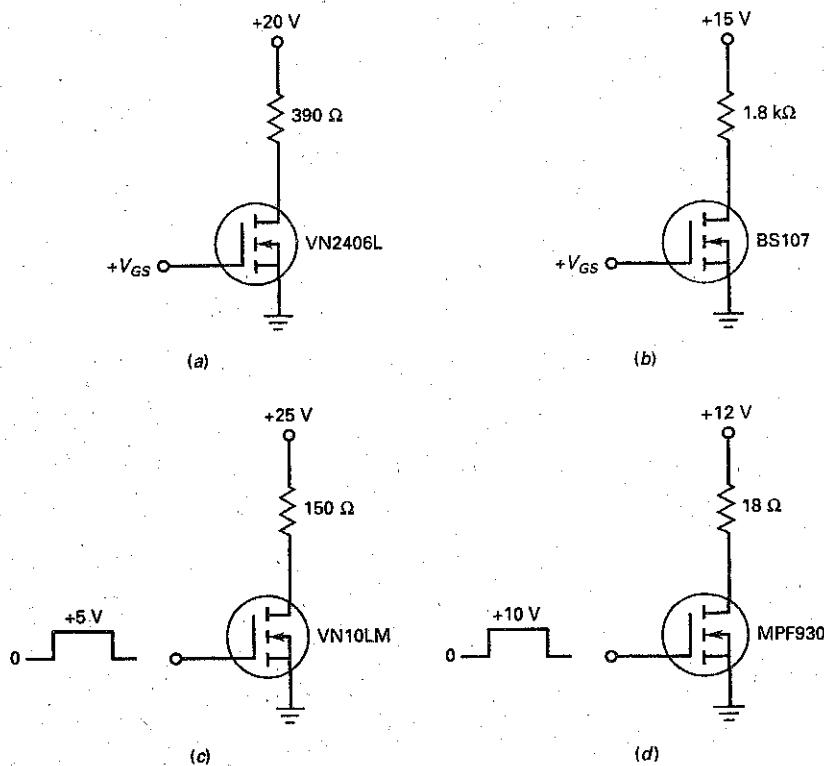


Figure 14-37



- 14-9 An E-MOSFET has $R_{DS(on)} = 2 \Omega$ when $V_{GS(on)} = 3 \text{ V}$ and $I_{D(on)} = 500 \text{ mA}$. If it is biased in the ohmic region, what is the voltage across it for each of these drain currents:

- a. $I_D(\text{sat}) = 25 \text{ mA}$
- c. $I_D(\text{sat}) = 100 \text{ mA}$
- b. $I_D(\text{sat}) = 50 \text{ mA}$
- d. $I_D(\text{sat}) = 200 \text{ mA}$

- 14-10 **MultiSim** What is the voltage across the E-MOSFET in Fig. 14-37a if $V_{GS} = 2.5 \text{ V}$? (Use Table 14-1.)

- 14-11 **MultiSim** Calculate the drain voltage in Fig. 14-37b for a gate voltage of +3 V. Assume that $R_{DS(on)}$ is approximately the same as the value given in Table 14-1.

- 14-12 If V_{GS} is high in Fig. 14-37c, what is the voltage across the load resistor of Fig. 14-37?

- 14-13 Calculate the voltage across the E-MOSFET of Fig. 14-37d for a high input voltage.

- 14-14 What is the LED current in Fig. 14-38a when $V_{GS} = 5 \text{ V}$?

- 14-15 The relay of Fig. 14-38b closes when $V_{GS} = 2.6 \text{ V}$. What is the MOSFET current when the gate voltage is high? The current through the final load resistor?

SEC. 14-6 DIGITAL SWITCHING

- 14-16 An E-MOSFET has these values: $I_{D(\text{active})} = 1 \text{ mA}$ and $V_{DS(\text{active})} = 10 \text{ V}$. What does its drain resistance equal in the active region?

- 14-17 What is the output voltage in Fig. 14-39a when the input is low? When it is high?

- 14-18 In Fig. 14-39b, the input voltage is low. What is the output voltage? If the input goes high, what is the output voltage?

- 14-19 A square wave drives the gate of Fig. 14-39a. If the square wave has a peak-to-peak value large enough to drive the lower MOSFET into the ohmic region, what is the output waveform?

Figure 14-38

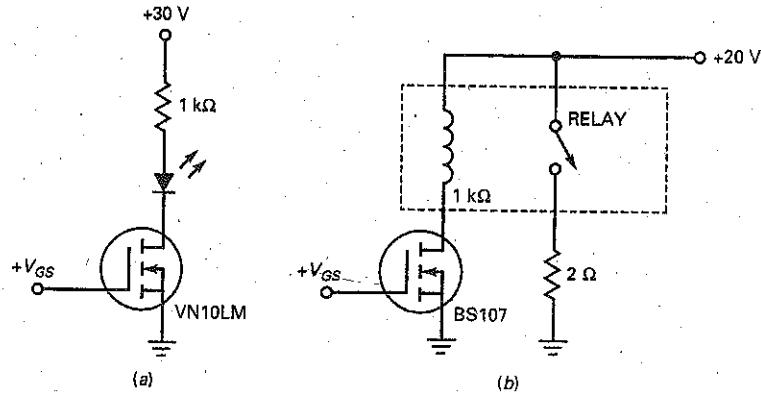


Figure 14-39

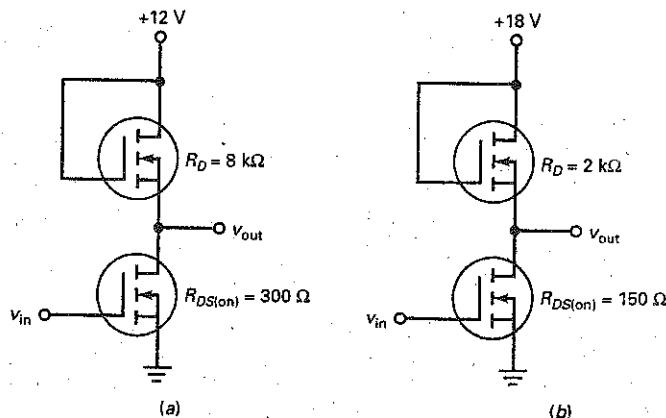
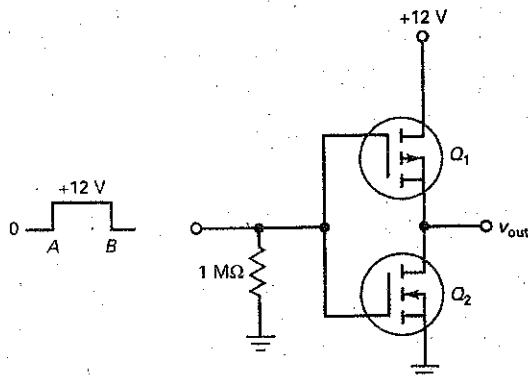


Figure 14-40



SEC. 14-7 CMOS

- 14-20 The MOSFETs of Fig. 14-40 have $R_{DS(on)} = 250 \Omega$ and $R_{DS(off)} = 5 M\Omega$. What is the output waveform?
- 14-21 The upper E-MOSFET of Fig. 14-40 has these values: $I_{D(on)} = 1 \text{ mA}$, $V_{DS(on)} = 1 \text{ V}$, $I_{D(off)} = 1 \mu\text{A}$, and $V_{DS(off)} = 10 \text{ V}$. What is the output voltage when the input voltage is low? When it is high?
- 14-22 A square wave with a peak value of 12 V and a frequency of 1 kHz is the input in Fig. 14-40. Describe the output waveform.
- 14-23 During the transition from low to high in Fig. 14-40, the input voltage is 6 V for an instant. At this time, both MOSFETs have active resistances of $R_D = 5 \text{ k}\Omega$. What is the current drain at this instant?

SEC. 14-8 POWER FETS

- 14-24 What is the current through the motor winding of Fig. 14-41 when the gate voltage is low? When it is high?

Figure 14-41

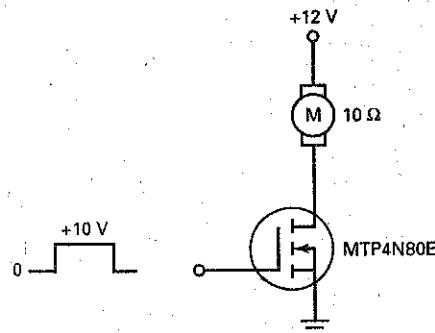
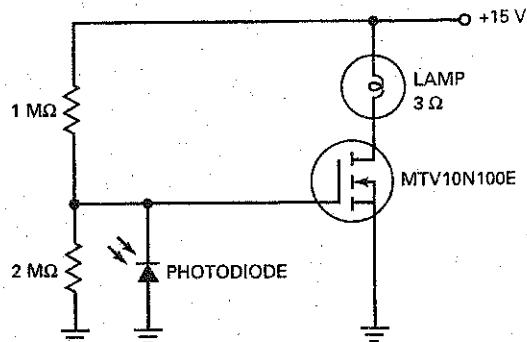


Figure 14-42



14-25 The motor winding of Fig. 14-41 is replaced by another with a resistance of 6Ω . What is the current through the winding when the gate voltage is high?

14-26 What is the current through the lamp of Fig. 14-42 when the gate voltage is low? When it is $+10 \text{ V}$?

14-27 The lamp of Fig. 14-42 is replaced by another with a resistance of 5Ω . What is the lamp power when it is dark?

14-28 What is the current through the water valve of Fig. 14-43 when the gate voltage is high? When it is low?

14-29 The supply voltage of Fig. 14-43 is changed to 12 V and the water valve is replaced by another with a resistance of 18Ω . What is the current through the water valve when the probes are underwater? When the probes are above the water?

Figure 14-43

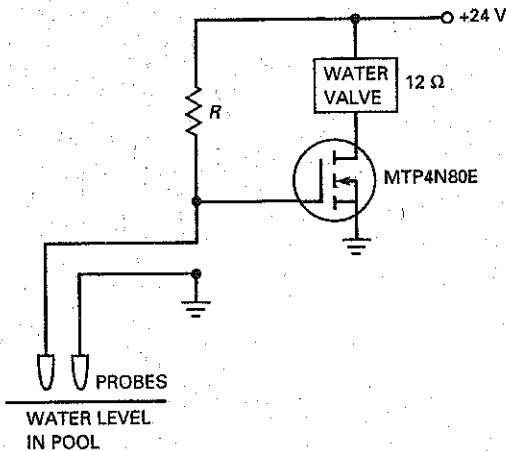
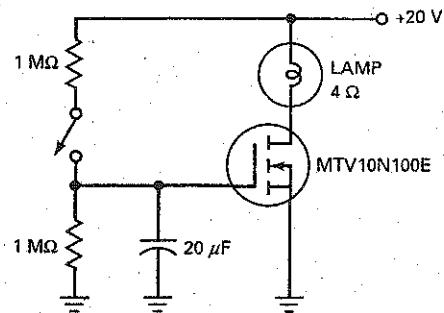


Figure 14-44



14-30 What is the RC time constant in Fig. 14-44? The lamp power at full brightness?

14-31 The two resistances in the gate circuit are doubled in Fig. 14-44. What is the RC time constant? If the lamp is changed to one with a resistance of 6Ω , what is the lamp current at full brightness?

SEC. 14-9 E-MOSFET AMPLIFIERS

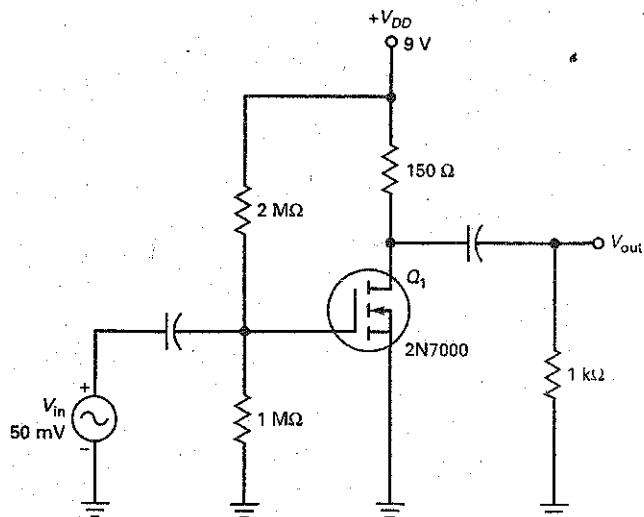
14-32 Find the constant k value and I_D of Fig. 14-45 using the minimum values of $I_{D(on)}$, $V_{GS(on)}$, and $V_{GS(th)}$ for the 2N7000.

14-33 Determine the g_m , A_V and V_{out} values for Fig. 14-45, using the minimum rated specifications.

14-34 In Fig. 14-45, change R_D to 50Ω . Find the constant k value and I_D using the typical values of $I_{D(on)}$, $V_{GS(on)}$, and $V_{GS(th)}$ for the 2N7000.

14-35 Determine the g_m , A_V and V_{out} values for Fig. 14-45, using the typical rated specifications, V_{DD} at $+12\text{ V}$ and $R_D = 15\Omega$.

Figure 14-45



Critical Thinking

- 14-36 In Fig. 14-37c, the gate input voltage is a square wave with a frequency of 1 kHz and a peak voltage of +5 V. What is the average power dissipation in the load resistor?
- 14-37 The gate input voltage of Fig. 14-37d is a series of rectangular pulses with a duty cycle of 25 percent. This means that the gate voltage is high for 25 percent of the cycle and low the rest of the time. What is the average power dissipation in the load resistor?
- 14-38 The CMOS inverter of Fig. 14-40 uses MOSFETs with $R_{DS(on)} = 100 \Omega$ and $R_{DS(off)} = 10 M\Omega$. What is the quiescent power consumption of the circuit? When a square-wave is the input, the average current through Q_1 is 50 μA . What is the power consumption?

- 14-39 If the gate voltage is 3 V in Fig. 14-42, what is the photodiode current?

- 14-40 The data sheet of an MTP16N25E shows a normalized graph of $R_{DS(on)}$ versus temperature. The normalized value increases linearly from 1 to 2.25 as the junction temperature increases from 25 to 125°C. If $R_{DS(on)} = 0.17 \Omega$ at 25°C, what does it equal at 100°C?

- 14-41 In Fig. 14-27, $V_{in} = 12 V$. If the transformer has a turns ratio of 4:1 and the output ripple is very small, what is the dc output voltage V_{out} ?

Job Interview Questions

1. Draw an E-MOSFET showing the p and n regions. Then, explain the off-on action.
2. Describe how active-load switching works. Use circuit diagrams in your explanation.
3. Draw a CMOS inverter and explain the circuit action.
4. Draw any circuit that shows a power FET controlling a large load current. Explain the off-on action. Include $R_{DS(on)}$ in your discussion.
5. Some people say that MOS technology revolutionized the world of electronics. Why?
6. List and compare the advantages and disadvantages of BJT and FET amplifiers.
7. Explain what happens when drain current starts to increase through a power FET.
8. Why must an E-MOSFET be handled with care?
9. Why is a thin metal wire connected around all the leads of a MOSFET during shipment?
10. What are some precautionary measures that are taken while working with MOS-devices?
11. Why would a designer generally select a MOSFET over a BJT for a power-switching function in a switching power supply?

Self-Test Answers

- | | | |
|------|-------|-------|
| 1. c | 10. d | 18. d |
| 2. d | 11. a | 19. c |
| 3. d | 12. b | 20. d |
| 4. c | 13. d | 21. a |
| 5. c | 14. c | 22. b |
| 6. d | 15. a | 23. d |
| 7. d | 16. b | 24. d |
| 8. c | 17. d | 25. c |
| 9. b | | |

Practice Problem Answers

- 14-1 V_{GS} I_D
-1 V 2.25 mA
-2 V 1 mA
0 V 4 mA
+1 V 6.25 mA
+2 V 9 mA

- 14-2 $V_{out} = 105.6 \text{ mV}$
14-3 $V_{out(\text{off})} = 20 \text{ V}$; $V_{out(\text{on})} = 0.198 \text{ V}$
14-4 $I_{LED} = 32 \text{ mA}$
14-6 $V_{out} = 20 \text{ V}$ and 198 mV
14-7 $R_{DS(\text{on})} \approx 222 \Omega$
14-8 If $V_{in} > V_{GS(\text{th})}$; $V_{out} = +15 \text{ V}$ pulse
- 14-9 $I_D = 0.996 \text{ A}$
14-10 $I_L = 2.5 \text{ A}$
14-13 $k = 5.48 \times 10^{-3} \text{ A/V}^2$; $I_D = 26 \text{ mA}$
14-14 $R_D = 4 \text{ k}\Omega$
14-15 $V_{GS} = 2.98 \text{ V}$; $I_D = 80 \text{ mA}$; $g_m = 183 \text{ mS}$; $A_V = 11.7$; $V_{out} = 1.17 \text{ V}$

15

Thyristors

- The word thyristor comes from the Greek and means "door," as in opening a door and letting something pass through it. A thyristor is a semiconductor device that uses internal feedback to produce switching action. The most important thyristors are the silicon controlled rectifier (SCR) and the triac. Like power FETs, the SCR and the triac can switch large currents on and off. Because of this, they can be used for overvoltage protection, motor controls, heaters, lighting systems, and other heavy-current loads. Insulated-gate bipolar transistors (IGBTs) are not included in the thyristor family, but are covered in this chapter as an important power-switching device.

Chapter Outline

- 15-1 The Four-Layer Diode
- 15-2 The Silicon Controlled Rectifier
- 15-3 The SCR-Crowbar
- 15-4 SCR Phase Control
- 15-5 Bidirectional Thyristors
- 15-6 IGBTs
- 15-7 Other Thyristors
- 15-8 Troubleshooting

Objectives

After studying this chapter, you should be able to:

- Describe the four-layer diode, how it is turned on, and how it is turned off.
- Explain the characteristics of SCRs.
- Demonstrate how to test SCRs.
- Calculate the firing and conduction angles of RC phase control circuits.
- Explain the characteristics of triacs and diacs.
- Compare the switching control of IGBTs to power MOSFETs.
- Describe the major characteristics of the photo-SCR and silicon controlled switch.
- Explain the operation of UJT and PUT circuits.

Vocabulary

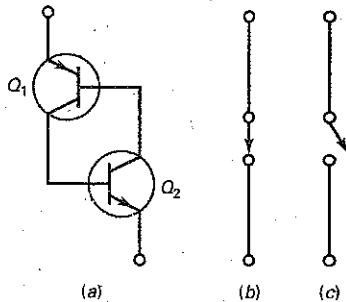
breakover
conduction angle
diac
firing angle
four-layer diode
gate trigger current I_{GT}
gate trigger voltage V_{GT}

holding current
Insulated-gate bipolar transistor (IGBT)
low-current drop-out
programmable unijunction transistor (PUT)
sawtooth generator

Schockley diode
SCR
silicon unilateral switch (SUS)
thyristor
triac
unijunction transistor (UJT)

15-1 The Four-Layer Diode

Figure 15-1 Transistor latch.



Thyristor operation can be explained in terms of the equivalent circuit shown in Fig. 15-1a. The upper transistor Q_1 is a *pnp* device, and the lower transistor Q_2 is an *npn* device. The collector of Q_1 drives the base of Q_2 . Similarly, the collector of Q_2 drives the base of Q_1 .

Positive Feedback

The unusual connection of Fig. 15-1a uses *positive feedback*. Any change in the base current of Q_2 is amplified and fed back through Q_1 to magnify the original change. This positive feedback continues changing the base current of Q_2 until both transistors go into either saturation or cutoff.

For instance, if the base current of Q_2 increases, the collector current of Q_2 increases. This increases the base current of Q_1 and the collector current of Q_1 . More collector current in Q_1 will further increase the base current of Q_2 . This amplify-and-feedback action continues until both transistors are driven into saturation. In this case, the overall circuit acts like a closed switch (Fig. 15-1b).

On the other hand, if something causes the base current of Q_2 to decrease, the collector current of Q_2 decreases, the base current of Q_1 decreases, the collector current of Q_1 decreases, and the base current of Q_2 decreases further. This action continues until both transistors are driven into cutoff. Then, the circuit acts like an open switch (Fig. 15-1c).

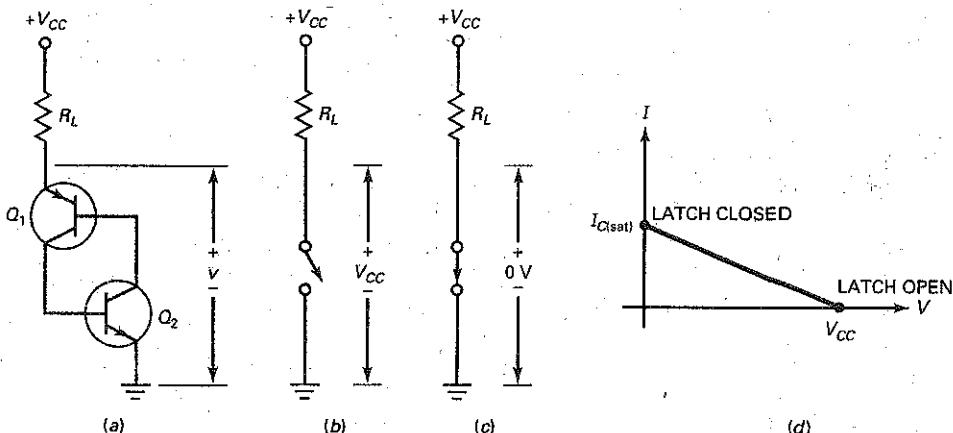
The circuit of Fig. 15-1a is stable in either of two states: *open* or *closed*. It will remain in either state indefinitely until acted on by an outside force. If the circuit is open, it stays open until something increases the base current of Q_2 . If the circuit is closed, it stays closed until something decreases the base current of Q_2 . Because the circuit can remain in either state indefinitely, it is called a *latch*.

Closing a Latch

Figure 15-2a shows a latch connected to a load resistor with a supply voltage of V_{CC} . Assume that the latch is open, as shown in Fig. 15-2b. Because there is no current through the load resistor, the voltage across the latch equals the supply voltage. So, the operating point is at the lower end of the dc load line (Fig. 15-2d).

The only way to close the latch of Fig. 15-2b is by **breakover**. This means using a large enough supply voltage V_{CC} to break down the Q_1 collector diode. Since the collector current of Q_1 increases the base current of Q_2 , the positive

Figure 15-2 Latching circuit.



GOOD TO KNOW

The four-layer diode is rarely, if ever, used in modern circuit design. In fact, most device manufacturers no longer make them. In spite of the fact that the device is nearly obsolete, it is covered in detail here because most of the operating principles of the four-layer diode can be applied to many of the more commonly used thyristors. In fact, most thyristors are nothing more than slight variations of the basic four-layer diode.

feedback will start. This drives both transistors into saturation, as previously described. When saturated, both transistors ideally look like short circuits, and the latch is closed (Fig. 15-2c). Ideally, the latch has zero voltage across it when it is closed and the operating point is at the upper end of the load line (Fig. 15-2d).

In Fig. 15-2a, breakdown can also occur if Q_2 breaks down first. Although breakdown starts with the breakdown of either collector diode, it ends with both transistors in the saturated state. This is why the term *breakover* is used instead of *breakdown* to describe this kind of latch closing.

Opening a Latch

How do we open the latch of Fig. 15-2a? By reducing the V_{CC} supply to zero. This forces the transistors to switch from saturation to cutoff. We call this type of opening **low-current drop-out** because it depends on reducing the latch current to a value low enough to bring the transistors out of saturation.

The Schockley Diode

Figure 15-3a was originally called a Schockley diode after the inventor. Several other names are also used for this device: **four-layer diode**, **pnpn diode**, and **silicon unilateral switch (SUS)**. The device lets current flow in only one direction.

The easiest way to understand how it works is to visualize it separated into two halves, as shown in Fig. 15-3b. The left half is a *pnp transistor*, and the right half is an *npn transistor*. Therefore, the four-layer diode is equivalent to the latch of Fig. 15-3c.

Figure 15-3d shows the schematic symbol of a four-layer diode. The only way to close a four-layer diode is by breakover. The only way to open it is by low-current drop-out, which means reducing the current to less than the **holding current** (given on data sheets). The holding current is the low value of current where the transistors switch from saturation to cutoff.

After a four-layer diode breaks over, the voltage across it ideally drops to zero. In reality, there is some voltage across the latched diode. Figure 15-3e shows current versus voltage for a 1N5158 that is latched on. As you can see, the voltage across the device increases when the current increases: 1 V at 0.2 A, 1.5 V at 0.95 A, 2 V at 1.8 A, and so on.

Breakover Characteristic

Figure 15-4 shows the graph of current versus voltage of a four-layer diode. The device has two operating regions: cutoff and saturation. The dashed line is the

Figure 15-3 Four-layer diode.

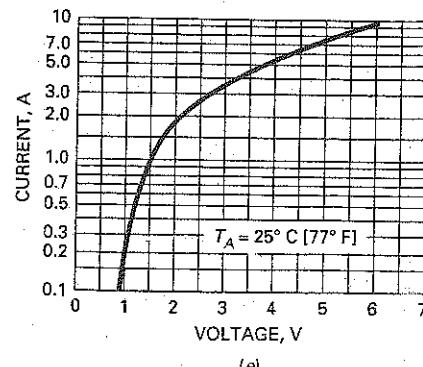
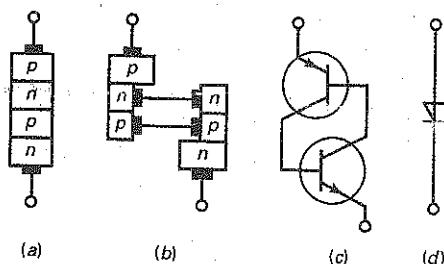
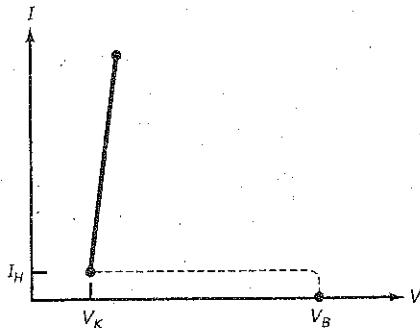


Figure 15-4 Breakover characteristic.



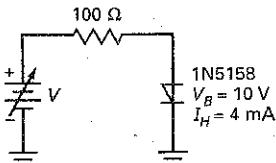
transition path between cutoff and saturation. It is dashed to indicate that the device switches rapidly between the off and on states.

When the device is at cutoff, it has zero current. If the voltage across diode tries to exceed V_B , the device breaks over and moves rapidly along the dashed line to the saturation region. When the diode is in saturation, it is operating on the upper line. As long as the current through it is greater than the holding current I_H , the diode remains latched in the on state. If the current becomes less than I_H , the device switches into cutoff.

The ideal approximation of a four-layer diode is an open switch when cut off and a closed switch when saturated. The second approximation includes the knee voltage V_K , approximately 0.7 V in Fig. 15-4. For higher approximations, use computer simulation software or refer to the data sheet of the four-layer diode.

Example 15-1

Figure 15-5 Example.



The diode of Fig. 15-5 has a breakover voltage of 10 V. If the input voltage of Fig. 15-5 is increased to +15 V, what is the diode current?

SOLUTION Since an input voltage of 15 V is more than the break-over voltage of 10 V, the diode breaks over. Ideally, the diode is like a closed switch, so the current is:

$$I = \frac{15 \text{ V}}{100 \Omega} = 150 \text{ mA}$$

To a second approximation:

$$I = \frac{15 \text{ V} - 0.7 \text{ V}}{100 \Omega} = 143 \text{ mA}$$

For a more accurate answer, look at Fig. 15-3e and you will see that the voltage is 0.9 V when the current is around 150 mA. Therefore, an improved answer is:

$$I = \frac{15 \text{ V} - 0.9 \text{ V}}{100 \Omega} = 141 \text{ mA}$$

PRACTICE PROBLEM 15-1 In Fig. 15-5, determine the diode current if the input voltage V is 12 V, to a second approximation.

Example 15-2

The diode of Fig. 15-5 has a holding current of 4 mA. The input voltage is increased to 15 V to latch the diode, and then decreased to open the diode. What is the input voltage that opens the diode?

SOLUTION The diode opens when the current is slightly less than the holding current, given as 4 mA. At this small current, the diode voltage is approximately equal to the knee voltage, 0.7 V. Since 4 mA flows through $100\ \Omega$, the input voltage is:

$$V_{in} = 0.7\text{ V} + (4\text{ mA})(100\ \Omega) = 1.1\text{ V}$$

So, the input voltage has to be reduced from 15 V to slightly less than 1.1 V to open the diode.

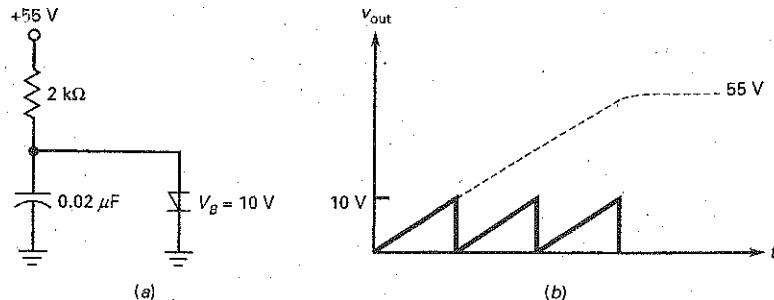
PRACTICE PROBLEM 15-2 Repeat Example 15-2 using a diode with a holding current of 10 mA.

Example 15-3

Figure 15-6a shows a sawtooth generator. The capacitor charges toward the supply voltage, as shown in Fig. 15-6b. When the capacitor voltage reaches +10 V, the diode breaks over. This discharges the capacitor, producing the flyback (sudden voltage drop) of the output waveform. When the voltage is ideally zero, the diode opens and the capacitor begins to charge again. In this way, we get the ideal sawtooth shown in Fig. 15-6b.

What is the RC time constant for capacitor charging? What is the frequency of the sawtooth wave if its period is approximately 20 percent of the time constant?

Figure 15-6 Sawtooth generator.



SOLUTION The RC time constant is:

$$RC = (2\text{ k}\Omega)(0.02\text{ }\mu\text{F}) = 40\text{ }\mu\text{s}$$

The period is approximately 20 percent of the time constant. So:

$$T = 0.2(40\text{ }\mu\text{s}) = 8\text{ }\mu\text{s}$$

The frequency is:

$$f = \frac{1}{8\text{ }\mu\text{s}} = 125\text{ kHz}$$

PRACTICE PROBLEM 15-3 Using Fig. 15-6, change the resistor value to $1\text{ k}\Omega$ and solve for the sawtooth frequency.

GOOD TO KNOW

SCRs are designed to handle higher values of current and voltage than any other type of thyristor.

Presently, some SCRs are capable of controlling large currents up to 1.5 kA and voltages in excess of 2 kV.

15-2 The Silicon Controlled Rectifier

The SCR is the most widely used thyristor. It can switch very large currents on and off. Because of this, it is used to control motors, ovens, air conditioners, and induction heaters.

Triggering the Latch

By adding an input terminal to the base of Q_2 , as shown in Fig. 15-7a, we can create a second way to close the latch. Here is the theory of operation: When the latch is open, as shown in Fig. 15-7b, the operating point is at the lower end of the dc load line (Fig. 15-7d). To close the latch, we can couple a trigger (sharp pulse) into the base of Q_2 , as shown in Fig. 15-7a. The trigger momentarily increases the base current of Q_2 . This starts the positive feedback, which drives both transistors into saturation.

When saturated, both transistors ideally look like short circuits, and the latch is closed (Fig. 15-7c). Ideally, the latch has zero voltage across it when it is closed, and the operating point is at the upper end of the load line (Fig. 15-7d).

Gate Triggering

Figure 15-8a shows the structure of the SCR. The input is called the *gate*, the top is the *anode*, and the bottom is the *cathode*. The SCR is far more useful than a four-layer diode because the gate triggering is easier than breakdown triggering.

Figure 15-7 Transistor latch with trigger input.

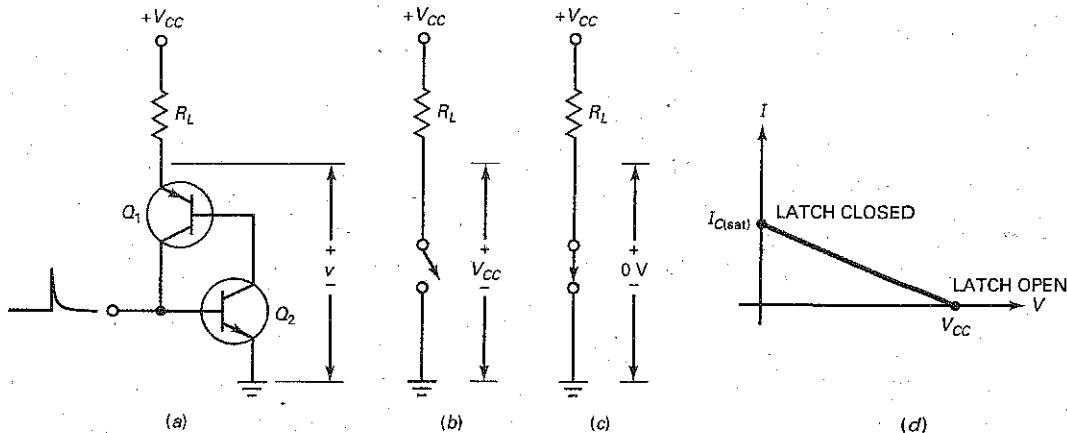


Figure 15-8 Silicon controlled rectifier (SCR).

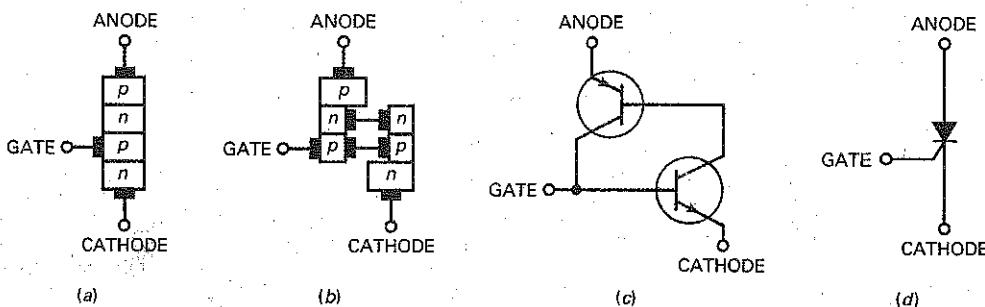
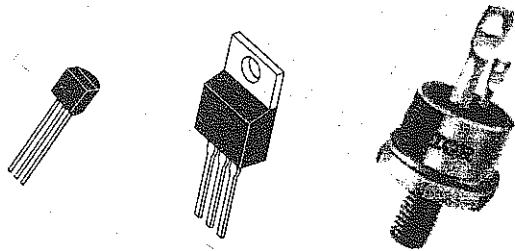


Figure 15-9 Typical SCRs.



Again, we can visualize the four doped regions separated into two transistors, as shown in Fig. 15-8b. Therefore, the SCR is equivalent to a latch with a trigger input (Fig. 15-8c). Schematic diagrams use the symbol of Fig. 15-8d. Whenever you see this symbol, remember that it is equivalent to a latch with a trigger input. Typical SCRs are shown in Fig. 15-9.

Since the gate of an SCR is connected to the base of an internal transistor, it takes at least 0.7 V to trigger an SCR. Data sheets list this voltage as the **gate trigger voltage** V_{GT} . Rather than specify the input resistance of the gate, a manufacturer gives the minimum input current needed to turn on the SCR. Data sheets list this current as the **gate trigger current** I_{GT} .

Fig. 15-10 shows a data sheet for the 2N6504 series of SCRs. For this series, it shows typical trigger voltage and current values of:

$$V_{GT} = 1.0 \text{ V}$$

$$I_{GT} = 9.0 \text{ mA}$$

This means that the source driving the gate of a typical 2N6504 series SCR has to supply 9.0 mA at 1.0 V to latch the SCR.

Also, the breakdown voltage or blocking voltage is specified as its peak repetitive off state forward voltage, V_{DRM} , and its peak repetitive off state reverse voltage, V_{RRM} . Depending on which SCR of the series is used, the breakdown voltage ranges from 50 V to 800 V.

Required Input Voltage

An SCR like the one shown in Fig. 15-11 has a gate voltage V_G . When this voltage is more than V_{GT} , the SCR will turn on and the output voltage will drop from $+V_{CC}$ to a low value. Sometimes, a gate resistor is used as shown here. This resistor limits the gate current to a safe value. The input voltage needed to trigger an SCR has to be more than:

$$V_{in} = V_{GT} + I_{GT}R_G \quad (15-1)$$

In this equation, V_{GT} and I_{GT} are the gate trigger voltage and current for the device. For instance, the data sheet of a 2N4441 gives $V_{GT} = 0.75 \text{ V}$ and $I_{GT} = 10 \text{ mA}$. When you have the value of R_G , the calculation of V_{in} is straightforward. If a gate resistor is not used, R_G is the Thevenin resistance of the circuit driving the gate. Unless Eq. (15-1) is satisfied, the SCR cannot turn on.

Resetting the SCR

After the SCR has turned on, it stays on even though you reduce the gate supply, V_{in} , to zero. In this case, the output remains low indefinitely. To reset the SCR, you must reduce the anode to cathode current to a value less than its holding current, I_H . This can be done by reducing V_{CC} to a low value. The data sheet for the

Figure 15-10 SCR data sheet.

2N6504 Series

Preferred Device

Silicon Controlled Rectifiers

Reverse Blocking Thyristors

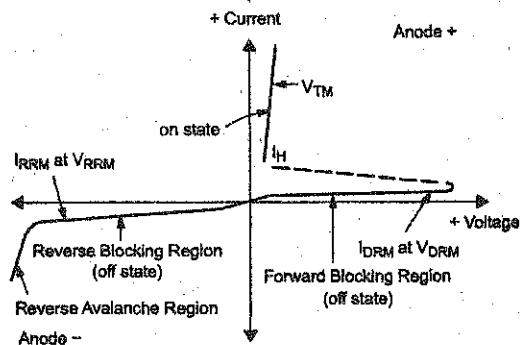
Designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supply crowbar circuits.

Features

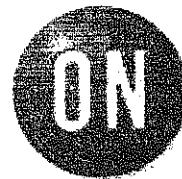
- Glass Passivated Junctions with Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Constructed for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts
- 300 A Surge Current Capability
- Pb-Free Packages are Available*

2N6504 Series

Voltage Current Characteristic of SCR



Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On State Voltage
I_H	Holding Current



ON Semiconductor®

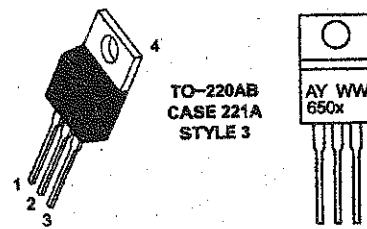
<http://onsemi.com>

SCRs

25 AMPERES RMS
50 thru 800 VOLTS



MARKING DIAGRAM



x = 4, 5, 7, 8 or 9
A = Assembly Location
Y = Year
WW = Work Week

PIN ASSIGNMENT	
1	Cathode
2	Anode
3	Gate
4	Anode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Figure 15-10 (continued)

2N6504 Series

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (Note 1) (Gate Open, Sine Wave 50 to 60 Hz, $T_J = 25$ to 125°C)	V_{DRM} , V_{RRM}		V
2N6504		50	
2N6505		100	
2N6507		400	
2N6508		600	
2N6509		800	
On-State Current RMS (180° Conduction Angles; $T_C = 85^\circ\text{C}$)	$I_{(RMS)}$	25	A
Average On-State Current (180° Conduction Angles; $T_C = 85^\circ\text{C}$)	$I_{(AV)}$	16	A
Peak Non-repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, $T_J = 100^\circ\text{C}$)	$I_{(SM)}$	250	A
Forward Peak Gate Power (Pulse Width $\leq 1.0 \mu\text{s}$, $T_C = 85^\circ\text{C}$)	P_{GM}	20	W
Forward Average Gate Power ($t = 8.3 \text{ ms}$, $T_C = 85^\circ\text{C}$)	$P_{G(AV)}$	0.5	W
Forward Peak Gate Current (Pulse Width $\leq 1.0 \mu\text{s}$, $T_C = 85^\circ\text{C}$)	I_{GM}	2.0	A
Operating Junction Temperature Range	T_J	-40 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{sg}	-40 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction-to-Case	R_{JC}	1.5	$^\circ\text{C}/\text{W}$
*Maximum Lead Temperature for Soldering Purposes 1/8 in from Case for 10 Seconds	T_L	260	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
*Peak Repetitive Forward or Reverse Blocking Current (V_{AK} = Rated V_{DRM} or V_{RRM} , Gate Open)	$I_{(DRM)}$, $I_{(RRM)}$	-	-	10 2.0	μA mA

ON CHARACTERISTICS

*Forward On-State Voltage (Note 2) ($I_{TM} = 50 \text{ A}$)	V_{TM}	-	-	1.8	V
*Gate Trigger Current (Continuous dc) ($V_{AK} = 12 \text{ Vdc}$, $R_L = 100 \Omega$)	I_{GT}	-	9.0 -	30 75	mA
*Gate Trigger Voltage (Continuous dc) ($V_{AK} = 12 \text{ Vdc}$, $R_L = 100 \Omega$, $T_C = -40^\circ\text{C}$)	V_{GT}	-	1.0	1.5	V
Gate Non-Trigger Voltage ($V_{AK} = 12 \text{ Vdc}$, $R_L = 100 \Omega$, $T_J = 125^\circ\text{C}$)	V_{GD}	0.2	-	-	V
*Holding Current ($V_{AK} = 12 \text{ Vdc}$, Initiating Current = 200 mA, Gate Open) $T_C = -40^\circ\text{C}$	I_H	-	18 -	40 80	mA
*Turn-On Time ($I_{TM} = 25 \text{ A}$, $I_{GT} = 50 \text{ mA dc}$)	t_{on}	-	1.5	2.0	μs
Turn-Off Time (V_{DRM} = rated voltage) ($I_{TM} = 25 \text{ A}$, $I_R = 25 \text{ A}$) ($I_{TM} = 25 \text{ A}$, $I_R = 25 \text{ A}$, $T_J = 125^\circ\text{C}$)	t_{off}	-	15 35	-	μs

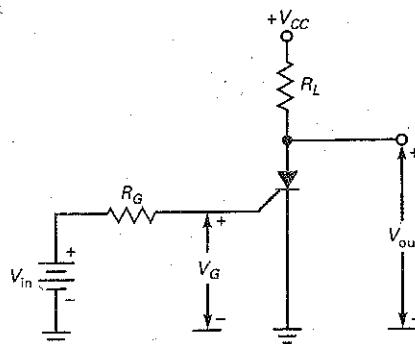
DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage (Gate Open, Rated V_{DRM} , Exponential Waveform)	dV/dt	-	'50	-	$\text{V}/\mu\text{s}$
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*Indicates JEDEC Registered Data.

2. Pulse Test; Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

Figure 15-11 Basic SCR circuit.



2N6504 lists a typical holding current value of 18 mA. SCRs with lower and higher power ratings generally have lower and higher respective holding current values. Since the holding current flows through the load resistor in Fig. 15-11, the supply voltage for turnoff has to be less than:

$$V_{CC} = 0.7 \text{ V} + I_H R_L \quad (15-2)$$

Besides reducing V_{CC} , other methods can be used to reset the SCR. Two common methods are current interruption and forced commutation. By either opening the series switch, as shown in Fig. 15-12a, or closing the parallel switch in Fig. 15-12b, the anode-to-cathode current will drop below its holding current value and the SCR will switch to its off state.

Another method used to reset the SCR is forced commutation, as shown in Fig. 15-12c. When the switch is depressed, a negative V_{AK} voltage is momentarily applied. This reduces the forward anode-to-cathode current below I_H and turns off the SCR. In actual circuits, the switch can be replaced with a BJT or FET device.

Figure 15-12 Resetting the SCR.

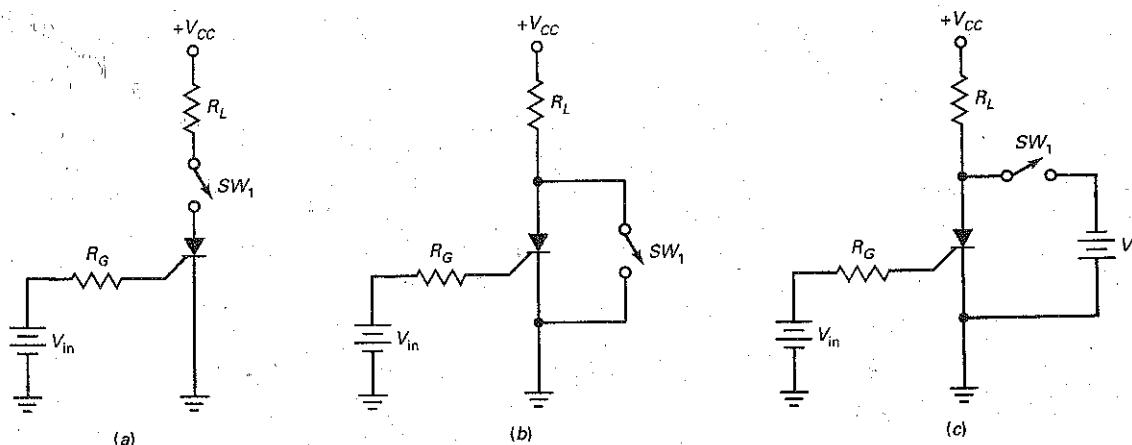
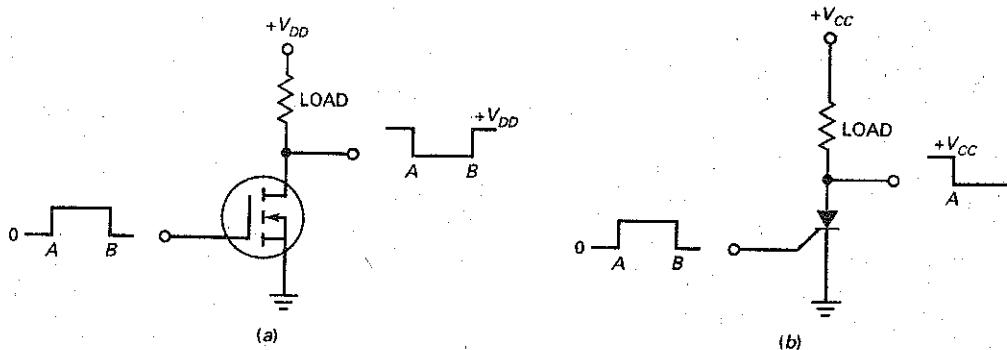


Figure 15-13 Power FET versus SCR.



Power FET versus SCR

Although both the power FET and the SCR can switch large currents on and off, the two devices are fundamentally different. The key difference is the way they turn off. The gate voltage of a power FET can turn the device on and off. This is not the case with an SCR. The gate voltage can only turn it on.

Figure 15-13 illustrates the difference. In Fig. 15-13a, when the input voltage to the power FET goes high, the output voltage goes low. When the input voltage goes low, the output voltage goes high. In other words, a rectangular input pulse produces an inverted rectangular output pulse.

In Fig. 15-13b, when the input voltage to the SCR goes high, the output voltage goes low. But when the input voltage goes low, the output voltage stays low. With an SCR, a rectangular input pulse produces a negative-going output step. The SCR does not reset.

Because the two devices have to be reset in different ways, their applications tend to be different. Power FETs respond like push-button switches, whereas SCRs respond like single pole single-throw switches. Since it is easier to control the power FET, you will see it used more often as an interface between digital ICs and heavy loads. In applications in which latching is important, you will see the SCR used.

Example 15-4

III Multisim

In Fig. 15-14, the SCR has a trigger voltage of 0.75 V and a trigger current of 7 mA. What is the input voltage that turns the SCR on? If the holding current is 6 mA, what is the supply voltage that turns it off?

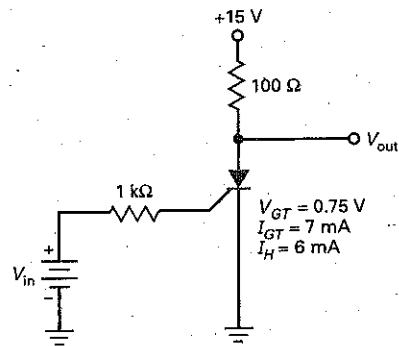
SOLUTION With Eq. (15-1), the minimum input voltage needed to trigger is:

$$V_{in} = 0.75 \text{ V} + (7 \text{ mA})(1 \text{ k}\Omega) = 7.75 \text{ V}$$

With Eq. (15-2), the supply voltage that turns off the SCR is:

$$V_{CC} = 0.7 \text{ V} + (6 \text{ mA})(100 \Omega) = 1.3 \text{ V}$$

Figure 15-14 Example.

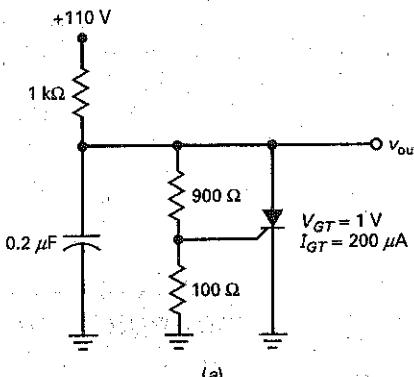


PRACTICE PROBLEM 15-4 In Fig. 15-14, determine the input voltage needed to trigger the SCR on and the supply voltage that turns off the SCR, using the typical rated values for a 2N6504 SCR.

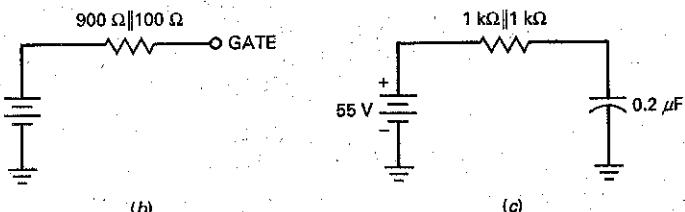
Example 15-5

What does the circuit of Fig. 15-15a do? What is the peak output voltage? What is the frequency of the sawtooth wave if its period is approximately 20 percent of the time constant?

Figure 15-15 Example.



(a)



(b)

(c)

SOLUTION As the capacitor voltage increases, the SCR eventually *fires* (turns on) and rapidly discharges the capacitor. When the SCR opens, the capacitor begins charging again. Therefore, the output voltage is a sawtooth wave similar to the one in Fig. 15-15b, discussed in Example 15-3.

Figure 15-15b shows the Thevenin circuit facing the gate. The Thevenin resistance is:

$$R_{TH} = 900 \Omega \parallel 100 \Omega = 90 \Omega$$

With Eq. (15-1), the input voltage needed to trigger is:

$$V_{in} = 1 \text{ V} + (200 \mu\text{A})(90 \Omega) \approx 1 \text{ V}$$

Because of the 10:1 voltage divider, the gate voltage is one-tenth of the output voltage. Therefore, the output voltage at the SCR firing point is:

$$V_{peak} = 10(1 \text{ V}) = 10 \text{ V}$$

Figure 15-15c shows the Thevenin circuit facing the capacitor when the SCR is off. From this, you can see that the capacitor will try charging to a final voltage of +50 V with a time constant of:

$$RC = (500 \Omega)(0.2 \mu\text{F}) = 100 \mu\text{s}$$

Since the period of the sawtooth is approximately 20 percent of this:

$$T = 0.2(100 \mu\text{s}) = 20 \mu\text{s}$$

The frequency is:

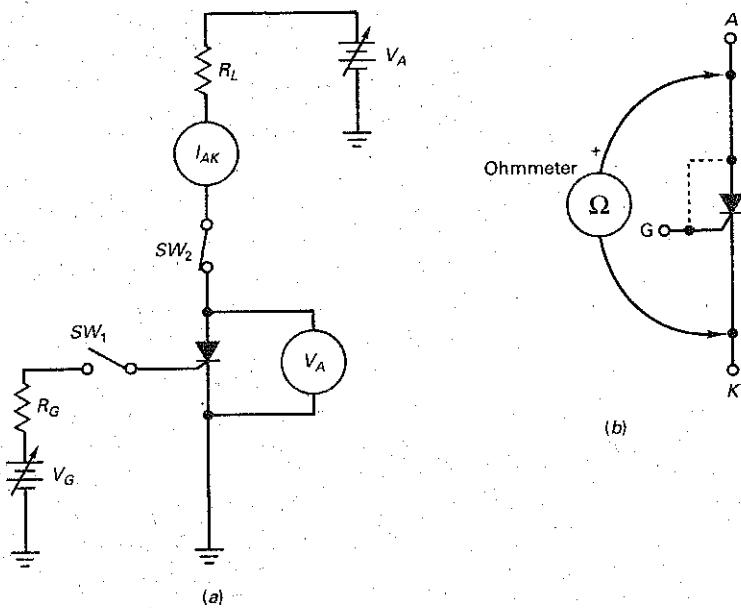
$$f = \frac{1}{20 \mu\text{s}} = 50 \text{ kHz}$$

Testing SCRs

Thyristors, like SCRs, handle large amounts of current and must block high-voltage values. Because of this, they may fail under these conditions. Common failures are A-K opens, A-K shorts, and no gate control. Fig. 15-16a shows a circuit that can test the operation of SCRs. Before SW_1 is pushed, I_{AK} should be zero and V_{AK} should be approximately equal to V_A . When SW_1 is momentarily pushed, I_{AK} should rise to a level near V_A/R_L and V_{AK} should drop to approximately 1 V. V_A and R_L must be selected to provide the necessary current and power levels. When SW_1 is released, the SCR should remain in the on state. The anode supply voltage, V_A , can then be reduced until the SCR drops out of conduction. By observing the anode current value just before the SCR turns off, you can determine the SCR's holding current.

Another method to test SCRs is by using an ohmmeter. The ohmmeter must be able to provide the necessary gate voltage and current to turn on the SCR and, just as important, provide the holding current required to keep the SCR in the on state. Many analog VOMs are capable of outputting approximately 1.5 V and 100 mA in the $R \times 1$ range. In Fig. 15-16b, the ohmmeter is placed across the anode-cathode leads. With either polarity connection, the result should be a very high resistance. With the positive test lead connected to the anode and negative test lead connected to the cathode, connect a jumper wire from the anode to the gate. The SCR should turn on and show a low resistance reading. When the gate lead is disconnected, the SCR should remain in the on state. Momentarily disconnecting the anode test lead will turn the SCR off.

Figure 15-16 Testing SCRs: (a) Test circuit; (b) Ohmmeter.



15-3 The SCR Crowbar

If anything happens inside a power supply to cause its output voltage to go excessively high, the results can be devastating. Why? Because some loads such as expensive digital ICs cannot withstand too much supply voltage without being destroyed. One of the most important applications of the SCR is to protect delicate and expensive loads against overvoltages from a power supply.

Prototype

Figure 15-17 shows a power supply of V_{CC} applied to a protected load. Under normal conditions, V_{CC} is less than the breakdown voltage of the zener diode. In this case, there is no voltage across R , and the SCR remains open. The load receives a voltage of V_{CC} , and all is well.

Now, assume that the supply voltage increases for any reason whatsoever. When V_{CC} is too large, the zener diode breaks down and a voltage appears across R . If this voltage is greater than the gate trigger voltage of the SCR, the SCR fires and becomes a closed latch. The action is similar to throwing a crowbar

Figure 15-17 SCR crowbar.

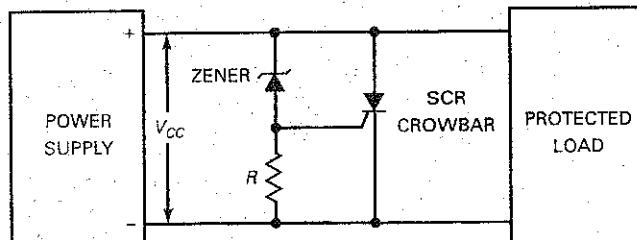
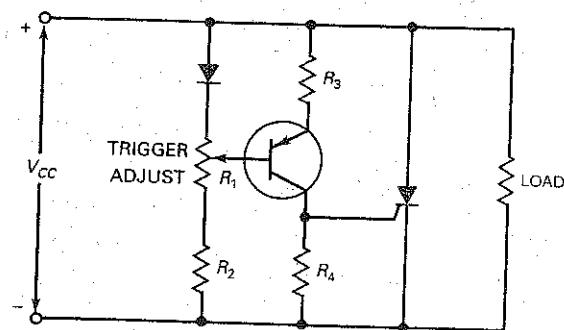


Figure 15-18 Adding transistor gain to crowbar.



across the load terminals. Because the SCR turn-on is very fast ($1\ \mu s$ for a 2N4441), the load is quickly protected against the damaging effects of a large overvoltage. The overvoltage that fires the SCR is:

$$V_{CC} = V_Z + V_{GT} \quad (15-3)$$

Crowbarring, though a drastic form of protection, is necessary with many digital ICs because they can't take much overvoltage. Rather than destroy expensive ICs, therefore, we can use an SCR crowbar to short the load terminals at the first sign of overvoltage. With an SCR crowbar, a fuse or *current limiting* (discussed later) is needed to prevent damage to the power supply.

Adding Voltage Gain

The crowbar of Fig. 15-17 is a *prototype*, a basic circuit that can be modified and improved. It is adequate for many applications as is. But it suffers from a *soft turn-on* because the knee at zener breakdown is curved rather than sharp. When we take into account the tolerance in zener voltages, the soft turn-on can result in the supply voltage becoming dangerously high before the SCR fires.

One way to overcome the soft turn-on is by adding some voltage gain, as shown in Fig. 15-18. Normally, the transistor is off. But when the output voltage increases, the transistor eventually turns on and produces a large voltage across R_4 . Since the transistor provides a swamped voltage gain of approximately R_4/R_3 , a small overvoltage can trigger the SCR.

Notice that an ordinary diode is being used, not a zener diode. This diode temperature-compensates the transistor's base-emitter diode. The *trigger adjust* allows us to set the *trip point* of the circuit, typically around 10 to 15 percent above the normal voltage.

IC Voltage Gain

Figure 15-19 shows an even better solution. The triangular box is an IC amplifier called a *comparator* (discussed in later chapters). This amplifier has a noninverting (+) input and an inverting (-) input. When the noninverting input is greater than the inverting input, the output is positive. When the inverting input is greater than the noninverting input, the output is negative.

The amplifier has a very large voltage gain, typically 100,000 or more. Because of its large voltage gain, the circuit can detect the slightest overvoltage. The zener diode produces 10 V, which goes to the minus input of the amplifier. When the supply voltage is 20 V (normal output), the trigger adjust is set to produce slightly less than 10 V on the positive input. Since the negative input is greater than the positive, the amplifier output is negative and the SCR is open.

Figure 15-19 Adding IC amplifier to crowbar.

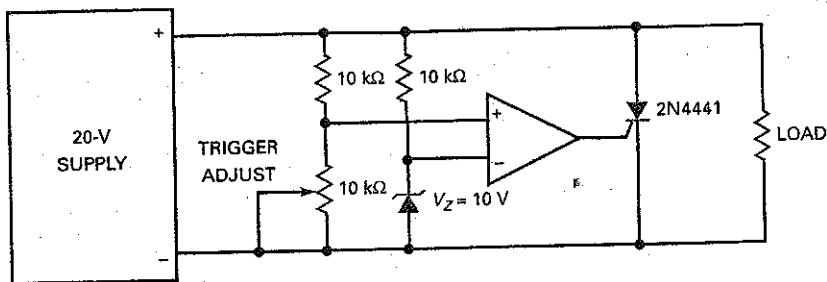
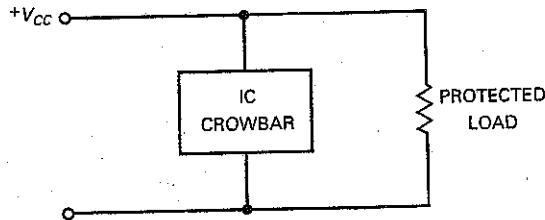


Figure 15-20 IC crowbar.



If the supply voltage rises above 20 V, the positive input to the amplifier becomes greater than 10 V. Then, the amplifier output becomes positive and the SCR fires. This rapidly shuts down the supply by crowbarring the load terminals.

Integrated Crowbar

The simplest solution is to use an IC crowbar, as shown in Fig. 15-20. This is an integrated circuit with a built-in zener diode, transistors, and an SCR. The RCA SK9345 series of IC crowbars is an example of what is commercially available. The SK9345 protects power supplies of +5 V, the SK9346 protects +12 V, and the SK9347 protects +15 V.

If an SK9345 is used in Fig. 15-20, it will protect the load with a supply voltage of +5 V. The data sheet of an SK9345 indicates that it fires at +6.6 V with a tolerance of ± 0.2 V. This means that it fires between 6.4 and 6.8 V. Since 7 V is the maximum rating of many digital ICs, the SK9345 protects the load under all operating conditions.

Example 15-6

Multisim

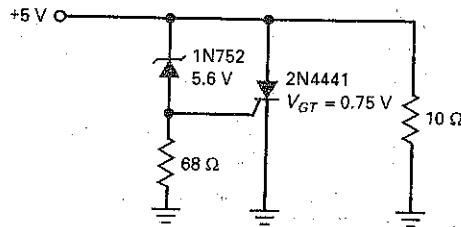
Calculate the supply voltage that turns on the crowbar of Fig. 15-21.

SOLUTION The 1N752 has a breakdown voltage of 5.6 V, and the 2N4441 has a gate trigger voltage of 0.75 V. With Eq. (15-3):

$$V_{CC} = V_Z + V_{GT} = 5.6\text{ V} + 0.75\text{ V} = 6.35\text{ V}$$

When the supply voltage increases to this level, the SCR fires.

Figure 15-21 Example.



The prototype crowbar is all right if the application is not too critical about the exact supply voltage at which the SCR turns on. For instance, the 1N752 has a tolerance of ± 10 percent, which means that the breakdown voltage may vary from 5.04 to 6.16 V. Furthermore, the trigger voltage of a 2N4441 has a worst-case maximum of 1.5 V. So, the overvoltage can be as high as:

$$V_{CC} = 6.16 \text{ V} + 1.5 \text{ V} = 7.66 \text{ V}$$

Since many digital ICs have a maximum rating of 7 V, the simple crowbar of Fig. 15-21 cannot be used to protect them.

PRACTICE PROBLEM 15-6 Repeat Example 15-6 using a 1N4733A zener diode. This diode has a zener voltage of $5.1 \text{ V} \pm 5\%$.

15-4 SCR Phase Control

Table 15-1 shows some commercially available SCRs. The gate trigger voltages vary from 0.8 to 2 V, and the gate trigger currents range from $200 \mu\text{A}$ to 50 mA. Also notice that anode currents vary from 1.5 to 70 A. Devices like these can control heavy industrial loads by using phase control.

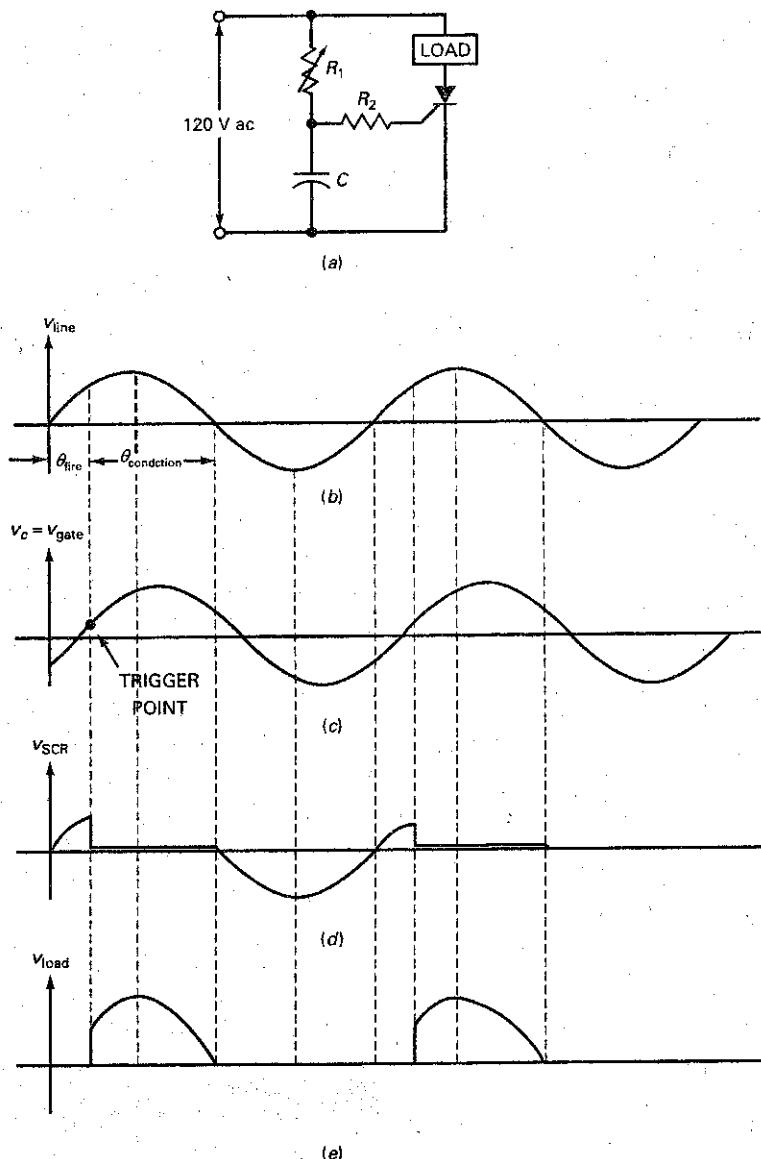
RC Circuit Controls Phase Angle

Figure 15-22a shows ac line voltage being applied to an SCR circuit that controls the current through a heavy load. In this circuit, variable resistor R_1 and capacitor

Table 15-1 SCR Sampler

Device	V_{GT}, V	I_{GT}	I_{\max}, A	V_{\max}, V
TCR22-2	0.8	$200 \mu\text{A}$	1.5	50
T106B1	0.8	$200 \mu\text{A}$	4	200
S4020L	1.5	15 mA	10	400
S6025L	1.5	39 mA	25	600
S1070W	2	50 mA	70	100

Figure 15-22 SCR phase control.



C shift the phase angle of the gate signal. When R_1 is zero, the gate voltage is in phase with the line voltage, and the SCR acts like a half-wave rectifier. R_2 limits the gate current to a safe level.

When R_1 increases, however, the ac gate voltage lags the line voltage by an angle between 0 and 90° , as shown in Figs. 15-22b and c. Before the trigger point shown in Fig. 15-22c, the SCR is off and the load current is zero. At the trigger point, the capacitor voltage is large enough to trigger the SCR. When this happens, almost all of the line voltage appears across the load and the load current becomes high. Ideally, the SCR remains latched until the line voltage reverses polarity. This is shown in Figs. 15-22c and d.

GOOD TO KNOW

In Fig. 15-22a, another *RC* phase-shifting network can be added to provide control from approximately 0 to 180°.

The angle at which the SCR fires is called the **firing angle**, shown as θ_{fire} in Fig. 15-22a. The angle between the start and end of conduction is called the **conduction angle**, shown as $\theta_{\text{conduction}}$. The *RC* phase controller of Fig. 15-22a can change the firing angle between 0 and 90°, which means that the conduction angle changes from 180 to 90°.

The shaded portions of Fig. 15-22b show when the SCR is conducting. Because R_1 is variable, the phase angle of the gate voltage can be changed. This allows us to control the shaded portions of the line voltage. Stated another way: We can control the average current through the load. This is useful for changing the speed of a motor, the brightness of a lamp, or the temperature of an induction furnace.

By using circuit analysis techniques studied in basic electricity courses, we can determine the approximate phase shifted voltage across the capacitor. This gives us the approximate firing angle and conduction angle of the circuit. To determine the voltage across the capacitor, use the following steps:

First, find the capacitive reactance of C by:

$$X_C = \frac{1}{2\pi f C}$$

The impedance and phase angle of the *RC* phase-shift circuit is:

$$Z_T = \sqrt{R^2 + X_C^2} \quad (15-4)$$

$$\theta_Z = \angle - \arctan \frac{X_C}{R} \quad (15-5)$$

Using the input voltage as our reference point, the current through C is:

$$I_C \angle \theta = \frac{V_{in} \angle 0^\circ}{Z_T \angle -\arctan \frac{X_C}{R}}$$

Now, the voltage value and phase of the capacitor can be found by:

$$V_C = (I_C \angle \theta)(X_C \angle -90^\circ)$$

The amount of delayed phase shift will be the approximate firing angle of the circuit. The conduction angle is found by subtracting the firing angle from 180°.

Example 15-7

 MultiSim

Using Fig. 15-22a, find the approximate firing angle and conduction angle when $R = 26 \text{ k}\Omega$.

SOLUTION The approximate firing angle can be found by solving for the voltage value and its phase shift across the capacitor. This is found by:

$$X_C = \frac{1}{2\pi f C} = \frac{1}{(2\pi)(60 \text{ Hz})(0.1 \mu\text{F})} = 26.5 \text{ k}\Omega$$

Because capacitive reactance is at an angle of -90° , $X_C = 26.5 \text{ k}\Omega \angle -90^\circ$. Next, find the total *RC* impedance Z_T and its angle by:

$$Z_T = \sqrt{R^2 + X_C^2} = \sqrt{(26 \text{ k}\Omega)^2 + (26.5 \text{ k}\Omega)^2} = 37.1 \text{ k}\Omega$$

$$\theta_Z = \angle - \arctan \frac{X_C}{R} = \angle - \arctan \frac{26.5 \text{ k}\Omega}{26 \text{ k}\Omega} = -45.5^\circ$$

Therefore, $Z_T = 37.1 \text{ k}\Omega \angle -45.5^\circ$.

Using the ac input as our reference, the current through C is:

$$I_C = \frac{V_{in} \angle 0^\circ}{Z_T \angle \theta} = \frac{120 \text{ V}_ac \angle 0^\circ}{37.1 \text{ k}\Omega \angle -45.5^\circ} = 3.23 \text{ mA} \angle 45.5^\circ$$

Now, the voltage across C can be found by:

$$V_C = (I_C \angle \theta)(X_C \angle -90^\circ) = (3.23 \text{ mA} \angle 45.5^\circ)(26.5 \text{ k}\Omega \angle -90^\circ)$$

$$V_C = 85.7 \text{ V}_ac \angle -44.5^\circ$$

With the voltage phase shift across the capacitor of -44.5° , the firing angle of the circuit is approximately -45.5° . After the SCR fires, it will remain on until its current drops below I_H . This will occur approximately when the ac input is zero volts.

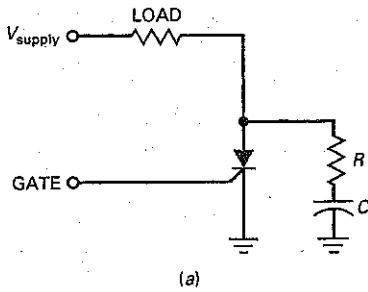
Therefore, the conduction angle is:

$$\text{conduction } \theta = 180^\circ - 44.5^\circ = 135.5^\circ$$

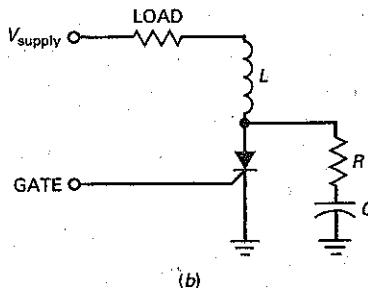
PRACTICE PROBLEM 15-7 Using Fig. 15-22a, find the approximate firing angle and conduction angle when $R = 50 \text{ k}\Omega$.

The *RC* phase controller of Fig. 15-22a is a basic way of controlling the average current through the load. The controllable range of current is limited because the phase angle can change from only 0 to 90° . With op amps and more sophisticated *RC* circuits, we can change the phase angle from 0 to 180° . This allows us to vary the average current all the way from zero to maximum.

Figure 15-23 (a) *RC* snubber protects SCR against rapid voltage rise; (b) inductor protects SCR against rapid current rise.



(a)



(b)

Critical Rate of Rise

When ac voltage is used to supply the anode of an SCR, it is possible to get false triggering. Because of capacitances inside an SCR, rapidly changing supply voltages may trigger the SCR. To avoid false triggering of an SCR, the rate of voltage change must not exceed the *critical rate of voltage rise* specified on the data sheet. For instance, the 2N6504 has a critical rate of voltage rise of $50 \text{ V}/\mu\text{s}$. To avoid false triggering, the anode voltage must not rise faster than $50 \text{ V}/\mu\text{s}$.

Switching transients are the main cause of exceeding the critical rate of voltage rise. One way to reduce the effects of switching transients is with an *RC snubber*, shown in Fig. 15-23a. If a high-speed switching transient does appear on the supply voltage, its rate of rise is reduced at the anode because of the *RC* time constant.

Large SCRs also have a *critical rate of current rise*. For instance, the C701 has a critical rate of current rise of $150 \text{ A}/\mu\text{s}$. If the anode current tries to rise faster than this, the SCR will be destroyed. Including an inductor in series with the load (Fig. 15-23b) reduces the rate of current rise to a safe level.

15-5 Bidirectional Thyristors

The two devices discussed so far, the four-layer diode and the SCR, are unidirectional because current can flow in only one direction. The **diac** and **triac** are *bidirectional thyristors*. These devices can conduct in either direction. The diac is sometimes called a *silicon bidirectional switch (SBS)*.

Diac

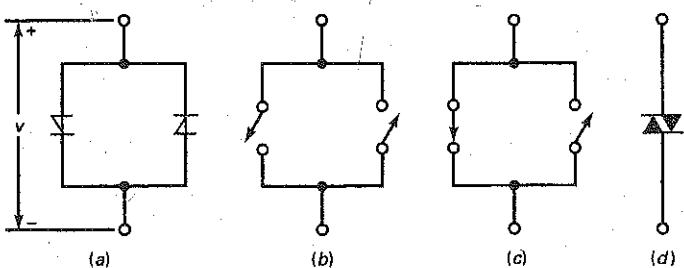
The diac can latch current in either direction. The equivalent circuit of a diac is two four-layer diodes in parallel, as shown in Fig. 15-24a, ideally the same as the latches in Fig. 15-24b. The diac is nonconducting until the voltage across it exceeds the breakdown voltage in either direction.

For instance, if v has the polarity indicated in Fig. 15-24a, the left diode conducts when v exceeds the breakdown voltage. In this case, the left latch closes, as shown in Fig. 15-24c. When v has the opposite polarity, the right latch closes. Figure 15-24d shows the schematic symbol for a diac.

Triac

The triac acts like two SCRs in reverse parallel (Fig. 15-25a), equivalent to the two latches of Fig. 15-25b. Because of this, the triac can control current in both directions. If v has the polarity shown in Fig. 15-25a, a positive trigger will close

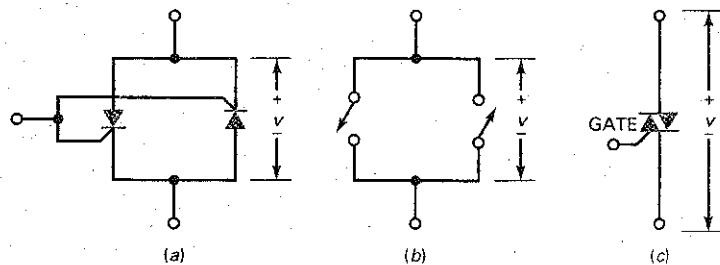
Figure 15-24 Diac.



GOOD TO KNOW

Triacs are often used in light dimmer controls.

Figure 15-25 Triac.



the left latch. When v has opposite polarity, a negative trigger will close the right latch. Figure 15-25c is the schematic symbol for a triac.

Fig. 15-26 shows the data sheet for a FKP8N80 triac. As the name triac implies, it is a bidirectional (ac) triode thyristor. Notice, at the end of the data sheet, the quadrant definitions or modes of triac operation. The triac normally operates in quadrants I and III during typical ac applications. Since this device is most sensitive in quadrant I, a diac is often used in conjunction with the triac to provide symmetrical ac conduction.

Table 15-2 shows some commercially available triacs. Because of their internal structure, triacs have higher gate trigger voltages and currents than comparable SCRs. As you can see, the gate trigger voltages of Table 15-2 are from 2 to 2.5 V and the gate trigger currents are from 10 to 50 mA. The maximum anode currents are from 1 to 15 A.

Phase Control

Figure 15-27a shows an RC circuit that varies the phase angle of the gate voltage to a triac. The circuit can control the current through a heavy load. Figure 15-27b and c shows the line voltage and lagging gate voltage. When the capacitor voltage is large enough to supply the trigger current, the triac conducts. Once on, the triac continues to conduct until the line voltage returns to zero. Figs. 15-27d and 15-27e show the respective voltages across the triac and the load.

Although triacs can handle large currents, they are not in the same class as SCRs, which have much higher current ratings. Nevertheless, when conduction on both half cycles is important, triacs are useful devices especially in industrial applications.

Table 15-2 Triac Sampler

Device	V_{GT} , V	I_{GT} , mA	I_{max} , A	V_{max} , V
Q201E3	2	10	1	200
Q4004L4	2.5	25	4	400
Q5010R5	2.5	50	10	500
Q6015R5	2.5	50	15	600

Figure 15-26 Triac data sheet.

FKPF8N80

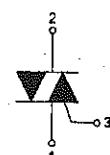
 FKPF8N80																																																													
Application Explanation <ul style="list-style-type: none"> • Switching mode power supply, light dimmer, electric flasher unit, hair drier • TV sets, stereo, refrigerator, washing machine • Electric blanket, solenoid driver, small motor control • Photo copier, electric tool 																																																													
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 1: T ₁ 2: T ₂ 3: Gate																																																													
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Figure 15-26 (continued)

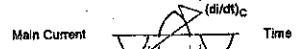
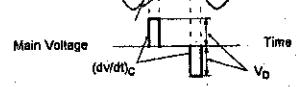
FKPF8N80

Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition			Min.	Typ.	Max.	Units
I_{DRM}	Repetitive Peak Off-State Current	V_{DRM} applied			-	-	20	μA
V_{TM}	On-State Voltage	$T_C=25^\circ\text{C}$, $I_{TM}=12\text{A}$ Instantaneous measurement			-	-	1.5	V
V_{GT}	Gate Trigger Voltage (Note 2)	I	$V_D=12\text{V}$, $R_L=20\Omega$	$T2(+)$, Gate (+)	-	-	1.5	V
		II		$T2(+)$, Gate (-)	-	-	1.5	V
		III		$T2(-)$, Gate (-)	-	-	1.5	V
I_{GR}	Gate Trigger Current (Note 2)	I	$V_D=12\text{V}$, $R_L=20\Omega$	$T2(+)$, Gate (+)	-	-	30	mA
		II		$T2(+)$, Gate (-)	-	-	30	mA
		III		$T2(-)$, Gate (-)	-	-	30	mA
V_{GD}	Gate Non-Trigger Voltage	$T_J=125^\circ\text{C}$, $V_D=1/2V_{DRM}$			0.2	-	-	V
I_H	Holding Current	$V_D = 12\text{V}$, $I_{TM} = 1\text{A}$					50	mA
I_L	Latching Current	I, III	$V_D = 12\text{V}$, $I_G = 1.2I_{GR}$				50	mA
		II					70	mA
dv/dt	Critical Rate of Rise of Off-State Voltage	V_{DRM} = Rated, $T_J = 125^\circ\text{C}$, Exponential Rise				300		$\text{V}/\mu\text{s}$
$(dv/dt)_C$	Critical Rate of Rise of Off-State Commutating Voltage (Note 3)				10	-	-	$\text{V}/\mu\text{s}$

Notes:

1. Gate Open
2. Measurement using the gate trigger characteristics measurement circuit
3. The critical-rate of rise of the off-state commutating voltage is shown in the table below
4. The contact thermal resistance $R_{TH(\text{C}-\text{J})}$ in case of greasing is $0.5^\circ\text{C}/\text{W}$

V_{DRM} (V)	Test Condition	Commutating voltage and current waveforms (Inductive load)	
FKPF8N80	1. Junction Temperature $T_J=125^\circ\text{C}$ 2. Rate of decay of on-state commutating current $(dv/dt)_C = -4.5\text{A}/\text{ms}$ 3. Peak off-state voltage $V_D = 400\text{V}$	  	

Quadrant Definitions for a Triac

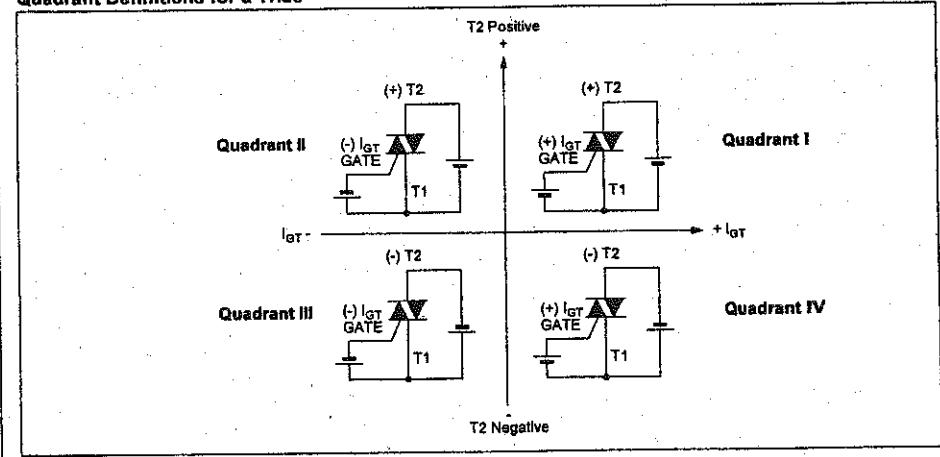


Figure 15-27 Triac phase control.

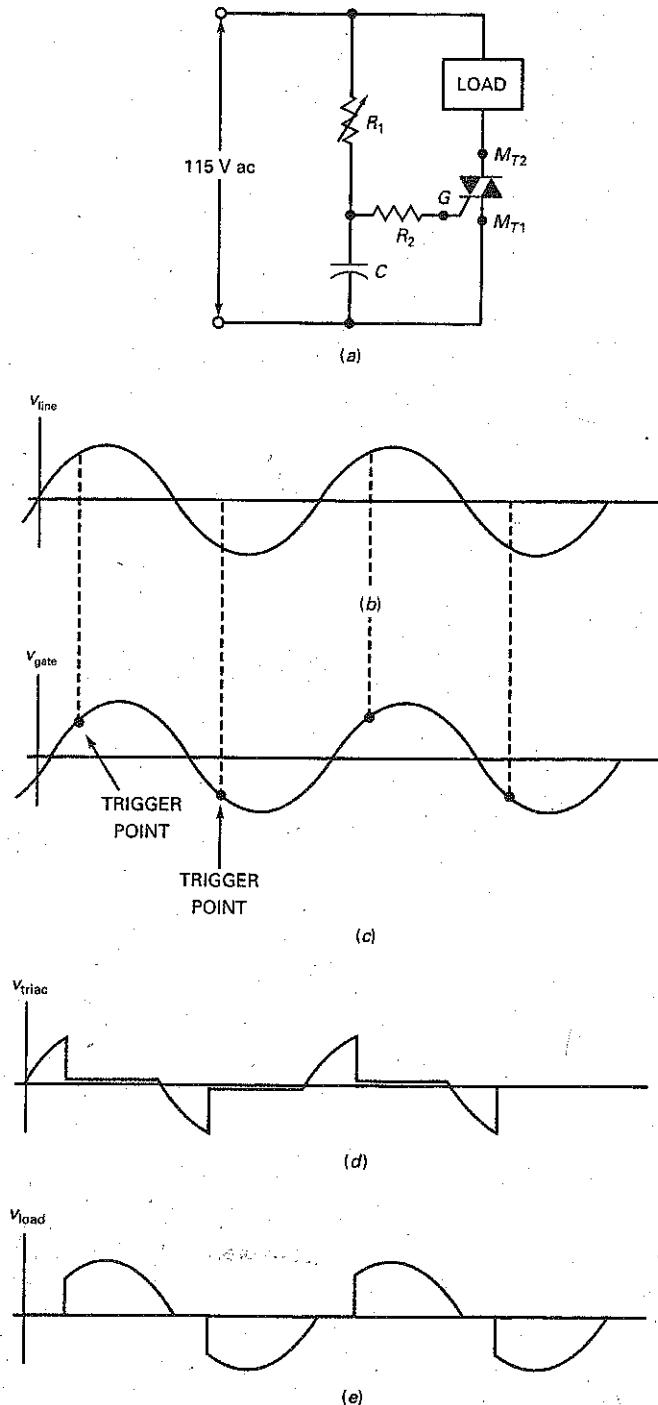
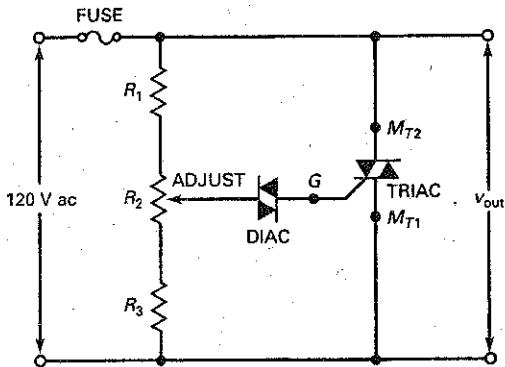


Figure 15-28 Triac crowbar.



GOOD TO KNOW

The diac in Fig. 15-28 is used to ensure that the triggering point is the same for both the positive and the negative alternations of the applied voltage.

Triac Crowbar

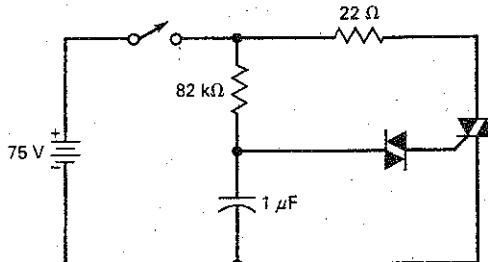
Figure 15-28 shows a triac crowbar that can be used to protect equipment against excessive line voltage. If the line voltage becomes too high, the diac breaks over and triggers the triac. When the triac fires, it blows the fuse. A potentiometer R_2 allows us to set the trigger point.

Example 15-8

III Multisim

In Fig. 15-29, the switch is closed. If the triac has fired, what is the approximate current through the $22\text{-}\Omega$ resistor?

Figure 15-29 Example.



SOLUTION Ideally, the triac has zero volts across it when conducting. Therefore, the current through the $22\text{-}\Omega$ resistor is:

$$I = \frac{75 \text{ V}}{22 \Omega} = 3.41 \text{ A}$$

If the triac has 1 or 2 V across it, the current is still close to 3.41 A because the large supply voltage swamps the effect of the triac on voltage.

PRACTICE PROBLEM 15-8 Using Fig. 15-29, change V_{in} to 120 V and calculate the approximate current through the $22\text{-}\Omega$ resistor.

Example 15-9

In Fig. 15-29, the switch is closed. The MPT32 is a diac with a breakdown voltage of 32 V. If the triac has a trigger voltage of 1 V and a trigger current of 10 mA, what is the capacitor voltage that triggers the triac?

SOLUTION As the capacitor charges, the voltage across the diac increases. When the diac voltage is slightly less than 32 V, the diac is on the verge of breakdown. Since the triac has a trigger voltage of 1 V, the capacitor voltage needs to be:

$$V_{in} = 32 \text{ V} + 1 \text{ V} = 33 \text{ V}$$

At this input voltage, the diac breaks over and triggers the triac.

PRACTICE PROBLEM 15-9 Repeat Example 15-9 using a diac with a 24 V breakdown value.

15-6 IGBTs

Basic Construction

Power MOSFETs and BJTs can both be used in high-power switching applications. The MOSFET has the advantage of greater switching speed, and the BJT has lower conduction losses. By combining the low conduction loss of a BJT with the switching speed of a power MOSFET, we can begin to approach an ideal switch.

This hybrid device exists and is called an **insulated-gate bipolar transistor (IGBT)**. The IGBT has essentially evolved from power MOSFET technology. Its structure and operation closely resembles a power MOSFET. Fig. 15-30 shows the basic structure of an *n*-channel IGBT. Its structure resembles an *n*-channel power MOSFET constructed on a *p*-type substrate. As shown, it has gate, emitter, and collector leads.

Figure 15-30 Basic IGBT structure.

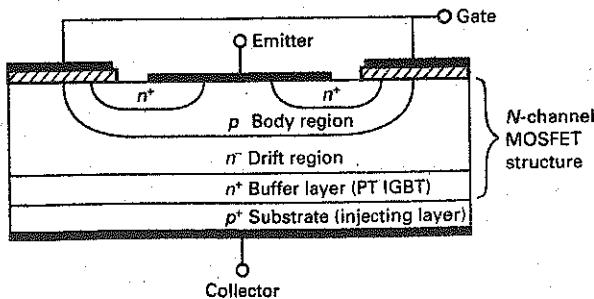
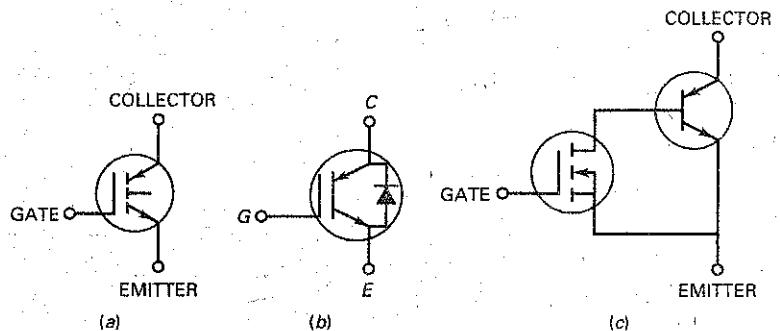


Figure 15-31 IGBTs: (a) and (b) Schematic symbols; (c) simplified equivalent circuit.



Two versions of this device are referred to as punch-through (PT) and nonpunch-through (NPT) IGBTs. Fig. 15-30 shows the structure of a PT IGBT. The PT IGBT has an n^+ buffer layer between its p^+ and n^- regions, and the NPT device has no n^+ buffer layer.

NPT versions have higher conduction $V_{CE(on)}$ values than PT versions and a positive temperature coefficient. The positive temperature coefficient makes the NPT suited for paralleling. PT versions, with the extra n^+ layer, have the advantage of higher switching speeds. They also have a negative temperature coefficient.

IGBT Control

Figures 15-31a and b show two common schematic symbols for an n -channel IGBT. Also, Fig. 15-31c shows a simplified equivalent circuit for this device. As you can see, the IGBT is essentially a power MOSFET on the input side and a BJT on the output side. The input control is a voltage between the gate and emitter leads. The output is a current between the collector and emitter leads.

The IGBT is a normally off high-input impedance device. When the input voltage, V_{GE} , is large enough, collector current will begin to flow. This minimum voltage value is the gate threshold voltage, $V_{GE(th)}$. Fig. 15-32 shows the data sheet for a FGL60N100BNTD IGBT using NPT-Trench technology. The typical $V_{GE(th)}$ for this device is listed as 5.0 V when $I_C = 60$ mA. The maximum continuous collector current is shown to be 60 A. Another important on characteristic is its collector to emitter saturation voltage, $V_{CE(sat)}$. The typical $V_{CE(sat)}$ value, shown on the data sheet, is 1.5 V at a collector current of 10 A and 2.5 V at a collector current of 60 A.

IGBT Advantages

Conduction losses of IGBTs are related to the forward voltage drop of the device, and the MOSFET conduction loss is based on its $R_{DS(on)}$ values. For low-voltage applications, power MOSFETs can have extremely low $R_{D(on)}$ resistances. In high-voltage applications, however, MOSFETs have increased $R_{DS(on)}$ values resulting in increased conduction losses. The IGBT does not have this characteristic. IGBTs also have a much higher collector-emitter breakdown voltage as compared to the V_{DSS} maximum value of MOSFETs. As shown in the data sheet of Fig. 15-32, the V_{CES} value is 1000 V. This is important in applications using higher-voltage inductive loads. As compared to BJTs, IGBTs have a much higher input impedance and have much simpler gate drive requirements. Although the IGBT cannot match the switching speed of the MOSFET, new IGBT families are being developed for high-frequency applications. IGBTs are, therefore, effective solutions for high-voltage and current applications at moderate frequencies.

Figure 15-32 IGBT data sheet.



FGL60N100BNTD

NPT-Trench IGBT

IGBT

FGL60N100BNTD

General Description

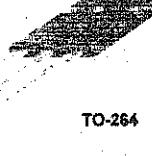
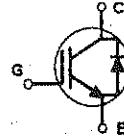
Trench insulated gate bipolar transistors (IGBTs) with NPT technology show outstanding performance in conduction and switching characteristics as well as enhanced avalanche ruggedness. These devices are well suited for Induction Heating (I-H) applications

Features

- High Speed Switching
- Low Saturation Voltage : $V_{CE(sat)} = 2.5 \text{ V}$ @ $I_C = 60\text{A}$
- High Input Impedance
- Built-in Fast Recovery Diode

Application

Micro-Wave Oven, I-H Cooker, I-H Jar, Induction Heater, Home Appliance

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Description	FGL60N100BNTD	Units
V_{CES}	Collector-Emitter Voltage	1000	V
V_{GES}	Gate-Emitter Voltage	± 25	V
I_C	Collector Current @ $T_C = 25^\circ\text{C}$	60	A
	Collector Current @ $T_C = 100^\circ\text{C}$	42	A
$I_{CM(1)}$	Pulsed Collector Current	120	A
I_F	Diode Continuous Forward Current @ $T_C = 100^\circ\text{C}$	15	A
P_D	Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$	180	W
	Maximum Power Dissipation @ $T_C = 100^\circ\text{C}$	72	W
T_J	Operating Junction Temperature	-55 to +150	$^\circ\text{C}$
$T_{Storage}$	Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temp. for soldering Purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Notes :

(1) Repetitive rating : Pulse width limited by max. junction temperature

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{SJC}(\text{IGBT})$	Thermal Resistance, Junction-to-Case	--	0.69	$^\circ\text{C}/\text{W}$
$R_{SJC}(\text{DIODE})$	Thermal Resistance, Junction-to-Case	--	2.08	$^\circ\text{C}/\text{W}$
R_{JA}	Thermal Resistance, Junction-to-Ambient	--	25	$^\circ\text{C}/\text{W}$

FGL60N100BNTD Rev. A

Figure 15-32 (continued)

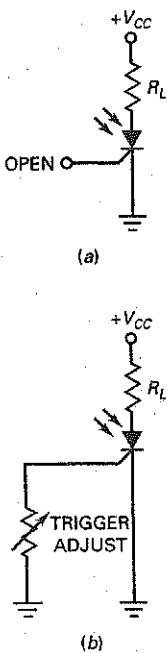
FGL60N100BNTD

Electrical Characteristics of IGBT

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{CES}	Collector Emitter Breakdown Voltage	$V_{GE} = 0\text{V}, I_C = 1\text{mA}$	1000	—	—	V
I_{CES}	Collector Cut-Off Current	$V_{CE} = 1000\text{V}, V_{GE} = 0\text{V}$	—	—	1.0	mA
I_{GES}	G-E Leakage Current	$V_{GE} = \pm 25, V_{CE} = 0\text{V}$	—	—	± 500	nA
On Characteristics						
$V_{GE(\text{th})}$	G-E Threshold Voltage	$I_C = 60\text{mA}, V_{CE} = V_{GE}$	4.0	5.0	7.0	V
$V_{CE(\text{sat})}$	Collector to Emitter Saturation Voltage	$I_C = 10\text{A}, V_{GE} = 15\text{V}$	—	1.5	1.8	V
		$I_C = 60\text{A}, V_{GE} = 15\text{V}$	—	2.5	2.9	V
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{CE}=10\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$	—	6000	—	pF
C_{oss}	Output Capacitance		—	260	—	pF
C_{res}	Reverse Transfer Capacitance		—	200	—	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{CC} = 600\text{V}, I_C = 60\text{A}, R_G = 51\Omega, V_{GE}=15\text{V}, \text{Resistive Load, } T_C = 25^\circ\text{C}$	—	140	—	ns
t_r	Rise Time		—	320	—	ns
$t_{d(off)}$	Turn-Off Delay Time		—	630	—	ns
t_f	Fall Time		—	130	250	ns
Q_g	Total Gate Charge	$V_{CE} = 600\text{V}, I_C = 60\text{A}, V_{GE} = 15\text{V}, T_C = 25^\circ\text{C}$	—	275	350	nC
Q_{ge}	Gate-Emitter Charge		—	45	—	nC
Q_{gc}	Gate-Collector Charge		—	95	—	nC
Electrical Characteristics of DIODE $T_C = 25^\circ\text{C}$ unless otherwise noted						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{FM}	Diode Forward Voltage	$I_F = 15\text{A}$	—	1.2	1.7	V
		$I_F = 60\text{A}$	—	1.8	2.1	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 60\text{A}, di/dt = 20\text{ A/us}$	—	1.2	1.5	us
I_R	Instantaneous Reverse Current	$V_{RRM} = 1000\text{V}$	—	0.05	2	uA

Figure 15-33 Photo-SCR.



15-7 Other Thyristors

SCRs, triacs, and IGBTs are important thyristors. But there are others worth looking at briefly. Some of these thyristors, like the photo-SCR, are still used in special applications. Others, like the UJT, were popular at one time but have been mostly replaced by op amps and timer ICs.

Photo-SCR

Figure 15-33a shows a *photo-SCR*, also known as a *light-activated SCR*. The arrows represent incoming light that passes through a window and hits the depletion layers. When the light is strong enough, valence electrons are dislodged from their orbits and become free electrons. The flow of free electrons starts the positive feedback, and the photo-SCR closes.

After a light trigger has closed the photo-SCR, it remains closed, even though the light disappears. For maximum sensitivity to light, the gate is left open, as shown in Fig. 15-33a. To get an adjustable trip point, we can include the trigger adjust shown in Fig. 15-33b. The resistance between the gate and ground diverts some of the light-produced electrons and reduces the sensitivity of the circuit to the incoming light.

Gate-Controlled Switch

As mentioned earlier, low-current drop-out is the normal way to open an SCR. But the *gate-controlled switch* is designed for easy opening with a reverse-biased trigger. A gate-controlled switch is closed by a positive trigger and opened by a negative trigger.

Figure 15-34 shows a gate-controlled circuit. Each positive trigger closes the gate-controlled switch, and each negative trigger opens it. Because of this, we get the square-wave output shown. The gate-controlled switch has been used in counters, digital circuits, and other applications in which a negative trigger is available.

Silicon Controlled Switch

Figure 15-35a shows the doped regions of a *silicon controlled switch*. Now an external lead is connected to each doped region. Visualize the device separated into two halves (Fig. 15-35b). Therefore, it's equivalent to a latch with access to both bases (Fig. 15-35c). A forward-bias trigger on either base will close the silicon controlled switch. Likewise, a reverse-bias trigger on either base will open the device.

Figure 15-34 Gate-controlled switch.

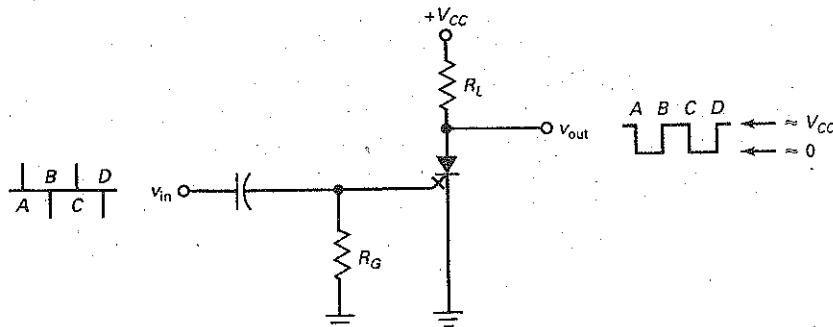


Figure 15-35 Silicon controlled switch.

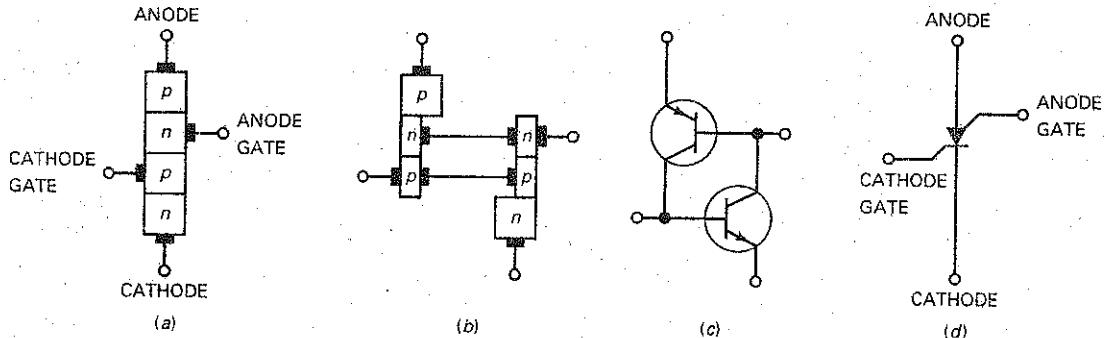


Figure 15-35d shows the schematic symbol for a silicon controlled switch. The lower gate is called the *cathode gate*, and the upper gate is the *anode gate*. The silicon controlled switch is a low-power device compared to the SCR. It handles currents in milliamperes rather than amperes.

Unijunction Transistor and PUT

The unijunction transistor (UJT) has two doped regions, as shown in Fig. 15-36a. When the input voltage is zero, the device is nonconducting. When we increase the input voltage above the *standoff voltage* (given on a data sheet), the resistance between the *p* region and the lower *n* region becomes very small, as shown in Fig. 15-36b. Figure 15-36c is the schematic symbol for a UJT.

The UJT can be used to form a pulse-generating circuit called a UJT relaxation oscillator, as shown in Fig. 15-37. In this circuit, the capacitor charges toward V_{BB} . When the capacitor voltage reaches a value equal to the standoff voltage, the UJT turns on. The internal lower base (lower *n* region) resistance quickly drops in value allowing the capacitor to discharge. The capacitor discharge continues until low-current dropout occurs. When this happens, the UJT turns off and the capacitor begins to once again charge toward V_{BB} . The charging RC time constant is normally significantly larger than the discharge time constant.

The sharp pulse waveform developed across the external resistor at B_1 can be used as a trigger source for controlling the conduction angle of SCR and triac circuits. The waveform developed across the capacitor can be used in applications where a sawtooth generator is needed.

The programmable unijunction transistor (PUT) is a four-layer *pnnp* device, which is used to produce trigger pulses and waveforms similar to UJT circuits. The schematic symbol is shown in Fig. 15-38a.

Figure 15-36 Unijunction transistor.

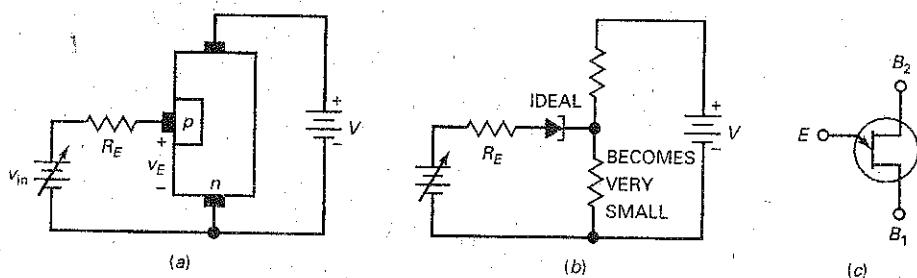


Figure 15-37 UJT relaxation oscillator.

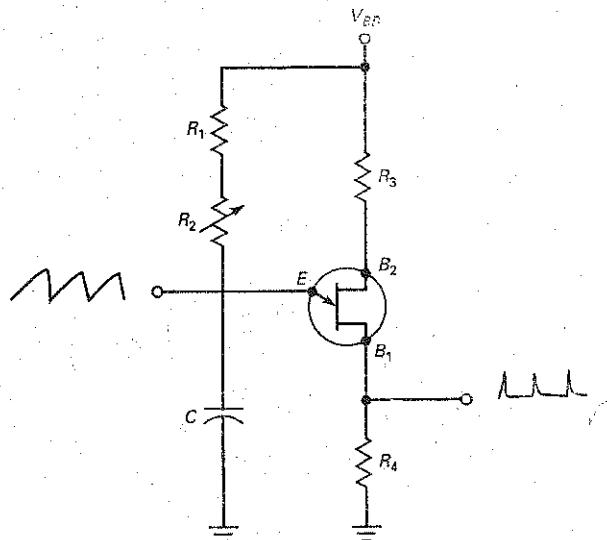
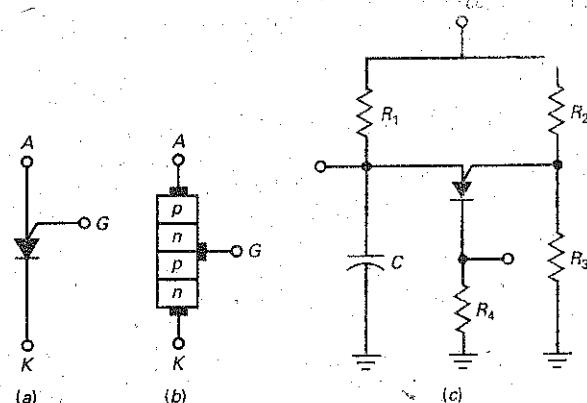


Figure 15-38 PUT: (a) symbol; (b) structure; (c) PUT circuit.



Its basic construction, shown in Fig. 15-38b, is very different from a UJT, more closely resembling an SCR. The gate lead is connected to the *n* layer next to the anode. This *pn* junction is used to control the on and off states of the device. The cathode terminal is connected to a voltage point lower than the gate, typically at a ground point. When the anode voltage becomes approximately 0.7 V higher than the gate voltage, the PUT turns on. The device will remain in the on state until its anode current falls below the rated holding current, normally given as its valley current, I_v . When this happens, the device returns to its off state.

The PUT is considered to be programmable because the gate voltage can be determined by an external voltage divider. This is shown in Fig. 15-38c. The

external resistors, R_2 and R_3 , establish the gate voltage, V_G . By changing these resistor values, the voltage on the gate can be modified or "programmed," thus changing the required anode voltage for firing. When the capacitor charges up through R_1 , it must reach a voltage value approximately 0.7 V higher than V_G . At that point, the PUT turns and the capacitor discharges. As with the UJT, sawtooth and trigger-pulse waveforms can be developed for controlling thyristors.

UJTs and PUTs were popular at one time for building oscillators, timers, and other circuits. But, as mentioned earlier, op amps and timer ICs (such as the 555), along with microcontrollers, have replaced these devices in many of their applications.

15-8 Troubleshooting

When you troubleshoot a circuit to find faulty resistors, diodes, transistors, and so on, you are troubleshooting at the *component level*. The troubleshooting problems of earlier chapters gave you troubleshooting practice at the component level. Troubleshooting at this level is an excellent foundation for troubleshooting at higher levels because it teaches you how to think logically, using Ohm's law as your guide.

Now, we want to practice troubleshooting at the *system level*. This means thinking in terms of *functional blocks*, which are the smaller jobs being done by the different parts of the overall circuit. To get the idea of this higher level of troubleshooting, look at the troubleshooting section at the end of this chapter (Fig. 15-48).

Here you see a block diagram of a power supply with an SCR crowbar. The power supply has been drawn in terms of its functional blocks. If you measure the voltages at the different points, you can often isolate the trouble to a particular block. Then you can continue troubleshooting at the component level, if necessary.

Often, a manufacturer's instruction manual includes block diagrams of the equipment in which the function of each block is specified. For instance, a television receiver can be drawn in terms of its functional blocks. Once you know what the input and output signals of each block are supposed to be, you can troubleshoot the television receiver to isolate the defective block. After you isolate the defective block, you can either replace the entire block or continue troubleshooting at the component level.

Summary

SEC. 15-1 THE FOUR-LAYER DIODE

A thyristor is a semiconductor device that uses internal positive feedback to produce latching action. The four-layer diode, also called a Shockley diode, is the simplest thyristor. Breakover closes it, and low-current drop-out opens it.

SEC. 15-2 THE SILICON CONTROLLED RECTIFIER

The silicon controlled rectifier (SCR) is the most widely used thyristor. It can switch very large currents on and off. To turn it on, we need to apply a minimum gate trigger voltage and current. To turn it off,

we need to reduce the anode voltage to almost zero.

SEC. 15-3 THE SCR CROWBAR

One important application of the SCR is to protect delicate and expensive loads against supply overvoltages. With an SCR crowbar, a fuse or current-limiting circuit

is needed to prevent excessive current from damaging the power supply.

SEC. 15-4 SCR PHASE CONTROL

An *RC* circuit can vary the lag angle of gate voltage from 0 to 90°. This allows us to control the average load current. By using more advanced phase control circuits, we can vary the phase angle from 0 to 180° and have greater control over the average load current.

SEC. 15-5 BIDIRECTIONAL THYRISTORS

The diac can latch current in either direction. It is open until the voltage across it exceeds the breakdown voltage. The triac is a gate-controlled device

similar to an SCR. With a phase controller, a triac gives us full-wave control of the average load current.

SEC. 15-6 IGBTs

The IGBT is a hybrid device composed of a power MOSFET on the input side and a BJT on the output side. This combination produces a device with simple input gate drive requirements and low conduction losses on the output. IGBTs have an advantage over power MOSFETs in high-voltage, high-current switching applications.

SEC. 15-7 OTHER THYRISTORS

The photo-SCR latches when the incoming light is strong enough. The

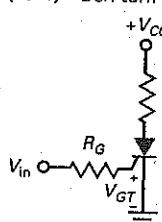
gate-controlled switch is designed to close with a positive trigger and open with a negative trigger. The silicon controlled switch has two input trigger gates, either of which can close or open the device. The unijunction transistor has been used to build oscillators and timing circuits.

SEC. 15-8 TROUBLESHOOTING

When you troubleshoot a circuit to find defective resistors, diodes, transistors, and so on, you are troubleshooting at the component level. When you are troubleshooting to find a defective functional block, you are troubleshooting at the system level.

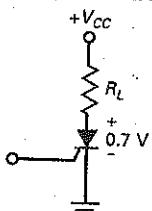
Derivations

(15-1) SCR turn-on:



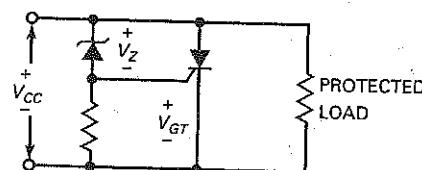
$$V_{in} = V_{GT} + I_{GT}R_G$$

(15-2) SCR reset:



$$V_{cc} = 0.7 \text{ V} + I_{HR}R_L$$

(15-3) Overvoltage:



$$V_{cc} = V_Z + V_{GT}$$

(15-4) RC phase control impedance:

$$Z_T = \sqrt{R^2 + X_C^2}$$

(15-5) RC phase control angle:

$$\theta_Z = -\arctan \frac{X_C}{R}$$

Student Assignments

1. A thyristor can be used as
 - a. A resistor
 - b. An amplifier
 - c. A switch
 - d. A power source
2. Positive feedback means that the returning signal
 - a. Opposes the original change
 - b. Aids the original change
 - c. Is equivalent to negative feedback
 - d. Is amplified
3. A latch always uses
 - a. Transistors
 - b. Negative feedback
 - c. Current
 - d. Positive feedback
4. To turn on a four-layer diode, you need
 - a. A positive trigger
 - b. Low-current drop-out
5. The minimum input current that can turn on a thyristor is called the
 - a. Holding current
 - b. Trigger current
 - c. Breakover current
 - d. Low-current drop-out

6. The only way to stop a four-layer diode that is conducting is by
 a. A positive trigger
 b. Low-current drop-out
 c. Breakover
 d. Reverse-bias triggering
7. The minimum anode current that keeps a thyristor turned on is called the
 a. Holding current
 b. Trigger current
 c. Breakover current
 d. Low-current drop-out
8. A silicon controlled rectifier has
 a. Two external leads
 b. Three external leads
 c. Four external leads
 d. Three doped regions
9. An SCR is usually turned on by
 a. Breakover
 b. A gate trigger
 c. Breakdown
 d. Holding current
10. SCRs are
 a. Low-power devices
 b. Four-layer diodes
 c. High-current devices
 d. Bidirectional
11. The usual way to protect a load from excessive supply voltage is with a
 a. Crowbar
 b. Zener diode
 c. Four-layer diode
 d. Thyristor
12. An RC snubber protects an SCR against
 a. Supply overvoltages
 b. False triggering
 c. Breakover
 d. Crowbarring
13. When a crowbar is used with a power supply, the supply needs to have a fuse or
 a. Adequate trigger current
 b. Holding current
 c. Filtering
 d. Current limiting
14. The photo-SCR responds to
 a. Current c. Humidity
 b. Voltage d. Light
15. The diac is a
 a. Transistor
 b. Unidirectional device
 c. Three-layer device
 d. Bidirectional device
16. The triac is equivalent to
 a. A four-layer diode
 b. Two diacs in parallel
 c. A thyristor with a gate lead
 d. Two SCRs in parallel
17. The unijunction transistor acts as a
 a. Four-layer diode c. Triac
 b. Diac d. Latch
18. Any thyristor can be turned on with
 a. Breakover
 b. Forward-bias triggering
 c. Low-current drop-out
 d. Reverse-bias triggering
19. A Schottky diode is the same as
 a. a four-layer diode c. a diac
 b. an SCR d. a triac
20. The trigger voltage of an SCR is closest to
 a. 0 c. 4 V
 b. 0.7 V d. Breakover voltage
21. Any thyristor can be turned off with
 a. Breakover
 b. Forward-bias triggering
 c. Low-current drop-out
 d. Reverse-bias triggering
22. Exceeding the critical rate of rise produces
 a. Excessive power dissipation
 b. False triggering
 c. Low-current drop-out
 d. Reverse-bias triggering
23. A four-layer diode is sometimes called a
 a. Unijunction transistor
 b. Diac
 c. *pnpn* diode
 d. Switch
24. A latch is based on
 a. Negative feedback
 b. Positive feedback
 c. The four-layer diode
 d. SCR action
25. An SCR can switch to the on state if
 a. Its forward breakover voltage is exceeded
 b. I_{GT} is applied
 c. The critical rate of voltage rise is exceeded
 d. All of the above
26. To properly test an SCR using an ohmmeter
 a. The ohmmeter must supply the SCR's breakdown voltage
 b. The ohmmeter cannot supply more than 0.7 V
 c. The ohmmeter must supply the SCR's reverse breakdown voltage
 d. The ohmmeter must supply the SCR's holding current
27. The maximum firing angle with a single RC phase control circuit is
 a. 45°
 b. 90°
 c. 180°
 d. 360°
28. A triac is generally considered most sensitive in
 a. Quadrant I
 b. Quadrant II
 c. Quadrant III
 d. Quadrant IV
29. An IGBT is essentially a
 a. BJT on the input and MOSFET on the output
 b. MOSFET on the input and MOSFET on the output
 c. MOSFET on the input and BJT on the output
 d. BJT on the input and BJT on the output
30. The maximum on-state output voltage of an IGBT is
 a. $V_{GS(on)}$
 b. $V_{CE(sat)}$
 c. $R_{DS(on)}$
 d. V_{CES}
31. A PUT is considered programmable by using
 a. External gate resistors
 b. Applying preset cathode voltage levels
 c. An external capacitor
 d. Doped *pn* junctions

Problems

SEC. 15-1 THE FOUR-LAYER DIODE

- 15-1 The 1N5160 of Fig. 15-39a is conducting. If we allow 0.7 V across the diode at the drop-out point, what is the value of V when the diode opens?
- 15-2 The capacitor of Fig. 15-39b charges from 0.7 to 12 V, causing the four-layer diode to break over. What is the current through the 5-k Ω resistor just before the diode breaks over? The current through the 5-k Ω resistor when diode is conducting?
- 15-3 What is the charging time constant in Fig. 15-39b? The period of the sawtooth equals the time constant. What does the frequency equal?
- 15-4 If the breakdown voltage of Fig. 15-39a changes to 20 V and the holding current changes to 3 mA, what is the voltage V that turns on the diode? What is the voltage that turns it off?
- 15-5 If the supply voltage is changed to 50 V in Fig. 15-39b, what is the maximum voltage across the capacitor? What is the time constant if the resistance is doubled and the capacitance is tripled?

Figure 15-39

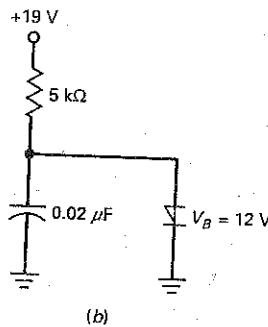
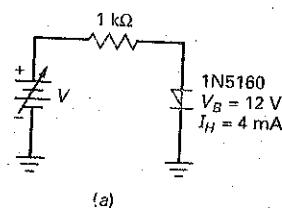


Figure 15-40

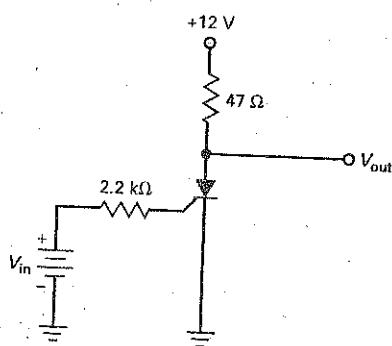
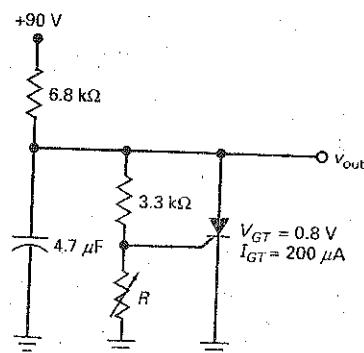
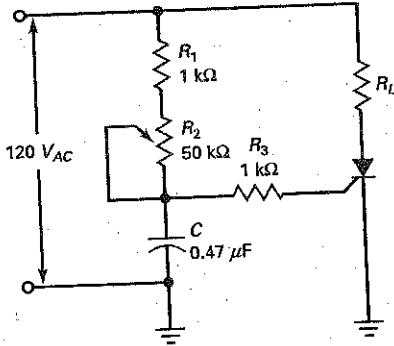


Figure 15-41



- 15-11 In Fig. 15-41, R is adjusted to $750\ \Omega$. What is the charging time constant for the capacitor? What is the Thevenin resistance facing the gate?
- 15-12 The resistor R_2 in Fig. 15-42 is set to $4.6\ k\Omega$. What are the approximate firing and conduction angles for this circuit? How much ac voltage is across C ?
- 15-13 Using Fig. 15-42, when adjusting R_2 , what are the minimum and maximum firing angle values?
- 15-14 What are the minimum and maximum conduction angles of the SCR in Fig. 15-42?

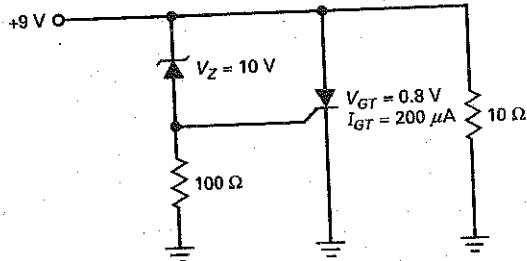
Figure 15-42



SEC. 15-3 THE SCR CROWBAR

- 15-15 Calculate the supply voltage that triggers the crowbar of Fig. 15-43.
- 15-16 If the zener diode of Fig. 15-43 has a tolerance of ± 10 percent and the trigger voltage can be as high as $1.5\ V$, what is the maximum supply voltage where crowbarring takes place?
- 15-17 If the zener voltage in Fig. 15-43 is changed from 10 to $12\ V$, what is the voltage that triggers the SCR?
- 15-18 The zener diode of Fig. 15-43 is replaced by a 1N759. What is the supply voltage that triggers the SCR crowbar?

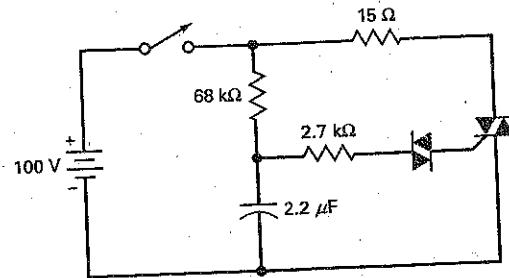
Figure 15-43



SEC. 15-5 BIDIRECTIONAL THYRISTORS

- 15-19 The diac of Fig. 15-44 has a breakdown voltage of $20\ V$, and the triac has a V_{GT} of $2.5\ V$. What is the capacitor voltage that turns on the triac?
- 15-20 What is the load current in Fig. 15-44 when the triac is conducting?
- 15-21 All resistances are doubled in Fig. 15-44, and the capacitance is tripled. If the diac has a breakdown voltage of $28\ V$ and the triac has a gate trigger voltage of $2.5\ V$, what is the capacitor voltage that fires the triac?

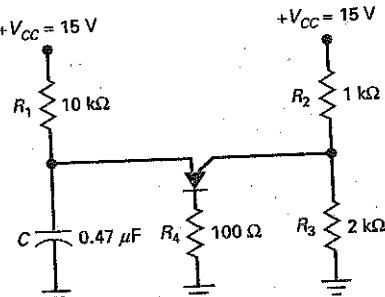
Figure 15-44



SEC. 15-7 OTHER THYRISTORS

- 15-22 In Fig. 15-45, what is the anode and gate voltage values when the PUT fires?
- 15-23 What will be the ideal peak voltage across R_4 in Fig. 15-45, when the PUT fires?
- 15-24 In Fig. 15-45, what will the voltage waveform across the capacitor look like? What will be the minimum and maximum voltage values of this waveform?

Figure 15-45



Critical Thinking

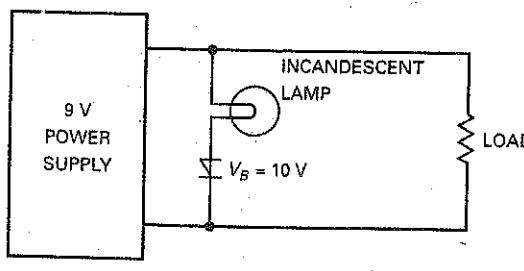
15-25 Figure 15-46a shows an overvoltage indicator. What is the voltage that turns on the lamp?

15-26 What is the peak output voltage in Fig. 15-46b?

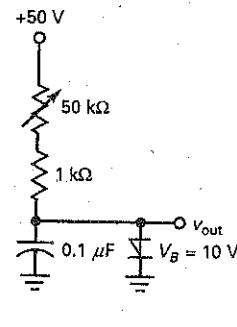
15-27 If the period of the sawtooth is 20 percent of the time constant, what is the minimum frequency in Fig. 15-46b? What is the maximum frequency?

15-28 The circuit of Fig. 15-47 is in a dark room. What is the output voltage? When a bright light is turned on, the thyristor fires. What is the approximate output voltage? What is the current through the $100\ \Omega$?

Figure 15-46

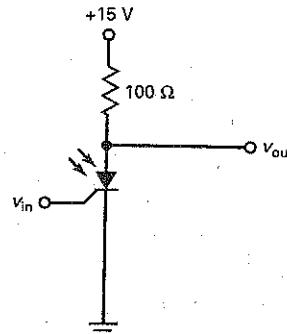


(a)



(b)

Figure 15-47



Troubleshooting

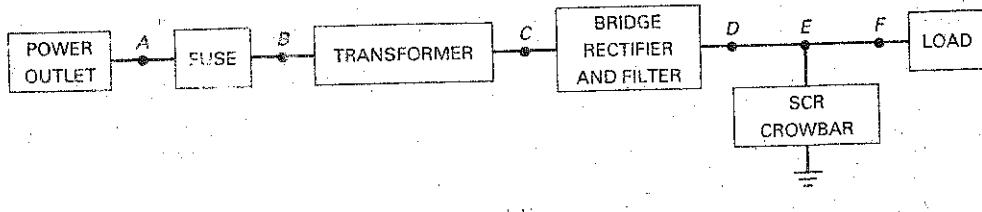
Use Fig. 15-48 for the remaining problems. This power supply has a bridge rectifier working into a capacitor-input filter. Therefore, the filtered dc voltage is approximately equal to the peak secondary voltage. All listed values are in volts, unless otherwise indicated. Also, the measured voltages at points A, B, and C are given as rms values. The measured voltages at points D, E, and F are given as dc voltages. In this

exercise, you are troubleshooting at the system level; that is, you are to locate the most suspicious block for further testing. For instance, if the voltage is OK at point B but incorrect at point C, your answer should be *transformer*.

15-29 Find Troubles 1 to 4.

15-30 Find Troubles 4 to 8.

Figure 15-48 Troubleshooting measurements.



(a)

Troubleshooting

Trouble	V_A	V_B	V_C	V_D	V_E	V_F	R_L	SCR
OK	115	115	12.7	18	18	18	$100\ \Omega$	Off
T1	115	115	12.7	18	0	0	$100\ \Omega$	Off
T2	0	0	0	0	0	0	$100\ \Omega$	Off
T3	115	115	0	0	0	0	$100\ \Omega$	Off
T4	115	0	0	0	0	0	0	Off
T5	130	130	14.4	20.5	20.5	20.5	$100\ \Omega$	Off
T6	115	115	12.7	0	0	0	$100\ \Omega$	Off
T7	115	115	12.7	18	18	0	$100\ \Omega$	Off
T8	115	0	0	0	0	0	$100\ \Omega$	Off

(b)

Job Interview Questions

- Draw a two-transistor latch. Then, explain how the positive feedback can drive the transistors into saturation and into cutoff.
- Draw a basic SCR crowbar. What is the theory of operation behind this circuit? In other words, tell me all the details of how it works.
- Draw a phase-controlled SCR circuit. Include the waveforms for ac line voltage and gate voltage. Then explain the theory of operation.
- In thyristor circuits, what is the purpose of snubber networks?
- How might one employ an SCR in an alarm circuit? Why would this device be preferable to one using a transistor trigger? Draw a simple schematic.
- Where in the field of electronics would a technician find thyristors in use?
- Compare a power BJT, a power FET, and an SCR for use in high-power amplification.
- Explain the differences in operation between the Shockley diode and an SCR.
- Compare a power MOSFET and an IGBT used for high-power switching.

Self-Test Answers

- | | | | | | | |
|------|-------|-------|-------|-------|-------|-------|
| 1. c | 6. b | 11. a | 16. d | 21. c | 26. d | 30. b |
| 2. b | 7. a | 12. b | 17. d | 22. b | 27. b | 31. a |
| 3. d | 8. b | 13. d | 18. a | 23. c | 28. a | |
| 4. c | 9. b | 14. d | 19. a | 24. b | 29. c | |
| 5. b | 10. c | 15. d | 20. b | 25. d | | |

Practice Problem Answers

15-1 $I_D = 113 \text{ mA}$

15-2 $V_{in} = 1.7 \text{ V}$

15-3 $F = 250 \text{ kHz}$

15-4 $V_{in} = 10 \text{ V}; V_{CC} = 2.5 \text{ V}$

15-6 $V_{CC} = 6.86 \text{ V} (\text{worst case})$

15-7 $\theta_{\text{firing}} = 62^\circ; \theta_{\text{conduction}} = 118^\circ$

15-8 $I_R = 5.45 \text{ A}$

15-9 $V_n = 25 \text{ V}$

16

Frequency Effects

- Earlier chapters discussed amplifiers operating in their normal frequency range. Now, we want to discuss how an amplifier responds when the input frequency is outside this normal range. With ac amplifiers, the voltage gain decreases when the input frequency is too low or too high. On the other hand, dc amplifiers have voltage gain all the way down to zero frequency. It is only at higher frequencies that the voltage gain of a dc amplifier falls off. We can use decibels to describe the decrease in voltage gain and a Bode plot to graph the response of an amplifier.

Chapter Outline

- 16-1 Frequency Response of an Amplifier
- 16-2 Decibel Power Gain
- 16-3 Decibel Voltage Gain
- 16-4 Impedance Matching
- 16-5 Decibels above a Reference
- 16-6 Bode Plots
- 16-7 More Bode Plots
- 16-8 The Miller Effect
- 16-9 Risetime-Bandwidth Relationship
- 16-10 Frequency Analysis of BJT Stages
- 16-11 Frequency Analysis of FET Stages
- 16-12 Frequency Effects of Surface-Mount Circuits

Objectives

After studying this chapter, you should be able to:

- Calculate decibel power gain and decibel voltage gain and state the implications of the impedance-matched condition.
- Sketch Bode plots for both magnitude and phase.
- Use Miller's theorem to calculate the equivalent input and output capacitances in a given circuit.
- Describe the risetime-bandwidth relationship.
- Explain how coupling capacitors and emitter-bypass capacitors produce the low-cutoff frequencies in BJT stages.
- Explain how the collector or drain-bypass capacitors and the input Miller capacitance produce the high-cutoff frequencies in BJT and FET stages.

Vocabulary

Bode plot	feedback capacitor	midband of an amplifier
cutoff frequencies	frequency response	Miller effect
dc amplifier	half-power frequencies	risetime T_R
decibel power gain	internal capacitances	stray-wiring capacitance
decibels	inverting amplifier	unity-gain frequency
decibel voltage gain	lag circuit	
dominant capacitor	logarithmic scale	

16-1 Frequency Response of an Amplifier

GOOD TO KNOW

The frequency response of an amplifier can be determined experimentally by applying a square-wave signal to the amplifier input and noting the output response. As you recall from earlier studies, a square wave contains a fundamental frequency and an infinite number of odd-order harmonics. The shape of the output square wave will reveal whether the low and high frequencies are being properly amplified. The frequency of the square wave should be approximately one-tenth the frequency of the upper cutoff frequency of the amplifier. If the output square wave is an exact replica of the input square wave, the frequency response of the amplifier is obviously sufficient for the applied frequency.

16-1 Frequency Response of an Amplifier

The **frequency response** of an amplifier is the graph of its gain versus the frequency. In this section, we will discuss the frequency response of ac and dc amplifiers. Earlier, we discussed a CE amplifier with coupling and bypass capacitors. This is an example of an *ac amplifier*, one designed to amplify ac signals. It is also possible to design a *dc amplifier*, one that can amplify dc signals as well as ac signals.

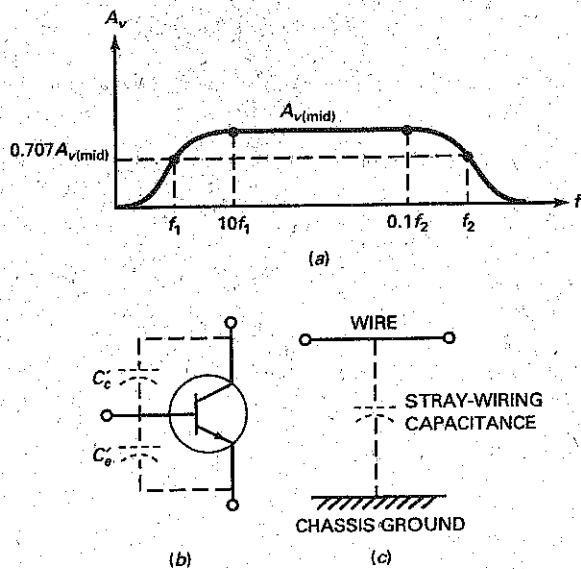
Response of an AC Amplifier

Figure 16-1a shows the *frequency response* of an ac amplifier. In the middle range of frequencies, the voltage gain is maximum. This middle range of frequencies is where the amplifier is normally operated. At low frequencies, the voltage gain decreases because the coupling and bypass capacitors no longer act like short circuits. Instead, their capacitive reactances are large enough to drop some of the ac signal voltage. The result is a loss of voltage gain as we approach zero hertz (0 Hz).

At high frequencies, the voltage gain decreases for other reasons. To begin with, a transistor has internal capacitances across its junctions, as shown in Fig. 16-1b. These capacitances provide bypass paths for the ac signal. As the frequency increases, the capacitive reactances become low enough to prevent normal transistor action. The result is a loss of voltage gain.

Stray-wiring capacitance is another reason for a loss of voltage gain at high frequencies. Figure 16-1c illustrates the idea. Any connecting wire in a transistor circuit acts like one plate of a capacitor, and the chassis ground acts like the other plate. The stray-wiring capacitance that exists between this wire and ground is unwanted. At higher frequencies, its low capacitive reactance prevents the ac current from reaching the load resistor. This is equivalent to saying that the voltage gain drops off.

Figure 16-1 (a) Frequency response of ac amplifier; (b) internal capacitance of transistor; (c) connecting wire forms capacitance with chassis.



Cutoff Frequencies

The frequencies at which the voltage gain equals 0.707 of its maximum value are called the **cutoff frequencies**. In Fig. 16-1a, f_1 is the lower cutoff frequency and f_2 is the upper cutoff frequency. The cutoff frequencies are also referred to as the **half-power frequencies** because the load power is half of its maximum value at these frequencies.

Why is the output power half of maximum at the cutoff frequencies? When the voltage gain is 0.707 of the maximum value, the output voltage is 0.707 of the maximum value. Recall that power equals the square of voltage divided by resistance. When you square 0.707, you get 0.5. This is why the load power is half of its maximum value at the cutoff frequencies.

Midband

We will define the **midband of an amplifier** as the band of frequencies between $10f_1$ and $0.1f_2$. In the midband, the voltage gain of the amplifier is approximately maximum, designated by $A_{v(mid)}$. Three important characteristics of any ac amplifier are its $A_{v(mid)}$, f_1 , and f_2 . Given these values, we know how much voltage gain there is in the midband and where the voltage gain is down to $0.707A_{v(mid)}$.

Outside the Midband

Although an amplifier normally operates in the midband, there are times when we want to know what the voltage gain is outside of the midband. Here is an approximation for calculating the voltage gain of an ac amplifier:

$$A_v = \frac{A_{v(mid)}}{\sqrt{1 + (f_1/f)^2} \sqrt{1 + (f/f_2)^2}} \quad (16-1)$$

Given $A_{v(mid)}$, f_1 , and f_2 , we can calculate the voltage gain at any frequency f . This equation assumes that one dominant capacitor is producing the lower cutoff frequency, and one dominant capacitor is producing the upper cutoff frequency. A **dominant capacitor** is one that is more important than all others in determining the cutoff frequency.

Equation (16-1) is not as formidable as it first appears. There are only three frequency ranges to analyze: the midband, below midband, and above midband. In the midband, $f_1/f \approx 0$ and $f/f_2 \approx 0$. Therefore, both radicals in Eq. (16-1) are approximately 1, and Eq. (16-1) simplifies to:

$$\text{Midband: } A_v = A_{v(mid)} \quad (16-2)$$

Below the midband, $f/f_2 \approx 0$. As a result, the second radical equals 1 and Eq. (16-1) simplifies to:

$$\text{Below midband: } A_v = \frac{A_{v(mid)}}{\sqrt{1 + (f_1/f)^2}} \quad (16-3)$$

Above midband, $f_1/f \approx 0$. As a result, the first radical equals 1 and Eq. (16-1) simplifies to:

$$\text{Above midband: } A_v = \frac{A_{v(mid)}}{\sqrt{1 + (f/f_2)^2}} \quad (16-4)$$

Response of a DC Amplifier

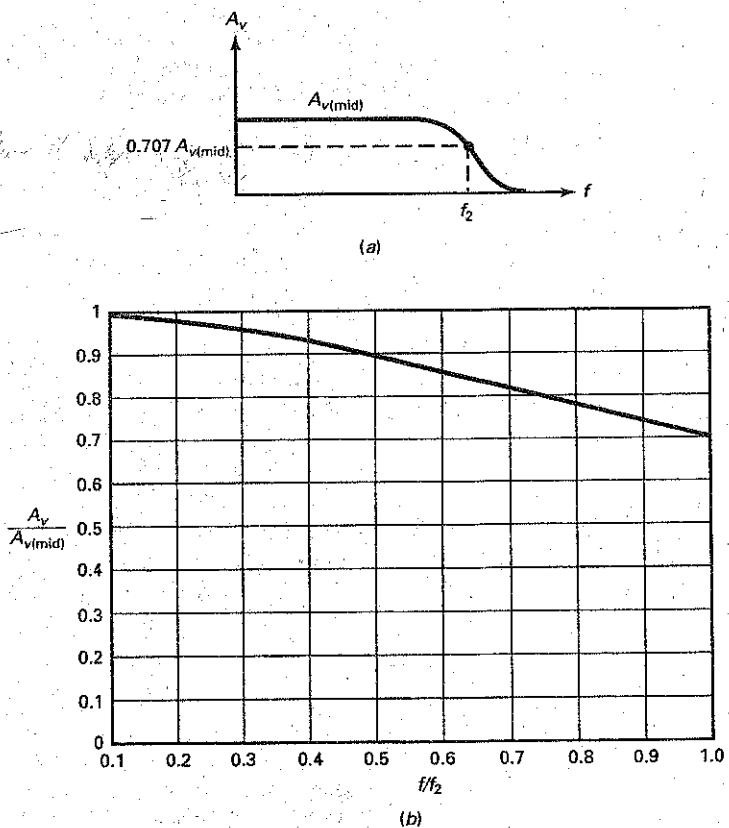
As mentioned in Chap. 12, a designer can use direct coupling between amplifier stages. This allows the circuit to amplify all the way down to zero hertz (0 Hz). This type of amplifier is called a **dc amplifier**.

Figure 16-2a shows the frequency response of a dc amplifier. Since there is no lower cutoff frequency, the two important characteristics of a dc amplifier

GOOD TO KNOW

In Fig. 16-2, the bandwidth includes the frequencies from 0 Hz up to f_2 . To say it another way, the bandwidth in Fig. 16-2 equals f_2 .

Figure 16-2 Frequency response of dc amplifier.



are $A_{v(\text{mid})}$ and f_2 . Given these two values on a data sheet, we have the voltage gain of the amplifier in the midband and its upper cutoff frequency.

The dc amplifier is more widely used than the ac amplifier because most amplifiers are now being designed with op amps instead of with discrete transistors. An *op amp* is a dc amplifier that has high voltage gain, high input impedance, and low output impedance. A wide variety of op amps are commercially available as integrated circuits (ICs).

Most dc amplifiers are designed with one dominant capacitance that produces the cutoff frequency f_2 . Because of this, we can use the following formula to calculate the voltage gain of typical dc amplifiers:

$$A_v = \frac{A_{v(\text{mid})}}{\sqrt{1 + (f/f_2)^2}} \quad (16-5)$$

For instance, when $f = 0.1f_2$:

$$A_v = \frac{A_{v(\text{mid})}}{\sqrt{1 + (0.1)^2}} = 0.995 A_{v(\text{mid})}$$

This says that the voltage gain is within a half percent of maximum when the input frequency is one-tenth of the upper cutoff frequency. In other words, the voltage gain is approximately 100 percent of maximum.

Table 16-1 Between Midband and Cutoff

f/f_2	$A_v/A_{v(\text{mid})}$	Percent (approx.)
0.1	0.995	100
0.2	0.981	98
0.3	0.958	96
0.4	0.928	93
0.5	0.894	89
0.6	0.857	86
0.7	0.819	82
0.8	0.781	78
0.9	0.743	74
1	0.707	70

Between Midband and Cutoff

With Eq. (16-5), we can calculate the voltage gain in the region between midband and cutoff. Table 16-1 shows the normalized values of frequency and voltage gain. When $f/f_2 = 0.1$, $A_v/A_{v(\text{mid})} = 0.995$. When f/f_2 increases, the normalized voltage gain decreases until it reaches 0.707 at the cutoff frequency. As an approximation, we can say that the voltage gain is 100 percent of maximum when $f/f_2 = 0.1$. Then, it decreases to 98 percent, 96 percent, and so on, until it is approximately 70 percent at the cutoff frequency. Figure 16-2b shows the graph of $A_v/A_{v(\text{mid})}$ versus f/f_2 .

Example 16-1

Figure 16-3a shows an ac amplifier with a midband voltage gain of 200. If the cutoff frequencies are $f_1 = 20 \text{ Hz}$ and $f_2 = 20 \text{ kHz}$, what does the frequency response look like? What is the voltage gain if the input frequency is 5 Hz? If it is 200 kHz?

SOLUTION In the midband, the voltage gain is 200. At either cutoff frequency, it equals:

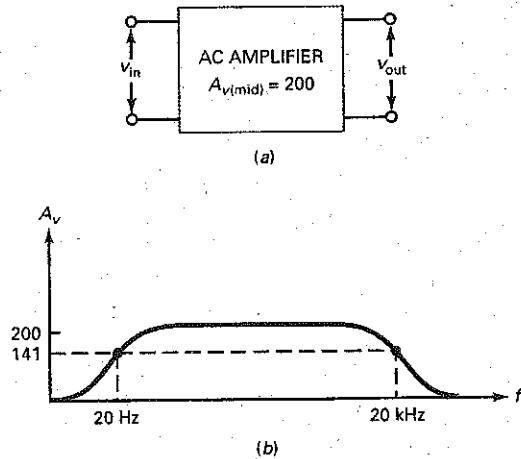
$$A_v = 0.707(200) = 141$$

Figure 16-3b shows the frequency response.

With Eq. (16-3), we can calculate the voltage gain for an input frequency of 5 Hz:

$$A_v = \frac{200}{\sqrt{1 + (20/5)^2}} = \frac{200}{\sqrt{1 + (4)^2}} = \frac{200}{\sqrt{17}} = 48.5$$

Figure 16-3 AC amplifier and its frequency response.



In a similar way, we can use Eq. (16-4) to calculate the voltage gain for an input frequency of 200 kHz:

$$A_v = \frac{200}{\sqrt{1 + (200/20)^2}} = 19.9$$

PRACTICE PROBLEM 16-1 Repeat Example 16-1 using an ac amplifier with a midband voltage gain of 100.

Example 16-2

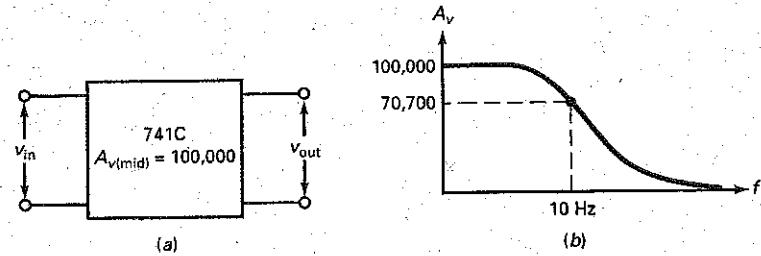
Figure 16-4a shows a 741C, an op amp with a midband voltage gain of 100,000. If $f_2 = 10$ Hz, what does the frequency response look like?

SOLUTION At the cutoff frequency of 10 Hz, the voltage gain is 0.707 of its midband value:

$$A_v = 0.707(100,000) = 70,700$$

Figure 16-4b shows the frequency response. Notice that the voltage gain is 100,000 at a frequency of zero hertz (0 Hz). As the input frequency approaches

Figure 16-4 The 741C and its frequency response.



10 Hz, the voltage gain decreases until it equals approximately 70 percent of maximum.

PRACTICE PROBLEM 16-2 Repeat Example 16-2 with $A_{v(\text{mid})} = 200,000$.

Example 16-3

In the preceding example, what is the voltage gain for each of the following input frequencies: 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz?

SOLUTION Since the cutoff frequency is 10 Hz, an input frequency of:

$$f = 100 \text{ Hz, } 1 \text{ kHz, } 10 \text{ kHz, } \dots$$

gives a ratio f/f_2 of:

$$f/f_2 = 10, 100, 1000, \dots$$

Therefore, we can use Eq. (16-5) as follows to calculate the voltage gains:

$$f = 100 \text{ Hz: } A_v = \frac{100,000}{\sqrt{1 + (10)^2}} \approx 10,000$$

$$f = 1 \text{ kHz: } A_v = \frac{100,000}{\sqrt{1 + (100)^2}} = 1000$$

$$f = 10 \text{ kHz: } A_v = \frac{100,000}{\sqrt{1 + (1000)^2}} = 100$$

$$f = 100 \text{ kHz: } A_v = \frac{100,000}{\sqrt{1 + (10,000)^2}} = 10$$

$$f = 1 \text{ MHz: } A_v = \frac{100,000}{\sqrt{1 + (100,000)^2}} = 1$$

Each time the frequency increases by a *decade* (a factor of 10), the voltage gain decreases by a factor of 10.

PRACTICE PROBLEM 16-3 Repeat Example 16-3 with $A_{v(\text{mid})} = 200,000$.

16-2 Decibel Power Gain

We are about to discuss decibels, a useful method for describing frequency response. But before we do, we need to review some ideas from basic mathematics.

Review of Logarithms

Suppose we are given this equation:

$$x = 10^y \quad (16-6)$$

This equation can be solved for y in terms of x to get:

$$y = \log_{10} x$$

This says that y is the logarithm (or exponent) of 10 that gives x . Usually, the 10 is omitted, and the equation is written as:

$$y = \log x \quad (16-7)$$

With a calculator that has the common log function, you can quickly find the y value for any x value. For instance, here is how to calculate the value of y for $x = 10, 100$, and 1000 :

$$y = \log 10 = 1$$

$$y = \log 100 = 2$$

$$y = \log 1000 = 3$$

As you can see, each time x increases by a factor of 10, y increases by 1.

You can also calculate y values, given decimal values of x . For instance, here are the values of y for $x = 0.1, 0.01$, and 0.001 :

$$y = \log 0.1 = -1$$

$$y = \log 0.01 = -2$$

$$y = \log 0.001 = -3$$

Each time x decreases by a factor of 10, y decreases by 1.

Definition of $A_{p(\text{dB})}$

In Chap. 12, power gain A_p was defined as the output power divided by the input power:

$$A_p = \frac{P_{\text{out}}}{P_{\text{in}}}$$

Decibel power gain is defined as:

$$A_{p(\text{dB})} = 10 \log A_p \quad (16-8)$$

Since A_p is the ratio of output power to input power, A_p has no units or dimensions. When you take the logarithm of A_p , you get a quantity that has no units or dimensions. But to make sure that $A_{p(\text{dB})}$ is never confused with A_p , we attach the unit *decibel* (abbreviated *dB*) to all answers for $A_{p(\text{dB})}$.

For instance, if an amplifier has a power gain of 100, it has a decibel power gain of:

$$A_{p(\text{dB})} = 10 \log 100 = 20 \text{ dB}$$

As another example, if $A_p = 100,000,000$, then:

$$A_{p(\text{dB})} = 10 \log 100,000,000 = 80 \text{ dB}$$

In both of these examples, the log equals the number of zeros: 100 has two zeros, and 100,000,000 has eight zeros. You can use the zero count to find the logarithm whenever the number is a multiple of 10. Then, you can multiply by 10 to get the decibel answer. For instance, a power gain of 1000 has three zeros; multiply by 10 to get 30 dB. A power gain of 100,000 has five zeros; multiply by 10 to get 50 dB. This shortcut is useful for finding decibel equivalents and checking answers.

Decibel power gain is often used on data sheets to specify the power gain of devices. One reason for using decibel power gain is that logarithms compress numbers. For instance, if an amplifier has a power gain that varies from 100 to 100,000,000, the decibel power gain varies from 20 to 80 dB. As you can see, decibel power gain is a more compact notation than ordinary power gain.

Table 16-2 Properties of Power Gain

Factor	Decibel, dB
$\times 2$	+3
$\times 0.5$	-3
$\times 10$	+10
$\times 0.1$	-10

Two Useful Properties

Decibel power gain has two useful properties:

1. Each time the ordinary power gain increases (decreases) by a factor of 2, the decibel power gain increases (decreases) by 3 dB.
2. Each time the ordinary power gain increases (decreases) by a factor of 10, the decibel power gain increases (decreases) by 10 dB.

Table 16-2 shows these properties in compact form. The following examples will demonstrate these properties.

Example 16-4

Calculate the decibel power gain for the following values: $A_p = 1, 2, 4$, and 8 .

SOLUTION With a calculator, we get the following answers:

$$A_{p(\text{dB})} = 10 \log 1 = 0 \text{ dB}$$

$$A_{p(\text{dB})} = 10 \log 2 = 3 \text{ dB}$$

$$A_{p(\text{dB})} = 10 \log 4 = 6 \text{ dB}$$

$$A_{p(\text{dB})} = 10 \log 8 = 9 \text{ dB}$$

Each time A_p increases by a factor of 2, the decibel power gain increases by 3 dB. This property is always true. Whenever you double the power gain, the decibel power gain increases by 3 dB.

PRACTICE PROBLEM 16-4 Find $A_{p(\text{dB})}$ for power gains of 10, 20, and 40.

Example 16-5

Calculate the decibel power gain for each of these values: $A_p = 1, 0.5, 0.25$, and 0.125 .

SOLUTION

$$A_{p(\text{dB})} = 10 \log 1 = 0 \text{ dB}$$

$$A_{p(\text{dB})} = 10 \log 0.5 = -3 \text{ dB}$$

$$A_{p(\text{dB})} = 10 \log 0.25 = -6 \text{ dB}$$

$$A_{p(\text{dB})} = 10 \log 0.125 = -9 \text{ dB}$$

Each time A_p decreases by a factor of 2, the decibel power gain decreases by 3 dB.

PRACTICE PROBLEM 16-5 Repeat Example 16-5 for power gains of 4, 2, 1, and 0.5.

Example 16-6

Calculate the decibel power gain for the following values: $A_p = 1, 10, 100$, and 1000.

SOLUTION

$$A_{p(\text{dB})} = 10 \log 1 = 0 \text{ dB}$$

$$A_{p(\text{dB})} = 10 \log 10 = 10 \text{ dB}$$

$$A_{p(\text{dB})} = 10 \log 100 = 20 \text{ dB}$$

$$A_{p(\text{dB})} = 10 \log 1000 = 30 \text{ dB}$$

Each time A_p increases by a factor of 10, the decibel power gain increases by 10 dB.

PRACTICE PROBLEM 16-6 Calculate the decibel power gain for A_p values of 5, 50, 500, and 5000.

Example 16-7

Calculate the decibel power gain for each of these values: $A_p = 1, 0.1, 0.01$, and 0.001.

SOLUTION

$$A_{p(\text{dB})} = 10 \log 1 = 0 \text{ dB}$$

$$A_{p(\text{dB})} = 10 \log 0.1 = -10 \text{ dB}$$

$$A_{p(\text{dB})} = 10 \log 0.01 = -20 \text{ dB}$$

$$A_{p(\text{dB})} = 10 \log 0.001 = -30 \text{ dB}$$

Each time the A_p decreases by a factor of 10, the decibel power gain decreases by 10 dB.

PRACTICE PROBLEM 16-7 Calculate the decibel power gain for A_p values of 20, 2, 0.2, 0.02.

16-3. Decibel Voltage Gain

Voltage measurements are more common than power measurements. For this reason, decibels are even more useful with voltage gain.

Definition

As defined in earlier chapters, voltage gain is the output voltage divided by the input voltage:

$$A_v = \frac{V_{\text{out}}}{V_{\text{in}}}$$

Decibel voltage gain is defined as:

$$A_{v(\text{dB})} = 20 \log A_v \quad (16-9)$$

The reason for using 20 instead of 10 in this definition is because power is proportional to the square of voltage. As will be discussed in the next section, this definition produces an important derivation for impedance-matched systems.

If an amplifier has a voltage gain of 100,000, it has a decibel voltage gain of:

$$A_{v(\text{dB})} = 20 \log 100,000 = 100 \text{ dB}$$

We can use a shortcut whenever the number is a multiple of 10. Count the number of zeros and multiply by 20 to get the decibel equivalent. In the foregoing calculation, count five zeros and multiply by 20 to get the decibel voltage gain of 100 dB.

As another example, if an amplifier has a voltage gain that varies from 100 to 100,000,000, then its decibel voltage gain varies from 40 to 160 dB.

Basic Rules for Voltage Gain

Here are the useful properties for decibel voltage gain:

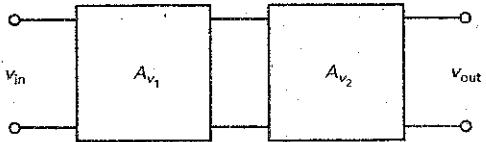
1. Each time the voltage gain increases (decreases) by a factor of 2, the decibel voltage gain increases (decreases) by 6 dB.
2. Each time the voltage gain increases (decreases) by a factor of 10, the decibel voltage gain increases (decreases) by 20 dB.

Table 16-3 summarizes these properties.

Table 16-3 Properties of Voltage Gain

Factor	Decibel, dB
×2	+6
×0.5	-6
×10	+20
×0.1	-20

Figure 16-5 Two stages of voltage gain.



Cascaded Stages

In Fig. 16-5, the total voltage gain of the two-stage amplifier is the product of the individual voltage gains:

$$A_v = (A_{v_1})(A_{v_2}) \quad (16-10)$$

For instance, if the first stage has a voltage gain of 100 and the second stage has a voltage gain of 50, the total voltage gain is:

$$A_v = (100)(50) = 5000$$

Something unusual happens in Eq. (16-10) when we use the decibel voltage gain instead of the ordinary voltage gain:

$$A_{v(\text{dB})} = 20 \log A_v = 20 \log (A_{v_1}(A_{v_2})) = 20 \log A_{v_1} + 20 \log A_{v_2}$$

This can be written as:

$$A_{v(\text{dB})} = A_{v_1(\text{dB})} + A_{v_2(\text{dB})} \quad (16-11)$$

This equation says that the total decibel voltage gain of two cascaded stages equals the sum of the individual decibel voltage gains. The same idea applies to any number of stages. This additive property of decibel gain is one reason for its popularity.

Example 16-8

What is the total voltage gain in Fig. 16-6a? Express this in decibels. Next, calculate the decibel voltage gain of each stage and the total decibel voltage gain using Eq. (16-11).

SOLUTION With Eq. (16-10), the total voltage gain is:

$$A_v = (100)(200) = 20,000$$

In decibels, this is:

$$A_{v(\text{dB})} = 20 \log 20,000 = 86 \text{ dB}$$

You can use a calculator to get 86 dB, or you can use the following shortcut: The number 20,000 is the same as 2 times 10,000. The number 10,000 has four zeros, which means that the decibel equivalent is 80 dB. Because of the factor of 2, the final answer is 6 dB higher, or 86 dB.

Next, we can calculate the decibel voltage gain of each stage as follows:

$$A_{v_1(\text{dB})} = 20 \log 100 = 40 \text{ dB}$$

$$A_{v_2(\text{dB})} = 20 \log 200 = 46 \text{ dB}$$

Figure 16-6 Voltage gains and decibel equivalents.

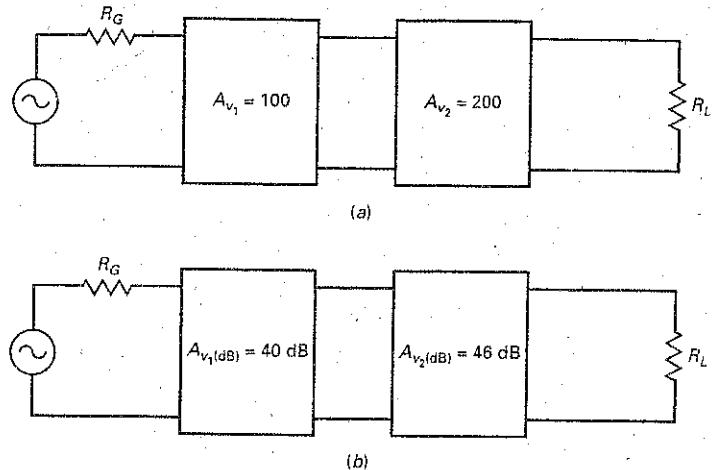


Figure 16-6b shows these decibel voltage gains. With Eq. (16-11), the total decibel voltage gain is:

$$A_{v(\text{dB})} = 40 \text{ dB} + 46 \text{ dB} = 86 \text{ dB}$$

As you can see, adding the decibel voltage gain of each stage gives us the same answer calculated earlier.

PRACTICE PROBLEM 16-8 Repeat Example 16-8 with stage voltage gains of 50 and 200.

GOOD TO KNOW

When the impedances are not matched in an amplifier, the decibel power gains can be calculated with the use of the following equation:

$$A_{p(\text{dB})} = 20 \log A_v + 10 \log R_{in}/R_{out}$$

where A_v represents the voltage gain of the amplifier, and R_{in} and R_{out} represent the input and output resistances respectively.

16-4 Impedance Matching

Figure 16-7a shows an amplifier stage with a generator resistance of R_G , an input resistance of R_{in} , an output resistance of R_{out} , and a load resistance of R_L . Up to now, most of our discussions have used different impedances.

In many communication systems (microwave, television, and telephone), all impedances are matched; that is, $R_G = R_{in} = R_{out} = R_L$. Figure 16-7b illustrates the idea. As indicated, all impedances equal R . The impedance R is 50 Ω in microwave systems, 75 Ω (coaxial cable) or 300 Ω (twin-lead) in television systems, and 600 Ω in telephone systems. Impedance matching is used in these systems because it produces maximum power transfer.

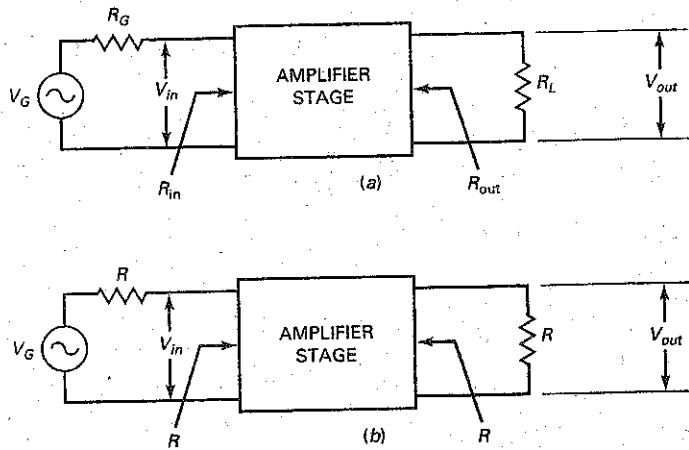
In Fig. 16-7b, the input power is:

$$P_{in} = \frac{V_{in}^2}{R}$$

and the output power is:

$$P_{out} = \frac{V_{out}^2}{R}$$

Figure 16-7 Impedance matching.



The power gain is:

$$A_p = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{V_{\text{out}}^2/R}{V_{\text{in}}^2/R} = \frac{V_{\text{out}}^2}{V_{\text{in}}^2} = \left(\frac{V_{\text{out}}}{V_{\text{in}}}\right)^2$$

or

$$A_p = A_v^2 \quad (16-12)$$

This says that the power gain equals the square of the voltage gain in any impedance-matched system.

In terms of decibels:

$$A_{p(\text{dB})} = 10 \log A_p = 10 \log A_v^2 = 20 \log A_v$$

or

$$A_{p(\text{dB})} = A_{v(\text{dB})} \quad (16-13)$$

This says that the decibel power gain equals the decibel voltage gain. Equation (16-13) is true for any impedance-matched system. If a data sheet states that the gain of a system is 40 dB, then both decibel power gain and voltage gain equal 40 dB.

Converting Decibel to Ordinary Gain

When a data sheet specifies the decibel power gain or voltage gain, you can convert the decibel gain to ordinary gain with the following equations:

$$A_p = \text{antilog } \frac{A_{p(\text{dB})}}{10} \quad (16-14)$$

and

$$A_v = \text{antilog } \frac{A_{v(\text{dB})}}{20} \quad (16-15)$$

The antilog is the inverse logarithm. These conversions are easily done on a scientific calculator that has a log function and an inverse key.

Example 16-9

Figure 16-8 shows impedance-matched stages with $R = 50 \Omega$. What is the total decibel gain? What is the total power gain? The total voltage gain?

SOLUTION The total decibel voltage gain is:

$$A_{v(\text{dB})} = 23 \text{ dB} + 36 \text{ dB} + 31 \text{ dB} = 90 \text{ dB}$$

The total decibel power gain also equals 90 dB because the stages are impedance-matched.

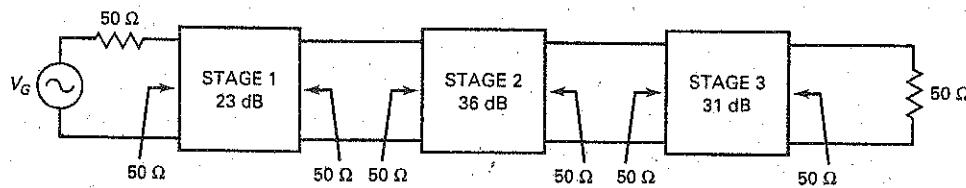
With Eq. (16-14), the total power gain is:

$$A_p = \text{antilog } \frac{90 \text{ dB}}{10} = 1,000,000,000$$

and the total voltage gain is:

$$A_v = \text{antilog } \frac{90 \text{ dB}}{20} = 31,623$$

Figure 16-8 Impedance matching in a 50- Ω system.



PRACTICE PROBLEM 16-9 Repeat Example 16-9 with stage gains of 10 dB, -6 dB, and 26 dB.

Example 16-10

In the preceding example, what is the ordinary voltage gain of each stage?

SOLUTION The first stage has a voltage gain of:

$$A_{v_1} = \text{antilog } \frac{23 \text{ dB}}{20} = 14.1$$

The second stage has a voltage gain of:

$$A_{v_2} = \text{antilog } \frac{36 \text{ dB}}{20} = 63.1$$

The third stage has a voltage gain of:

$$A_{v_3} = \text{antilog } \frac{31 \text{ dB}}{20} = 35.5$$

PRACTICE PROBLEM 16-10 Repeat Example 16-10 with stage gains of 10 dB, -6 dB, and 26 dB.

16-5 Decibels above a Reference

In this section, we will discuss two more ways to use decibels. Besides applying decibels to power and voltage gains, we can use *decibels above a reference*. The reference levels used in this section are the milliwatt and the volt.

The Milliwatt Reference

Decibels are sometimes used to indicate the power level above 1 mW. In this case, the label *dBm* is used instead of dB. The *m* at the end of dBm reminds us of the milliwatt reference. The dBm equation is:

$$P_{\text{dBm}} = 10 \log \frac{P}{1 \text{ mW}} \quad (16-16)$$

where P_{dBm} is the power expressed in dBm. For instance, if the power is 2 W, then:

$$P_{\text{dBm}} = 10 \log \frac{2 \text{ W}}{1 \text{ mW}} = 10 \log 2000 = 33 \text{ dBm}$$

Using dBm is a way of comparing the power to 1 mW. If a data sheet says that the output of a power amplifier is 33 dBm, it is saying that the output power is 2 W. Table 16-4 shows some dBm values.

You can convert any dBm value to its equivalent power by using this equation:

$$P = \text{antilog} \frac{P_{\text{dBm}}}{10} \quad (16-17)$$

where P is the power in milliwatts.

The Volt Reference

Decibels can also be used to indicate the voltage level above 1 V. In this case, the label *dBV* is used. The dBV equation is:

$$V_{\text{dBV}} = 20 \log \frac{V}{1 \text{ V}}$$

Table 16-4 | Power in dBm

Power	P_{dBm}
1 μW	-30
10 μW	-20
100 μW	-10
1 mW	0
10 mW	10
100 mW	20
1 W	30



GOOD TO KNOW

Audio communication systems that have input and output resistances of 600Ω use the dBm unit to indicate the actual power output of an amplifier, an attenuator, or an entire system.

GOOD TO KNOW

The unit decibel millivolt (dBmV) is frequently used in cable television systems for the measurement of signal intensity. In this system, a signal of 1 mV across $75\ \Omega$ is the reference level that corresponds to 0 dB. The dBmV unit is used to indicate the actual output voltage of an amplifier, attenuator, or an entire system.

Table 16-5 Voltage in dBV

Voltage	V _{dBV}
10 μV	-100
100 μV	-80
1 mV	-60
10 mV	-40
100 mV	-20
1 V	0
10 V	+20
100 V	+40

Since the denominator equals 1, we can simplify the equation to:

$$V_{dBV} = 20 \log V \quad (16-18)$$

where V is dimensionless. For instance, if the voltage is 25 V, then:

$$V_{dBV} = 20 \log 25 = 28 \text{ dBV}$$

Using dBV is a way of comparing the voltage to 1 V. If a data sheet says that the output of a voltage amplifier is 28 dBV, it is saying that the output voltage is 25 V. If the output level or sensitivity of a microphone is specified as -40 dBV, its output voltage is 10 mV. Table 16-5 shows some dBV values.

You can convert any dBV value to its equivalent voltage using this equation:

$$V = \text{antilog } \frac{V_{dBV}}{20} \quad (16-19)$$

where V is the voltage in volts.

Example 16-11

A data sheet says that the output of an amplifier is 24 dBm. What is the output power?

SOLUTION With a calculator and Eq. (16-17):

$$P = \text{antilog } \frac{24 \text{ dBm}}{10} = 251 \text{ mW}$$

PRACTICE PROBLEM 16-11 What is the power output of an amplifier rated at 50 dBm?

Example 16-12

If a data sheet says that the output of an amplifier is -34 dBV , what is the output voltage?

SOLUTION With Eq. (16-18):

$$V = \text{antilog} \frac{-34 \text{ dBV}}{20} = 20 \text{ mV}$$

PRACTICE PROBLEM 16-12 Given a microphone rating of -54.5 dBV , what is the output voltage?

16-6 Bode Plots

Figure 16-9 shows the frequency response of an ac amplifier. Although it contains some information such as the midband voltage gain and the cutoff frequencies, it is an incomplete picture of the amplifier's behavior. This is where the **Bode plot** comes in. Because this type of graph uses decibels, it can give us more information about the amplifier's response outside the midband.

Octaves

The middle C on a piano has a frequency of 256 Hz. The next-higher C is an octave higher, and it has a frequency of 512 Hz. The next-higher C has a frequency of 1024 Hz, and so on. In music, the word *octave* refers to a doubling of the frequency. Every time you go up one octave, you have doubled the frequency.

In electronics, an octave has a similar meaning for ratios like f_1/f and f/f_2 . For instance, if $f_1 = 100 \text{ Hz}$ and $f = 50 \text{ Hz}$, the f_1/f ratio is:

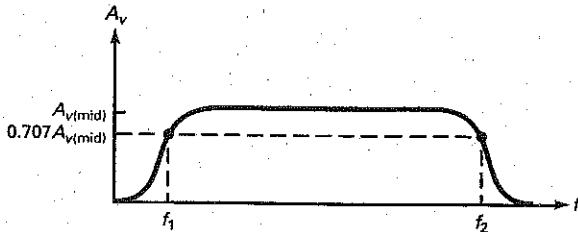
$$\frac{f_1}{f} = \frac{100 \text{ Hz}}{50 \text{ Hz}} = 2$$

We can describe this by saying that f is one octave below f_1 . As another example, suppose $f = 400 \text{ kHz}$ and $f_2 = 200 \text{ kHz}$. Then:

$$\frac{f}{f_2} = \frac{400 \text{ kHz}}{200 \text{ kHz}} = 2$$

This means that f is one octave above f_2 .

Figure 16-9 Frequency response of an ac amplifier.



Decades

A *decade* has a similar meaning for ratios like f_1/f and f/f_2 , except that a factor of 10 is used instead of a factor of 2. For instance, if $f_1 = 500$ Hz and $f = 50$ Hz, the f_1/f ratio is

$$\frac{f_1}{f} = \frac{500 \text{ Hz}}{50 \text{ Hz}} = 10$$

We can describe this by saying that f is one decade below f_1 . As another example, suppose $f = 2$ MHz and $f_2 = 200$ kHz. Then:

$$\frac{f}{f_2} = \frac{2 \text{ MHz}}{200 \text{ kHz}} = 10$$

This means that f is one decade above f_2 .

Linear and Logarithmic Scales

Ordinary graph paper has a *linear scale* on both axes. This means that the spaces between the numbers are the same for all numbers, as shown in Fig. 16-10a. With a linear scale, you start at 0 and proceed in uniform steps toward higher numbers. All the graphs discussed up to now have used linear scales.

Sometimes we may prefer to use a *logarithmic scale* because it compresses very large values and allows us to see over many decades. Figure 16-10b shows a logarithmic scale. Notice that the numbering begins with 1. The space between 1 and 2 is much larger than the space between 9 and 10. By compressing the scale logarithmically as shown here, we can take advantage of certain properties of logarithms and decibels.

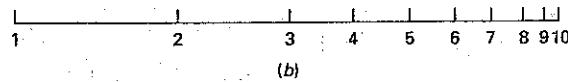
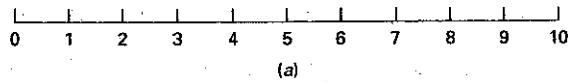
Both ordinary graph paper and semilogarithmic paper are available. Semilogarithmic graph paper has a linear scale on the vertical axis and a logarithmic scale on the horizontal axis. People use semilogarithmic paper when they want to graph a quantity like voltage gain over many decades of frequency.

Graph of Decibel Voltage Gain

Figure 16-11a shows the frequency response of a typical ac amplifier. The graph is similar to Fig. 16-9, but this time we are looking at the decibel voltage gain versus frequency as it would appear on semilogarithmic paper. A graph like this is called a *Bode plot*. The vertical axis uses a linear scale, and the horizontal axis uses a logarithmic scale.

As shown, the decibel voltage gain is maximum in the midband. At each cutoff frequency, the decibel voltage gain is down slightly from the maximum value. Below f_1 , the decibel voltage gain decreases 20 dB per decade. Above f_2 , the decibel voltage gain decreases 20 dB per decade. Decreases of 20 dB per decade occur in an amplifier where there is one dominant capacitor producing the lower cutoff frequency and one dominant bypass capacitor producing the upper cutoff frequency, as discussed in Sec. 16-1.

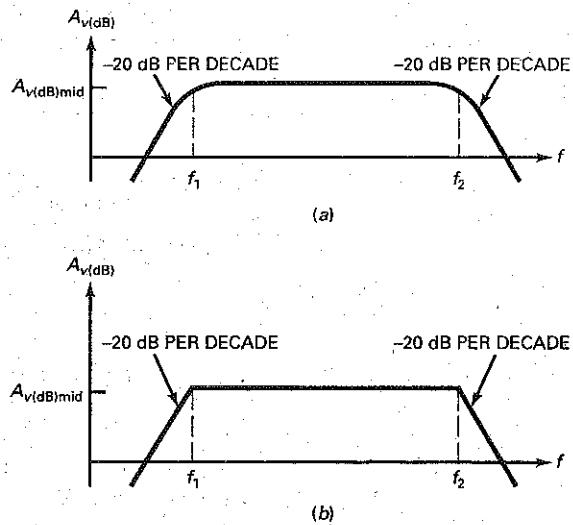
Figure 16-10 Linear and logarithmic scales.



GOOD TO KNOW

The main advantage of using logarithmic spacing is that a larger range of values can be shown in one plot without losing resolution in the smaller values.

Figure 16-11 (a) Bode plot; (b) ideal Bode plot.



At the cutoff frequencies, f_1 and f_2 , the voltage gain is 0.707 of the midband value. In terms of decibels:

$$A_V(\text{dB}) = 20 \log 0.707 = -3 \text{ dB}$$

We can describe the frequency response of Fig. 16-11a in this way: In the midband, the voltage gain is maximum. Between the midband and each cutoff frequency, the voltage gain gradually decreases until it is down 3 dB at the cutoff frequency. Then, the voltage gain rolls off (decreases) at a rate of 20 dB per decade.

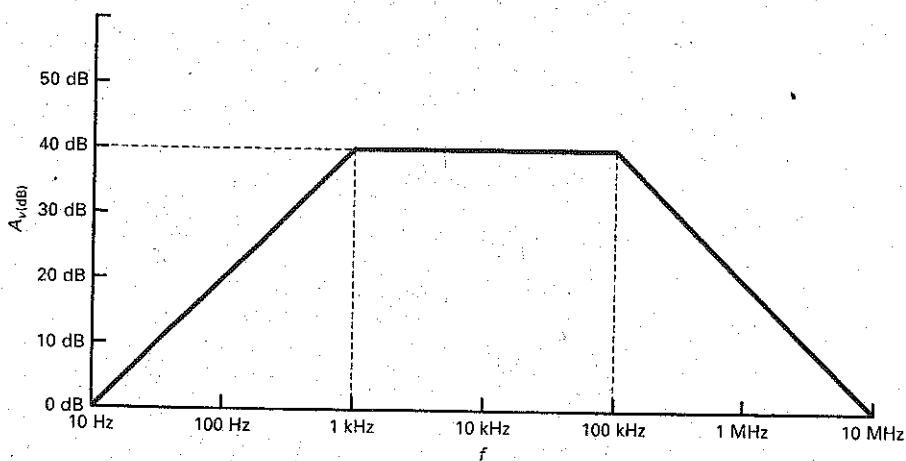
Ideal Bode Plot

Figure 16-11b shows the frequency response in *ideal* form. Many people prefer using the ideal Bode plot because it is easy to draw and gives approximately the same information. Anyone looking at this ideal graph knows that the decibel voltage gain is down 3 dB at the cutoff frequencies. The ideal Bode plot contains all the original information when this correction of 3 dB is mentally included.

Ideal Bode plots are approximations that allow us to draw the frequency response of an amplifier quickly and easily. They let us concentrate on the main issues rather than being caught in the details of exact calculations. For instance, an ideal Bode plot like Fig. 16-12 gives us a quick visual summary of an amplifier's frequency response. We can see the midband voltage gain (40 dB), the cutoff frequencies (1 kHz and 100 kHz), and roll-off rate (20 dB per decade). Also notice that the voltage gain equals 0 dB (unity or 1) at $f = 10 \text{ Hz}$ and $f = 10 \text{ MHz}$. Ideal graphs like these are very popular in industry.

Incidentally, many technicians and engineers use the term *corner frequency* instead of *cutoff frequency*. This is because the ideal Bode plot has a sharp corner at each cutoff frequency. Another term often used is *break frequency*. This is because the graph breaks at each cutoff frequency and then decreases at a rate of 20 dB per decade.

Figure 16-12 Ideal Bode plot of an ac amplifier.



Example 16-13

The data sheet for a 741C op amp gives a midband voltage gain of 100,000, a cutoff frequency of 10 Hz, and roll-off rate of 20 dB per decade. Draw the ideal Bode plot. What is the ordinary voltage gain at 1 MHz?

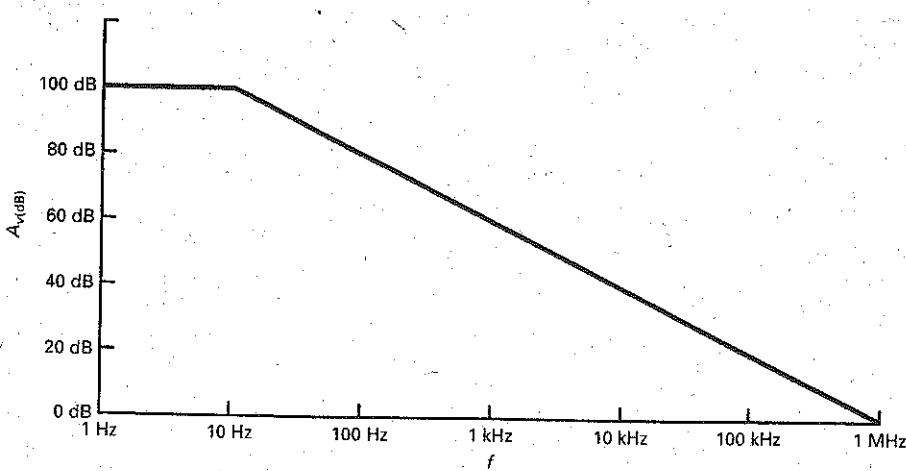
SOLUTION As mentioned in Sec. 16-1, op amps are dc amplifiers, so they have only an upper cutoff frequency. For a 741C, $f_2 = 10 \text{ Hz}$. The midband voltage gain in decibels is:

$$A_{v(\text{dB})} = 20 \log 100,000 = 100 \text{ dB}$$

The ideal Bode plot has a midband voltage gain of 100 dB up to 10 Hz. Then, it decreases 20 dB per decade.

Figure 16-13 shows the ideal Bode plot. After breaking at 10 Hz, the response rolls off 20 dB per decade until it equals 0 dB at 1 MHz. The ordinary voltage is unity (1) at this frequency. Data sheets often list the **unity-gain frequency** (symbolized f_{unity}) because it immediately tells you the frequency limitation of the op amp. The device can provide voltage gain up to unity-gain frequency but not beyond it.

Figure 16-13 Ideal Bode plot of a dc amplifier.



16-7 More Bode Plots

Ideal Bode plots are useful approximations for preliminary analysis. But sometimes, we need more accurate answers. For instance, the voltage gain of an op amp gradually decreases between the midband and the cutoff frequency. Let us look at this transition region more closely.

Between Midband and Cutoff

In Sec. 16-1, we introduced the following equation for the voltage gain of an amplifier above midband:

$$A_v = \frac{A_{v(\text{mid})}}{\sqrt{1 + (f/f_2)^2}} \quad (16-20)$$

With this equation, we can calculate the voltage gain in the transition region between midband and cutoff. For instance, here are the calculations for $f/f_2 = 0.1$, 0.2, and 0.3:

$$A_v = \frac{A_{v(\text{mid})}}{\sqrt{1 + (0.1)^2}} = 0.995 A_{v(\text{mid})}$$

$$A_v = \frac{A_{v(\text{mid})}}{\sqrt{1 + (0.2)^2}} = 0.981 A_{v(\text{mid})}$$

$$A_v = \frac{A_{v(\text{mid})}}{\sqrt{1 + (0.3)^2}} = 0.958 A_{v(\text{mid})}$$

Continuing like this, we can calculate the remaining values shown in Table 16-6.

Table 16-6 includes the dB values for $A_v/A_{v(\text{mid})}$. The decibel entries are calculated as follows:

$$(A_v/A_{v(\text{mid})})_{\text{dB}} = 20 \log 0.995 = -0.04 \text{ dB}$$

$$(A_v/A_{v(\text{mid})})_{\text{dB}} = 20 \log 0.981 = -0.17 \text{ dB}$$

$$(A_v/A_{v(\text{mid})})_{\text{dB}} = 20 \log 0.958 = -0.37 \text{ dB}$$

Table 16-6 Between Midband and Cutoff

f/f_2	$A_v/A_{v(\text{mid})}$	$A_v/A_{v(\text{mid})}_{\text{dB}}$, dB
0.1	0.995	-0.04
0.2	0.981	-0.17
0.3	0.958	-0.37
0.4	0.928	-0.65
0.5	0.894	-0.97
0.6	0.857	-1.3
0.7	0.819	-1.7
0.8	0.781	-2.2
0.9	0.743	-2.6
1	0.707	-3

and so on. We seldom need the values of Table 16-6. But occasionally, we may want to refer to this table for an accurate value of voltage gain in the region between midband and cutoff.

Lag Circuit

Most op amps include an *RC* lag circuit that rolls off the voltage gain at a rate of 20 dB per decade. This prevents *oscillations*, unwanted signals that can appear under certain conditions. Later chapters will explain oscillations and how the internal lag circuit of an op amp prevents these unwanted signals.

Figure 16-14 shows a circuit with bypass capacitor. As discussed in Sec. 9-2, R represents the Thevenized resistance facing the capacitor. This circuit is often called a **lag circuit** because the output voltage lags the input voltage at higher frequencies. Stated another way: If the input voltage has a phase angle of 0° , the output voltage has a phase angle between 0° and -90° .

At low frequencies, the capacitive reactance approaches infinity, and the output voltage equals the input voltage. As the frequency increases, the capacitive reactance decreases, which decreases the output voltage. Recall from basic courses in electricity that the output voltage for this circuit is:

$$V_{\text{out}} = \frac{X_C}{\sqrt{R^2 + X_C^2}} V_{\text{in}}$$

If we rearrange the foregoing equation, the voltage gain of Fig. 16-14 is:

$$A_v = \frac{X_C}{\sqrt{R^2 + X_C^2}} \quad (16-21)$$

Because the circuit has only passive devices, the voltage gain is always less than or equal to 1.

The cutoff frequency of a lag circuit is where the voltage gain is 0.707. The equation for cutoff frequency is:

$$f_2 = \frac{1}{2\pi RC} \quad (16-22)$$

At this frequency, $X_C = R$ and the voltage gain is 0.707.

Bode Plot of Voltage Gain

By substituting $X_C = 1/2\pi f C$ into Eq. (16-21) and rearranging, we can derive this equation:

$$A_v = \frac{1}{\sqrt{1 + (f/f_2)^2}} \quad (16-23)$$

This equation is similar to Eq. (16-20), where $A_{v(\text{mid})}$ equals 1. For example, when $f/f_2 = 0.1, 0.2$, and 0.3 , we get:

$$A_v = \frac{1}{\sqrt{1 + (0.1)^2}} = 0.995$$

$$A_v = \frac{1}{\sqrt{1 + (0.2)^2}} = 0.981$$

$$A_v = \frac{1}{\sqrt{1 + (0.3)^2}} = 0.958$$

Continuing like this and converting to decibels, we get the values shown in Table 16-7.

Figure 16-14 An *RC* bypass circuit.

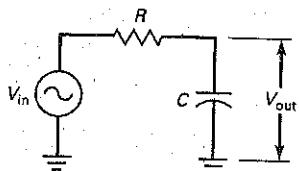


Table 16-7 Response of Lag Circuit

f/f_2	A_v	$A_{v(\text{dB})}$, dB
0.1	0.995	-0.04
1	0.707	-3
10	0.1	-20
100	0.01	-40
1000	0.001	-60

Figure 16-15 Ideal Bode plot of a lag circuit.

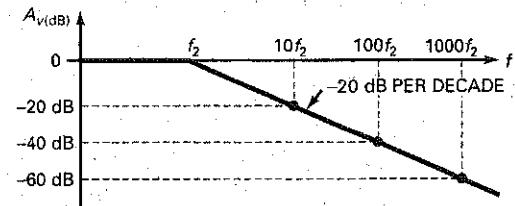


Figure 16-15 shows the ideal Bode plot of a lag circuit. In the midband, the decibel voltage gain is 0 dB. The response breaks at f_2 and then rolls off at a rate of 20 dB per decade.

6 dB per Octave

Above the cutoff frequency, the decibel voltage gain of a lag circuit decreases 20 dB per decade. This is equivalent to 6 dB per octave, which is easily proved as follows: When $f/f_2 = 10, 20$, and 40 , the voltage gain is:

$$A_v = \frac{1}{\sqrt{1 + (10)^2}} = 0.1$$

$$A_v = \frac{1}{\sqrt{1 + (20)^2}} = 0.05$$

$$A_v = \frac{1}{\sqrt{1 + (40)^2}} = 0.025$$

The corresponding decibel voltage gains are:

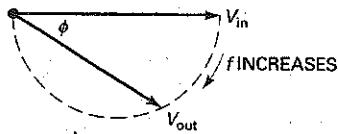
$$A_{v(\text{dB})} = 20 \log 0.1 = -20 \text{ dB}$$

$$A_{v(\text{dB})} = 20 \log 0.05 = -26 \text{ dB}$$

$$A_{v(\text{dB})} = 20 \log 0.025 = -32 \text{ dB}$$

In other words, you can describe the frequency response of a lag circuit above the cutoff frequency in either of two ways: You can say that the decibel voltage gain decreases at a rate of 20 dB per decade, or you can say that it decreases at a rate of 6 dB per octave.

Figure 16-16 Phasor diagram of lag circuit.



Phase Angle

The charging and discharging of a capacitor produce a lag in the output voltage of an *RC* bypass circuit. In other words, the output voltage will lag the input voltage by a phase angle ϕ . Figure 16-16 shows how ϕ varies with frequency. At zero hertz (0 Hz), the phase angle is 0° . As the frequency increases, the phase angle of the output voltage changes gradually from 0 to -90° . At very high frequencies, $\phi = -90^\circ$.

When necessary, we can calculate the phase angle with this equation from basic courses:

$$\phi = -\arctan \frac{R}{X_C} \quad (16-24)$$

By substituting $X_C = 1/2\pi fC$ into Eq. (16-24) and rearranging, we can derive this equation:

$$\phi = -\arctan \frac{f}{f_2} \quad (16-25)$$

With a calculator that has the tangent function and an inverse key, we can easily calculate the phase angle for any value of f/f_2 . Table 16-8 shows a few values for ϕ . For example, when $f/f_2 = 0.1, 1$, and 10 , the phase angles are:

$$\phi = -\arctan 0.1 = -5.71^\circ$$

$$\phi = -\arctan 1 = -45^\circ$$

$$\phi = -\arctan 10 = -84.3^\circ$$

Bode Plot of Phase Angle

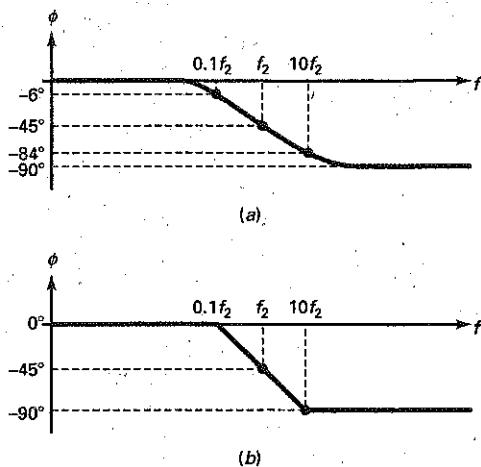
Figure 16-17 shows how the phase angle of a lag circuit varies with the frequency. At very low frequencies, the phase angle is zero. When $f = 0.1f_2$, the phase angle is approximately -6° . When $f = f_2$, the phase angle equals -45° . When $f = 10f_2$, the phase angle is approximately -84° . Further increases in frequency produce little change because the limiting value is -90° . As you can see, the phase angle of a lag circuit is between 0 and -90° .

A graph like Fig. 16-17a is a Bode plot of the phase angle. Knowing that the phase angle is -6° at $0.1f_2$ and 84° at $10f_2$ is of little value except to

Table 16-8 Response of Lag Circuit

f/f_2	ϕ
0.1	-5.71°
1	-45°
10	-84.3°
100	-89.4°
1000	-89.9°

Figure 16-17 Bode plots of phase angle.



indicate how close the phase angle is to its limiting value. The ideal Bode plot of Fig. 16-17b is more useful for preliminary analysis. This is the one to remember because it emphasizes these ideas:

1. When $f = 0.1f_2$, the phase angle is approximately zero.
2. When $f = f_2$, the phase angle is -45° .
3. When $f = 10f_2$, the phase angle is approximately -90° .

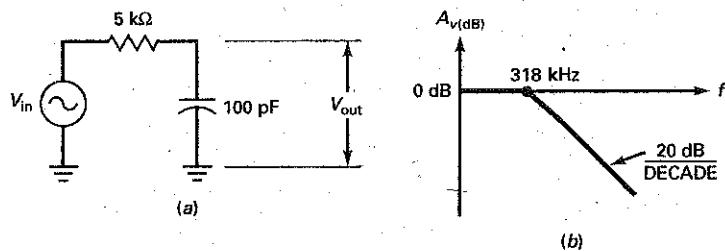
Another way to summarize the Bode plot of the phase angle is this: At the cutoff frequency, the phase angle equals -45° . A decade below the cutoff frequency, the phase angle is approximately 0° . A decade above the cutoff frequency, the phase angle is approximately -90° .

Example 16-14

Multisim

Draw the ideal Bode plot for the lag circuit of Fig. 16-18a.

Figure 16-18 A lag circuit and its Bode plot.



SOLUTION With Eq. (16-22), we can calculate the cutoff frequency:

$$f_2 = \frac{1}{2\pi(5\text{ k}\Omega)(100\text{ pF})} = 318\text{ kHz}$$

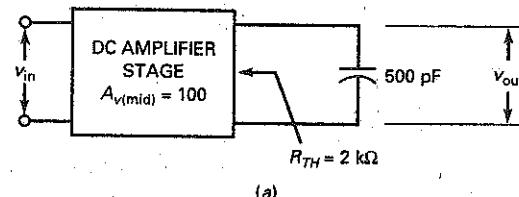
Figure 16-18b shows the ideal Bode plot. The voltage gain is 0 dB at low frequencies. The frequency response breaks at 318 kHz and then rolls off at a rate of 20 dB/decade.

PRACTICE PROBLEM 16-14 Using Fig. 16-18, change R to 10 k Ω and calculate the cutoff frequency.

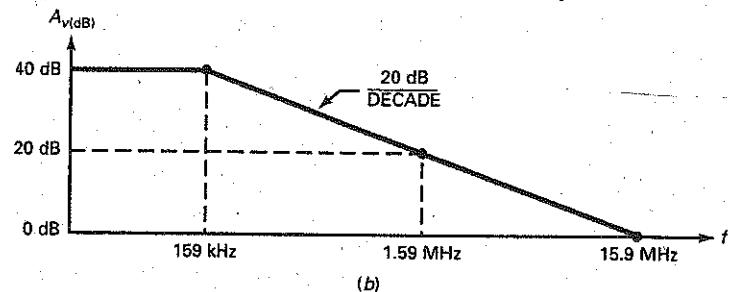
Example 16-15

In Fig. 16-19a, the dc amplifier stage has a midband voltage gain of 100. If the Thevenin resistance facing the bypass capacitor is 2 k Ω , what is the ideal Bode plot? Ignore all capacitances inside the amplifier stage.

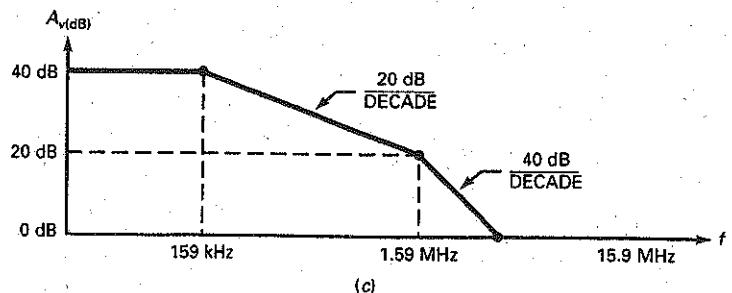
Figure 16-19 (a) DC amplifier and bypass capacitor; (b) ideal Bode plot; (c) Bode plot with second break frequency.



(a)



(b)



(c)

SOLUTION The Thevenin resistance and the bypass capacitor are a lag circuit with a cutoff frequency of:

$$f_2 = \frac{1}{2\pi(2 \text{ k}\Omega)(500 \text{ pF})} = 159 \text{ kHz}$$

The amplifier has a midband voltage gain of 100, which is equivalent to 40 dB.

Figure 16-19b shows the ideal Bode plot. The decibel voltage gain is 40 dB from zero to the cutoff frequency of 159 kHz. The response then rolls off at a rate of 20 dB per decade until it reaches a f_{unify} of 15.9 MHz.

PRACTICE PROBLEM 16-15 Repeat Example 16-15 using a Thevenin resistance of 1 kΩ.

Example 16-16

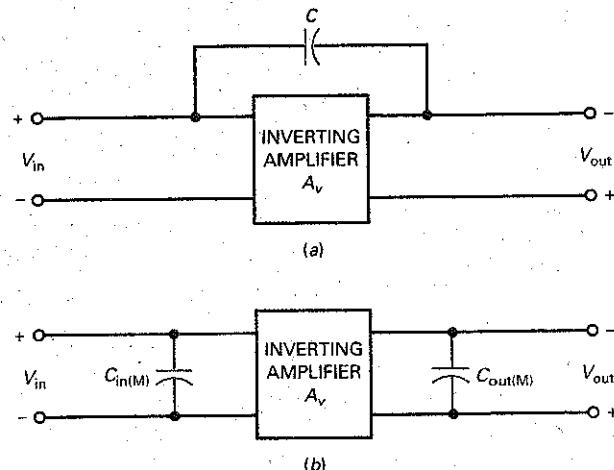
Suppose the amplifier stage of Fig. 16-19a has an internal lag circuit with a cutoff frequency of 1.59 MHz. What effect will this have on the ideal Bode plot?

SOLUTION Figure 16-19c shows the frequency response. The response breaks at 159 kHz, the cutoff frequency produced by the external 500-pF capacitor. The voltage gain rolls off at 20 dB per decade until the frequency is 1.59 MHz. At this point, the response breaks again because this is the cutoff frequency of internal lag circuit. The gain then rolls off at a rate of 40 dB per decade.

16-8 The Miller Effect

Figure 16-20a shows an inverting amplifier with a voltage gain of A_v . Recall that an inverting amplifier produces an output voltage that is 180° out of phase with the input voltage.

Figure 16-20 (a) Inverting amplifier; (b) Miller effect produces large input capacitor.



Feedback Capacitor

In Fig. 16-20a, the capacitor between the input and output terminals is called a **feedback capacitor** because the amplified output signal is being fed back to the input. A circuit like this is difficult to analyze because the feedback capacitor affects the input and output circuits simultaneously.

Converting the Feedback Capacitor

Fortunately, there is a shortcut called *Miller's theorem* that converts the capacitor into two separate capacitors, as shown in Fig. 16-20b. This equivalent circuit is easier to work with because the feedback capacitor has been split into two new capacitances, $C_{in(M)}$ and $C_{out(M)}$. With complex algebra, it is possible to derive the following equations:

$$C_{in(M)} = C(A_v + 1) \quad (16-26)$$

$$C_{out(M)} = C\left(\frac{A_v + 1}{A_v}\right) \quad (16-27)$$

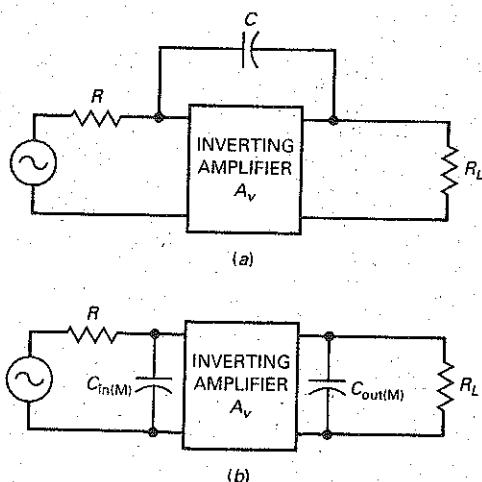
Miller's theorem converts the feedback capacitor into two equivalent capacitors, one for the input side and the other for the output side. This makes two simple problems out of one big one. Equations (16-26) and (16-27) are valid for any inverting amplifier such as a CE amplifier, a swamped CE amplifier, or an inverting op amp. In these equations, A_v is the midband voltage gain.

Usually, A_v is much greater than 1, and $C_{out(M)}$ is approximately equal to the feedback capacitance. The striking thing about Miller's theorem is the effect it has on the input capacitance $C_{in(M)}$. It's as though the feedback capacitance has been amplified to get a new capacitance that is $A_v + 1$ times larger. This phenomenon, known as the **Miller effect**, has useful applications because it creates artificial or virtual capacitors that are much larger than the feedback capacitor.

Compensating an Op Amp

As discussed in Sec. 16-7, most op amps are *internally compensated*, which means that they include one dominant bypass capacitor that rolls off the voltage gain at a rate of 20 dB per decade. The Miller effect is used to produce this dominant bypass capacitor.

Figure 16-21 Miller effect produces an input lag circuit.



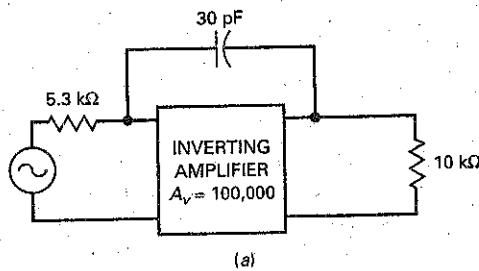
Here is the basic idea: One of the amplifier stages in an op amp has a feedback capacitor as shown in Fig. 16-21a. With Miller's theorem, we can convert this feedback capacitor into the two equivalent capacitors shown in Fig. 16-21b. Now, there are two lag circuits, one on the input side and one on the output side. Because of the Miller effect, the bypass capacitor on the input side is much larger than the bypass capacitor on the output side. As a result, the input lag circuit is dominant; that is, it determines the cutoff frequency of the stage. The output bypass capacitor usually has no effect until the input frequency is several decades higher.

In a typical op amp, the input lag circuit of Fig. 16-21b produces a dominant cutoff frequency. The voltage gain breaks at this cutoff frequency and then rolls off at a rate of 20 dB per decade until the input frequency reaches the unity-gain frequency.

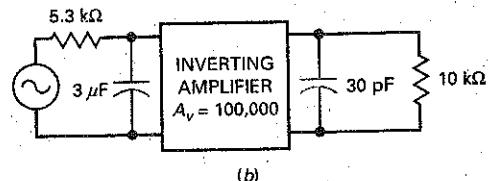
Example 16-17

The amplifier of Fig. 16-22a has a voltage gain of 100,000. Draw the ideal Bode plot.

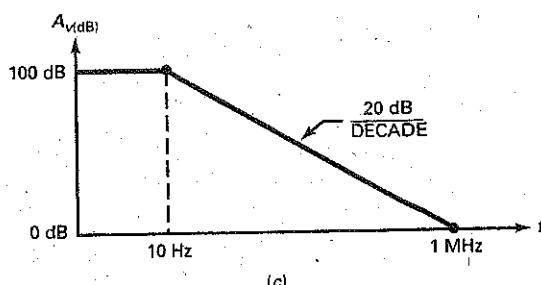
Figure 16-22 Amplifier with feedback capacitor and its Bode plot.



(a)



(b)



(c)

SOLUTION Start by converting the feedback capacitor to its Miller components. Since the voltage gain is much greater than 1:

$$C_{in(M)} = 100,000(30 \text{ pF}) = 3 \mu\text{F}$$

$$C_{out(M)} = 30 \text{ pF}$$

Figure 16-22b shows the input and output Miller capacitances. The dominant lag circuit on the input side has a cutoff frequency of:

$$f_2 = \frac{1}{2\pi RC} = \frac{1}{2\pi(5.3 \text{ k}\Omega)(3 \mu\text{F})} = 10 \text{ Hz}$$

Since a voltage gain of 100,000 is equivalent to 100 dB, we can draw the ideal Bode plot shown in Fig. 16-22c.

PRACTICE PROBLEM 16-17 Using Fig. 16-22a, determine $C_{in(M)}$ and $C_{out(M)}$ if the voltage gain is 10,000.

16-9 Risetime-Bandwidth Relationship

Sine-wave testing of an amplifier means that we use a sinusoidal input voltage and measure the sinusoidal output voltage. To find the upper cutoff frequency, we have to vary the input frequency until the voltage gain drops 3 dB from the midband value. Sine-wave testing is one approach. But there is a faster and simpler way to test an amplifier by using a square wave instead of a sine wave.

Risetime

The capacitor is initially uncharged in Fig. 16-23a. If we close the switch, the capacitor voltage will rise exponentially toward the supply voltage V . The risetime T_R is the time it takes the capacitor voltage to go from 0.1V (called the *10 percent point*) to 0.9V (called the *90 percent point*). If it takes 10 μs for the exponential waveform to go from the 10 percent point to the 90 percent point, the waveform has a risetime of:

$$T_R = 10 \mu\text{s}$$

Instead of using a switch to apply the sudden step in voltage, we can use a square-wave generator. For instance, Fig. 16-23b shows the leading edge of a square wave driving the same RC circuit as before. The risetime is still the time it takes for the voltage to go from the 10 percent point to the 90 percent point.

Figure 16-23c shows how several cycles will look. Although the input voltage changes almost instantly from one voltage level to another, the output voltage takes much longer to make its transitions because of the bypass capacitor. The output voltage cannot suddenly step, because the capacitor has to charge and discharge through the resistance.

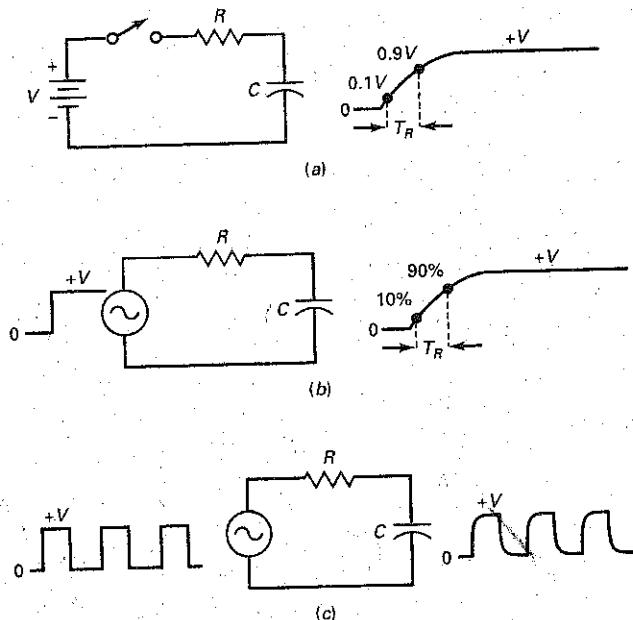
Relationship between T_R and RC

By analyzing the exponential charge of a capacitor, it is possible to derive this equation for the risetime:

$$T_R = 2.2RC$$

(16-28)

Figure 16-23 (a) Risetime; (b) voltage step produces output exponential; (c) square-wave testing.



This says that the risetime is slightly more than two RC time constants. For instance, if R equals $10\text{ k}\Omega$ and C is 50 pF , then:

$$RC = (10\text{ k}\Omega)(50\text{ pF}) = 0.5\ \mu\text{s}$$

The risetime of the output waveform equals:

$$T_R = 2.2RC = 2.2(0.5\ \mu\text{s}) = 1.1\ \mu\text{s}$$

Data sheets often specify the risetime because it is useful to know the response to a voltage step when analyzing switching circuits.

An Important Relationship

As mentioned earlier, a dc amplifier typically has one dominant lag circuit that rolls off the voltage gain at a rate of 20 dB per decade until f_{unity} is reached. The cutoff frequency of this lag circuit is given by:

$$f_2 = \frac{1}{2\pi RC}$$

which can be solved for RC to get:

$$RC = \frac{1}{2\pi f_2}$$

When we substitute this into Eq. (16-28) and simplify, we get this widely used equation:

$$f_2 = \frac{0.35}{T_R} \quad (16-29)$$

This is an important result because it converts risetime to cutoff frequency. It means that we can test an amplifier with a square wave to find the cutoff frequency. Since square-wave testing is much faster than sine-wave testing, many engineers and technicians use Eq. (16-29) to find the upper cutoff frequency of an amplifier.

Equation (16-29) is called the *risetime-bandwidth relationship*. In a dc amplifier, the word *bandwidth* refers to all the frequencies from zero up to the cutoff frequency. Often, bandwidth is used as a synonym for *cutoff frequency*. If the data sheet for a dc amplifier gives a bandwidth of 100 kHz, it means that the upper cutoff frequency equals 100 kHz.

Example 16-18

What is the upper cutoff frequency for the circuit shown in Fig. 16-24a?

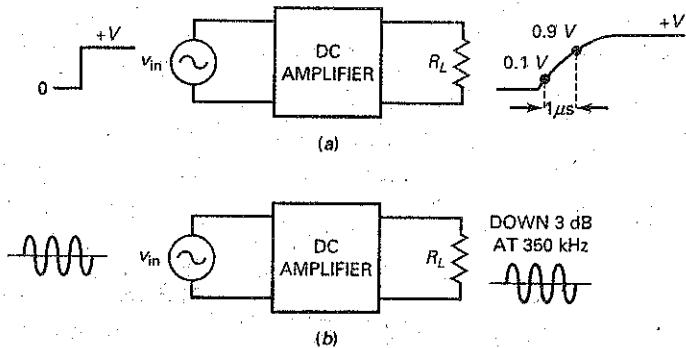
SOLUTION In Fig. 16-24a, the risetime is 1 μ s. With Eq. (16-29):

$$f_2 = \frac{0.35}{1 \mu\text{s}} = 350 \text{ kHz}$$

Therefore, the circuit of Fig. 16-24a has an upper cutoff frequency of 350 kHz. An equivalent statement is that the circuit has a bandwidth of 350 kHz.

Figure 16-24b illustrates the meaning of sine-wave testing. If we change the input voltage from a square wave to a sine wave, we will get a sine-wave output. By increasing the input frequency, we can eventually find the cutoff frequency of 350 kHz. In other words, we would get the same result with sine-wave testing, except that it is slower than square-wave testing.

Figure 16-24 Risetime and cutoff frequency are related.



PRACTICE PROBLEM 16-18 An RC circuit has $R = 2 \text{ k}\Omega$ and $C = 100 \text{ pF}$. Determine the risetime of the output waveform and its upper cutoff frequency.

16-10 Frequency Analysis of BJT Stages

A wide variety of op amps is now commercially available with unity-gain frequencies from 1 to over 200 MHz. Because of this, most amplifiers are now built using op amps. Since op amps are the heart of analog systems, the analysis of discrete amplifier stages is less important than it once was. The next section briefly discusses the low- and high-cutoff frequencies of a voltage-divider biased CE stage. We will look at the effects of individual components on the circuit's frequency response, starting with the low-frequency cutoff point.

Input Coupling Capacitor

When an ac signal is coupled into an amplifier stage, the equivalent looks like Fig. 16-25a. Facing the capacitor is the generator resistance and the input resistance of the stage. This coupling circuit has a cutoff frequency of:

$$f_1 = \frac{1}{2\pi RC} \quad (16-30)$$

where R is the sum of R_G and R_{in} . Figure 16-25b shows the frequency response.

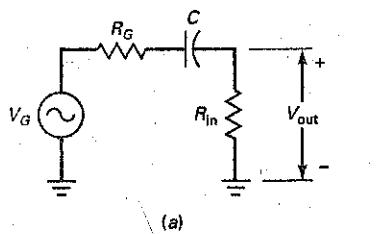
Output Coupling Capacitor

Figure 16-26a shows the output side of a BJT stage. After applying Thevenin's theorem, we get the equivalent circuit of Fig. 16-26b. Equation (16-30) can be used to calculate the cutoff frequency, where R is the sum of R_C and R_L .

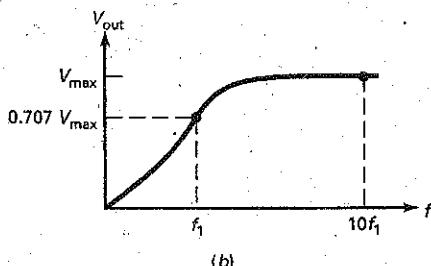
Emitter Bypass Capacitor

Figure 16-27a shows a CE amplifier. Figure 16-27b shows the effect that the emitter bypass capacitor has on the output voltage. Facing the emitter bypass capacitor

Figure 16-25 Coupling circuit and its frequency response.

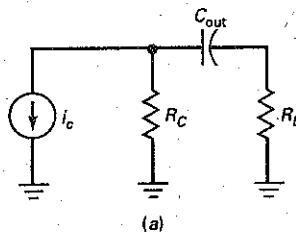


(a)

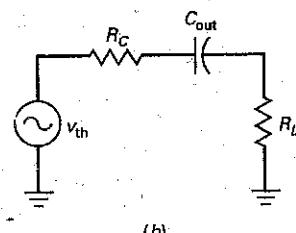


(b)

Figure 16-26 Output coupling capacitor.

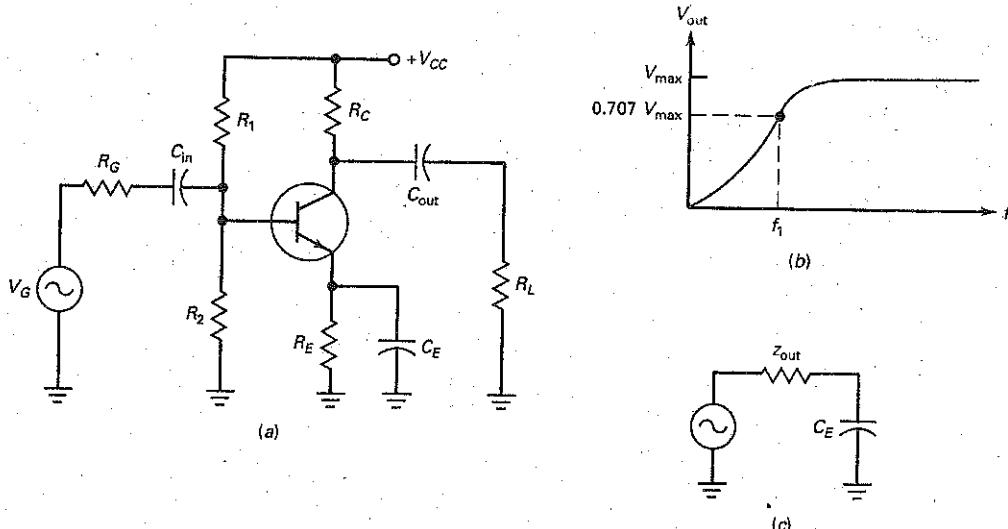


(a)



(b)

Figure 16-27 Effect of the emitter bypass capacitor.



is the Thevenin circuit of Fig. 16-27c. The cutoff frequency is given by:

$$f_1 = \frac{1}{2\pi z_{out} C_E} \quad (16-31)$$

The output impedance z_{out} was discussed in Chap. 11 and is given by Eqs. (11-5) and (11-6).

The input coupling, output coupling, and emitter bypass capacitors each produce a cutoff frequency. Usually, one of these is dominant. When the frequency decreases, the gain breaks at this dominant cutoff frequency. Then, it rolls off at a rate of 20 dB per decade until it breaks again at the next cutoff frequency. It then rolls off at 40 dB per decade until it breaks a third time. With further decreases in frequency, the voltage gain rolls off at 60 dB per decade.

Example 16-19

Using the circuit values shown in Fig. 16-28a, calculate the low-cutoff frequency for each coupling and bypass capacitor. Compare the results to a measurement using a Bode plot. (Use 150 for the dc and ac beta values.)

SOLUTION In Fig. 16-28a, we will analyze each coupling capacitor and each bypass capacitor separately. When analyzing each capacitor, treat the other two capacitors as ac shorts.

From past dc calculations of this circuit, $r'_e = 22.7 \Omega$. The Thevenin resistance facing the input coupling capacitor is:

$$R = R_G + R_1 \| R_2 \| R_{in(base)}$$

where

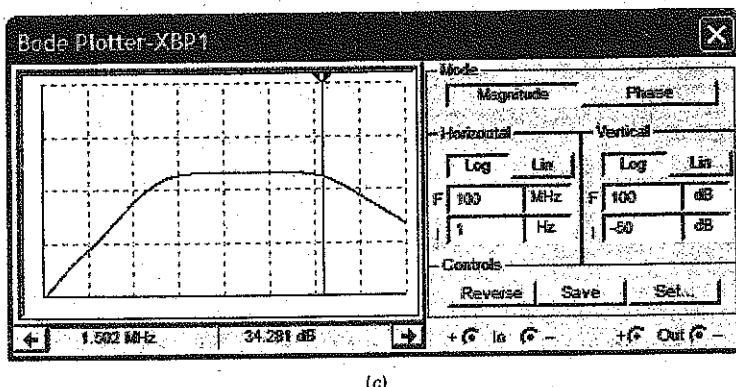
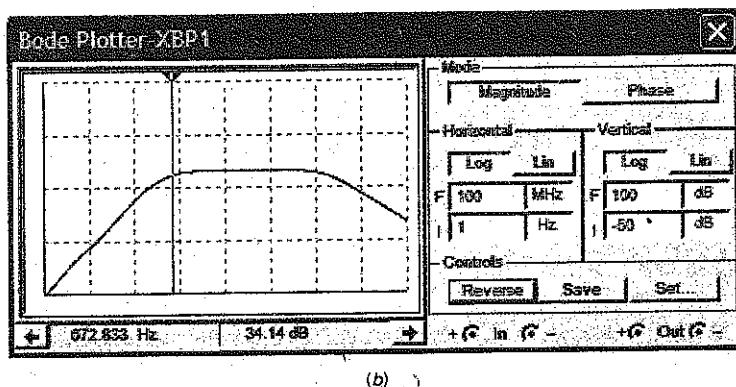
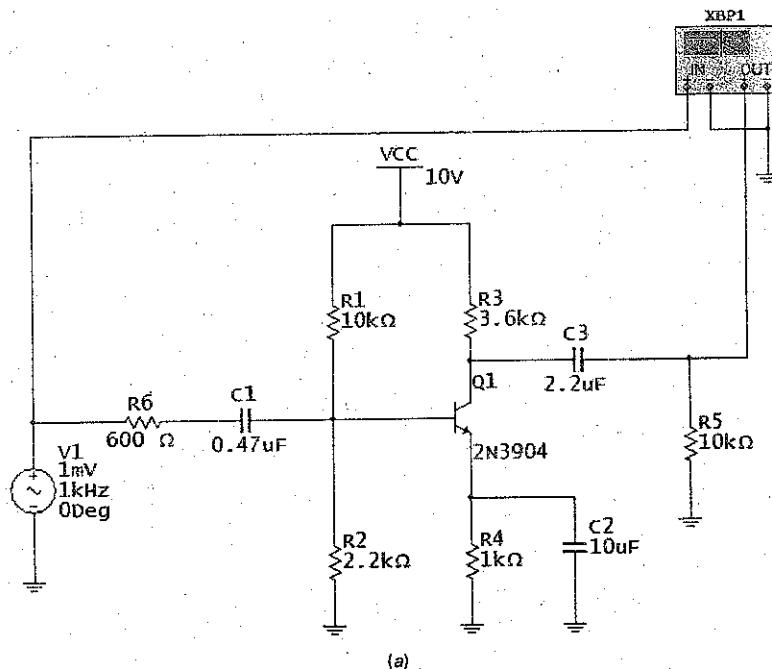
$$R_{in(base)} = (\beta)(r'_e) = (150)(22.7 \Omega) = 3.41 \text{ k}\Omega$$

Therefore,

$$R = 600 \Omega + (10 \text{ k}\Omega \| 2.2 \text{ k}\Omega \| 3.41 \text{ k}\Omega)$$

$$R = 600 \Omega + 1.18 \text{ k}\Omega = 1.78 \text{ k}\Omega$$

Figure 16-28 (a) CE amplifier using MultiSim; (b) low-frequency response; (c) high-frequency response.



Using Eq. (16-30), the input coupling circuit has a cutoff frequency of:

$$f_1 = \frac{1}{2\pi RC} = \frac{1}{(2\pi)(1.78 \text{ k}\Omega)(0.47 \mu\text{F})} = 190 \text{ Hz}$$

Next, the Thevenin resistance facing the output coupling capacitor is:

$$R = R_C + R_L = 3.6 \text{ k}\Omega + 10 \text{ k}\Omega = 13.6 \text{ k}\Omega$$

The output coupling circuit will have a cutoff frequency of:

$$f_1 = \frac{1}{2\pi RC} = \frac{1}{(2\pi)(13.6 \text{ k}\Omega)(2.2 \mu\text{F})} = 5.32 \text{ Hz}$$

Now, the Thevenin resistance facing the emitter-bypass capacitor is found by:

$$Z_{\text{out}} = 1 \text{ k}\Omega \parallel 22.7 \Omega + \frac{10 \text{ k}\Omega \parallel 2.2 \text{ k}\Omega \parallel 600 \Omega}{150}$$

$$Z_{\text{out}} = 1 \text{ k}\Omega \parallel (22.7 \Omega + 3.0 \Omega)$$

$$Z_{\text{out}} = 1 \text{ k}\Omega \parallel 25.7 \Omega = 25.1 \Omega$$

Therefore, the cutoff frequency for the bypass circuit is:

$$f_1 = \frac{1}{2\pi Z_{\text{out}} C_E} = \frac{1}{(2\pi)(25.1 \Omega)(10 \mu\text{F})} = 635 \text{ Hz}$$

The results show that:

$$f_1 = 190 \text{ Hz} \quad \text{input-coupling capacitor}$$

$$f_1 = 5.32 \text{ Hz} \quad \text{output-coupling capacitor}$$

$$f_1 = 635 \text{ Hz} \quad \text{emitter-bypass capacitor}$$

As you can see by the results, the emitter-bypass circuit becomes the dominant lower frequency cutoff value.

The measured midpoint voltage gain, $A_{v(\text{mid})}$, in the Bode plot of Fig. 16-28b, is 37.1 dB. The Bode plot shows an approximate 3 dB drop at a frequency of 673 Hz. This is close to our calculation.

PRACTICE PROBLEM 16-19 Using Fig. 16-28a, change the input coupling capacitor to 10 μF and the emitter bypass capacitor to 100 μF . Determine the new dominant cutoff frequency.

Collector Bypass Circuit

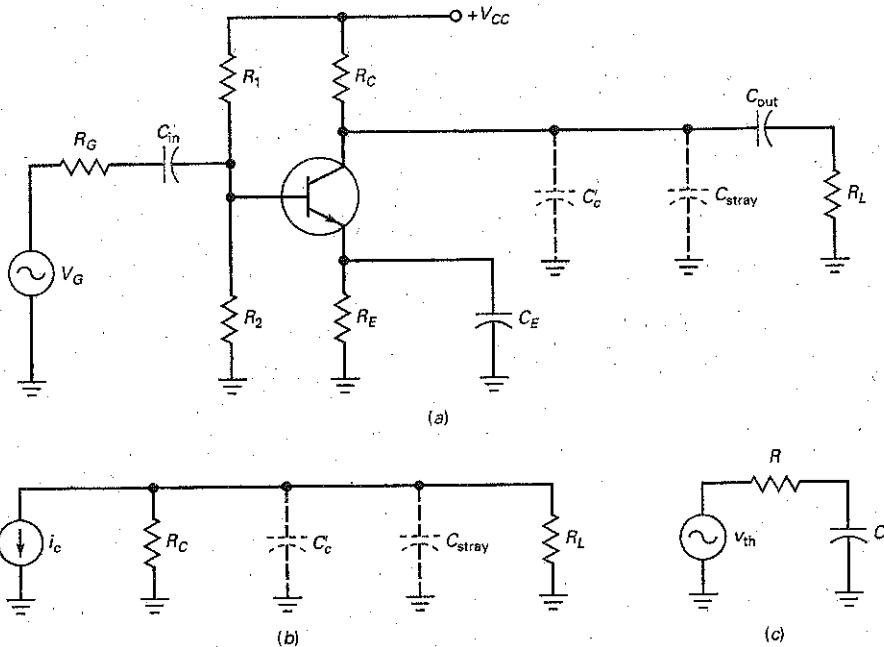
The high-frequency response of an amplifier involves a significant amount of detail and requires accurate values to get good results. We will use some detail in our discussion, but more accurate results can be obtained with circuit simulation software.

Figure 16-29a shows a CE stage with stray-wiring capacitance C_{stray} . Just to the left is C'_c , a quantity usually specified on the data sheet of a transistor. This is the internal capacitance between the collector and the base. Although C'_c and C_{stray} are very small, they will have an effect when the input frequency is high enough.

Figure 16-29b is the ac equivalent circuit, and Fig. 16-29c is the Thevenin equivalent circuit. The cutoff frequency of this lag circuit is:

$$f_2 = \frac{1}{2\pi RC} \tag{16-32}$$

Figure 16-29 Internal and stray-wiring capacitance produce upper cutoff frequency.



where $R = R_C \parallel R_L$ and $C = C_c + C_{\text{stray}}$. It is important to keep wires as short as possible in high-frequency work because the stray-wiring capacitance degrades bandwidth by lowering the cutoff frequency.

Base Bypass Circuit

The transistor has two internal capacitances, C'_c and C'_e , as shown in Fig. 16-30. Since C'_c is a feedback capacitor, it can be converted into two components. The input Miller component then appears in parallel with C'_e . The cutoff frequency of this base bypass circuit is given by Eq. (16-32), where R is the Thevenin resistance facing the capacitance. The capacitance is the sum of C'_e and the input Miller component.

The collector bypass capacitor and Miller input capacitance each produce a cutoff frequency. Normally, one of these is dominant. When the frequency increases, the gain breaks at this dominant cutoff frequency. Then, it rolls off at a rate

Figure 16-30 High-frequency analysis includes internal transistor capacitances.

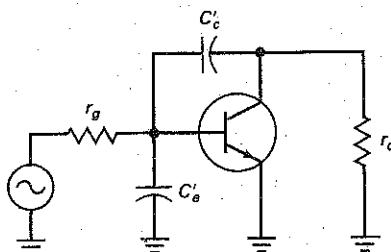
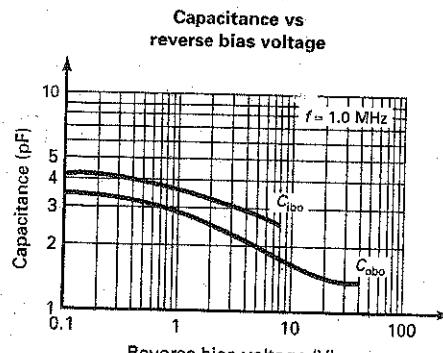


Figure 16-31 The 2N3904 data: (a) internal capacitance; (b) changes with reverse voltage.

Small signal characteristics

f_T	Current gain-bandwidth product	$I_C = 10 \text{ mA}, V_{CE} = 20 \text{ V}$, $f = 100 \text{ MHz}$	300	MHz
C_{obo}	Output capacitance	$V_{CB} = 5.0 \text{ V}, I_E = 0$, $f = 1.0 \text{ MHz}$	4.0	pF
C_{ibo}	Input capacitance	$V_{EB} = 0.5 \text{ V}, I_C = 0$, $f = 1.0 \text{ MHz}$	8.0	pF
NF	Noise figure	$I_C = 100 \mu\text{A}, V_{CE} = 5.0 \text{ V}$, $R_S = 1.0 \text{ k}\Omega, f = 10 \text{ Hz to } 15.7 \text{ kHz}$	5.0	dB

(a)



(b)

of 20 dB per decade until it breaks again at the second cutoff frequency. With further decreases in frequency, the voltage gain rolls off at 40 dB per decade.

On data sheets, C'_e may be listed as C_{be} , C_{ob} , or C_{obo} . This value is specified at a particular transistor operating condition. As an example, the C_{obo} value for a 2N3904 is specified as 4.0 pF when $V_{CB} = 5.0 \text{ V}$, $I_E = 0$, and frequency is 1 MHz. C'_e is often listed as C_{be} , C_{ib} , or C_{obo} on data sheets. The data sheet for a 2N3904 specifies a C_{ibo} value of 4 pF when $V_{CB} = 5.0 \text{ V}$, $I_E = 0$, and frequency is 1 MHz. These values are shown in Fig. 16-31a under Small Signal Characteristics.

Each of these internal capacitance values will vary, depending on the circuit condition. Fig. 16-31b shows how C_{obo} changes as the amount of reverse bias V_{CB} changes. Also, C_{be} is dependent on the transistor's operating point. When not given on a data sheet, C_{be} can be approximated by:

$$C_{be} \approx \frac{1}{2\pi f_T r'_e} \quad (16-33)$$

where f_T is the current gain-bandwidth product normally listed on the data sheet. The value r_g , shown in Fig. 16-30, is equal to:

$$r_g = R_G \parallel R_1 \parallel R_2 \quad (16-34)$$

and r_c is found by:

$$r_c = R_C \parallel R_L \quad (16-35)$$

Example 16-20

Multisim

Using the circuit values shown in Fig. 16-28a, calculate the high-frequency cutoff values for the base bypass circuit and the collector bypass circuit. Use 150 for beta and 10 pF for the stray output capacitance. Compare the results to a Bode plot using simulation software.

SOLUTION First determine the values of transistor input and output capacitance.

In our previous dc calculations of this circuit, we determined that $V_B = 1.8$ V and $V_C = 6.04$ V. This results in a collector-to-base reverse voltage of approximately 4.2 V. Using the graph of Fig. 16-31b, the value of C_{obo} or C'_e at this reverse voltage is 2.1 pF. The value of C'_e can be found using Eq. (16-33) as:

$$C'_e = \frac{1}{(2\pi)(300 \text{ MHz})(22.7 \Omega)} = 23.4 \text{ pF}$$

Since the voltage gain for this amplifier circuit is:

$$A_v = \frac{r_e'}{r_e} = \frac{2.65 \text{ k}\Omega}{22.7 \Omega} = 117$$

The input Miller capacitance is found by:

$$C_{in(M)} = C_C(A_v + 1) = 2.1 \text{ pF}(117 + 1) = 248 \text{ pF}$$

Therefore, the base bypass capacitance equals:

$$C = C'_e + C_{in(M)} = 23.4 \text{ pF} + 248 \text{ pF} = 271 \text{ pF}$$

The resistance value facing this capacitance is:

$$R = r_g \parallel R_{in(base)} = 450 \Omega \parallel (150)(22.7 \Omega) = 397 \Omega$$

Now, using Eq. (16-32), the base bypass circuit cutoff frequency is:

$$f_2 = \frac{1}{(2\pi)(397 \Omega)(271 \text{ pF})} = 1.48 \text{ MHz}$$

The collector bypass circuit cutoff frequency is found by first determining the total output bypass capacitance:

$$C = C'_C + C_{stray}$$

Using Eq. (16-27), the output Miller capacitance is found by:

$$C_{out(M)} = C_C \left(\frac{A_v + 1}{A_v} \right) = 2.1 \text{ pF} \left(\frac{117 + 1}{117} \right) \cong 2.1 \text{ pF}$$

The total output bypass capacitance is:

$$C = 2.1 \text{ pF} + 10 \text{ pF} = 12.1 \text{ pF}$$

The resistance facing this capacitance is:

$$R = R_C \parallel R_L = 3.6 \text{ k}\Omega \parallel 10 \text{ k}\Omega = 2.65 \text{ k}\Omega$$

Therefore, the collector bypass circuit cutoff frequency is:

$$f_2 = \frac{1}{(2\pi)(2.65 \text{ k}\Omega)(12.1 \text{ pF})} = 4.96 \text{ MHz}$$

The dominant cutoff frequency is determined by the lower of the two cutoff frequencies. In Fig. 16-28a, the Bode plot using MultiSim shows a high-frequency cutoff of approximately 1.5 MHz.

PRACTICE PROBLEM 16-20 If the stray capacitance in Example 16-20 is 40 pF, determine the collector bypass cutoff frequency.

16-11 Frequency Analysis of FET Stages

The frequency response analysis of FET circuits is very similar to that of BJT circuits. In most cases, the FET will have an input coupling circuit and an output coupling circuit, one of which will determine the low-frequency cutoff point. The gate and drain will have an unwanted bypass circuit mainly as the result of the FET's internal capacitances. Along with stray wiring capacitance, this will determine the high-frequency cutoff point.

Low-Frequency Analysis

Fig. 16-32 shows an E-MOSFET common-source amplifier circuit using voltage-divider bias. Because of the very high input resistance of the MOSFET, the resistance R facing the input coupling capacitor is:

$$R = R_G + R_1 \parallel R_2 \quad (16-36)$$

and the input coupling cutoff frequency is found by:

$$f_1 = \frac{1}{2\pi RC}$$

The output resistance facing the output coupling capacitor is:

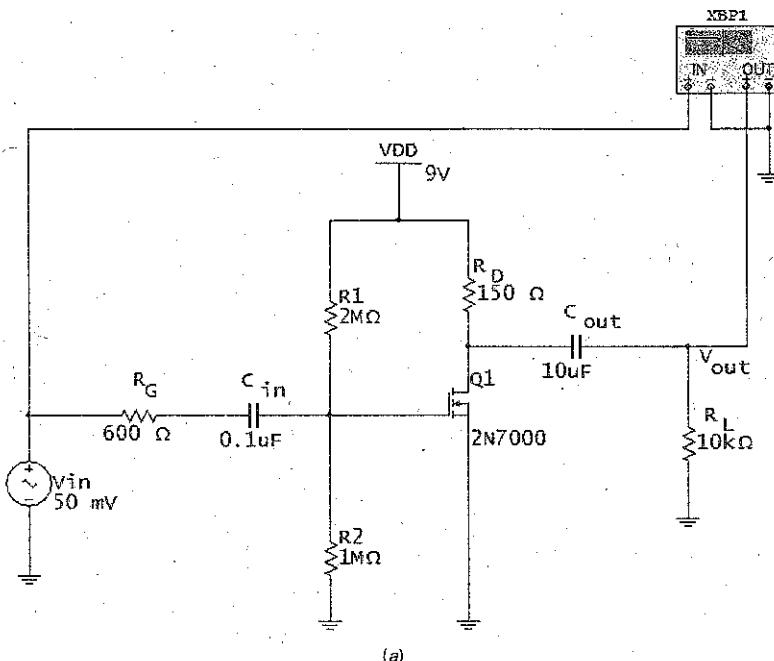
$$R = R_D + R_L$$

and the output coupling cutoff frequency is found by:

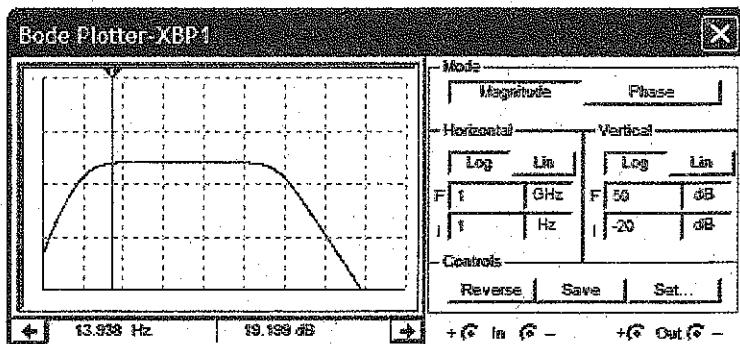
$$f_1 = \frac{1}{2\pi RC}$$

As you can see, the low-frequency analysis of the FET circuit is very similar to the BJT circuit. Because of the very high input resistance of the FET, larger voltage-divider-resistor values can be used. This results in being able to use a much smaller input-coupling capacitor.

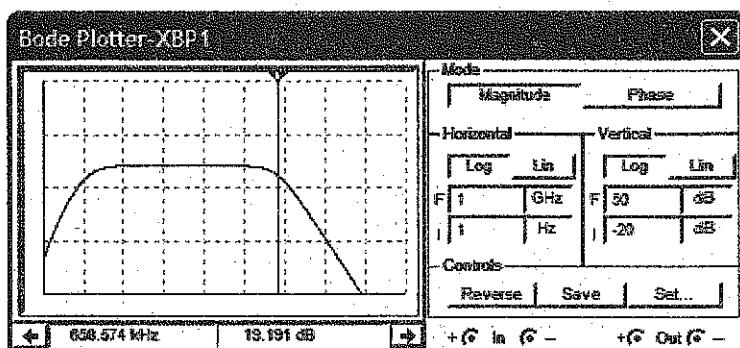
Figure 16-32 FET frequency analysis: (a) E-MOSFET amplifier; (b) low-frequency response; (c) high-frequency response.



(a)



(b)



(c)

Example 16-21

III Multisim

Using the circuit shown in Fig. 16-32, determine the input-coupling circuit and output-coupling circuit low-frequency cutoff points. Compare the calculated values to a Bode plot using MultiSim.

SOLUTION The Thevenin resistance facing the input-coupling capacitor is:

$$R = 600 \Omega + 2 \text{ M}\Omega \| 1 \text{ M}\Omega = 667 \text{ k}\Omega$$

and the input-coupling cutoff frequency is:

$$f_1 = \frac{1}{(2\pi)(667 \text{ k}\Omega)(0.1 \mu\text{F})} = 2.39 \text{ Hz}$$

Next, the Thevenin resistance facing the output coupling capacitor is found by:

$$R = 150 \Omega + 1 \text{ k}\Omega = 1.15 \text{ k}\Omega$$

and the output coupling cutoff frequency is:

$$f_1 = \frac{1}{(2\pi)(130 \Omega)(10 \mu\text{F})} = 13.8 \text{ Hz}$$

Therefore, the dominant low-frequency cutoff value is 13.8 Hz. The midpoint voltage gain of this circuit is 22.2 dB. The Bode plot in 16-32b shows a 3 dB loss at approximately 14 Hz. This is very close to the calculated value.

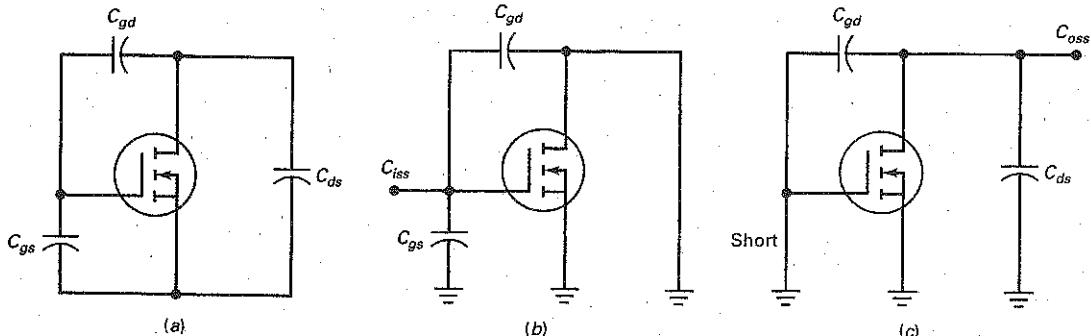
High-Frequency Analysis

Like the high-frequency analysis of a BJT circuit, determining the high-frequency cutoff point of a FET involves a significant amount of detail and requires the use of accurate values. As with the BJT, FETs have internal capacitances C_{gs} , C_{gd} , and C_{ds} as shown in Fig. 16-33a. These capacitance values are not important at low frequencies, but become significant at high frequencies.

Because these capacitances are difficult to measure, manufacturers measure and list the FET capacitances under short-circuit conditions. For example, C_{iss} is the input capacitance with an ac short across the output. When doing this, C_{gd} becomes in parallel with C_{gs} (Fig. 16-33b) so C_{iss} is found by:

$$C_{iss} = C_{ds} + C_{gd}$$

Figure 16-33 Measuring FET capacitances.



Data sheets often list C_{oss} , the capacitance looking back into the FET with a short across the input terminals (Fig. 16-33c), as:

$$C_{oss} = C_{ds} + C_{gd}$$

Data sheets also commonly list the feedback capacitance C_{rss} . The feedback capacitance is equal to:

$$C_{rss} = C_{gd}$$

By using these equations, we can determine that:

$$C_{gd} = C_{rss} \quad (16-37)$$

$$C_{gs} = C_{iss} - C_{rss} \quad (16-38)$$

$$C_{ds} = C_{oss} - C_{rss} \quad (16-39)$$

The gate-to-drain capacitance C_{gd} is used to determine the input Miller capacitance $C_{in(M)}$ and the output Miller capacitance $C_{out(M)}$. These values are found by:

$$C_{in(M)} = C_{gd} (A_v + 1) \quad (16-40)$$

and

$$C_{out(M)} = C_{gd} \left(\frac{A_v + 1}{A_v} \right) \quad (16-41)$$

where $A_v = g_m r_d$ for the common-source amplifier.

Example 16-22

MOSFET

In the MOSFET amplifier circuit of Fig. 16-32, the 2N7000 has these capacitances given on a data sheet:

$$C_{iss} = 60 \text{ pF}$$

$$C_{oss} = 25 \text{ pF}$$

$$C_{rss} = 5.0 \text{ pF}$$

If $g_m = 97 \text{ mS}$, what are the high-frequency cutoff values for the gate and drain circuits? Compare the calculations to a Bode plot.

SOLUTION Using the given data sheet capacitance values, we can determine the FET's internal capacitances by:

$$C_{gd} = C_{rss} = 5.0 \text{ pF}$$

$$C_{gs} = C_{iss} - C_{rss} = 60 \text{ pF} - 5 \text{ pF} = 55 \text{ pF}$$

$$C_{ds} = C_{oss} - C_{rss} = 25 \text{ pF} - 5 \text{ pF} = 20 \text{ pF}$$

To determine the Miller input capacitance, we must first find the voltage gain of the amplifier. This is found by:

$$A_v = g_m r_d = (93 \text{ mS})(150 \Omega \parallel 1 \text{ k}\Omega) = 12.1$$

Therefore, $C_{in(M)}$ is:

$$C_{in(M)} = C_{gd} (A_v + 1) = 5.0 \text{ pF} (12.1 + 1) = 65.5 \text{ pF}$$

The gate bypass capacitance is found by:

$$C = C_{gs} + C_{in(M)} = 55 \text{ pF} + 65.5 \text{ pF} = 120.5 \text{ pF}$$

The resistance facing C is:

$$R = R_G \parallel R_1 \parallel R_2 = 600 \Omega \parallel 2 \text{ M}\Omega \parallel 1 \text{ M}\Omega \approx 600 \Omega$$

The gate-bypass cutoff frequency is:

$$f_2 = \frac{1}{(2\pi)(600 \Omega)(120.5 \text{ pF})} = 2.2 \text{ MHz}$$

Next, the drain-bypass capacitance is found by:

$$C = C_{ds} + C_{out(M)}$$

$$C = 20 \text{ pF} + 5.0 \text{ pF} \left(\frac{12.1 + 1}{12.1} \right) = 25.4 \text{ pF}$$

The resistance r_d facing this capacitance is:

$$r_d = R_D \parallel R_L = 150 \Omega \parallel 1 \text{ k}\Omega = 130 \Omega$$

The drain-bypass cutoff frequency is therefore:

$$f_2 = \frac{1}{(2\pi)(130 \Omega)(25.4 \text{ pF})} = 48 \text{ MHz}$$

As shown in Fig. 16-32c, the high-frequency cutoff frequency measured using MultiSim is approximately 638 kHz. As you can see, this measurement differs significantly from our calculations. This somewhat inaccurate result demonstrates the difficulty of choosing the correct internal capacitance values of the device, which are critical to the calculations.

PRACTICE PROBLEM 16-22 Given that $C_{iss} = 25 \text{ pF}$, $C_{oss} = 10 \text{ pF}$, and $C_{rss} = 5 \text{ pF}$, determine the values of C_{gd} , C_{gs} , and C_{ds} .

Summary Table 16-1 shows some of the equations used for frequency analysis of a common-emitter BJT amplifier stage and a common-source FET amplifier stage.

Conclusion

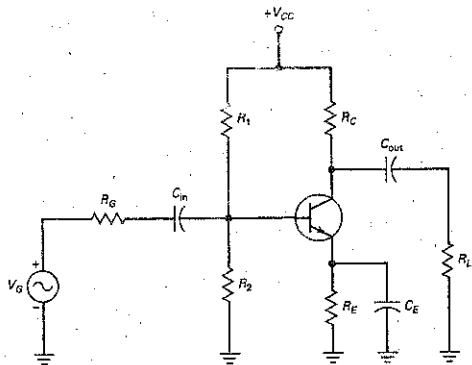
We have examined some of the issues involved in the frequency analysis of discrete BJT and FET amplifier stages. If done manually, the analysis can be tedious and time-consuming. The discussion was deliberately kept somewhat brief here because the frequency analysis of discrete amplifiers is now mainly done on a computer. We hope, you can see how some of the individual components shape the frequency response.

If you need to analyze a discrete amplifier stage, use MultiSim or an equivalent circuit simulator. MultiSim loads all the parameters of the BJT or FET, quantities like C'_C , C'_e , C_{oss} , and C_{iss} , as well as the midband quantities like β , r'_e , and g_m . In other words, MultiSim contains built-in data sheets of devices. For instance, when you select a 2N3904, MultiSim will load all the parameters (including at high frequencies) for a 2N3904. This is a tremendous time saver.

Furthermore, you can use the Bode plotter in MultiSim to see the frequency response. With a Bode plotter, you can measure the midband voltage gain and the cutoff frequencies. In short, using MultiSim or other circuit simulation software is the fastest and most accurate way to analyze the frequency response of a discrete BJT or FET amplifier.

Summary Table 16-1

Amplifier Frequency Analysis

**Low-frequency analysis**

Base input:

$$R = R_g + R_1 \parallel R_2 \parallel R_{in(base)}$$

$$f_1 = \frac{1}{2\pi(R)(C_{in})}$$

Collector output:

$$R = R_c + R_L$$

$$f_1 = \frac{1}{2\pi(R)(C_{out})}$$

Emitter bypass:

$$Z_{out} = R_E \parallel r'_e + \frac{R_1 \parallel R_2 \parallel R_g}{\beta}$$

$$f_1 = \frac{1}{2\pi(R)(C_E)}$$

High-frequency analysis

Base bypass:

$$R = R_g \parallel R_1 \parallel R_2 \parallel R_{in(base)}$$

$$C_{in(M)} = C_C (A_v + 1)$$

$$C = C_E + C_{in(M)}$$

$$f_2 = \frac{1}{2\pi(R)(C)}$$

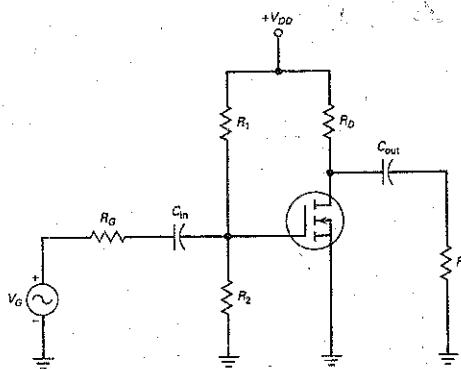
Collector bypass:

$$R = R_c \parallel R_L$$

$$C_{out(M)} = C_C \left(\frac{A_v + 1}{A_v} \right)$$

$$C = C_{ds} + C_{out(M)} + C_{stray}$$

$$f_2 = \frac{1}{2\pi(R)(C)}$$

**Low-frequency analysis**

Gate input:

$$R = R_g + R_1 \parallel R_2$$

$$f_1 = \frac{1}{2\pi(R)(C_{in})}$$

Drain output:

$$R = R_D + R_L$$

$$f_1 = \frac{1}{2\pi(R)(C_{out})}$$

High-frequency analysis

Gate bypass:

$$R = R_g \parallel R_1 \parallel R_2$$

$$C_{in(M)} = C_{gd} (A_v + 1)$$

$$C = C_{gs} + C_{in(M)}$$

$$f_2 = \frac{1}{2\pi(R)(C)}$$

Drain bypass:

$$R = R_D \parallel R_L$$

$$C_{out(M)} = C_{gd} \left(\frac{A_v + 1}{A_v} \right)$$

$$C = C_{ds} + C_{out(M)} + C_{stray}$$

$$f_2 = \frac{1}{2\pi(R)(C)}$$

16-12 Frequency Effects of Surface-Mount Circuits

Stray capacitance and inductance become serious considerations for discrete and IC devices that are operating above 100 kHz. With conventional feed-through components, there are three sources of stray effects:

1. The geometry and internal structure of the device.
2. The printed-circuit layout, including the orientation of the devices and the conductive tracks.
3. The external leads on the device.

Using SM components virtually eliminates item 3 from the list, thus increasing the amount of control design engineers have over stray effects among components on a circuit board.

Summary

SEC. 16-1 FREQUENCY RESPONSE OF AN AMPLIFIER

The frequency response is the graph of voltage gain versus input frequency. An ac amplifier has a lower and an upper cutoff frequency. A dc amplifier has only an upper cutoff frequency. Coupling and bypass capacitors produce the lower cutoff frequency. Internal transistor capacitances and stray-wiring capacitances produce the upper cutoff frequency.

SEC. 16-2 DECIBEL POWER GAIN

Decibel power gain is defined as 10 times the common logarithm of the power gain. When the power gain increases by a factor of 2, the decibel power gain increases by 3 dB. When the power gain increases by a factor of 10, the decibel power gain increases by 10 dB.

SEC. 16-3 DECIBEL VOLTAGE GAIN

Decibel voltage gain is defined as 20 times the common logarithm of the voltage gain. When the voltage gain increases by a factor of 2, the decibel voltage gain

increases by 6 dB. When the voltage gain increases by a factor of 10, the decibel voltage gain increases by 20 dB. The total decibel voltage gain of cascaded stages equals the sum of the individual decibel voltage gains.

SEC. 16-4 IMPEDANCE MATCHING

In many systems, all impedances are matched because this produces maximum power transfer. In an impedance-matched system, the decibel power gain and the decibel voltage gain are equal.

SEC. 16-5 DECIBELS ABOVE A REFERENCE

Besides using decibels with power and voltage gains, we can use decibels above a reference. Two popular references are the milliwatt and the volt. Decibels with the 1 milliwatt reference are labeled dBm, and decibels with the 1 volt reference are labeled dBV.

SEC. 16-6 BODE PLOTS

An octave refers to a factor of 2 change of frequency. A decade refers to a factor of 10 change in frequency. A graph of

decibel voltage gain versus frequency is called a Bode plot. Ideal Bode plots are approximations that allow us to draw the frequency response quickly and easily.

SEC. 16-7 MORE BODE PLOTS

In a lag circuit, the voltage gain breaks at the upper cutoff frequency and then rolls off at a rate of 20 dB per decade, equivalent to 6 dB per octave. We can also draw a Bode plot of phase angle versus frequency. With a lag circuit, the phase angle is between 0 and -90° .

SEC. 16-8 THE MILLER EFFECT

A feedback capacitor from the output to the input of an inverting amplifier is equivalent to two capacitors. One capacitor is across the input terminals, and the other is across the output terminals. The Miller effect refers to the input capacitance being $A_v + 1$ times the feedback capacitance.

SEC. 16-9 RISETIME-BANDWIDTH RELATIONSHIP

When a voltage step is used as the input to a dc amplifier, the risetime of the output is the time between the 10 and

90 percent points. The upper cutoff frequency equals 0.35 divided by the risetime. This gives us a quick and easy way to measure the bandwidth of a dc amplifier.

16-10 FREQUENCY ANALYSIS OF BJT STAGES

The input coupling capacitor, output coupling capacitor, and emitter bypass capacitor produce the low cutoff

frequencies. The collector bypass capacitor and the input Miller capacitance produce the high cutoff frequencies. Frequency analysis of bipolar and FET stages is typically done with MultiSim or an equivalent circuit simulator.

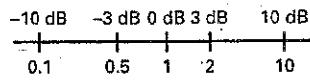
frequencies (like a BJT stage). The drain bypass capacitances, along with the gate capacitance and input Miller capacitance, produce the high cutoff frequencies. Frequency analysis of BJT and FET stages are typically done with MultiSim or an equivalent circuit simulator.

16-11 FREQUENCY ANALYSIS OF FET STAGES

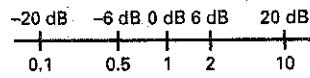
The input and output coupling capacitors of a FET stage produce the low cutoff

Definitions

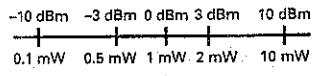
(16-8) Decibel power gain:



(16-9) Decibel voltage gain:



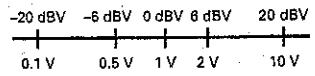
(16-16) Decibels referenced to 1 mW:



$$A_p(\text{dB}) = 10 \log A_p$$

$$P_{\text{dBm}} = 10 \log \frac{P}{1 \text{ mW}}$$

(16-18) Decibels referenced to 1 V:

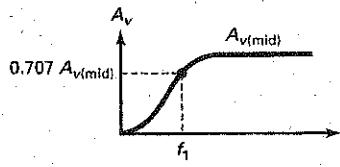


$$A_v(\text{dB}) = 20 \log A_v$$

$$V_{\text{dBV}} = 20 \log V$$

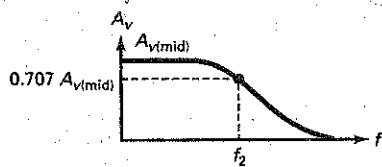
Derivations

(16-3) Below the midband:



$$A_v = \frac{A_v(\text{mid})}{\sqrt{1 + (f_1/f)^2}}$$

(16-4) Above the midband:



$$A_v = \frac{A_v(\text{mid})}{\sqrt{1 + (f/f_2)^2}}$$

(16-10) Total voltage gain:



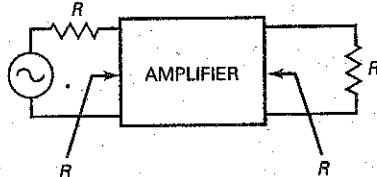
$$A_v = (A_v1)(A_v2)$$

(16-11) Total decibel voltage gain:



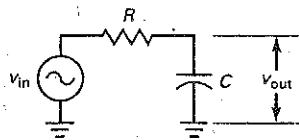
$$A_v(\text{dB}) = A_v1(\text{dB}) + A_v2(\text{dB})$$

(16-13) Impedance-matched system:



$$A_p(\text{dB}) = A_v(\text{dB})$$

(16-22) Cutoff frequency:

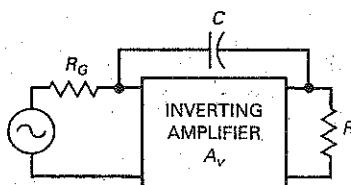


$$f_2 = \frac{1}{2\pi RC}$$

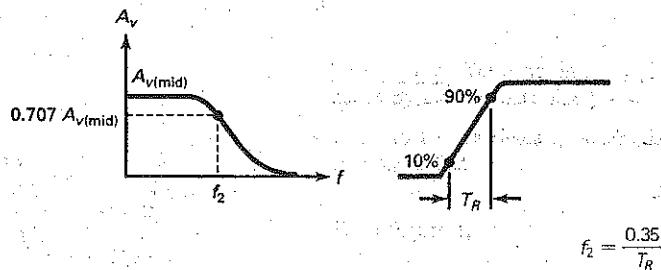
(16-26) Miller effect: $C_{in(M)} = C(A_v + 1)$

and

$$(16-27) C_{out(M)} = C \left(\frac{A_v + 1}{A_v} \right)$$



(16-29) Risetime-bandwidth:



Student Assignments

1. Frequency response is a graph of voltage gain versus
 - a. Frequency
 - b. Power gain
 - c. Input voltage
 - d. Output voltage
2. At low frequencies, the coupling capacitors produce a decrease in
 - a. Input resistance
 - b. Voltage gain
 - c. Generator resistance
 - d. Generator voltage
3. The stray-wiring capacitance has an effect on the
 - a. Lower cutoff frequency
 - b. Midband voltage gain
 - c. Upper cutoff frequency
 - d. Input resistance
4. At the lower or upper cutoff frequency, the voltage gain is
 - a. $0.35A_{v(\text{mid})}$
 - b. $0.5A_{v(\text{mid})}$
 - c. $0.707A_{v(\text{mid})}$
 - d. $0.995A_{v(\text{mid})}$
5. If the power gain doubles, the decibel power gain increases by
 - a. A factor of 2
 - b. 3 dB
 - c. 6 dB
 - d. 10 dB
6. If the voltage gain doubles, the decibel voltage gain increases by
 - a. A factor of 2
 - b. 3 dB
 - c. 6 dB
 - d. 10 dB

7. If the voltage gain is 10, the decibel voltage gain is
- 6 dB
 - 20 dB
 - 40 dB
 - 60 dB
8. If the voltage gain is 100, the decibel voltage gain is
- 6 dB
 - 20 dB
 - 40 dB
 - 60 dB
9. If the voltage gain is 2000, the decibel voltage gain is
- 40 dB
 - 46 dB
 - 66 dB
 - 86 dB
10. Two stages have decibel voltage gains of 20 and 40 dB. The total ordinary voltage gain is
- 1
 - 10
 - 100
 - 1000
11. Two stages have voltage gains of 100 and 200. The total decibel voltage gain is
- 46 dB
 - 66 dB
 - 86 dB
 - 106 dB
12. One frequency is 8 times another frequency. How many octaves apart are the two frequencies?
- 1
 - 2
 - 3
 - 4
13. If $f_1 = 1 \text{ MHz}$, and $f_2 = 10 \text{ Hz}$, the ratio f_1/f_2 represents how many decades?
- 2
 - 3
 - 4
 - 5
14. Semilogarithmic paper means that
- One axis is linear, and the other is logarithmic
 - One axis is linear, and the other is semilogarithmic
 - Both axes are semilogarithmic
 - Neither axis is linear
15. If you want to improve the high-frequency response of an amplifier, which of these approaches would you try?
- Decrease the coupling capacitances
 - Increase the emitter bypass capacitance
 - Shorten leads as much as possible
 - Increase the generator resistance
16. The voltage gain of an amplifier decreases 20 dB per decade above 20 kHz. If the midband voltage gain is 86 dB, what is the ordinary voltage gain at 20 MHz?
- 20
 - 200
 - 2000
 - 20,000
17. In a BJT amplifier circuit, C_e is the same as
- C_{be}
 - C_b
 - C_{bo}
 - Any of the above
18. In a BJT amplifier circuit, increasing the value of C_{in} and C_{out} will
- Decrease A_v at low frequencies
 - Increase A_v at low frequencies
 - Decrease A_v at high frequencies
 - Increase A_v at high frequencies
19. Input coupling capacitors in FET circuits
- Are normally larger than in BJT circuits
 - Determine the high-frequency cutoff value
 - Are normally smaller than in BJT circuits
 - Are treated as ac opens
20. On FET data sheets, C_{oss} is
- Equal to $C_{ds} + C_{gd}$
 - Equal to $C_{gs} - C_{rss}$
 - Equal to C_{gd}
 - Equal to $C_{iss} - C_{rss}$

Problems

SEC. 16-1 FREQUENCY RESPONSE OF AN AMPLIFIER

- 16-1 An amplifier has a midband voltage gain of 1000. If cutoff frequencies are $f_1 = 100 \text{ Hz}$ and $f_2 = 100 \text{ kHz}$, what does the frequency response look like? What is the voltage gain if the input frequency is 20 Hz? If it is 300 kHz?
- 16-2 Suppose an op amp has a midband voltage gain of 500,000. If the upper cutoff frequency is 15 Hz, what does the frequency response look like?
- 16-3 A dc amplifier has a midband voltage gain of 200. If the upper cutoff frequency is 10 kHz, what is the voltage gain for each of these input frequencies: 100 kHz, 200 kHz, 500 kHz, and 1 MHz?

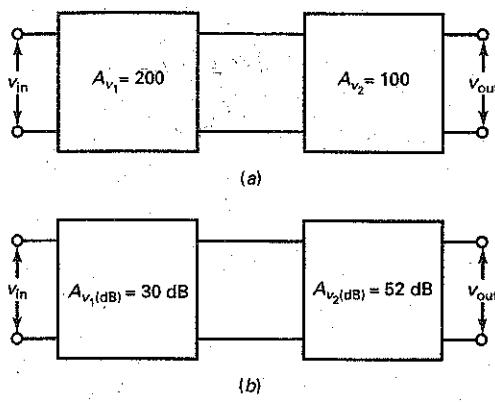
SEC. 16-2 DECIBEL POWER GAIN

- 16-4 Calculate the decibel power gain for $A_p = 5, 10, 20$, and 40.
- 16-5 Calculate the decibel power gain for $A_p = 0.4, 0.2, 0.1$, and 0.05.
- 16-6 Calculate the decibel power gain for $A_p = 2, 20, 200$, and 2000.
- 16-7 Calculate the decibel power gain for $A_p = 0.4, 0.04$, and 0.004.

SEC. 16-3 DECIBEL VOLTAGE GAIN

- 16-8 What is the total voltage gain in Fig. 16-34a? Convert the answer to decibels.

Figure 16-34



- 16-9 Convert each stage gain in Fig. 16-34a to decibels.
- 16-10 What is the total decibel voltage gain in Fig. 16-34b? Convert this to ordinary voltage gain.
- 16-11 What is the ordinary voltage gain of each stage in Fig. 16-34b?
- 16-12 What is the decibel voltage gain of an amplifier if it has an ordinary voltage gain of 100,000?
- 16-13 The data sheet of an LM380, an audio power amplifier, gives a decibel voltage gain of 34 dB. Convert this to ordinary voltage gain.
- 16-14 A two-stage amplifier has these stage gains: $A_{v1} = 25.8$ and $A_{v2} = 117$. What is the decibel voltage gain of each stage? The total decibel voltage gain?

SEC. 16-4 IMPEDANCE MATCHING

16-15 If Fig. 16-35 is an impedance-matched system, what is the total decibel voltage gain? The decibel voltage gain of each stage?

16-16 If the stages of Fig. 16-35 are impedance-matched, what is the load voltage? The load power?

SEC. 16-5 DECIBELS ABOVE A REFERENCE

16-17 If the output power of a preamplifier is 20 dBm, how much power is this in milliwatts?

16-18 How much output voltage does a microphone have when its output is -45 dBV?

16-19 Convert the following powers to dBm: 25 mW, 93.5 mW, and 4.87 W.

16-20 Convert the following voltages to dBV: 1 μ V, 34.8 mV, 12.9 V, and 345 V.

SEC. 16-6 BODE PLOTS

16-21 The data sheet of an op amp gives a midband voltage gain of 200,000, a cutoff frequency of 10 Hz, and a roll-off rate of 20 dB per decade. Draw the ideal Bode plot. What is the ordinary voltage gain at 1 MHz?

16-22 The LF351 is an op amp with a voltage gain of 316,000, a cutoff frequency of 40 Hz, and a roll-off rate of 20 dB per decade. Draw the ideal Bode plot.

SEC. 16-7 MORE BODE PLOTS

16-23 **III Multisim** Draw the ideal Bode plot for the lag circuit of Fig. 16-36a.

16-24 **III Multisim** Draw the ideal Bode plot for the lag circuit of Fig. 16-36b.

16-25 What is the ideal Bode plot for the stage of Fig. 16-37?

Figure 16-35

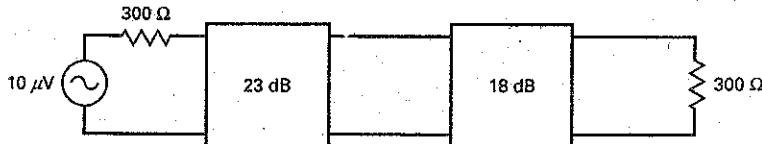


Figure 16-36

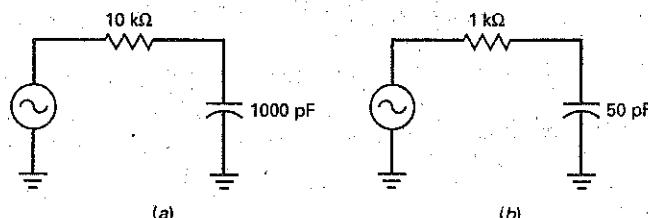
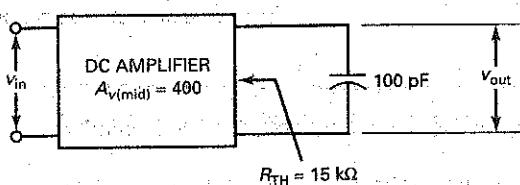


Figure 16-37



SEC. 16-8 THE MILLER EFFECT

- 16-26 What is the input Miller capacitance in Fig. 16-38 if $C = 5 \text{ pF}$ and $A_v = 200,000$?
- 16-27 Draw the ideal Bode plot for the input lag circuit of Fig. 16-38 with $A_v = 250,000$ and $C = 15 \text{ pF}$.
- 16-28 If the feedback capacitor of Fig. 16-38 is 50 pF , what is the input Miller capacitance when $A_v = 200,000$?
- 16-29 Draw the ideal Bode plot for Fig. 16-38 with a feedback capacitance of 100 pF and a voltage gain of $150,000$.

SEC. 16-9 RISETIME-BANDWIDTH RELATIONSHIP

- 16-30 An amplifier has the step response shown in Fig. 16-39a. What is its upper cutoff frequency?
- 16-31 What is the bandwidth of an amplifier if the risetime is $0.25 \mu\text{s}$?
- 16-32 The upper cutoff frequency of an amplifier is 100 kHz . If it is square-wave tested, what would the risetime of the amplifier output be?
- 16-33 In Fig. 16-40, what is the low-cut-off frequency for the base coupling circuit?

Figure 16-38

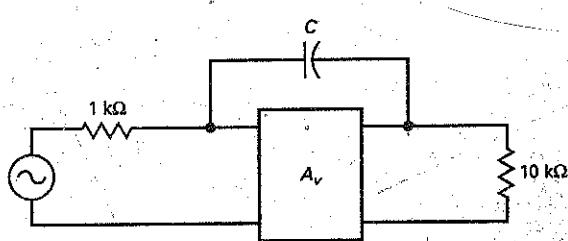


Figure 16-39

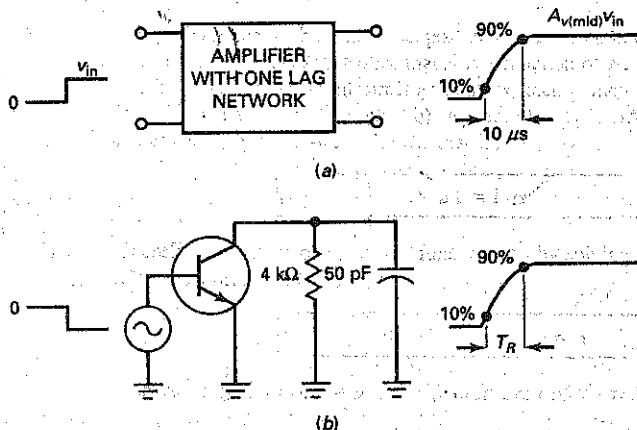
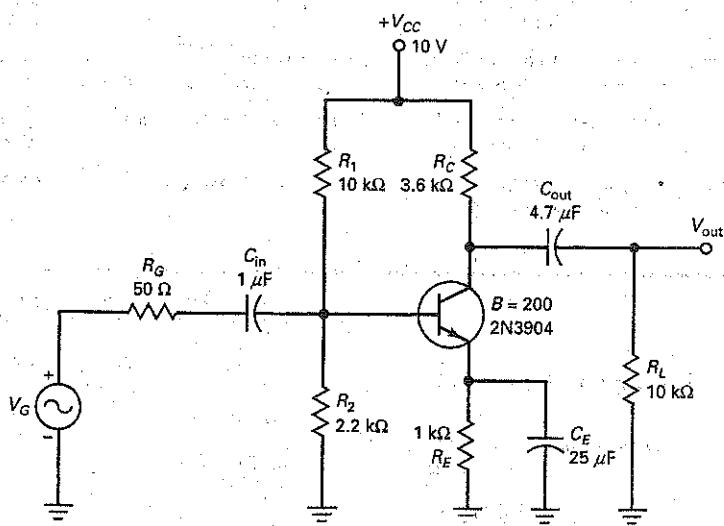


Figure 16-40



16-34 In Fig. 16-40, what is the low-cutoff frequency for the collector coupling circuit?

16-35 In Fig. 16-40, what is the low-cutoff frequency for the emitter bypass circuit?

16-36 In Fig. 16-40, C_C is given as $2\ pF$, $C_E = 10\ pF$, and C_{stray} is $5\ pF$. Determine the high-frequency cutoff values for both base-input and collector-output circuits.

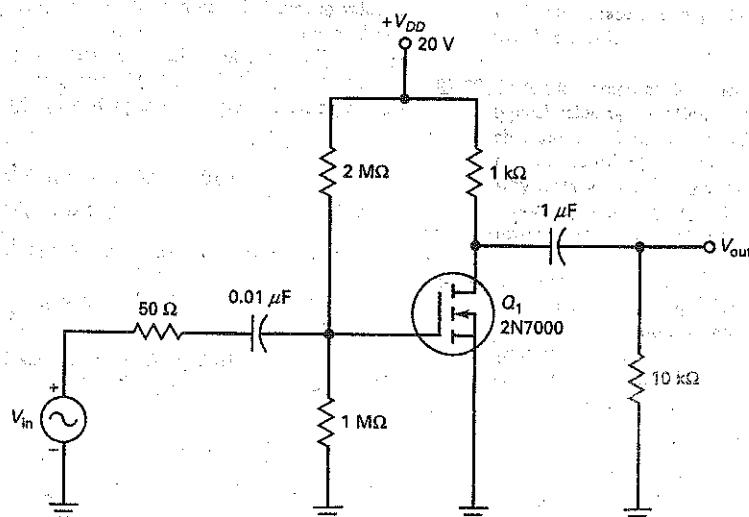
16-37 The circuit of Fig. 16-41 uses an E-MOSFET with these specifications: $g_m = 16.5\ mS$, $C_{iss} = 30\ pF$, $C_{oss} = 20\ pF$,

and $C_{rss} = 5.0\ pF$. Determine the FET's internal capacitance values for C_{gd} , C_{gs} , and C_{ds} .

16-38 In Fig. 16-41, what is the dominant low-cutoff frequency?

16-39 In Fig. 16-41, determine the high-frequency cutoff values for both gate input and drain output circuits.

Figure 16-41



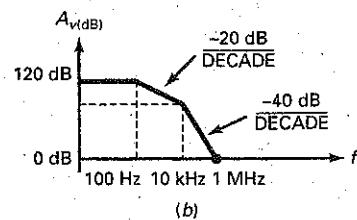
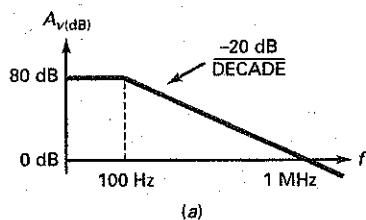
Critical Thinking

- 16-40 In Fig. 16-42a, what is the decibel voltage gain when $f = 20 \text{ kHz}$? When $f = 44.4 \text{ kHz}$?
- 16-41 In Fig. 16-42b, what is the decibel voltage gain when $f = 100 \text{ kHz}$?
- 16-42 The amplifier of Fig. 16-39a has a midband voltage gain of 100. If the input voltage is a step of 20 mV, what is the output voltage at the 10 percent point? The 90 percent point?

- 16-43 Figure 16-39b is an equivalent circuit. What is the risetime of the output voltage?

- 16-44 You have two data sheets for amplifiers. The first shows a cutoff frequency of 1 MHz. The second gives a risetime of 1 μs . Which amplifier has the greater bandwidth?

Figure 16-42



Job Interview Questions

- This morning I breadboarded an amplifier stage and used a lot of wire. The upper cutoff frequency tested much lower than it should be. Do you have any suggestions?
- On my lab bench is a dc amplifier, an oscilloscope, and a function generator that can produce sine, square, or triangular waves. Tell me how to find the bandwidth of the amplifier.
- Without using your calculator, I want you to convert a voltage gain of 250 to its decibel equivalent.
- I would like you to draw an inverting amplifier with a feedback capacitor of 50 pF and a voltage gain of 10,000. Next, I want you to draw the ideal Bode plot for the input lag circuit.
- Assume that the front panel of your oscilloscope notes that its vertical amplifier has a risetime of 7 ns. What does this say about the bandwidth of the instrument?
- How would you measure the bandwidth of a dc amplifier?
- Why does the decibel voltage gain use a factor of 20 but the power gain uses a factor of 10?
- Why is impedance matching important in some systems?
- What is the difference between dB and dBm?
- Why is a dc amplifier called a dc amplifier?
- A radio station engineer needs to test the voltage gain over several decades. What type of graph paper would be most useful in this situation?
- Have you ever heard of MultiSim (EWB)? If so, what is it?

Self-Test Answers

- | | | |
|------|-------|-------|
| 1. a | 8. c | 15. c |
| 2. b | 9. c | 16. a |
| 3. c | 10. d | 17. d |
| 4. c | 11. c | 18. b |
| 5. b | 12. c | 19. c |
| 6. c | 13. d | 20. a |
| 7. b | 14. a | |

Practice Problem Answers

- 16-1 $A_{V(\text{mid})} = 70.7$; A_V at 5 Hz = 24.3; A_V at 200 kHz = 9.95
- 16-2 A_V at 10 Hz = 141
- 16-3 20,000 at 100 Hz; 2000 at 1 kHz; 200 at 10 kHz; 20 at 100 kHz; 2.0 at 1 MHz
- 16-4 10 A_p = 10 dB; 20 A_p = 13 dB; 40 A_p = 16 dB
- 16-5 4 A_p = 6 dB; 2 A_p = 3 dB; 1 A_p = 0 dB; 0.5 A_p = -3 dB
- 16-6 5 A_p = 7 dB; 50 A_p = 17 dB; 500 A_p = 27 dB; 5000 A_p = 37 dB
- 16-7 20 A_p = 13 dB; 2 A_p = 3 dB; 0.2 A_p = -7 dB; 0.02 A_p = -17 dB
- 16-8 50 A_V = 34 dB; 200 A_V = 46 dB; $A_{V(\text{dB})}$ = 10,000; $A_{V(\text{dB})}$ = 80 dB
- 16-9 $A_{V(\text{dB})}$ = 30 dB; A_p = 1,000; A_V = 31.6
- 16-10 $A_{V1} = 3.16$; $A_{V2} = 0.5$; $A_{V3} = 20$
- 16-11 $P = 1,000 \text{ W}$
- 16-12 $V_{\text{out}} = 1.88 \text{ mV}$
- 16-14 $f_2 = 159 \text{ kHz}$
- 16-15 $f_2 = 318 \text{ kHz}$; $f_{\text{unity}} = 31.8 \text{ MHz}$
- 16-17 $C_{\text{in}(M)} = 0.3 \mu\text{F}$; $C_{\text{out}(M)} = 30 \text{ pF}$
- 16-18 $T_R = 440 \text{ ns}$; $f_2 = 795 \text{ kHz}$
- 16-19 $f_1 = 63 \text{ Hz}$
- 16-20 $f_2 = 1.43 \text{ MHz}$
- 16-22 $C_{gd} = 5 \text{ pF}$; $C_{gs} = 20 \text{ pF}$; $C_{ds} = 5 \text{ pF}$

17 Differential Amplifiers

- The term **operational amplifier (op amp)** refers to an amplifier that performs a mathematical operation. Historically, the first op amps were used in analog computers, where they did addition, subtraction, multiplication, and so on. At one time, op amps were built as discrete circuits. Now, most op amps are integrated circuits (ICs).

The typical op amp is a dc amplifier with very high voltage gain, very high input impedance, and very low output impedance. The unity-gain frequency is from 1 to more than 20 MHz, depending on the part number. An IC op amp is a complete functional block with external pins. By connecting these pins to supply voltages and a few components, we can quickly build all kinds of useful circuits.

The input circuit used in most op amps is the differential amplifier. This amplifier configuration establishes many of the IC's input characteristics. The differential amplifier may also be configured in a discrete form to be used in communications, instrumentation, and industrial control circuits. This chapter will focus on the differential amplifier used in ICs.

Chapter Outline

- 17-1** The Differential Amplifier
- 17-2** DC Analysis of a Diff Amp
- 17-3** AC Analysis of a Diff Amp
- 17-4** Input Characteristics of an Op.Amp
- 17-5** Common-Mode Gain
- 17-6** Integrated Circuits
- 17-7** The Current Mirror
- 17-8** The Loaded Diff Amp

Objectives

After studying this chapter, you should be able to:

- Perform a dc analysis of a differential amplifier.
- Perform an ac analysis of a differential amplifier.
- Define input bias current, input offset current, and input offset voltage.
- Explain common-mode gain and common-mode rejection ratio.
- Describe how integrated circuits are manufactured.
- Apply Thevenin's theorem to a loaded differential amplifier.

Vocabulary

active load resistor	differential input	inverting input
common-mode rejection ratio (CMRR)	differential output	monolithic IC
common-mode signal	hybrid IC	noninverting input
compensating diode	input bias current	operational amplifier (op amp)
current mirror	input offset current	single-ended
differential amplifier (diff amp)	input offset voltage	tail current
	integrated circuit (IC)	

17-1 The Differential Amplifier

Transistors, diodes, and resistors are the only practical components in typical ICs. Capacitors may also be used, but they are small, usually less than 50 pF. For this reason, IC designers cannot use coupling and bypass capacitors the way a discrete circuit designer can. Instead, the IC designer has to use direct coupling between stages and also needs to eliminate the emitter bypass capacitor without losing too much voltage gain.

The **differential amplifier (diff amp)** is the key. The design of this circuit is extremely clever because it eliminates the need for an emitter bypass capacitor. For this and other reasons, the diff amp is used as the input stage of almost every IC op. amp.

Differential Input and Output

Figure 17-1 shows a diff amp. It is two CE stages in parallel with a common emitter resistor. Although it has two input voltages (v_1 and v_2) and two collector voltages (v_{c1} and v_{c2}), the overall circuit is considered to be one stage. Because there are no coupling or bypass capacitors, there is no lower cutoff frequency.

The ac output voltage v_{out} is defined as the voltage between the collectors with the polarity shown in Fig. 17-1:

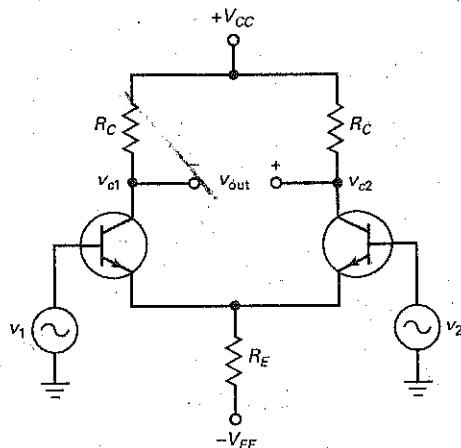
$$v_{out} = v_{c2} - v_{c1} \quad (17-1)$$

This voltage is called a **differential output** because it combines the two ac collector voltages into one voltage that equals the difference of the collector voltages. Note: We will use lowercase letters for v_{out} , v_{c1} , and v_{c2} because they are ac voltages that include zero hertz (0 Hz) as a special case.

Ideally, the circuit has identical transistors and equal collector resistors. With perfect symmetry, v_{out} is zero when the two input voltages are equal. When v_1 is greater than v_2 , the output voltage has the polarity shown in Fig. 17-1. When v_2 is greater than v_1 , the output voltage is inverted and has the opposite polarity.

The diff amp of Fig. 17-1 has two separate inputs. Input v_1 is called the **noninverting input** because v_{out} is in phase with v_1 . On the other hand, v_2 is called the **inverting input** because v_{out} is 180° out of phase with v_2 . In some applications, only the noninverting input is used and the inverting input is grounded. In

Figure 17-1 Differential input and differential output.



other applications, only the inverting input is active and the noninverting input is grounded.

When both the noninverting and inverting input voltages are present, the total input is called a **differential input** because the output voltage equals the voltage gain times the difference of the two input voltages. The equation for the output voltage is:

$$v_{\text{out}} = A_v(v_1 - v_2) \quad (17-2)$$

where A_v is the voltage gain. We will derive the equation for voltage gain in Sec. 17-3.

Single-Ended Output

A differential output like that of Fig. 17-1 requires a floating load because neither end of the load can be grounded. This is inconvenient in many applications since loads are often **single-ended**; that is, one end is grounded.

Figure 17-2a shows a widely used form of the diff amp. This has many applications because it can drive single-ended loads like CE stages, emitter followers, and other circuits. As you can see, the ac output signal is taken from the collector on the right side. The collector resistor on the left has been removed because it serves no useful purpose.

Because the input is differential, the ac output voltage is still given by $A_v(v_1 - v_2)$. With a single-ended output, however, the voltage gain is half as much as with a differential output. We get half as much voltage gain with a single-ended output because the output is coming from only one of the collectors.

Incidentally, Fig. 17-2b shows the block-diagram symbol for a diff amp with a differential input and a single-ended output. The same symbol is used for

Figure 17-2 (a) Differential input and single-ended output; (b) block diagram symbol.

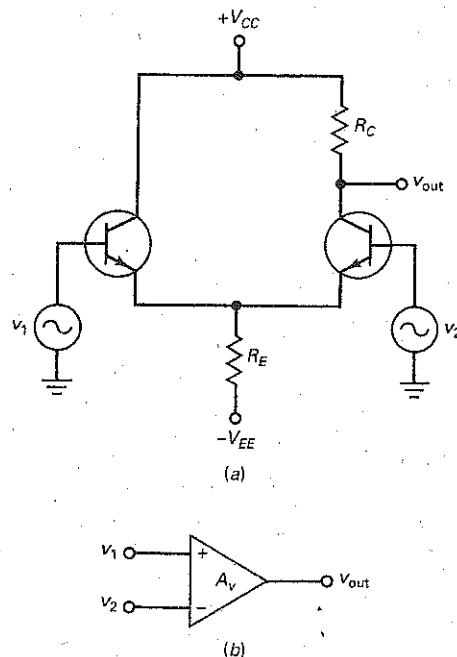
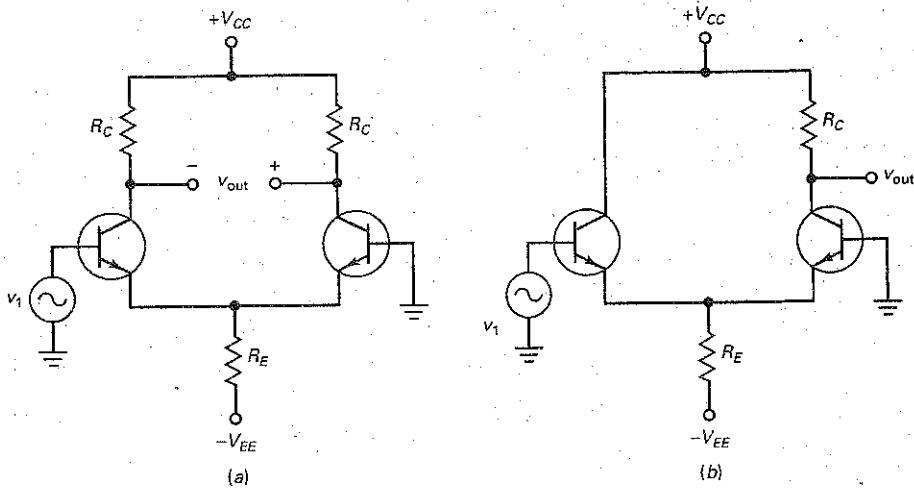


Figure 17-3 (a) Noninverting input and differential output; (b) noninverting input and single-ended output.



an op amp. The plus sign (+) represents the noninverting input, and the minus sign (-) is the inverting input.

Noninverting-Input Configurations

Often, only one of the inputs is active and the other is grounded, as shown in Fig. 17-3a. This configuration has a noninverting input and a differential output. Since $v_2 = 0$, Eq. (17-2) gives:

$$v_{\text{out}} = A_v (v_1) \quad (17-3)$$

Figure 17-3b shows another configuration for the diff amp. This one has a noninverting input and a single-ended output. Since v_{out} is the ac output voltage, Eq. (17-3) is still valid, but the voltage gain A_v will be half as much because the output is taken from only one side of the diff amp.

Inverting-Input Configurations

In some applications, v_2 is the active input and v_1 is the grounded input, as shown in Fig. 17-4a. In this case, Eq. (17-2) simplifies to:

$$v_{\text{out}} = -A_v (v_2) \quad (17-4)$$

The minus sign in Eq. (17-4) indicates phase inversion.

Figure 17-4b shows the final configuration that we will discuss. Here we are using the inverting input with a single-ended output. In this case, the ac output voltage is still given by Eq. (17-4).

Conclusion

Table 17-1 summarizes the four basic configurations of a diff amp. The general case has a differential input and differential output. The remaining cases are subsets of the general case. For instance, to get single-ended input operation, one of the inputs is used and the other is grounded. When the input is single-ended, either the noninverting input v_1 or the inverting input v_2 may be used.

Figure 17-4 (a) Inverting input and differential output; (b) inverting input and single-ended output.

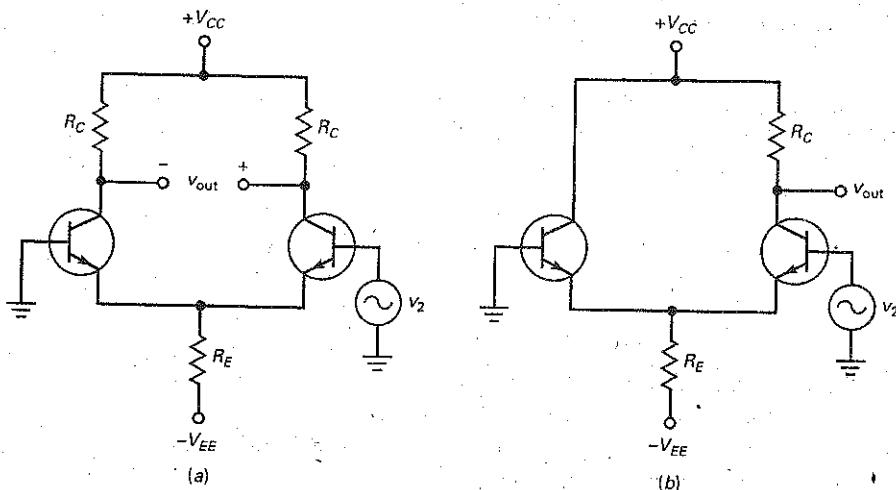


Table 17-1 Diff-Amp Configurations

Input	Output	v_{in}	v_{out}
Differential	Differential	$v_1 - v_2$	$v_{c2} - v_{c1}$
Differential	Single-ended	$v_1 - v_2$	v_{c2}
Single-ended	Differential	v_1 or v_2	$v_{c2} - v_{c1}$
Single-ended	Single-ended	v_1 or v_2	v_{c2}

17-2 DC Analysis of a Diff Amp

Figure 17-5a shows the dc equivalent circuit for a diff amp. Throughout this discussion, we will assume identical transistors and equal collector resistors. Also, both bases are grounded in this preliminary analysis.

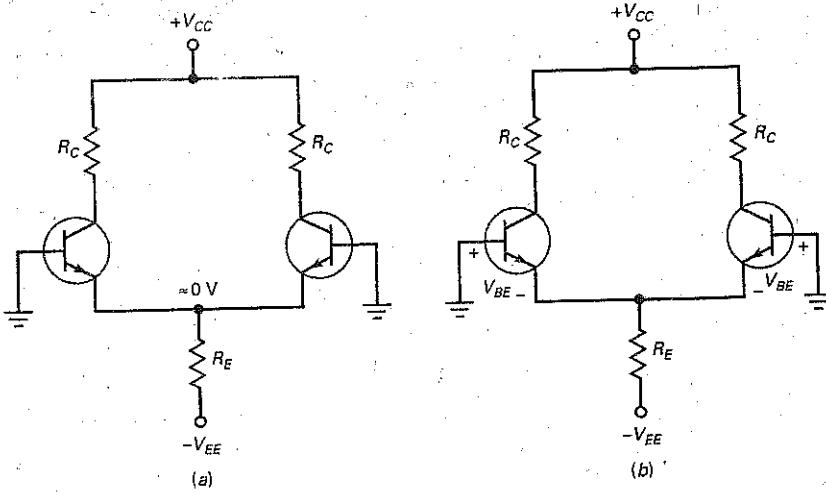
The bias used here should look familiar. It is almost identical to the two-supply emitter bias (TSEB) discussed in Chap. 8. If you recall, most of the negative supply voltage in a TSEB circuit appears across the emitter resistor. This sets up a fixed emitter current.

Ideal Analysis

A diff amp is sometimes called a *long-tail pair* because the two transistors share a common resistor R_E . The current through this common resistor is called the **tail current**. If we ignore the V_{BE} drops across the emitter diodes of Fig. 17-5a, then the top of the emitter resistor is ideally a dc ground point. In this case, all of V_{EE} appears across R_E and the tail current is:

$$I_T = \frac{V_{EE}}{R_E} \quad (17-5)$$

Figure 17-5 (a) Ideal dc analysis; (b) second approximation.



This equation is fine for troubleshooting and preliminary analysis because it quickly gets to the point, which is that almost all the emitter supply voltage appears across the emitter resistor.

When the two halves of Fig. 17-5a are perfectly matched, the tail current will split equally. Therefore, each transistor has an emitter current of:

$$I_E = \frac{I_T}{2} \quad (17-6)$$

The dc voltage on either collector is given by this familiar equation:

$$V_C = V_{CC} - I_C R_C \quad (17-7)$$

Second Approximation

We can improve the dc analysis by including the V_{BE} drop across each emitter diode. In Fig. 17-5b, the voltage at the top of the emitter resistor is one V_{BE} drop below ground. Therefore, the tail current is:

$$I_T = \frac{V_{EE} - V_{BE}}{R_E} \quad (17-8)$$

where $V_{BE} = 0.7$ V for silicon transistors.

Effect of Base Resistors on Tail Current

In Fig. 17-5b, both bases are grounded for simplicity. When base resistors are used, they have a negligible effect on the tail current in a well-designed diff amp. Here is the reason: When base resistors are included in the analysis, the equation for tail current becomes:

$$I_T = \frac{V_{EE} - V_{BE}}{R_E + R_B/2\beta_{dc}}$$

In any practical design, $R_B/2\beta_{dc}$ is less than 1 percent of R_E . This is why we prefer using either Eq. (17-5) or Eq. (17-8) to calculate tail current.

Although base resistors have a negligible effect on the tail current, they can produce input error voltages when the two halves of the diff amp are not perfectly symmetrical. We will discuss these input error voltages in a later section.

Example 17-1

What are the ideal currents and voltages in Fig. 17-6a?

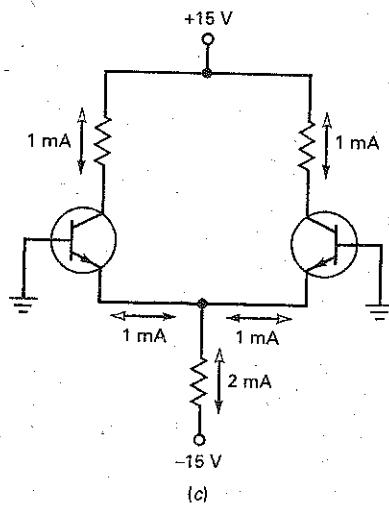
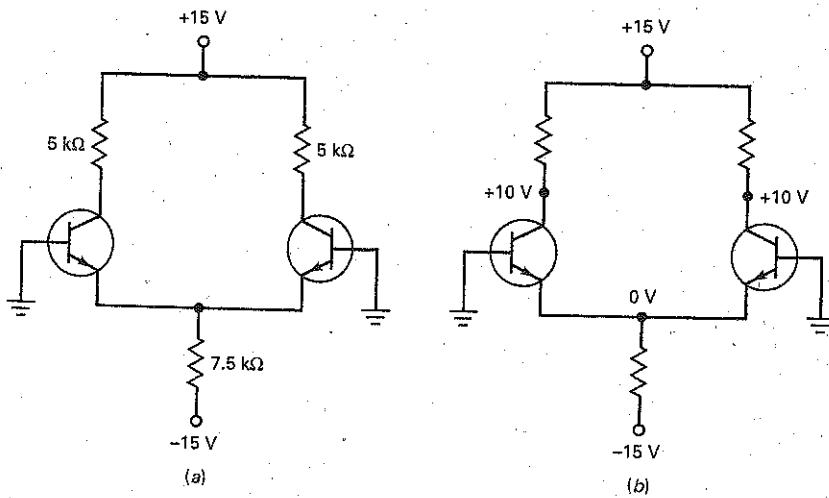
SOLUTION With Eq. (17-5), the tail current is:

$$I_T = \frac{15 \text{ V}}{7.5 \text{ k}\Omega} = 2 \text{ mA}$$

Each emitter current is half of the tail current:

$$I_E = \frac{2 \text{ mA}}{2} = 1 \text{ mA}$$

Figure 17-6 Example.



Each collector has a quiescent voltage of approximately:

$$V_C = 15 \text{ V} - (1 \text{ mA})(5 \text{ k}\Omega) = 10 \text{ V}$$

Figure 17-6b shows the dc voltages, and Fig. 17-6c shows the currents. (Note: The standard arrowhead indicates conventional flow, and the triangular arrowhead indicates electron flow.)

PRACTICE PROBLEM 17-1 In Fig. 17-6a, change R_E to 5 k Ω and find the ideal currents and voltages.

Example 17-2

MultiSim

Recalculate the currents and voltages for Fig. 17-6a using the second approximation.

SOLUTION The tail current is:

$$I_T = \frac{15 \text{ V} - 0.7 \text{ V}}{7.5 \text{ k}\Omega} = 1.91 \text{ mA}$$

Each emitter current is half of the tail current:

$$I_E = \frac{1.91 \text{ mA}}{2} = 0.955 \text{ mA}$$

and each collector has a quiescent voltage of:

$$V_C = 15 \text{ V} - (0.955 \text{ mA})(5 \text{ k}\Omega) = 10.2 \text{ V}$$

As you can see, the answers change only slightly when the second approximation is used. In fact, if the same circuit is built and tested with MultiSim (EWB), the following answers result with 2N3904 transistors:

$$I_T = 1.912 \text{ mA}$$

$$I_E = 0.956 \text{ mA}$$

$$I_C = 0.950 \text{ mA}$$

$$V_C = 10.25 \text{ V}$$

These answers are almost the same as the second approximation and not much different from the ideal answers. The point is that ideal analysis is adequate for many situations. If you need more accuracy, use either the second approximation or MultiSim analysis.

PRACTICE PROBLEM 17-2 Repeat Example 17-2 using a 5 k Ω emitter resistor.

Example 17-3

MultiSim

What are the currents and voltages in the single-ended output circuit of Fig. 17-7a?

SOLUTION Ideally, the tail current is:

$$I_T = \frac{12 \text{ V}}{5 \text{ k}\Omega} = 2.4 \text{ mA}$$

Each emitter current is half of the tail current:

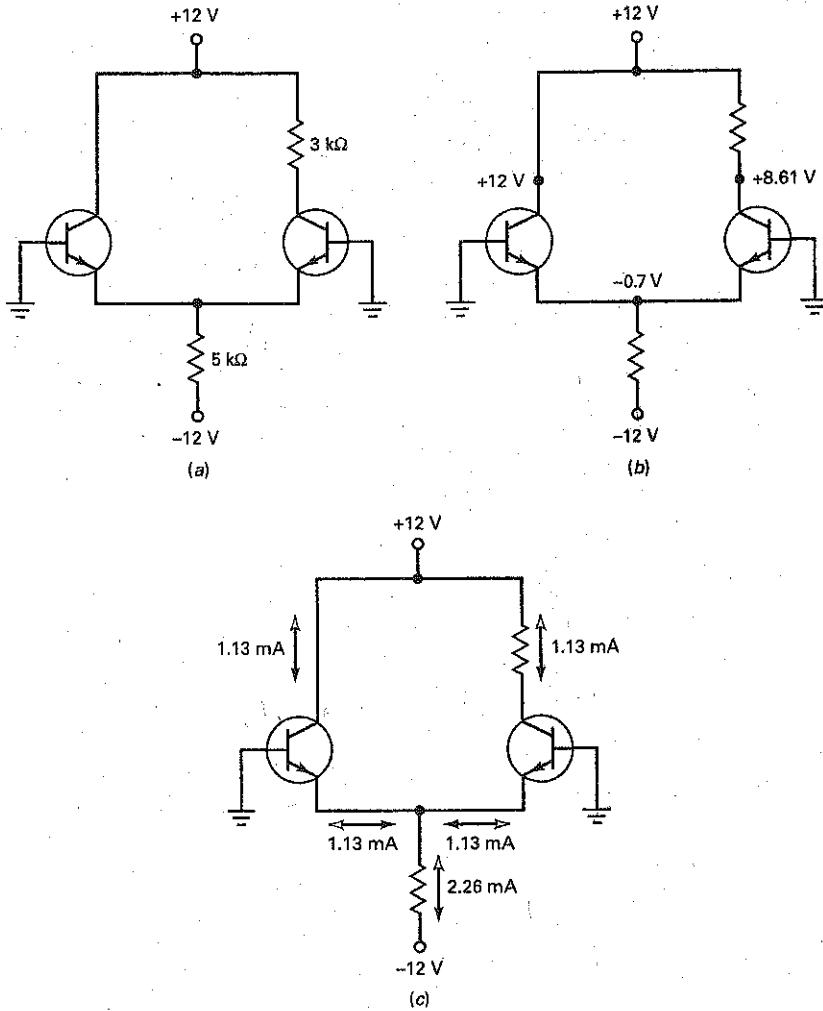
$$I_E = \frac{2.4 \text{ mA}}{2} = 1.2 \text{ mA}$$

The collector on the right has a quiescent voltage of approximately:

$$V_C = 12 \text{ V} - (1.2 \text{ mA})(3 \text{ k}\Omega) = 8.4 \text{ V}$$

and the one on the left has 12 V.

Figure 17-7 Example.



With the second approximation, we can calculate:

$$I_T = \frac{12 \text{ V} - 0.7 \text{ V}}{5 \text{ k}\Omega} = 2.26 \text{ mA}$$

$$I_E = \frac{2.26 \text{ mA}}{2} = 1.13 \text{ mA}$$

$$V_C = 12 \text{ V} - (1.13 \text{ mA})(3 \text{ k}\Omega) = 8.61 \text{ V}$$

Figure 17-7b shows the dc voltages, and Fig. 17-7c shows the currents for the second approximation.

PRACTICE PROBLEM 17-3 In Fig. 17-7a, change R_E to 3 kΩ. Determine the currents and voltages with the second approximation.

17-3 AC Analysis of a Diff Amp

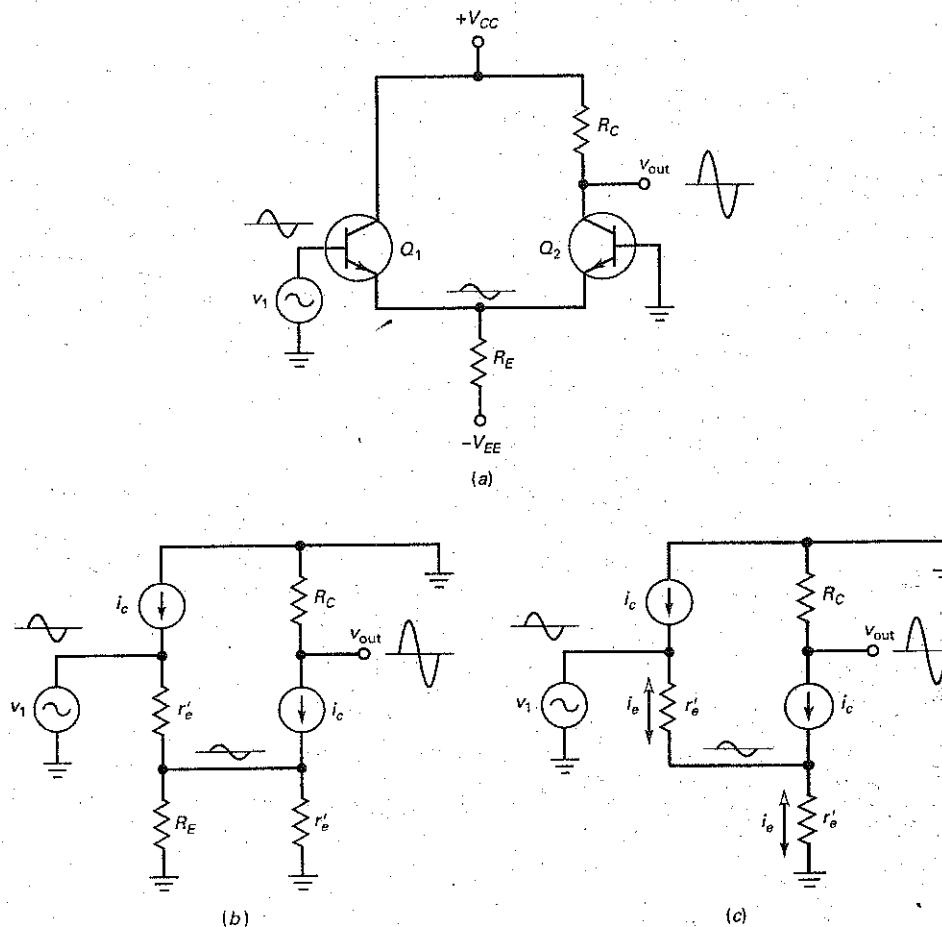
In this section, we will derive the equation for the voltage gain of a diff amp. We will start with the simplest configuration, the noninverting input and single-ended output. After deriving its voltage gain, we will extend the results to the other configurations.

Theory of Operation

Figure 17-8a shows a noninverting input and single-ended output. With a large R_E , the tail current is almost constant when a small ac signal is present. Because of this, the two halves of a diff amp respond in a complementary manner to the noninverting input. In other words, an increase in the emitter current of Q_1 produces a decrease in the emitter current of Q_2 . Conversely, a decrease in the emitter current of Q_1 produces an increase in the emitter current of Q_2 .

In Fig. 17-8a, the left transistor Q_1 acts like an emitter follower that produces an ac voltage across the emitter resistor. This ac voltage is half of the input voltage v_1 . On the positive half cycle of input voltage, the Q_1 emitter current increases, the Q_2 emitter current decreases, and the Q_2 collector voltage increases.

Figure 17-8 (a) Noninverting input and single-ended output; (b) ac equivalent circuit; (c) simplified ac equivalent circuit.



Similarly, on the negative half cycle of input voltage, the Q_1 emitter current decreases, the Q_2 emitter current increases, and the Q_2 collector voltage decreases. This is why the amplified output sine wave is in phase with the noninverting input.

Single-Ended Output Gain

Figure 17-8b shows the ac equivalent circuit. Notice that each transistor has an r'_e . Also, the biasing resistor R_E is in parallel with the r'_e of the right transistor. In any practical design, R_E is much greater than r'_e . Because of this, we can ignore R_E in a preliminary analysis.

Figure 17-8c shows the simplified equivalent circuit. Notice that the input voltage v_1 is across the first r'_e in series with the second r'_e . Since the two resistances are equal, the voltage across each r'_e is half of the input voltage. This is why the ac voltage across the tail resistor of Fig. 17-8a is half of the input voltage.

In Fig. 17-8c, the ac output voltage is:

$$v_{\text{out}} = i_c R_C$$

and the ac input voltage is:

$$v_{\text{in}} = i_e r'_e + i_{e'} r'_e = 2i_e r'_e$$

Dividing v_{out} by v_{in} gives the voltage gain:

$$\text{Single-ended output: } A_v = \frac{R_C}{2r'_e} \quad (17-9)$$

A final point: In Fig. 17-8a, a quiescent dc voltage V_C exists at the output terminal. This voltage is not part of the ac signal. The ac voltage v_{out} is any change from the quiescent voltage. In an op amp, the quiescent dc voltage is removed in a later stage because it is unimportant.

Differential-Output Gain

Figure 17-9 shows the ac equivalent circuit for a noninverting input and differential output. The analysis is almost identical to the previous example, except that the output voltage is twice as much since there are two collector resistors:

$$v_{\text{out}} = v_{c2} - v_{c1} = i_c R_C - (-i_c R_C) = 2i_c R_C$$

(Note: The second minus sign appears because the v_{c1} signal is 180° out of phase with v_{c2} , as shown in Fig. 17-9.)

Figure 17-9 Noninverting input and differential output.

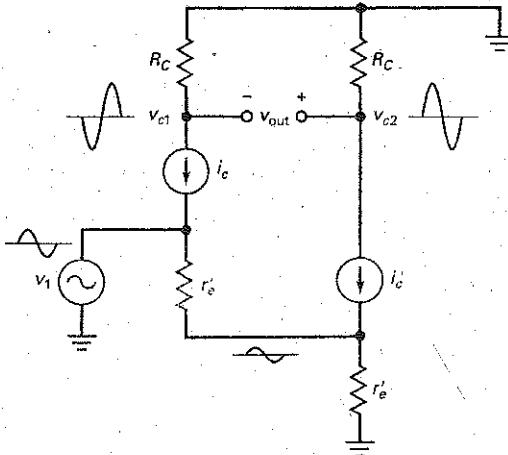
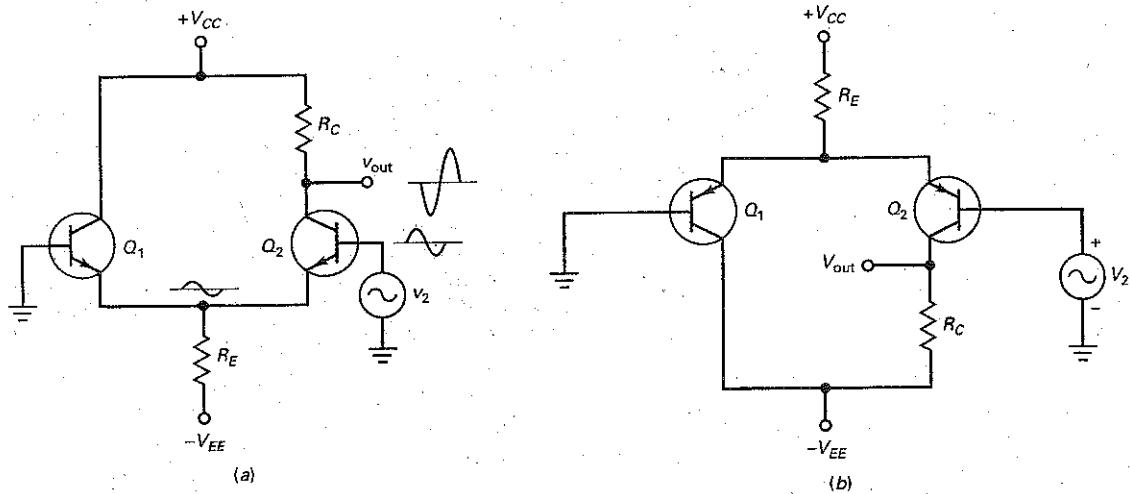


Figure 17-10 (a) Inverting input with single-ended output; (b) *pnp* version.



The ac input voltage is still equal to:

$$v_{in} = 2i_e r'_e$$

Dividing the output voltage by the input voltage gives the voltage gain:

$$\text{Differential output: } A_v = \frac{R_C}{r'_e} \quad (17-10)$$

This is easy to remember because it is the same as the voltage gain for a CE stage.

Inverting-Input Configurations

Figure 17-10a shows an inverting input and single-ended output. The ac analysis is almost identical to the noninverting analysis. In this circuit, the inverting input v_2 produces an amplified and inverted ac voltage at the final output. The r'_e of each transistor is still part of a voltage divider in the ac equivalent circuit. This is why the ac voltage across R_E is half of the inverting input voltage. If a differential output is used, the voltage gain is twice as much as previously discussed.

The diff amp in Fig. 17-10b is an upside-down *pnp* version of Fig. 17-10a. As discussed in Chap. 8, *pnp* transistors are often used in transistor circuits using positive power supplies. These *pnp* transistors are drawn in an upside-down configuration. As with the *npn* versions, the inputs and outputs may be either differential or single ended.

Differential-Input Configurations

The differential-input configurations have both inputs active at the same time. The ac analysis can be simplified by using the superposition theorem as follows: Since we know how a diff amp behaves with noninverting and inverting inputs, we can combine the two results to get the equations for differential-input configurations.

Table 17-2 | Diff-Amp Voltage Gains

Input	Output	A_v	v_{out}
Differential	Differential	R_C/r'_e	$A_v(v_1 - v_2)$
Differential	Single-ended	$R_C/2r'_e$	$A_v(v_1 - v_2)$
Single-ended	Differential	R_C/r'_e	A_vv_1 or $-A_vv_2$
Single-ended	Single-ended	$R_C/2r'_e$	A_vv_1 or $-A_vv_2$

The output voltage for a noninverting input is:

$$A_v(v_1)$$

and the output voltage for an inverting input is:

$$v_{out} = -A_v(v_2)$$

By combining the two results, we get the equation for a differential input:

$$v_{out} = A_v(v_1 - v_2)$$

Table of Voltage Gains

Table 17-2 summarizes the voltage gains for the diff-amp configurations. As you can see, the voltage gain is maximum with a differential output. The voltage gain is cut in half when a single-ended output is used. Also, when a single-ended output is used, the input may be noninverting or inverting.

Input Impedance

In a CE stage, the input impedance of the base is:

$$z_{in} = \beta r'_e$$

In a diff amp, the input impedance of either base is twice as high:

$$z_{in} = 2\beta r'_e \quad (17-11)$$

The input impedance of a diff amp is twice as high because there are two ac emitter resistances r'_e in the ac equivalent circuit instead of one. Equation (17-11) is valid for all configurations because any ac input signal sees two ac emitter resistances in the path between the base and ground.

Example 17-4

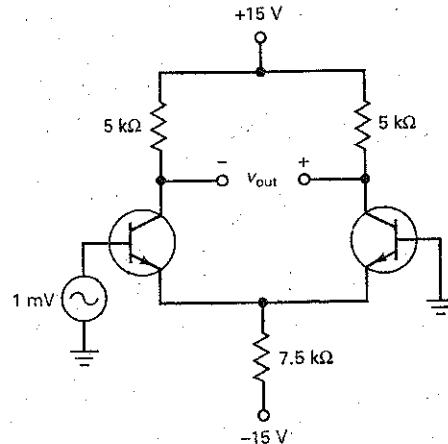
III Multisim

In Fig. 17-11, what is the ac output voltage? If $\beta = 300$, what is the input impedance of the diff amp?

SOLUTION We analyzed the dc equivalent circuit in Example 17-1. Ideally, 15 V is across the emitter resistor, producing a tail current of 2 mA, which means that the dc emitter current in each transistor is:

$$I_E = 1 \text{ mA}$$

Figure 17-11 Example.



Now, we can calculate the ac emitter resistance:

$$r'_e = \frac{25 \text{ mV}}{1 \text{ mA}} = 25 \Omega$$

The voltage gain is:

$$A_v = \frac{5 \text{ k}\Omega}{25 \text{ V}} = 200$$

The ac output voltage is:

$$v_{\text{out}} = 200(1 \text{ mV}) = 200 \text{ mV}$$

and the input impedance of the diff amp is:

$$z_{\text{in(base)}} = 2(300)(25 \Omega) = 15 \text{ k}\Omega$$

PRACTICE PROBLEM 17-4 Repeat Example 17-4 with R_E changed to 5 kΩ.

Example 17-5



Repeat the preceding example using the second approximation to calculate the quiescent emitter current.

SOLUTION In Example 17-2, we calculated a dc emitter current of:

$$I_E = 0.955 \text{ mA}$$

The ac emitter resistance is:

$$r'_e = \frac{25 \text{ mV}}{0.955 \text{ mA}} = 26.2 \Omega$$

Since the circuit has a differential output, the voltage gain is:

$$A_v = \frac{5 \text{ k}\Omega}{26.2 \text{ }\Omega} = 191$$

The ac output voltage is:

$$v_{\text{out}} = 191(1 \text{ mV}) = 191 \text{ mV}$$

and the input impedance of the diff amp is:

$$z_{\text{in(base)}} = 2(300)(26.2 \text{ }\Omega) = 15.7 \text{ k}\Omega$$

If the circuit is simulated with MultiSim, the following answers result for 2N3904 transistors:

$$v_{\text{out}} = 172 \text{ mV}$$

$$z_{\text{in(base)}} = 13.4 \text{ k}\Omega$$

The MultiSim output voltage and the input impedance are both slightly lower than our calculated values. When using specific part numbers for transistors, MultiSim loads in all kinds of higher-order transistor parameters that produce almost exact answers. This is why you must use a computer if you need high accuracy. Otherwise, rest satisfied with approximate methods of analysis.

Example 17-6

Repeat Example 17-4 for $v_2 = 1 \text{ mV}$ and $v_1 = 0$.

SOLUTION Instead of driving the noninverting input, we are driving the inverting input. Ideally, the output voltage has the same magnitude, 200 mV, but it is inverted. The input impedance is approximately 15 k Ω .

Example 17-7

What is the ac output voltage in Fig. 17-12? If $\beta = 300$, what is the input impedance of the diff amp?

SOLUTION Ideally, 15 V is across the emitter resistor, so that the tail current is:

$$I_T = \frac{15 \text{ V}}{1 \text{ M}\Omega} = 15 \mu\text{A}$$

Since the emitter current in each transistor is half of the tail current:

$$r'_e = \frac{25 \text{ mV}}{7.5 \mu\text{A}} = 3.33 \text{ k}\Omega$$

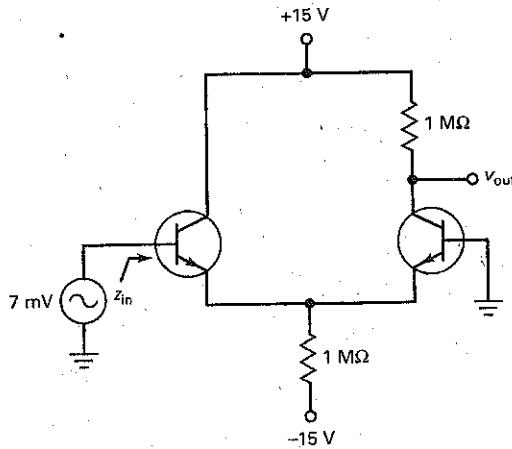
The voltage gain for the single-ended output is:

$$A_v = \frac{1 \text{ M}\Omega}{2(3.33 \text{ k}\Omega)} = 150$$

The ac output voltage is:

$$v_{\text{out}} = 150(7 \text{ mV}) = 1.05 \text{ V}$$

Figure 17-12 Example.



and the input impedance of the base is:

$$z_{in} = 2(300)(3.33 \text{ k}\Omega) = 2 \text{ M}\Omega$$

PRACTICE PROBLEM 17-7 Repeat Example 17-7 with R_E changed to 500 k Ω .

17-4 Input Characteristics of an Op Amp

Assuming perfect symmetry in a diff amp is a good approximation for many applications. But in precision applications, we can no longer treat the two halves of a diff amp as identical. There are three characteristics on the data sheet of every op amp that a designer uses when more accurate answers are needed. They are the input bias current, the input offset current, and the input offset voltage.

Input Bias Current

In an integrated op amp, the β_{dc} of each transistor in the first stage is slightly different, which means that the base currents in Fig. 17-13 are slightly different. The input bias current is defined as the average of the dc base currents:

$$I_{in(bias)} = \frac{I_{B1} + I_{B2}}{2} \quad (17-12)$$

For instance, if $I_{B1} = 90 \text{ nA}$ and $I_{B2} = 70 \text{ nA}$, the input bias current is:

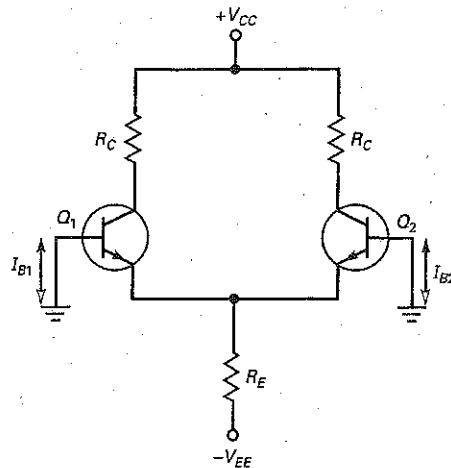
$$I_{in(bias)} = \frac{90 \text{ nA} + 70 \text{ nA}}{2} = 80 \text{ nA}$$

With bipolar op amps, the input bias current is typically in nanoamperes. When op amps use JFETs in the input diff amp, the input bias current is in picoamperes.

GOOD TO KNOW

An op amp that uses JFETs in the input differential amplifier and bipolar transistors for the following stages is called a *bi-FET op amp*.

Figure 17-13 Different base currents.



The input bias current will flow through the resistances between the bases and ground. These resistances may be discrete resistances, or they may be the Thevenin resistances of the input sources.

Input Offset Current

The input offset current is defined as the difference of the dc base currents:

$$I_{\text{in(off)}} = I_{B1} - I_{B2} \quad (17-13)$$

This difference in the base currents indicates how closely the transistors are matched. If the transistors are identical, the input offset current is zero because both base currents will be equal. But almost always, the two transistors are slightly different and the two base currents are not equal.

As an example, suppose $I_{B1} = 90 \text{ nA}$ and $I_{B2} = 70 \text{ nA}$. Then:

$$I_{\text{in(off)}} = 90 \text{ nA} - 70 \text{ nA} = 20 \text{ nA}$$

The Q_1 transistor has 20 nA more base current than the Q_2 transistor. This can cause a problem when large base resistances are used.

Base Currents and Offsets

By rearranging Eqs. (17-12) and (17-13), we can derive these two equations for the base currents:

$$I_{B1} = I_{\text{in(bias)}} + \frac{I_{\text{in(off)}}}{2} \quad (17-13a)$$

$$I_{B2} = I_{\text{in(bias)}} - \frac{I_{\text{in(off)}}}{2} \quad (17-13b)$$

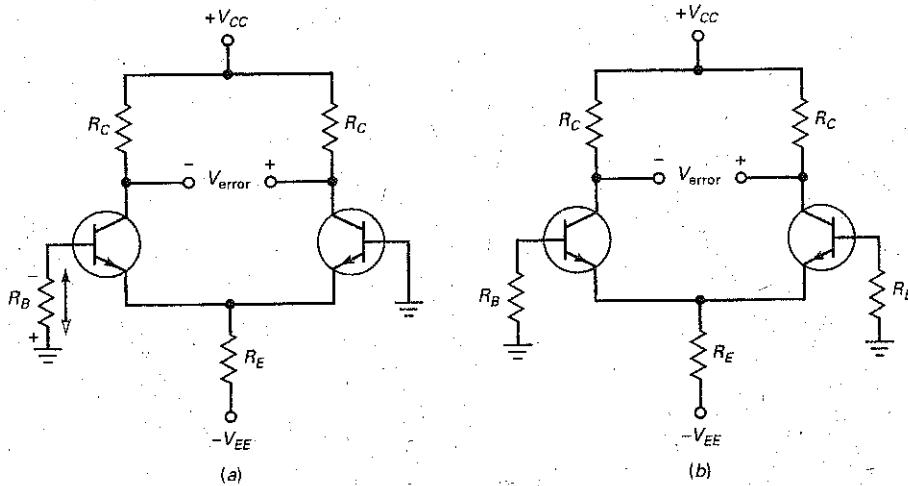
Data sheets always list $I_{\text{in(bias)}}$ and $I_{\text{in(off)}}$, but not I_{B1} and I_{B2} . With these equations, we can calculate the base currents. These equations assume that I_{B1} is greater than I_{B2} . If I_{B2} is greater than I_{B1} , transpose the equations.

Effect of Base Current

Some diff amps are operated with a base resistance on only one side, as shown in Fig. 17-14a. Because of the base current direction, the base current through R_B produces a noninverting dc input voltage of:

$$V_I = -I_{B1}R_B$$

Figure 17-14 (a) Base resistor produces unwanted input voltage; (b) equal base resistance on other side reduces error voltage.



(Note: Capital letters are used here and elsewhere for dc error voltages like V_1 . For simplicity, we will treat V_1 as an absolute value. This voltage has the same effect as a genuine input signal. When this false signal is amplified, an unwanted dc voltage V_{error} appears across the output, as shown in Fig. 17-14a.)

For instance, if a data sheet gives $I_{\text{in(bias)}} = 80 \text{ nA}$ and $I_{\text{in(off)}} = 20 \text{ nA}$, Eqs. (17-13a) and (17-13b) give:

$$I_{B1} = 80 \text{ nA} + \frac{20 \text{ nA}}{2} = 90 \text{ nA}$$

$$I_{B2} = 80 \text{ nA} - \frac{20 \text{ nA}}{2} = 70 \text{ nA}$$

If $R_B = 1 \text{ k}\Omega$, the noninverting input has an error voltage of:

$$V_1 = (90 \text{ nA})(1 \text{ k}\Omega) = 90 \mu\text{V}$$

Effect of Input Offset Current

One way to reduce the output error voltage is by using an equal base resistance on the other side of the diff amp, as shown in Fig. 17-14b. In this case, we have a differential dc input of:

$$V_{\text{in}} = I_{B1}R_B - I_{B2}R_B = (I_{B1} - I_{B2})R_B$$

or

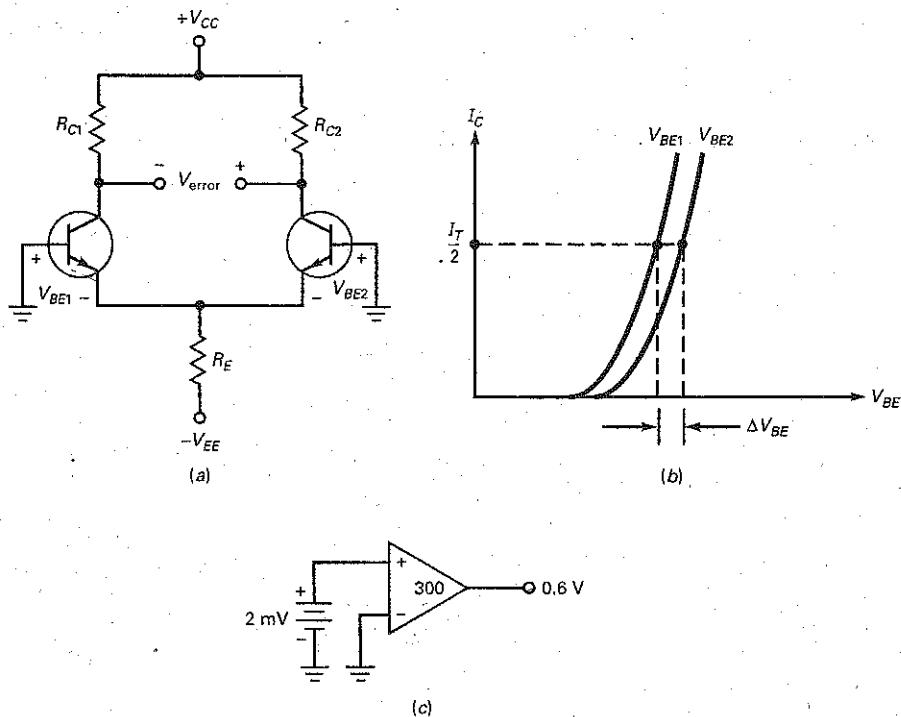
$$V_{\text{in}} = I_{\text{in(off)}}R_B \quad (17-14)$$

Since $I_{\text{in(off)}}$ is usually less than 25 percent of $I_{\text{in(bias)}}$, the input error voltage is much less when equal base resistors are used. For this reason, designers often include an equal base resistance on the opposite side of a diff amp, as shown in Fig. 17-14b.

For instance, if $I_{\text{in(bias)}} = 80 \text{ nA}$ and $I_{\text{in(off)}} = 20 \text{ nA}$, then a base resistance of $1 \text{ k}\Omega$ produces an input error voltage of:

$$V_{\text{in}} = (20 \text{ nA})(1 \text{ k}\Omega) = 20 \mu\text{V}$$

Figure 17-15 (a) Different collector resistors produce error when bases are grounded; (b) different base-emitter curves added to error; (c) input offset voltage is equivalent to an unwanted input voltage.



Input Offset Voltage

When a diff amp is integrated as the first stage of an op amp, the two halves are almost but not quite identical. To begin with, the two collector resistances may be different, as shown in Fig. 17-15a. Because of this, an error voltage appears across the output.

Another source of error is the different V_{BE} curves for each transistor. For instance, suppose that the two base-emitter curves have the same current, as shown in Fig. 17-15b. Because the curves are slightly different, there is a difference between the two V_{BE} values. This difference adds to the error voltage. Besides R_C and V_{BE} , other transistor parameters may differ slightly on each half of the diff amp.

The **input offset voltage** is defined as the input voltage that would produce the same output error voltage in a perfect diff amp. As an equation:

$$V_{in(off)} = \frac{V_{error}}{A_v} \quad (17-15)$$

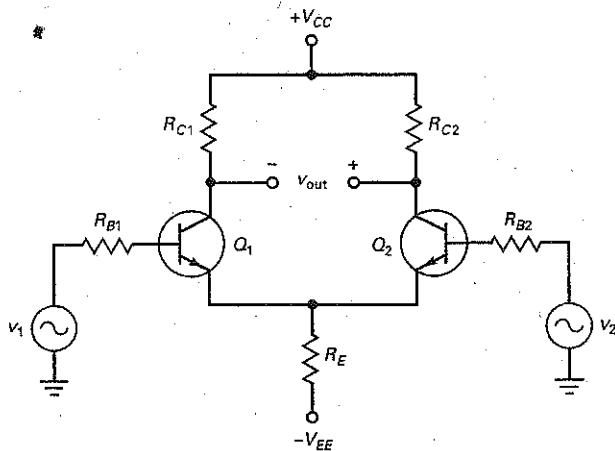
In this equation, V_{error} does not include the effects of input bias and offset current because both bases are grounded when V_{error} is measured.

For instance, if a diff amp has an output error voltage of 0.6 V and a voltage gain of 300, the input offset voltage is:

$$V_{in(off)} = \frac{0.6 \text{ V}}{300} = 2 \text{ mV}$$

Figure 17-15c illustrates the idea. An input offset voltage of 2 mV is driving a diff amp with a voltage gain of 300 to produce an error voltage of 0.6 V.

Figure 17-16 Output of diff amp includes desired signal and error voltage.



Combined Effects

In Fig. 17-16, the output voltage is the superposition of all input effects. To begin with, there is the ideal ac input:

$$v_{in} = v_1 - v_2$$

This is what we want. It is the voltage coming from the two input sources. It is amplified to produce the desired ac output:

$$v_{out} = A_v(v_1 - v_2)$$

Then, there are the three unwanted dc error inputs. With Eqs. (17-13a) and (17-13b), we can derive these formulas:

$$V_{1err} = (R_{B1} - R_{B2})I_{in(bias)} \quad (17-16)$$

$$V_{2err} = (R_{B1} + R_{B2}) \frac{I_{in(off)}}{2} \quad (17-17)$$

$$V_{3err} = V_{in(off)} \quad (17-18)$$

The advantage of these formulas is that they use $I_{in(bias)}$ and $I_{in(off)}$, quantities on the data sheet. The three dc errors are amplified to produce the output error voltage:

$$V_{error} = A_v(V_{1err} + V_{2err} + V_{3err}) \quad (17-19)$$

In many cases, V_{error} can be ignored. This will depend on the application. For instance, if we are building an ac amplifier, V_{error} may not be important. It is only when we are building some kind of precision dc amplifier that V_{error} needs to be taken into account.

Equal Base Resistances

When the bias and offset errors cannot be ignored, here are the remedies. As already mentioned, one of the first things a designer can do is to use equal base resistances: $R_{B1} = R_{B2} = R_B$. This brings the two halves of the diff amp into a closer alignment because Eqs. (17-16) through (17-19) become:

$$V_{1err} = 0$$

$$V_{2err} = R_B I_{in(off)}$$

$$V_{3err} = V_{in(off)}$$

Table 17-3 | Sources of Output Error Voltage

Description	Cause	Solution
Input bias current	Voltage across a single R_B	Use equal R_B on other side
Input offset current	Unequal current gains	Data sheet nulling methods
Input offset voltage	Unequal R_C and V_{BE}	Data sheet nulling methods

If further compensation is necessary, the best approach is to use the *nulling circuits* suggested on the data sheets. Manufacturers optimize the design of these nulling circuits, which should be used if output error voltage is a problem. We will discuss nulling circuits in a later chapter.

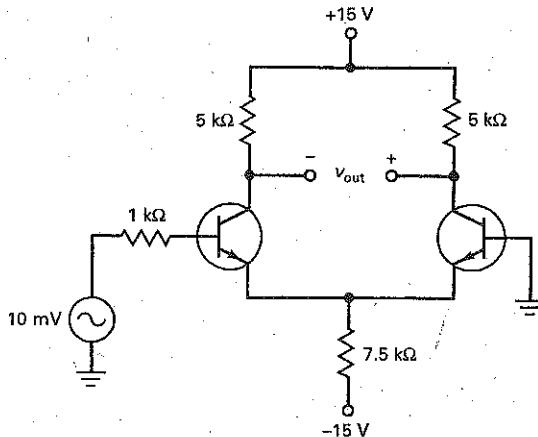
Conclusion

Table 17-3 summarizes the sources of output error voltage. In many applications, the output error voltage is either small enough to ignore or not important in the particular application. In precision applications, in which the dc output is important, some form of nulling is used to eliminate the effects of input bias and offset. Designers usually null the output with methods suggested on the manufacturer's data sheet.

Example 17-8

The diff amp of Fig. 17-17 has $A_v = 200$, $I_{in(bias)} = 3 \mu\text{A}$, $I_{in(off)} = 0.5 \mu\text{A}$, and $V_{in(off)} = 1 \text{ mV}$. What is the output error voltage? If a matching base resistor is used, what is the output error voltage?

Figure 17-17. Example.



SOLUTION With Eqs. (17-16) to (17-18):

$$V_{1\text{err}} = (R_{B1} - R_{B2})I_{\text{in(bias)}} = (1 \text{ k}\Omega)(3 \mu\text{A}) = 3 \text{ mV}$$

$$V_{2\text{err}} = (R_{B1} + R_{B2}) \frac{I_{\text{in(off)}}}{2} = (1 \text{ k}\Omega)(0.25 \mu\text{A}) = 0.25 \text{ mV}$$

$$V_{3\text{err}} = V_{\text{in(off)}} = 1 \text{ mV}$$

The output error voltage is:

$$V_{\text{error}} = 200(3 \text{ mV} + 0.25 \text{ mV} + 1 \text{ mV}) = 850 \text{ mV}$$

When a matching base resistance of $1 \text{ k}\Omega$ is used on the inverting side,

$$V_{1\text{err}} = 0$$

$$V_{2\text{err}} = R_B I_{\text{in(off)}} = (1 \text{ k}\Omega)(0.5 \mu\text{A}) = 0.5 \text{ mV}$$

$$V_{3\text{err}} = V_{\text{in(off)}} = 1 \text{ mV}$$

The output error voltage is:

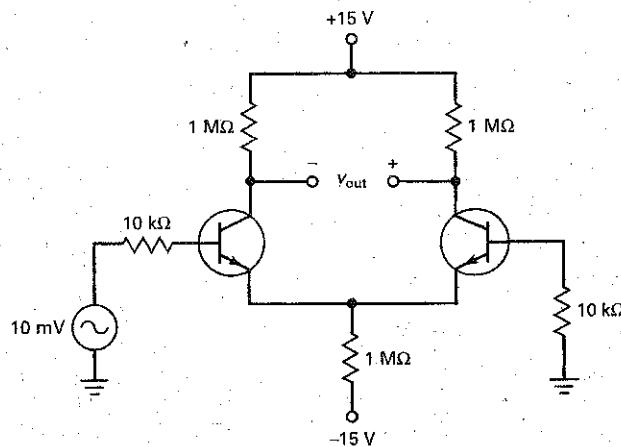
$$V_{\text{error}} = 200(0.5 \text{ mV} + 1 \text{ mV}) = 300 \text{ mV}$$

PRACTICE PROBLEM 17-8 In Fig. 17-17, what is the output error voltage if the diff amp has a voltage gain of 150?

Example 17-9

The diff amp of Fig. 17-18 has $A_v = 300$, $I_{\text{in(bias)}} = 80 \text{ nA}$, $I_{\text{in(off)}} = 20 \text{ nA}$, and $V_{\text{in(off)}} = 5 \text{ mV}$. What is the output error voltage?

Figure 17-18 Example.



SOLUTION The circuit uses equal base resistors. With the equations shown above:

$$V_{1\text{err}} = 0$$

$$V_{2\text{err}} = (10 \text{ k}\Omega)(20 \text{ nA}) = 0.2 \text{ mV}$$

$$V_{3\text{err}} = 5 \text{ mV}$$

The total output error voltage is:

$$V_{\text{error}} = 300(0.2 \text{ mV} + 5 \text{ mV}) = 1.56 \text{ V}$$

PRACTICE PROBLEM 17-9 Repeat Example 17-9 using $I_{\text{in(off)}} = 10 \text{ nA}$.

17-5 Common-Mode Gain

Figure 17-19a shows a differential input and single-ended output. The same input voltage, $v_{\text{in(CM)}}$ is being applied to each base. This voltage is called a **common-mode signal**. If the diff amp is perfectly symmetrical, there is no ac output voltage with a common-mode input signal because $v_1 = v_2$. When a diff amp is not perfectly symmetrical, there will be a small ac output voltage.

In Fig. 17-19a, equal voltages are applied to the noninverting and inverting inputs. Nobody would deliberately use a diff amp this way because the output voltage is ideally zero. The reason for discussing this type of input is because most static, interference, and other kinds of undesirable pickup are common-mode signals.

Here is how a common-mode signal appears: The connecting wires on the input bases act like small antennas. If the diff amp is operating in an environment with a lot of electromagnetic interference, each base acts like a small antenna that picks up an unwanted signal voltage. One of the reasons the diff amp is so popular is because it discriminates against these common-mode signals. In other words, a diff amp does not amplify common-mode signals.

Here is an easy way to find the voltage gain for a common-mode signal: We can redraw the circuit, as shown in Fig. 17-19b. Since equal voltages $v_{\text{in(CM)}}$ drive both inputs simultaneously, there is almost no current through the wire between the emitters. Therefore, we can remove the connecting wire, as shown in Fig. 17-20.

Figure 17-19 (a) Common-mode input signal; (b) equivalent circuit.

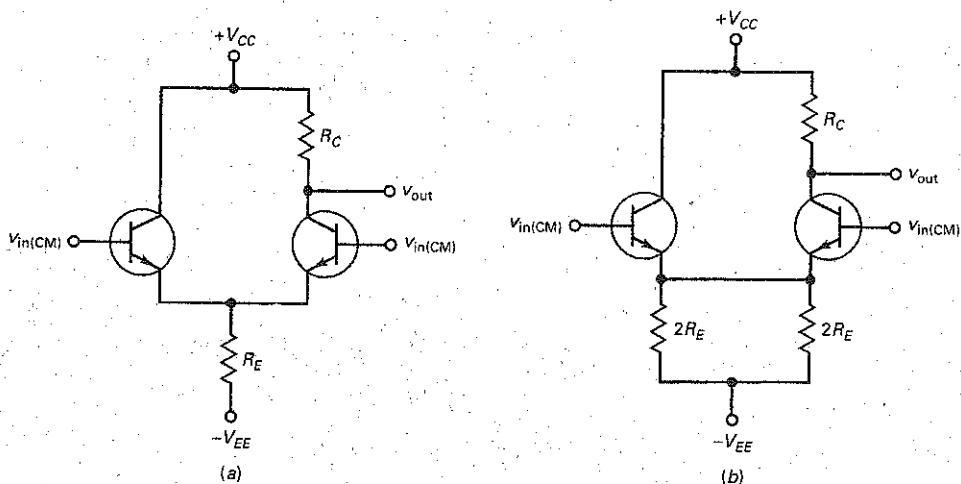
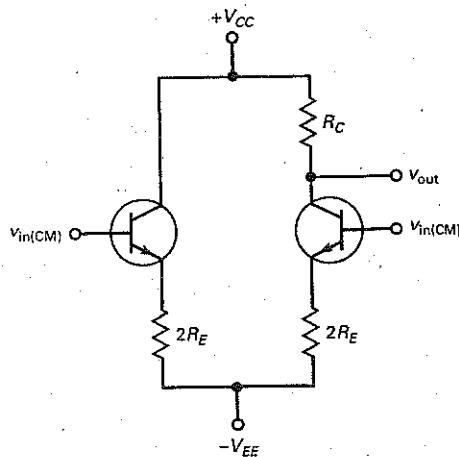


Figure 17-20 Right side acts like swamped amplifier with common-mode input.



With a common-mode signal, the right side of the circuit is equivalent to a heavily swamped CE amplifier. Since R_E is always much greater than r'_e , the swamped voltage gain is approximately:

$$A_{v(CM)} = \frac{R_C}{2R_E} \quad (17-20)$$

With typical values of R_C and R_E , the common-mode voltage gain is usually less than 1.

Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) is defined as the voltage gain divided by common-mode voltage gain. In symbols:

$$\text{CMRR} = \frac{A_v}{A_{v(CM)}} \quad (17-21)$$

For instance, if $A_v = 200$ and $A_{v(CM)} = 0.5$, CMRR = 400.

The higher the CMRR, the better. A high CMRR means that the diff amp is amplifying the wanted signal and discriminating against the common-mode signal.

Data sheets usually specify CMRR in decibels, using the following formula for the decibel conversion:

$$\text{CMRR}_{\text{dB}} = 20 \log \text{CMRR} \quad (17-22)$$

As an example, if CMRR = 400:

$$\text{CMRR}_{\text{dB}} = 20 \log 400 = 52 \text{ dB}$$

Example 17-10

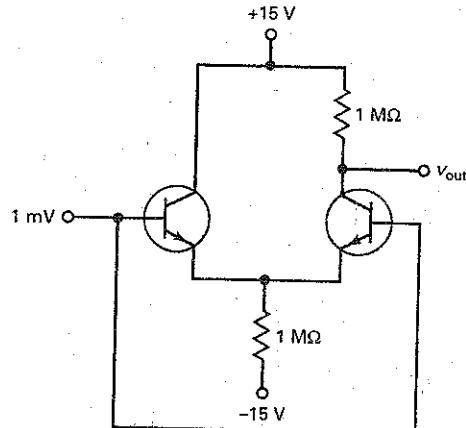
MultiSim

In Fig. 17-21, what is the common-mode voltage gain? The output voltage?

SOLUTION With Eq. (17-20):

$$A_{v(CM)} = \frac{1 \text{ M}\Omega}{2 \text{ M}\Omega} = 0.5$$

Figure 17-21 Example.



The output voltage is:

$$v_{\text{out}} = 0.5(1 \text{ mV}) = 0.5 \text{ mV}$$

As you can see, the diff amp attenuates (weakens) the common-mode signal rather than amplifying it.

PRACTICE PROBLEM 17-10 Repeat Example 17-10 with R_E changed to $2 \text{ M}\Omega$.

Example 17-11

In Fig. 17-22, $A_v = 150$, $A_{v(\text{CM})} = 0.5$, and $v_{\text{in}} = 1 \text{ mV}$. If the base leads are picking up a common-mode signal of 1 mV , what is the output voltage?

SOLUTION The input has two components, the desired signal and a common-mode signal. Both are equal in amplitude. The desired component is amplified to get an output of:

$$v_{\text{out1}} = 150(1 \text{ mV}) = 150 \text{ mV}$$

The common-mode signal is attenuated to get an output of:

$$v_{\text{out2}} = 0.5(1 \text{ mV}) = 0.5 \text{ mV}$$

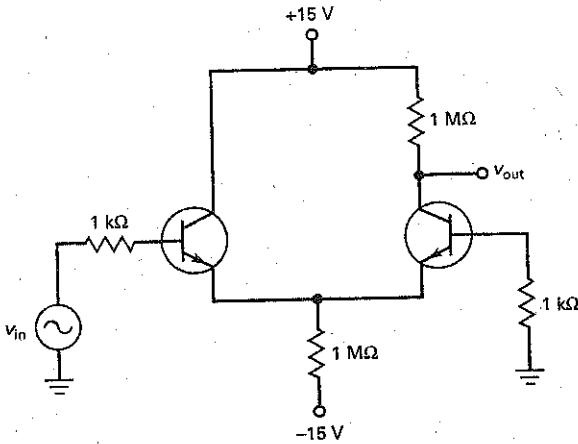
The total output is the sum of these two components:

$$v_{\text{out}} = v_{\text{out1}} + v_{\text{out2}}$$

The output contains both components, but the desired component is 300 times greater than the unwanted component.

This example shows why the diff amp is useful as the input stage of an op amp. It attenuates the common-mode signal. This is a distinct advantage over

Figure 17-22 Example.



the ordinary CE amplifier, which amplifies a stray pickup signal the same way it amplifies the desired signal.

PRACTICE PROBLEM 17-11 In Fig. 17-22, change A_v to 200 and find the output voltage.

Example 17-12

A 741 is an op amp with $A_v = 200,000$ and $\text{CMRR}_{\text{dB}} = 90 \text{ dB}$. What is the common-mode voltage gain? If the desired and common-mode signal each has a value of $1 \mu\text{V}$, what is the output voltage?

SOLUTION

$$\text{CMRR} = \text{antilog } \frac{90 \text{ dB}}{20} = 31,600$$

Rearranging Eq. (17-21):

$$A_{v(\text{CM})} = \frac{A_v}{\text{CMRR}} = \frac{200,000}{31,600} = 6.32$$

The desired output component is:

$$v_{\text{out1}} = 200,000(1 \mu\text{V}) = 0.2 \text{ V}$$

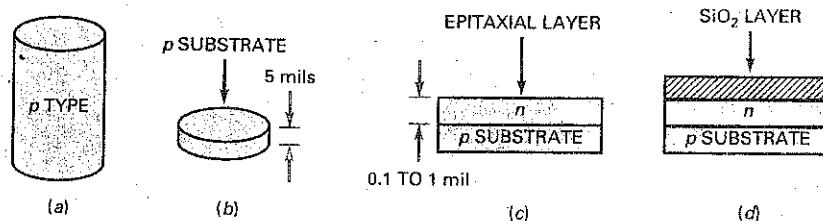
The common-mode output is:

$$v_{\text{out2}} = 6.32(1 \mu\text{V}) = 6.32 \mu\text{V}$$

As you can see, the desired output is much larger than the common-mode output.

PRACTICE PROBLEM 17-12 Repeat Example 17-12 using an op amp gain of 100,000.

Figure 17-23 (a) *p* crystal; (b) wafer; (c) epitaxial layer; (d) insulating layer.



17-6 Integrated Circuits

The invention of the **integrated circuit (IC)** in 1959 was a major breakthrough because the components are no longer discrete; they are *integrated*. This means that they are produced and connected during the manufacturing process on a single *chip*, a small piece of semiconductor material. Because the components are microscopically small, a manufacturer can place thousands of these integrated components in the space occupied by a single discrete transistor.

What follows is a brief description of how an IC is made. Current manufacturing processes are much more complicated, but the simplified discussion will give you the basic idea behind the making of a bipolar IC.

Basic Idea

First, the manufacturer produces a *p* crystal several inches long (Fig. 17-23a). This is sliced into many thin *wafers*, as in Fig. 17-23b. One side of the wafer is lapped and polished to get rid of surface imperfections. This wafer is called the *p substrate*. It will be used as a chassis for the integrated components. Next, the wafers are put into a furnace. A gas mixture of silicon atoms and pentavalent atoms passes over the wafers. This forms a thin layer of *n*-type semiconductor on the heated surface of the substrate (see Fig. 17-23c). We call this thin layer an *epitaxial layer*. As shown in Fig. 17-23c, the epitaxial layer is about 0.1 to 1 mil thick.

To prevent contamination of the epitaxial layer, pure oxygen is blown over the surface. The oxygen atoms combine with the silicon atoms to form a layer of silicon dioxide (SiO₂) on the surface, as shown in Fig. 17-23d. This glasslike layer of SiO₂ seals off the surface and prevents further chemical reactions. Sealing off the surface like this is known as *passivation*.

The wafer is then cut into the rectangular areas shown in Fig. 17-24. Each of these areas will be a separate chip after the wafer is cut. But before the wafer is cut, the manufacturer produces hundreds of circuits on the wafer, one on each chip area of Fig. 17-24. This simultaneous mass production is the reason for the low cost of ICs.

Here is how an integrated transistor is formed: Part of the SiO₂ is etched off, exposing the epitaxial layer (see Fig. 17-25a). The wafer is then put into a furnace, and trivalent atoms are diffused into the epitaxial layer. The concentration of trivalent atoms is enough to change the exposed epitaxial layer from *n* material to *p* material. Therefore, we get an island of *n* material under the SiO₂ layer (Fig. 17-25b). Oxygen is again blown over the surface to form the complete SiO₂ layer shown in Fig. 17-25c.

A hole is now etched in the center of the SiO₂ layer. This exposes the *n* epitaxial layer (Fig. 17-25d). The hole in the SiO₂ layer is called a *window*. We are now looking down at what will be the collector of the transistor.

Figure 17-24 Cutting wafer into chips.

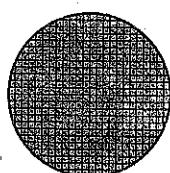
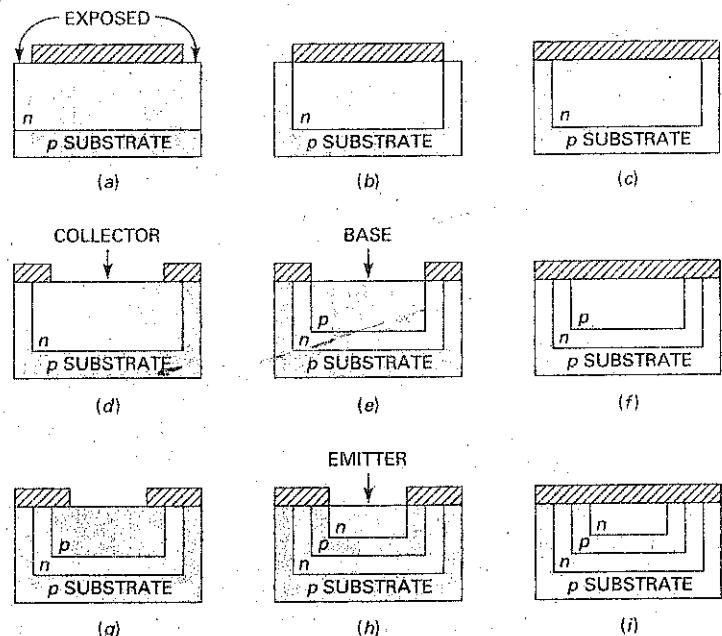


Figure 17-25 Steps in making a transistor.



To get the base, we pass trivalent atoms through this window; these impurities diffuse into the epitaxial layer and form an island of *p*-type material (Fig. 17-25*e*). Then, the SiO_2 layer is re-formed by passing oxygen over the wafer (Fig. 17-25*f*).

To form the emitter, we etch a window in the SiO_2 layer and expose the *p* island (Fig. 17-25*g*). By diffusing pentavalent atoms into the *p* island, we can form the small *n* island shown in Fig. 17-25*h*.

We then passivate the structure by blowing oxygen over the wafer (Fig. 17-25*i*). By etching windows in the SiO_2 layer, we can deposit metal to make electrical contact with the emitter, base, and collector. This gives us the integrated transistor of Fig. 17-26*a*.

To get a diode, we follow the same steps up to the point at which the *p* island has been formed and sealed off (Fig. 17-25*f*). Then, we etch windows to expose the *p* and *n* islands. By depositing metal through these windows, we make electrical contact with the cathode and anode of the integrated diode (Fig. 17-26*b*). By etching two windows above the *p* island of Fig. 17-25*f*, we can make metallic contact with this *p* island; this gives us an integrated resistor (Fig. 17-26*c*).

Figure 17-26 Integrated components: (a) Transistor; (b) diode; (c) resistor.

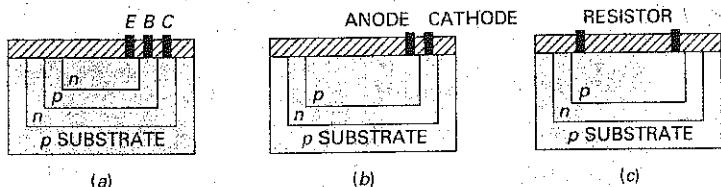
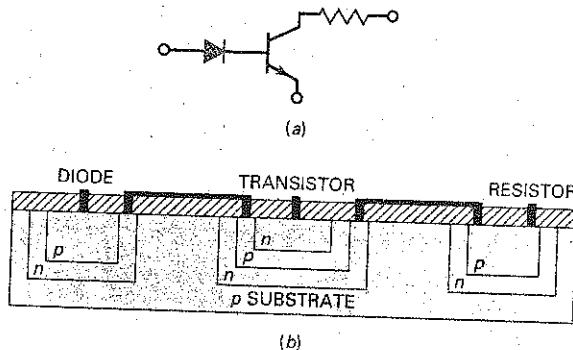


Figure 17-27 Simple IC.



Transistors, diodes, and resistors are easy to fabricate on a chip. For this reason, almost all ICs use these components. It is not practical to integrate inductors and large capacitors on the surface of a chip.

A Simple Example

To give you an idea of how a circuit is produced, look at the simple three-component circuit of Fig. 17-27a. To fabricate this circuit, we would simultaneously produce hundreds of circuits like this on a wafer. Each chip area would resemble Fig. 17-27b. The diode and resistor would be formed at the point mentioned earlier. At a later step, the emitter of the transistor would be formed. Then we would etch windows and deposit metal to connect the diode, transistor, and resistor, as shown in Fig. 17-27b.

Regardless of how complicated a circuit may be, producing it is mainly a process of etching windows, forming *p* and *n* islands, and connecting the integrated components. The *p* substrate isolates the integrated components from each other. In Fig. 17-27b, there are depletion layers between the *p* substrate and the three *n* islands that touch it. Because the depletion layers have essentially no current carriers, the integrated components are insulated from one another. This kind of insulation is known as *depletion-layer isolation*.

Types of ICs

The integrated circuits we have described are called **monolithic ICs**. The word *monolithic* is from the Greek and means "one stone." The word is appropriate because the components are part of one chip. Monolithic ICs are the most common type of IC. Since their invention, manufacturers have been producing monolithic ICs to carry out all kinds of functions.

Commercially available types can be used as amplifiers, voltage regulators, crowbars, AM receivers, television circuits, and computer circuits. But the monolithic IC has power limitations. Since most monolithic ICs are about the size of a discrete small-signal transistor, they are used in low-power applications.

When higher power is needed, thin-film and thick-film ICs may be used. These devices are larger than monolithic ICs but smaller than discrete circuits. With a thin- or thick-film IC, the passive components like resistors and capacitors are integrated, but the transistors and diodes are connected as discrete components to form a complete circuit. Therefore, commercially available thin- and thick-film circuits are combinations of integrated and discrete components.

Another IC used in high-power applications is the **hybrid IC**. Hybrid ICs combine two or more monolithic ICs in one package, or they combine monolithic ICs with thin- or thick-film circuits. Hybrid ICs are widely used for high-power audio-amplifier applications from 5 to more than 50 W.

Levels of Integration

Figure 17-27b is an example of *small-scale integration (SSI)*; only a few components have been integrated to form a complete circuit. SSI refers to ICs with fewer than 12 integrated components. Most SSI chips use integrated resistors, diodes, and bipolar transistors.

Medium-scale integration (MSI) refers to ICs that have from 12 to 100 integrated components per chip. Either bipolar transistors or MOS transistors (enhancement-mode MOSFETs) can be used as the integrated transistors of an IC. Again, most MSI chips use bipolar components.

Large-scale integration (LSI) refers to ICs with more than a hundred components. Since it takes fewer steps to make an integrated MOS transistor, a manufacturer can produce more components on a chip than is possible with bipolar transistors.

Very large scale integration (VLSI) refers to placing thousands (or hundreds of thousands) of components on a single chip. Nearly all modern chips employ VLSI.

Finally, there is *ultra large scale integration (ULSI)*, which refers to placing more than 1 million components on a single chip. The Intel Pentium P4 microprocessor uses ULSI technology. Various versions of this microprocessor have been developed, with the Intel P4 Prescott version containing approximately 125 million transistors. Current expectations are to have 1 billion components on a chip by the year 2011. The exponential growth often referred to as Moore's law will be challenged at this time. However, new technologies, such as nanotechnology, will allow the continued growth to occur.

GOOD TO KNOW

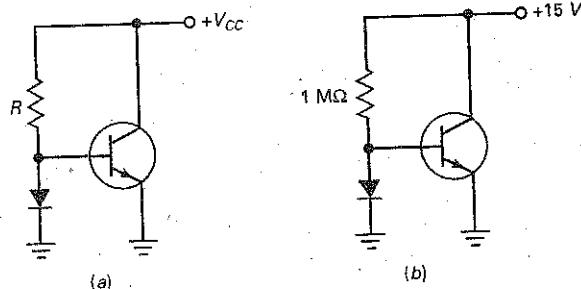
The current mirror concept is used with class B push-pull amplifiers, in which the compensating diodes on the base side match the base-emitter junctions of the push-pull transistors.

17-7 The Current Mirror

With ICs, there is a way to increase the voltage gain and CMRR of a diff amp. Figure 17-28a shows a compensating diode in parallel with the emitter diode of a transistor. The current through the resistor is given by:

$$I_R = \frac{V_{CC} - V_{BE}}{R} \quad (17-23)$$

Figure 17-28 The current mirror.



If the compensating diode and the emitter diode have identical current-voltage curves, the collector current will equal the current through the resistor:

$$I_C = I_R \quad (17-24)$$

A circuit like Fig. 17-28a is called a **current mirror** because the collector current is a mirror image of the resistor current. With ICs, it is relatively easy to match the characteristics of the compensating diode and the emitter diode because both components are on the same chip. Current mirrors are used as current sources and active loads in the design of IC op amps.

Current Mirror Sources the Tail Current

With a single-ended output, the voltage gain of a diff amp is $R_C/2r'_e$ and the common-mode voltage gain is $R_C/2R_E$. The ratio of the two gains gives:

$$\text{CMRR} = \frac{R_E}{r'_e}$$

The larger we can make R_E , the greater the CMRR.

One way to get a high equivalent R_E is to use a current mirror to produce the tail current, as shown in Fig. 17-29. The current through the compensating diode is:

$$I_R = \frac{V_{CC} + V_{EE} - V_{BE}}{R} \quad (17-25)$$

Because of the current mirror, the tail current has the same value. Since Q_4 acts like a current source, it has a very high output impedance. As a result, the equivalent R_E of the diff amp is in hundreds of megohms and the CMRR is dramatically improved.

Active Load

The voltage gain of a single-ended diff amp is $R_C/2r'_e$. The larger we can make R_C , the greater the voltage gain. Figure 17-30 shows a current mirror used as an **active load resistor**. Since Q_6 is a *pnp* current source Q_2 sees an equivalent R_C that is hundreds of megohms. As a result, the voltage gain is much higher with an active load than with an ordinary resistor. Active loading like this is used in most op amps.

Figure 17-29 Current mirror sources the tail current.

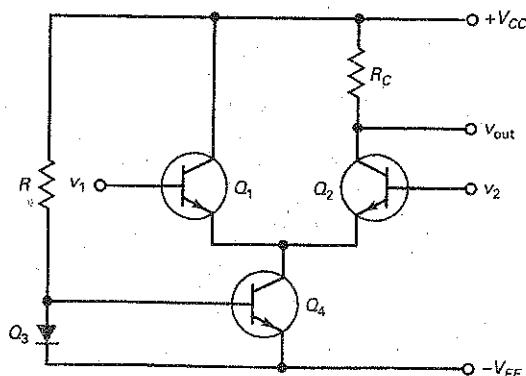
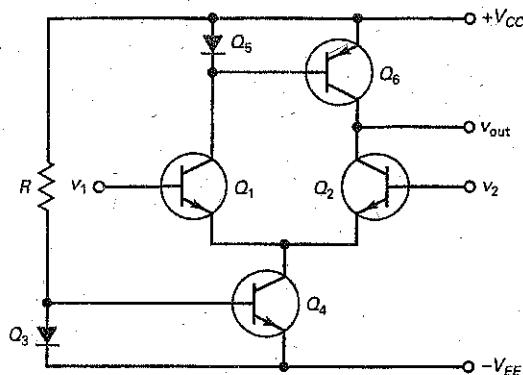


Figure 17-30 Current mirror is an active load.



17-8 The Loaded Diff Amp

In the earlier discussions of a diff amp, we did not use a load resistor. When a load resistor is used, the analysis becomes much more complicated, especially with a differential output.

Figure 17-31a shows a differential output with a load resistor between the collectors. There are several ways to calculate the effect that this load resistor has on the output voltage. If you try to solve this with Kirchhoff loop equations, you will have a very difficult problem. But with Thevenin's theorem, the problem unravels very quickly.

Here is how it is done: If we open the load resistor in Fig. 17-31a, the Thevenin voltage is the same as the v_{out} calculated in earlier discussions. Also, looking into the open AB terminals with all sources zeroed, we see a Thevenin resistance of $2R_C$. (Note: Because the transistors are current sources, they become open when zeroed.)

Figure 17-31 (a) Diff amp with load resistor; (b) Thevenin equivalent circuit for differential output; (c) Thevenin equivalent circuit for single-ended output.

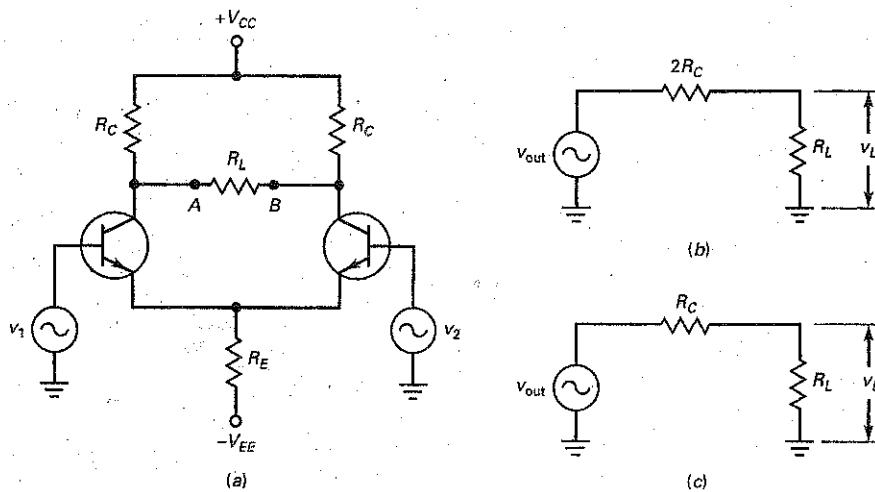
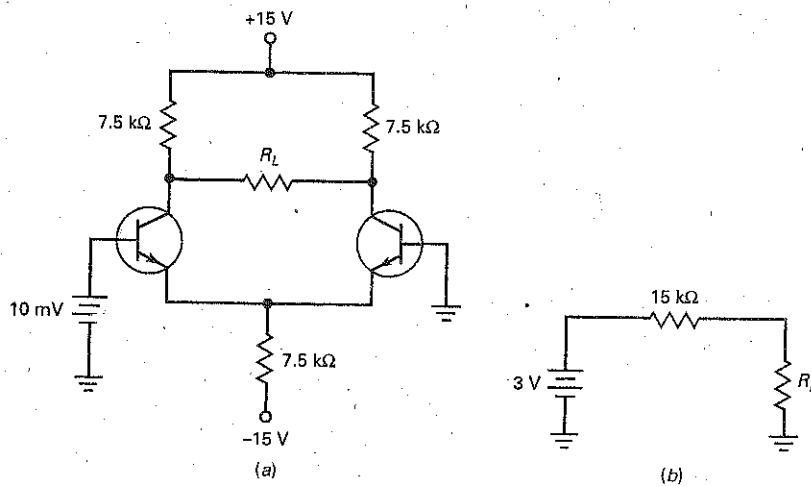


Figure 17-31b shows the Thevenin equivalent circuit. The ac output voltage v_{out} is the same output voltage discussed in earlier sections. After calculating v_{out} , finding the load voltage is easy because all we need is Ohm's law. If a diff amp has a single-ended output, the Thevenin equivalent circuit simplifies to Fig. 17-31c.

Example 17-13

What is the load voltage in Fig. 17-32a when $R_L = 15 \text{ k}\Omega$?

Figure 17-32 Example.



SOLUTION Ideally, the tail current is 2 mA, the emitter current is 1 mA, and $r'_e = 25 \Omega$. The unloaded voltage gain is:

$$A_v = \frac{R_C}{r'_e} = \frac{7.5 \text{ k}\Omega}{25 \Omega} = 300$$

The Thevenin or unloaded output voltage is:

$$v_{out} = A_v(v_1) = 300(10 \text{ mV}) = 3 \text{ V}$$

The Thevenin resistance is:

$$R_{TH} = 2R_C = 2(7.5 \text{ k}\Omega) = 15 \text{ k}\Omega$$

Figure 17-32b is the Thevenin equivalent circuit. With a load resistance of $15 \text{ k}\Omega$, the load voltage is:

$$v_L = 0.5(3 \text{ V}) = 1.5 \text{ V}$$

PRACTICE PROBLEM 17-13 In Fig. 17-32a, find the load voltage when $R_L = 10 \text{ k}\Omega$.

Example 17-14

MultiSim

An ammeter is used for the load resistance in Fig. 17-32a. What is the current through the ammeter?

SOLUTION In Fig. 17-32b, the load resistance is ideally zero and the load current is:

$$i_L = \frac{3 \text{ V}}{15 \text{ k}\Omega} = 0.2 \text{ mA}$$

Without Thevenin's theorem, this would be a very difficult problem to solve.

PRACTICE PROBLEM 17-14 Repeat Example 17-14 with an input voltage of 20 mV.

Summary

SEC. 17-1 THE DIFFERENTIAL AMPLIFIER

A diff amp is the typical input stage of an op amp. It has no coupling or bypass capacitors. Because of this, it has no lower cutoff frequency. The input may be differential, noninverting, or inverting. The output may be single-ended or differential.

SEC. 17-2 DC ANALYSIS OF A DIFF AMP

The diff amp uses two-supply emitter bias to produce the tail current. When a diff amp is perfectly symmetrical, each emitter current is half the tail current. Ideally, the voltage across the emitter resistor equals the negative supply voltage.

SEC. 17-3 AC ANALYSIS OF A DIFF AMP

Because the tail current is ideally constant, an increase in the emitter current of one transistor produces a decrease in the emitter current of the other transistor. With a differential output, the voltage gain is R_C/r_e . With a

single-ended output, the voltage gain is half as much.

SEC. 17-4 INPUT CHARACTERISTICS OF AN OP AMP

Three important input characteristics of an op amp are the input bias current, input offset current, and input offset voltage. The input bias and offset currents produce unwanted input error voltages when they flow through the base resistors. The input offset voltage is an equivalent input error produced by differences in R_C and V_{BE} .

SEC. 17-5 COMMON-MODE GAIN

Most static, interference, and other kinds of electromagnetic pickup are common-mode signals. The diff amp discriminates against common-mode signals. The CMRR is the voltage gain divided by the common-mode gain. The higher the CMRR, the better.

SEC. 17-6 INTEGRATED CIRCUITS

Monolithic ICs are complete circuit functions on a single chip such as amplifiers, voltage regulators, and

computer circuits. For high-power applications, thin-film, thick-film, and hybrid ICs may be used. SSI refers to fewer than 12 components, MSI to between 12 and 100 components, LSI to more than 100 components, VLSI to more than 1000 components, and ULSI to more than 1 million components.

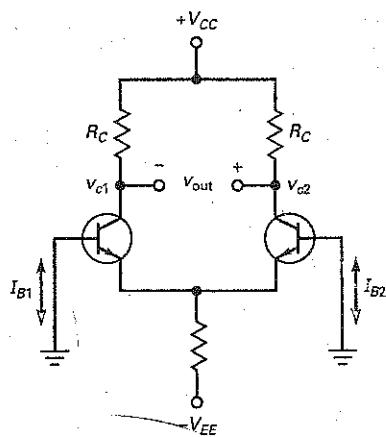
SEC. 17-7 THE CURRENT MIRROR

The current mirror is used in ICs because it is a convenient way to create current sources and active loads. The advantages of using current mirrors are increases in voltage gain and CMRR.

SEC. 17-8 THE LOADED DIFF AMP

When a load resistance is used with a diff amp, the best approach is to use Thevenin's theorem. Calculate the ac output voltage v_{out} as discussed in earlier sections. This voltage is equal to the Thevenin voltage. Use a Thevenin resistance of $2R_C$ with a differential output and R_C with a single-ended output.

Definitions



(17-1) Differential output:

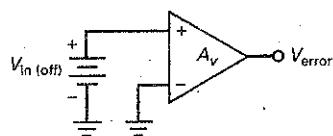
$$V_{out} = V_{c2} - V_{c1}$$

(17-12) Input bias current:

$$I_{in(bias)} = \frac{I_{B1} + I_{B2}}{2}$$

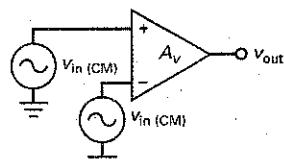
(17-13) Input offset current:

$$I_{in(off)} = I_{B1} - I_{B2}$$



(17-15) Input offset voltage:

$$V_{in(off)} = \frac{V_{error}}{A_v}$$



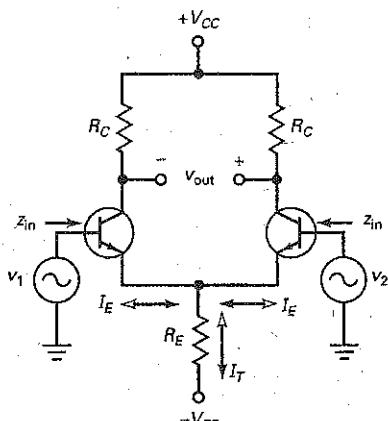
(17-21) Common-mode rejection ratio:

$$CMRR = \frac{A_v}{A_{v(CM)}}$$

(17-22) Decibel CMRR:

$$CMRR_{dB} = 20 \log CMRR$$

Derivations



(17-2) Differential output:

$$V_{out} = A_v(v_1 - v_2)$$

(17-5) Tail current:

$$I_T = \frac{V_{EE}}{R_E}$$

(17-6) Emitter current:

$$I_E = \frac{I_T}{2}$$

(17-9) Single-ended output:

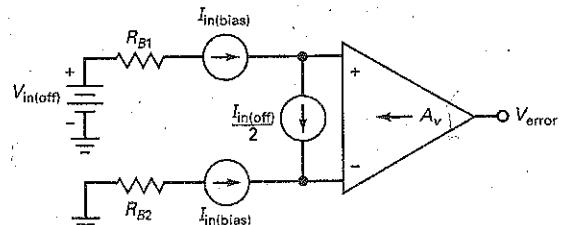
$$A_v = \frac{R_C}{2r'_e}$$

(17-10) Differential output:

$$A_v = \frac{R_C}{r'_e}$$

(17-11) Input impedance:

$$Z_{in} = 2\beta r'_e$$



(17-16) First error voltage:

$$V_{1\text{err}} = (R_{B1} - R_{B2}) I_{\text{in(bias)}}$$

(17-17) Second error voltage:

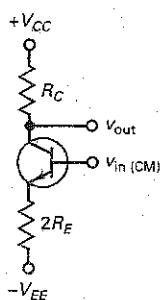
$$V_{2\text{err}} = (R_{B1} + R_{B2}) \frac{I_{\text{in(off)}}}{2}$$

(17-18) Third error voltage:

$$V_{3\text{err}} = V_{\text{in(off)}}$$

(17-19) Total output error voltage:

$$V_{\text{error}} = A_v (V_{1\text{err}} + V_{2\text{err}} + V_{3\text{err}})$$



(17-20) Common-mode voltage gain:

$$A_v(\text{CM}) = \frac{R_C}{2R_E}$$

Student Assignments

1. Monolithic ICs are
 - a. Forms of discrete circuits
 - b. On a single chip
 - c. Combinations of thin-film and thick-film circuits
 - d. Also called hybrid ICs
2. The op amp can amplify
 - a. AC signals only
 - b. DC signals only
 - c. Both ac and dc signals
 - d. Neither ac nor dc signals
3. Components are soldered together in
 - a. Discrete circuits
 - b. Integrated circuits
 - c. SSI
 - d. Monolithic ICs
4. The tail current of a diff amp is
 - a. Half of either collector current
 - b. Equal to either collector current
 - c. Two times either collector current
 - d. Equal to the difference in base currents
5. The node voltage at the top of the tail resistor is closest to
 - a. Collector supply voltage
 - b. Zero
 - c. Emitter supply voltage
 - d. Tail current times base resistance
6. The input offset current equals the
 - a. Difference between the two base currents
 - b. Average of the two base currents
7. The tail current equals the
 - a. Difference between the two emitter currents
 - b. Sum of the two emitter currents
 - c. Collector current divided by current gain
 - d. Collector voltage divided by collector resistance
8. The voltage gain of a diff amp with an unloaded differential output is equal to R_C divided by
 - a. r'_e
 - b. $r'_e/2$
 - c. $2r'_e$
 - d. R_E
9. The input impedance of a diff amp equals r'_e times
 - a. 0
 - b. R_C
 - c. R_E
 - d. 2β
10. A dc signal has a frequency of
 - a. 0 Hz
 - b. 60 Hz
 - c. 0 to more than 1 MHz
 - d. 1 MHz
11. When the two input terminals of a diff amp are grounded,
 - a. The base currents are equal
 - b. The collector currents are equal
12. One source of output error voltage is
 - a. Input bias current
 - b. Difference in collector resistors
 - c. Tail current
 - d. Common-mode voltage gain
13. A common-mode signal is applied to
 - a. The noninverting input
 - b. The inverting input
 - c. Both inputs
 - d. The top of the tail resistor
14. The common-mode voltage gain is
 - a. Smaller than the voltage gain
 - b. Equal to the voltage gain
 - c. Greater than the voltage gain
 - d. None of the above
15. The input stage of an op amp is usually a
 - a. Diff amp
 - b. Class B push-pull amplifier
 - c. CE amplifier
 - d. Swamped amplifier
16. The tail of a diff amp acts like a
 - a. Battery
 - b. Current source
 - c. Transistor
 - d. Diode

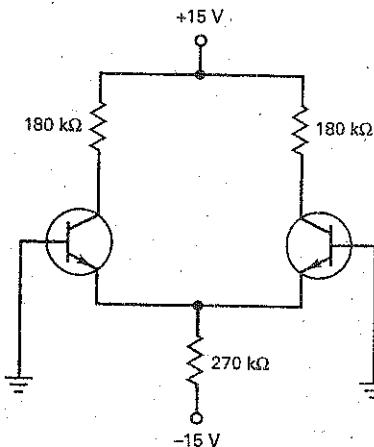
17. The common-mode voltage gain of a diff amp is equal to R_C divided by
- r'_e
 - $r'_e/2$
 - $2r'_e$
 - $2R_E$
18. When the two bases are grounded in a diff amp, the voltage across each emitter diode is
- Zero
 - 0.7 V
 - The same
 - High
19. The common-mode rejection ratio is
- Very low
 - Often expressed in decibels
- c. Equal to the voltage gain
d. Equal to the common-mode voltage gain
20. The typical input stage of an op amp has a
- Single-ended input and single-ended output
 - Single-ended input and differential output
 - Differential input and single-ended output
 - Differential input and differential output
21. The input offset current is usually
- Less than the input bias current
 - Equal to zero
 - Less than the input offset voltage
 - Unimportant when a base resistor is used
22. With both bases grounded, the only offset that produces an error is the
- Input offset current
 - Input bias current
 - Input offset voltage
 - β
23. The voltage gain of a loaded diff amp is
- Larger than the unloaded voltage gain
 - Equal to $\frac{R_C}{r'_e}$
 - Smaller than the unloaded voltage gain
 - Impossible to determine

Problems

SEC. 17-2 DC ANALYSIS OF A DIFF AMP

- 17-1 What are the ideal currents and voltages in Fig. 17-33?
- 17-2 **Multisim** Repeat Prob. 17-1 using the second approximation.
- 17-3 What are the ideal currents and voltages in Fig. 17-34?
- 17-4 **Multisim** Repeat Prob. 17-3 using the second approximation.

Figure 17-33



SEC. 17-3 AC ANALYSIS OF A DIFF AMP

- 17-5 In Fig. 17-35, what is the ac output voltage? If $\beta = 275$, what is the input impedance of the diff amp? Use the ideal approximation to get the tail current.
- 17-6 Repeat Prob. 17-5 using the second approximation.

- 17-7 Repeat Prob. 17-5 by grounding the noninverting input and using an input of $v_2 = 1 \text{ mV}$.

SEC. 17-4 INPUT CHARACTERISTICS OF AN OP AMP

- 17-8 The diff amp of Fig. 17-36 has $A_v = 360$, $I_{\text{in(bias)}} = 600 \text{ nA}$, $I_{\text{in(off)}} = 100 \text{ nA}$, and $V_{\text{in(off)}} = 1 \text{ mV}$. What is the output error voltage? If a matching base resistor is used, what is the output error voltage?
- 17-9 The diff amp of Fig. 17-36 has $A_v = 250$, $I_{\text{in(bias)}} = 1 \mu\text{A}$, $I_{\text{in(off)}} = 200 \text{ nA}$, and $V_{\text{in(off)}} = 5 \text{ mV}$. What is the output error voltage? If a matching base resistor is used, what is the output error voltage?

SEC. 17-5 COMMON-MODE GAIN

- 17-10 What is the common-mode voltage gain of Fig. 17-37? If a common-mode voltage of $20 \mu\text{V}$ exists on both bases, what is the common-mode output voltage?
- 17-11 In Fig. 17-37, $v_{in} = 2 \text{ mV}$ and $v_{in(CM)} = 5 \text{ mV}$. What is the ac output voltage?
- 17-12 A 741C is an op amp with $A_v = 100,000$ and a minimum CMRR_{dB} = 70 dB. What is the common-mode voltage gain? If a desired common-mode signal each has a value of $5 \mu\text{V}$, what is the output voltage?
- 17-13 If the supply voltages are reduced to $+10 \text{ V}$ and -10 V , what is the common-mode rejection ratio of Fig. 17-37? Express the answer in decibels.

- 17-14 The data sheet of an op amp gives $A_v = 150,000$ and CMRR = 85 dB. What is the common-mode voltage gain?

SEC. 17-8 THE LOADED DIFF AMP

- 17-15 A load resistance of $27 \text{ k}\Omega$ is connected across the differential output of Fig. 17-36. What is the load voltage?
- 17-16 What is the load current in Fig. 17-36 if an ammeter is across the output?

Figure 17-34

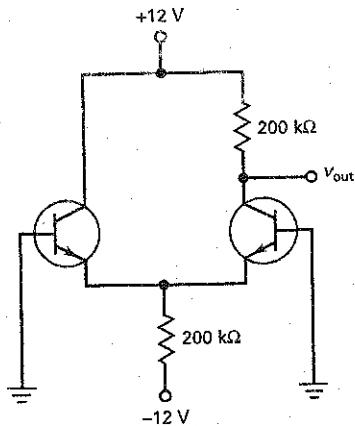


Figure 17-36

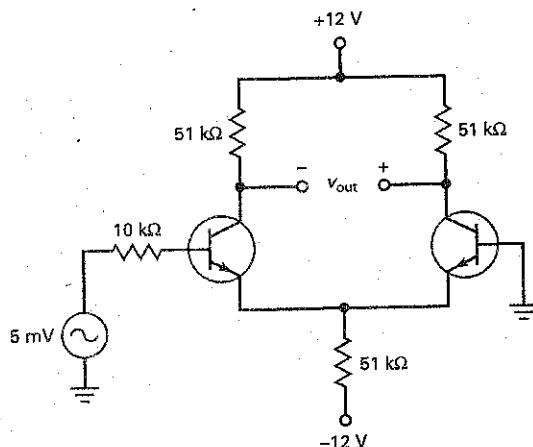


Figure 17-35

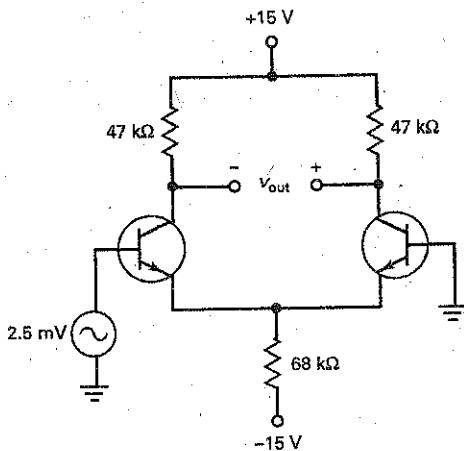
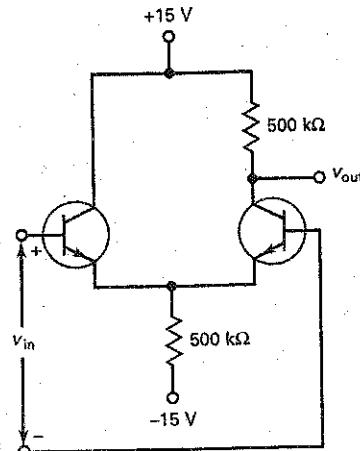


Figure 17-37



Troubleshooting

17-17 Somebody builds the diff amp of Fig. 17-35 without a ground on the inverting input. What does the output voltage equal? Based on your preceding answer, what does any diff amp or op amp need to work properly?

17-18 In Fig. 17-34, 20 kΩ is mistakenly used for the upper 200 kΩ. What does the output voltage equal?

17-19 In Fig. 17-34, V_{out} is almost zero. The input bias current is 80 nA. Which of the following is the trouble?

- Upper 200 kΩ shorted
- Lower 200 kΩ open
- Left base open
- Both inputs shorted together

Critical Thinking

17-20 In Fig. 17-34, the transistors are identical with $\beta_{dc} = 200$. What is the output voltage?

17-21 What are base voltages in Fig. 17-34 if each transistor has $\beta_{dc} = 300$?

17-22 In Fig. 17-38, transistors Q_3 and Q_5 are connected to act like compensating diodes for Q_4 and Q_6 . What is the tail current? The current through the active load?

Figure 17-38

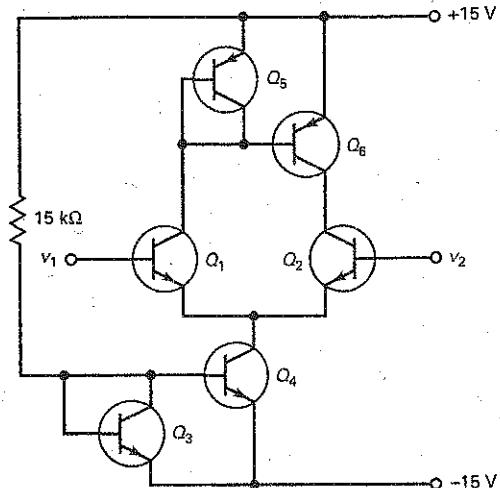
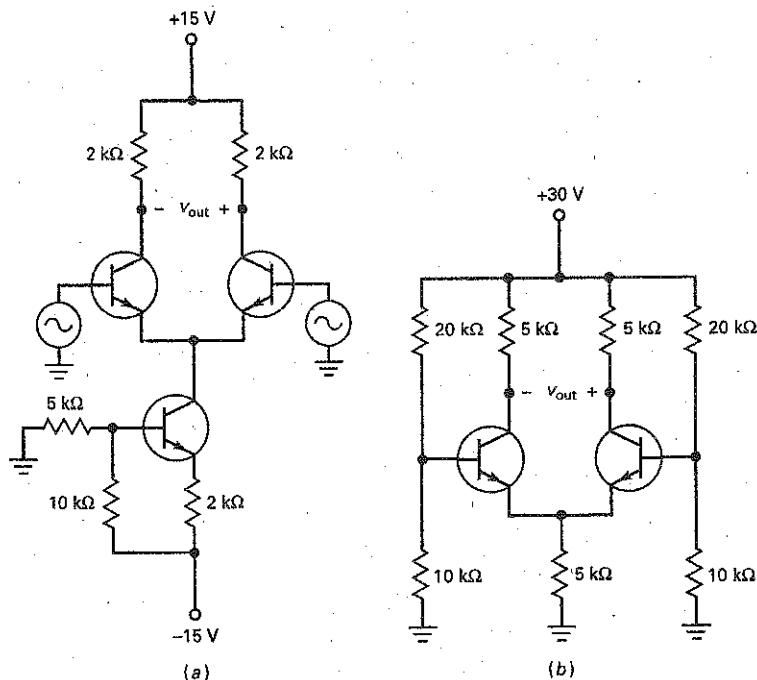


Figure 17-39



Up-Down Circuit Analysis

17-27 In Fig. 17-40, predict the response of each dependent variable in the rows labeled I_{B1} and I_{B2} .

17-28 In Fig. 17-40, predict the response of each dependent variable in the rows labeled R_E and R_C .

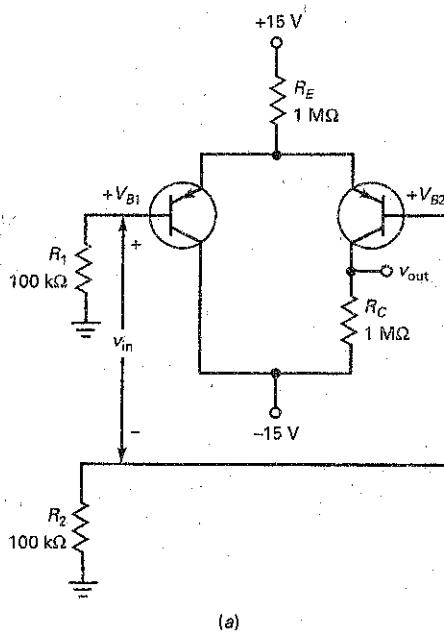
17-23 The $15\text{ k}\Omega$ of Fig. 17-38 is changed to get a tail current of $15\text{ }\mu\text{A}$. What is the new value of resistance?

17-24 At room temperature, the output voltage of Fig. 17-34 has a value of 6.0 V . As the temperature increases, the V_{BE} of each emitter diode decreases. If the left V_{BE} decreases 2 mV per degree and the right V_{BE} decreases 2.1 mV per degree, what is the output voltage at 75°C ?

17-25 The dc resistance of each signal source in Fig. 17-39a is zero. What is the r'_e of each transistor? If the ac output voltage is between the collectors, what is the voltage gain?

17-26 If the transistors are identical in Fig. 17-39b, what is the tail current? The voltage between the left collector and ground? Between the right collector and ground?

Figure 17-40



(a)

Up-Down Circuit Analysis

Increase	V_{B1}	V_{B2}	V_{in}	V_{out}	I_T
I_{B1}					
I_{B2}					
R_E					
R_C					
$\pm V_{CC}$					

(b)

Job-Interview Questions

1. Please draw the six configurations of a diff amp and identify the inputs and outputs as noninverting, inverting, single-ended, or differential.
2. Draw a diff amp with a differential input and single-ended output. Tell me how you would calculate the tail current, the emitter currents, and the collector voltages.
3. Draw any diff amp that has a voltage gain of R_C/r_e . Now, draw any other diff amp that has a voltage gain of $R_C/2r_e$.
4. Tell me what a common-mode signal is and what advantage a diff amp has when this kind of signal is present at the input.
5. A diff amp has an ammeter connected across its differential output. How would you go about calculating the current through the ammeter?
6. Assume that you have a diff amp circuit with a tail resistor. You have determined that the CMRR of the circuit is not acceptable. How could you improve the CMRR?
7. Explain the concept of a current mirror and why it is used.
8. Should CMRR be a large or a small number? Why?
9. In a diff amp, both emitters are tied together and get current from a common resistor. If you were to replace the common resistor with any type of component, what would you use to improve operation?
10. Why does a diff amp have a higher input impedance than a CE amplifier?
11. What does a current mirror simulate; that is, what is it used as?
12. What are the advantages of using current mirrors?
13. How do you test a 741 op amp with an ohmmeter?

Self-Test Answers

- | | | |
|------|-------|-------|
| 1. b | 9. d | 17. d |
| 2. c | 10. a | 18. c |
| 3. a | 11. c | 19. b |
| 4. c | 12. b | 20. c |
| 5. b | 13. c | 21. a |
| 6. a | 14. a | 22. c |
| 7. b | 15. a | 23. c |
| 8. a | 16. b | |

Practice Problem Answers

- | | | |
|--|--|--|
| 17-1 $I_T = 3 \text{ mA}$; $I_E = 1.5 \text{ mA}$; $V_C = 7.5 \text{ V}$;
$V_E = 0 \text{ V}$ | 17-7 $I_T = 30 \mu\text{A}$; $r'_e = 1.67 \text{ k}\Omega$; $A_v = 300$;
$V_{out} = 2.1 \text{ V}$; $z_m = 1 \text{ M}\Omega$ | 17-12 $A_{v(CM)} = 3.16$; $V_{out1} = 0.1 \text{ V}$;
$V_{out2} = 3.16 \mu\text{V}$ |
| 17-2 $I_T = 2.86 \text{ mA}$; $I_E = 1.42 \text{ mA}$;
$V_C = 7.85 \text{ V}$; $V_E = -0.7 \text{ V}$ | 17-9 $V_{error} = 638 \text{ mV}$ | 17-13 $V_L = 1.2 \text{ V}$ |
| 17-3 $I_T = 3.77 \text{ mA}$; $I_E = 1.88 \text{ mA}$;
$V_E = 6.35 \text{ V}$ | 17-10 $A_{v(CM)} = 0.25$; $V_{out} = 0.25 \text{ V}$ | 17-14 $I_L = 0.4 \text{ mA}$ |
| 17-4 $I_E = 1.5 \text{ mA}$; $r'_e = 1.67 \Omega$; $A_v = 300$;
$V_{out} = 300 \text{ mV}$; $z_{in(base)} = 10 \text{ k}\Omega$ | 17-11 $V_{out1} = 200 \text{ mV}$; $V_{out2} = 0.5 \text{ mV}$;
$V_{out} = 200 \text{ mV} + 0.5 \text{ mV}$ | |

18

Operational Amplifiers

- Although some high-power op amps are available, most are low-power devices with a maximum power rating of less than a watt. Some op amps are optimized for their bandwidth, others for low input offsets, others for low noise, and so on. This is why the variety of commercially available op amps is so large. You can find an op amp for almost any analog application.

Op amps are some of the most basic active components in analog systems. For instance, by connecting two external resistors, we can adjust the voltage gain and bandwidth of an op amp to our exact requirements. Furthermore, with other external components, we can build waveform converters, oscillators, active filters, and other interesting circuits.

Chapter Outline

- 18-1 Introduction to Op Amps
- 18-2 The 741 Op Amp
- 18-3 The Inverting Amplifier
- 18-4 The Noninverting Amplifier
- 18-5 Two Op-Amp Applications
- 18-6 Linear ICs
- 18-7 Op Amps as Surface-Mount Devices

Objectives

After studying this chapter, you should be able to:

- List the characteristics of ideal op amps and 741 op amps.
- Define slew rate and use it to find the power bandwidth of an op amp.
- Analyze an op-amp inverting amplifier.
- Analyze an op-amp noninverting amplifier.
- Explain how summing amplifiers and voltage followers work.
- List other linear integrated circuits and discuss how they are applied.

Vocabulary

BIFET op amp	noninverting amplifier	slew rate
bootstrapping	nulling circuit	summing amplifier
closed-loop voltage gain	open-loop bandwidth	virtual ground
compensating capacitor	open-loop voltage gain	virtual short
first-order response	output error voltage	voltage-controlled voltage source (VCS)
gain-bandwidth product (GBW)	power bandwidth	voltage follower
inverting amplifier	power supply rejection ratio (PSRR)	voltage step
mixer	short-circuit output current	

18-1 Introduction to Op Amps

Figure 18-1 shows a block diagram of an op amp. The input stage is a diff amp, followed by more stages of gain, and a class B push-pull emitter follower. Because a diff amp is the first stage, it determines the input characteristics of the op amp. In most op amps the output is single-ended, as shown. With positive and negative supplies, the single-ended output is designed to have a quiescent value of zero. This way, zero input voltage ideally results in zero output voltage.

Not all op amps are designed like Fig. 18-1. For instance, some do not use a class B push-pull output, and others may have a double-ended output. Also, op amps are not as simple as Fig. 18-1 suggests. The internal design of a monolithic op amp is very complicated, using dozens of transistors as current mirrors, active loads, and other innovations that are not possible in discrete designs. For our needs, Fig. 18-1 captures two important features that apply to typical op amps: the differential input and the single-ended output.

Figure 18-2a is the schematic symbol of an op amp. It has noninverting and inverting inputs and a single-ended output. Ideally, this symbol means that the

Figure 18-1 Block diagram of an op amp.

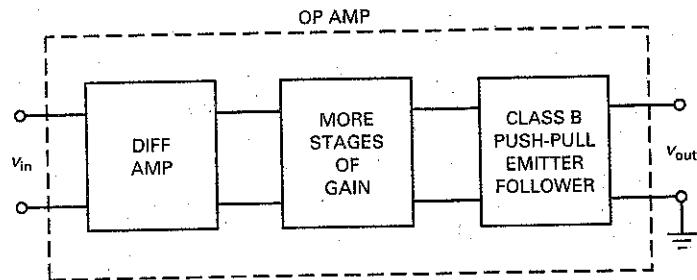


Figure 18-2 (a) Schematic symbol for op amp; (b) equivalent circuit of op amp.

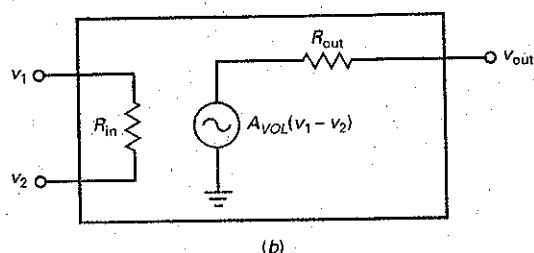
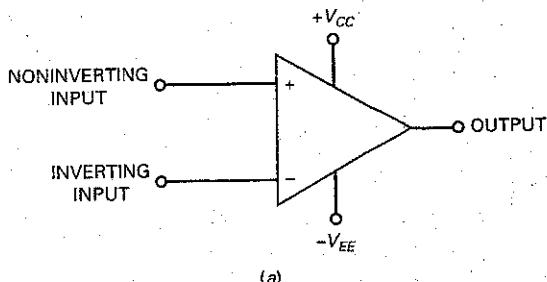


Table 18-1 Typical Op-Amp Characteristics

Quantity	Symbol	Ideal	LM741C	LF157A
Open-loop voltage gain	A_{VOL}	Infinite	100,000	200,000
Unity-gain frequency	f_{unity}	Infinite	1 MHz	20 MHz
Input resistance	R_{in}	Infinite	2 MΩ	$10^{12} \Omega$
Output resistance	R_{out}	Zero	75 Ω	100 Ω
Input bias current	$I_{in(bias)}$	Zero	80 nA	30 pA
Input offset current	$I_{in(off)}$	Zero	20 nA	3 pA
Input offset voltage	$V_{in(off)}$	Zero	2 mV	1 mV
Common-mode rejection ratio	CMRR	Infinite	90 dB	100 dB

amplifier has infinite voltage gain, infinite input impedance, and zero output impedance. The ideal op amp represents a perfect voltage amplifier and is often referred to as a **voltage-controlled voltage source (VCVS)**. We can visualize a VCVS as shown in Fig. 18-2b, where R_{in} is infinite and R_{out} is zero.

Table 18-1 summarizes the characteristics of an ideal op amp. The ideal op amp has infinite voltage gain, infinite unity-gain frequency, infinite input impedance, and infinite CMRR. It also has zero output resistance, zero bias current, and zero offsets. This is what manufacturers would build if they could. What they actually can build approaches these ideal values.

For instance, the LM741C of Table 18-1 is a standard op amp, a classic that has been available since the 1960s. Its characteristics are the minimum of what to expect from a monolithic op amp. The LM741C has a voltage gain of 100,000, a unity-gain frequency of 1 MHz, an input impedance of 2 MΩ, and so on. Because the voltage gain is so high, the input offsets can easily saturate the op amp. This is why practical circuits need external components between the input and output of an op amp to stabilize the voltage gain. For instance, in many applications negative feedback is used to adjust the overall voltage gain to a much lower value in exchange for stable linear operation.

When no feedback path (or loop) is used, the voltage gain is maximum and is called the **open-loop voltage gain**, designated A_{VOL} . In Table 18-1, notice that the A_{VOL} of the LM741C is 100,000. Although not infinite, this open-loop voltage gain is very high. For instance, an input as small as 10 μV produces an output of 1 V. Because the open-loop voltage gain is very high, we can use heavy negative feedback to improve the overall performance of a circuit.

The 741C has a unity-gain frequency of 1 MHz. This means that we can get usable voltage gain almost as high as 1 MHz. The 741C has an input resistance of 2 MΩ, an output resistance of 75 Ω, an input bias current of 80 nA, an input offset current of 20 nA, an input offset voltage of 2 mV, and a CMRR of 90 dB.

When higher input resistance is needed, a designer can use a **BIFET op amp**. This type of op amp incorporates JFETs and bipolar transistors on the same chip. The JFETs are used in the input stage to get smaller input bias and offset currents; the bipolar transistors are used in the later stages to get more voltage gain.

The LF157A is an example of a BIFET op amp. As shown in Table 18-1, the input bias current is only 30 pA, and the input resistance is $10^{12} \Omega$. The

GOOD TO KNOW

Most modern general-purpose op amps are now produced with BIFET technology because this provides superior performance over bipolar op amps. BIFET op amps, being more modern, generally have more enhanced performance characteristics, which include wider bandwidth, higher slew rate, larger power output, higher input impedances, and lower bias currents.

LF157A has a voltage gain of 200,000 and a unity-gain frequency of 20 MHz. With this device, we can get voltage gain up to 20 MHz.

18-2 The 741 Op Amp

In 1965 Fairchild Semiconductor introduced the μ A709, the first widely used monolithic op amp. Although successful, this first-generation op amp had many disadvantages. These led to an improved op amp known as the μ A741. Because it is inexpensive and easy to use, the μ A741 has been an enormous success. Other 741 designs have appeared from various manufacturers. For instance, Motorola produces the MC1741, National Semiconductor the LM741, and Texas Instruments the SN72741. All these monolithic op amps are equivalent to the μ A741 because they have the same specifications on their data sheets. For convenience, most people drop the prefixes and refer to this widely used op amp simply as the 741.

An Industry Standard

The 741 has become an industry standard. As a rule, you try to use it first in your designs. In cases when you cannot meet a design specification with a 741, you upgrade to a better op amp. Because it is a standard, we will use the 741 as a basic device in our discussions. Once you understand the 741, you can branch out to other op amps.

Incidentally, the 741 has different versions numbered 741, 741A, 741C, 741E, and 741N. These differ in their voltage gain, temperature range, noise level, and other characteristics. The 741C (the C stands for "commercial grade") is the least expensive and most widely used. It has an open-loop voltage gain of 100,000, an input impedance of $2\text{ M}\Omega$, and an output impedance of $75\text{ }\Omega$. Fig. 18-3 shows three popular package styles and their respective pin outs.

Figure 18-3 The 741 package style and pin outs: (a) Dual-in-line; (b) ceramic flatpak; and (c) metal can.

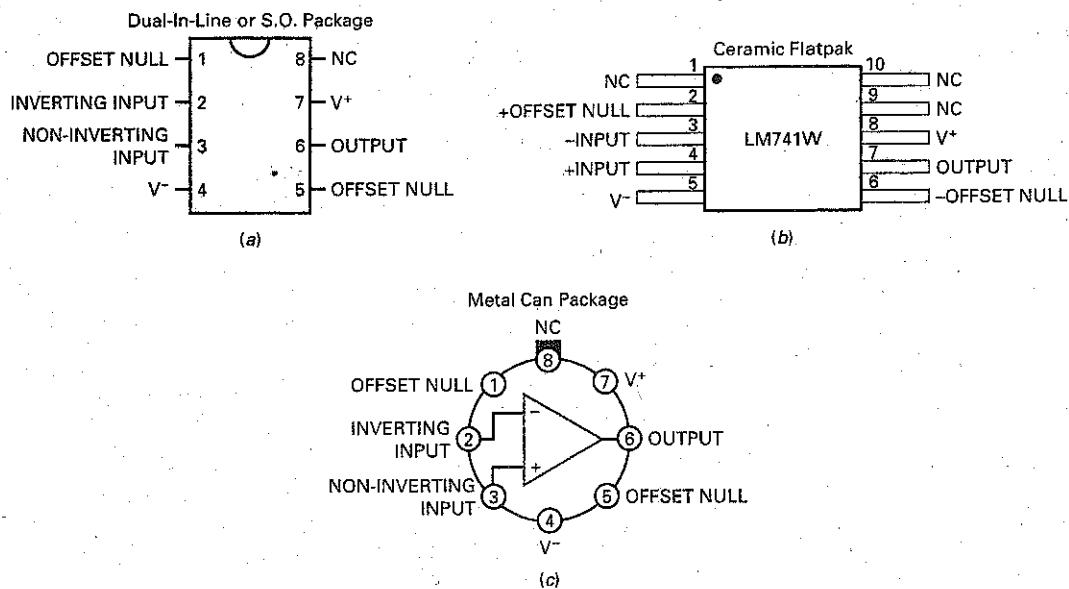
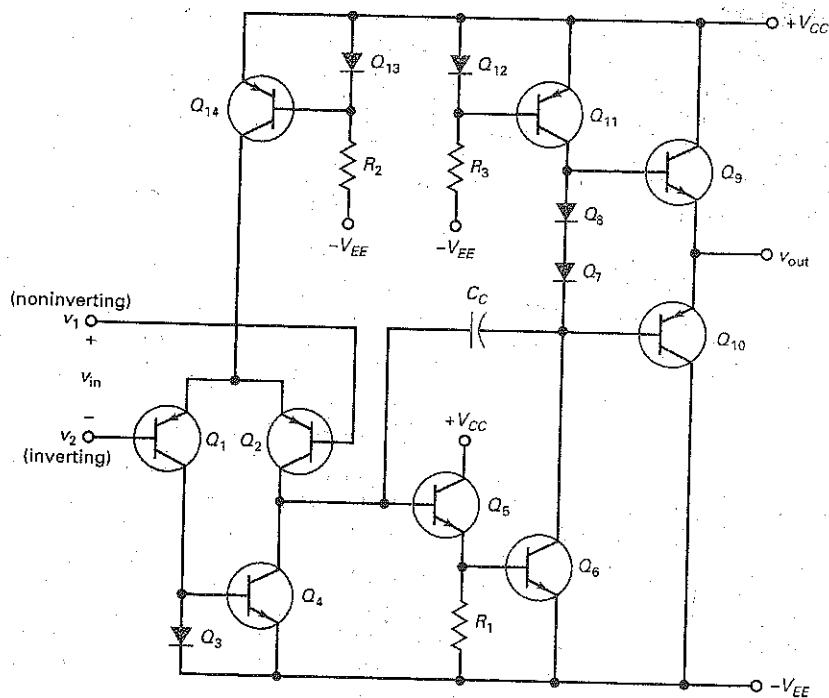


Figure 18-4 Simplified schematic diagram of 741.



The Input Diff Amp

Figure 18-4 is a simplified schematic diagram of the 741. This circuit is equivalent to the 741 and many later-generation op amps. You do not need to understand every detail about the circuit design, but you should have a general idea of how the circuit works. With that in mind, here is the basic idea behind a 741.

The input stage is a diff amp (Q_1 and Q_2). In the 741, Q_{14} is a current source that replaces the tail resistor. R_2 , Q_{13} , and Q_{14} are a current mirror that produces the tail current for Q_1 and Q_2 . Instead of using an ordinary resistor as the collector resistor of the diff amp, the 741 uses an active load resistor. This active load Q_4 acts like a current source with an extremely high impedance. Because of this, the voltage gain of the diff amp is much higher than with a passive load resistor.

The amplified signal from the diff amp drives the base of Q_5 , an emitter follower. This stage steps up the impedance level to avoid loading down the diff amp. The signal out of Q_5 goes to Q_6 . Diodes Q_7 and Q_8 are part of the biasing for the final stage. Q_{11} is an active load resistor for Q_6 . Therefore, Q_6 and Q_{11} are like a CE driver stage with a very high voltage gain.

The Final Stage

The amplified signal out of the CE driver stage (Q_6) goes to the final stage, which is a class B push-pull emitter follower (Q_9 and Q_{10}). Because of the split supply (equal positive V_{CC} and negative V_{EE} voltages), the quiescent output is ideally 0 V when the input voltage is zero. Any deviation from 0 V is called the **output error voltage**.

GOOD TO KNOW

Although the 741 is usually connected to both a positive and a negative supply voltage, the op amp can still be operated using a single supply voltage. For example, the $-V_{EE}$ input could be grounded, and the $+V_{CC}$ input could be connected to a positive dc supply voltage.

When v_1 is greater than v_2 , the input voltage v_{in} produces a positive output voltage v_{out} . When v_2 is greater than v_1 , the input voltage v_{in} produces a negative output voltage v_{out} . Ideally, v_{out} can be as positive as $+V_{CC}$ and as negative as $-V_{EE}$ before clipping occurs. The output swing is within 1 to 2 V of each supply voltage because of voltage drops inside the 741.

Active Loading

In Fig. 18-4, we have two examples of *active loading* (using transistors instead of resistors for loads) as discussed in Chap. 17. First, there is the active load Q_4 on the input diff amp. Second, there is the active load Q_{11} in the CE driver stage. Because current sources have high output impedances, active loads produce much higher voltage gain than is possible with resistors. These active loads produce a typical voltage gain of 100,000 for the 741C. Active loading is very popular in integrated circuits (ICs) because it is easier and less expensive to fabricate transistors on a chip than it is to fabricate resistors.

Frequency Compensation

In Fig. 18-4, C_c is a **compensating capacitor**. Because of the Miller effect (discussed in Chap. 16), this small capacitor (typically 30 pF) is multiplied by the voltage gain of Q_5 and Q_6 to get a much larger equivalent capacitance of:

$$C_{in(M)} = (A_v + 1)C_c$$

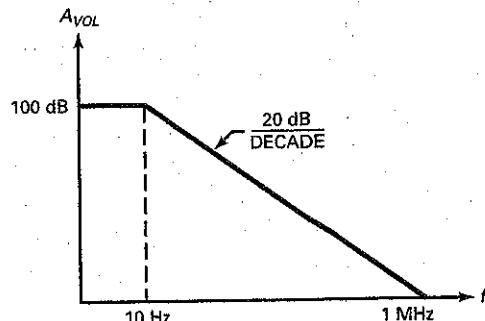
where A_v is the voltage gain of the Q_5 and Q_6 stages.

The resistance facing this Miller capacitance is the output impedance of the diff amp. Therefore, we have a lag circuit, as described in Chap. 16. This lag circuit produces a cutoff frequency of 10 Hz in a 741C. The open-loop gain of the op amp is down 3 dB at this cutoff frequency. Then, A_{VOL} decreases approximately 20 dB per decade until reaching the unity-gain frequency.

Figure 18-5 shows the ideal Bode plot of open-loop voltage gain versus frequency. The 741C has an open-loop voltage gain of 100,000, equivalent to 100 dB. Since the open-loop cutoff frequency is 10 Hz, the voltage gain breaks at 10 Hz and then rolls off at a rate of 20 dB per decade until it is 0 dB at 1 MHz.

A later chapter discusses *active filters*, circuits that use op amps, resistors, and capacitors to tailor the frequency response for different applications. At that time, we will discuss circuits that produce a first-order response (20 dB per decade rolloff), a second-order response (40 dB per decade rolloff), a third-order response (60 dB per decade rolloff), and so on. An op amp that is internally compensated, such as the 741C, has a **first-order response**.

Figure 18-5 Ideal Bode plot of open-loop voltage gain for 741C.



Incidentally, not all op amps are internally compensated. Some require the user to connect an external compensating capacitor to prevent oscillations. The advantage of using external compensation is that a designer has more control over the high-frequency performance. Although an external capacitor is the simplest way to compensate, more complicated circuits can be used that not only provide compensation but also produce a higher f_{unity} than is possible with internal compensation.

Bias and Offsets

As discussed in Chap. 17, a diff amp has input bias and offsets that produce an output error when there is no input signal. In many applications, the output error is small enough to ignore. But when the output error cannot be ignored, a designer can reduce it by using equal base resistors. This eliminates the problem of bias current, but not the offset current or offset voltage.

This is why it is best to eliminate output error by using the **nulling circuit** given on the data sheet. This recommended nulling circuit works with the internal circuitry to eliminate the output error and also to minimize *thermal drift*, a slow change in output voltage caused by the effect of changing temperature on op-amp parameters. Sometimes, the data sheet of an op amp does not include a nulling circuit. In this case, we have to apply a small input voltage to null the output. We will discuss this method later.

Figure 18-6 shows the nulling method suggested on the data sheet of a 741C. The ac source driving the inverting input has a Thevenin resistance of R_B . To neutralize the effect of input bias current (80 nA) flowing through this source resistance, a discrete resistor of equal value is added to the noninverting input, as shown.

To eliminate the effect of an input offset current of 20 nA and an input offset voltage of 2 mV, the data sheet of a 741C recommends using a 10-k Ω potentiometer between pins 1 and 5. By adjusting this potentiometer with no input signal, we can null or zero the output voltage.

Common-Mode Rejection Ratio

For a 741C, CMRR is 90 dB at low frequencies. Given equal signals, one a desired signal and the other a common-mode signal, the desired signal will be 90 dB larger at the output than the common-mode signal. In ordinary numbers, this means that the desired signal will be approximately 30,000 times larger than the common-mode signal. At higher frequencies, reactive effects degrade

Figure 18-6 Compensation and nulling used with 741C.

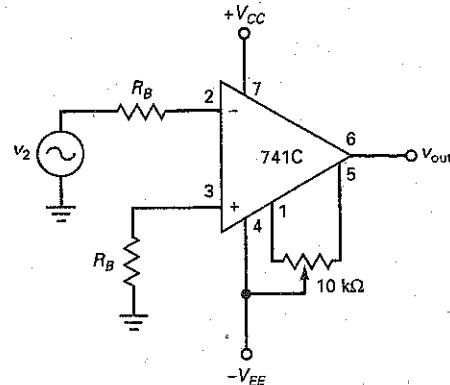
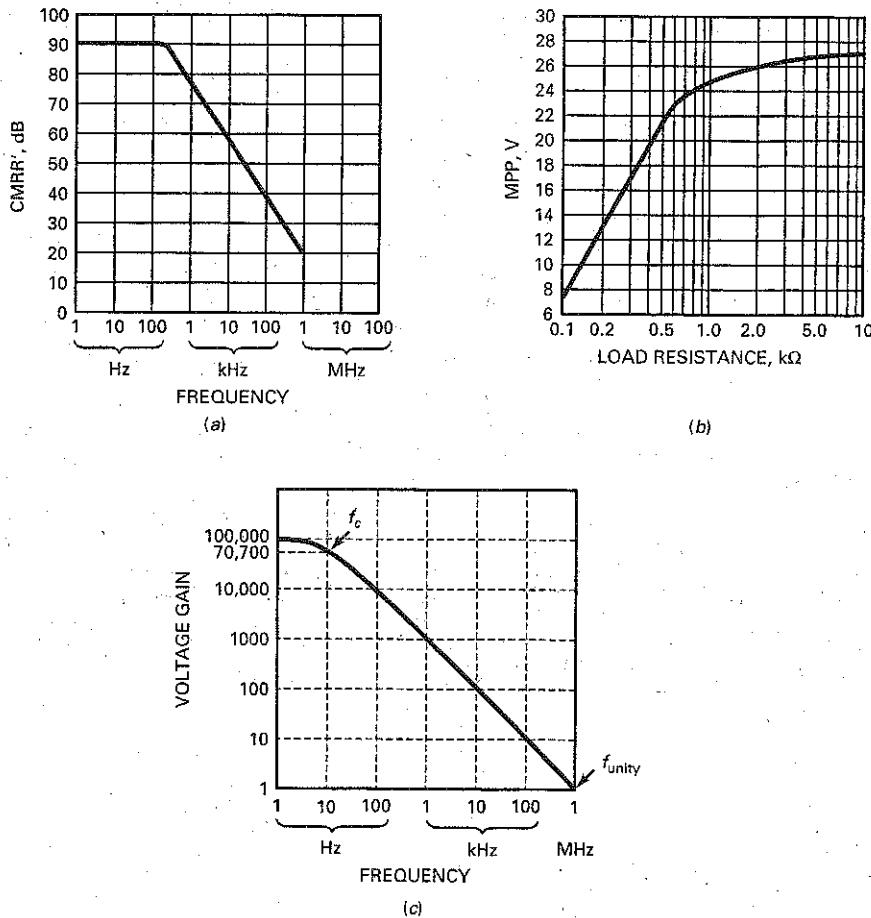


Figure 18-7 Typical 741C graphs for CMRR, MPP, and A_{VOL} .



CMRR, as shown in Fig. 18-7a. Notice that CMRR is approximately 75 dB at 1 kHz, 56 dB at 10 kHz, and so on.

Maximum Peak-to-Peak Output

As discussed in Chap. 12, the MPP value of an amplifier is the maximum peak-to-peak output that the amplifier can produce. Since the quiescent output of an op amp is ideally zero, the ac output voltage can swing positively or negatively. For load resistances that are much larger than R_{out} , the output voltage can swing almost to the supply voltages. For instance, if $V_{CC} = +15$ V and $V_{EE} = -15$ V, the MPP value with a load resistance of 10 k Ω is ideally 30 V.

With a nonideal op amp, the output cannot swing all the way to the value of the supply voltages because there are small voltage drops in the final stage of the op amp. Furthermore, when the load resistance is not large compared to R_{out} , some of the amplified voltage is dropped across R_{out} , which means that the final output voltage is smaller.

Figure 18-7b shows MPP versus load resistance for a 741C with supply voltages of +15 V and -15 V. Notice that MPP is approximately 27 V for an R_L of 10 k Ω . This means that the output saturates positively at +13.5 V and negatively

at -13.5 V. When the load resistance decreases, MPP decreases as shown. For instance, if the load resistance is only $275\ \Omega$, MPP decreases to 16 V, which means that the output saturates positively at $+8$ V and negatively at -8 V.

Short-Circuit Current

In some applications, an op amp may drive a load resistance of approximately zero. In this case, you need to know the value of the **short-circuit output current**. The data sheet of a 741C lists a short-circuit output current of 25 mA. This is the maximum output current the op amp can produce. If you are using small load resistors (less than $75\ \Omega$), don't expect to get a large output voltage because the voltage cannot be greater than the 25 mA times the load resistance.

Frequency Response

Figure 18-7c shows the small-signal frequency response of a 741C. In the mid-band, the voltage gain is $100,000$. The 741C has a cutoff frequency f_c of 10 Hz. As indicated, the voltage gain is $70,700$ (down 3 dB) at 10 Hz. Above the cutoff frequency, the voltage gain decreases at a rate of 20 dB per decade (first-order response).

The unity-gain frequency is the frequency at which the voltage gain equals 1 . In Fig. 18-7c, f_{unity} is 1 MHz. Data sheets usually specify the value of f_{unity} because it represents the upper limit on the useful gain of an op amp. For instance, the data sheet of a 741C lists an f_{unity} of 1 MHz. This means that the 741C can amplify signals up to 1 MHz. Beyond 1 MHz, the voltage gain is less than 1 and the 741C is useless. If a designer needs a higher f_{unity} , better op amps are available. For instance, the LM318 has an f_{unity} of 15 MHz, which means that it can produce usable voltage gain all the way to 15 MHz.

Slew Rate

The compensating capacitor inside a 741C performs a very important function: It prevents oscillations that would interfere with the desired signal. But there is a disadvantage. The compensating capacitor needs to be charged and discharged. This creates a speed limit on how fast the output of the op amp can change.

Here is the basic idea: Suppose the input voltage to an op amp is a positive voltage step, a sudden transition in voltage from one dc level to a higher dc level. If the op amp were perfect, we would get the ideal response shown in Fig. 18-8a. Instead, the output is the positive exponential waveform shown. This occurs because the compensating capacitor must be charged before the output voltage can change to the higher level.

In Fig. 18-8a, the initial slope of the exponential waveform is called the **slew rate**, symbolized S_R . The definition of slew rate is:

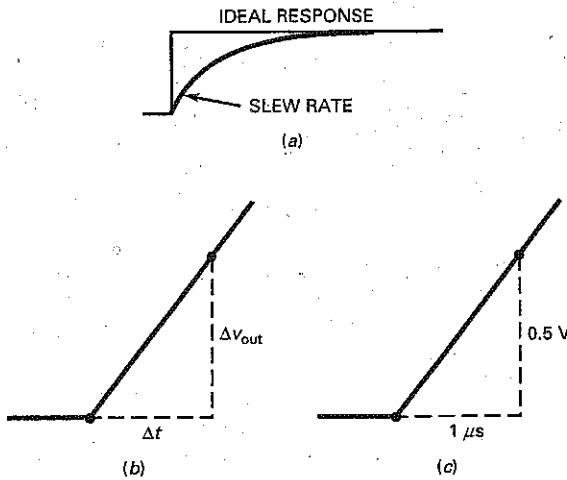
$$S_R = \frac{\Delta v_{\text{out}}}{\Delta t} \quad (18-1)$$

where the Greek letter Δ (delta) stands for "the change in." In words, the equation says that slew rate equals the change in output voltage divided by the change in time.

Figure 18-8b illustrates the meaning of slew rate. The initial slope equals the vertical change divided by the horizontal change between two points on the early part of the exponential wave. For instance, if the exponential wave increases 0.5 V during the first microsecond, as shown in Fig. 18-8c, the slew rate is:

$$S_R = \frac{0.5\ \text{V}}{1\ \mu\text{s}} = 0.5\ \text{V}/\mu\text{s}$$

Figure 18-8 (a) Ideal and actual responses to an input step voltage; (b) illustrating definition of slew rate; (c) slew rate equals $0.5 \text{ V}/\mu\text{s}$.



The slew rate represents the fastest response that an op amp can have. For instance, the slew rate of a 741C is $0.5 \text{ V}/\mu\text{s}$. This means that the output of a 741C can change no faster than 0.5 V in a microsecond. In other words, if a 741C is driven by a large step in input voltage, we do not get a sudden step in output voltage. Instead, we get an exponential output wave. The initial part of this output waveform will look like Fig. 18-8c.

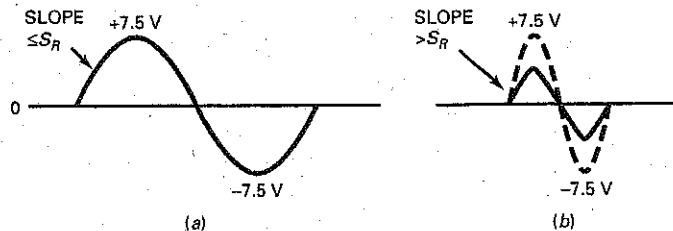
We can also get slew-rate limiting with a sinusoidal signal. Here is how it occurs: In Fig. 18-9a, the op amp can produce the output sine wave shown only if the initial slope of the sine wave is less than the slew rate. For instance, if the output sine wave has an initial slope of $0.1 \text{ V}/\mu\text{s}$, a 741C can produce this sine wave with no trouble at all because its slew rate is $0.5 \text{ V}/\mu\text{s}$. On the other hand, if the sine wave has an initial slope of $1 \text{ V}/\mu\text{s}$, the output is smaller than it should be and it looks triangular instead of sinusoidal, as shown in Fig. 18-9b.

The data sheet of an op amp always specifies the slew rate because this quantity limits the large-signal response of an op amp. If the output sine wave is very small or the frequency is very low, slew rate is no problem. But when the signal is large and the frequency is high, slew rate will distort the output signal.

With calculus, it is possible to derive this equation:

$$S_S = 2\pi f V_p$$

Figure 18-9 (a) Initial slope of a sine wave; (b) distortion occurs if initial slope exceeds slew rate.



where S_S is the initial slope of the sine wave, f is its frequency, and V_p is its peak value. To avoid slew-rate distortion of a sine wave, S_S has to be less than or equal to S_R . When the two are equal, we are at the limit, on the verge of slew-rate distortion. In this case:

$$S_R = S_S = 2\pi f V_p$$

Solving for f gives:

$$f_{\max} = \frac{S_R}{2\pi V_p} \quad (18-2)$$

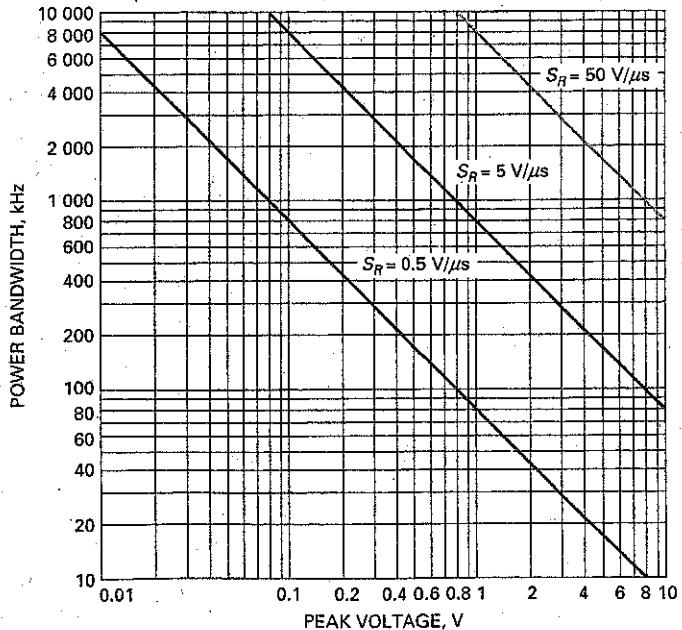
where f_{\max} is the highest frequency that can be amplified without slew-rate distortion. Given the slew rate of an op amp and the peak output voltage desired, we can use Eq. (18-2) to calculate the maximum undistorted frequency. Above this frequency, we will see slew-rate distortion on an oscilloscope.

The frequency f_{\max} is sometimes called the **power bandwidth** or *large-signal bandwidth* of the op amp. Figure 18-10 is a graph of Eq. (18-2) for three slew rates. Since the bottom graph is for a slew rate of $0.5 \text{ V}/\mu\text{s}$, it is useful with a 741C. Since the top graph is for a slew rate of $50 \text{ V}/\mu\text{s}$, it is useful with an LM318 (it has a minimum slew rate of $50 \text{ V}/\mu\text{s}$).

For instance, suppose we are using a 741C. To get an undistorted output peak voltage of 8 V, the frequency can be no higher than 10 kHz (see Fig. 18-10). One way to increase the f_{\max} is to accept less output voltage. By trading off peak value for frequency, we can improve the power bandwidth. As an example, if our application can accept a peak output voltage of 1 V, f_{\max} increases to 80 kHz.

There are two bandwidths to consider when analyzing the operation of an op-amp circuit: the small-signal bandwidth determined by the first-order response of the op amp and the large-signal or power bandwidth determined by the slew rate. More will be said about these two bandwidths later.

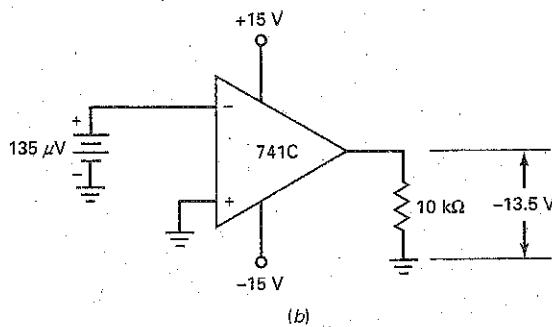
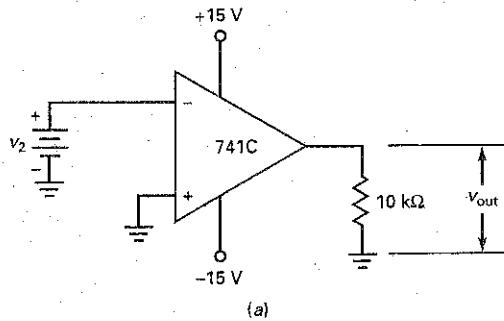
Figure 18-10 Graph of power bandwidth versus peak voltage.



Example 18-1

How much inverting input voltage does it take to drive the 741C of Fig. 18-11a into negative saturation?

Figure 18-11 Example.



SOLUTION Figure 18-11b shows that MPP equals 27 V for a load resistance of $10\text{ k}\Omega$, which translates into an output of -13.5 V for negative saturation. Since the 741C has an open-loop voltage gain of 100,000, the required input voltage is:

$$v_2 = \frac{13.5\text{ V}}{100,000} = 135\text{ }\mu\text{V}$$

Figure 18-11b summarizes the answer. As you can see, an inverting input of $135\text{ }\mu\text{V}$ produces negative saturation, an output voltage of -13.5 V .

PRACTICE PROBLEM 18-1 Repeat Example 18-1 where $A_{VOL} = 200,000$.

Example 18-2

What is the common-mode rejection ratio of a 741C when the input frequency is 100 kHz?

SOLUTION In Fig. 18-7a, we can read a CMRR of approximately 40 dB at 100 kHz. This is equivalent to 100, which means that the desired signal receives

100 times more amplification than a common-mode signal when the input frequency is 100 kHz.

PRACTICE PROBLEM 18-2 What is the CMRR of a 741C when the input frequency is 10 kHz?

Example 18-3

What is the open-loop voltage gain of a 741C when the input frequency is 1 kHz? 10 kHz? 100 kHz?

SOLUTION In Fig. 18-7c, the voltage gain is 1000 for 1 kHz, 100 for 10 kHz, and 10 for 100 kHz. As you can see, the voltage gain decreases by a factor of 10 each time the frequency increases by a factor of 10.

Example 18-4

The input voltage to an op amp is a large voltage step. The output is an exponential waveform that changes to 0.25 V in 0.1 μ s. What is the slew rate of the op amp?

SOLUTION With Eq. (18-1):

$$S_R = \frac{0.25 \text{ V}}{0.1 \mu\text{s}} = 2.5 \text{ V}/\mu\text{s}$$

PRACTICE PROBLEM 18-4 If the measured output voltage changes 0.8 V in 0.2 μ s, what is the slew rate?

Example 18-5

The LF411A has a slew rate of 15 V/ μ s. What is the power bandwidth for a peak output voltage of 10 V?

SOLUTION With Eq. (18-2):

$$f_{max} = \frac{S_R}{2\pi V_p} = \frac{15 \text{ V}/\mu\text{s}}{2\pi(10 \text{ V})} = 239 \text{ kHz}$$

PRACTICE PROBLEM 18-5 Repeat Example 18-5 using a 741C and $V_p = 200$ mV.

Example 18-6

What is the power bandwidth for each of the following?

$$S_R = 0.5 \text{ V}/\mu\text{s} \text{ and } V_p = 8 \text{ V}$$

$$S_R = 5 \text{ V}/\mu\text{s} \text{ and } V_p = 8 \text{ V}$$

$$S_R = 50 \text{ V}/\mu\text{s} \text{ and } V_p = 8 \text{ V}$$

SOLUTION With Fig. 18-10, read each power bandwidth to get these approximate answers: 10 kHz, 100 kHz, and 1 MHz.

PRACTICE PROBLEM 18-6 Repeat Example 18-6 with $V_p = 1$ V.

18-3 The Inverting Amplifier

The inverting amplifier is the most basic op-amp circuit. It uses negative feedback to stabilize the overall voltage gain. The reason we need to stabilize the overall voltage gain is because A_{VOL} is too high and unstable to be of any use without some form of feedback. For instance, the 741C has a minimum A_{VOL} of 20,000 and a maximum A_{VOL} of more than 200,000. An unpredictable voltage gain of this magnitude and variation is useless without feedback.

Inverting Negative Feedback

Figure 18-12 shows an inverting amplifier. To keep the drawing simple, the power-supply voltages are not shown. In other words, we are looking at the ac equivalent circuit. An input voltage v_{in} drives the inverting input through resistor R_1 . This results in an inverting input voltage of v_2 . The input voltage is amplified by the open-loop voltage gain to produce an inverted output voltage. The output voltage is fed back to the input through feedback resistor R_f . This results in negative feedback because the output is 180° out of phase with the input. In other words, any changes in v_2 produced by the input voltage are opposed by the output signal.

Here is how the negative feedback stabilizes the overall voltage gain: If the open-loop voltage gain A_{VOL} increases for any reason, the output voltage will increase and feed back more voltage to the inverting input. This opposing feedback voltage reduces v_2 . Therefore, even though A_{VOL} has increased, v_2 has decreased, and the final output increases much less than it would without the negative feedback. The overall result is a very slight increase in output voltage, so small that it is hardly noticeable. In Chap. 19, we will discuss the mathematical details of negative feedback and you will better understand how small the changes are.

Virtual Ground

When we connect a piece of wire between some point in a circuit and ground, the voltage of the point becomes zero. Furthermore, the wire provides a path for current to flow to ground. A *mechanical ground* (a wire between a point and ground) is ground to both voltage and current.

A **virtual ground** is different. This type of ground is a widely used shortcut for analyzing an inverting amplifier. With a virtual ground, the analysis of an inverting amplifier and related circuits becomes incredibly easy.

The concept of a virtual ground is based on an ideal op amp. When an op amp is ideal, it has infinite open-loop voltage gain and infinite input resistance. Because of this, we can deduce the following ideal properties for the inverting amplifier of Fig. 18-13:

1. Since R_{in} is infinite, i_2 is zero.
2. Since A_{VOL} is infinite, v_2 is zero.

Figure 18-12 The inverting amplifier.

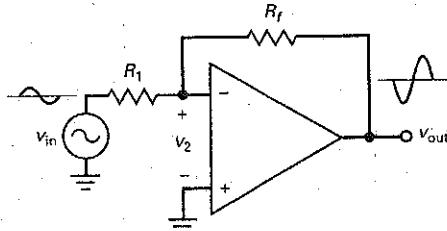
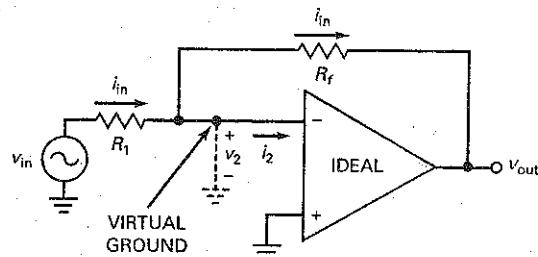


Figure 18-13 The concept of virtual ground: shorted to voltage and open to current.



Since i_2 is zero in Fig. 18-13, the current through R_f must equal the input current through R_1 , as shown. Furthermore, since v_2 is zero, the virtual ground shown in Fig. 18-13 means that the inverting input acts like a ground for voltage but an open for current!

Virtual ground is very unusual. It is like half of a ground because it is a short for voltage but an open for current. To remind us of this half-ground quality, Fig. 18-13 uses a dashed line between the inverting input and ground. The dashed line means that no current can flow to ground. Although virtual ground is an ideal approximation, it gives very accurate answers when used with heavy negative feedback.

Voltage Gain

In Fig. 18-14, visualize a virtual ground on the inverting input. Then, the right end of R_1 is a voltage ground, so we can write:

$$v_{in} = i_{in} R_1$$

Similarly, the left end of R_f is a voltage ground, so the magnitude of output voltage is:

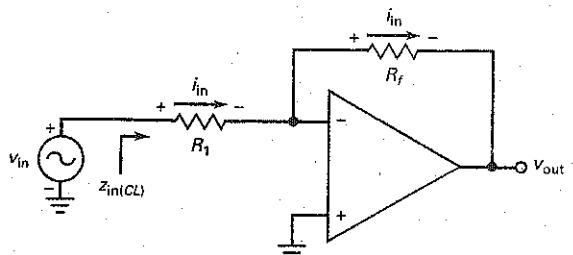
$$v_{out} = -i_{in} R_f$$

Divide v_{out} by v_{in} to get the voltage gain:

$$A_{v(CL)} = \frac{-R_f}{R_1} \quad (18-3)$$

where $A_{v(CL)}$ is the closed-loop voltage gain. This is called the **closed-loop voltage gain** because it is the voltage when there is a feedback path between the output and the input. Because of the negative feedback, the closed-loop voltage gain $A_{v(CL)}$ is always smaller than the open-loop voltage gain A_{VOL} .

Figure 18-14 Inverting amplifier has same current through both resistors.



Look at how simple and elegant Eq. (18-3) is. The closed-loop voltage gain equals the ratio of the feedback resistance to the input resistance. For instance, if $R_1 = 1 \text{ k}\Omega$ and $R_f = 50 \text{ k}\Omega$, the closed-loop voltage gain is 50. Because of the heavy negative feedback, this closed-loop voltage gain is very stable. If A_{VOL} varies because of temperature change, supply voltage variations, or op-amp replacement, $A_{V(CL)}$ will still be very close to 50. Chapter 19 will discuss gain stability in more detail. The negative sign in the voltage gain equation indicates a 180° phase shift.

Input Impedance

GOOD TO KNOW

An inverting amplifier can have more than one input because, with the virtual ground point, each input is effectively isolated from the other. Each input sees its own input resistance and nothing else.

In some applications, a designer may want a specific input impedance. This is one of the advantages of an inverting amplifier; it is easy to set up a desired input impedance. Here is why: Since the right end of R_1 is virtually grounded, the closed-loop input impedance is:

$$z_{in(CL)} = R_1 \quad (18-4)$$

This is the impedance looking into the left end of R_1 , as shown in Fig. 18-14. For instance, if an input impedance of $2 \text{ k}\Omega$ and a closed-loop voltage gain of 50 is needed, a designer can use $R_1 = 2 \text{ k}\Omega$ and $R_f = 100 \text{ k}\Omega$.

Bandwidth

The **open-loop bandwidth** or cutoff frequency of an op amp is very low because of the internal compensating capacitor. For a 741C:

$$f_{2(OL)} = 10 \text{ Hz}$$

At this frequency, the open-loop voltage gain breaks and rolls off in a first-order response.

When negative feedback is used, the overall bandwidth increases. Here is the reason: When the input frequency is greater than $f_{2(OL)}$, A_{VOL} decreases 20 dB per decade. When v_{out} tries to decrease, less opposing voltage is fed back to the inverting input. Therefore, v_2 increases and compensates for the decrease in A_{VOL} . Because of this, $A_{V(CL)}$ breaks at a higher frequency than $f_{2(OL)}$. The greater the negative feedback, the higher the closed-loop cutoff frequency. Stated another way: The smaller $A_{V(CL)}$ is, the higher $f_{2(CL)}$ is.

Figure 18-15 illustrates how the closed-loop bandwidth increases with negative feedback. As you can see, the heavier the negative feedback (smaller $A_{V(CL)}$), the greater the closed-loop bandwidth. Here is the equation for closed-loop bandwidth:

$$f_{2(CL)} = \frac{f_{unity}}{A_{V(CL)} + 1} \quad (\text{inverting amplifier only})$$

In most applications, $A_{V(CL)}$ is greater than 10 and the equation simplifies to:

$$f_{2(CL)} = \frac{f_{unity}}{A_{V(CL)}} \quad (\text{noninverting}) \quad (18-5)$$

For instance, when $A_{V(CL)}$ is 10:

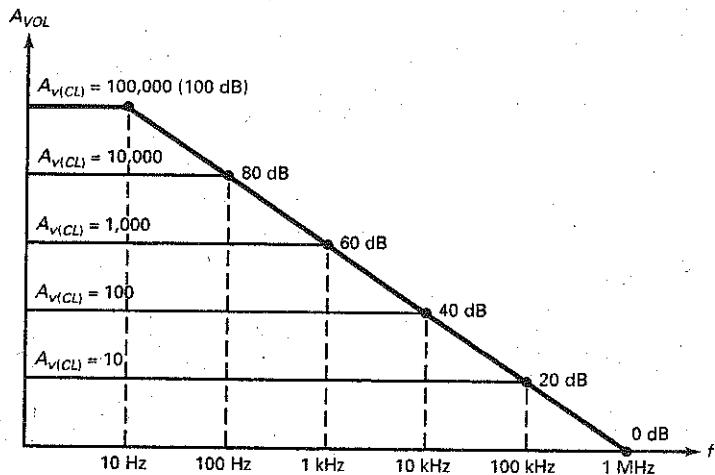
$$f_{2(CL)} = \frac{1 \text{ MHz}}{10} = 100 \text{ kHz}$$

which agrees with Fig. 18-14. If $A_{V(CL)}$ is 100:

$$f_{2(CL)} = \frac{1 \text{ MHz}}{100} = 10 \text{ kHz}$$

which also agrees.

Figure 18-15 Lower voltage gain produces more bandwidth.



Equation (18-5) can be rearranged into:

$$f_{\text{unity}} = A_{V(CL)} f_{2(CL)} \quad (18-6)$$

Notice that the unity-gain frequency equals the product of gain and bandwidth. For this reason, many data sheets refer to the unity-gain frequency as the **gain-bandwidth product (GBW)**.

(Note: No consistent symbol is used on data sheets for the open-loop voltage gain. You may see any of the following: A_{OL} , A_v , A_{vo} , and A_{vol} . It is usually clear from the data sheet that all these symbols represent the open-loop voltage gain of the op amp. We will use A_{VOL} in this book.)

Bias and Offsets

Negative feedback reduces the output error caused by input bias current, input offset current, and input offset voltage. Chapter 17 discussed the three input error voltages and the equation for total output error voltage:

$$V_{\text{error}} = A_{VOL}(V_{1\text{err}} + V_{2\text{err}} + V_{3\text{err}})$$

When negative feedback is used, this equation may be written as:

$$V_{\text{error}} \cong \pm A_{V(CL)}(\pm V_{1\text{err}} \pm V_{2\text{err}} \pm V_{3\text{err}}) \quad (18-7)$$

where V_{error} is the total output error voltage. Notice that the Eq. (18-7) includes \pm signs. Data sheets do not include \pm signs because it is implied that errors can be in either direction. For instance, either base current can be larger than the other, and the input offset voltage can be plus or minus.

In mass production, the input errors may add up in the worst possible way. The input errors were discussed in Chap. 17 and are repeated here:

$$V_{1\text{err}} = (R_{B1} - R_{B2})I_{\text{in(bias)}} \quad (18-8)$$

$$V_{2\text{err}} = (R_{B1} + R_{B2}) \frac{I_{\text{in(off)}}}{2} \quad (18-9)$$

$$V_{3\text{err}} = V_{\text{in(off)}} \quad (18-10)$$

When $A_{v(CL)}$ is small, the total output error given by Eq. (18-7) may be small enough to ignore. If not, resistor compensation and offset nulling will be necessary.

In an inverting amplifier, R_{B2} is the Thevenin resistance seen when looking back from the inverting input toward the source. This resistance is given by:

$$R_{B2} = R_1 \parallel R_f \quad (18-11)$$

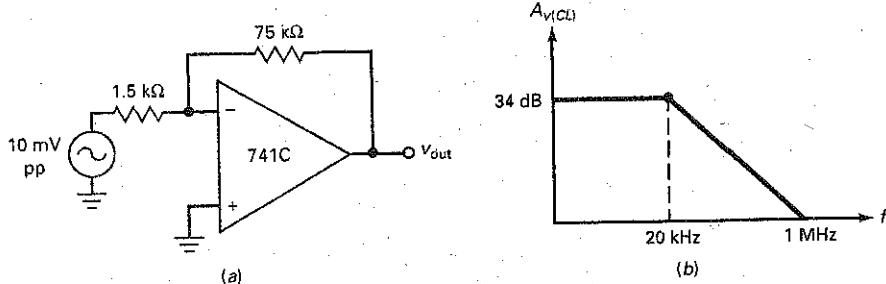
If it is necessary to compensate for input bias current, an equal resistance R_{B1} should be connected to the noninverting input. This resistance has no effect on the virtual-ground approximation because no ac signal current flows through it.

Example 18-7

 Multisim

Figure 18-16a is an ac equivalent circuit, so we can ignore the output error caused by input bias and offsets. What are closed-loop voltage gain and bandwidth? What is the output voltage at 1 kHz? At 1 MHz?

Figure 18-16 Example.



SOLUTION With Eq. (18-3), the closed-loop voltage gain is:

$$A_{v(CL)} = \frac{-75 \text{ k}\Omega}{1.5 \text{ k}\Omega} = -50$$

With Eq. (18-5), the closed-loop bandwidth is:

$$f_{2(CL)} = \frac{1 \text{ MHz}}{50} = 20 \text{ kHz}$$

Figure 18-16b shows the ideal Bode plot of the closed-loop voltage gain. The decibel equivalent of 50 is 34 dB. (Shortcut: 50 is half of 100, or down 6 dB from 40 dB.)

The output voltage at 1 kHz is:

$$v_{\text{out}} = (-50)(10 \text{ mV pp}) = -500 \text{ mV pp}$$

Since 1 MHz is the unity-gain frequency, the output voltage at 1 MHz is:

$$v_{\text{out}} = -10 \text{ mV pp}$$

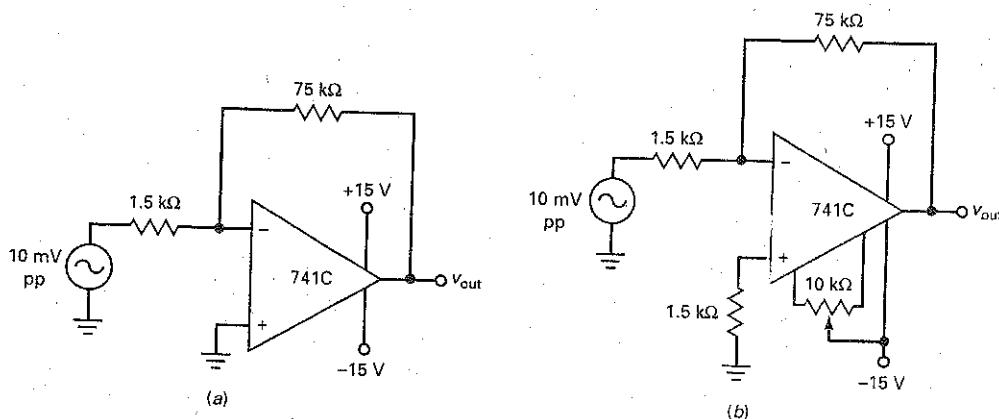
Again, the minus (-) output value indicates a 180° phase shift between the input and output.

PRACTICE PROBLEM 18-7 In Fig. 18-16a, what is the output voltage at 100 kHz? [Hint: Use Eq. (16-20).]

Example 18-8

What is the output voltage in Fig. 18-17 when v_{in} is zero? Use the typical values given in Table 18-1.

Figure 18-17 Example.



SOLUTION Table 18-1 shows these values for a 741C: $I_{in(bias)} = 80 \text{ nA}$, $I_{in(off)} = 20 \text{ nA}$, and $V_{in(off)} = 2 \text{ mV}$. With Eq. (18-11):

$$R_{B2} = R_1 \parallel R_f = 1.5 \text{ k}\Omega \parallel 75 \text{ k}\Omega = 1.47 \text{ k}\Omega$$

With Eqs. (18-8) to (18-10), the three input error voltages are:

$$V_{1err} = (R_{B1} - R_{B2})I_{in(bias)} = (-1.47 \text{ k}\Omega)(80 \text{ nA}) = -0.118 \text{ mV}$$

$$V_{2err} = (R_{B1} + R_{B2}) \frac{I_{in(off)}}{2} = (1.47 \text{ k}\Omega)(10 \text{ nA}) = 0.0147 \text{ mV}$$

$$V_{3err} = V_{in(off)} = 2 \text{ mV}$$

The closed-loop voltage gain is 50, calculated in the previous example. With Eq. (18-7), adding the errors in the worst possible way gives an output error voltage of:

$$V_{error} = \pm 50(0.118 \text{ mV} + 0.0147 \text{ mV} + 2 \text{ mV}) = \pm 107 \text{ mV}$$

PRACTICE PROBLEM 18-8 Repeat Example 18-8 using an LF157A op amp.

Example 18-9

In the foregoing example, we used typical parameters. The data sheet of a 741C lists the following worst-case parameters: $I_{in(bias)} = 500 \text{ nA}$, $I_{in(off)} = 200 \text{ nA}$, and $V_{in(off)} = 6 \text{ mV}$. Recalculate the output voltage when v_{in} is zero in Fig. 18-17a.

SOLUTION With Eqs. (18-8) to (18-10), the three input error voltages are:

$$V_{1err} = (R_{B1} - R_{B2})I_{in(bias)} = (-1.47 \text{ k}\Omega)(500 \text{ nA}) = -0.735 \text{ mV}$$

$$V_{2err} = (R_{B1} + R_{B2}) \frac{I_{in(off)}}{2} = (1.47 \text{ k}\Omega)(100 \text{ nA}) = 0.147 \text{ mV}$$

$$V_{3err} = V_{in(off)} = 6 \text{ mV}$$

Adding the errors in the worst possible way gives an output error voltage of:

$$V_{\text{error}} = \pm 50(0.735 \text{ mV} + 0.147 \text{ mV} + 6 \text{ mV}) = \pm 344 \text{ mV}$$

In Example 18-7, the desired output voltage was 500 mV pp. Can we ignore the large output error voltage? It depends on the application. For instance, suppose we only need to amplify audio signals with frequencies between 20 Hz and 20 kHz. Then, we can capacitively couple the output into the load resistor or next stage. This will block the dc output error voltage but transmit the ac signal. In this case, the output error is irrelevant.

On the other hand, if we want to amplify signals with frequencies from 0 to 20 kHz, then we need to use a better op amp (lower bias and offsets), or modify the circuit as shown in Fig. 18-17b. Here, we have added a compensating resistor to the noninverting input to eliminate the effect of input bias current. Also, we are using a 10-kΩ potentiometer to null the effects of input offset current and input offset voltage.

18-4 The Noninverting Amplifier

The **noninverting amplifier** is another basic op-amp circuit. It uses negative feedback to stabilize the overall voltage gain. With this type of amplifier, the negative feedback also increases the input impedance and decreases the output impedance.

Basic Circuit

Figure 18-18 shows the ac equivalent circuit of a noninverting amplifier. An input voltage v_{in} drives the noninverting input. This input voltage is amplified to produce the in-phase output voltage shown. Part of output voltage is fed back to the input through a voltage divider. The voltage across R_1 is the feedback voltage applied to the inverting input. This feedback voltage is almost equal to the input voltage. Because of the high open-loop voltage gain, the difference between v_1 and v_2 is very small. Since the feedback voltage opposes the input voltage, we have negative feedback.

Here is how the negative feedback stabilizes the overall voltage gain: If the open-loop voltage gain A_{VOL} increases for any reason, the output voltage will increase and feed back more voltage to the inverting input. This opposing feedback voltage reduces the net input voltage $v_1 - v_2$. Therefore, even though A_{VOL} increases, $v_1 - v_2$ decreases, and the final output increases much less than it

Figure 18-18 The noninverting amplifier.

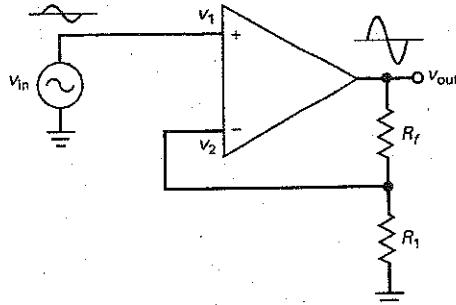
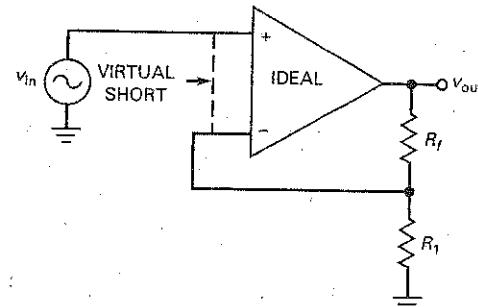


Figure 18-19 A virtual short exists between the two op-amp inputs.



would without the negative feedback. The overall result is only a very slight increase in output voltage.

Virtual Short

When we connect a piece of wire between two points in a circuit, the voltage of both points with respect to ground is equal. Furthermore, the wire provides a path for current to flow between the two points. A *mechanical short* (a wire between two points) is a short for both voltage and current.

A **virtual short** is different. This type of short can be used for analyzing noninverting amplifiers. With a virtual short, we can quickly and easily analyze noninverting amplifiers and related circuits.

The virtual short uses these two properties of an ideal op amp:

1. Since R_{in} is infinite, both input currents are zero.
2. Since A_{VOL} is infinite, $v_1 - v_2$ is zero.

Figure 18-19 shows a virtual short between the input terminals of the op amp. The virtual short is a short for voltage but an open for current. As a reminder, the dashed line means that no current can flow through it. Although the virtual short is an ideal approximation, it gives very accurate answers when used with heavy negative feedback.

Here is how we will use the virtual short: Whenever we analyze a noninverting amplifier or a similar circuit, we can visualize a virtual short between the input terminals of the op amp. As long as the op amp is operating in the linear region (not positively or negatively saturated), the open-loop voltage gain approaches infinity and a virtual short exists between the two input terminals.

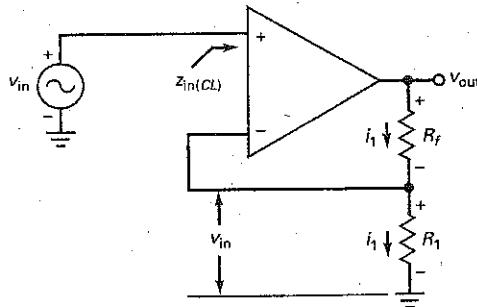
One more point: Because of the virtual short, the inverting input voltage follows the noninverting input voltage. If the noninverting input voltage increases or decreases, the inverting input voltage immediately increases or decreases to the same value. This follow-the-leader action is called **bootstrapping** (as in "pulling yourself up by your bootstraps"). The noninverting input pulls the inverting input up or down to an equal value. Described another way, the inverting input is bootstrapped to the noninverting input.

Voltage Gain

In Fig. 18-20, visualize a virtual short between the input terminals of the op amp. Then, the virtual short means that the input voltage appears across R_1 , as shown. So, we can write:

$$v_{in} = i_1 R_1$$

Figure 18-20 Input voltage appears across R_1 and same current flows through resistors.



Since no current can flow through a virtual short, the same i_1 current must flow through R_f , which means that the output voltage is given by:

$$v_{\text{out}} = i_1(R_f + R_1)$$

Divide v_{out} by v_{in} to get the voltage gain:

$$A_{v(CL)} = \frac{R_f + R_1}{R_1}$$

or

$$A_{v(CL)} = \frac{R_f}{R_1} + 1 \quad (18-12)$$

This is easy to remember because it is the same as the equation for an inverting amplifier, except that we add 1 to the ratio of resistances. Also note that the output is in phase with the input. Therefore, no $(-)$ sign is used in the voltage gain equation.

Other Quantities

The closed-loop input impedance approaches infinity. In the next chapter, we will mathematically analyze the effect of negative feedback and will show that negative feedback increases the input impedance. Since the open-loop input impedance is already very high ($2 \text{ M}\Omega$ for a 741C), the closed-loop input impedance will be even higher.

The effect of negative feedback on bandwidth is the same as with an inverting amplifier:

$$f_{2(CL)} = \frac{f_{\text{unity}}}{A_{v(CL)}}$$

Again, we can trade off voltage gain for bandwidth. The smaller the closed-loop voltage gain, the greater the bandwidth.

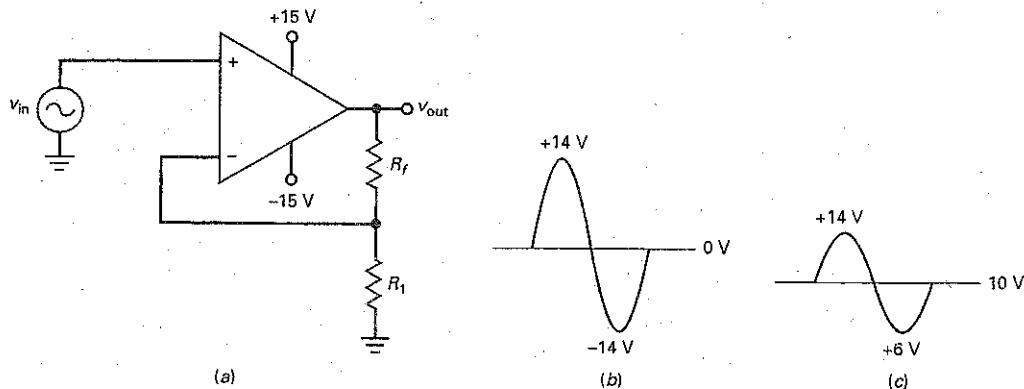
The input error voltages caused by input bias current, input offset current, and input offset voltage are analyzed the same way as with an inverting amplifier. After calculating each input error, we can multiply by the closed-loop voltage gain to get the total output error.

R_{B2} is the Thevenin resistance seen when looking from the inverting input toward the voltage divider. This resistance is the same as for an inverting amplifier:

$$R_{B2} = R_1 \parallel R_f$$

If it is necessary to compensate for input bias current, an equal resistance R_{B1} should be connected to the noninverting input. This resistance has no effect on the virtual-short approximation because no ac signal current flows through it.

Figure 18-21 Output error voltage reduces MPP.



Output Error Voltage Reduces MPP

As previously discussed, if we are amplifying ac signals, we can capacitively couple the output signal to the load. In this case, we can ignore the output error voltage unless it is excessively large. If the output error voltage is large, it will significantly reduce the MPP, the maximum unclipped peak-to-peak output.

For instance, if there is no output error voltage, the noninverting amplifier of Fig. 18-21a can swing to within approximately a volt or two of either supply voltage. For simplicity, assume that the output signal can swing from +14 to -14 V, giving an MPP of 28 V, as shown in Fig. 18-21b. Now, suppose the output error voltage is +10 V, as shown in Fig. 18-21c. With this large output error voltage, the maximum unclipped peak-to-peak swing is from +14 to +6 V, an MPP of only 8 V. This may still be all right if the application does not require a large output signal. Here is the point to remember: The greater the output error voltage, the smaller the MPP value.

Example 18-10

In Fig. 18-22a, what is closed-loop voltage gain and bandwidth? What is the output voltage at 250 kHz?

SOLUTION With Eq. (18-12):

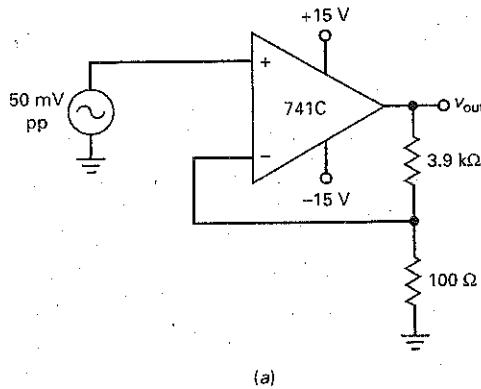
$$A_{v(CL)} = \frac{3.9 \text{ k}\Omega}{100 \Omega} + 1 = 40$$

Dividing the unity-gain frequency by the closed-loop voltage gain gives:

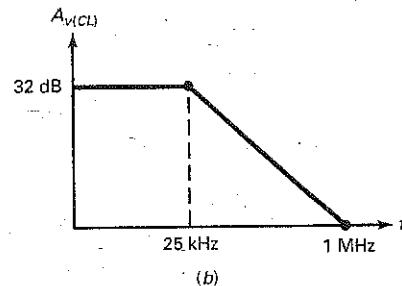
$$f_2(CL) = \frac{1 \text{ MHz}}{40} = 25 \text{ kHz}$$

Figure 18-22b shows the ideal Bode plot of closed-loop voltage gain. The decibel equivalent of 40 is 32 dB. (Shortcut: $40 = 10 \times 2 \times 2$ or $20 \text{ dB} + 6 \text{ dB} + 6 \text{ dB} = 32 \text{ dB}$.) Since the $A_{v(CL)}$ breaks at 25 kHz, it is down 20 dB at 250 kHz. This means that $A_{v(CL)} = 12 \text{ dB}$ at 250 kHz, which is equivalent to an

Figure 18-22 Example.



(a)



(b)

ordinary voltage gain of 4. Therefore, the output voltage at 250 kHz is:

$$v_{\text{out}} = 4(50 \text{ mV pp}) = 200 \text{ mV pp}$$

PRACTICE PROBLEM 18-10 In Fig. 18-22, change the $3.9 \text{ k}\Omega$ resistor to $4.9 \text{ k}\Omega$. Solve for $A_{V(CL)}$ and v_{out} at 200 kHz.

Example 18-11

For convenience, we repeat the worst-case parameters of a 741C: $I_{\text{in(bias)}} = 500 \text{ nA}$, $I_{\text{in(off)}} = 200 \text{ nA}$, and $V_{\text{in(off)}} = 6 \text{ mV}$. What is the output error voltage in Fig. 18-22a?

SOLUTION R_{B2} is the parallel equivalent of $3.9 \text{ k}\Omega$ and 100Ω , which is approximately 100Ω . With Eqs. (18-8) to (18-10), the three input error voltages are:

$$V_{1\text{err}} = (R_{B1} - R_{B2})I_{\text{in(bias)}} = (-100 \Omega)(500 \text{ nA}) = -0.05 \text{ mV}$$

$$V_{2\text{err}} = (R_{B1} + R_{B2}) \frac{I_{\text{in(off)}}}{2} = (100 \Omega)(100 \text{ nA}) = 0.01 \text{ mV}$$

$$V_{3\text{err}} = V_{\text{in(off)}} = 6 \text{ mV}$$

Adding the errors in the worst possible way gives an output error voltage of:

$$V_{\text{error}} = \pm 40(0.05 \text{ mV} + 0.01 \text{ mV} + 6 \text{ mV}) = \pm 242 \text{ mV}$$

If this output error voltage is a problem, we can use a $10-\text{k}\Omega$ potentiometer, as previously described, to null the output.

18-5 Two Op-Amp Applications

Op-amp applications are so broad and varied that it is impossible to discuss them comprehensively in this chapter. Besides, we need to understand negative feedback better before looking at some of the more advanced applications. For now, let us take a look at two practical circuits.

The Summing Amplifier

Whenever we need to combine two or more analog signals into a single output, the **summing amplifier** of Fig. 18-23a is a natural choice. For simplicity, the circuit shows only two inputs, but we can have as many inputs as needed for the application. A circuit like this amplifies each input signal. The gain for each *channel* or input is given by the ratio of the feedback resistance to the appropriate input resistance. For instance, the closed-loop voltage gains of Fig. 18-23a are:

$$A_{v1(CL)} = \frac{-R_f}{R_1} \quad \text{and} \quad A_{v2(CL)} = \frac{-R_f}{R_2}$$

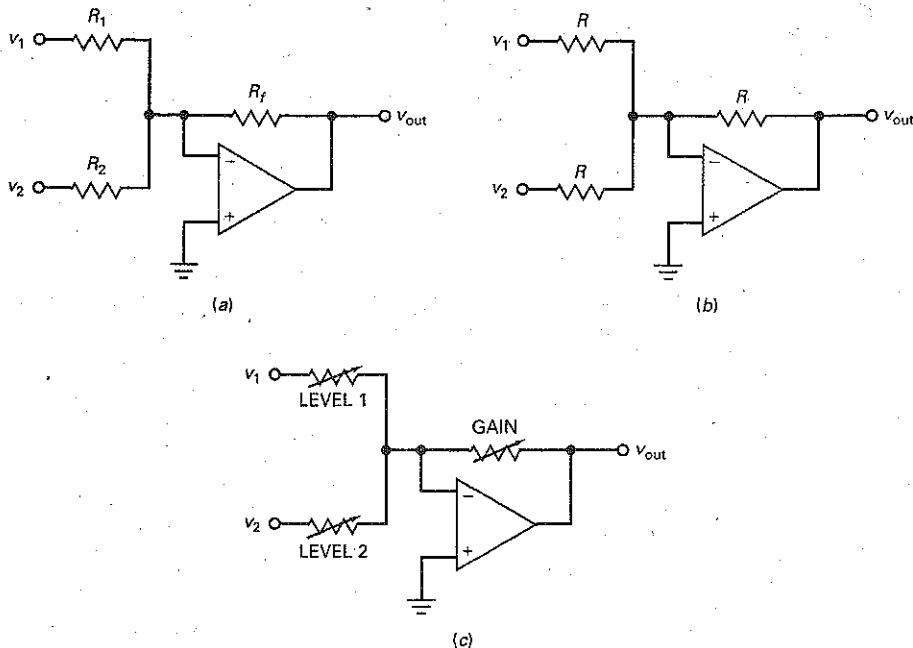
The summing circuit combines all the amplified input signals into a single output, given by:

$$v_{out} = A_{v1(CL)}v_1 + A_{v2(CL)}v_2 \quad (18-13)$$

It is easy to prove Eq. (18-13). Since the inverting input is a virtual ground, the total input current is:

$$i_{in} = i_1 + i_2 = \frac{v_1}{R_1} + \frac{v_2}{R_2}$$

Figure 18-23 Summing amplifier.



Because of the virtual ground, all this current flows through the feedback resistor, producing an output voltage with a magnitude of:

$$v_{\text{out}} = (i_1 + i_2)R_f = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2\right)$$

Here you see that each input voltage is multiplied by its channel gain and added to produce the total output. The same result applies to any number of inputs.

In some applications, all resistances are equal, as shown in Fig. 18-23b. In this case, each channel has a closed-loop voltage gain of unity (1) and the output is given by:

$$v_{\text{out}} = -(v_1 + v_2 + \dots + v_n)$$

This is a convenient way of combining input signals and maintaining their relative sizes. The combined output signal can then be processed by more circuits.

Figure 18-23c is a **mixer**, a convenient way to combine audio signals in a high-fidelity audio system. The adjustable resistors allow us to set the level of each input, and the gain control allows us to adjust the combined output volume. By decreasing LEVEL 1, we can make the v_1 signal louder at the output. By decreasing LEVEL 2, we can make the v_2 signal louder. By increasing GAIN, we can make both signals louder.

A final point: If a summing circuit needs to be compensated by adding an equal resistance to the noninverting input, the resistance to use is the Thevenin resistance looking from the inverting input back to the sources. This resistance is given by the parallel equivalent of all resistances connected to the virtual ground:

$$R_{B2} = R_1 \parallel R_2 \parallel R_f \parallel \dots \parallel R_n \quad (18-14)$$

Voltage Follower

In Chap. 11, we discussed the emitter follower and saw how useful it was for increasing the input impedance while producing an output signal that was almost equal to the input. The **voltage follower** is the equivalent of an emitter follower, except that it works much better.

Figure 18-24a shows the ac equivalent circuit for a voltage follower. Although it appears deceptively simple, the circuit is very close to ideal because the negative feedback is maximum. As you can see, the feedback resistance is zero. Therefore, all the output voltage is fed back to the inverting input. Because of the virtual short between the op-amp inputs, the output voltage equals the input voltage:

$$v_{\text{out}} = v_{\text{in}}$$

which means that the closed-loop voltage gain is:

$$A_{v(CL)} = 1 \quad (18-15)$$

We can get the same result by calculating the closed-loop voltage gain with Eq. (18-12). Since $R_f = 0$ and $R_1 = \infty$:

$$A_{v(CL)} = \frac{R_f}{R_1} + 1 = 1$$

Therefore, the voltage follower is a perfect follower circuit because it produces an output voltage that is exactly equal to the input voltage (or close enough to satisfy almost any application).

Furthermore, the maximum negative feedback produces a closed-loop input impedance that is much higher than the open-loop input impedance ($2 \text{ M}\Omega$ for a 741C). Also, a maximum negative feedback produces a closed-loop output impedance that is much lower than the open-loop output impedance (75Ω for a 741C). Therefore, we have an almost perfect method for converting a high-impedance source to a low-impedance source.

Figure 18-24 (a) Voltage follower has unity gain and maximum bandwidth; (b) voltage follower allows high-impedance source to drive low-impedance load with no loss of voltage.

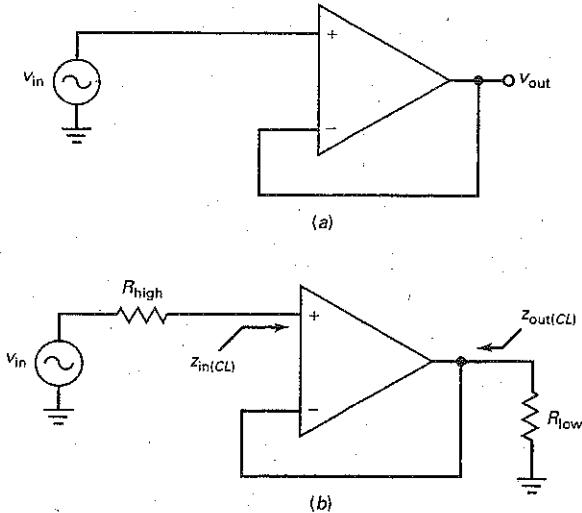


Figure 18-24b illustrates the idea. The input ac source has a high output impedance R_{high} . The load has a low impedance R_{low} . Because of the maximum negative feedback in a voltage follower, the closed-loop input impedance $Z_{\text{in(CL)}}$ is incredibly high and the closed-loop output impedance $Z_{\text{out(CL)}}$ is incredibly low. As a result, all the input source voltage appears across the load resistor.

The crucial point to understand is this: The voltage follower is the ideal interface to use between a high-impedance source and a low-impedance load. Basically, it transforms the high-impedance voltage source into a low-impedance voltage source. You will see the voltage follower used a great deal in practice.

Since $A_{v(CL)} = 1$ in a voltage follower, the closed-loop bandwidth is maximum and equal to:

$$f_{2(CL)} = f_{\text{unity}} \quad (18-16)$$

Another advantage is the low output offset error because the input errors are not amplified. Since $A_{v(CL)} = 1$, the total output error voltage equals the worst-case sum of the input errors.

Example 18-12

Multisim

Three audio signals drive the summing amplifier of Fig. 18-25. What is the ac output voltage?

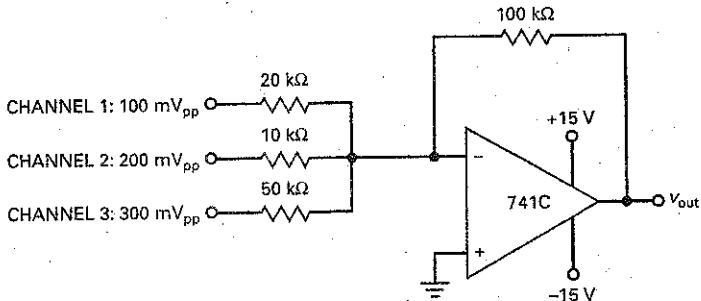
SOLUTION The channels have closed-loop voltage gains of:

$$A_{v1(CL)} = \frac{-100 \text{ k}\Omega}{20 \text{ k}\Omega} = -5$$

$$A_{v2(CL)} = \frac{-100 \text{ k}\Omega}{10 \text{ k}\Omega} = -10$$

$$A_{v3(CL)} = \frac{-100 \text{ k}\Omega}{50 \text{ k}\Omega} = -2$$

Figure 18-25 Example.



The output voltage is:

$$v_{\text{out}} = (-5)(100 \text{ mV}_{\text{pp}}) + (-10)(200 \text{ mV}_{\text{pp}}) + (-2)(300 \text{ mV}_{\text{pp}}) = -3.1 \text{ V}_{\text{pp}}$$

Again, the negative sign indicates a 180° phase shift.

If it is necessary to compensate for input bias by adding an equal R_B to the noninverting input, the resistance to use is:

$$R_{B2} = 20 \text{ k}\Omega \parallel 10 \text{ k}\Omega \parallel 50 \text{ k}\Omega \parallel 100 \text{ k}\Omega = 5.56 \text{ k}\Omega$$

The nearest standard value of 5.6 kΩ would be fine. A nulling circuit would take care of the remaining input errors.

PRACTICE PROBLEM 18-12 Using Fig. 18-25, the input channel voltages are changed from peak-to-peak values to positive dc values. What is the output dc voltage?

Example 18-13

III Multisim

An ac voltage source of 10 mV_{pp} with an internal resistance of 100 kΩ drives the voltage follower of Fig. 18-26a. The load resistance is 1 Ω. What is the output voltage? The bandwidth?

SOLUTION The closed-loop voltage gain is unity. Therefore:

$$v_{\text{out}} = 10 \text{ mV}_{\text{pp}}$$

and the bandwidth is:

$$f_{2(\text{CL})} = 1 \text{ MHz}$$

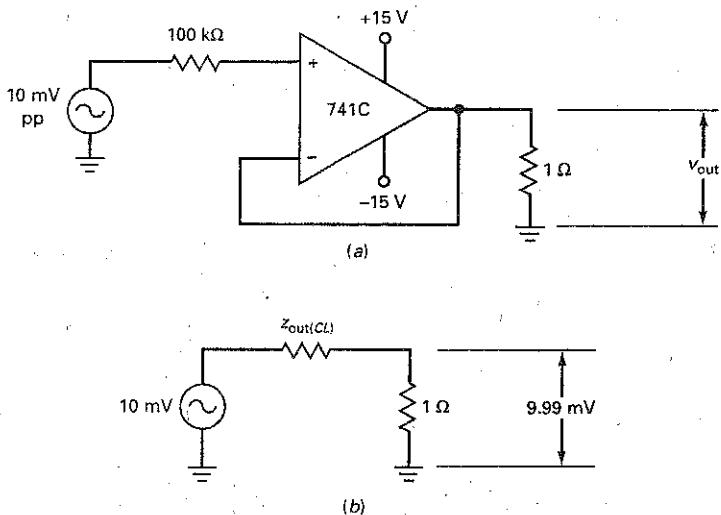
This example echoes the idea discussed earlier. The voltage follower is an easy way to transform a high-impedance source into a low-impedance source. It does what the emitter follower does, only far better.

PRACTICE PROBLEM 18-13 Repeat Example 18-13 using an LF157A op amp.

Example 18-14

When the voltage follower of Fig. 18-26a is built with MultiSim, the output voltage across the 1-Ω load is 9.99 mV. Show how to calculate the closed-loop output impedance.

Figure 18-26 Example.



SOLUTION

$$v_{out} = 9.99 \text{ mV}$$

The closed-loop output impedance is the same as the Thevenin resistance facing the load resistor. In Fig. 18-26b, the load current is:

$$i_{out} = \frac{9.99 \text{ mV}}{1 \Omega} = 9.99 \text{ mA}$$

This load current flows through $z_{out(CL)}$. Since the voltage across $z_{out(CL)}$ is 0.01 mV:

$$z_{out(CL)} = \frac{0.01 \text{ mV}}{9.99 \text{ mA}} = 0.001 \Omega$$

Let the significance of this sink in. In Fig. 18-26a, the voltage source with an internal impedance of 100 kΩ has been converted to a voltage source with an internal impedance of only 0.001 Ω. Small output impedances like this mean that we are approaching the ideal voltage source first discussed in Chap. 1.

PRACTICE PROBLEM 18-14 In Fig. 18-26a, if the loaded output voltage is 9.95 mV, calculate the closed-loop output impedance.

GOOD TO KNOW

Integrated circuits, like op amps, are replacing transistors in electronic circuits, just as transistors once replaced vacuum tubes. Op amps and linear ICs, however, are actually microelectronic circuits.

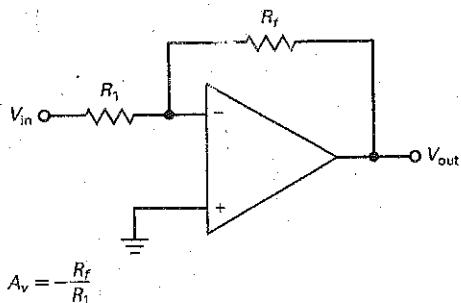
Summary Table 18-1 shows the basic op-amp circuits we have discussed to this point.

18-6 Linear ICs

Op amps represent about a third of all linear ICs. With op amps we can build a wide variety of useful circuits. Although the op amp is the most important linear IC, other linear ICs such as audio amplifiers, video amplifiers, and voltage regulators are also widely used.

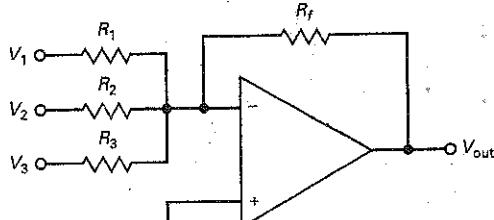
Summary Table 18-1 Basic Op-Amp Configurations

Inverting amp



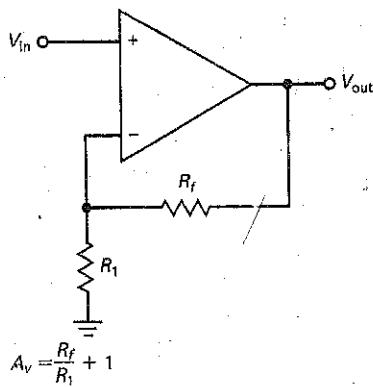
$$A_v = -\frac{R_f}{R_1}$$

Summing amp



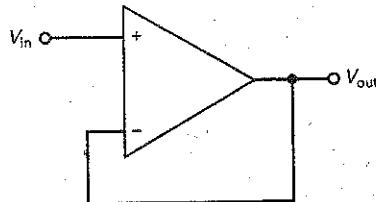
$$V_{out} = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

Noninverting amp



$$A_v = \frac{R_f}{R_1} + 1$$

Voltage follower



$$A_v = 1$$

Table of Op Amps

In Table 18-2, the prefix *LF* indicates a BIFET op amp. For instance, LF351 is the first entry in the table. This BIFET op amp has a maximum input offset voltage of 10 mV, a maximum input bias current of 0.2 nA, and a maximum input offset current of 0.1 nA. It can deliver a short-circuit current of 10 mA. It has a unity-gain frequency of 4 MHz, a slew rate of 13 V/ μ s, an open-loop voltage gain of 88 dB, and a common-mode rejection ratio of 70 dB.

The table contains two more quantities not previously discussed. First, there is the power supply rejection ratio (PSRR). This quantity is defined as:

$$\text{PSRR} = \frac{\Delta V_{in(off)}}{\Delta V_S} \quad (18-17)$$

In words, the equation says that the power-supply rejection ratio equals the change in the input offset voltage divided by the change in the supply voltages. In making this measurement, the manufacturer varies both supplies simultaneously and symmetrically. If $V_{CC} = +15$ V, $V_{EE} = -15$ V, and $\Delta V_S = +1$ V, then V_{CC} becomes +16 V and V_{EE} becomes -16 V.

Here is what Eq. (18-17) means: Because of the imbalance in the input diff amp plus other internal effects, a change in the supply voltage will produce an output error voltage. Dividing this output error voltage by the closed-loop voltage gain gives the change in the input offset voltage. For instance, the LF351 of

Table 18-2 | Typical Parameters of Selected Op Amps at 25°C

Number	$V_{in(off)}$ max, mV	$I_{in(max)}$ max, nA	$I_{in(off)}$ max, nA	I_{out} max, mA	f_{unity} typ, MHz	S_R typ, $\text{V}/\mu\text{s}$	A_{VOZ} typ, dB	CMRR min., dB	PSRR min., dB	Drift, typ, $\mu\text{V}/^\circ\text{C}$	Description of Op Amps
LF351	10	0.2	0.1	10	4	13	88	70	-76	10	BIFET
LF353	10	0.2	0.1	10	4	13	88	70	-76	10	Dual BIFET
LF356	5	0.2	0.05	20	5	12	94	85	-85	5	BIFET, wideband
LF411A	0.5	200	100	20	4	15	88	80	-80	10	Low offset BIFET
LM12	7	300	100	10 A†	0.7	9	94	75	-80	50	High-power, 80 W out
LM301A	7.5	250	50	10	1+	0.5+	108	70	-70	30	External compensation
LM307	7.5	250	50	10	1	0.5	108	70	-70	30	Improved 709, internal comp
LM308	7.5	7	1	5	0.3	0.15	108	80	-80	30	Precision
LM318	10	500	200	10	15	70	86	70	-65	—	High speed, high slew rate
LM324	4	10	2	5	0.1	0.05	94	80	-90	10	Low-power quad
LM348	6	500	200	25	1	0.5	100	70	-70	—	Quad 741
LM675	10	2 μA^*	500	3 A†	5.5	8	90	70	-70	25	High-power, 25 W out
LM741C	6	500	200	25	1	0.5	100	70	-70	—	Original classic
LM747C	6	500	200	25	1	0.5	100	70	-70	—	Dual 741
LM833	5	1 μA^*	200	10	15	7	90	80	-80	2	Low noise
LM1458	6	500	200	20	1	0.5	104	70	-77	—	Dual
OP-07A	0.025	2	1	10	0.6	0.17	110	110	-100	0.6	Precisión
OP-21A	0.1	100	4	—	0.6	0.25	120	100	-104	1	Low-power precision
OP-42E	0.75	0.2	0.04	25	10	58	114	88	-86	10	High-speed BIFET
OP-64E	0.75	300	100	20	200	200	100	110	-105	—	Very high speed and bandwidth
TL072	10	0.2	0.05	10	3	13	88	70	-70	10	Low-noise BIFET dual
TL074	10	0.2	0.05	10	3	13	88	70	-70	10	Low-noise BIFET quad
TL082	3	0.2	0.01	10	3	13	94	80	-80	10	Low-noise BIFET dual
TL084	3	0.2	0.01	10	3	13	94	80	-80	10	Low-noise BIFET quad

*For the LM675 and LM833, this value is commonly expressed in microampères.
†For the LM12 and LM675, this value is commonly expressed in amperes.

Table 18-2 has a PSRR in decibels of -76 dB. When we convert this to an ordinary number we get:

$$\text{PSRR} = \text{antilog } \frac{-76 \text{ dB}}{20} = 0.000158$$

or, as it is sometimes written:

$$\text{PSRR} = 158 \mu\text{V/V}$$

This tells us that a change of 1 V in the supply voltage will produce a change in the input offset voltage of $158 \mu\text{V}$. Therefore, we have one more source of input error that joins the three input errors discussed earlier.

The last parameter shown for the LF351 is the *drift* of $10 \mu\text{V}/^\circ\text{C}$. This is defined as the temperature coefficient of the input offset voltage. It tells us how much the input offset voltage increases with temperature. A drift of $10 \mu\text{V}/^\circ\text{C}$ means that the input offset voltage increases $10 \mu\text{V}$ for each degree increase in degrees Celsius. If the internal temperature of the op amp increases by 50°C , the input offset voltage of an LF351 increases by $500 \mu\text{V}$.

The op amps in Table 18-2 were selected to show you the variety of commercially available devices. For example, the LF411A is a low-offset BIFET with an input offset voltage of only 0.5 mV . Most op amps are low-power devices, but not all. The LM675 is a high-power op amp. It has a short-circuit current of 3 A and can deliver 25 W to a load resistor. Even more powerful is the LM12. It has a short-circuit current of 10 A and can produce a load power of 80 W . Several LM12s can be operated in parallel for even greater power output. Applications include heavy-duty voltage regulators, high-quality audio amplifiers, and servo-control systems.

When you need a high slew rate, an LM318 can slew at a rate of $70 \text{ V}/\mu\text{s}$. And then there is the OP-64E, which has a slew rate of $200 \text{ V}/\mu\text{s}$. High slew rate and bandwidth usually go together. As you can see, LM318 has an f_{unity} of 15 MHz , and the OP-64E has an f_{unity} of 200 MHz .

Many of the op amps are available as dual and quad op amps. This means that there are either two or four op amps in the same package. For instance, the LM747C is a dual 741C. The LM348 is a quad 741. The single and dual op amps fit in a package with 8 pins, and the quad op amp comes in packages with 14 pins.

Not all op amps need two supply voltages. For the instance, the LM324 has four internally compensated op amps. Although it can operate with two supplies like most op amps, it was specifically designed for a single power supply, a definite advantage in many applications. Another convenience of the LM324 is that it can work with a single power supply as low as $+5 \text{ V}$, the standard voltage for many digital systems.

Internal compensation is convenient and safe because an internally compensated op amp will not break into oscillations under any condition. The price paid for this safety is a loss of design control. This is why some op amps offer external compensation. For instance, LM301A is compensated by connecting an external 30-pF capacitor. But the designer has the option of overcompensating with a larger capacitor or undercompensating with smaller capacitor. Overcompensation can improve low-frequency operation, whereas undercompensation can increase the bandwidth and slew rate. This is why a plus sign (+) has been added to the f_{unity} and S_R of the LM301A in Table 18-2.

All op amps have imperfections, as we have seen. Precision op amps try to minimize these imperfections. For instance, the OP-07A is a precision op amp with the following worst-case parameters: input offset voltage is only 0.025 mV , CMRR is at least 110 dB , PSRR is at least 100 dB , and drift is only $0.6 \mu\text{V}/^\circ\text{C}$. Precision op amps are necessary for stringent applications such as measurement and control.

In subsequent chapters, we will discuss more applications of op amps. At that time, you will see how op amps can be used in a wide variety of linear circuits, nonlinear circuits, oscillators, voltage regulators, and active filters.

Audio Amplifiers

Preamplifiers (preamps) are audio amplifiers with less than 50 mW of output power. Preamps are optimized for low noise because they are used at the front end of audio systems, where they amplify weak signals from optical sensors, magnetic tape heads, microphones, and so on.

An example of an IC preamp is the LM381, a low-noise dual preamp. Each amplifier is completely independent of the other. The LM381 has a voltage gain of 112 dB and a 10-V power bandwidth of 75 kHz. It operates from a positive supply of 9 to 40 V. Its input impedance is 100 k Ω , and its output impedance is 150 Ω . The LM381's input stage is a diff amp, which allows differential or single-ended input.

Medium-level audio amplifiers have output powers from 50 to 500 mW. These are useful near the output end of portable electronic devices such as cell phones and CD players. An example is the LM4818 audio power amplifier, which has an output power of 350 mW.

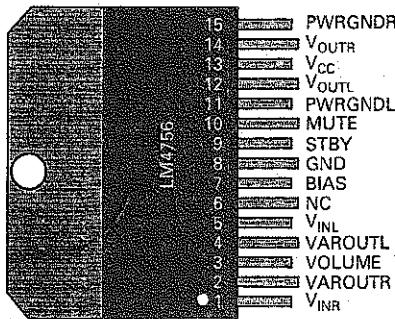
Audio power amplifiers deliver more than 500 mW of output power. They are used in high-fidelity amplifiers, intercoms, AM-FM radios, and other applications. The LM380 is an example. It has a voltage gain of 34 dB, a bandwidth of 100 kHz, and an output power of 2 W. As another example, the LM4756 power amp has an internally set voltage gain of 30 dB and can deliver 7 W/channel. Fig. 18-27 shows the package style and pin out for this IC. Notice the dual offset pin arrangement.

Figure 18-28 shows a simplified schematic diagram of the LM380. The input diff amp uses *pnp* inputs. The signal can be directly coupled, which is an advantage with transducers. The diff amp drives a current-mirror load (Q_5 and Q_6). The output of the current mirror goes to an emitter follower (Q_7) and CE driver (Q_8). The output stage is a class B push-pull emitter follower (Q_{13} and Q_{14}). There is an internal compensating capacitor of 10 pF that rolls off the decibel voltage gain at a rate of 20 dB per decade. This capacitor produces a slew rate of approximately 5 V/ μ s.

Figure 18-27 The LM4756 package style and pin out.

Connection diagrams

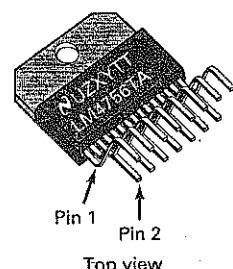
Plastic package



Top view

(a)

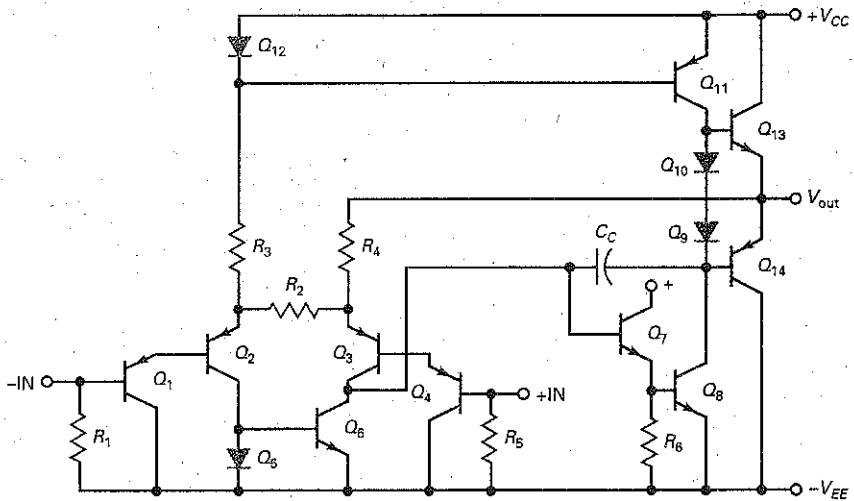
Plastic package



Top view

(b)

Figure 18-28 Simplified schematic diagram of LM380.



Video Amplifiers

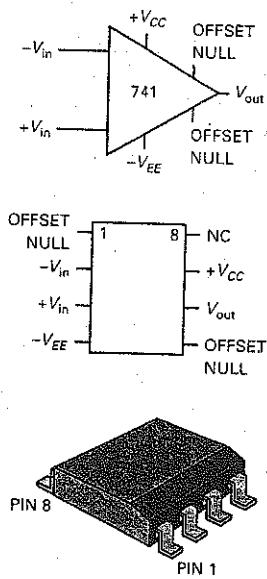
A video or wideband amplifier has a flat response (constant decibel voltage gain) over a very broad range of frequencies. Typical bandwidths are well into the megahertz region. Video amps are not necessarily dc amps, but they often do have a response that extends down to zero frequency. They are used in applications in which the range of input frequencies is very large. For instance, many oscilloscopes handle frequencies from 0 to over 100 MHz; instruments like these use video amps to increase the signal strength before applying it to the cathode-ray tube. As another example, the LM7171 is a very high speed amplifier with a wide unity-gain bandwidth of 200 MHz and a slew rate of 4100 V/ μ s. This amplifier finds applications in video cameras, copiers and scanners, and HDTV amplifiers.

IC video amps have voltage gains and bandwidths that you can adjust by connecting different external resistors. For instance, the VLA702 has a decibel voltage gain of 40 dB and a cutoff frequency of 5 MHz; by changing external components, you can get useful gain to 30 MHz. The MC1553 has a decibel voltage gain of 52 dB and a bandwidth of 20 MHz; these are adjustable by changing external components. The LM733 has a very wide bandwidth; it can be set up to give 20 dB gain and a bandwidth of 120 MHz.

RF and IF Amplifiers

A radio-frequency (RF) amplifier is usually the first stage in an AM, FM, or television receiver. Intermediate-frequency (IF) amplifiers typically are the middle stages. ICs like the LM703 include RF and IF amplifiers on the same chip. The amplifiers are tuned (resonant) so that they amplify only a narrow band of frequencies. This allows the receiver to tune a desired signal from a particular radio or television station. As mentioned earlier, it is impractical to integrate inductors and large capacitors on a chip. For this reason, you have to connect external inductors and capacitors to the chip to get tuned amplifiers. Another example of RF ICs is the MBC13720. This low-noise amplifier is designed to operate in the 400 MHz to 2.4 GHz range, which is where many broadband wireless applications are found.

The SM version of the LM741 op amp.



Voltage Regulators

Chapter 4 discussed rectifiers and power supplies. After filtering, we have a dc voltage with ripple. This dc voltage is proportional to the line voltage; that is, it will change 10 percent if the line voltage changes 10 percent. In most applications, a 10 percent change in dc voltage is too much, and voltage regulation is necessary. Typical of IC voltage regulators is the LM340 series. Chips of this type can hold the output dc voltage to within 0.01 percent for normal changes in line voltage and load resistance. Other features include positive or negative output, adjustable output voltage, and short-circuit protection.

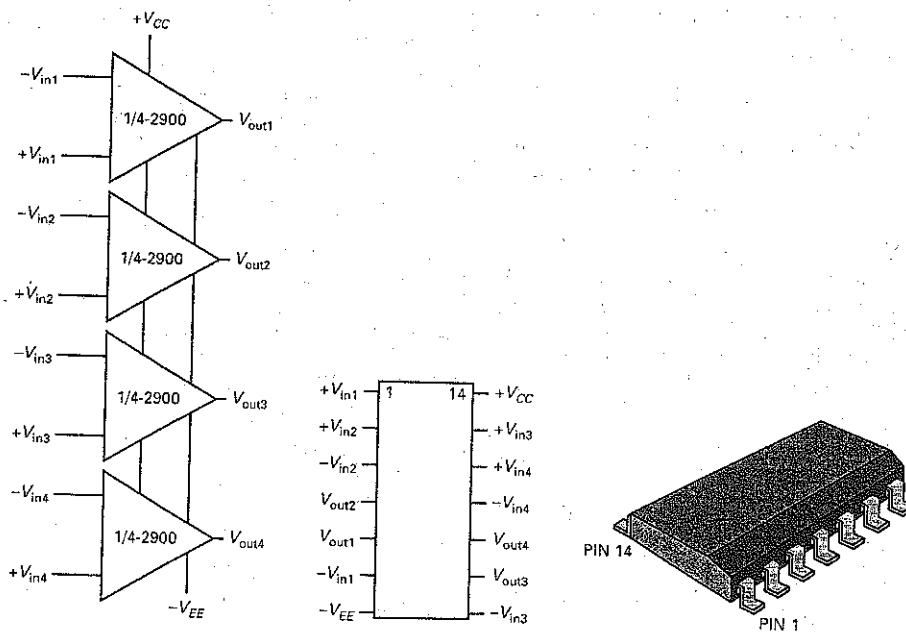
18-7 Op Amps as Surface-Mount Devices

Operational amplifiers and similar kinds of analog circuits are frequently available in surface-mount (SM) packages as well as in the more traditional dual-in-line IC forms. Because the pinout for most op amp tends to be relatively simple, the small outline package (SOP) is the preferred SM style.

For example, the LM741 op amp—the mainstay of school electronics labs for many years—is now available in the latest SOP package (at left). In this instance, the pinout of the surface-mount device (SMD) is the same as the pinout for the more familiar dual-in-line version.

The LM2900, a quad op amp, is an example of a more complex op-amp SMD package. This device is provided in a feed-through, 14-pin DIP and a 14-pin SOT (below). Conveniently, the pinouts are identical for the two packages.

A typical quad op-amp circuit provided in a 14-pin SOT package.



Summary

SEC. 18-1 INTRODUCTION TO OP AMPS

A typical op amp has a noninverting input, an inverting input, and a single-ended output. An ideal op amp has infinite open-loop voltage gain, infinite input resistance, and zero output impedance. It is a perfect amplifier, a voltage-controlled voltage source (VCS).

SEC. 18-2 THE 741 OP AMP

The 741 is a standard op amp that is widely used. It includes an internal compensating capacitor to prevent oscillations. With a large load resistance, the output signal can swing to within 1 or 2 V of either supply. With small load resistances, MPP is limited by the short-circuit current. The slew rate is the maximum speed at which the output voltage can change when driven by a step input. The power bandwidth is directly proportional to slew rate and inversely proportional to the peak output voltage.

SEC. 18-3 THE INVERTING AMPLIFIER

The inverting amplifier is the most basic op-amp circuit. It uses negative feedback

to stabilize the closed-loop voltage gain. The inverting input is a virtual ground because it is a short for voltage but an open for current. The closed-loop voltage gain equals the feedback resistance divided by the input resistance. The closed-loop bandwidth equals the unity-gain frequency divided by the closed-loop voltage gain.

SEC. 18-4 THE NONINVERTING AMPLIFIER

The noninverting amplifier is another basic op-amp circuit. It uses negative feedback to stabilize the closed-loop voltage gain. A virtual short is between the noninverting input and the inverting input. The closed-loop voltage gain equals $R_f/R_1 + 1$. The closed-loop bandwidth equals the unity-gain frequency divided by the closed-loop voltage gain.

SEC. 18-5 TWO OP-AMP APPLICATIONS

The summing amplifier has two or more inputs and one output. Each input is amplified by its channel gain. The output is the sum of the amplified inputs. If all channel gains equal unity, the output

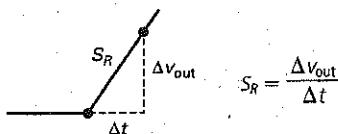
equals the sum of the inputs. In a mixer, a summing amplifier can amplify and combine audio signals. A voltage follower has a closed-loop voltage gain of unity and a bandwidth of f_{unity} . The circuit is useful as an interface between a high-impedance source and a low-impedance load.

SEC. 18-6 LINEAR ICs

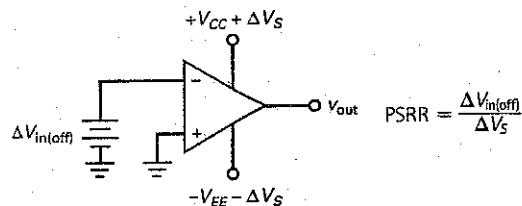
Op amps represent about a third of all linear ICs. A wide variety of op amps exists for almost any application. Some have very low input offsets, others have high bandwidths and slew rates, and others have low drifts. Dual and quad op amps are available. Even high-power op amps exist that can produce large load power. Other linear ICs include audio and video amplifiers, RF and IF amplifiers, and voltage regulators.

Definitions

(18-1) Slew rate:

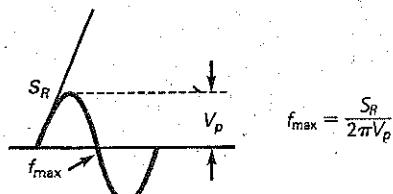


(18-17) Power-supply rejection ratio:

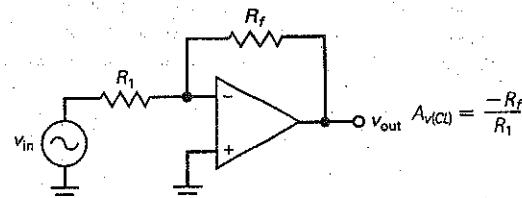


Derivations

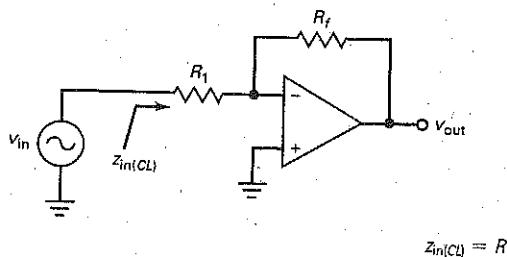
(18-2) Power bandwidth:



(18-3) Closed-loop voltage gain:

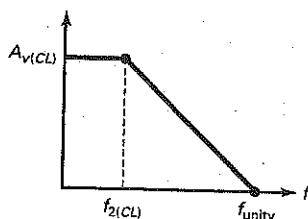


(18-4) Closed-loop input impedance:



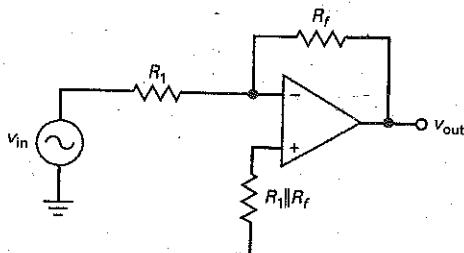
$$Z_{in(CL)} = R_1$$

(18-5) Closed-loop bandwidth:



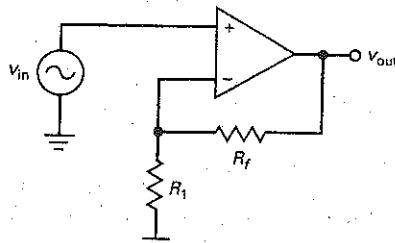
$$f_2(CL) = \frac{f_{unity}}{A_{V(CL)}}$$

(18-11) Compensating resistor:



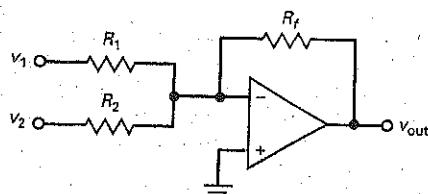
$$R_{B1} = R_1 \parallel R_f$$

(18-12) Noninverting amplifier:



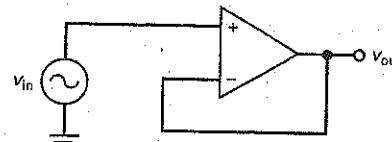
$$A_{V(CL)} = \frac{R_f}{R_1} + 1$$

(18-13) Summing amplifier:



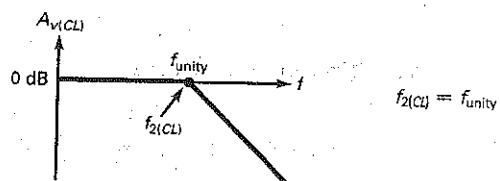
$$V_{out} = A_{V1(CL)}V_1 + A_{V2(CL)}V_2$$

(18-15) Voltage follower:



$$A_{V(CL)} = 1$$

(18-16) Follower bandwidth:



$$f_2(CL) = f_{unity}$$

Student Assignments

- What usually controls the open-loop cutoff frequency of an op amp?
 - Stray-wiring capacitance
 - Base-emitter capacitance
 - Collector-base capacitance
 - Compensating capacitance
- A compensating capacitor prevents
 - Voltage gain
 - Oscillations
 - Input offset current
 - Power bandwidth
- At the unity-gain frequency, the open-loop voltage gain is
 - 1
 - $A_{V(mid)}$
 - Zero
 - Very large
- The cutoff frequency of an op amp equals the unity-gain frequency divided by
 - The cutoff frequency
 - Closed-loop voltage gain
 - Unity
 - Common-mode voltage gain
- If the cutoff frequency is 20 Hz and the midband open-loop voltage gain is 1,000,000, the unity-gain frequency is
 - 20 Hz
 - 1 MHz
 - 2 MHz
 - 20 MHz
- If the unity-gain frequency is 5 MHz and the midband open-loop voltage gain is 100,000, the cutoff frequency is
 - 50 Hz
 - 1 MHz
 - 1.5 MHz
 - 15 MHz

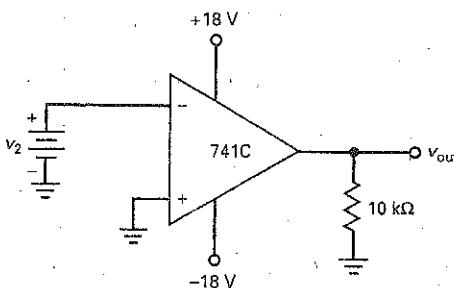
7. The initial slope of a sine wave is directly proportional to
- Slew rate
 - Frequency
 - Voltage gain
 - Capacitance
8. When the initial slope of a sine wave is greater than the slew rate,
- Distortion occurs
 - Linear operation occurs
 - Voltage gain is maximum
 - The op amp works best
9. The power bandwidth increases when
- Frequency decreases
 - Peak value decreases
 - Initial slope decreases
 - Voltage gain increases
10. A 741C contains
- Discrete resistors
 - Inductors
 - Active-load resistors
 - A large coupling capacitor
11. A 741C cannot work without
- Discrete resistors
 - Passive loading
 - DC return paths on the two bases
 - A small coupling capacitor
12. The input impedance of a BIFET op amp is
- Low
 - Medium
 - High
 - Extremely high
13. An LF157A is a
- Diff amp
 - Source follower
 - Bipolar op amp
 - BIFET op amp
14. If the two supply voltages are ± 12 V, the MPP value of an op amp is closest to
- 0
 - $+12$ V
 - -12 V
 - 24 V
15. The open-loop cutoff frequency of a 741C is controlled by
- A coupling capacitor
 - The output short circuit current
 - The power bandwidth
 - A compensating capacitor
16. The 741C has a unity-gain frequency of
- 10 Hz
 - 20 kHz
 - 1 MHz
 - 15 MHz
17. The unity-gain frequency equals the product of closed-loop voltage gain and the
- Compensating capacitance
 - Tail current
 - Closed-loop cutoff frequency
 - Load resistance
18. If f_{unity} is 10 MHz and midband open-loop voltage gain is 200,000, then the open-loop cutoff frequency of the op amp is
- 10 Hz
 - 20 Hz
 - 50 Hz
 - 100 Hz
19. The initial slope of a sine wave increases when
- Frequency decreases
 - Peak value increases
 - C_C increases
 - Slew rate decreases
20. If the frequency of the input signal is greater than the power bandwidth,
- Slew-rate distortion occurs
 - A normal output signal occurs
 - Output offset voltage increases
 - Distortion may occur
21. An op amp has an open base resistor. The output voltage will be
- Zero
 - Slightly different from zero
 - Maximum positive or negative
 - An amplified sine wave
22. An op amp has a voltage gain of 200,000. If the output voltage is 1 V, the input voltage is
- $2 \mu\text{V}$
 - $5 \mu\text{V}$
 - 10 mV
 - 1 V
23. A 741C has supply voltages of ± 15 V. If the load resistance is large, the MPP value is approximately
- 0
 - $+15$ V
 - 27 V
 - 30 V
24. Above the cutoff frequency, the voltage gain of a 741C decreases approximately
- 10 dB per decade
 - 20 dB per octave
 - 10 dB per octave
 - 20 dB per decade
25. The voltage gain of an op amp is unity at the
- Cutoff frequency
 - Unity-gain frequency
 - Generator frequency
 - Power bandwidth
26. When slew-rate distortion of a sine wave occurs, the output
- Is larger
 - Appears triangular
 - Is normal
 - Has no offset
27. A 741C has
- A voltage gain of 100,000
 - An input impedance of $2 \text{ M}\Omega$
 - An output impedance of 75Ω
 - All of the above
28. The closed-loop voltage gain of an inverting amplifier equals
- The ratio of the input resistance to the feedback resistance
 - The open-loop voltage gain
 - The feedback resistance divided by the input resistance
 - The input resistance
29. The noninverting amplifier has a
- Large closed-loop voltage gain
 - Small open-loop voltage gain
 - Large closed-loop input impedance
 - Large closed-loop output impedance
30. The voltage follower has a
- Closed-loop voltage gain of unity
 - Small open-loop voltage gain
 - Closed-loop bandwidth of zero
 - Large closed-loop output impedance
31. A summing amplifier can have
- No more than two input signals
 - Two or more input signals
 - A closed-loop input impedance of infinity
 - A small open-loop voltage gain

Problems

SEC. 18-2 THE 741 OP AMP

- 18-1 Assume that negative saturation occurs at 1 V less than the supply voltage with an 741C. How much inverting input voltage does it take to drive the op amp of Fig. 18-29 into negative saturation?

Figure 18-29



- 18-2 What is the common-mode rejection ratio of an LF157A at low frequencies? Convert this decibel value to an ordinary number.
- 18-3 What is the open-loop voltage gain of an LF157A when the input frequency is 1 kHz? 10 kHz? 100 kHz? (Assume a first-order response, that is, 20 dB per decade rolloff.)
- 18-4 The input voltage to an op amp is a large voltage step. The output is an exponential waveform that changes 2.0 V in 0.4 μ s. What is the slew rate of the op amp?
- 18-5 An LM318 has a slew rate of 70 V/ μ s. What is the power bandwidth for a peak output voltage of 7 V?
- 18-6 Use Eq. (18-2) to calculate the power bandwidth for each of the following:
- $S_R = 0.5 \text{ V}/\mu\text{s}$ and $V_p = 1 \text{ V}$
 - $S_R = 3 \text{ V}/\mu\text{s}$ and $V_p = 5 \text{ V}$
 - $S_R = 15 \text{ V}/\mu\text{s}$ and $V_p = 10 \text{ V}$

SEC. 18-3 THE INVERTING AMPLIFIER

- 18-7 **Multisim**: What are closed-loop voltage gain and bandwidth in Fig. 18-30? What is the output voltage at 1 kHz? At 10 MHz? Draw the ideal Bode plot of closed-loop voltage gain.

Figure 18-30

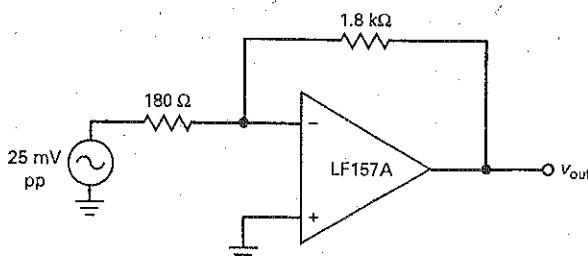
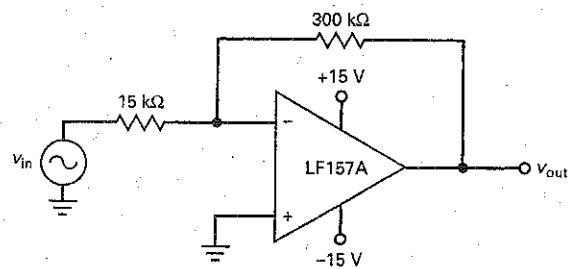


Figure 18-31



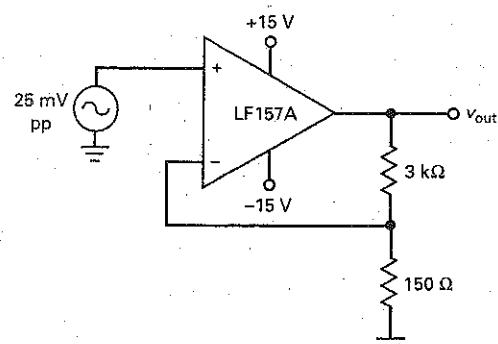
- 18-8 What is the output voltage in Fig. 18-31 when v_{in} is zero? Use the typical values of Table 18-1.

- 18-9 The data sheet of an LF157A lists the following worst-case parameters: $I_{in(bias)} = 50 \text{ pA}$, $I_{in(off)} = 10 \text{ pA}$, and $V_{in(off)} = 2 \text{ mV}$. Recalculate the output voltage when v_{in} is zero in Fig. 18-31.

SEC. 18-4 THE NONINVERTING AMPLIFIER

- 18-10 **Multisim**: In Fig. 18-32, what are the closed-loop voltage gain and bandwidth? The ac output voltage at 100 kHz?
- 18-11 What is the output voltage when v_{in} is reduced to zero in Fig. 18-32? Use the worst-case parameters given in Prob. 18-9.

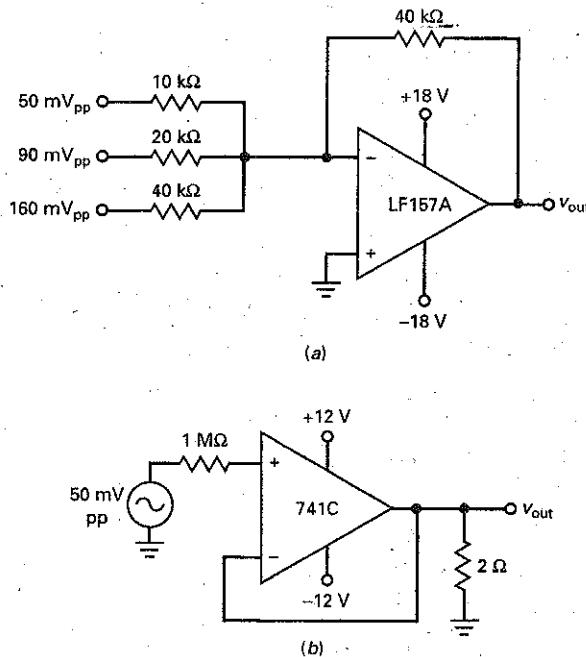
Figure 18-32



SEC. 18-5 TWO OP-AMP APPLICATIONS

- 18-12 **Multisim** In Fig. 18-33a, what is the ac output voltage? If a compensating resistor needs to be added to the noninverting input, what size should it be?

Figure 18-33



Critical Thinking

- 18-14 The adjustable resistor of Fig. 18-34 can be varied from 0 to 100 kΩ. Calculate the minimum and maximum closed-loop voltage gain and bandwidth.
- 18-15 Calculate the minimum and maximum closed-loop voltage gain and bandwidth in Fig. 18-35.

- 18-13 What is the output voltage in Fig. 18-33b? The bandwidth?

- 18-16 In Fig. 18-33b, the ac output voltage is 49.98 mV. What is the closed-loop output impedance?

- 18-17 What is the initial slope of a sine wave with a frequency of 15 kHz and a peak value of 2 V? What happens to the initial slope if the frequency increases to 30 kHz?

Figure 18-34

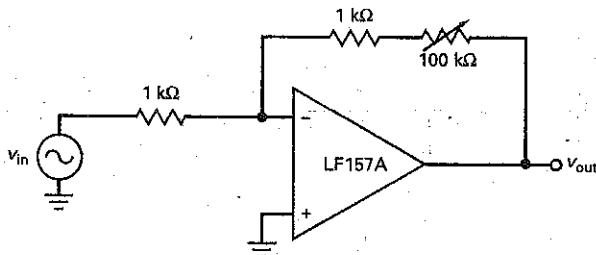
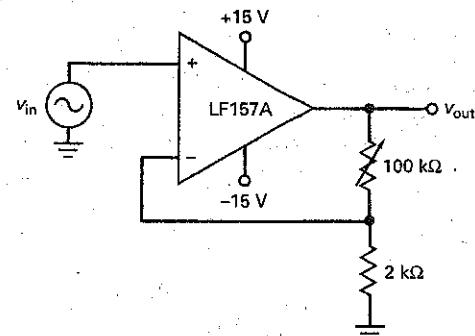


Figure 18-35



18-18 Which op amp in Table 18-3 has the following:

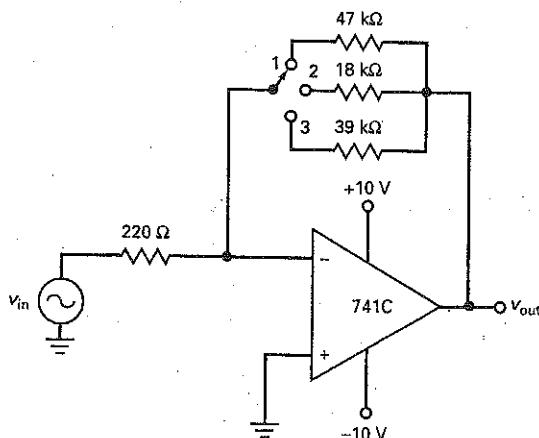
- Minimum input offset voltage
- Minimum input offset current
- Maximum output-current capability
- Maximum bandwidth
- Minimum drift

18-19 What is the CMRR of a 741C at 100 kHz? The MPP value when the load resistance is $500\ \Omega$? The open-loop voltage gain at 1 kHz?

18-20 If the feedback resistor in Fig. 18-33a is changed to a $100\text{-k}\Omega$ variable resistor, what is the maximum output voltage? The minimum?

18-21 In Fig. 18-36, what is the closed-loop voltage gain for each switch position?

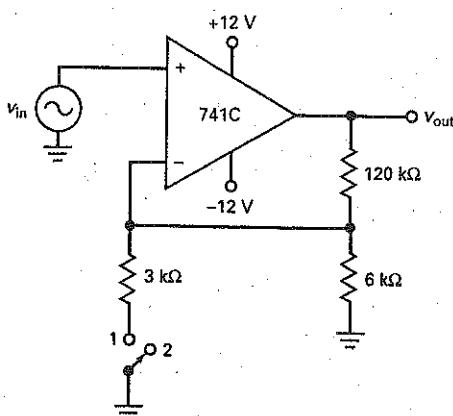
Figure 18-36



18-22 What is the closed-loop voltage gain for each switch position of Fig. 18-37? The bandwidth?

18-23 In wiring the circuit of Fig. 18-37, a technician leaves the ground off the $6\text{-k}\Omega$ resistor. What is the closed-loop voltage gain in each switch position?

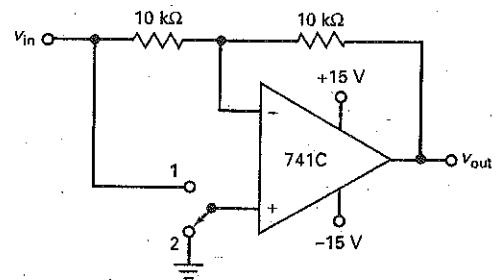
Figure 18-37



18-24 If the $120\text{-k}\Omega$ resistor opens in Fig. 18-37, what is the output voltage most likely to do?

18-25 What is the closed-loop voltage gain for each switch position of Fig. 18-38? The bandwidth?

Figure 18-38



18-26 If the input resistor of Fig. 18-38 opens, what is the closed-loop voltage gain for each switch position?

18-27 If the feedback resistor opens in Fig. 18-38, what is the output voltage most likely to do?

18-28 The worst-case parameters for a 741C are $I_{in(bias)} = 500\text{ nA}$, $I_{in(off)} = 200\text{ nA}$, and $V_{in(off)} = 6\text{ mV}$. What is the total output error voltage in Fig. 18-39?

18-29 In Fig. 18-39, the input signal has a frequency of 1 kHz. What is the ac output voltage?

18-30 If the capacitor is shorted in Fig. 18-39, what is the total output error voltage? Use the worst-case parameters given in Prob. 18-28.

Figure 18-39

