USING SEVEN-SEGMENT DISPLAYS — PART 1

By Ray Marston

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SEVEN-SEGMENT DISPLAYS

A very common requirement in modern electronics is that of displaying alphanumeric characters. Digital watches, pocket calculators, and digital multimeters and frequency meters are all examples of devices that use such displays. The best known type of alphanumeric indicator is the seven-segment display, which comprises seven independently-accessible photoelectric segments (such as LEDs or LCDs, or gas-discharge or fluorescent elements, etc.) arranged in the form shown in **Figure 1**.
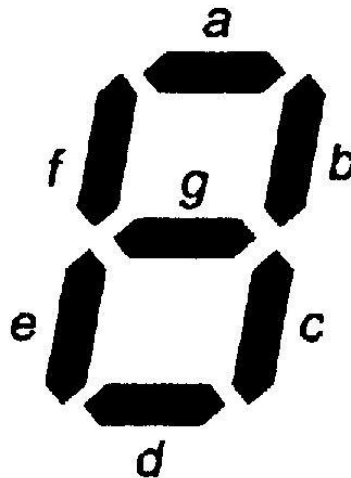
FIGURE 1. Standard form and notations of a seven-segment display.


The segments are conventionally notated from a to g in the manner shown in the diagram, and it is possible to make them display any number (numeral) from 0 to 9 or alphabetic character from A to F (in a mixture of upper and lower case letters) by activating these segments in various combinations, as shown in the truth table in **Figure 2**.

Segments (✓ = ON)							Display	Segments (✓ = ON)							Display
a	b	c	d	e	f	g		a	b	c	d	e	f	g	
✓	✓	✓	✓	✓	✓		0	✓	✓	✓	✓	✓	✓	✓	8
	✓	✓					1	✓	✓	✓			✓	✓	9
✓	✓		✓	✓		✓	2	✓	✓	✓		✓	✓	✓	A
✓	✓	✓	✓			✓	3			✓	✓	✓	✓	✓	b
	✓	✓			✓	✓	4	✓			✓	✓	✓		C
✓		✓	✓		✓	✓	5		✓	✓	✓	✓		✓	d
✓		✓	✓	✓	✓	✓	6	✓			✓	✓	✓	✓	E
✓	✓	✓					7	✓				✓	✓	✓	F

FIGURE 2. Truth table for a seven-segment display.

Practical seven-segment display devices must be provided with at least eight external connection terminals; seven of these give access to the individual photoelectric segments, and the eighth provides a common connection to all segments. If the display is an LED type, the seven individual LEDs may be arranged in the form shown in **Figure 3**, in which all LED anodes are connected to the common terminal, or they may be arranged as in **Figure 4**, in which all LED cathodes are connected to the common terminal. In the former case, the device is known as a common-anode seven-segment display; in the latter case, the device is known as a common-cathode seven-segment display.
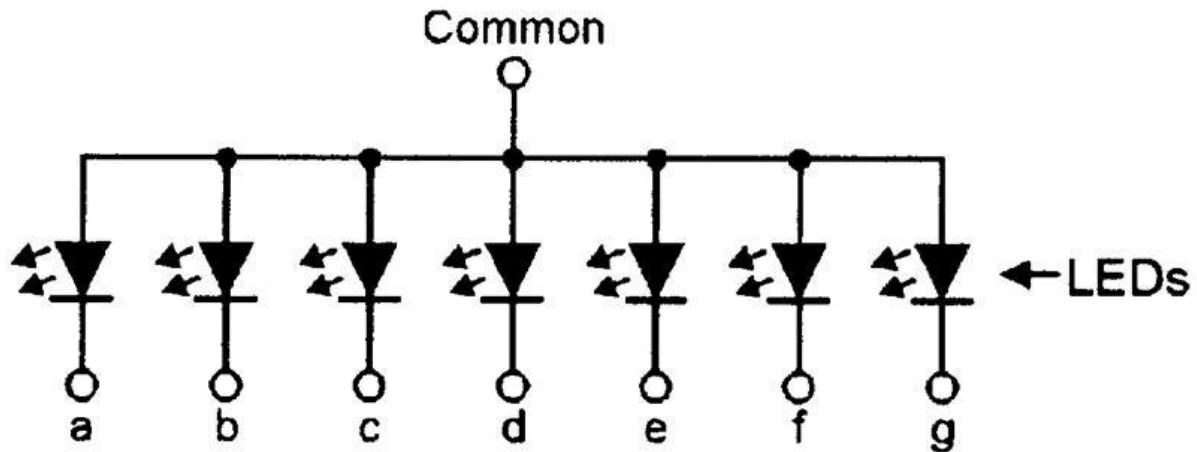
FIGURE 3. Schematic diagram of a common-anode seven-segment LED display.
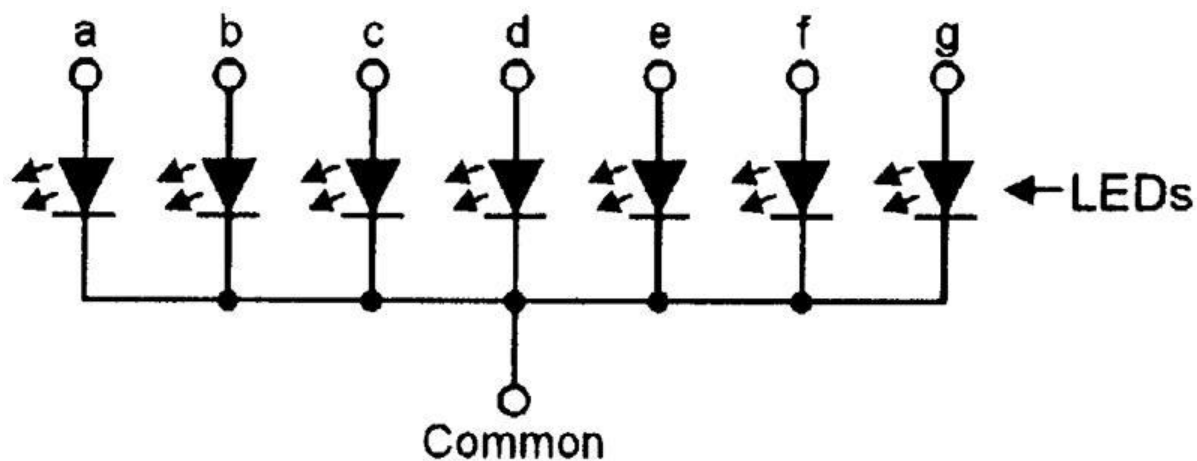
FIGURE 4. Schematic diagram of a common-cathode seven-segment LED display.

SEVEN-SEGMENT DISPLAY/DRIVERS

In most practical applications, seven-segment displays are used to give a visual indication of the output states of digital ICs such as decade counters and latches, etc. These outputs are usually in four-bit BCD (Binary Coded Decimal) form and are not suitable for directly driving seven-segment displays. Consequently, special BCD-to-seven-segment decoder/driver ICs are available to convert the BCD signal into a form suitable for driving these displays, and are connected between the BCD signals and the display in the manner shown in **Figure 5**.
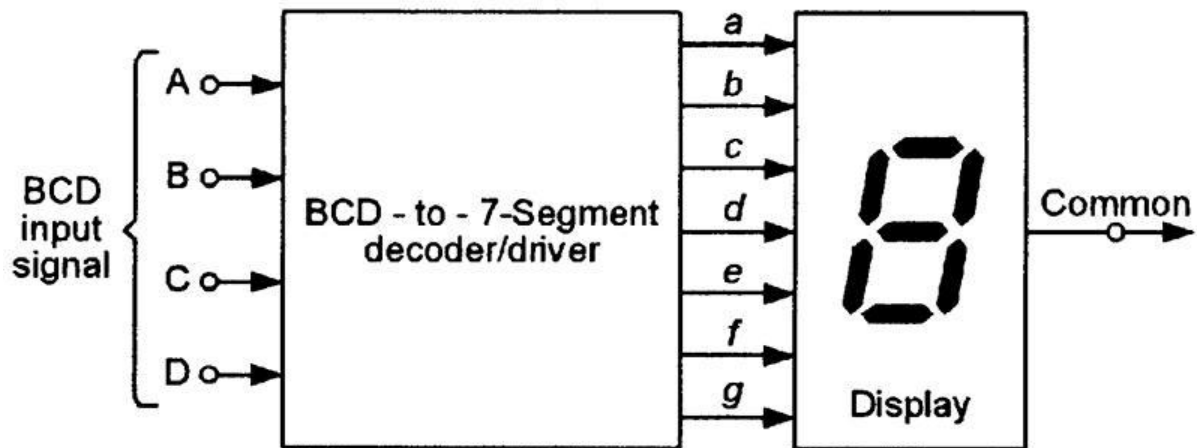
FIGURE 5. Basic connections of a BCD-to-seven-segment decoder/driver IC.

The table in **Figure 6** shows the relationship between the BCD signals and the displayed seven-segment numerals.

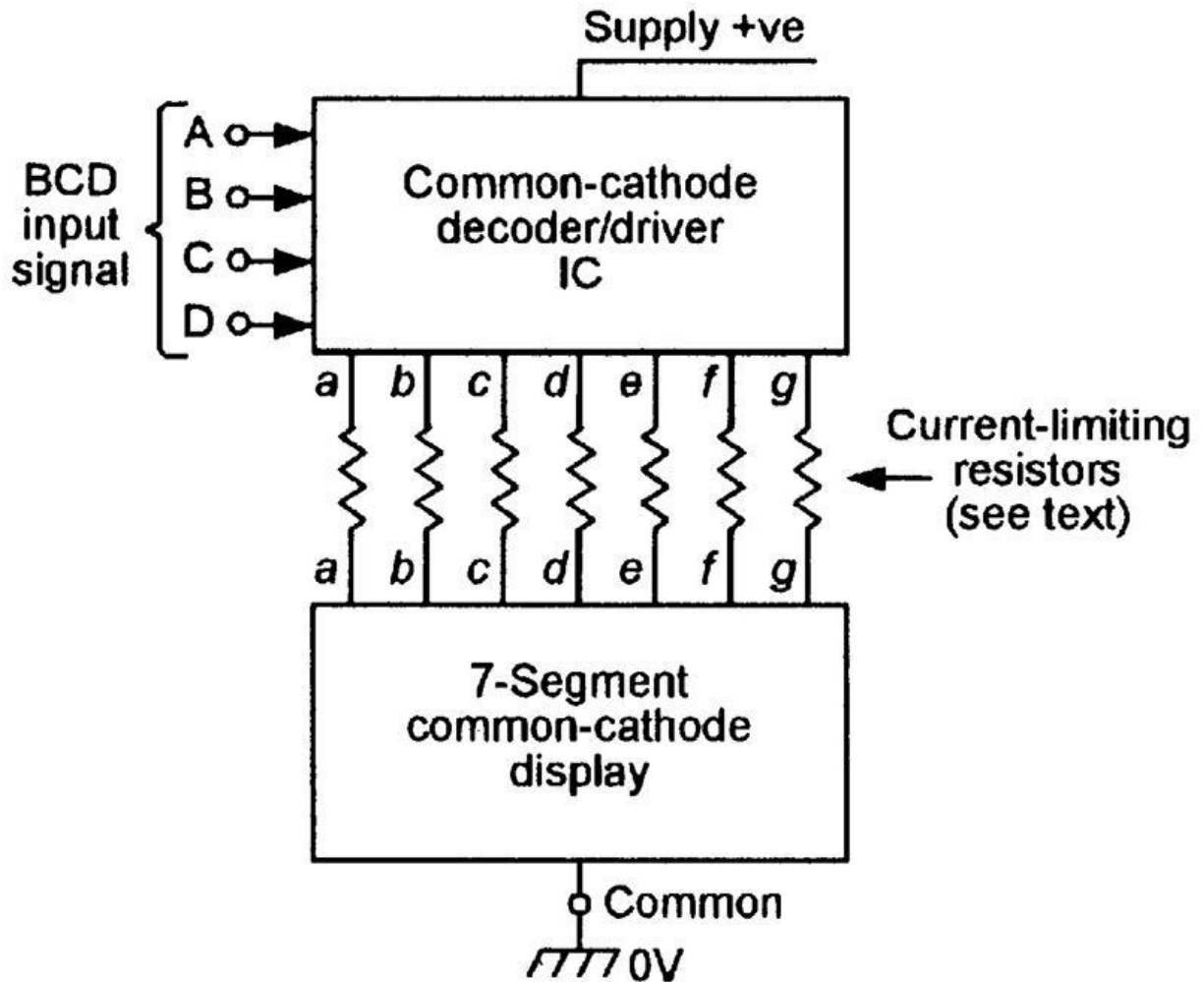| BCD Signal				Display	BCD Signal				Display
D	C	B	A		D	C	B	A	
0	0	0	0	*0*	0	1	0	1	*5*
0	0	0	1	*1*	0	1	1	0	*6*
0	0	1	0	*2*	0	1	1	1	*7*
0	0	1	1	*3*	1	0	0	0	*8*
0	1	0	0	*4*	1	0	0	1	*9*

0 = logic low   1 = logic high

FIGURE 6. Truth table of a BCD-to-seven-segment decoder/driver.

In practice, BCD-to-seven-segment decoder/driver ICs are usually available in a dedicated form that is suitable for driving only a single class of display unit, e.g., either common-anode LED type, or common-cathode LED type, or liquid crystal displays (LCDs). **Figures 7** to **9** show the methods of interconnecting each of these IC and display types.

Note in the case of the LED circuits (**Figures 7** and **8**) that, if the IC outputs are unprotected (as in the case of most TTL ICs), a current-limiting resistor must be wired in series with each display segment (about 150R with a 5V supply, or 680R at 15V); most CMOS ICs have internally current-limited outputs, and do not require the use of these external resistors. To drive a common-anode display (**Figure 7**), the driver must have an active-low output, in which each segment-driving output is normally high, but goes low to turn a segment on. To drive a common-cathode display (**Figure 8**), the driver must have an active-high output.
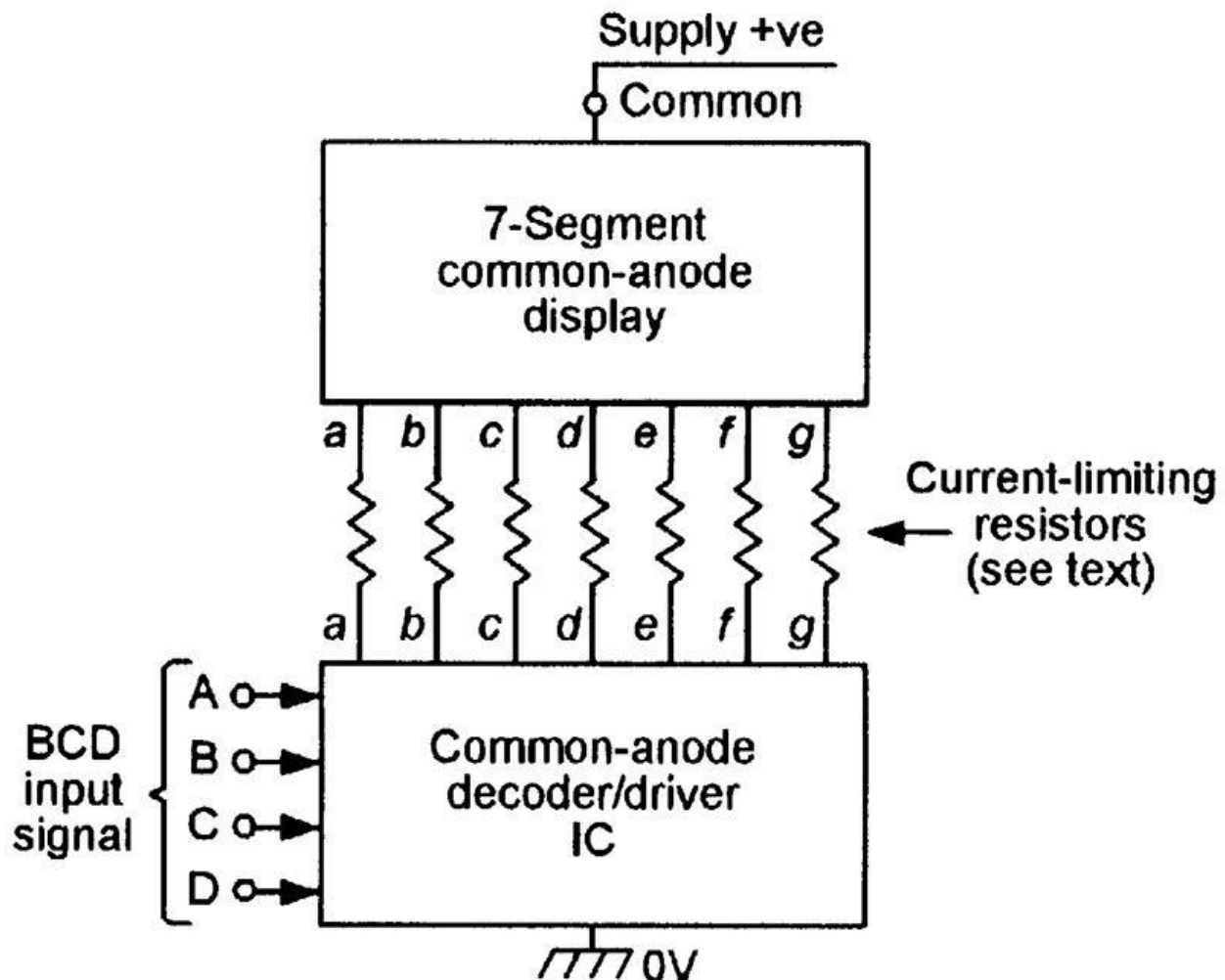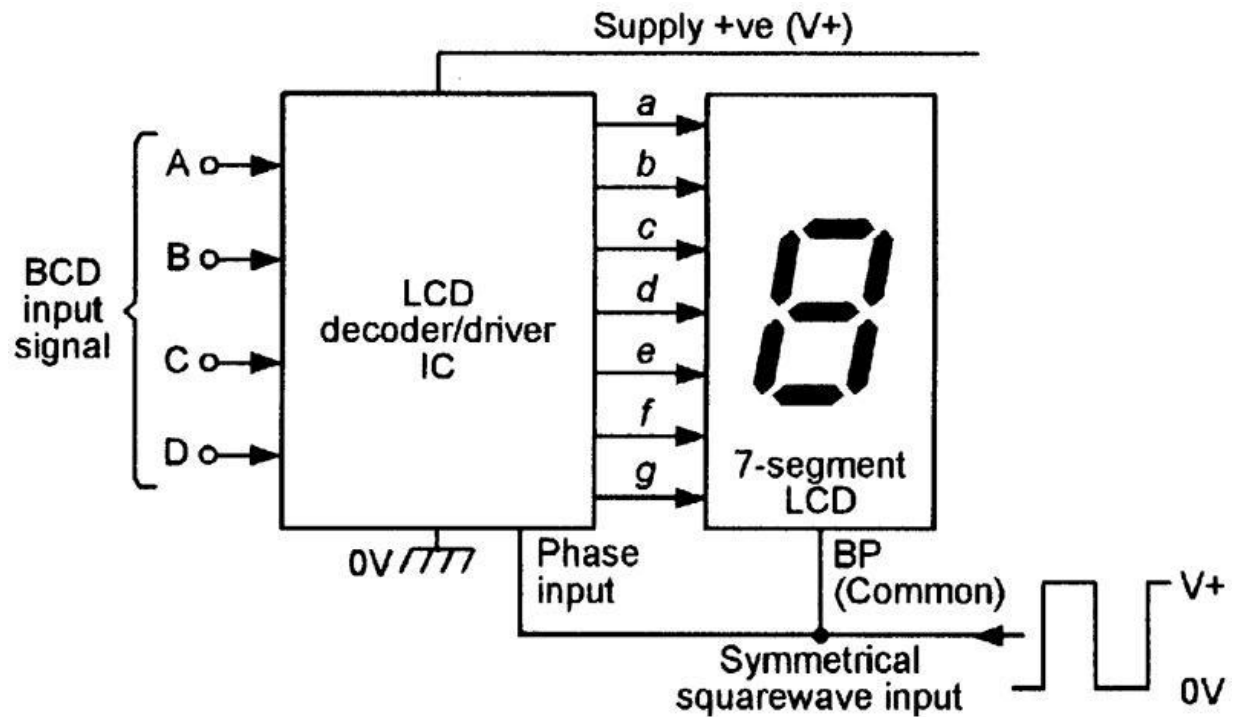
**FIGURE 8.** Method of driving a common-cathode LED display.

FIGURE 9. Method of driving a liquid-crystal display (LCD).

In the **Figure 9** LCD-driving circuit, the display's common BP (back-plane) terminal and the IC's phase input terminals must be driven by a symmetrical square wave (typically 30Hz to 200Hz) that switches fully between the two supply rail voltages (0V and V+), as shown. The full explanation for this is a little complicated, as follows.

To drive an LCD segment, the driving voltage must be applied between the segment and BP terminals. When the voltage is zero, the segment is effectively invisible. When the drive voltage has a significant positive or negative value, however, the segment becomes effectively visible, but if the drive voltage is sustained for more than a few hundred milliseconds, the segment may become permanently visible and be of no further value.

The way around this problem is — in principle — to drive the segment on via a perfectly symmetrical squarewave that switches alternately between identical positive and negative voltages, and thus has zero DC components and will not damage the LCD segment even if sustained permanently. In practice, this type of waveform is actually generated with the aid of an EX-OR True/Complement generator, connected as shown in **Figure 10(a)**.
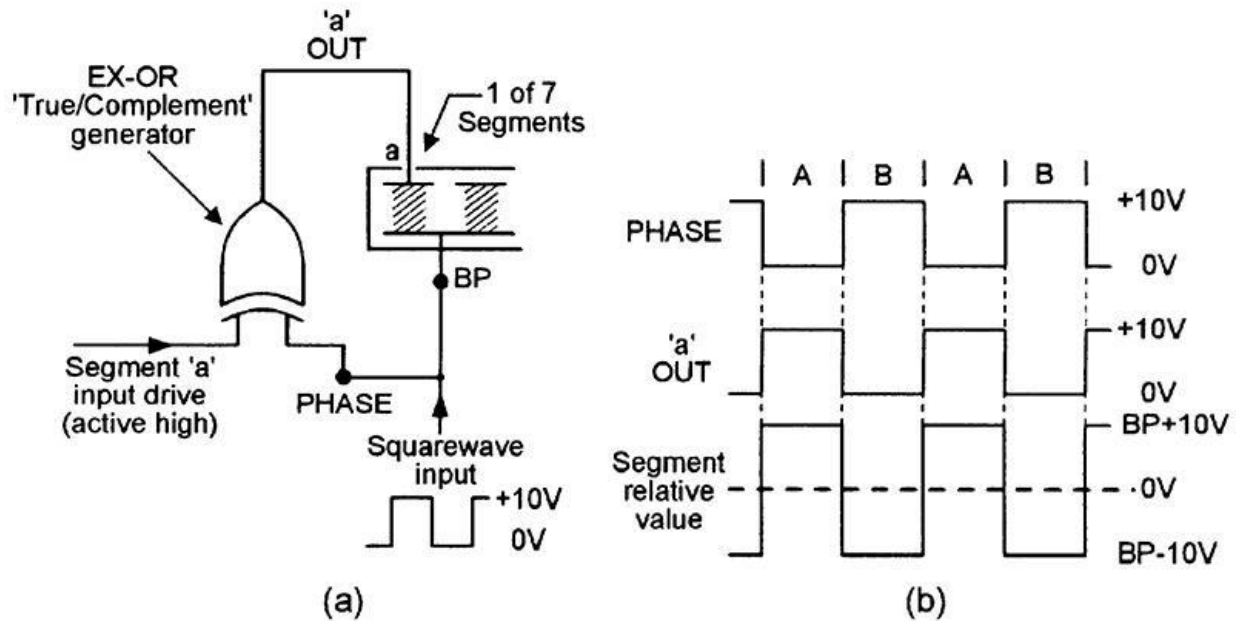
FIGURE 10. Basic LCD segment-drive circuit **(a)**, and voltage-doubling 'bridge-driven' segment waveforms **(b)**.

In **Figure 10(a)**, the basic segment 'a' input drive (which is active-high) is connected to one input of the EX-OR element, and the other EX-OR input terminal (which is notated PHASE) is driven by a symmetrical squarewave that switches fully between the circuit's supply rail voltages (shown as 0V and +10V) and is also applied to the LCD display's BP pin.

When the segment 'a' input drive is low, the EX-OR element gives a non-inverted (in-phase) 'a' output when the squarewave is at logic-0, and an inverted (anti-phase) 'a' output when the squarewave is at logic-1, and thus produces zero voltage difference between the 'a' segment and BP points under both these conditions. The segment is thus turned off under these conditions.

When the segment 'a' input drive is high, the EX-OR element gives the same phase action as just described, but in this case, the 'a' OUT pin is high and BP is low when the squarewave is at logic-0, and 'a' OUT is low and BP is high when the squarewave is at logic-1. The segment is thus turned on under these conditions.

Figure 10(b) shows the circuit waveforms that occur when the 'a' segment is turned on, with the 'a' segment and BP driven by anti-phase squarewaves. Thus, in part A of the waveform, the segment is 10V positive to BP, and in part B, it is 10V negative to BP, so the LCD is effectively driven by a squarewave with a peak-to-peak value of 20V, but with zero DC value. This form of drive is generally known as a voltage-doubling 'bridge drive' system. In practice, many LCD-driving ICs (such as the 4543B) incorporate this type of drive system in the form of a

seven-section EX-OR gate array interposed in series with the segment output pins, with access to its common line via a single PHASE terminal.

Note that any active-high seven-segment LED-driving decoder IC can be used to drive a seven-segment LCD display by interposing a bridge-driven seven-section EX-OR array between its segment output pins and the segment pins of the LCD display, as shown in **Figure 11**, in which a 74LS48 TTL IC is used in this specific way.
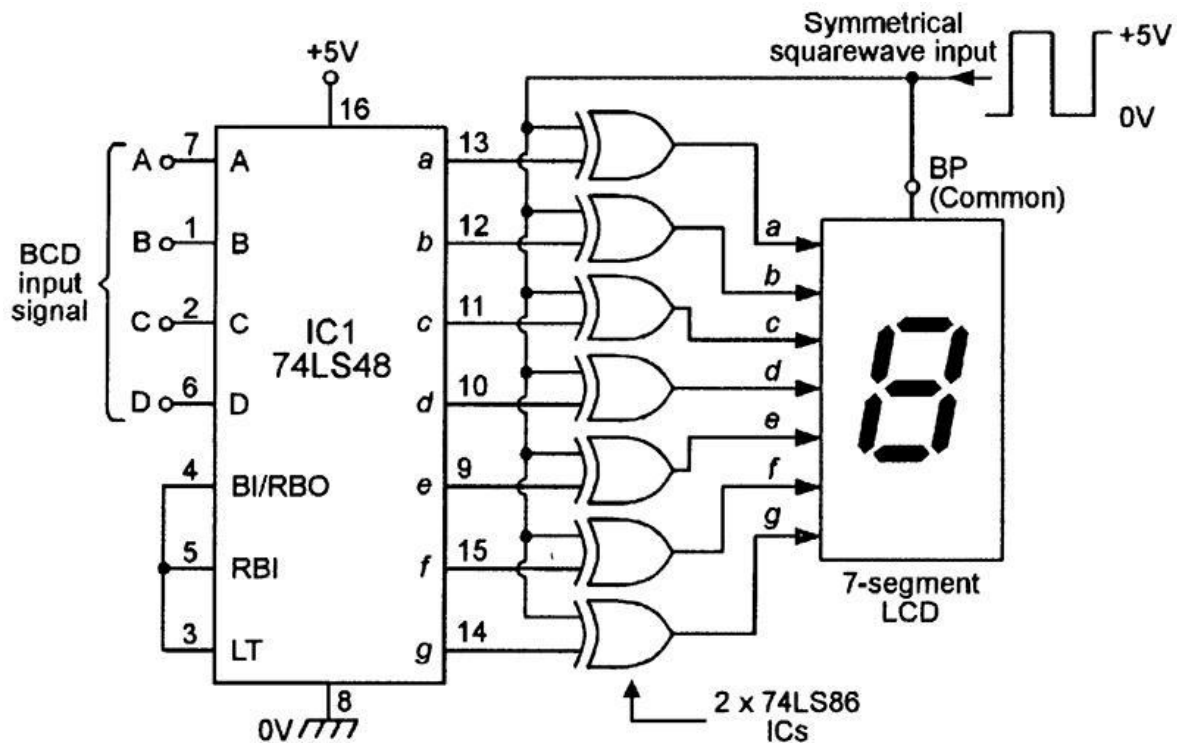
FIGURE 11. Basic way of using an active-high LED-driving decoder IC (such as the 74LS48 TTL type) to drive a seven-segment LCD via a bridge-driven seven-section EX-OR array.

CASCADED DISPLAYS

In most practical seven-segment display applications, several sets of displays and matching decoder/driver ICs are cascaded and used to make multi-digit display systems. **Figure 12**, for example, shows a very simple way of using three sets of decoder/driver ICs and displays in conjunction with three decade counter ICs to make a simple digital-readout frequency meter. Here, the amplified external frequency signal is fed to the input of the series-connected counters via one input of a two-input AND gate, which has its other (GATE) input waveform derived from a built-in timebase generator.
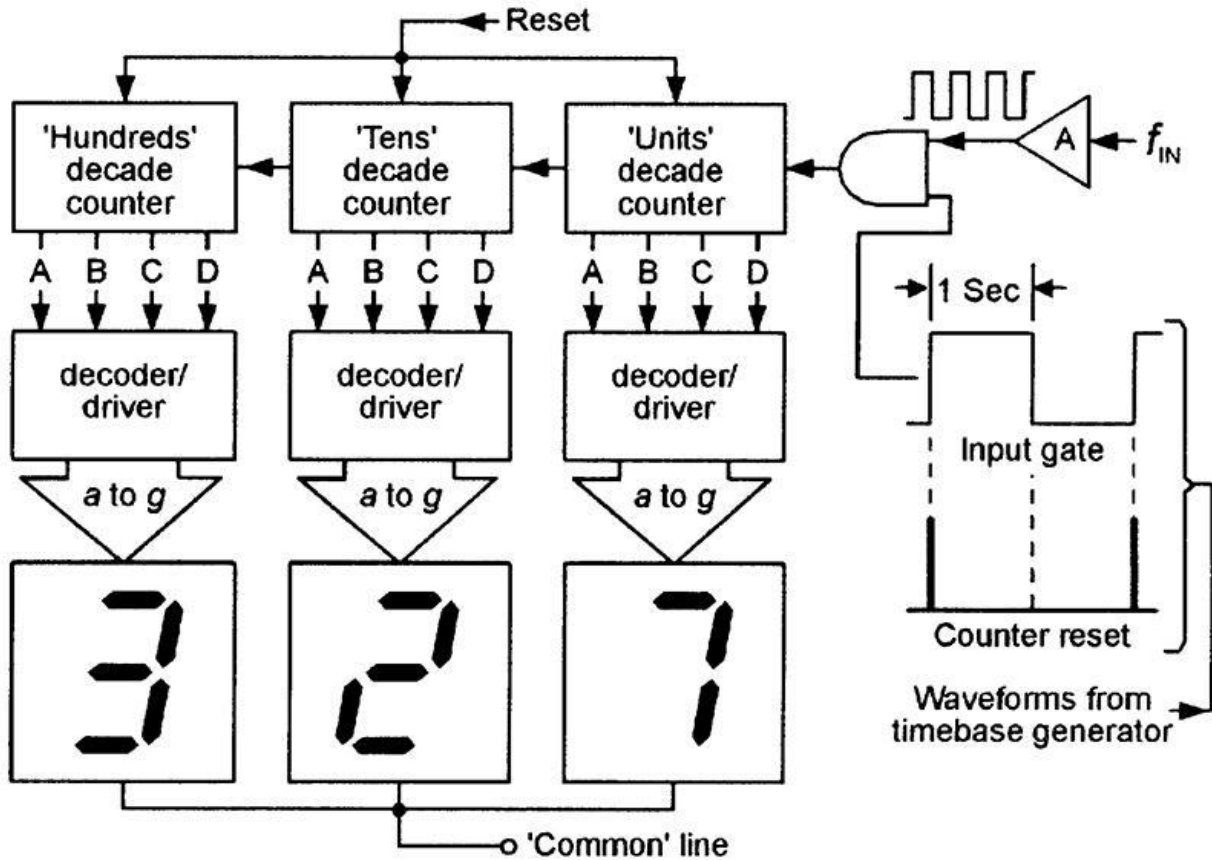
FIGURE 12. Simple digital frequency meter circuit.

The circuit's operating sequence is as follows:

When the timebase GATE input signal is low, the AND gate is closed and no input signals reach the counters. At the moment that the timebase GATE signal switches high, a brief RESET pulse is fed to all three counters, setting them all to zero count; simultaneously, the input gate opens, and remains open for a period of precisely one second, during which time the input-frequency pulses are summed by the counters.

At the end of the one second period, the gate closes and the timebase GATE signal goes low again, thus ending the count and enabling the displays to give a steady reading of that second's total pulse count (and thus the mean signal frequency). The whole process then repeats again one second later, when the timebase GATE signal again goes high.

DISPLAY LATCHING

The simple cascaded system described previously suffers from a major defect, in that the display becomes a blur during the actual counting period, becoming stable and readable only when each count is completed and the input gate is closed. This 'blur-and-read' type of display is very annoying to watch.

Figure 13 shows an improved frequency meter circuit that uses display latching to overcome the above defect. Here, a four-bit data latch is wired between the output of each counter and the input of its decoder/driver IC.
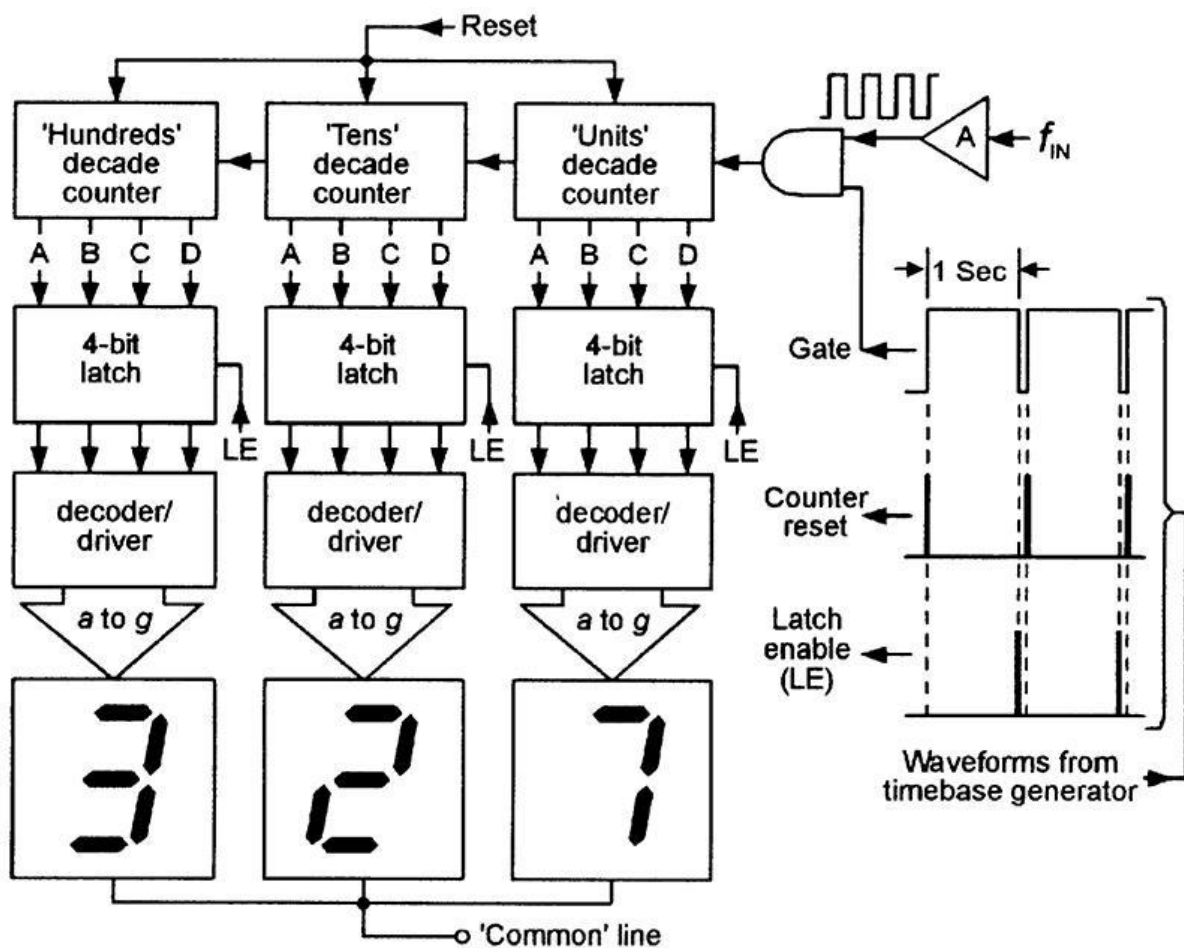
FIGURE 13. Improved digital frequency meter circuit.

This circuit operates as follows:

At the moment that the timebase GATE signal goes high, a RESET pulse is fed to all counters, setting them to zero. Simultaneously, the input gate is opened and the counters start to sum the input signal pulses. This count continues for precisely one second, and during this period, the four-bit latches prevent the counter output signals from reaching the display drivers; the display thus remains stable during this period.

At the end of the one second count period, the AND gate closes and terminates the count, and simultaneously a brief LATCH ENABLE pulse is fed to all latches, causing the prevailing BCD outputs of each counter to be latched into memory and then fed to the display via the decoder/driver ICs, thus causing the display to give a steady reading of the total pulse count (and thus the input frequency).

A few moments later, the sequence repeats again, with the counters resetting and then counting the input frequency pulses for one second, during which time the display gives a steady reading of the results of the previous count, and so on.

The **Figure 13** circuit thus generates a stable display that is updated once every second; in practice, the actual count period of this and the **Figure 12** circuit can be made any decade multiple or submultiple of one second, provided that the output display is suitably scaled.

Note that a three-digit frequency meter can indicate maximum frequencies of 999Hz when using a one-second timebase, 9.99kHz when using a 100mS timebase, 99.9kHz when using a 10mS timebase, and 999kHz when using a 1mS timebase. In reality, many decoder/driver ICs have built-in four-bit data latches.

MULTIPLEXING

Note from the **Figure 12** and **13** circuits that a total of at least 21 connections must be made between the IC circuitry and the seven-segment displays of a three-digit read-out unit; a total of at least 70 connections are needed if a 10-digit display is used. In reality, the number of IC-to-display connections can be greatly reduced by using the technique known as multiplexing. This technique can be understood with the aid of **Figures 14** and **15**.

Figure 14 shows how each digit of a three-digit common-cathode LED display can be individually activated using a total of only 10 external connections; the circuitry to the left of the dotted line should be regarded as 'electronic,' and to the right of the line as 'display' circuitry.
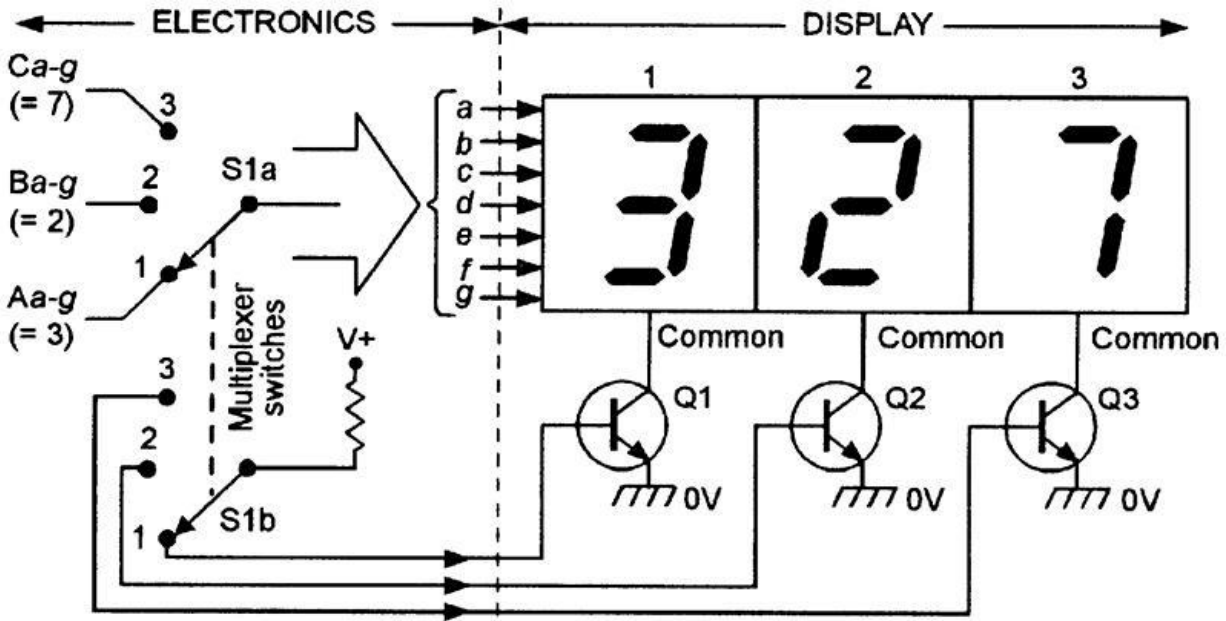
FIGURE 14. Method of multiplexing a three-digit common-cathode LED display.

In the display, all a segments are connected together, as also are all other (b to g) sets of segments, so that a total of only seven external a-to-g, connections are made to the display irrespective of the number of digits used.

Note, however, that none of the seven-segment displays are influenced by signals on these segment wires unless a display is enabled by connecting its common terminal to ground, and in **Figure 14**, this is achieved by activating switching transistors Q1 to Q3 via suitable external signals, which require the use of only one additional connection per display digit.

Note in **Figure 14** that three different sets of segment data can be selected via switch S1a which, in reality, would take the form of a ganged seven-pole three-way electronic switch (with one pole dedicated to each of the seven segment lines), and that any one of the three display digits can be selected via S1b and Q1 to Q3. These switches are ganged together and provide the actual multiplexer action, and should be regarded as fast-acting electronic switches that repeatedly switch through positions 1, 2, and 3. The operating sequence of the circuit is as follows.

Assume initially that the switch is in position 1. Under this condition, S1a selects segment data Aa-g, and S1b activates display 1 via Q1, so that display 1 shows the number 3. A few moments later, the switch jumps to position 2, selecting segment data Ba-g and activating display 2 via Q2, so that display 2 shows the number 2.

A few moments later, the switch jumps to position 3, causing display 3 to show the number 7. A few moments later, the whole cycle starts to repeat again, and so on add infinitum.

In practice, about 50 of these cycles occur each second, so the eye does not see the displays being turned on and off individually, but sees them as an apparently steady display that shows the number 327, or whatever other number is dictated by the segment data.

Note from the above description that, since each display is turned on for only one-third of each cycle, the mean current consumption of each display is one-third of the peak display current, and the LED brightness levels are correspondingly reduced. In practical multiplexers, the peak display current is made fairly high, to give adequate display brightness.

Figure 15 shows an example of an improved multiplexing (MUX) technique, as applied to a three-digit frequency meter. In this case, the MUX is interposed between the outputs of the three BCD data latches and the input of the BCD-to-seven- segment decoder/driver IC. This technique has two major advantages.
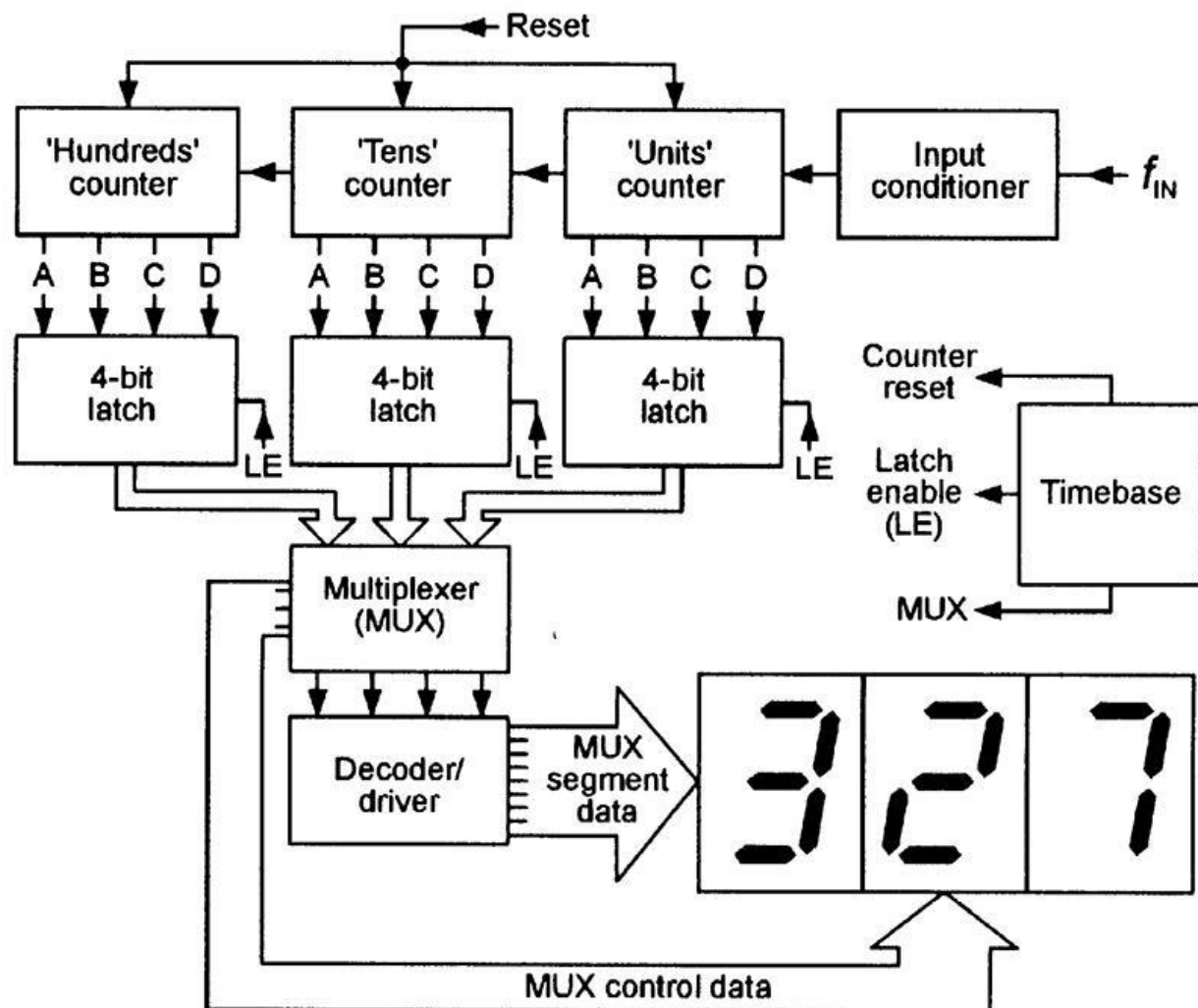
First, it calls for the use of only a single decoder/driver IC, irrespective of the number of readout digits used. Second, it calls for the use of a MUX incorporating only five ganged three-way sequencing switches (one for the control data and four for the BCD data), rather than the eight ganged three-way switches (one for the control data and seven for the segment data) called for in the **Figure 14** system.

In practice, all of the counting, latching, multiplexing, decoding, timing, and display-driving circuitry of **Figure 15** (and a great deal more) can easily be incorporated in a single LSI (large scale integration) chip that needs only 20 or so pins to make all necessary connections to the power supply, displays, and inputs, etc. Thus, a complete four-digit counter can be implemented using a dedicated IC in a circuit such as that shown in **Figure 16**, or a 3 1/2-digit DVM (digital voltmeter) can be implemented using a circuit such as that shown in **Figure 17**.
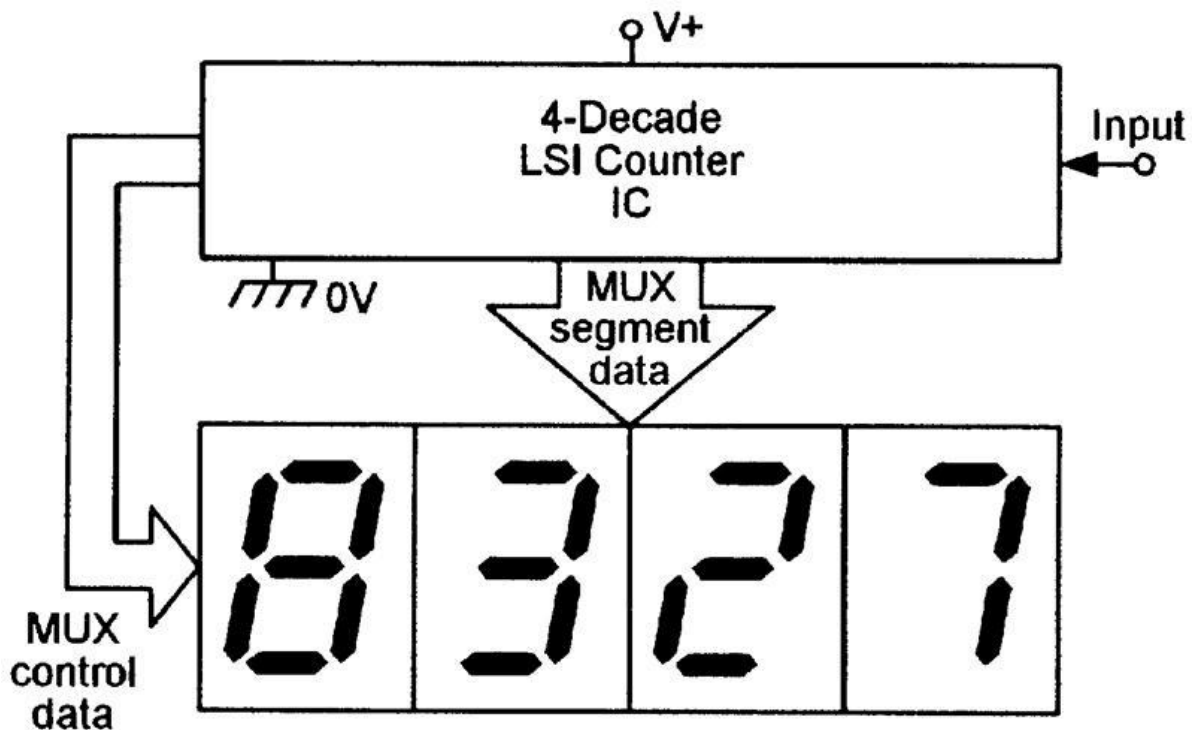
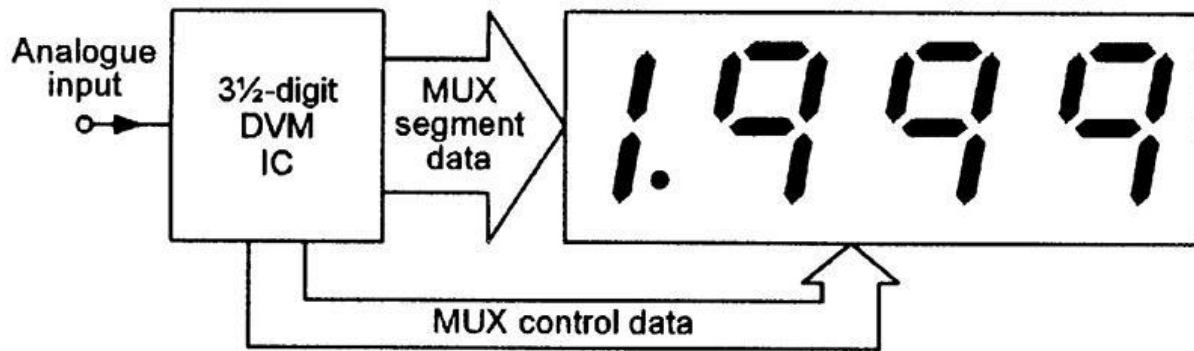**FIGURE 16.** A four-digit counter circuit, using a LSI chip.

FIGURE 17. A 3 1/2-digit DVM using a LSI chip.

RIPPLE BLANKING

If the basic four-digit **Figure 16** circuit is used to measure a count of 27, it will actually give a reading of 0027, unless steps are taken to provide automatic suppression of the two (unwanted) leading zeros. Similarly, if the 3 1/2-digit circuit of **Figure 17** is used to measure 0.1 volts, it will actually give a display of 0.100 volts, unless steps are taken to provide automatic suppression of the two (unwanted) trailing zeros.

In practice, automatic blanking of leading and/or trailing zeros can be obtained by using a ripple blanking technique, as illustrated in **Figures 18** and **19**. In these diagrams, each decoder/driver IC has a BCD input and a seven-segment output, and is provided with ripple blanking input (RBI) and output (RBO) terminals. If these terminals are active high, they will have the following characteristics.

If the RBI terminal is held low (at logic-0), the seven-segment outputs of the IC are enabled but the RBO terminal is disabled (held low). If the RBI terminal is biased high (at logic-1), the seven-segment outputs become disabled in the presence of a BCD '0000' input (= decimal zero), and the RBO output goes high under the same condition.

Thus, the RBO terminal is normally low and goes high only if a BCD '0000' input is present at the same time as the RBI terminal is high. With these characteristics in mind, refer now to **Figures 18** and **19**.

Figure 18 shows the ripple blanking technique used to provide leading-zero suppression in a four-digit display that is reading a count of 207. Here, the RBI input of the thousands or most significant digit (MSD) decoder/driver is tied high, so this display is automatically blanked in the presence of a zero, under which condition the RBO terminal is high.
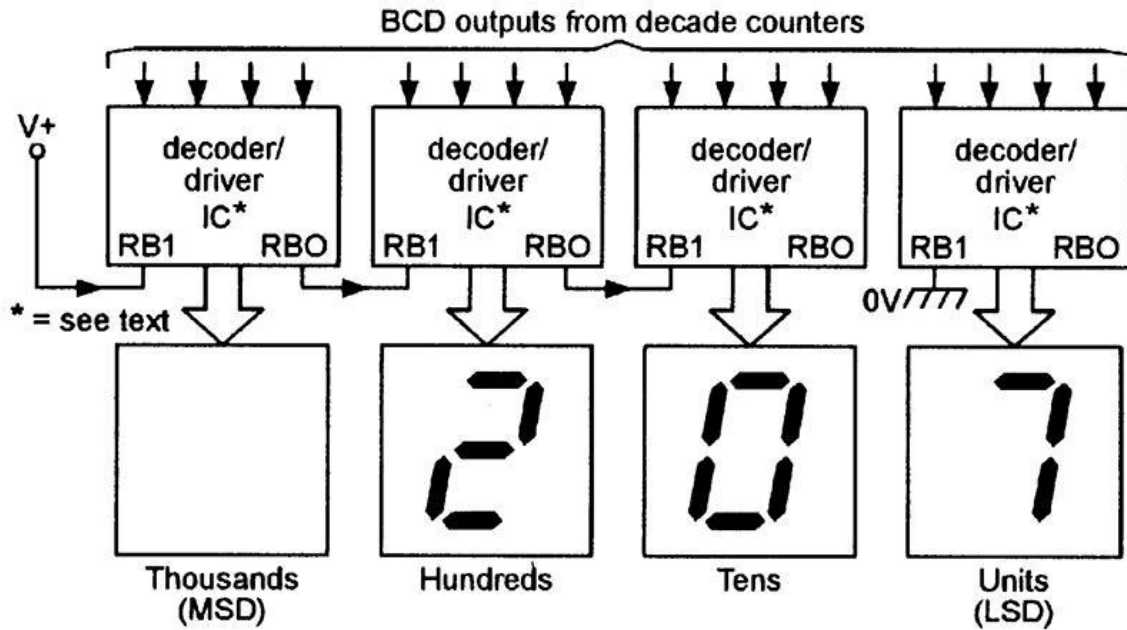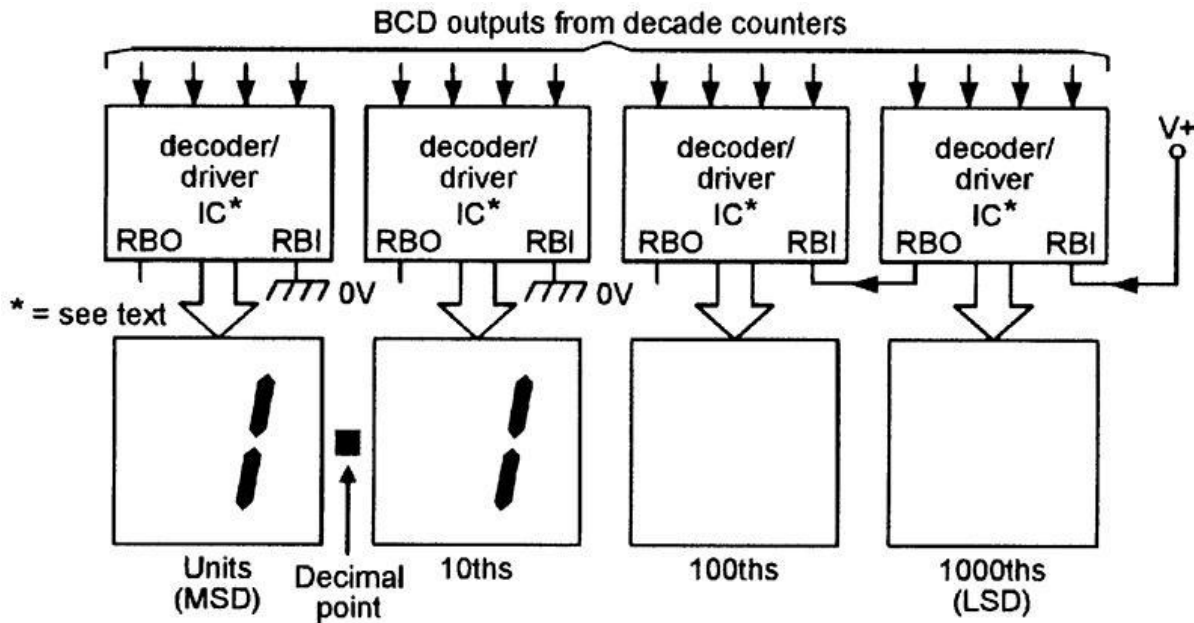
FIGURE 18. Ripple-blanking used to give leading-zero suppression in a four-digit counter.


Consequently, the RBI terminal of the hundreds IC is high, so its display reads 2, and the RBO terminal is low. The RBI input of the tens unit is thus also low, so its display reads 0 and its RBO output is low. The least significant digit (LSD) is that of the units readout, and this does not require zero suppression; consequently, its RBI input is grounded and it reads 7. The display thus gives a total reading of 207.

Note in the **Figure 18** leading zero suppression circuit that ripple blanking feedback is applied backwards, from the MSD to the LSD. **Figure 19** shows how trailing zero suppression can be obtained by reversing the direction of feedback, from the LSD to the MSD. Thus, when an input of 1.1 volts is fed to this circuit, the LSD is blanked, since its BCD input is '0000' and its RBI input is high. Its RBO terminal is high under this condition, so the 100ths digit is also blanked in the presence of a '0000' BCD input.

FIGURE 19. Ripple-blanking used to give trailing-zero suppression of the last two digits of a 3 1/2-digit DVM readout.

Practical decoder/driver ICs are often (but not always) provided with ripple blanking input and output terminals; often, these are active low. If a decoder/driver IC does not incorporate integral ripple blanking logic, it can usually be obtained by adding external logic similar to that shown in **Figure 20**, with the RBO terminal connected to the BLANKING input pin of the decoder/driver IC.
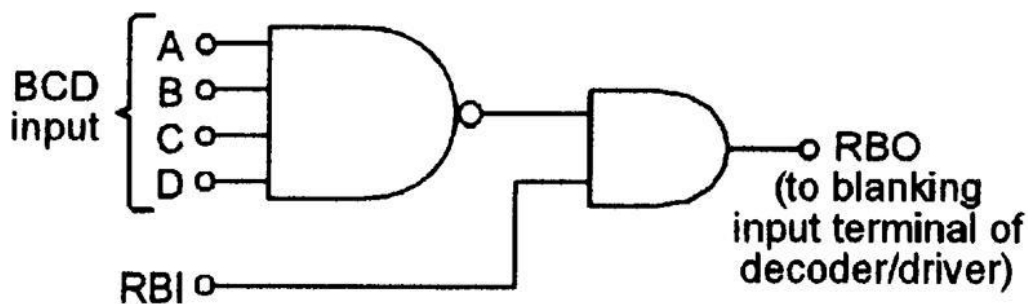
FIGURE 20. DIY ripple-blanking logic (active-high type).

In **Figure 20** (an active high circuit), the output of the four-input NOR gate goes high only in the presence of a '0000' BCD input, and the RBO output goes high only if the decimal zero input is present while RBI is high.

The next *and last* episode of this two-part feature will describe practical seven-segment decoder/driver ICs and circuits. **NV**

USING SEVEN-SEGMENT DISPLAYS — PART 2

By Ray Marston

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The opening episode of this special feature explained the basic operating and usage principles of seven-segment alphanumeric displays.

This concluding episode deals with practical seven-segment decoder/driver ICs.

PRACTICAL DECODER/DRIVER ICS

Decoder/driver ICs are available in both TTL and CMOS forms. Some of these devices have integral ripple-blanking facilities, others have built-in data latches, and a few even have built-in decade counter stages, etc. The rest of this article describes a few of the most popular of these devices.

The 74LS47 and 74LS48
These seven-segment decoder/driver ICs are members of the LS TTL family. They have integral ripple-blanking facilities, but do not incorporate data latches. **Figure 1** shows the functional diagrams and pin designations of these devices, each of which is housed in a 16-pin DIL package.
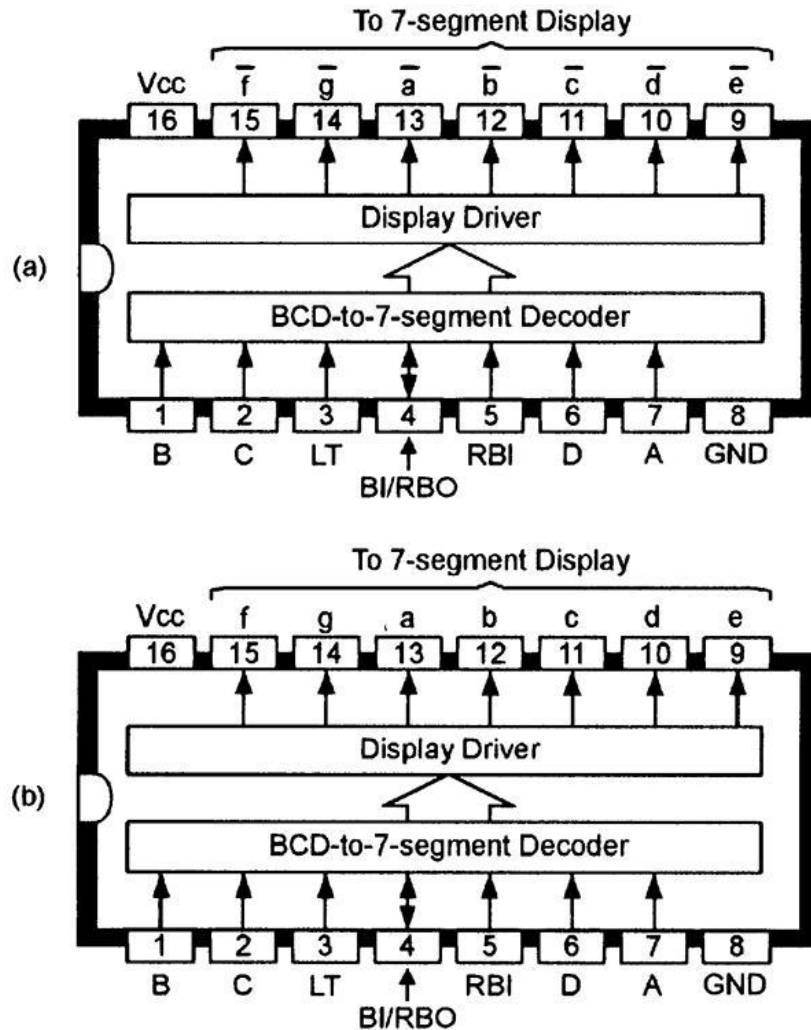
FIGURE 1. Functional diagram of the **(a)** 74LS47 and **(b)** 74LS48 BCD-to-seven-segment decoder/driver ICs.

The 74LS47 has active-low outputs designed for driving a common-anode LED display via external current-limiting resistors (Rx), as shown in **Figure 2**.
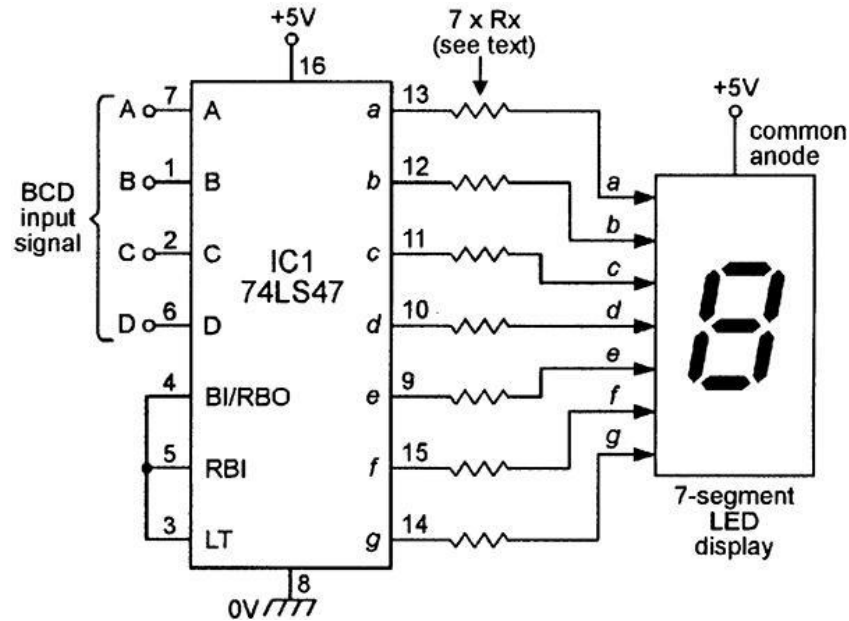
FIGURE 2. Basic way of using a 74LS47 IC to drive a common-anode LED display.

The 74LS48 has active-high outputs designed for driving a common-cathode LED display in a manner similar to that of **Figure 2**, but with the display's common terminal taken to ground. The Rx resistors must limit the segment currents to less than 24mA in the 74LS47, and less than 6mA in the 74LS48. The 74LS48 can be used to drive a seven-segment LCD display by using the connections already shown in *last month's* **Figure 11**.

Note from **Figure 1** that each of these ICs has three input 'control' terminals, these being designated LT (Lamp Test), BI/RBO, and RBI. The LT terminal drives all display outputs on when the terminal is driven to logic 0 with the RBO terminal open or at logic 1.

When the BI/RBO terminal is pulled low, all outputs are blanked; this pin also functions as a ripple-blanking output terminal. **Figure 3** shows how to connect the ripple-blanking terminals to give leading zero suppression on the first three digits of a four-digit display.
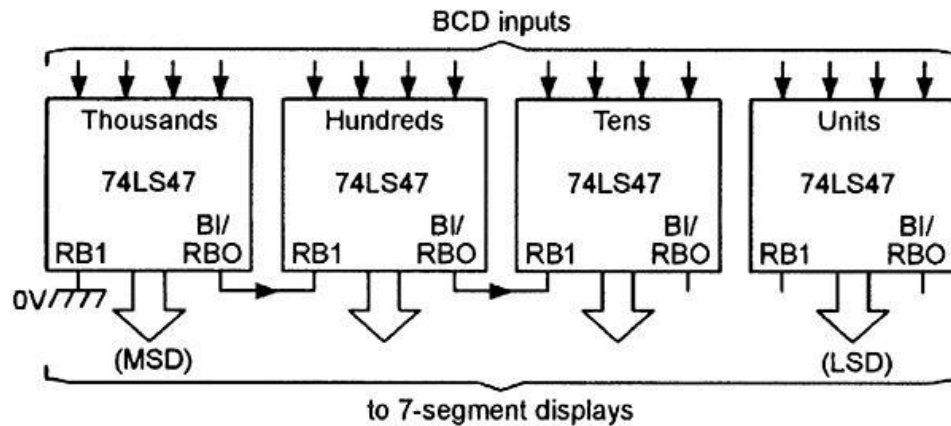
FIGURE 3. Method of applying leading-zero suppression to the first three digits of a four-digit display using 74LS47 ICs.

The 4511B

The most popular CMOS 4000B-series BCD-to-seven-segment LED-driving IC is the 4511B (also available as the 74HC4511), which has an integral four-bit data latch, but has no built-in ripple-blanking facilities.

Figure 4 shows the functional diagram and pin notations of the device, which can use any power source in the 5V to 15V range. The IC is ideally suited to driving common cathode LED displays, and uses NPN bipolar output transistor stages that can each source up to 25mA.
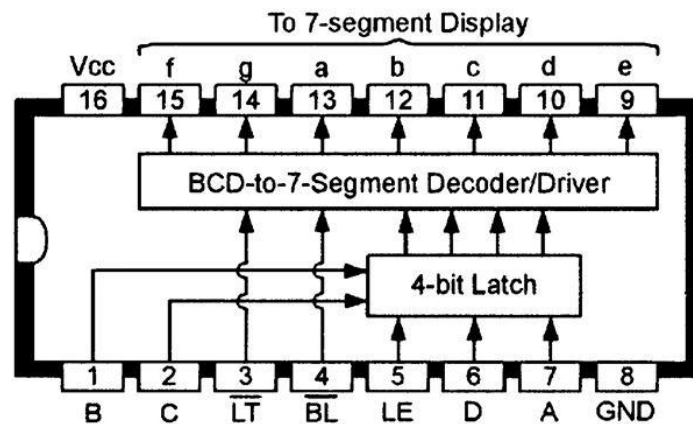
FIGURE 4. Functional diagram and pin notations of the 4511B seven-segment latch/decoder/LED-driver IC.

The 4511B is very easy to use, and has only three input control terminals; of these, the not-LT (pin 3) pin is normally tied high, but turns on all seven segments of the display when pulled low.

The not-BL (pin 4) terminal is also normally tied high, but blanks (turns off) all seven segments when pulled low.

Finally, the LE (latch enable) terminal (pin 5) enables the IC to give either direct or latched decoding operation. When LE is low, the IC gives direct decoding operation, but when LE is taken high, it freezes the display.

The 4511B can be used to drive most popular types of seven-segment displays. **Figure 5** shows the basic connections for driving a common-cathode LED display.
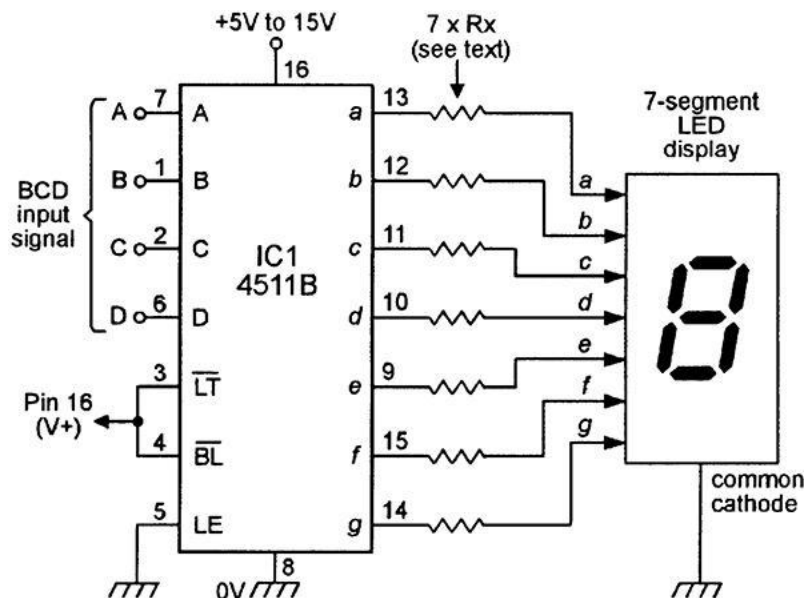
FIGURE 5. Basic way of using the 4511B to drive a seven-segment common-cathode LED display.

A current-limiting resistor (Rx) must be wired in series with each display segment and must have its value chosen to limit the segment current below 25mA.

Figures 6, 7, and **8** show how to modify the above circuit to drive LED common-anode displays, gas discharge displays, and low-brightness fluorescent displays, respectively.
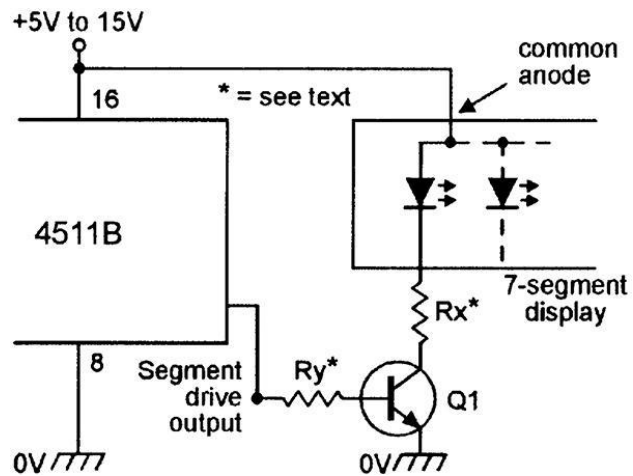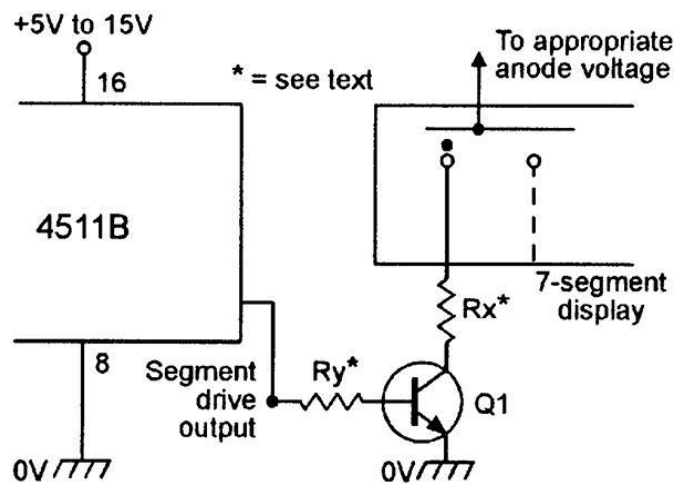
FIGURE 6. Driving a common-anode LED display.

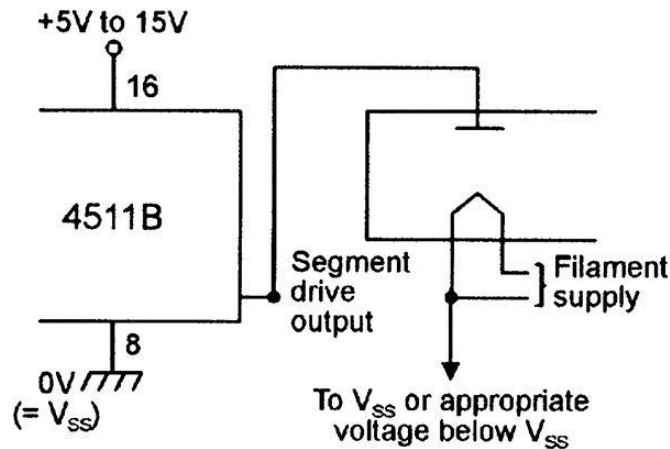**FIGURE 7.** Driving a gas discharge readout.

**FIGURE 8.** Driving a low-brightness fluorescent readout.

Note in the cases of **Figures 6** and **7** that an NPN buffer transistor must be interposed between each output drive segment and the input segment of the display.

In each case, Rx determines the operating segment current of the display, and Ry determines the base current of the transistor.

The 4511B can also be used to drive seven-segment liquid-crystal displays by using an external squarewave 'phase' signal and a set of EX-OR gates in a configuration similar to that of *last month's* **Figure 11**. In practice, however, it is far better to use a 4543B IC for this particular application.

The 4543B

The most popular 4000B-series BCD-to-seven-segment LCD-driving IC is the 4543B (also available as the 74HC4543), which has a built-in data latch. **Figure 9** shows the IC's functional diagram and pin notations.
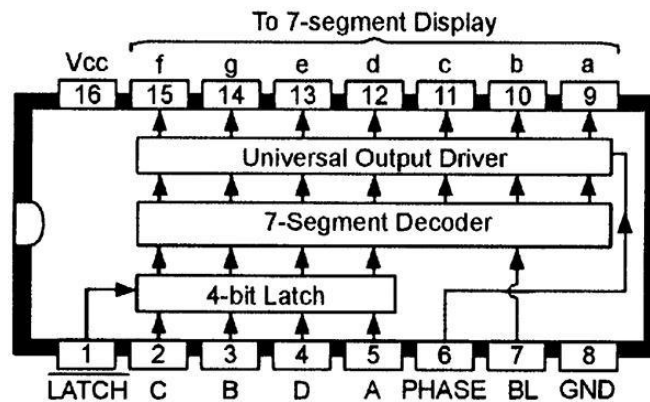

The device incorporates an EX-OR array (of the type shown in *last month's* **Figure 11**) in its output driver network, which can source or sink several milliamps of output current. This feature enables the IC to act as a universal unit that can drive common-cathode or common-anode LED or liquid-crystal seven-segment displays with equal ease, as shown in **Figures 10** to **13**.

The 4543B has three input control terminals, these being designated not-LATCH, PHASE, and BL (BLANK). In normal use, the not-LATCH terminal is biased high and the BL terminal is tied low. The state of the PHASE terminal depends on the type of display that is being driven. For driving LCD readouts, a squarewave (roughly 50Hz, swinging fully between the GND and Vcc values) must be applied to the PHASE terminal. For driving common-cathode LED displays, PHASE must be grounded. For driving common-anode displays, PHASE must be tied to logic high.

The display can be blanked at any time by driving the BL terminal to the logic-1 level. When the not-LATCH terminal is in its normal high (logic-1) state, BCD inputs are decoded and fed directly to the seven-segment output terminals of the IC. When the not-LATCH terminal is pulled low, the BCD input signals that are present at the moment of transition are latched into memory and fed (in decoded form) to the seven-segment outputs until the not-LATCH pin returns to the high state.

Figure 10 shows basic ways of using the 4543B to drive common-cathode and common-anode seven-segment LED displays; the 'R' resistance value must limit the output drive current to below 10mA per segment.
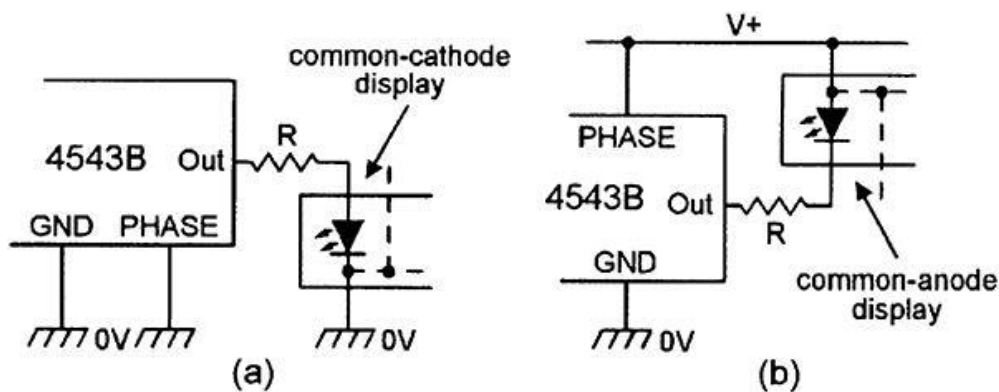
FIGURE 10. Way of using the 4543B to drive **(a)** common-cathode or **(b)** common-anode seven-segment LED displays.

Figure 11 shows the basic way of using the 4543B to drive a seven-segment LCD, and **Figures 12** and **13** show it used to drive other types of seven-segment displays. In **Figure 12**, Rx sets the segment current of the display and Ry sets the base current of the transistor (10mA maximum).
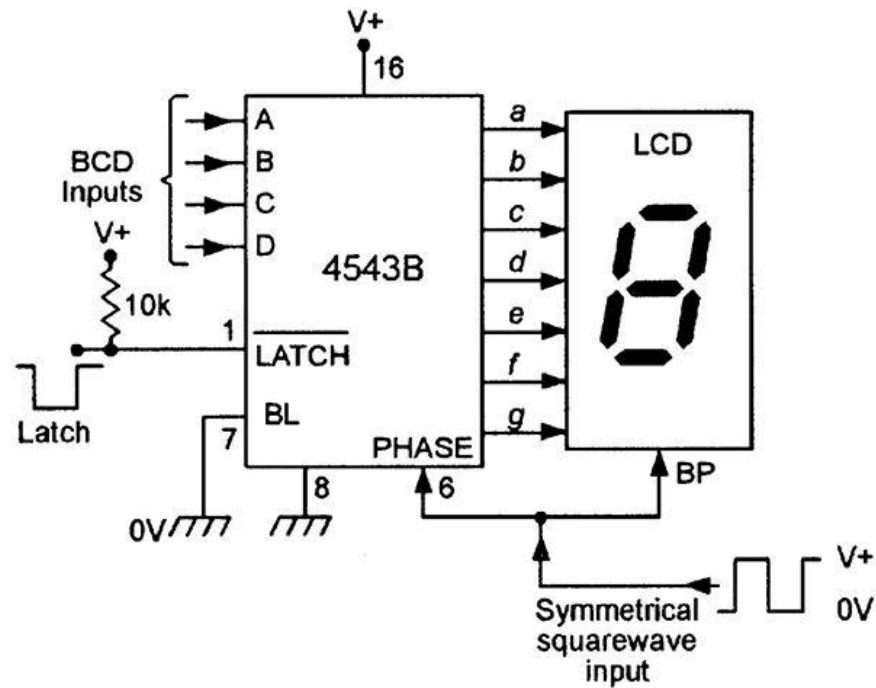
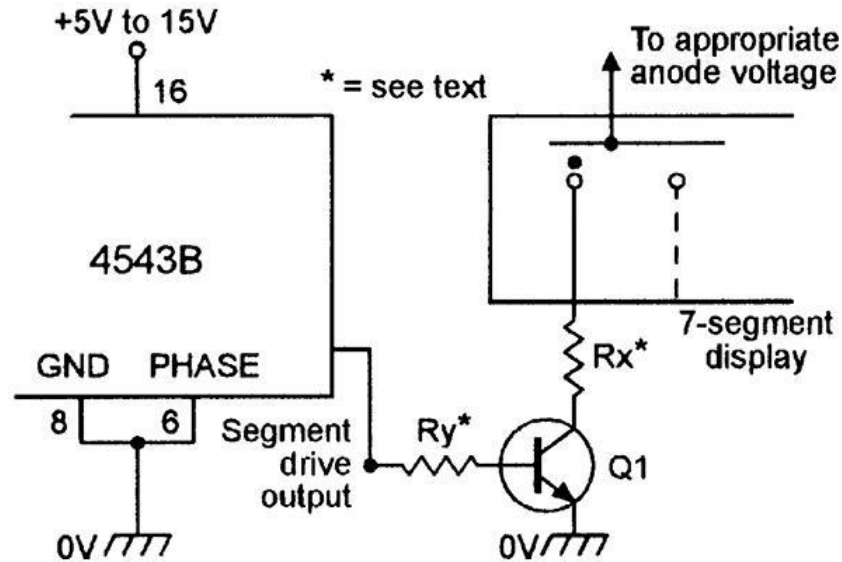**FIGURE 11.** Way of using the 4543B to drive a seven-segment LCD.
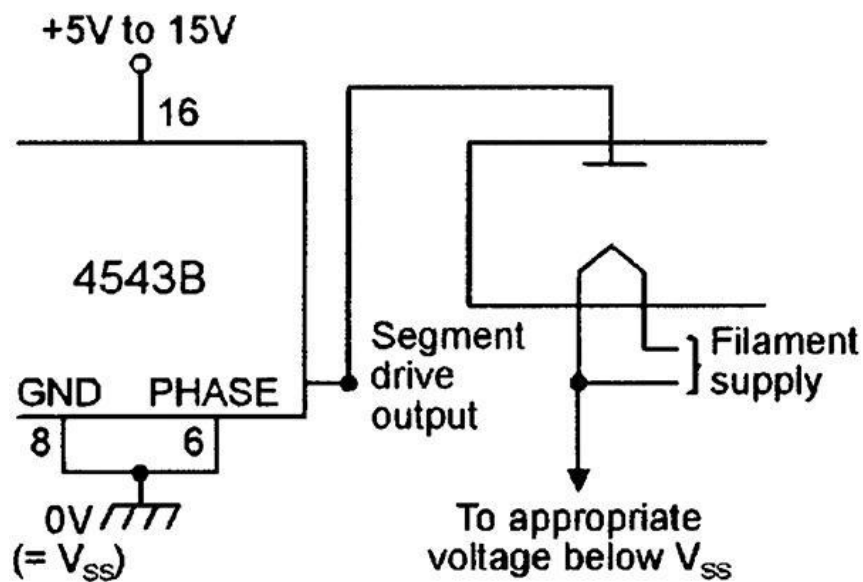
FIGURE 12. Driving a gas discharge readout with a 4543B.

FIGURE 13. Driving a fluorescent readout with a 4543B.

The 4026B

The 4026B IC is a complete decade counter with integral decoder/driver circuitry that can directly drive a seven-segment common-cathode LED display. The segment output currents are internally limited to about 5mA at 10V or 10mA at 15V. Enabling the display can be connected directly to the outputs of the IC without the use of external current-limiting resistors. The IC

does not incorporate a data latch and has no facility for ripple blanking. **Figure 14** shows the functional diagram and pin notations of the 4026B.
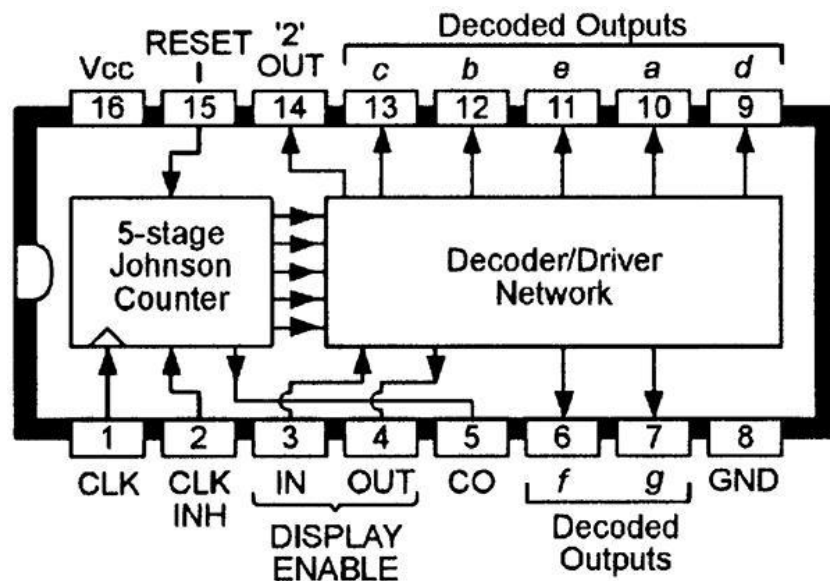
FIGURE 14. Functional diagram and pin notations of the 4026B decade counter with seven-segment display driver.

The 4026B has four input control terminals, and three auxiliary output terminals. The input terminals are designated CLK (CLOCK), CLK INH (CLOCK INHIBIT), RESET, and DISPLAY ENABLE IN. The IC incorporates a Schmitt Trigger on its CLK input line, and clock signals do not have to be pre-shaped. The counter is reset to zero by driving the RESET terminal high.

The CLK INH terminal must be grounded to allow normal counting operation. When CLK INH is high, the counters are inhibited. The display is blanked when the DISPLAY ENABLE IN terminal is grounded. The DISPLAY ENABLE IN terminal must be high for normal operation. Thus, in normal operation, the RESET and CLK INH terminals are grounded and the DISPLAY ENABLE IN terminal is held positive, as shown in **Figure 15**.
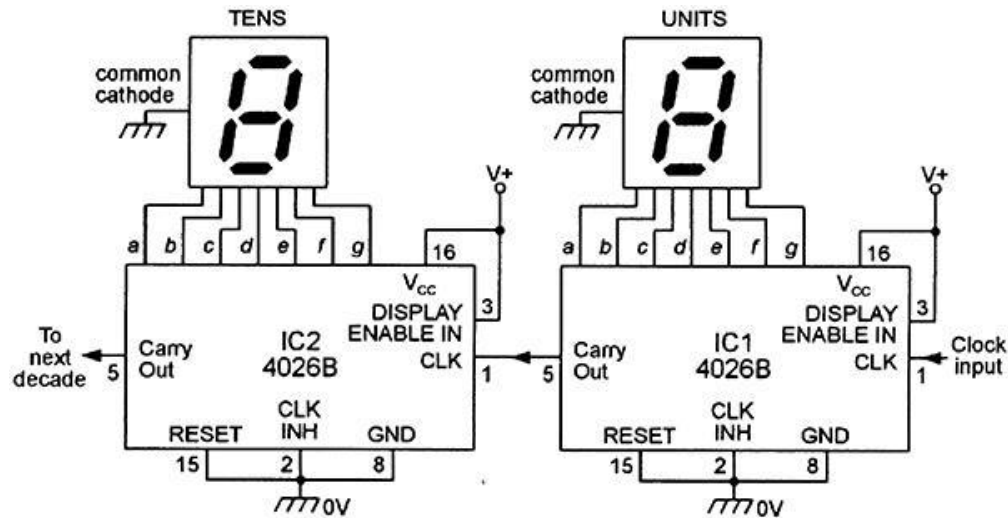
FIGURE 15. Basic method of cascading 4026B ICs.

The three auxiliary output terminals of the 4026B are designated DISPLAY ENABLE OUT, CO (CARRY OUT), and '2' OUT. The DISPLAY ENABLE OUT signal is a slightly delayed copy of the DISPLAY ENABLE IN input signal. The CO signal is a symmetrical square- wave at one-tenth of the CLK input frequency, and is useful in cascading 4026B counters. The '2' OUT terminal goes low only on a count of 2. **Figure 15** shows the basic circuit connections to be used when cascading stages.

The 4033B

This device (see **Figure 16**) can be regarded as a modified version of the 4026B, with the DISPLAY ENABLE IN and DISPLAY ENABLE OUT terminals eliminated and replaced by ripple blanking input (RBI) and output (RBO) terminals, and with the '2' OUT terminal replaced with a LT (LAMP TEST) terminal which activates all output segments when biased high.
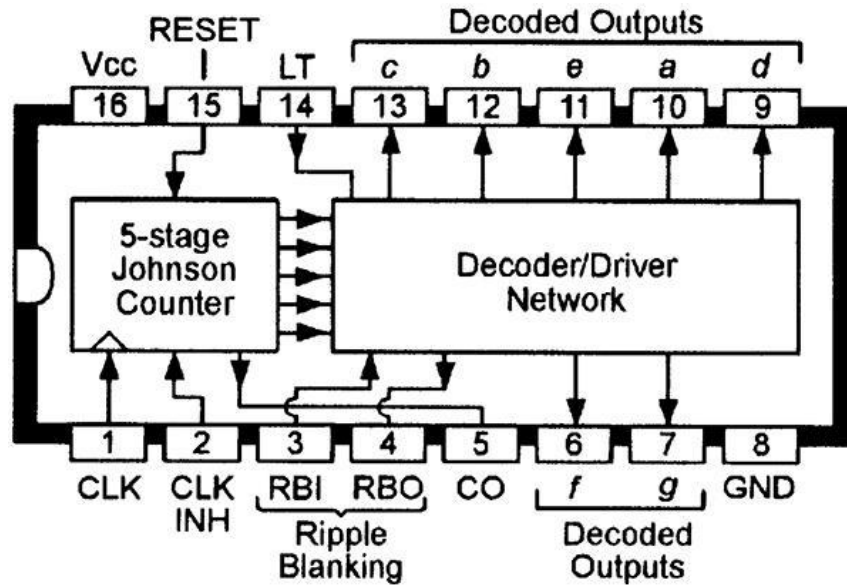
FIGURE 16. Functional diagram and pin notations of the 4033B decade counter with seven-segment display driver.

In normal use, the RESET, CLK INH, and LT terminals are all grounded and the RBI terminal is made positive, as shown in **Figure 17**. This configuration does not provide blanking of unwanted leading and/or trailing zeros.
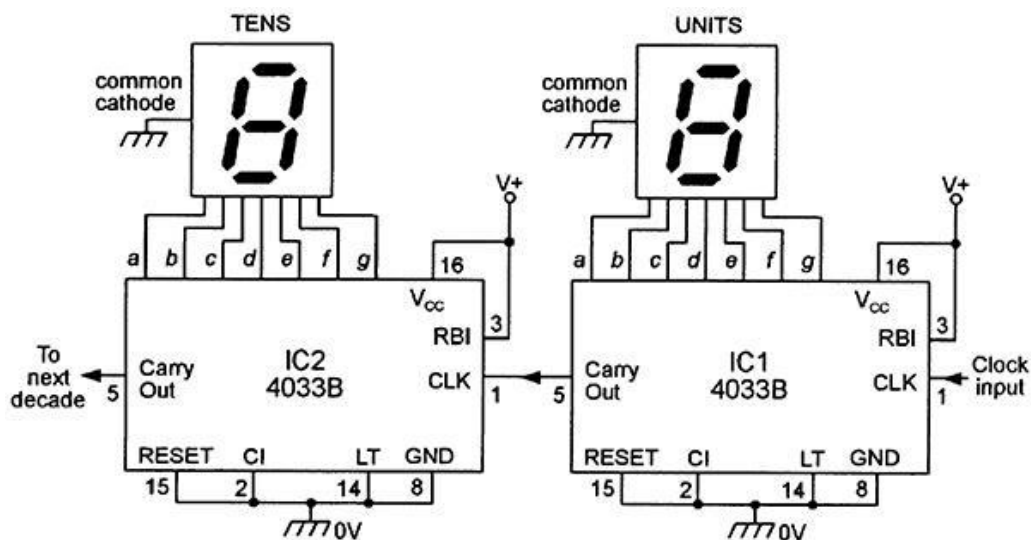

FIGURE 17. Basic method of cascading 4033B ICs (without zero suppression).

If cascaded 4033B ICs are required to give automatic leading-zero suppression, the basic **Figure 17** circuit must be modified as shown in **Figure 18** to provide ripple-blanking operation. Here, the RBI terminal of the most significant digit (MSD) is grounded, and its RBO terminal is connected to the RBI terminal of the next least-significant stage.
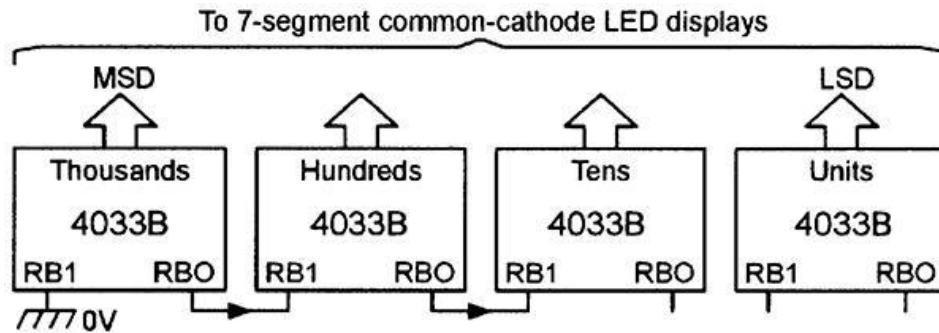
FIGURE 18. Method of modifying the Figure 17 circuit to give automatic leading-zero suppression.

This procedure is repeated on all except the LSD, which does not require zero suppression. If trailing-zero suppression is required, the direction of ripple-blanking feedback must be reversed with the RBI terminal of the LSD grounded and its RBO terminal wired to the RBI terminal of the next least-significant stage, and so on. **NV**