UMC

UM6845/A/B

CRT Controller

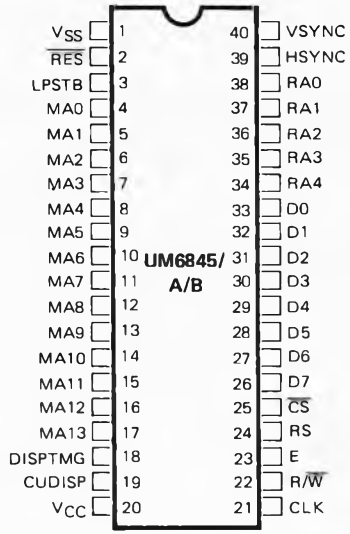
Features

- Applications including smart, programmable, intelligent CRT terminals; video games; information display
- Alphanumeric, semi-graphic, and full graphic capabilities
- Fully programmable via processor data bus with timing generation for almost any alphanumeric screen density
- Single +5 volt supply; TTL compatible I/O; NMOS technology
- Hardware scrolling by page, line, or character
- Provides CPUs with synchronous signals to external device
- Programmable cursor format
- Light pen registers and input strobe signal to latch light pen position on screen
- Operates without line buffer or external DMA; reading screen memory mutliplexed between CRTC and CPU
- Programmable interlace or non-interlace scan
- 14-bit display memory reading address width

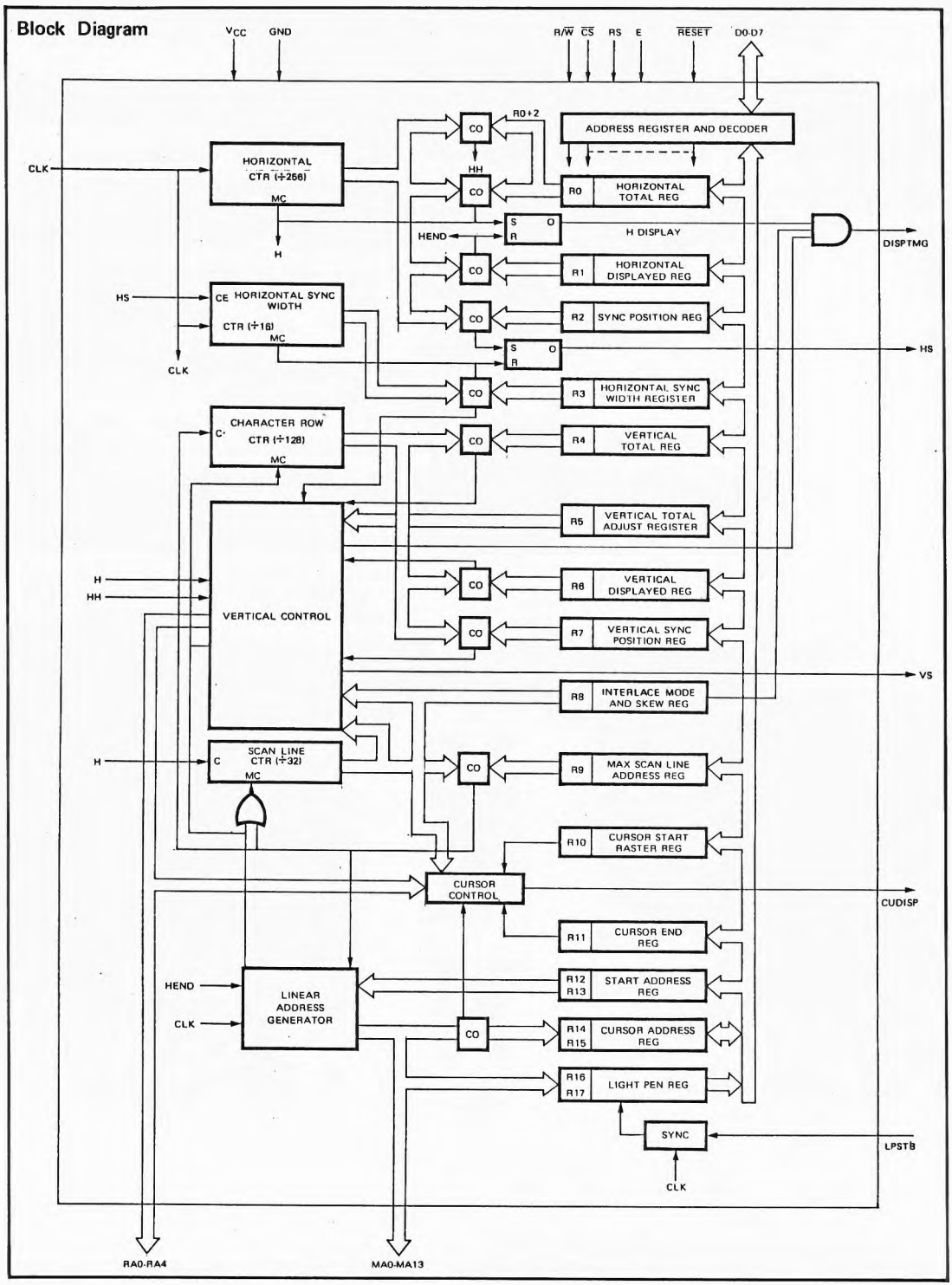
General Description

The CRTC UM6845/A/B comprises LSI controllers designed to provide interface between microcomputers and raster-scan-type CRT displays. The CRTC belongs to the MC6800 LSI family and is fully compatible with CPUs in both data lines and control lines. Its primary function is to generate timing signals which are necessary for raster-scan type CRT displays according to the specifications programmed by the CPU.

Pin Configuration



Block Diagram



Absolute Maximum Ratings *

Supply Voltage, V_{CC}** . . . . . −0.3~+7.0V
Input Voltage, V_{IN}** . . . . . −0.3~+7.0V
Operating Temperature, T_{OPR} . . . . . 0°~70°C
Storage Temperature, T_{STG} . . . . . −55°~+150°C

**With respect to V_{SS} (SYSTEM GND)

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics

(V_{CC} = 5V)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	–	4.75	5.0	5.25	V
Input Voltage	V_{IL}	–	−0.3	–	0.8	V
	V_{IH}	–	2.0	–	V_{CC}	V
Input Leakage Current	I_{IN}	V_{IN} = 0 – 5.25V (Except D0 – D7)	−2.5	–	2.5	μA
Three-State Input Current (Off-State)	I_{TSI}	V_{IN} = 0.4 – 2.4V, V_{CC} = 5.25V (D0 – D7)	−10	–	10	μA
Output "High" Voltage	V_{OH}	I_{LOAD} = 205A (D0 – D7)	2.4	–	–	V
		I_{LOAD} = −100μA (Other Outputs)				
Output "Low" Voltage	V_{OL}	I_{LOAD} = 1.6mA	–	–	0.4	V
Input Capacitance	C_{IN}	V_{IN} = 0, T_A = 25°C, F = 1.0 MHz; D0 – D7	–	–	12.5	pF
		V_{IN} = 0, T_A = 25°C, F = 1.0 MHz; Other Inputs	–	–	10.0	pF
Output Capacitance	C_{OUT}	V_{IN} = 0V, T_A = 25°C, f = 1.0 MHz	–	–	10.0	pF
Power Dissipation	P_D	T_A = 25°C, V_{CC} = 5.0V	–	–	1000	mW

A.C. Characteristics

(V_{CC} = 5V ± 5%, T_A = 0°C ~ 70°C)

BUS TIMING CHARACTERISTIC

MPU READ TIMING*

Item	Symbol	UM6845			UM6845A			UM6845B			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Enable Cycle Time	$t_{cyc}E$	1.0	–	–	0.666	–	–	0.5	–	–	μs
Enable "High" Pulse Width	PW_{EH}	0.45	–	–	0.280	–	–	0.22	–	–	μs
Enable "Low" Pulse Width	PW_{EL}	0.40	–	–	0.280	–	–	0.21	–	–	μs
Enable Rise and Fall Time	t_{Er}, t_{Ef}	–	–	25	–	–	25	–	–	25	μs
Address Set-up Time	t_{AS}	140	–	–	140	–	–	70	–	–	ns
Data Delay Time	t_{DDR}	–	–	320	–	–	200	–	–	180	ns
Data Hold Time	t_H	10	–	–	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	10	–	–	10	–	–	ns
Data Access Time	t_{ACC}	–	–	460	–	–	360	–	–	250	ns

* See Fig. 1

MPU WRITE TIMING*

Item	Symbol	UM6845			UM6845A			UM6845B			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Enable Cycle Time	$t_{cyc}E$	1.0	–	–	0.666	–	–	0.5	–	–	μs
Enable "High" Pulse Width	PW_{EH}	0.45	–	–	0.280	–	–	0.22	–	–	μs
Enable "Low" Pulse Width	PW_{EL}	0.40	–	–	0.280	–	–	0.21	–	–	μs
Enable Rise and Fall Time	t_{Er}, t_{Ef}	–	–	25	–	–	25	–	–	25	ns
Address Set-up Time	t_{AS}	140	–	–	140	–	–	70	–	–	ns
Data Set-up Time	t_{DSW}	195	–	–	80	–	–	60	–	–	ns
Data Hold Time	t_H	10	–	–	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	10	–	–	10	–	–	ns

* See Fig. 2

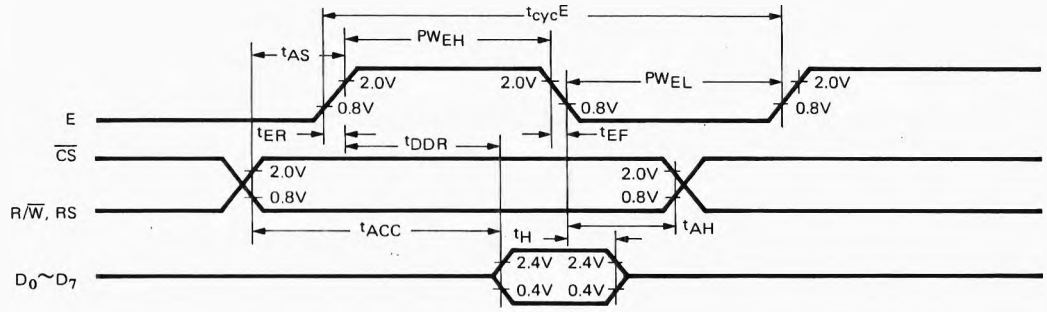


Figure 1. Read Sequence

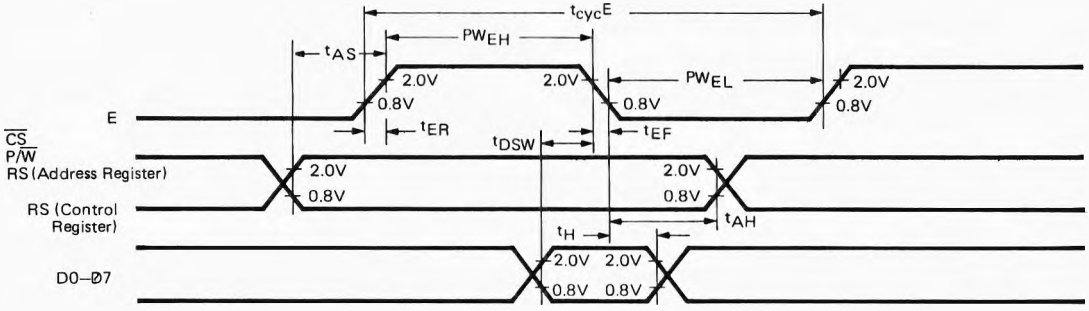


Figure 2. Write Sequence

CRTC SIGNAL TIMING*

Item	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	$t_{cyc}C$	270	–	–	ns
Clock "High" Pulse Width	PW_{CH}	130	–	–	ns
Clock "Low" Pulse Width	PW_{CL}	130	–	–	ns
Rise and Fall Time for Clock Input	t_{Cr}, t_{Cf}	–	–	20	ns
Memory Address Delay Time	t_{MAD}	–	–	160	ns
Raster Address Delay Time	t_{RAD}	–	–	160	ns
DISPTMG Delay Time	t_{DTD}	–	–	250	ns
CUDISP Delay Time	t_{CDD}	–	–	250	ns
Horizontal Sync Delay Time	t_{HSD}	–	–	200	ns
Vertical Sync Delay Time	t_{VSD}	–	–	250	ns
Light Pen Strobe Pulse Width	PW_{LPH}	60	–	–	ns
Light Pen Strobe	t_{LPD1}	–	–	70	ns
Uncertain Time of Acceptance	t_{LPD2}	–	–	0	ns

* See Fig. 3; Fig. 4

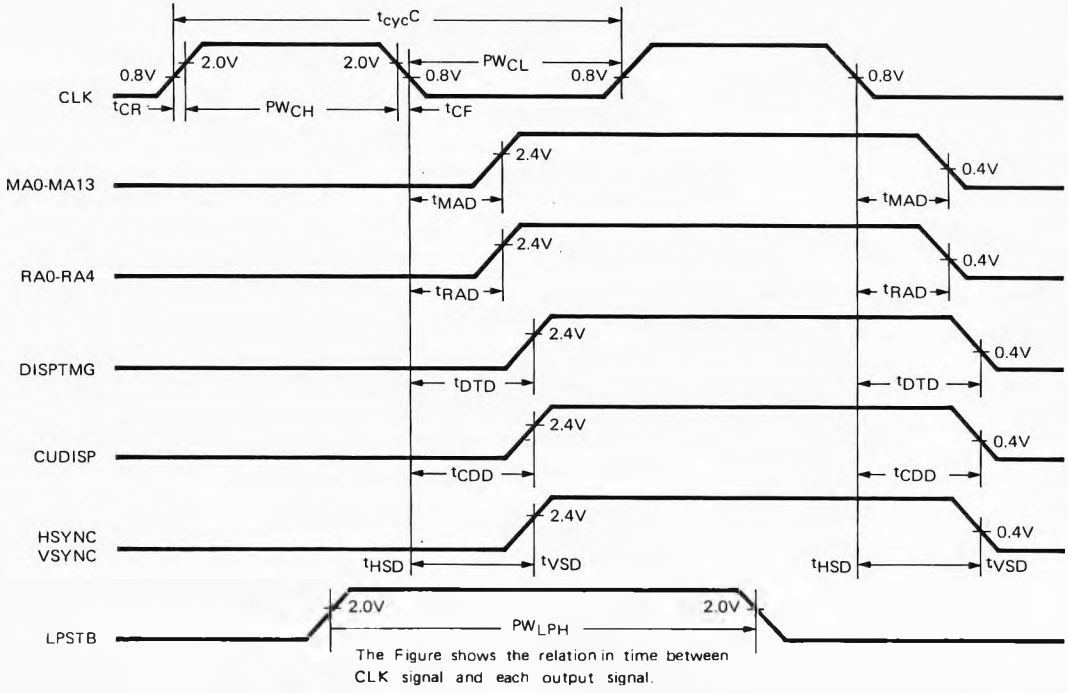


Figure 3. CRTC Timing Chart

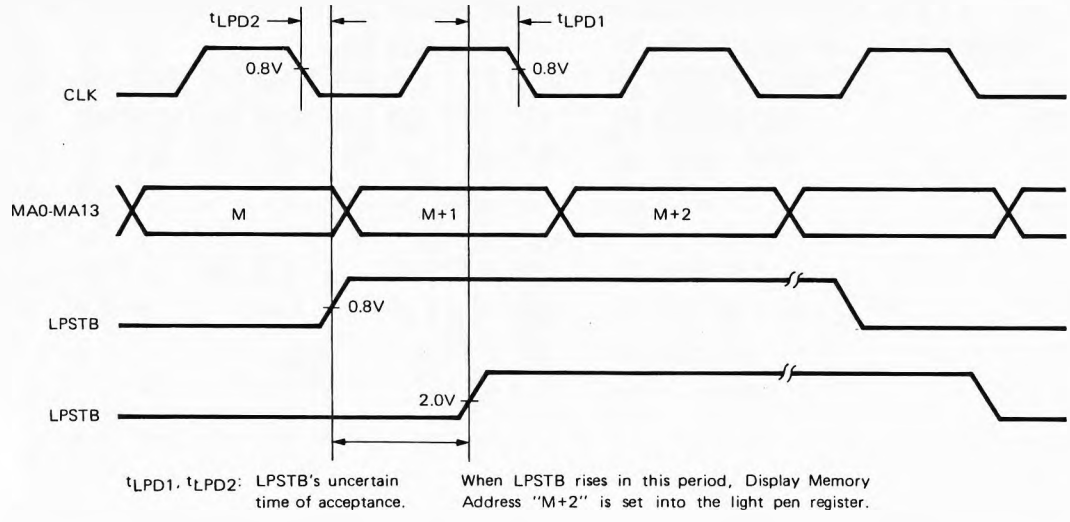


Figure 4. LPSTB Input Timing & Display Memory Address is Set Into the Light Pen Register.

Typical CRT Controller Application Block Diagram

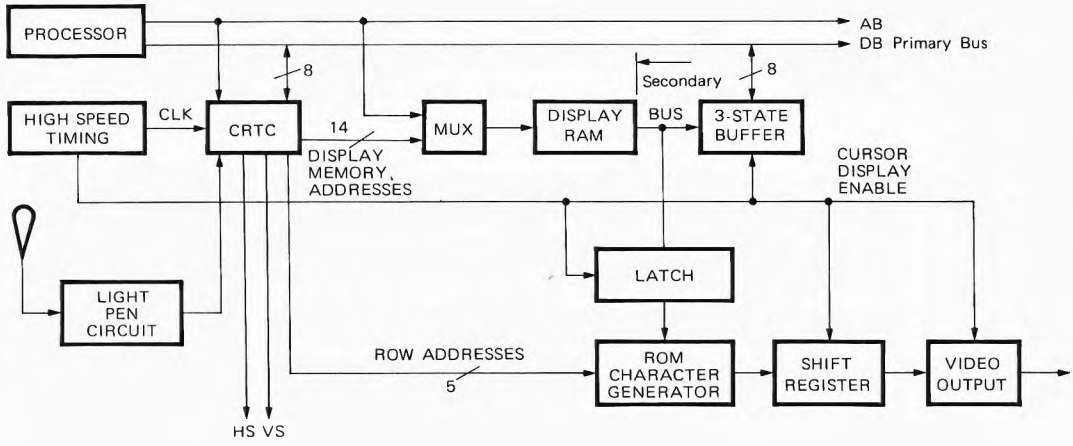


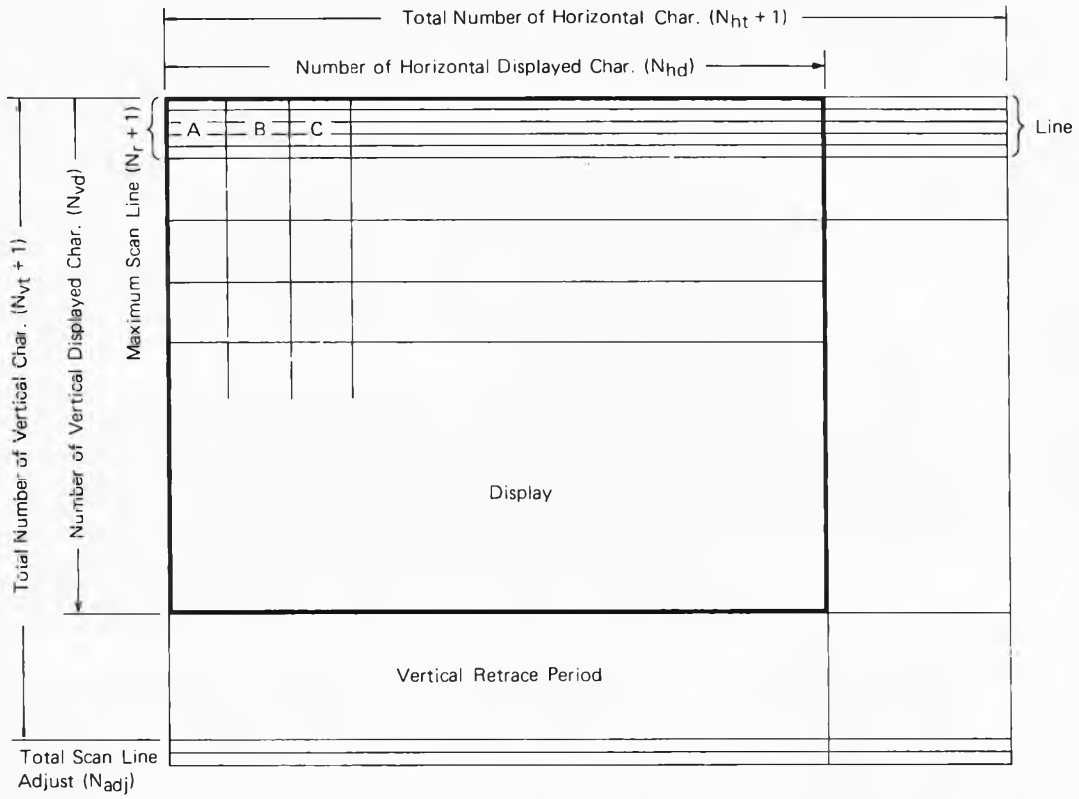
Figure 5. Typical CRT Controller Application

CRT Screen Format and Time Chart

REGISTER PROGRAMMED VALUES

Register	Register Name	Specified Value	Programmed (Written) Value
R0	Horizontal Total	$N_{ht}+1$	N_{ht}
R1	Horizontal Displayed	N_{hd}	N_{hd}
R2	Horizontal Sync Position	$N_{hsp}+1$	N_{hsp}
R3	Sync Width	N_{vsw}, N_{hsw}	N_{vsw}, N_{hsw}
R4	Vertical Total	$N_{vt}+1$	N_{vt}
R5	Vertical Total Adjust	N_{adj}	N_{adj}
R6	Vertical Displayed	N_{vd}	N_{vd}
R7	Vertical Sync Position	$N_{vsp}+1$	N_{vsp}
R8	Interlace & Skew		
R9	Maximum Raster Address	N_r+1/N_r+2	N_r
R10	Cursor Start Raster	N_{CSTART}	
R11	Cursor End Raster	N_{CEND}	
R12	Start Address (H)	0	
R13	Start Address (L)	0	
R14	Cursor (H)		
R15	Cursor (L)		
R16	Light Pen (H)		
R17	Light Pen L (L)		

SCREEN FORMAT



RESTRICTIONS ON PROGRAMMING INTERNAL REGISTER

(1) $0 < N_{hd} < N_{ht} + 1 \leqslant 256$

(2) $0 < N_{vd} < N_{vt} + 1 \leqslant 128$

(3) $0 \leqslant N_{hsp} \leqslant N_{ht}$

(4) $0 \leqslant N_{vsp} \leqslant N_{vt}$

(5) $0 \leqslant N_{CSTART} \leqslant N_{CEND} \leqslant N_r$ (Non-Interlace, Interlace Sync Modes)

$0 \leqslant N_{CSTART} \leqslant N_{CEND} \leqslant N_r + 1$ (Interlace Sync & Video Modes)

(6) $2 \leqslant N_r \leqslant 30$

(7) $3 \leqslant N_{ht}$ (Except Non-Interlace Mode)

$5 \leqslant N_{ht}$ (Non-Interlace Mode Only)

CRTC ADDRESSING FOR READING DISPLAY MEMORY

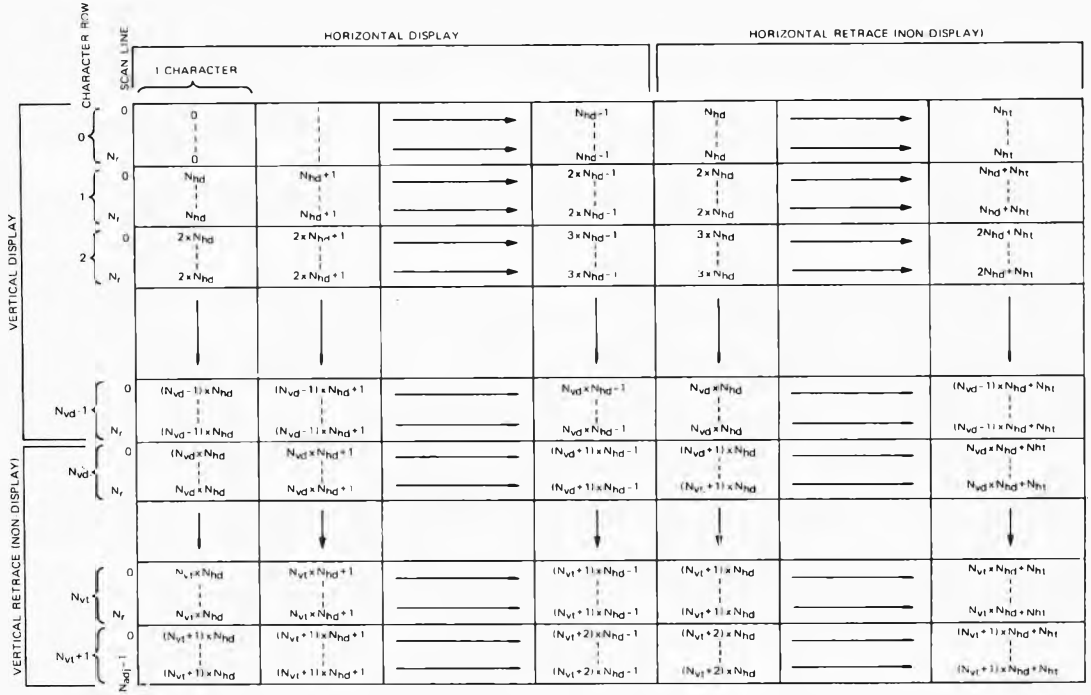


Figure 6. Display Memory Addressing (MA0-MA13) Stage Chart

Note: The initial MA is determined by the contents of state address register R12/R13. Timing is shown for R12/R13 = 0. Only Non-Interlace-and Interlace Sync Modes are shown.

CRTC HORIZONTAL TIMING

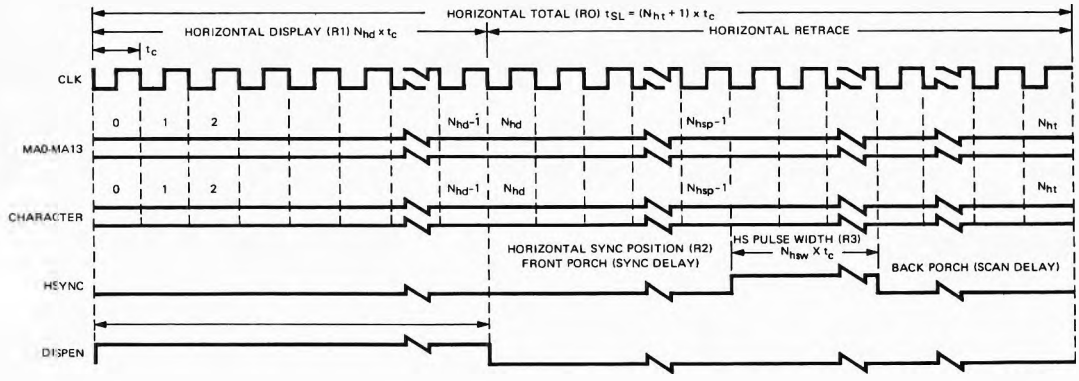


Figure 7. CRTC Horizontal Timing

CRTC VERTICAL TIMING

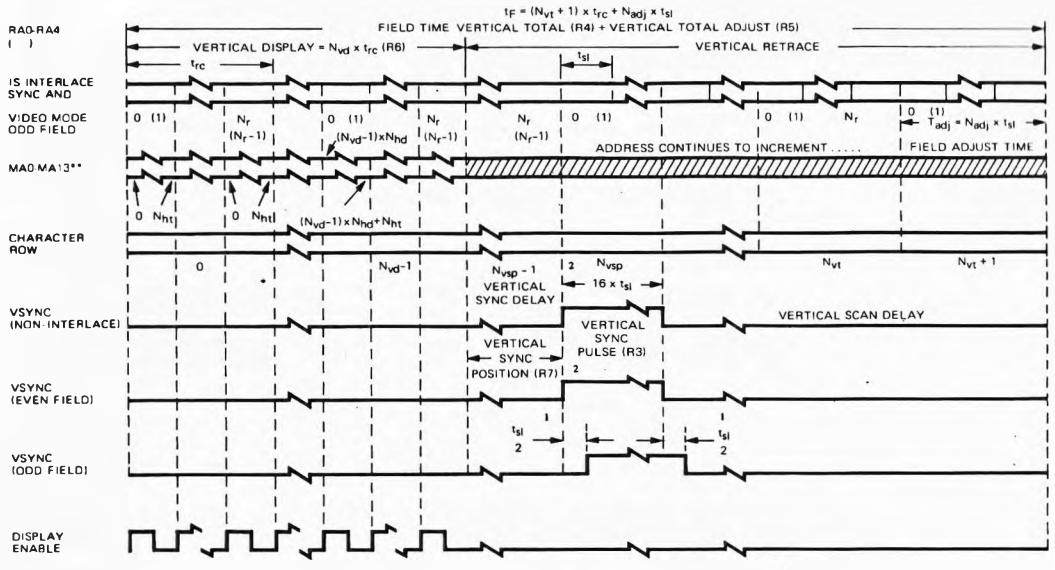


Figure 8. CRTC Vertical Timing

Notes: 1. The odd field is offset ½ horizontal scan time.

2. Vertical sync pulse may be programmed from 1 to 16 scan line times.

CURSOR DISPLAY TIMING

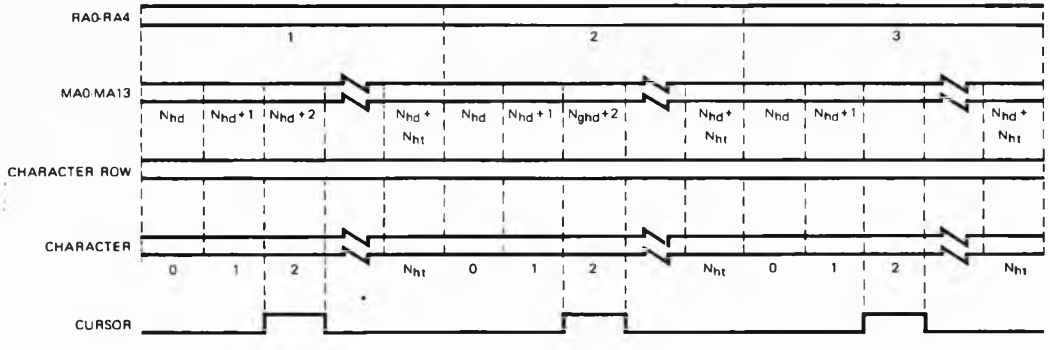


Figure 9. Cursor Timing

Notes: 1. Timing is shown for non-interlace and interlace modes.

2. Cursor Register = N_{hd} + 2.
3. Cursor start = 1.
4. Cursor end = 3.
5. R12/R13 = 0 for start address registers.

Example of Raster Scan Display

Fig. 10 shows an example where the same character is displayed in the non-interlace mode, interlace sync mode, and video mode.

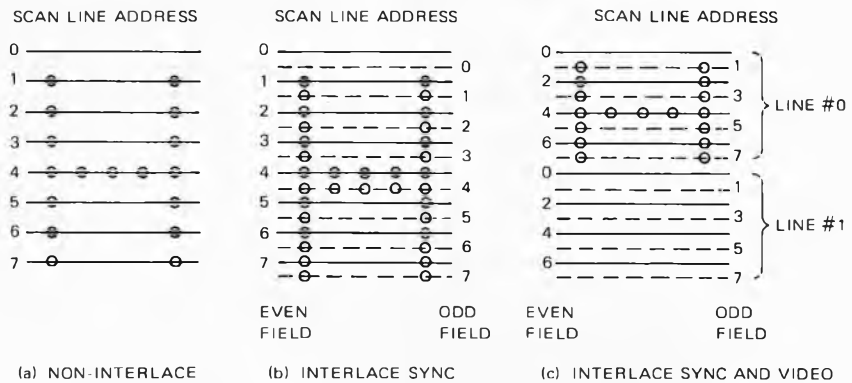


Figure 10. Interlace Control

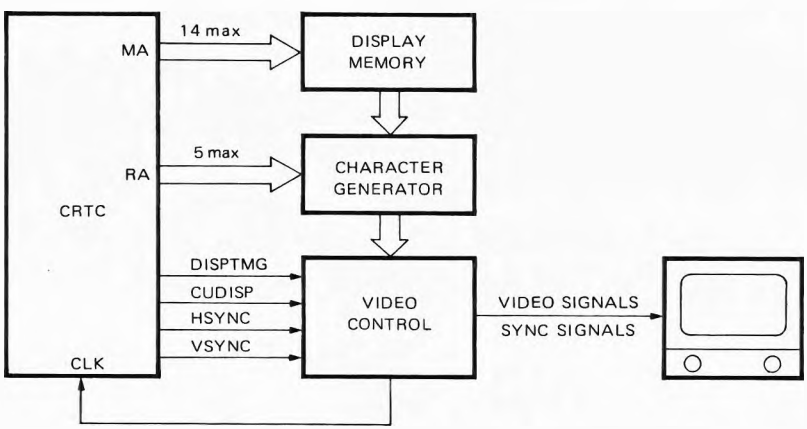


Figure 11. Interface to Display Control Unit

Fig. 11 shows the interface between the CRTC and the display control unit. The display control unit is mainly composed of Display Memory, Character Generator, and Video Control circuit. For display memory, 14 Memory Address lines (0-16383) are provided and for character generator, 5 Raster Address lines (0-31) are provided. For the video control circuit, DISPTMG signal is used to control the blank period of video signal. CUDISP signal is used as video signal to display the cursor on the CRT screen. Moreover, HSYNC and VSYNC signals are used as drive signals respectively for CRT horizontal and vertical deflection circuits.

Outputs from video control circuit (video signals and sync signals) are provided to CRT display unit to control the deflection and brightness of CRT, and thus characters displayed on the screen.

Circuitry Standards of Display Control Units

Fig. 12 shows a detailed schematic diagram of the display control unit. This diagram shows how to use CUDISP and DISPTMG signals. CUDISP and DISPTMG signals should be latched at least one time at external flip-flop F1 and F2, which creates a one-character delay time, so as to synchronize with the video signal from the parallel-serial converter. A high-speed D-type flip-flop as TTL is used for this purpose. After being delayed at F1 and F2, the DISPTMG signal is OR-ed with output from AND gate. By using this circuitry, blanking of horizontal and vertical retrace time is controlled and the cursor video is mixed with the character video signal.

Fig. 12 shows an example in which both display memory and CG can be accessed for horizontal one-character time. A time chart for this case is shown in Fig. 15 This method is used when a few characters need to be displayed horizontally on the screen.

When many characters are displayed horizontally on the screen and horizontal one-character time is so short that neither display memory nor CG can be accessed, the circuitry shown in Fig. 13 should be used. In this case, display memory output is latched and the CG is accessed at the next cycle. The time chart in this case is shown in Fig. 16 CUDISP and DISPTMG signals should be provided after being delayed by one-character time by using the skew bit of interface and the skew register (RS). Moreover, when there are troubles in the delay time of MA during horizontal one-character time on high speed display operation, the system shown in Fig. 14 should be adopted. The time chart in this case is shown in Fig. 17 Character video signal is delayed for a two-character time because each MA output and display memory outputs are latched and are made to be in phase with CUDISP and DISPTMG signals by delaying for a two-character time. Table 1 shows the circuitry selection standard of display units.

Table 1. Circuitry Standard of Display Control Unit

Case	Relation among t_{CH}, RM and CG	Timing Diagram	Interlace & Skew Register Bit Programming			
			C1	C0	D1	D0
1	$t_{CH} >$ RM Access + CG Access + t_{MAD}	Fig. 15	0	0	0	0
2	RM Access + CG Accwss + $t_{MAD} \geq t_{CH} >$ RM Access + t_{MAD}	Fig. 16	0	1	0	1
3	RM Access + $t_{MAD} \geq t_{CH} >$ RM Access	Fig. 17	1	0	1	0

t_{CH}: CHCP Period: t_{MAD}: MA Delay

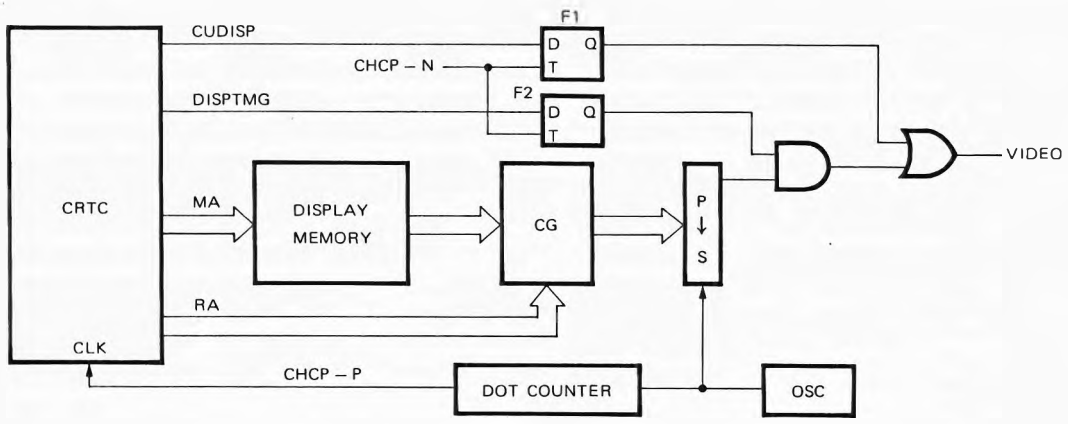


Figure 12. Display Control Unit (1)

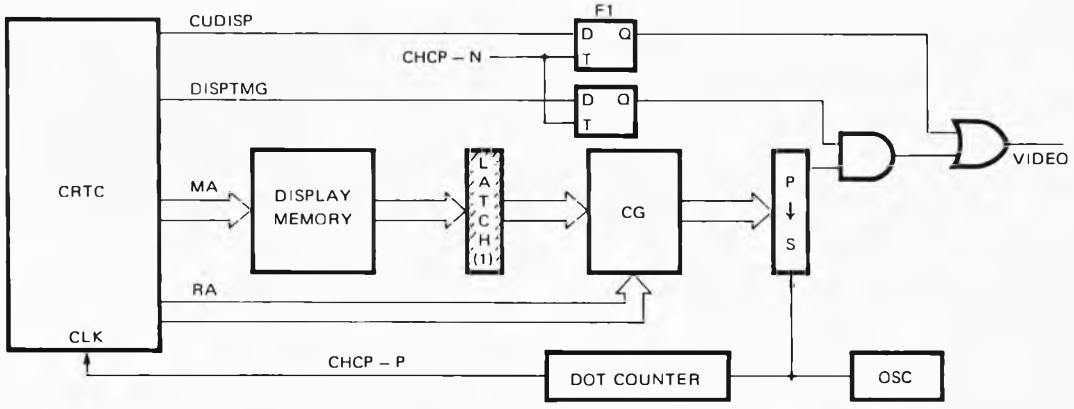


Figure 13. Display Control Unit (2)

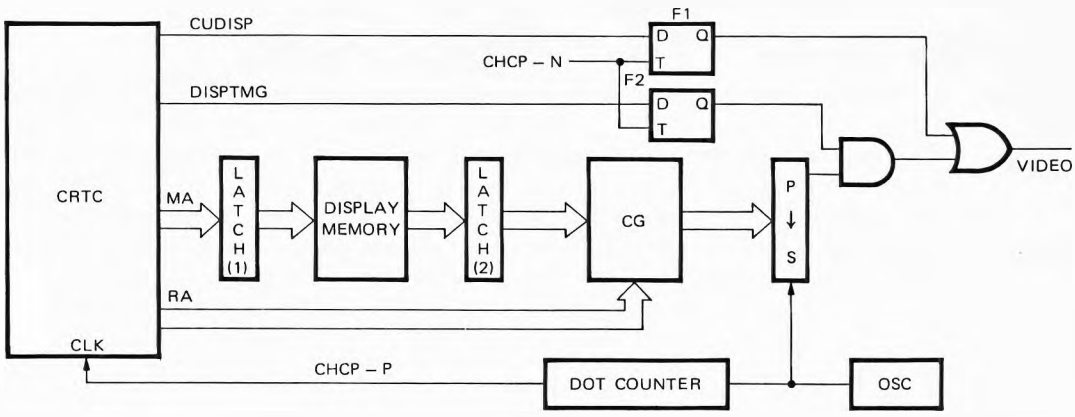


Figure 14. Display Control Unit (for high-speed display operation) (3)

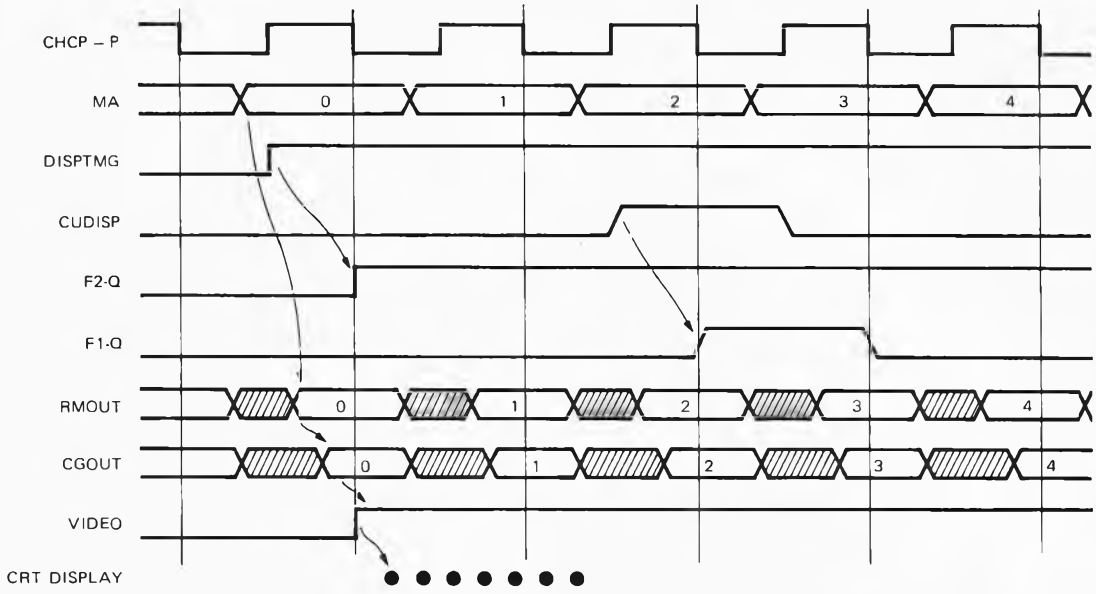


Figure 15. Time Chart of display Control Unit (1)

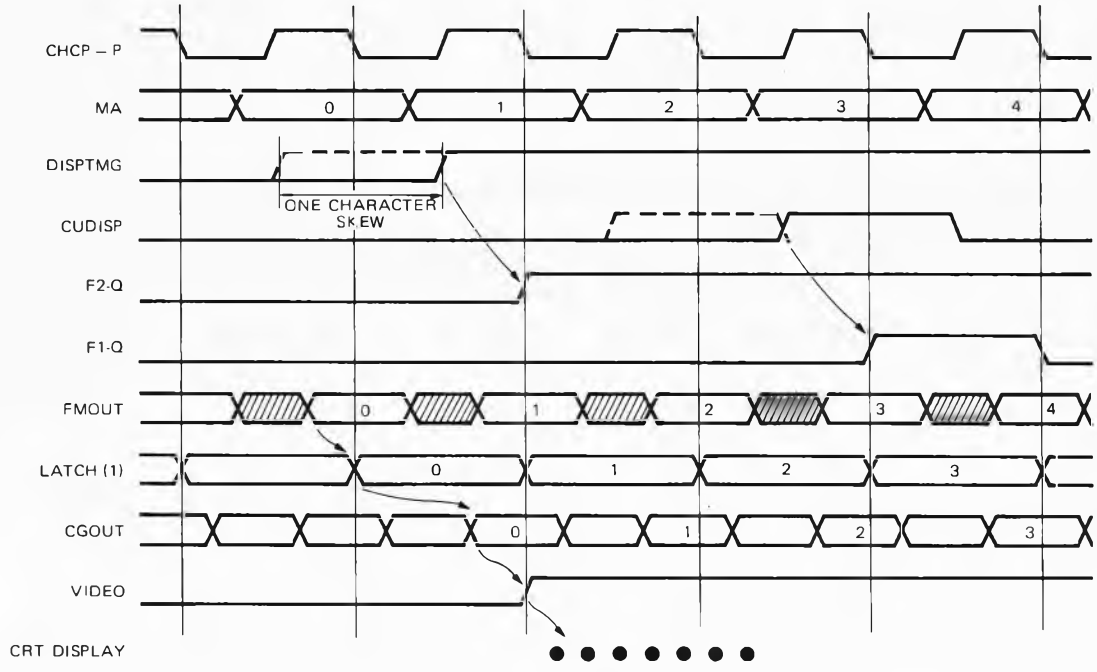


Figure 16. Time Chart of Display Control Unit (2)

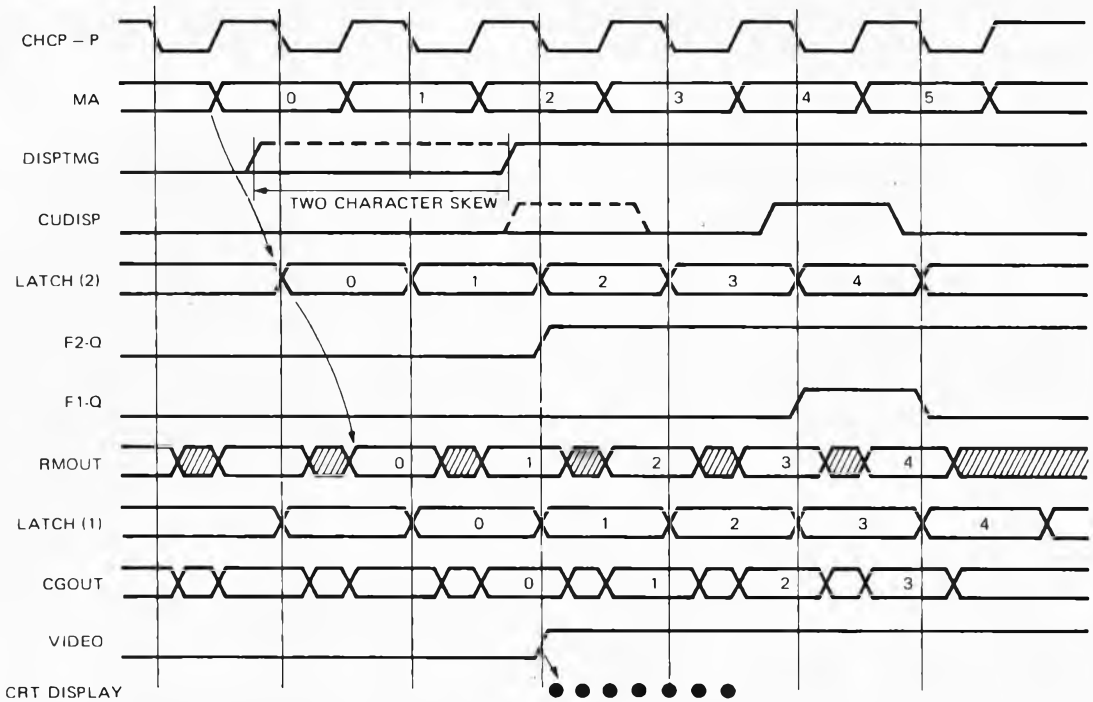


Figure 17. Time Chart of Display Unit (3)

How to Decide Parameters on the CRTC

Before the determination of parameters on the CRTC and the dot frequency of crystal, we must check the Specification of CRT Display Unit (Monitor) and the Screen Format. The output signal timing of CRTC, must be in the monitor specification for the normal display. (Such as DISPTMG, HSYNC, VSYNC.). Screen format includes:

(1) Horizontal display characters column number. (N_{hd})
(2) Vertical display row number. (N_{vd})
(3) Horizontal dot numbers per character. (Dot counter ($\div N\alpha$)).
(4) Vertical raster lines per row. ($N_r + 1$)

Example: for non-interlace mode one frame = 60Hz
then one raster line frequency
$= 60Hz \times [(N_{vt} + 1)(N_r + 1) + N_{adj}]$
CLK frequency of CRTC = raster line frequency $\times (N_{ht} + 1)$

dot frequency of crystal = $N\alpha \times$ CLK frequency of CRTC
$= 60Hz \times [(N_{vt} + 1)(N_r + 1) + N_{adj}] \times [N_{ht} + 1] \times N\alpha$

* Relation between R0-R7 is in Figure 18.

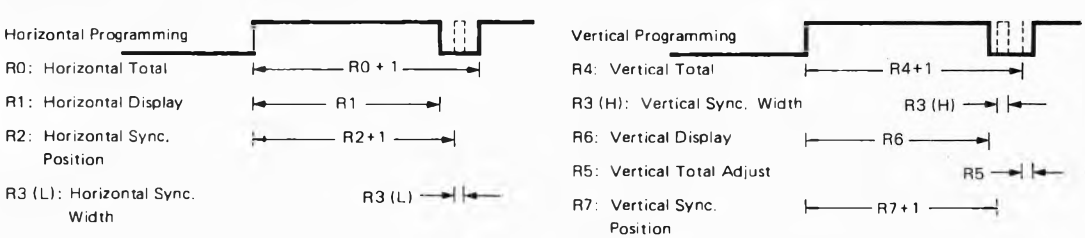


Figure 18.

Pin Description

Pin No.	Symbol	Name	Description
33, 32, 31, 30 29, 28, 27, 26	D0 – D7	Data Bus	Processor Interface
23	E	Enable	
25	$\overline{CS}$	Chip Select	
24	RS	Register Select	
22	R/$\overline{W}$	Read/Write	
40	VSYNC	Vertical Sync	CRT Control
39	HSYNC	Horizontal Sync	
18	DISPTMG	Display Enable	
4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17	MA0-MA13	Reading Memory Addresses	Reading Display Memory / Character Generator Addressing
38, 37, 36, 35, 34	RA0-RA4	Raster Addresses	
19	CUDISP	Cursor	Other Pins
21	CLK	Clock	
3	LPSTB	Light Pen Strobe	
20, 1	V_{CC} (+) V_{SS} (–)	Power	
2	$\overline{RES}$	Reset	

PROCESSOR INTERFACE

The CRTC interfaces to a processor bus on the bidirectional data bus (D0-D7) using $\overline{CS}$, RS, E, and R/$\overline{W}$ as control signals.

Data Bus (D0-D7)
The bidirectional data lines (D0-D7) allow data transfers between the CRTC internal register file and the processor. The data bus output drivers are 3-state buffers which remain in the high impedance state except when the processor performs a CRTC read operation.

Enable (E)
The Enable pin is a high impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the CRTC. This signal is usually derived from the processor clock and the high to low transition is the active edge.

Chip Select ($\overline{CS}$)
The $\overline{CS}$ line is a high impedance TTL/MOS compatible input which selects the CRTC, when low, to read or write the internal Register File. This signal should only be active when there is a valid stable address being decoded from the processor.

Register Select (RS)
The RS line is a high impedance TTL/MOS compatible input which selects either the Address Register (RS = "0") or one of the Data Registers (RS = "1") of the internal Register File.

Read/Write (R/$\overline{W}$)
The R/$\overline{W}$ line is a high impedance TTL/MOS compatible input which determines whether the internal Register File gets written or read. A write is active at low ("0").

CRT CONTROL

The CRTC provides Horizontal Sync (HS), Vertical Sync (VS), and Display Enable (DISPTMG) signals.

Vertical Sync (V SYNC)
The TTL compatible output is an active high signal which drives the monitor directly or is fed to Video Processing Logic for composite signal generation. This signal determines the vertical position of the displayed text.

Horizontal Sync (H SYNC)
This TTL compatible output is an active high signal which drives the monitor directly or is fed to Video Processing Logic for composite generation. This signal determines the horizontal position of the displayed text.

Display Enable (DISPTMG)
This TTL compatible output is an active high signal which indicates the CRTC is providing addressing in the active display area.

READING DISPLAY/CHARACTER GENERATOR ADDRESSING

The CRTC provides Memory Addresses (MA0-MA13) to scan the display RAM. Also provided are Raster Addresses (RA0-RA4) for the character ROM.

Reading Memory Addresses (MA0-MA13)
These 14 outputs are used to read the display memory.

Raster Addresses (RA0-RA4)
These 5 outputs from the internal Raster Counter address the character ROM for the row of a character.

OTHER PINS

Cursor (CUDISP)
This output signal indicates the cursor display signal sent to the video processing logic to display in the proper area.

Clock (CLK)
CLK, TTL/MOS compatible input is used to synchronize all CRT control signals. An external dot counter is used to derive this signal which is usually the character rate in an alphanumeric CRT. The active transition is high to low.

Light Pen Strobe (LPSTB)
This high impedance TTL/MOS compatible input latches the current display memory address in the register file. Latching is on the low to high edge and is synchronized internally to character clock.

V_{CC}, Gnd (V_{CC}, V_{SS}) Power Supply Pins.
Reset ($\overline{RES}$)
The $\overline{RES}$ input is used to reset the CRTC. An input low level on $\overline{RES}$ forces CRTC into the following status:

(a) All the counters in CRTC are cleared and the device stops the display operation.
(b) All the outputs go to low level.
(c) Control registers in CRTC remain unchanged.

This signal is different from other MC 6800 family in the following functions:

(a) $\overline{RES}$ signal has capability of reset function only when LPSTB is at low level.
(b) The CRTC starts the display operation immediately after the release of $\overline{RES}$ signal.

CRTC INTERNAL REGISTER ASSIGNMENT

Table 2. CRTC Internal Registers

$\overline{CS}$	RS	Address Register					Register #	Register File	Program Unit	Read	Write	Number of Bits							
		4	3	2	1	0						7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	–	–	–	–								
0	0	X	X	X	X	X	AR	Address Register	–	No	Yes								
0	1	0	0	0	0	0	R0	Horizontal Total *	Char.	No	Yes								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes								
0	1	0	0	0	1	0	R2	H. Sync Position*	Char.	No	Yes								
0	1	0	0	0	1	1	R3	Sync Width	V-Raster H-Char.	No	Yes	V1	V1	V1	V1	H	H	H	H
0	1	0	0	1	0	0	R4	Vertical Total *	Char. Row	No	Yes								
0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes								
0	1	0	0	1	1	0	R6	Vertical Displayed	Char. Row	No	Yes								
0	1	0	0	1	1	1	R7	V. Sync Position*	Char. Row	No	Yes								
0	1	0	1	0	0	0	R8	Interface Mode and Skew	–	No	Yes	C_1	C_0	D_1	D_0			I_1	I_0
0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes								
0	1	0	1	0	1	0	R10	Cursor Start Raster	Scan Line	No	Yes		B	P					
0	1	0	1	0	1	1	R11	Cursor End Raster	Scan Line	No	Yes								
0	1	0	1	1	0	0	R12	Start Address (H)	–	Yes	Yes	0	0						
0	1	0	1	1	0	1	R13	Start Address (L)	–	Yes	Yes								
0	1	0	1	1	1	0	R14	Cursor (H)	–	Yes	Yes	0	0						
0	1	0	1	1	1	1	R15	Cursor (L)	–	Yes	Yes								
0	1	1	0	0	0	0	R16	Light Pen (H)	–	Yes	No	0	0						
0	1	1	0	0	0	1	R17	Light Pen (L)	–	Yes	No								

Table 2. Shows The Register File In CRTC, The Registers Marked* (Written Value) = (Specified Value) – 1

REGISTER DESCRIPTION

Address Register (AR)

The Address Register is a 5-bit write-only register used as an "indirect" or "pointer" register. Its contents are the address of one of the other 18 registers in the file. When RS and $\overline{CS}$ are low, the Address Register itself is addressed. When RS is high, the register file is accessed. (see Table 2).

Horizontal Total Register (R0)

This 8 bit Register determines the horizontal frequency of H Sync output. It is the total of displayed plus non-displayed character time units minus one.

Horizontal Displayed Register (R1)

This 8 bit register determines the number of displayed characters per horizontal line.

Horizontal Sync Position Register (R2)

This 8 bit register determines the horizontal sync position on the horizontal line.

Sync Width Register (R3)

V	V	V	V	H	H	H	H

This 8 bit write-only register determines the width of the Vertical Sync (VS) pulse and the Horizontal Sync (HS) pulse.

The HS pulse width may be programmed from 1-to-15 character clock periods. The VS pulse width may be programmed from 1-to-16 Raster scan lines. (see Table 3).

Vertical Total Register (R4) and Vertical Total Adjust Register (R5)

The vertical frequency of VSYNC is determined by both R4 and R5. The calculated number of character line times is usually an integer plus a fraction to get exactly a 50 or 60 Hz vertical refresh rate. The integer number of Character line times minus one is programmed in the 7 bit write-only Vertical Total Register, the fraction is programmed in the 5 bit write-only Vertical Scan Adjust Register as a number of scan line times.

Vertical Displayed Register (R6)

This 7-bit write-only register specifies the number of displayed character rows on the CRT screen, and is programmed in character row times. Any number smaller than the contents of R4 may be programmed into R6.

Vertical Sync Position (R7)

This 7-bit write-only register controls the position of vertical sync with respect to the reference. It is programmed in character row times. Any number equal to or less than the vertical total (R4) may be used.

Interlace Mode and Skew Register (R8)

C_1	C_0	D_1	D_0			I_1	I_0

This is a register used to program raster scan mode and skew of CUDISP signals and DISPTMG signals. In the non-interlace mode, the rasters of even number field and odd number field are scan duplicated. In the interlace sync mode, the rasters of odd number field are scanned in the middle of even number fields. Thus, the same character pattern is displayed in both fields. In the interlace sync and video mode, the raster scan method is the same as the interlace sync mode, but it is controlled to display different character patterns in two fields. Skew function is used to delay the output timing of CUDISP and DISPTMG signals such that they are synchronized with serial video output signals. This is due to the time delay from display memory data to serial output character pattern. (see Table 4).

Table 3. Sync Width Register

VSW				Pulse Width Unit: H
2^7	2^6	2^5	2^4	
0	0	0	0	16H
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

H: Raster Period

HSW				Pulse Width Unit: CH
2^3	2^2	2^1	2^0	
0	0	0	0	Not Used
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

CH: Character Clock Period

Table 4. Interlace Mode and Skew Register

Interlace Mode (2^1, 2^0)	I_1	I_0	Raster Scan Mode
	0	0	Non-Interlace Mode
	1	0	Non-Interlace Mode
	0	1	Interlace Sync Mode
	1	1	Interlace Sync & Video Mode
Cursor Skew Bit (2^7, 2^6)	C_1	C_0	CUDISP Signal
	0	0	Non-Skew
	0	1	One-Character Skew
	1	0	Two-Character Skew
	1	1	Non-Output
DISPTMG Skew Bit (2^5, 2^4)	D_1	D_0	DISPTMG Signal
	0	0	Non-Skew
	0	1	One-Character Skew
	1	0	Two-Character Skew
	1	1	Non-Ouptut

Maximum Raster Address Register (R9)

This is a register used to program maximum raster addresses within 5-bits. This register defines total number of rasters per character including space. This register is programmed as follows.

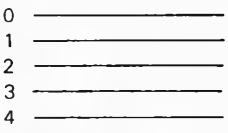
For Non-interlace Mode, Interlace Sync Mode

When total number of rasters is RN, (RN-1) shall be programmed.

For Interlace Sync & Video Mode

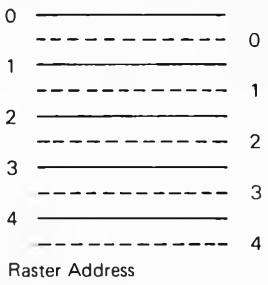
When total number of rasters is RN, (RN-2) shall be programmed.

Non-Interlace Mode



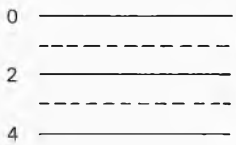
Total Number of Rasters 5
Programmed Value $N_r = 4$
(The same as displayed total number of rasters)

Interlace Sync Mode



Total Number of Rasters 5
Programmed Value $N_r = 4$
(In the interlace sync mode, total number of rasters in both the even and odd fields is ten. On programming, half of it is defined as total number of rasters).

Interlace Sync & Video Mode



Total Number of Rasters 5
Programmed Value $N_r = 3$
(Total number of rasters is displayed in the even field and the odd field)

Cursor Start Raster Register (R10)

This is a register used to program the cursor start raster address by lower 5-bits (2^0-2^4) and the cursor display mode higher 2-bits (2^5, 2^6). (see Table 5).

Table 5. Cursor Display Mode

Cursor Display Mode	B	P	Cursor Display Mode
(2^6, 2^5)	0	0	Non-blink
	0	1	Cursor Non-display
	1	0	Blink, 16 Field Period
	1	1	Blink, 32 Field Period

Cursor End Raster Register (R11)
This is a register used to program to cursor end raster address.

Start Address Register (R12, R13)
These are used to program the first address of refresh memory to read out. Paging and Scrolling is easily performed using this register. This register can be read but the higher 2-bits (2^6, 2^7) of R12 are always '0 ".

Cursor Register (R14, R15)
These two read/write registers store the cursor location. The higher 2-bits (2^6, 2^7) of R14 are always "0".

Light Pen Register (R16, R17)
These read-only registers are used to catch the detection address of the light pen. The higher 2-bits (2^6, 2^7) of R16 are always "0". Its value needs to be corrected by software because there is time delay from the address output of the CRTC to the signal input LPSTB pin of the CRTC. In the process raster is lit after the address output and the light pen detects it.

CRTC Register Comparison Table

NON-INTERLACE

Register	UM6845R/RA/RB MC6845 MC6845*1	MC6845R HD6845R	UM6845/A/B HD6845S	UM6845E/EA/EB
R0 Htotal	Total-1	Total-1	Total-1	Total-1
R1 Hdisp	Actual	Actual	Actual	Actual
R2 Hsync	Actual	Actual	Actual	Actual
R3 Sync Width	Horizontal (& Vertical *1)	Horizontal	Horizontal & Vertical	Horizontal & Vertical
R4 Vtotal	Total-1	Total-1	Total-1	Total-1
R5 Vtotal Adjustment	Any Value	Any Value	Any Value	Any Value
R6 Vdisp	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1
R8 B0-B1	Interlace	Interlace	Interlace	Interlace
Mode Select B2	–	–	–	Row/Column or Binary Addr.
B3	–	–	–	Shared or Transparent Addr.
B4	(Display Enable Skew *1)	–	Display Enable Skew	Display Enable Skew
B5	(Display Enable Skew *1)	–	Display Enable Skew	Cursor Skew
B6	(Cursor Skew *1)	–	Cursor Skew	RA4/
B7	(Cursor Skew *1)	–	Cursor Skew	Transparent
R9 Scan Lines	Total-1	Total-1	Total-1	Total-1
R10 Cursor Start	Actual	Actual	Actual	Actual
R11 Cursor End	Actual	Actual	Actual	Actual
R12/R13 Display Addr.	Write Only Read/Write (MC6845 & *1)	Read/Write	Read/Write	Write Only
R14/R15 Cursor Position	Read/Write	Read/Write	Read/Write	Read/Write
R16/R17 Position	Read Only	Read Only	Read Only	Read Only
R18/R19 Update Addr. Register	N/A	N/A	N/A	Transparent Mode Only
R31 Dummy Register	N/A	N/A	N/A	Transparent Mode Only
Status Register	Yes (UM6845R)	No	No	Yes

CRTC Register Comparison Table (Continued)

INTERLACE SYNC

Register	UM6845R/RA/RB MC6845 MC6845*1	MC6845R HD6845R	UM6845/A/B HD6845S	UM6845E/EA/EB
R0 Htotal	Total-1 = Odd or Even	Total-1 = Odd	Total-1 = Odd	Total-1 = Odd or Even

INTERLACE SYNC AND VIDEO

R4 Vtotal	Total-1	Total-1	Total-1	Total-1
R6 Vdisp	Total	Total/2	Total	Total
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1
R9 Scan Lines	Total-1 Odd/Even	Total-1 Only Even	Total-1 Odd/Even	Total-1 Odd/Even
R10 Cursor Start	Odd/Even	Both Odd	Odd/Even	Odd/Even
R11 Cursor End	Odd/Even	Both Even	Odd/Even	Odd/Even
Cclk	2.5 MHz	2.5 MHz	3.7 MHz	3.7 MHz

Ordering Information

Part Number	CPU Clock Rate	Package
UM6845	1MHz	40L DIP
UM6845A	1.5MHz	40L DIP
UM6845B	2MHz	40L DIP