Reducing CRT display overheads in Z80 systems using refresh-mode transfer

A method of greatly reducing the overhead for display maintenance with Z80-based VDUs is outlined. **Thomas Alexander and M V Subramanyam** use a special feature of this microprocessor to reduce processor workload from a normal 15-25% to less than 5%.

CRT displays Z80 refresh-based transfer

A CRT screen needs to be refreshed once every frame, 50 or 60 times a second. This involves the transfer, per frame, of up to 2 kbytes of data, and hence can use a lot of available CPU time. LSI display controllers using DMA transfer can reduce this overhead to reasonably low levels, but will still need 15–25% of bus time.

Usually, one of three methods is used to fill the CRT controller row buffers from memory

- shared memory, for instance in the 6847 controller
- DMA transfer using a DMA controller
- processor-controlled (software) DMA transfer

The first two require considerable hardware; the latter entails memory space and processing time.

Z80 REFRESH MECHANISM

This microprocessor is unique in that it directly supports dynamic RAM refresh. An internal 7-bit counter (the R register) emits a refresh address during the T_3 state of an opcode fetch machine cycle. The counter is incremented automatically and its contents are placed on A_0–A_6 of the address bus (see Figure 1). A control signal, $\overline{RFSH}$, indicates when an $\overline{RAS}$-only refresh can be carried out. During this period, the data bus is tristate, all other control lines inactive (high) and the interrupt register (I register) contents appear on A_8–A_{15}. (A_7 reflects the 8th bit of the R register, and can be set or reset by program control.)

Hence in every 128 successive opcode fetch cycles 128 consecutive 16-bit addresses (produced by concatenating the I and R registers) are emitted by the Z80, along with the $\overline{RFSH}$ signal.

CRT DISPLAY REQUIREMENTS

An 80 x 24 character display, with a 6 x 10 matrix for each character, needs 80 bytes to be supplied to the CRT controller every 600 μs (10 horizontal retrace periods of 60 μs each). Hence one byte should be transferred every 7 μs, on the average.

OPERATING PRINCIPLES

The basic idea is to use the 16-bit refresh address supplied by the CPU during T_4 to load the row buffers of a CRT controller (here, an 8275) from display memory. Between successive refresh periods, the refresh address will be automatically incremented; hence successive display characters are loaded into the buffers. Since the interval between successive T_3 states never exceeds 7 μs (worst case: 6 μs) the display will always be maintained. In addition, as the instruction decode does not require the system bus, the transfer is entirely transparent to the CPU. The only remaining work load is the reinitialization of the refresh counter and interrupt register at the start of each character line, once every 600 μs.

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HARDWARE DESCRIPTION

The extra hardware performs the following.

- An interrupt is generated at the leading edge of the 8275 DMA request signal, issued at the start of each character line.
- The refresh address emitted is allowed to access the display RAM, causing data to appear on the bus soon after $\overline{RFSH}$ is asserted low.
- Data is strobed into the 8275 buffer using its $\overline{DACK}$ (DMA grant acknowledge) and $\overline{WR}$ lines.
- When DREQ of the 8275 goes low again (80 bytes transferred), the transfer logic is reset.

The realization of the above is fairly straightforward. The implementation required five TTL chips, all 74-series SSI gates, flipflops and monostables.

Since the display RAM (two 6116's) should be accessible to both the Z80 and the 8275, the $\overline{RD}$ for the chips is obtained as an OR or the CPU $\overline{RD}$ line and the 8275 DACK

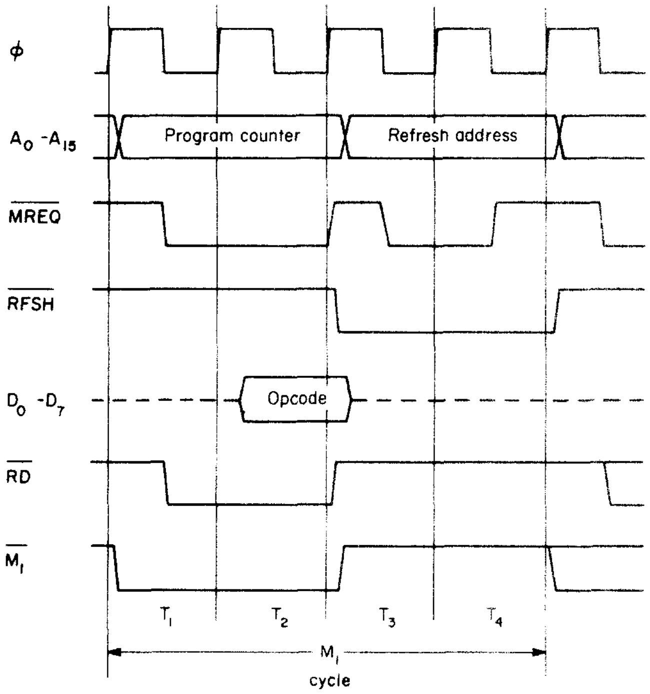

Figure 1. Z80 opcode fetch machine cycle