A low cost video display unit

Here is a new design for a low cost video display unit, capable of displaying data from a microcomputer on a standard TV receiver or monitor. It displays 16 lines of 32 characters and offers both flashing cursor and a destructive backspace facility. All timing is derived from a crystal oscillator, and no setting up is required.

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This Video Display Unit (VDU) was designed primarily for the microprocessor system user, who requires a video terminal of minimum complexity to enable him to communicate with his system. Therefore many of the unnecessary features of commercial style VDU's were abandoned in order to provide a cheap but effective video terminal for such applications.

Sixteen lines of 32 characters was selected as the screen format which allows for adequate display of program steps. With continuous roll-up facility, the user can see at least his last 16 lines of information. The cursor, indicating the position of the next character is fixed permanently on the bottom line (line 16). Carriage return and line feed (non-print characters) are decoded and these are normally all that would be required for a basic unit. However, a back space control function has been included mainly for the benefit of those who might use such a unit as a TV typewriter. This control allows editing of the bottom line before a line feed is given. Back space actually types a space in the location of the cursor after moving it back one character position.

The VDU uses all standard readily available TTL IC chips, except for six CMOS memory chips and the character generator chip.

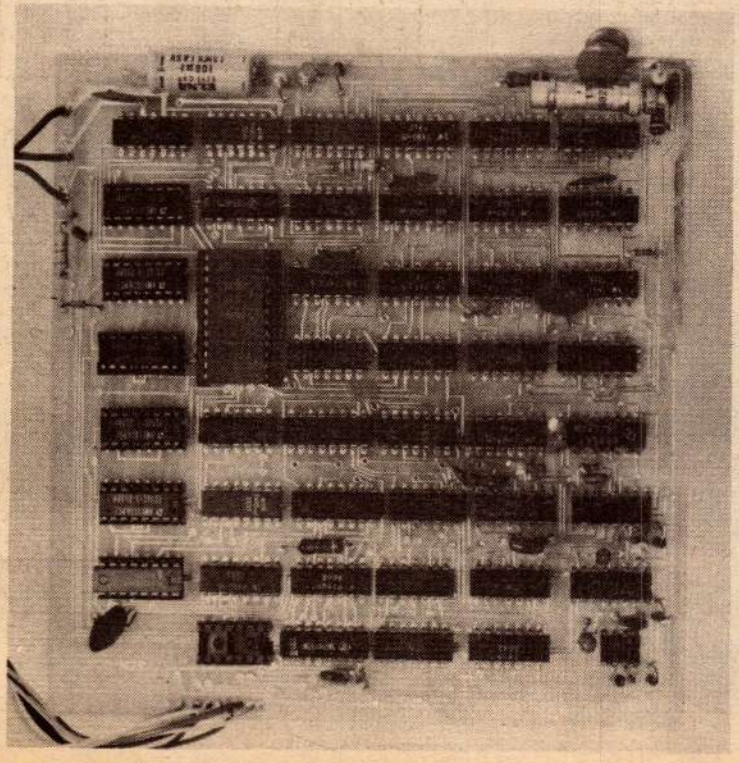
The method of actually displaying a character on a TV screen will not be described in detail here, as reference to the issue of EA for January 1977 should make this clear. The VDU described here uses the same character generator IC described in the earlier article (i.e., the 2513), and hence allows for the display of the full 64-character subset of ASCII known as "6-bit ASCII". This is the same character set displayed on most teleprinters.

A 4.7MHz crystal oscillator provides all of the clock pulses for the VDU. As can be seen from the block and circuit diagrams, this base frequency is divided down to produce the horizontal and vertical sync pulses required by the TV set. The 4.7MHz signal is also used to clock the output shift register used to convert the parallel "row data" from the character generator into the serial data required as video information by the TV display.

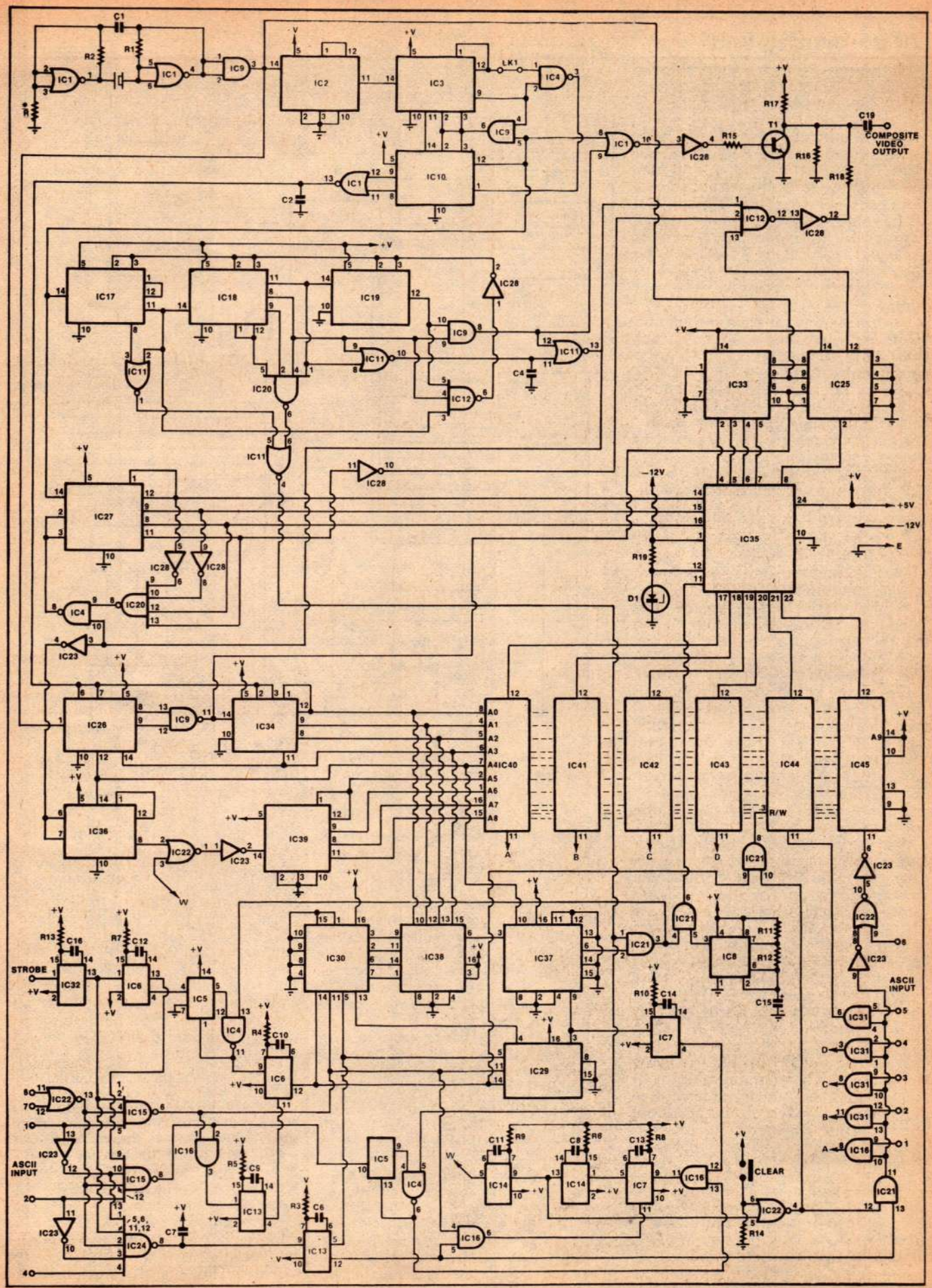
Incidentally it has been found that a 4.43MHz crystal of the type used in the subcarrier oscillator of colour TV receivers may be used instead of the nominal 4.7MHz crystal. This can be worthwhile, as the 4.43MHz crystal is generally cheaper and easier to obtain. Naturally when the lower frequency

SPECIFICATION

VDU displays the 6-bit ASCII character set, in 16 lines of 32 characters. All timing derived from a crystal-locked oscillator; no setting up required. Continuous line scrolling of display. Maximum input data rate 50 characters/sec. Destructive back space facility for editing. Flashing cursor indicates next character position. Uses standard TTL ICs for low cost.



At left is the assembled PC board. Note that the version shown here uses a 100pF capacitor paralleled by a 30pF trimmer in place of the crystal.


C1
R1
R2
IC1
IC9
IC2
IC3
LK1
IC4
IC10
C2
IC1
IC1
IC28
R17
T1
C19
COMPOSITE VIDEO OUTPUT
R15
R16
R18
IC12
IC28
IC17
IC18
IC19
IC28
IC9
IC11
IC11
IC20
IC12
C4
IC33
IC25
IC11
IC28
IC27
IC28
IC28
IC4
IC20
IC23
−12V
+5V
−12V
E
IC35
R19
D1
IC26
IC9
IC34
IC36
IC22
IC23
IC39
W
A0
A1
A2
A3
A4IC40
A5
A6
A7
A8
IC41
IC42
IC43
IC44
IC45
R/W
A9
A
B
C
D
IC21
IC23
IC22
IC23
ASCII INPUT
IC30
IC38
IC37
IC21
IC8
R11
R12
C15
R13
C16
R7
C12
STROBE
IC32
IC6
IC5
IC4
R4
C10
R10
C14
IC7
IC29
IC31
IC31
IC31
IC31
IC16
IC22
IC15
IC23
ASCII INPUT
IC15
IC24
IC16
IC13
R5
C9
IC5
IC4
C11
R9
C8
R6
C13
R8
IC14
IC14
IC7
IC16
W
CLEAR
IC22
R14
IC21
IC16
C7
R3
C6
IC13

Video display unit

crystal is used, both of the TV sync pulse frequencies are lower also, but most TV sets seem to be able to lock onto them quite easily. As the vertical frequency becomes 45.5Hz instead of 50Hz, some sets may produce a small amount of horizontal wavering or "snaking", particularly if there is some 50Hz ripple getting into the vertical oscillator from the receiver's power supply.

If such an effect is experienced and found annoying, then a 100pF capacitor with a 30pF trimmer in parallel may be substituted for the crystal if a 4.7MHz crystal is not available. The trimmer capacitor can be varied until the TV set locks onto the VDU sync pulses. Further trimming may be required to obtain a steady display.

Note that if this capacitor is used, a 220 ohm resistor is required as an addition between pins 2 and 3 (joined together) on IC1 and ground. This is indicated on the circuit diagram as R* and can be soldered onto the board, vertically, from the appropriate side of R2 and the outer ground line.

A further chain of frequency dividers generates the line address information for the character generator and the load pulses for the shift register. One load pulse occurs for every six clock pulses given to the shift register, thus loading it with the required five bits of data for a character row and also giving a single "dot" space between characters. Since this load pulse occurs for each character across the screen (i.e. 32 times for each horizontal TV scan) it becomes the ideal clock pulse for the memory address.

Nine address lines are required to address the memory, which holds each character to be displayed on the screen in its ASCII code. The memory is re-addressed each frame and therefore a character remains in its particular location in memory until changed by an external control signal. The memory consists of six 2102, 1k x 1 RAMS, six being required to hold the six bit ASCII code. This provides 1024 6 bit words, but only 512 are used.

The outputs of the memories are connected directly to the character generator. The memories are normally held in the read mode and each time the address changes, the outputs from the memories change to provide a six bit ASCII code for the character generator.

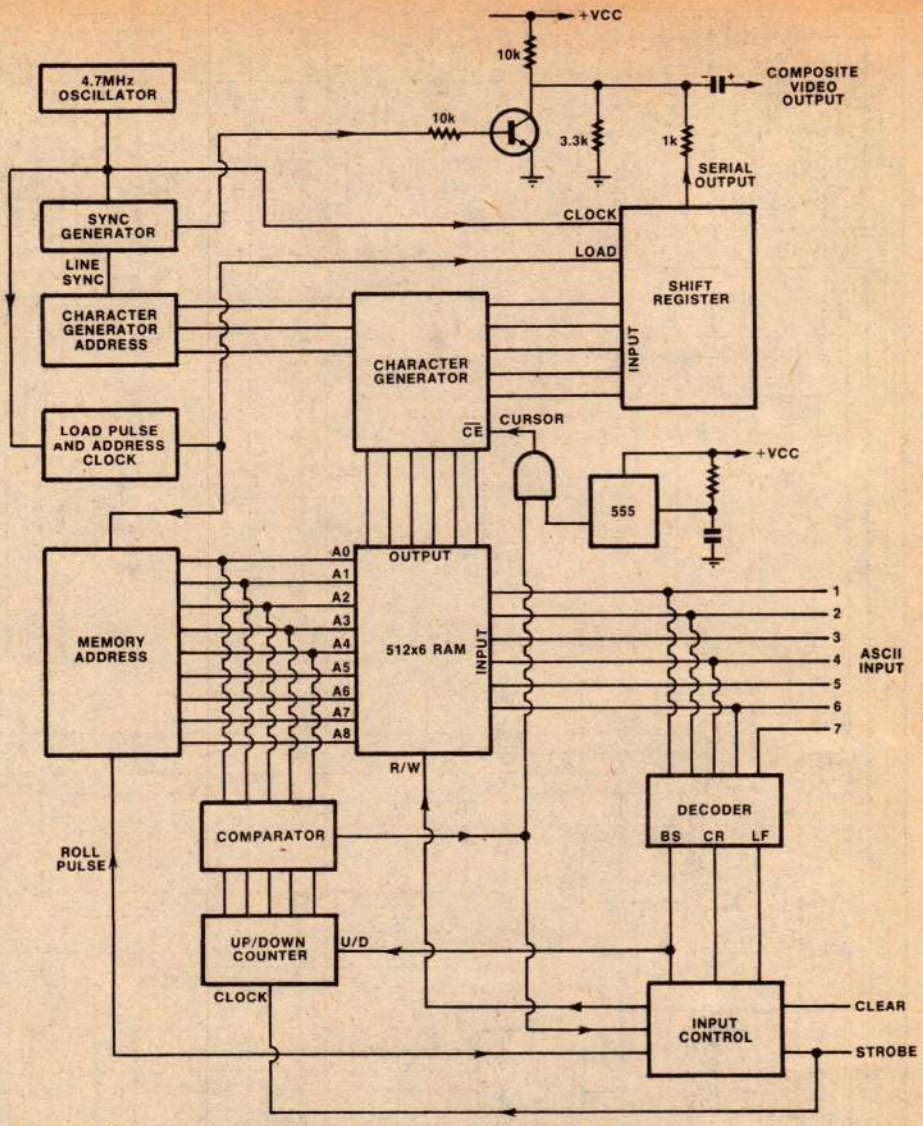
As just mentioned, an external control signal is required to change data held in memory. To do this we must have a written command, together with an indication as to where in memory its contents are going to change. Memory location indication is achieved by comparators and a set of counters that duplicates the memory address. This extra set of counters are advanced one count by the input strobe pulse, which indicates that a new character is being entered either from a keyboard or a computer. The comparator gives an output when the memory address equals the count on the duplicated set of counters, and this output is used to gate the ASCII input into the correct location in memory.

Because of this gating technique, a character can only be written into memory every frame, which immediately indicates a baud rate limitation of 500 baud. Since this VDU was designed for microprocessors, this modest baud rate should not be a problem as the VDU will operate at the 110, 150 or 300 baud rates used by most debug ROMS in microcomputers.

If the output of the comparators is fed to the CE-bar input on the character generator chip, it disables the chip for that particular location, and therefore a single bar is generated on the screen. This occurs instead of generating a character and therefore a cursor appears. Since the cursor appears permanently on the 16th line, only five of the nine address lines need to be compared, thus controlling the 32 positions along the line. The blinking effect of the cursor is achieved by gating the control signal with a low frequency astable multivibrator; a 555 timer has been used for this purpose.

At this point it should be clear that we now have a "page" of information displayed on the screen with a cursor indicating the next character position. Let's now take a look at how the scrolling of lines is achieved.

The memory address counters can be divided into two parts. The first five address lines control the 32 characters across each of the 16 lines, while the 16 lines themselves are controlled by the last four address lines. If at any time an extra clock pulse is given to this last address counter it would add an extra count and thus change the character line position as they appear on the screen. If the pulse is applied to this counter during the time that there is no



Above shows the block diagram, while at right is the component overlay pattern.

PARTS LIST

INTEGRATED CIRCUITS

IC1 7402	IC16 7408	IC31 7408
IC2 7493	IC17 7493	IC32 74123
IC3 7493	IC18 7493	IC33 7495
IC4 7400	IC19 7493	IC34 7493
IC5 7474	IC20 7420	IC35 2513
IC6 74123	IC21 7408	IC36 7492
IC7 74123	IC22 7402	IC37 7485
IC8 555	IC23 7404	IC38 7485
IC9 7408	IC24 7430	IC39 7493
IC10 7493	IC25 7495	IC40 2102
IC11 7402	IC26 7492	IC41 2102
IC12 7410	IC27 7493	IC42 2102
IC13 74123	IC28 7404	IC43 2102
IC14 74123	IC29 74191	IC44 2102
IC15 7420	IC30 74191	IC45 2102

RESISTORS

R1 470 ohms	R11 10k
R2 470 ohms	R12 120k
R3 22k	R13 10k
R4 6.8k	R14 470 ohms
R5 22k	R15 10k
R6 6.8k	R16 3.3k
R7 6.8k	R17 10k
R8 39k	R18 1k
R9 22k	R19 680 ohms
R10 6.8k	R* 220 ohms

CAPACITORS

C1 .01uF	C12 330pF
C2 330pF	C13 .33uF tant.
C3 .1uF	C14 .022uF
C4 330pF	C15 4.7uF tant.
C5 .1uF	C16 .027uF
C6 3.3uF tant.	C17 .1uF
C7 .001uF	C18 .1uF
C8 .022uF	C19 47uF 25V electro.
C9 3.3uF tant.	C20 .1uF
C10 22pF	C21 .1uF
C11 .082uF	

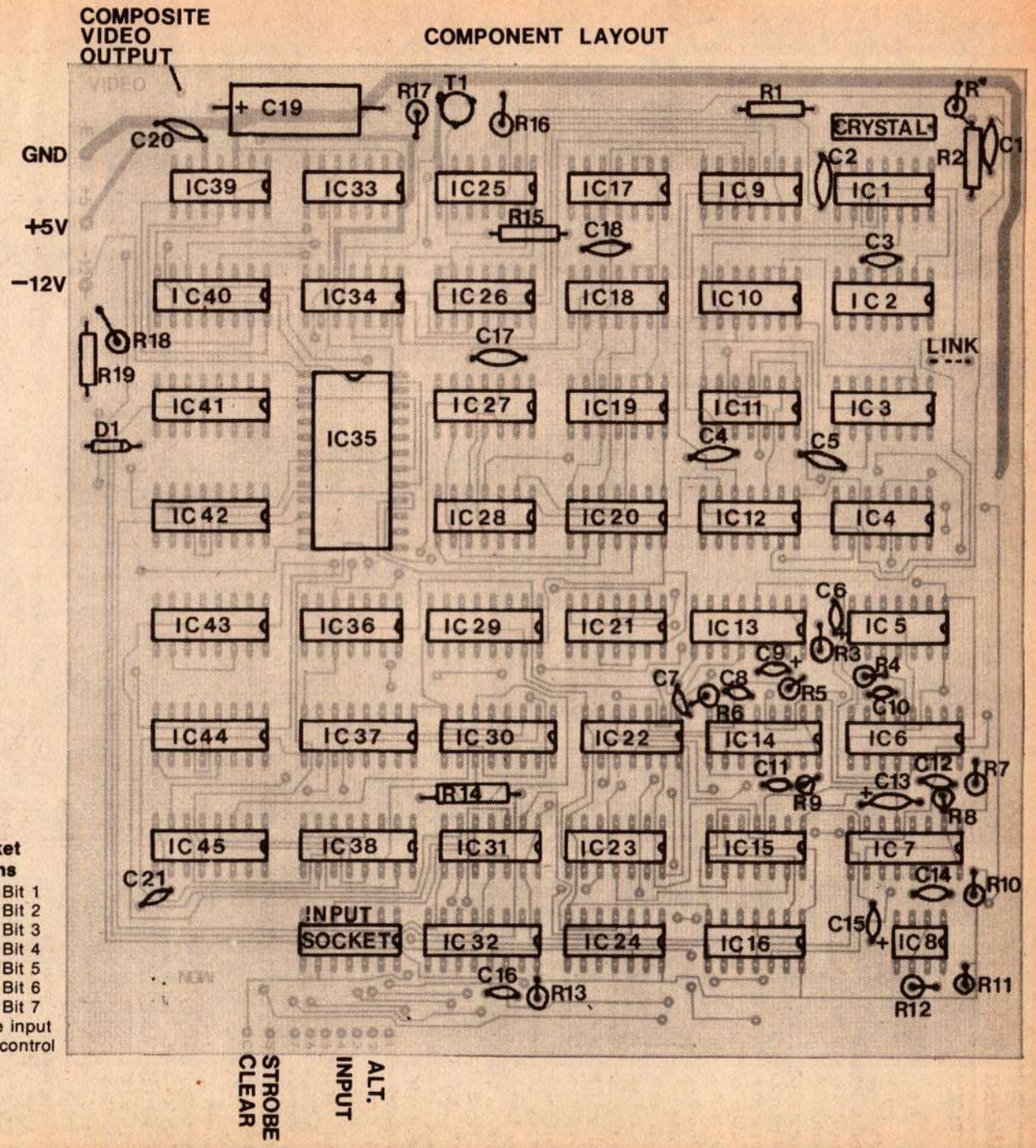
CRYSTAL 4.7MHz
or 100pF capacitor and 30pF trimmer

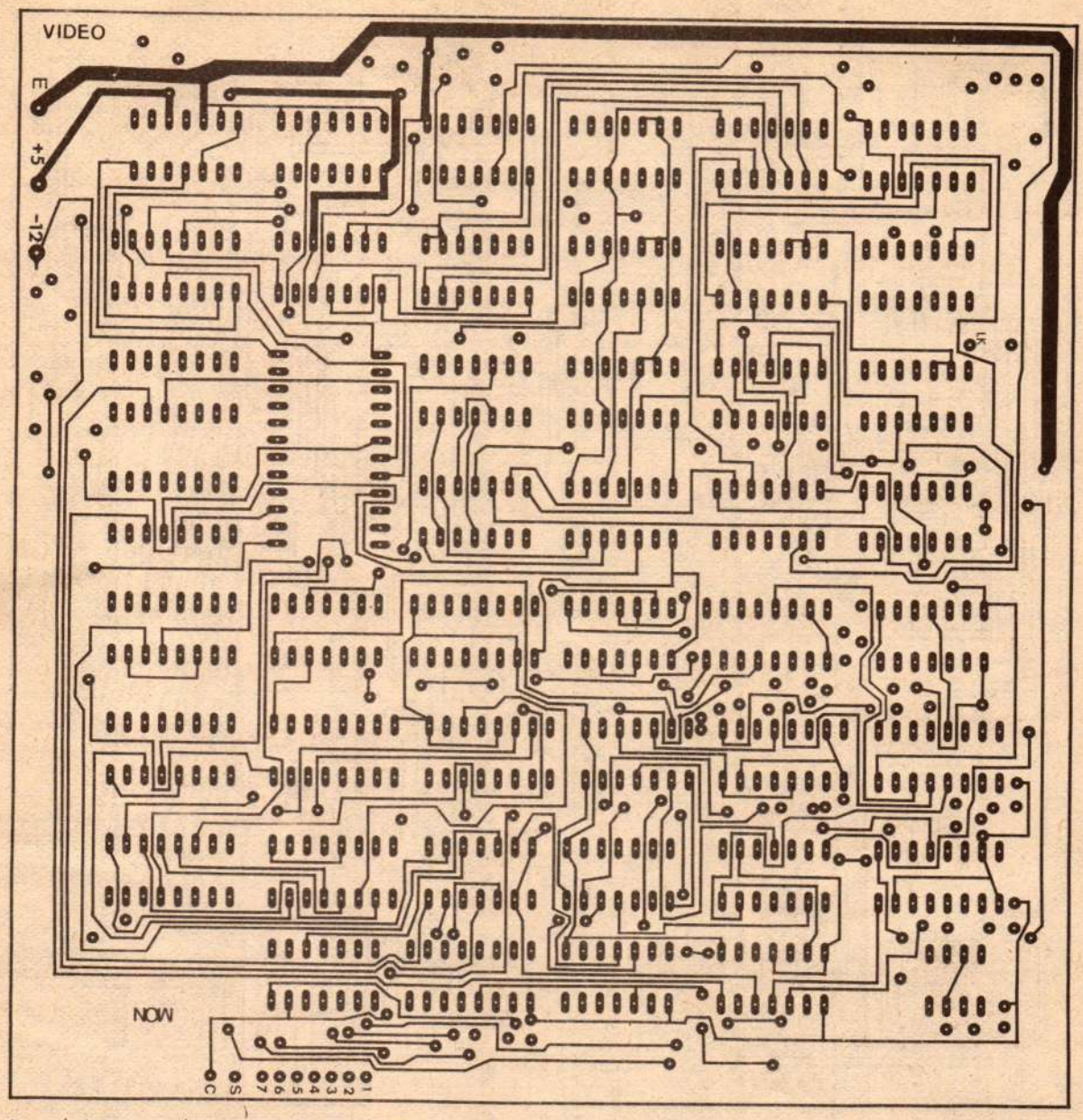
D1 BZX79C5V1

T1 BC109

Input Socket Connections

Pin 1 ASCII Bit 1
Pin 2 ASCII Bit 2
Pin 3 ASCII Bit 3
Pin 4 ASCII Bit 4
Pin 5 ASCII Bit 5
Pin 6 ASCII Bit 6
Pin 7 ASCII Bit 7
Pin 8 Strobe input
Pin 9 Clear control





Actual size reproduction of the PC pattern on the component side of the board.

display on the screen (i.e. the time between frames) then the next time a frame appears on the screen it will start at one extra character line due to this extra count. This extra clock pulse is generated at the end of a line, or when line feed is detected, and gives the scrolling effect.

When roll-up does occur another pulse is also generated which applies the ASCII code for a space to the memories and a write command is given at the same time. This immediately gives a clear line on line 16, to type onto after the previous line is rolled up.

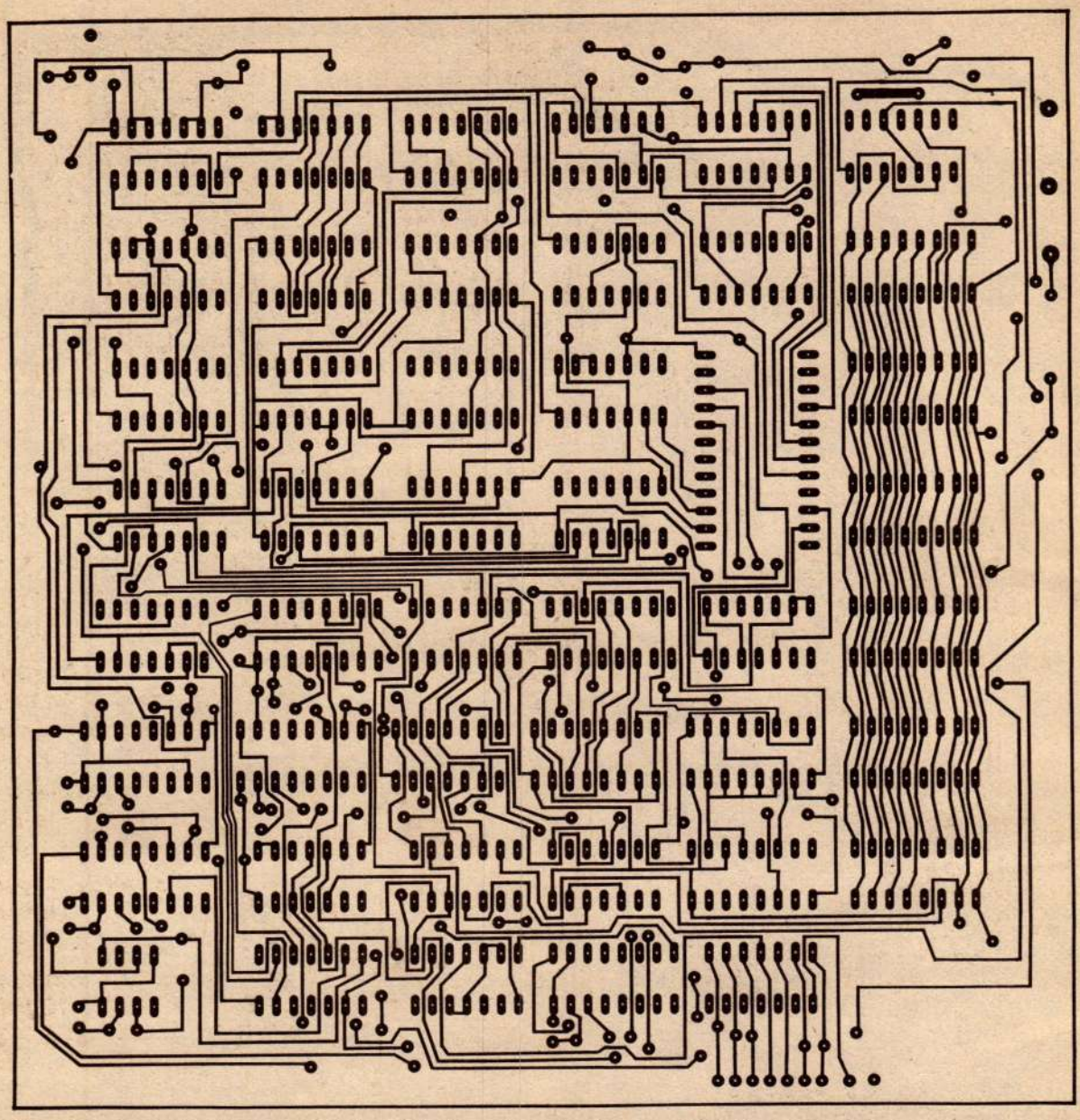
A decoder is used to detect when carriage return, line feed or back space information is given to the VDU. The control bit in the ASCII code — bit 7, is used for this purpose.

The video information from the shift register is fed to the output of transistor T1 via a 1k resistor, and is mixed with the inverted sync pulses which are applied to the base of the transistor. The 10k and 3.3k resistors provide the correct 1:3 ratio for sync and video information. This composite video is then output via an isolating capacitor and is suitable for applying to any video amplifier employed in standard TV sets.

Experience has shown that the video output from the VDU is suitable for applying to the grid or the base (depending on whether valve or solid state) of the video driver in a TV set without any alteration or disconnection of any components.

When checking for this input, one should ensure that the take-off for the sync separator is after this stage of amplification in the TV receiver.

There is absolutely no setting up required with the VDU. Random characters should appear on the TV screen as soon as power is switched on. To enable a clear screen when first turned on, a clear input has been provided on the PC board. It requires a switch to the +5V rail, or a logic "1" applied to it. This can be obtained from an unused key on the terminal's keyboard, giving manual clearing, or alternatively by means of a capacitor to



The PC pattern for the reverse side of the board, again shown actual size.

the +5V supply rail, to give automatic clearing on power-up. A 47uF tantalum should work.

A link, LK, has been provided on the PC board to provide an option regarding horizontal positioning of the VDU display. With the link out, the video information is generated in the centre of the period between horizontal sync pulses, giving a display which should be centred on most TV sets. If, however, it is found that the display is not in the centre of your TV screen, this link can be inserted and the whole picture will be shifted about three character widths to the right of the screen.

The printed circuit board for the VDU measures 155 x 160 mm and has an input socket facility where the required input data lines can be entered via a 14 pin DIP connector, using flat ribbon cable. This makes for a very neat connection. However, for those wishing to keep costs down, the same inputs are available at the edge of the PC board where wires can be soldered directly to the copper. The strobe input is triggered by a negative edge; if this is not available, an inverter on this line would be required.

Power supply requirements are +5 Volts at 1.2 Amps and -12 Volts at around 40mA. The higher +5V supply current is required because of the TTL chips used. Three terminal regulators rated for 1.5 Amps are adequate for this voltage supply.

A UART has not been included on the PC board because the VDU was considered to be a separate self-contained control system which accepts parallel data only, and if serial data is required by a microcomputer system then an external device such as a UART should be added. Parallel data is also acceptable to some microprocessors and makes for easier programming.

Editor's Note: For those who do wish to add serial interfacing and a keyboard, to produce a complete self-contained terminal, we hope to supply the necessary information shortly.